Optical, Wireless, and Optical Wireless Communication for a Brave New World

光、无线、及光无线通信，共创美好新世界

C. Patrick Yue 俞捷

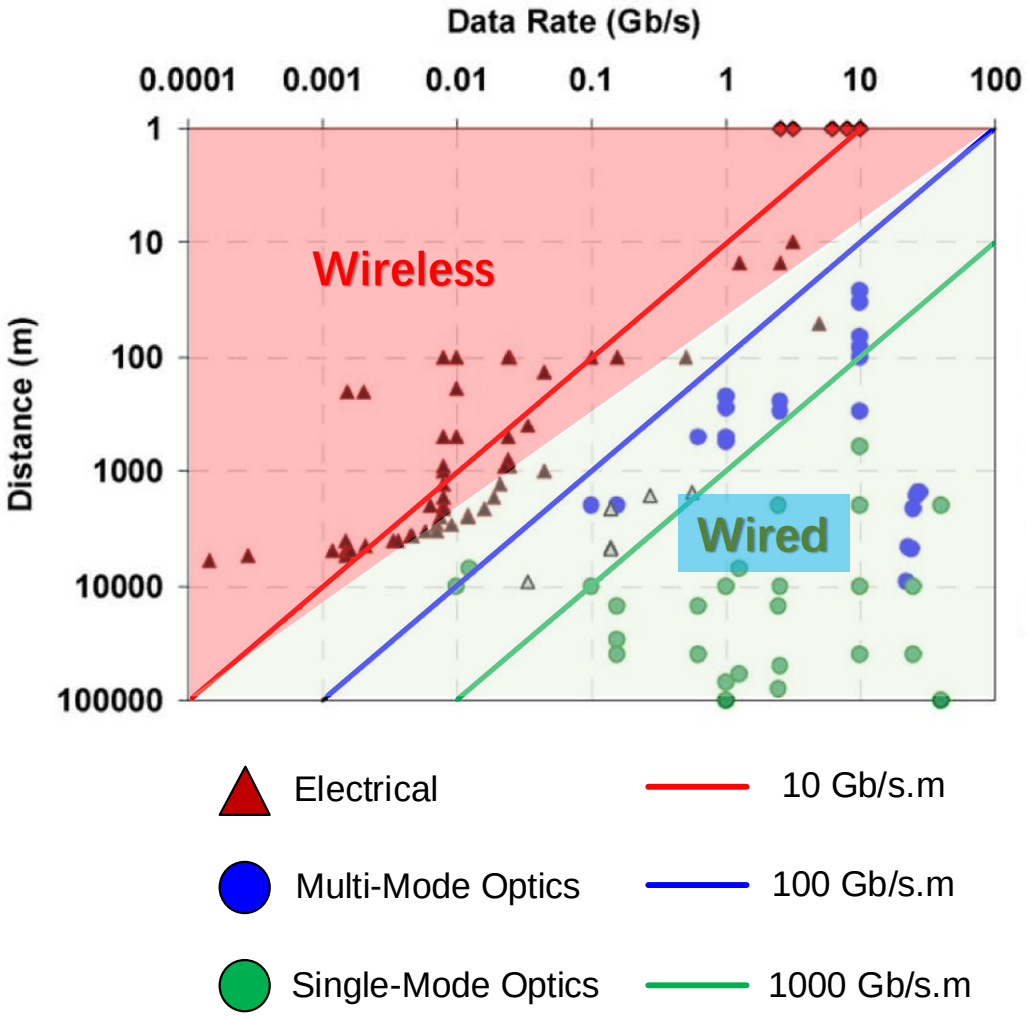
Hong Kong University of Science and Technology

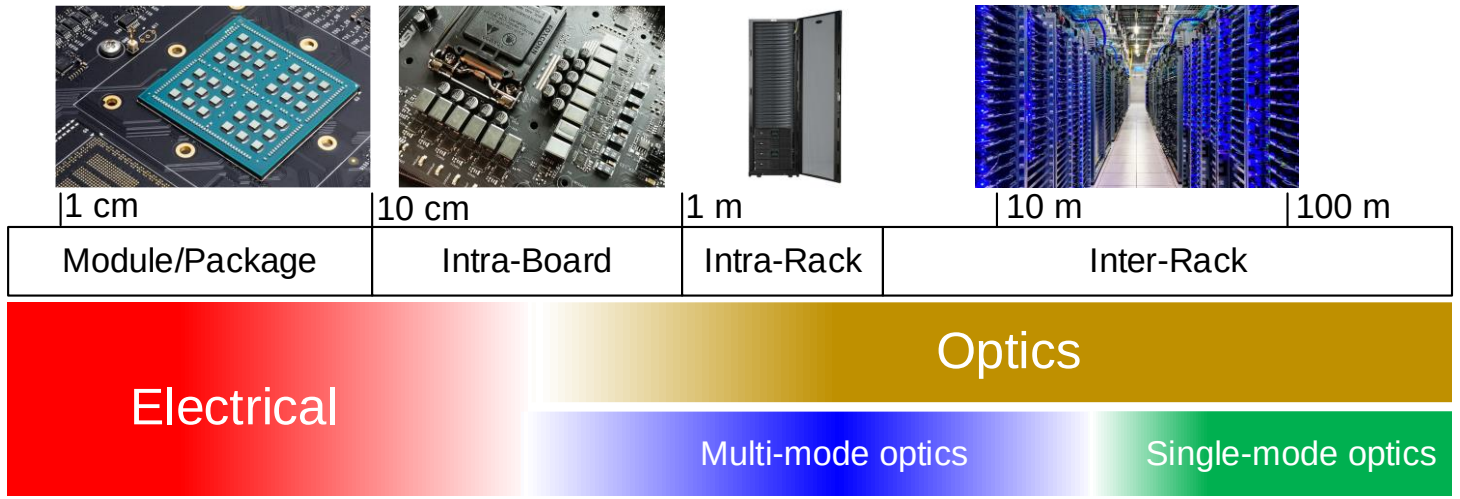
OWL ICDC ECE

Outline

- Optical, Wireless, and Optical Wireless – What? Why?
- Optical-Electronic Integrated Circuit (OEIC)
- CMOS mmWave Phased-Array IC
- High-SPLIQ IC for 6G Era
- New Potential Applications in the 6G Era
- Summary

Optical, Wireless, and Optical Wireless

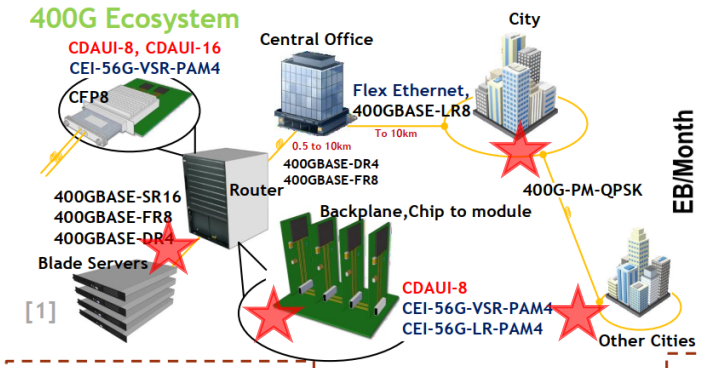


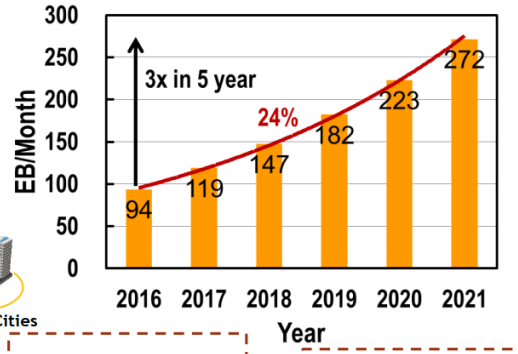


- **Copper: high loss, low bandwidth**
- **Fibers: low loss, high bandwidth, need OE-EO**
- **Optical for Distance X Data Rate > 100 Gb/s-m**
- **Cross-over opportunities!!**

➢ **High-Speed OWC, Short-Reach Optical**

Ethernet Wireline Link





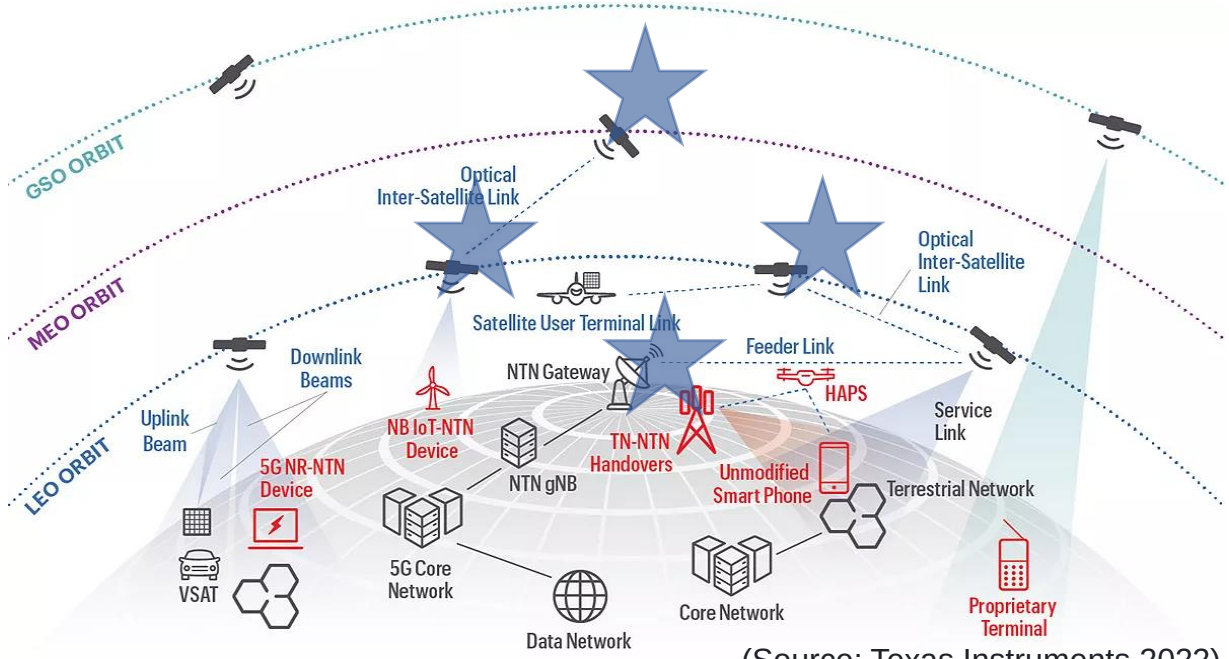
Global IP traffic Boom
5G Mobile Network
Internet of Things
Big Data & Cloud Computing

→ Increased data rate at every interfaces

→ Severer channel loss
Higher power

→ Higher power consumption on communication & cooling system

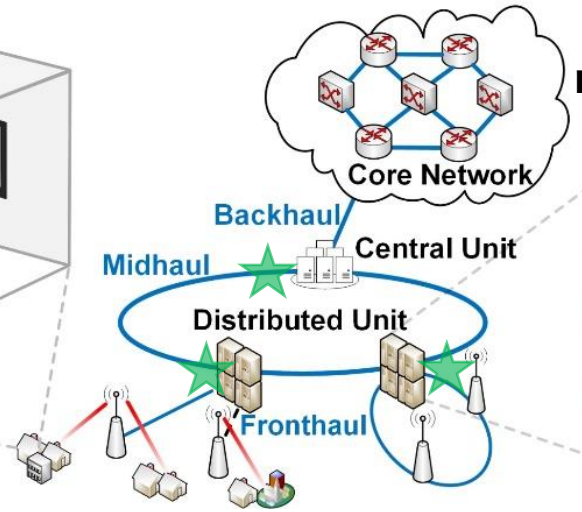
Motivation: Energy efficient high-speed data communication



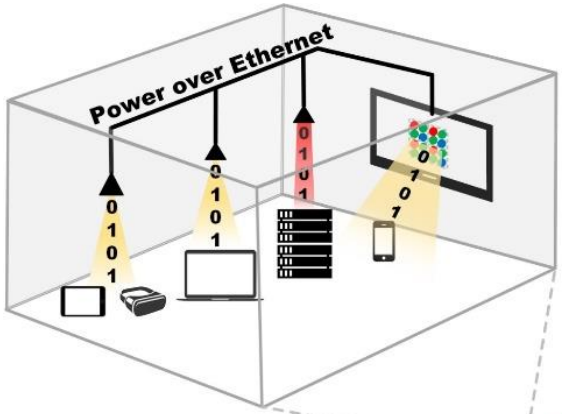
(Source: Texas Instruments,2022)

Non-terrestrial networks (NTN)

Optical fiber network for 5G network back-, mid-, front-haul connectivity



High-SPLIQ IC and SiP required in advanced enterprise communication applications

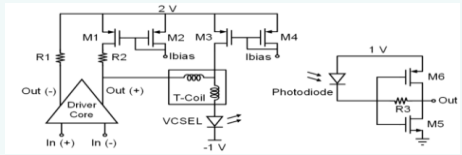


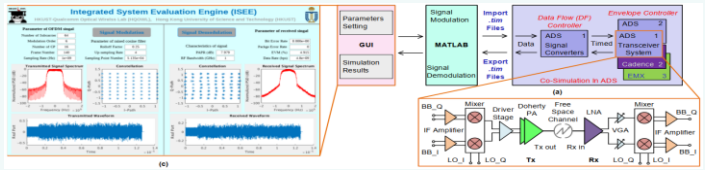
Optical-Electronic Integrated Circuit (OEIC)

CMOS Optoelectronic Interconnect Chip: Architecture Design

Fully-Integrated System Architecture Design and Verification

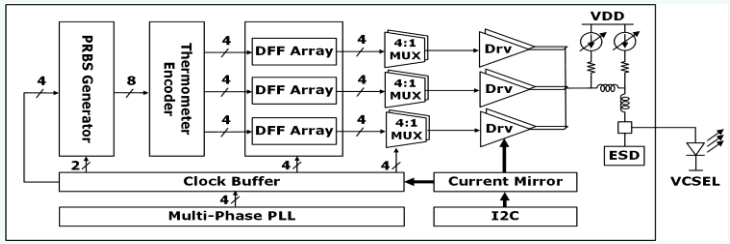
1. Top-down system simulation to clarify specifications for each module
2. Multi-chip system simulation throughout the entire design cycle
3. Support complex modulation scheme, like PAM-4, OFDM, QAM





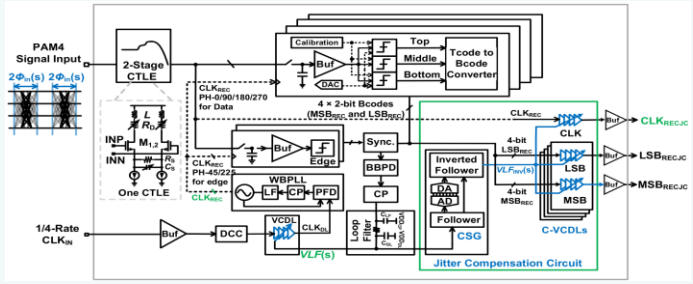
56-Gb/s PAM4 TX (ESSCIRC 2023)

- Thermometer-coded architecture
- Piecewise VCSEL nonlinearity compensation
- Pulse-based asymmetric edge compensation



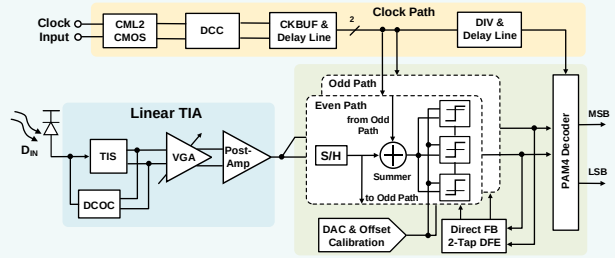
60-Gb/s PAM4 RX (JSSC 2023)

- Quarter-rate RX with jitter compensation CDR
- Wide jitter tolerance bandwidth + low jitter transfer



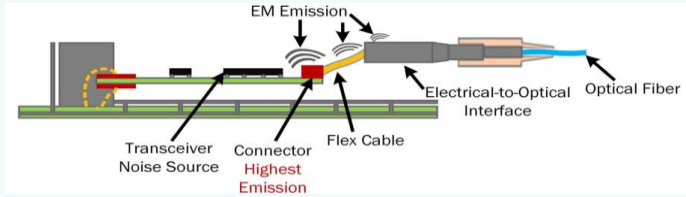
48-GHz PAM4 Optical RX (VLSI 2024)

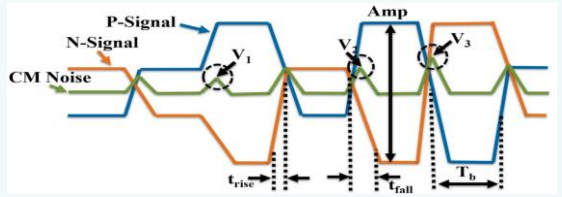
- Inductor-less + mixed signal decoding
- TAS-TIS topology for enhanced GBW
- Small area + low power

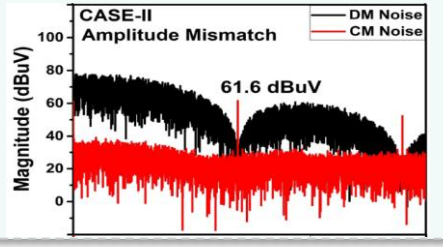


PAM4 Optoelectronic Interconnect Chip EMI Analysis and Cancellation

- Clarify radiation theory of CM noise
- Propose close-loop controlling of CM noise
- Propose CM noise cancellation circuit







广东省重点领域研发项目验收会

面向下一代以太网采用四电平脉冲幅度调制的CMOS全集成光电互联芯片的研究与设计

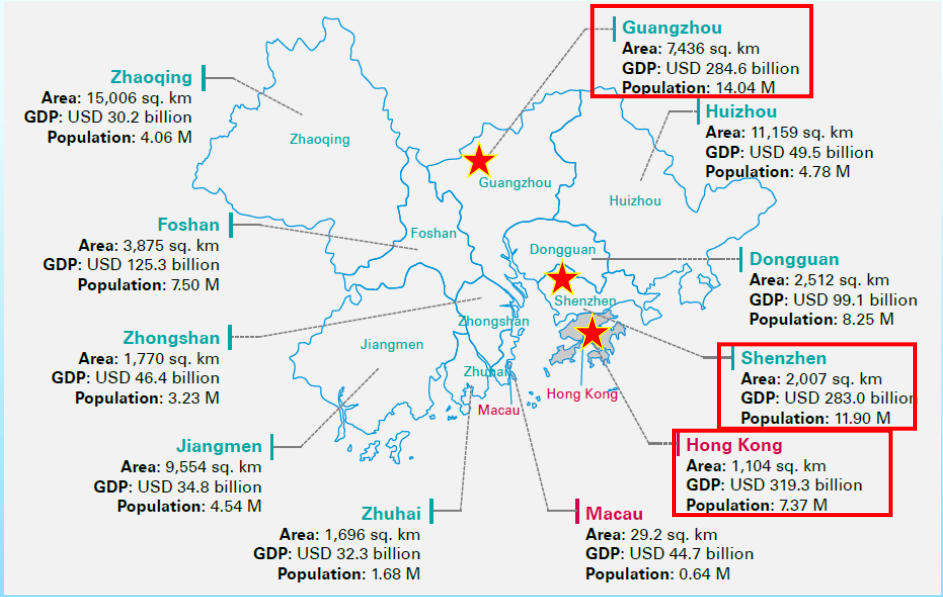
课题负责人：俞捷

课题汇报单位：香港科技大学

参与单位：

华南理工大学、南方科技大学

2024. 01. 22



项目分工

研究内容

PAM4光电互联芯片整体设计

PAM4光电互联芯片发射端信号失真补偿

PAM4光电互联芯片接收器前端设计

香港科技大学 俞捷教授

华南理工大学 陈志坚高工

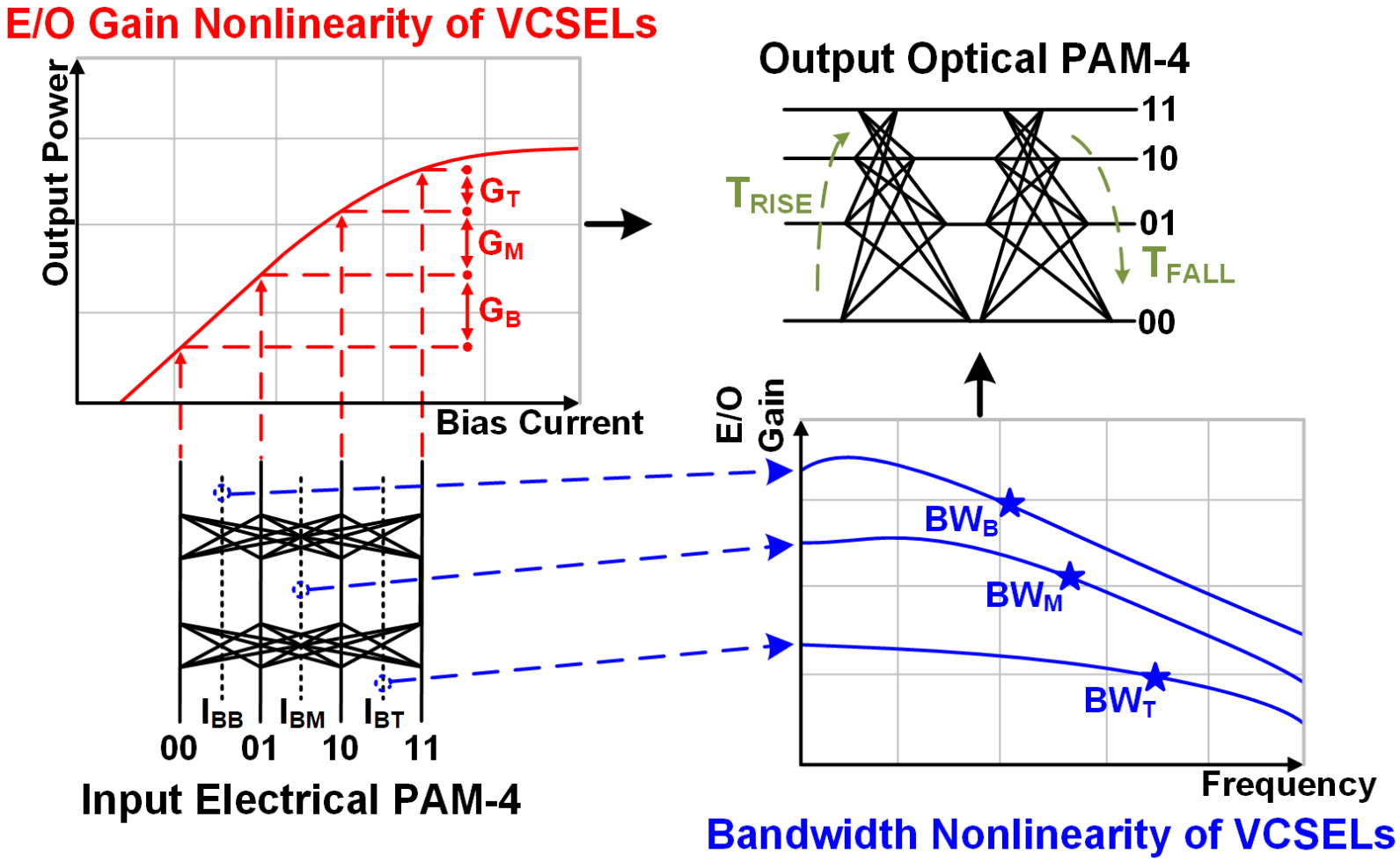
南方科技大学 余浩教授 潘权教授

项目实施

统筹项目工作计划和进度总体控制。负责组织课题工作的汇报、检查和验收

协助承担单位完成项目立项、中期审查、项目结题等工作

Nonlinearity of VCSEL Limits the Optical Signal Quality

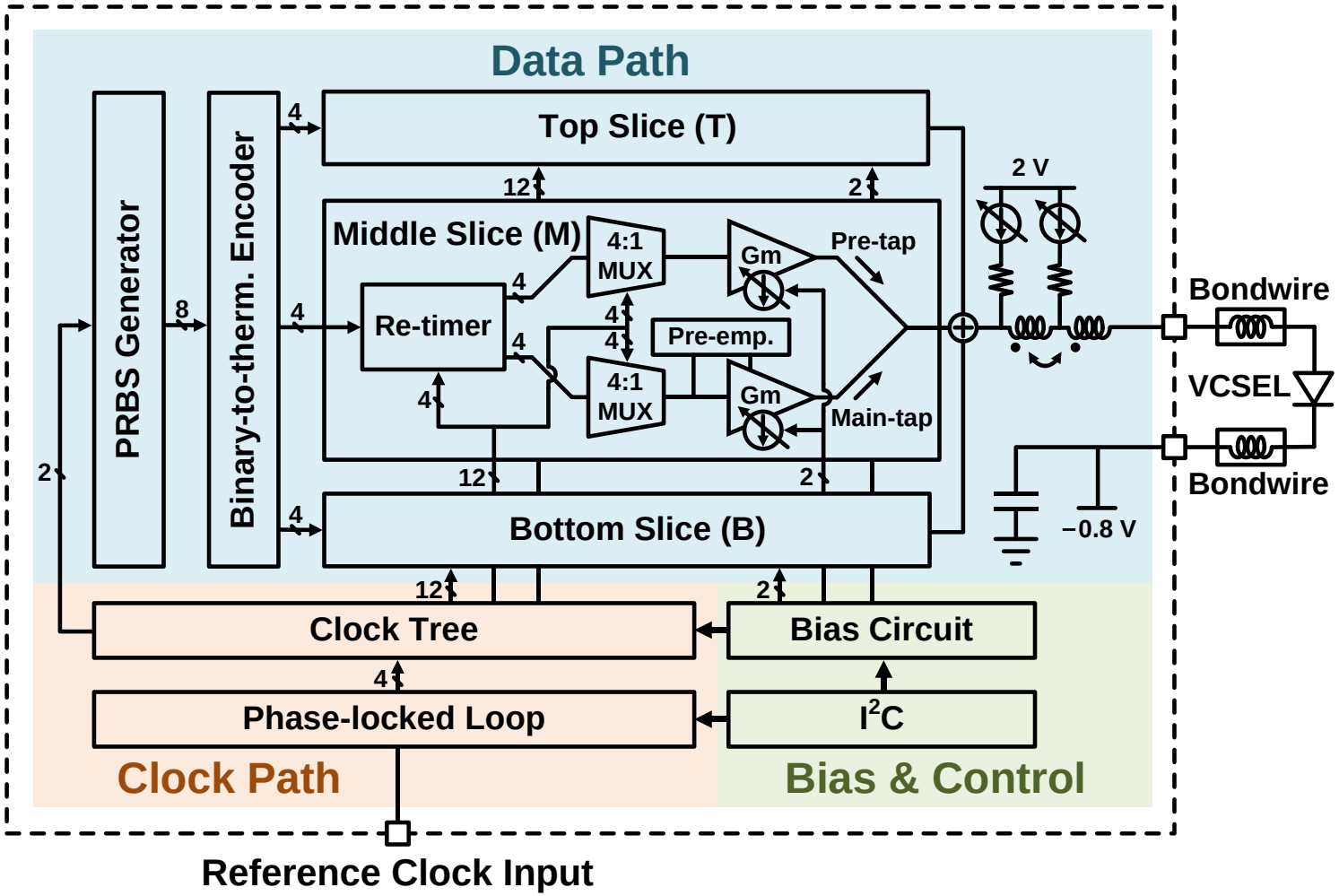


Non-idealities of VCSEL:

- ❑ **Bias Current ↑, E/O Gain ↓**
  ($G_B > G_M > G_T$)
- ❑ **Bias Current ↑, Bandwidth ↑**
  ($BW_B < BW_M < BW_T$)
- ❑ $T_{RISE} < T_{FALL}$

[1] F. Chen and **C. P. Yue**, ESSCIRC 2023, Lisbon, Portugal.

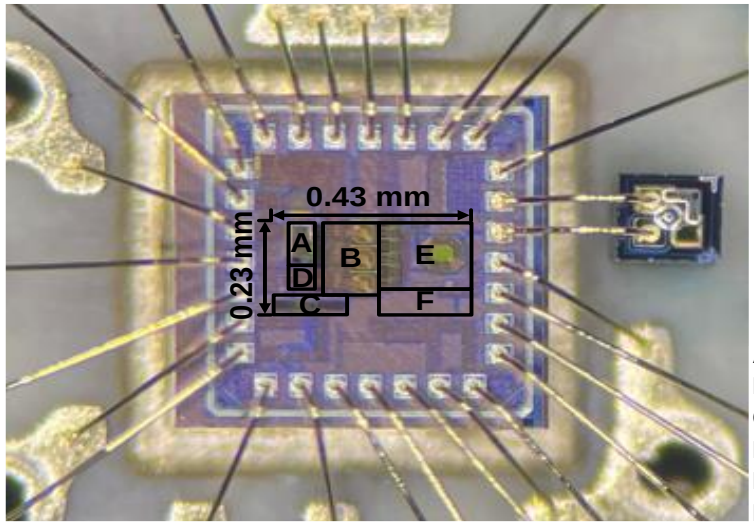
High-linearity 56-Gb/s PAM4 Optical Tx chip

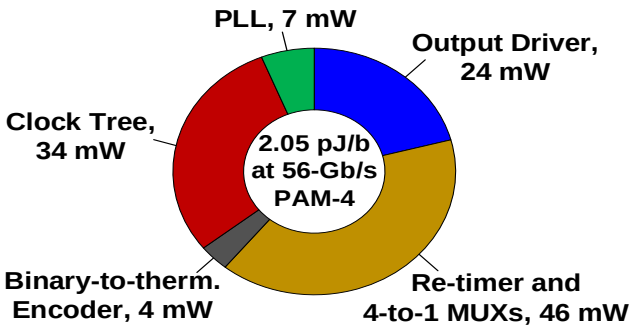


- ❑ **Data path**
  - 2-tap feed-forward equalizer
  - Gm cell-merged CTLE
  - Pre-emphasis circuit
- ❑ **Clock path**
  - Wideband phase-locked loop
  - Clock tree with cascading VCDLs
- ❑ **Bias & control part**
- ❑ **Optical part**
  - Wire-bonded anode-driven VCSEL
  - Negative bias for power saving

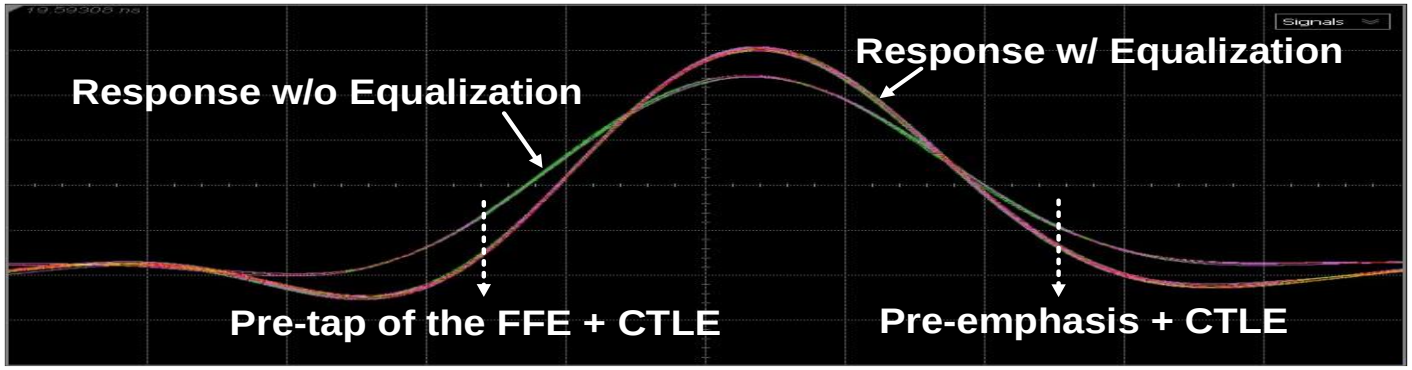
[1] F. Chen and **C. P. Yue**, ESSCIRC 2023, Lisbon, Portugal.

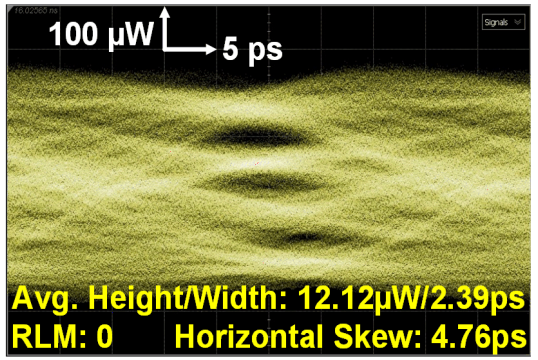
Optical Transmitter Measurement Results



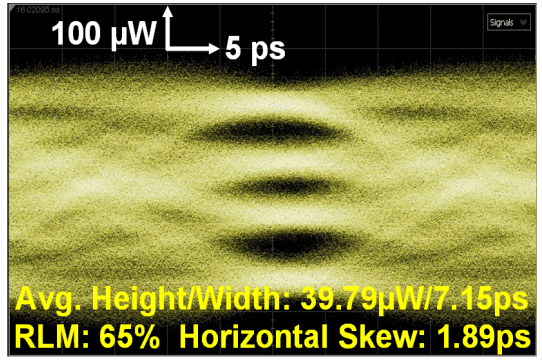


A — PRBS Generator + Binary-to-therm. Encoder
B — Re-timer + 4-to-1 Multiplexers
C — Phase-locked Loop
D — Clock Tree
E — Output Driver
F — Bias Circuit + I^2C

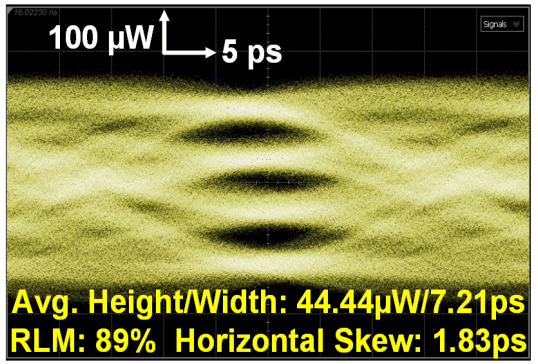




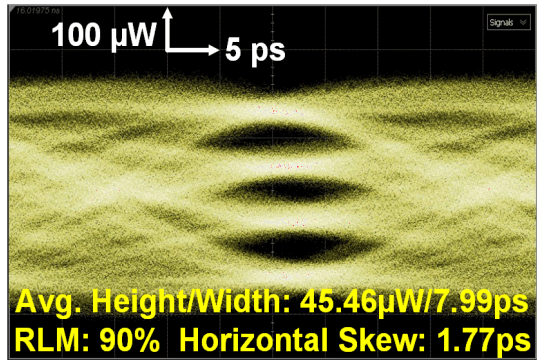
(a) EQ OFF, Equal Slice Gain



(b) Equal Slice EQ and Slice Gain



(c) Equal Slice EQ, Piecewise Tuned Slice Gain



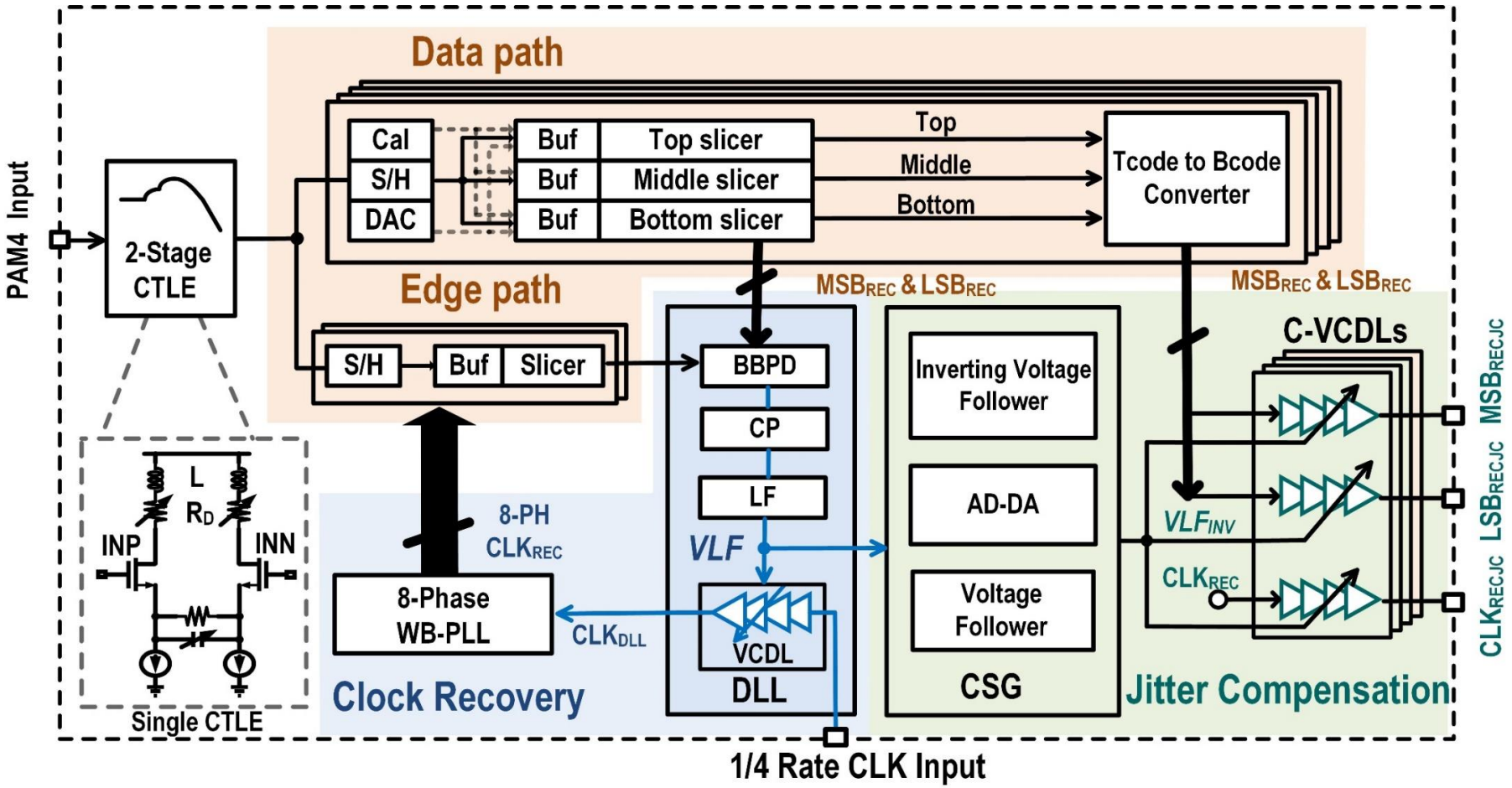
(d) Piecewise Tunned Slice EQ and Slice Gain

- Implemented in 40nm CMOS, 0.1 mm^2 of core area
- Tuned slice EQ and slice gain to compensate for the VCSEL nonlinearity

Comparison with the State-of-the-Art

	PTL'18	JSSC'22	VLSI'19	ASSCC'21	This work
Technology [nm]	65	40	65	40	40
Signalling scheme	1/2-rate PAM-4	1/4-rate PAM-4	1/4-rate PAM-4	1/4-rate PAM-4	1/4-rate PAM-4
Date rate [Gbps]	50	56	64	64	56
OMA [mW]	2.00	0.81	2.50	1.08	1.18
Power effi. [pJ/b]	5.12	1.73	2.69	2.09	2.05
Core area [mm^2]	0.31	0.47	0.28	0.16	0.10
Asymmetric equalization	2.5-tap DAC-based FFE	2-tap DAC-based FFE	3-tap LSB/MSB-based Asymmetric FFE	3-tap LSB/MSB-based Asymmetric FFE	2-tap FFE + CTLE + Pre-emphasis
Nonlinearity compensation	Full	Full	Partial	Partial	Full
Method type	Digital	Digital	Analog	Analog	Analog

PAM4 RX: Signal Equalization, Decoding, Clock and Data Recovery



- ❑ **Two-stage CTLE**
  - **Chanel loss compensation**
- ❑ **1/4-Rate architecture**
- ❑ **DLL-based CDR architecture**
- ❑ **Jitter compensation circuit:**
  - **40-MHz wide jitter bandwidth**
  - **attenuated -8-dB jitter transfer**

[1] L. Wang and **C. P. Yue**, JSSC 2023.

[2] L. Wang and **C. P. Yue**, VLSI 2021, Kyoto, Japan.

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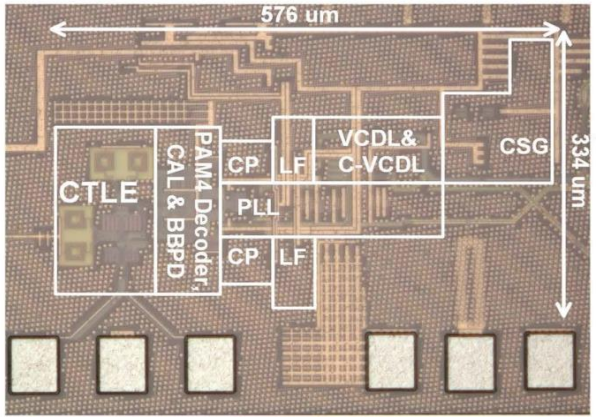
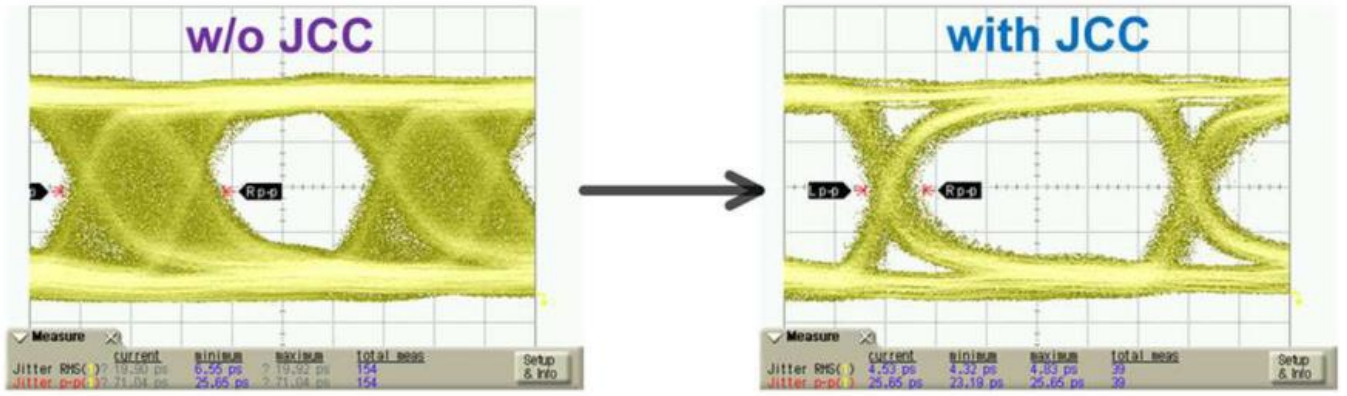
PAM-4 RX Measurement Results

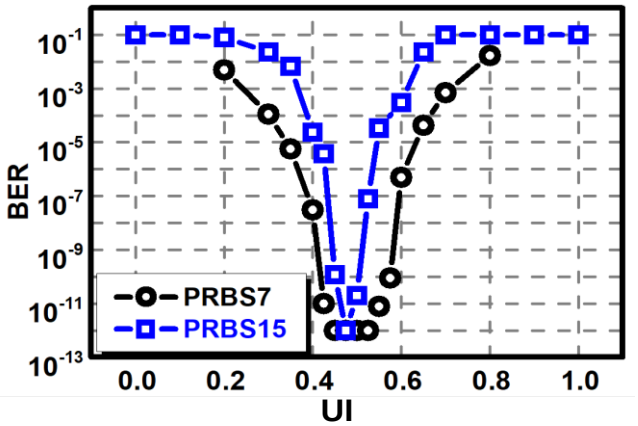
- Implemented in 40nm CMOS technology, 0.58 x 0.34 mm² of core area, Error-free under 60-Gb/s
- Up to 64% of the input jitter can be attenuated, improving the quality of decoded data



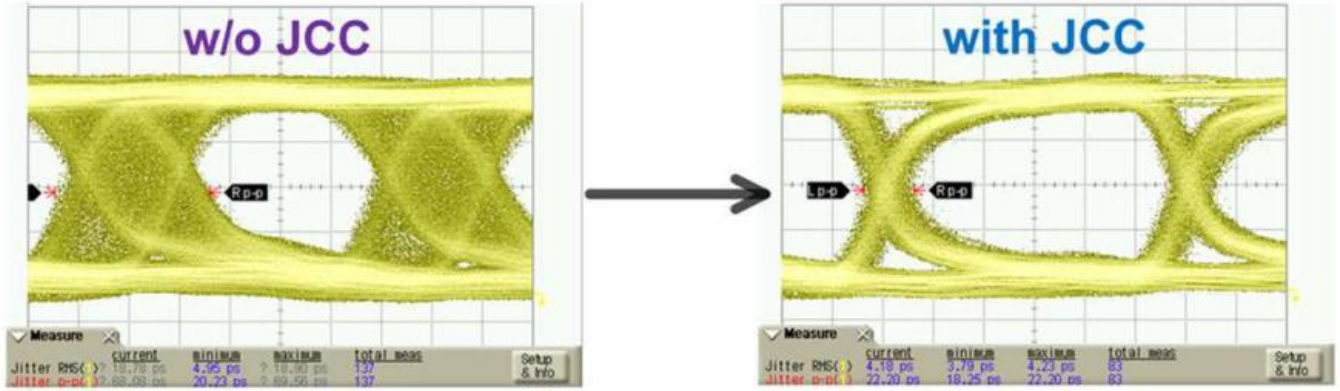
Chip Photo



Jitter Compensation Performance with 10-KHz Input Jitter



Bathtub Curve



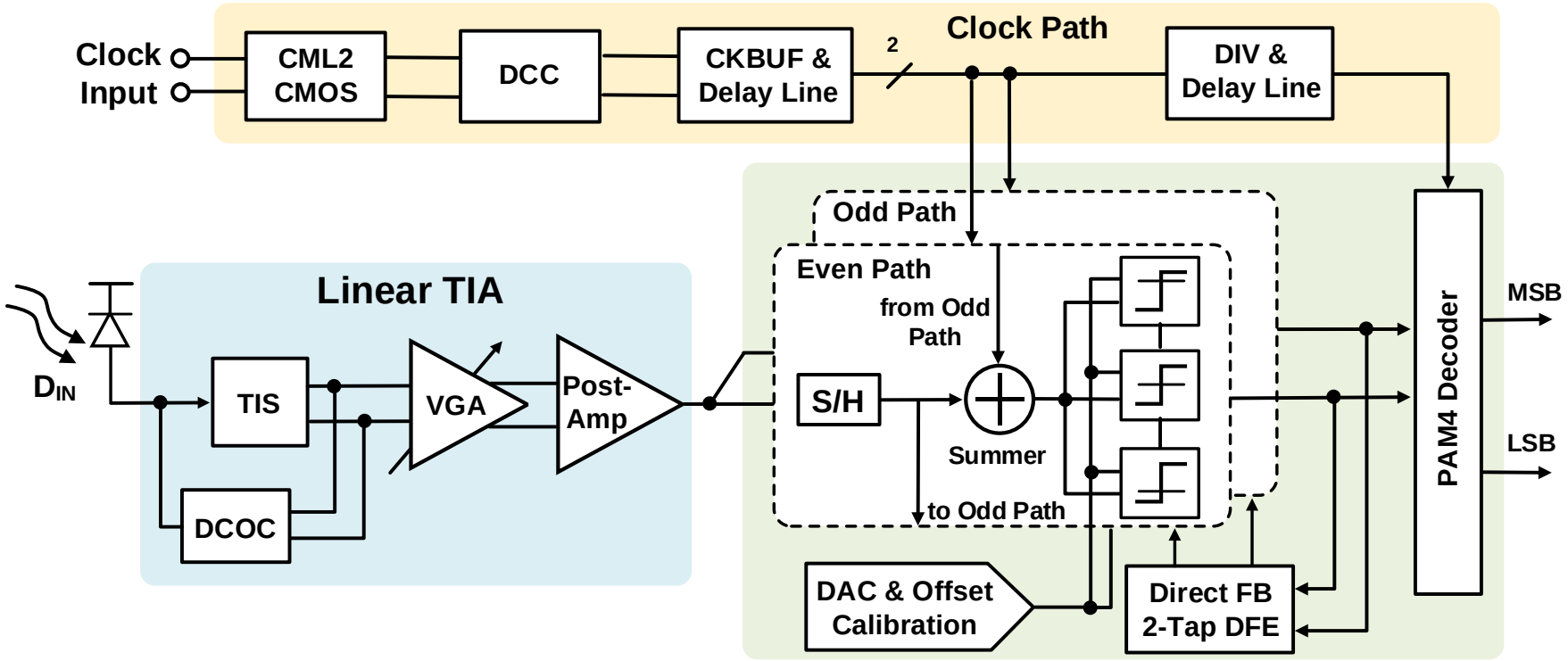
Jitter Compensation Performance with 1-MHz Input Jitter

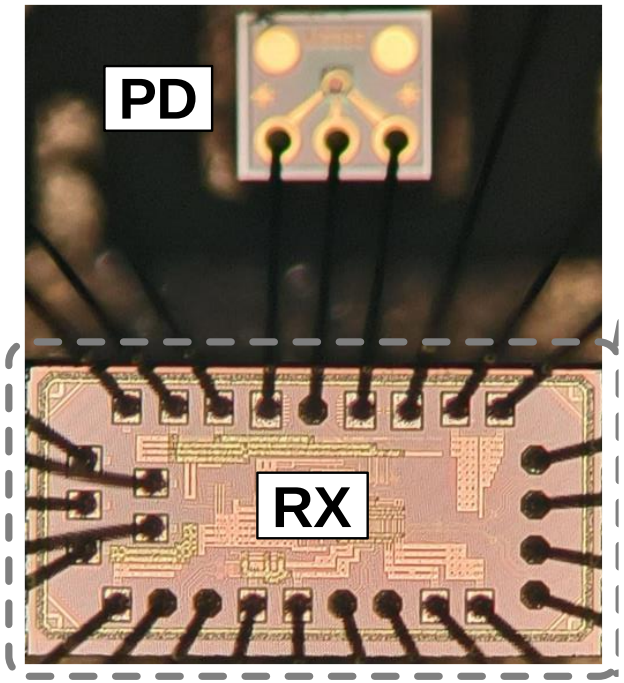
Comparison with the State-of-the-Art

	JSSC'19	JSSC'19	VLSI'14	JSSC'17	VLSI'14	This work
Technology	28-nm	40-nm	65-nm	65-nm	28nm	40-nm
Architecture	1/4-Rate NRZ	1/4-rate NRZ	1/4-rate NRZ	1/4-rate NRZ Adaptive LPF BW in CDR	1/4-rate NRZ Split path CDR	1/4-rate PAM4, JCCDR
JTOL [UI_{PP}] @ 3dB bandwidth	None @ 1 MHz	0.22 UIPP** @ 4 MHz	0.1 UIPP @ 1 MHz	0.41 UIPP @ 20 MHz	0.2 UIPP @ 8 MHz	0.2 UIPP 40 MHz
JTRAN [dB] @ 3dB bandwidth	None	0 ~ -3 dB @DC ~ 4 MHz	0 ~ -3 dB @DC ~ 1 MHz	0 ~ -3 dB @DC ~ 4 MHz	0 ~ -3 dB @DC ~ 3MHz	<-8 dB @All band
Data rate [Gb/s]	2-pairs × 16	25	14	40	4-lanes × 40	60
Power [mW]	2-pairs × 16.06	27***	7.8	225	4-lanes × 175	70.8
Power efficiency [pJ/bit]	1.004*	1.08***	0.56	5.625	4.375	1.18
Supply voltage (V)	0.9	None	0.8	1.2	None	1.0

A 48-Gb/s Half-Rate PAM-4 Optical Receiver

- No CTLE, using TAS-TIS amplifier for boosting gain-bandwidth (GBW) product
- Inductor-less design, achieving 0.06-mm^2 area efficiency in 28nm CMOS
- Half-rate architecture to simplify the clocking scheme and layout

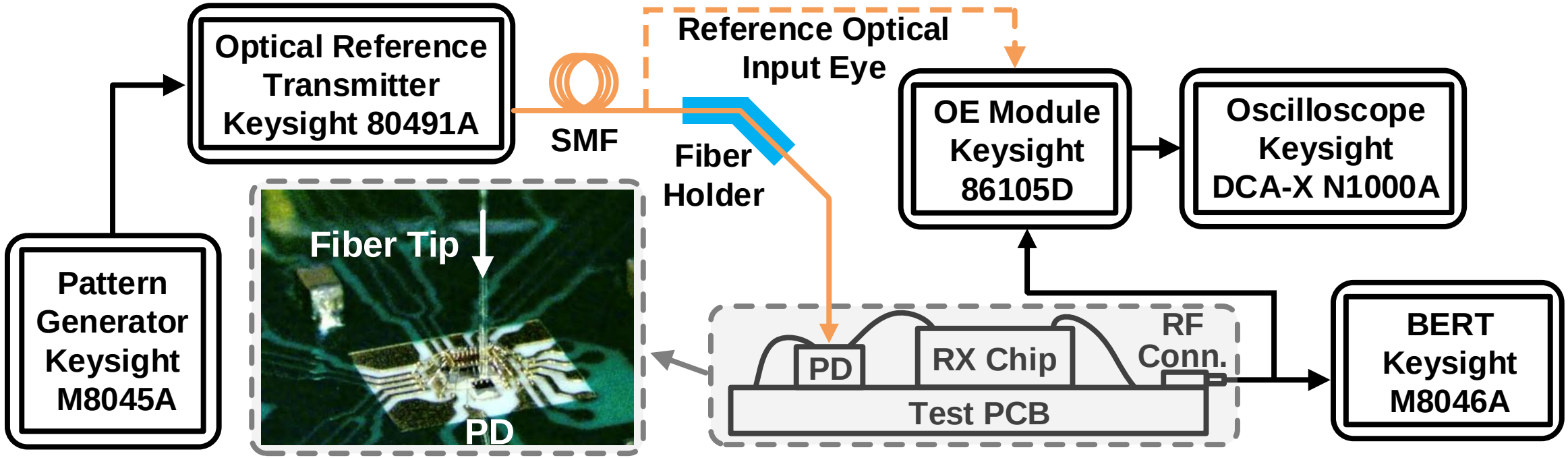




[1] C. Zhang and **C. P. Yue**, VLSI 2024, Honolulu, USA.

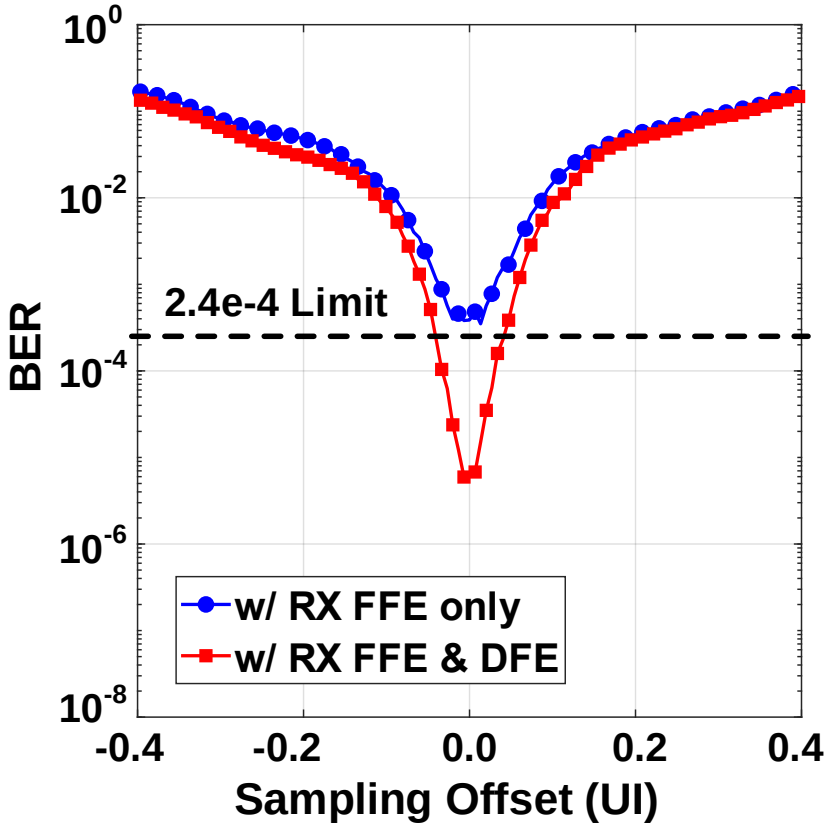
PAM-4 Optical Receiver Measurement Setup

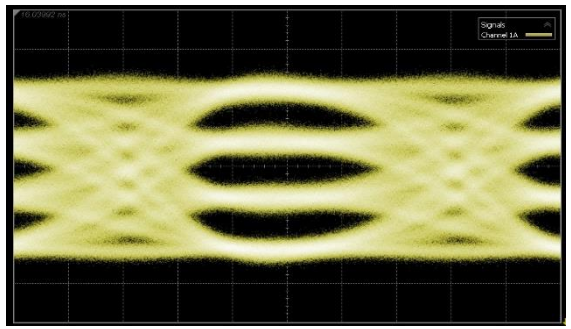
- A PD is wire-bonded with the receiver chip, the light (1308 nm) is coupled through an fiber
- The optical signal is converted to electrical signal, then amplified, decoded, and de-muxed on chip



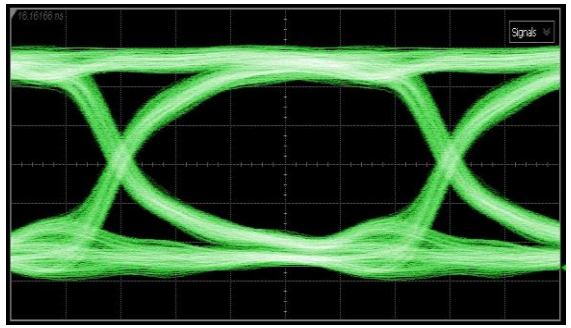
PAM-4 Optical Receiver Measurement Results

- By enabling the FFE, BER reaches 1e-5 with 48-Gb/s input, better than the standard of 2.4e-4
- Under 2.4e-4 BER target, -5.1-dBm sensitivity at 48 Gb/s is achieved

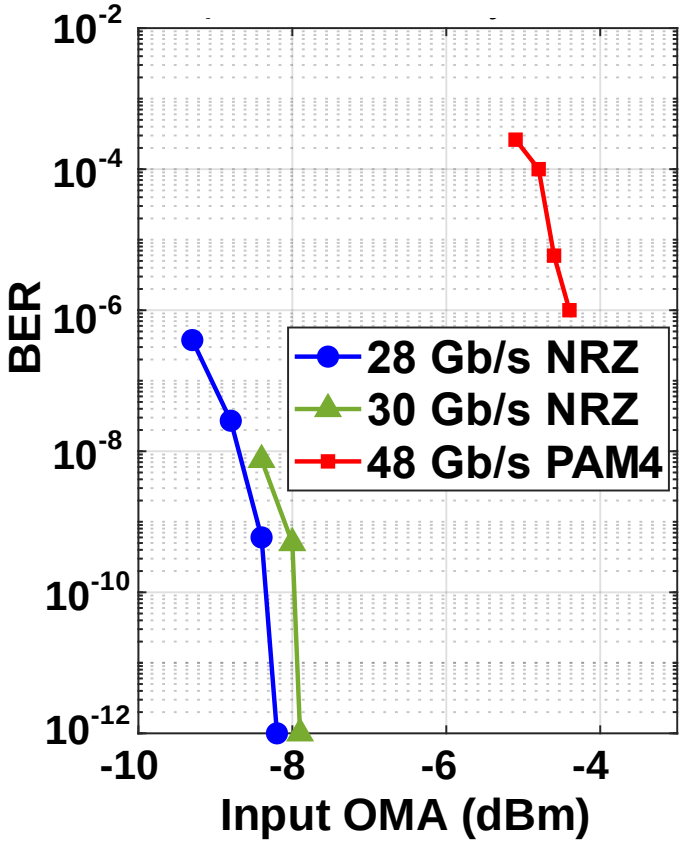




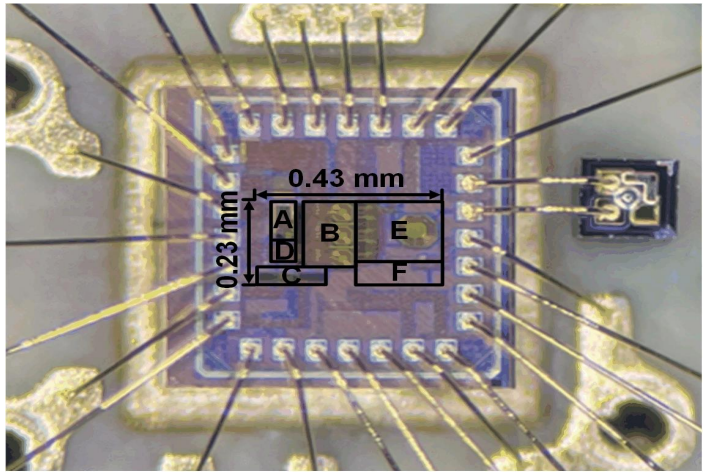
48-Gb/s PAM4 Input

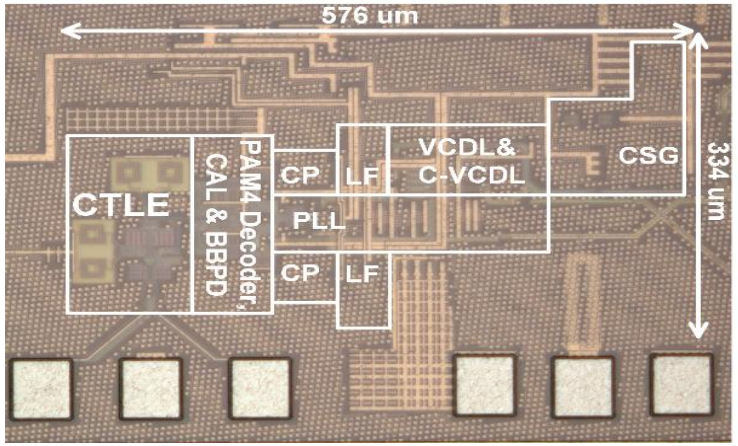


Decoded 6-Gb/s Output



VCSEL TRX Demo: 56-Gb/s PAM-4 VCSEL TX and RX





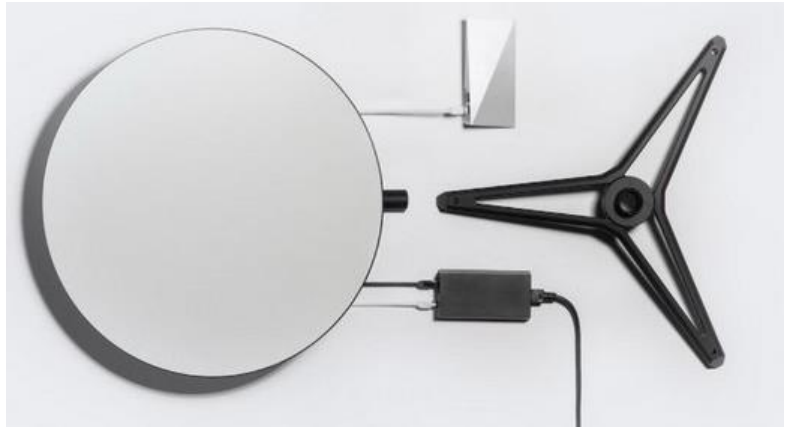
Link

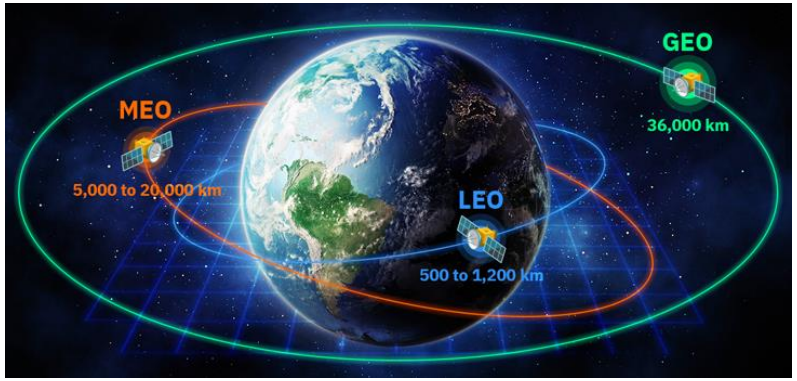
PAM4收发机芯片演示视频 ESSCIRC 2023+VLSI2021 Fuzhan Li_哔哩哔哩_bilibili

QR code

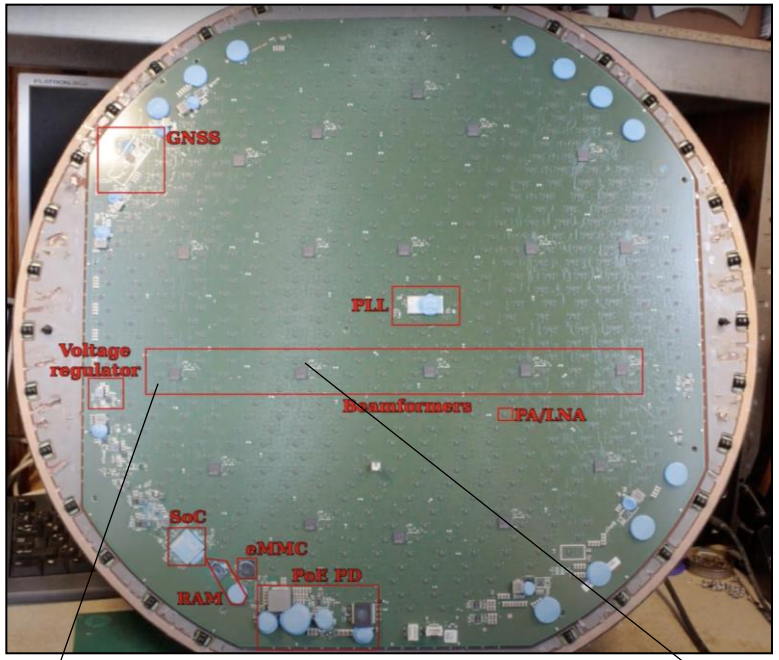
CMOS mmWave Phased-Array IC

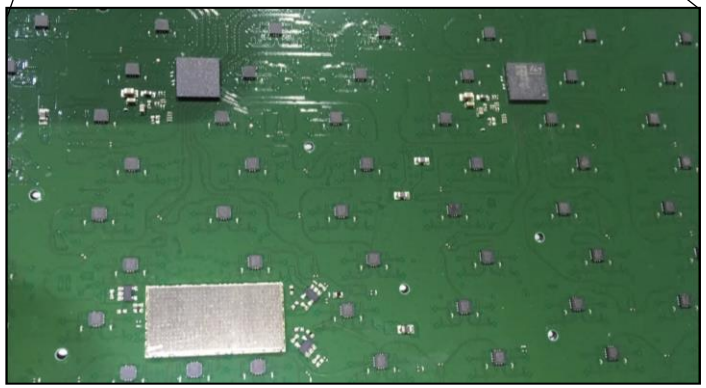
Starlink Satcom





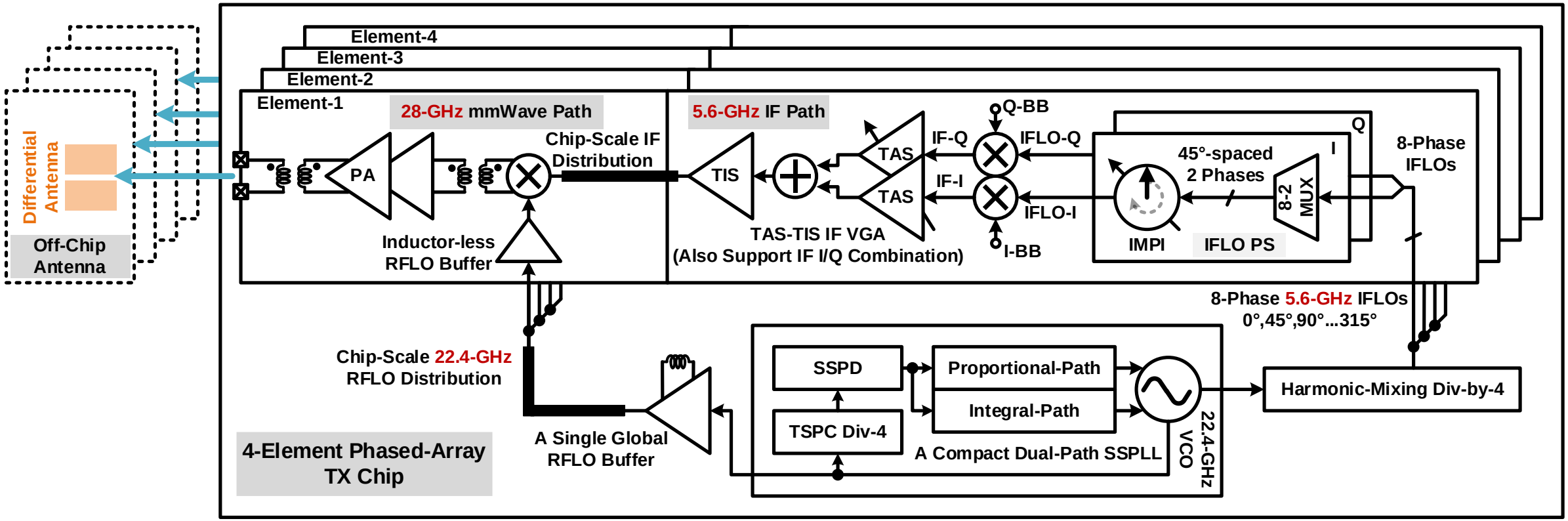
Starlink Ground Dish





- Mechanical satellite tracking employed
- Utilization of electrical and digital beamforming
- Architecture designed to minimize beamforming IC usage
- Focus on combining individual PAs and LNAs for gain enhancement

A Ka-Band Phased-Array Tx SoC in 40nm CMOS



Sliding-IF Architecture | **IFLO Phase Shifting + IF VGA** | **Integrated PLL** | **Differential Antenna**

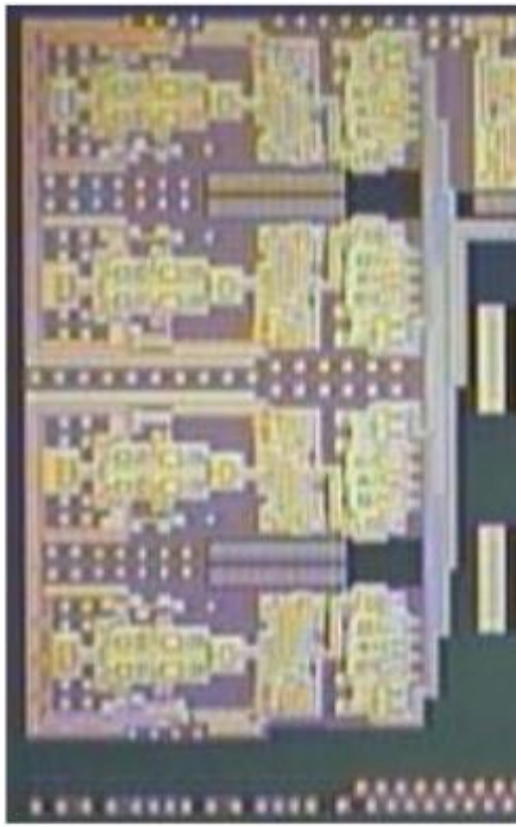
[1] L. Wang and **C. P. Yue**, ESSERC 2024, Brugges, Belgium.

[2] Z. Liu and **C. P. Yue**, IMS 2024, Washington, USA.

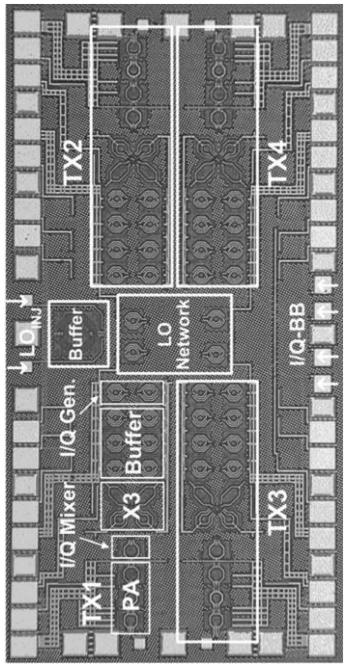
[3] L. Wang and **C. P. Yue**, CICC 2024, Denver, USA.

[4] L. Wang and **C. P. Yue**, JSSC 2024, Invited Special Issue.

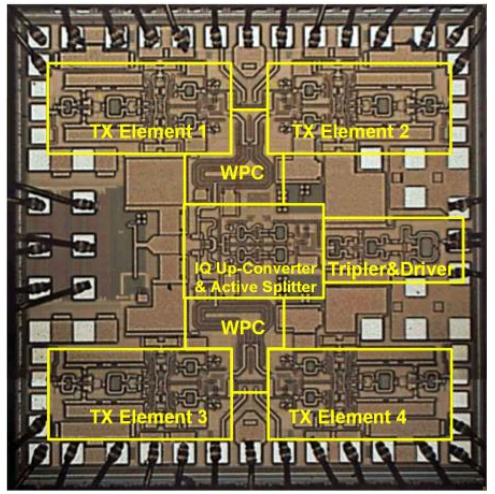
Area Efficiency Comparison



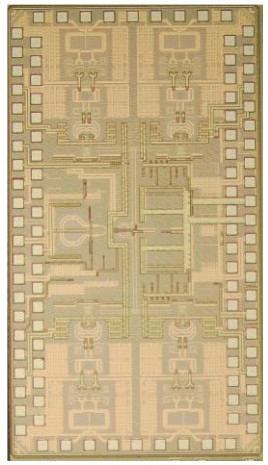
TMTT 2021, 38 GHz
4.3 x 2.2 mm²
w/o LO Gen.



JSSC 2010, 60 GHz
2.9 x 1.4 mm²
w/o LO Gen.

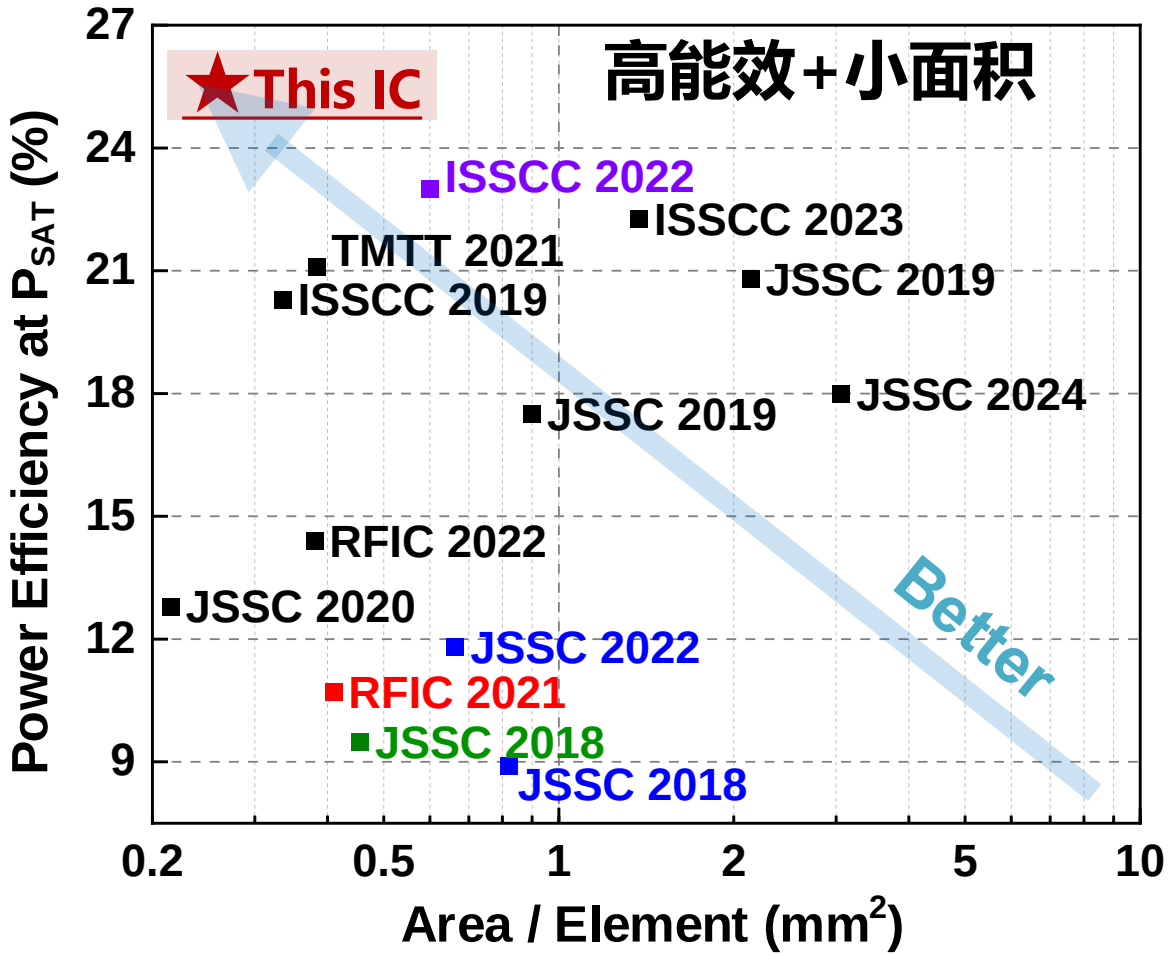


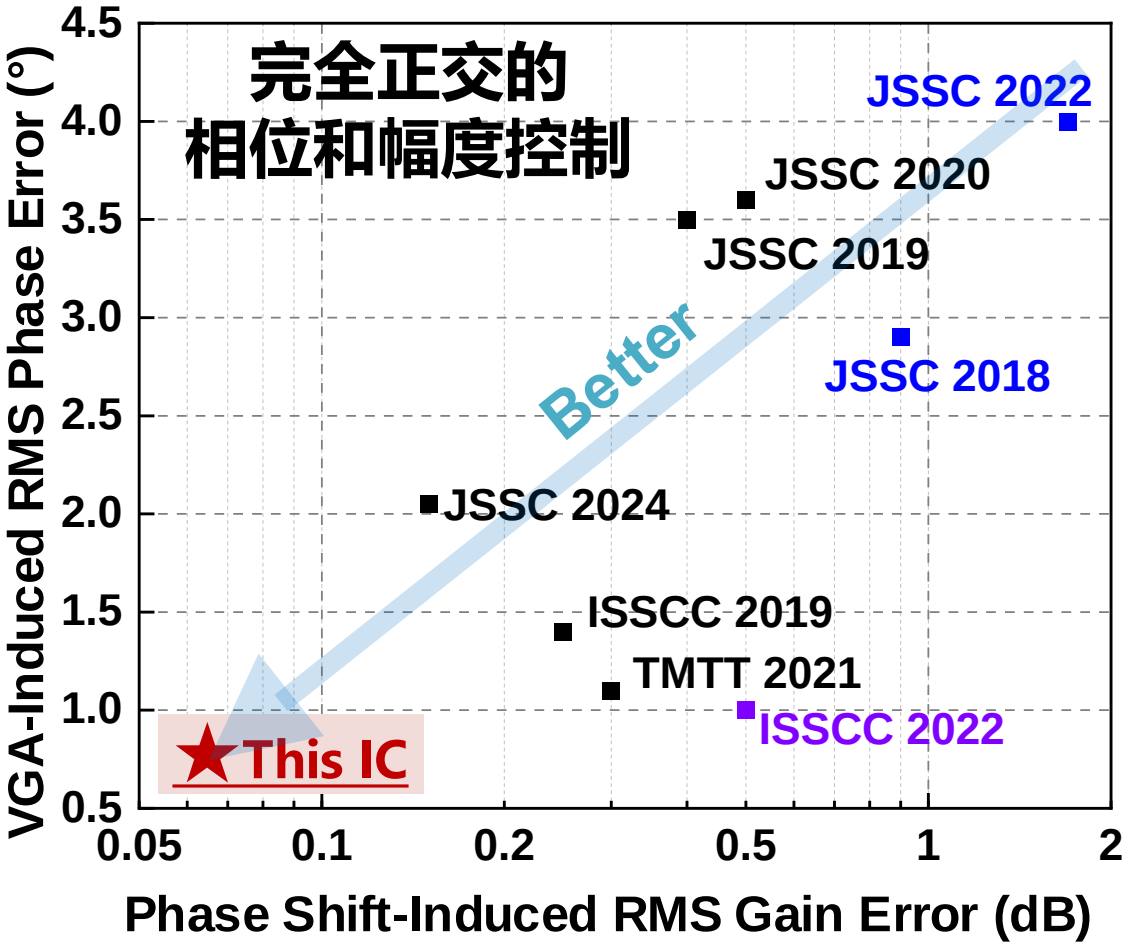
JSSC 2022, W band
2 x 2 mm²
w/o LO Gen.



This work, 28 GHz
1.87 x 1.16 mm²
with LO Gen

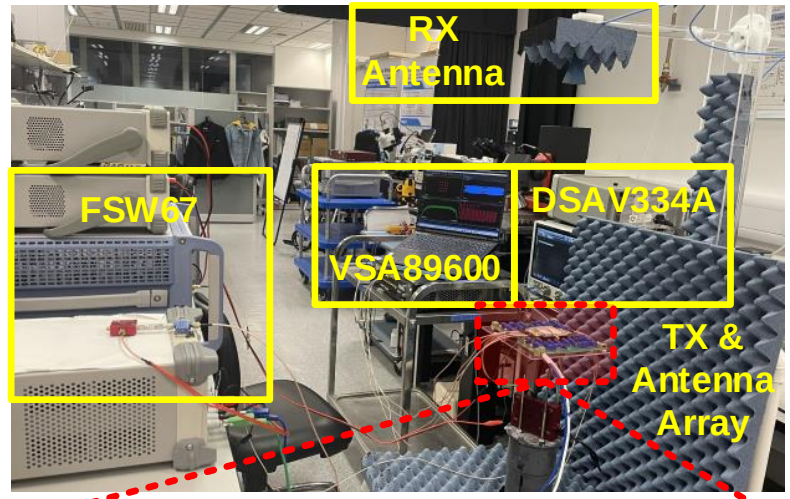
Comparison with the State-of-the-Art

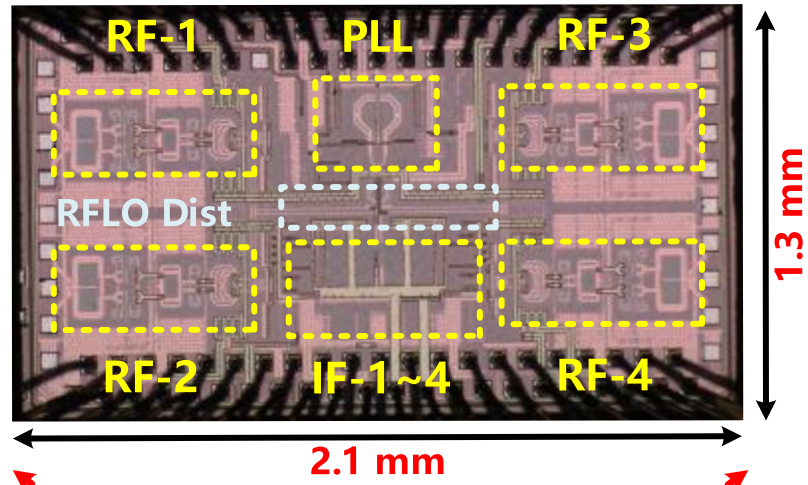


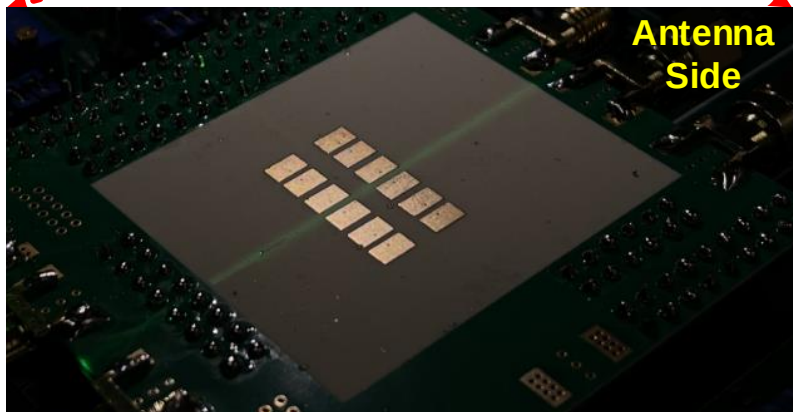


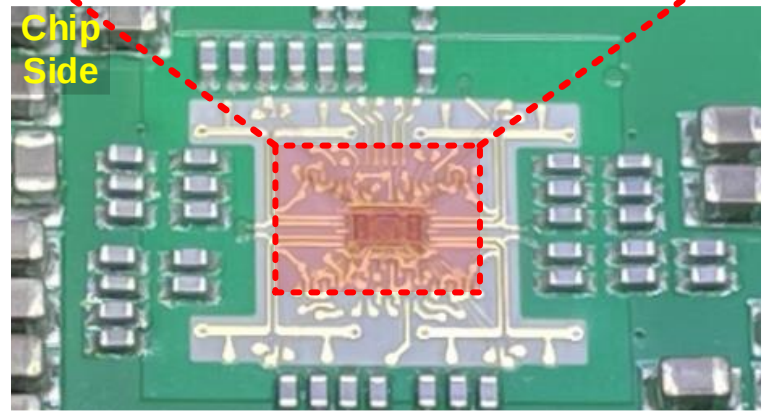
Beamformer Chip + Matching Network + Antenna

- Prototyped in 40-nm process
- Total area (4 elments): $1.3 \times 2.1\ mm^2$
- Core area per element: $0.26\ mm^2$
- Bonded + matching network + *differential antenna*

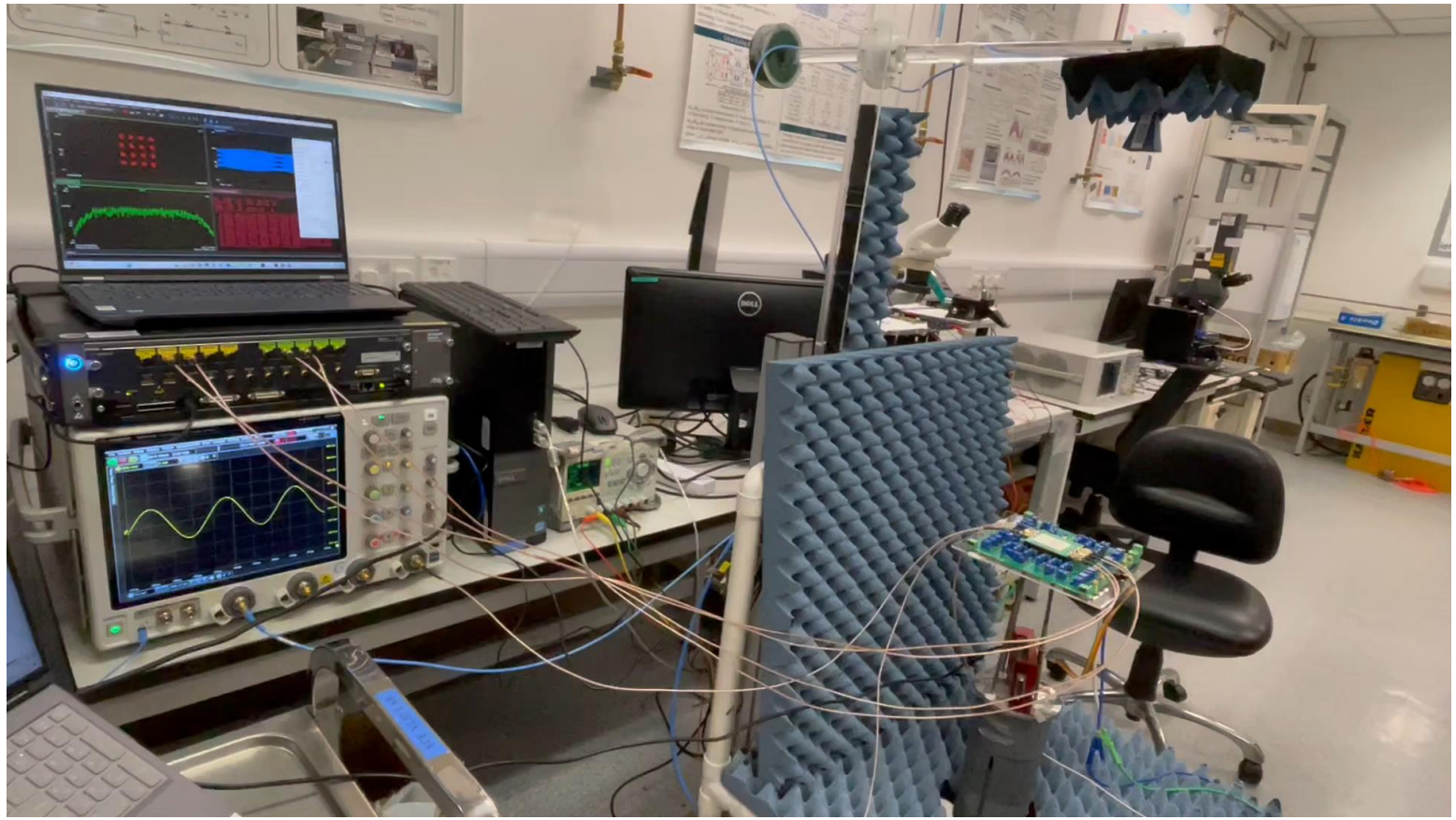


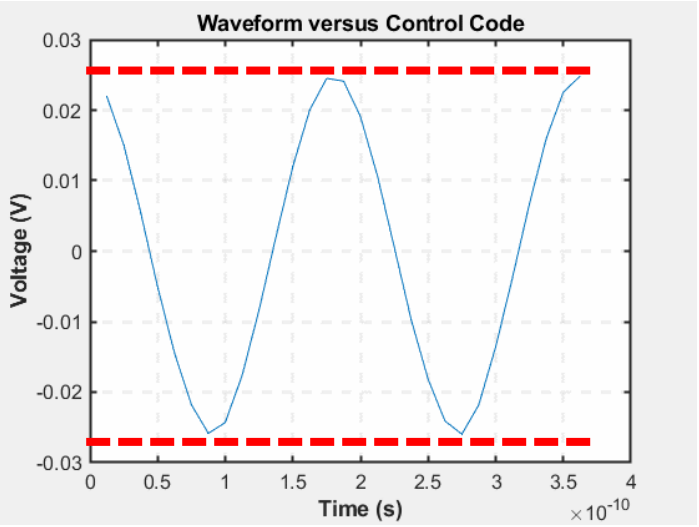


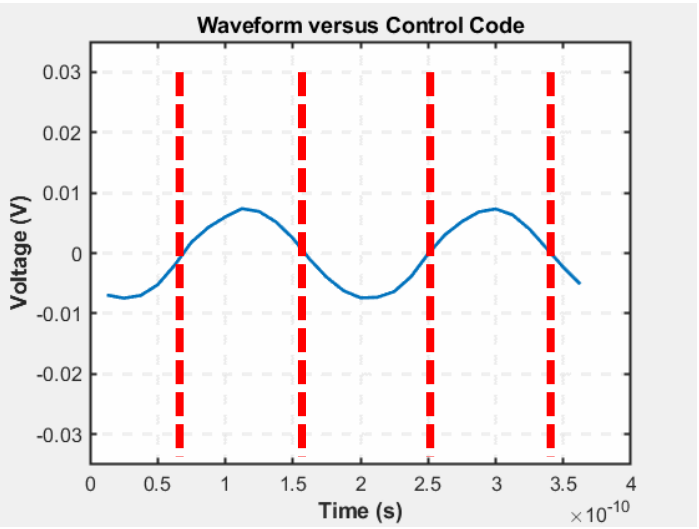




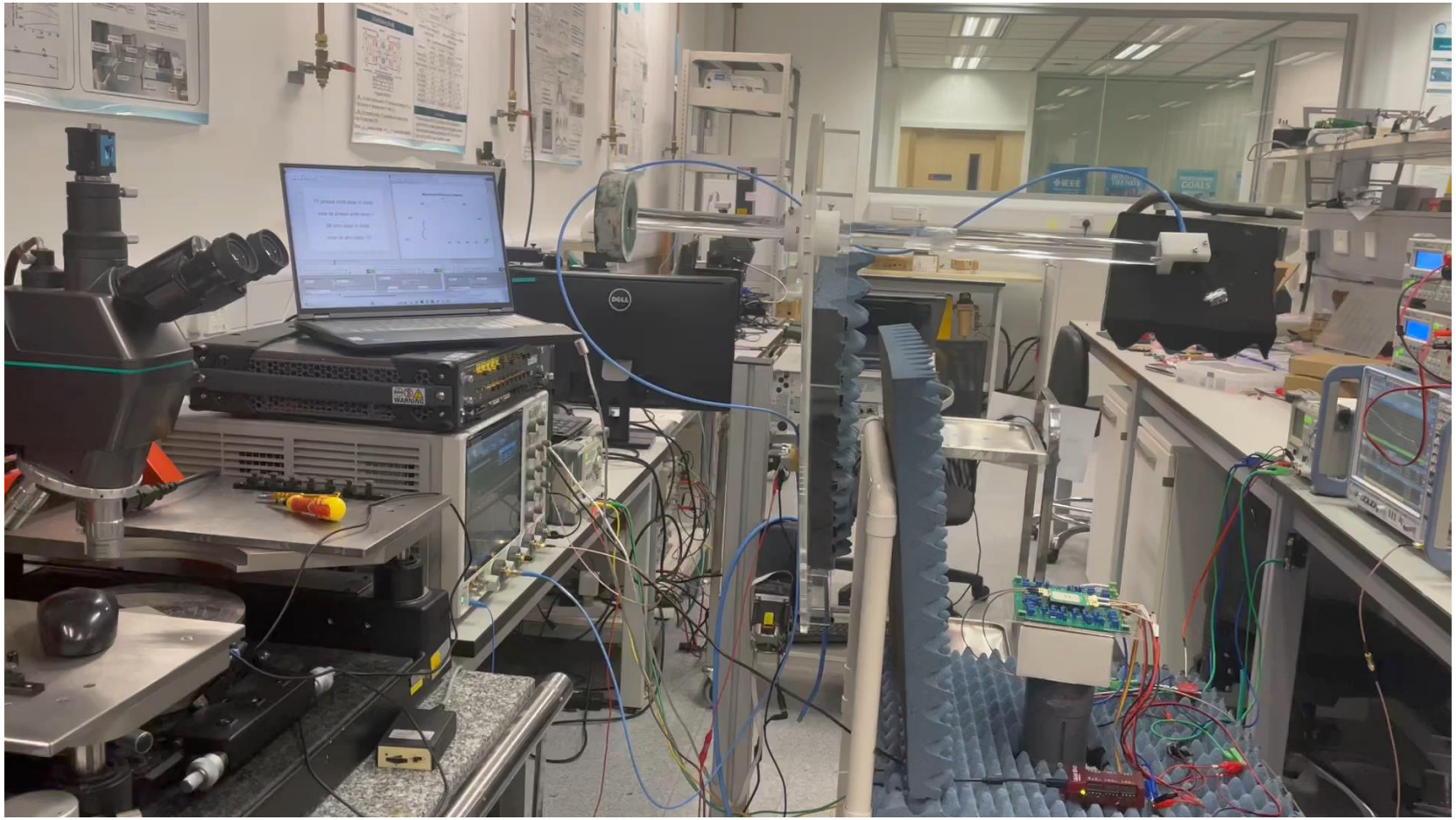
- **Phase Shift and Gain Control Demo**
  - ***Orthogonal*** **phase shift and gain control**

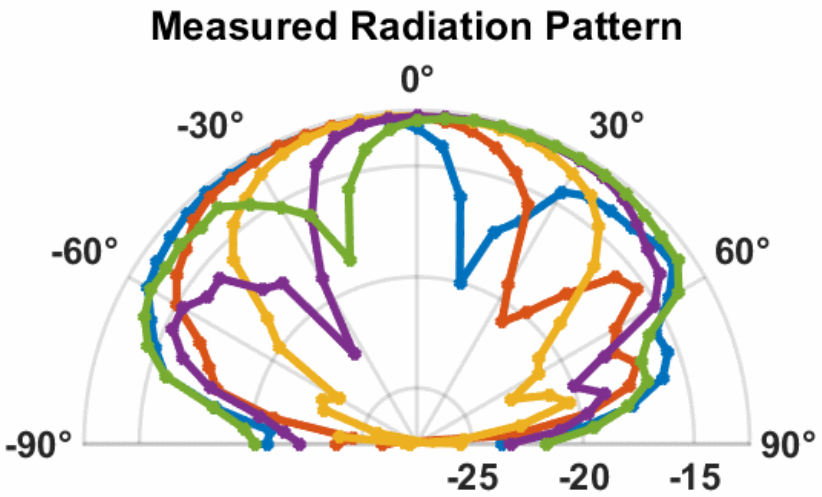


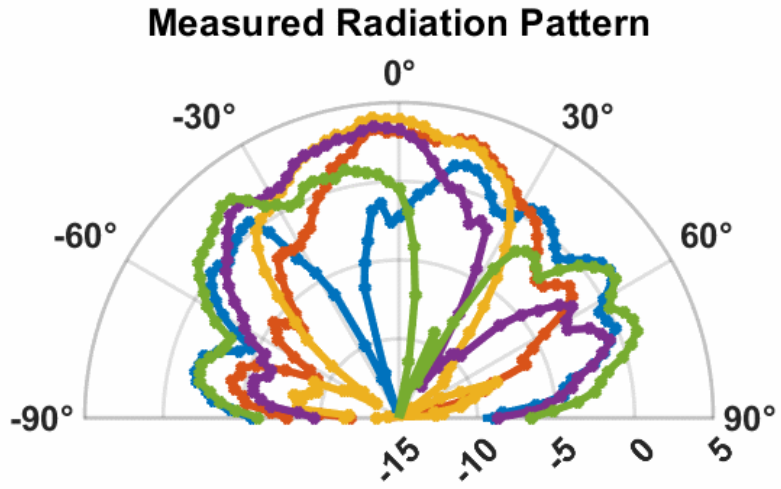




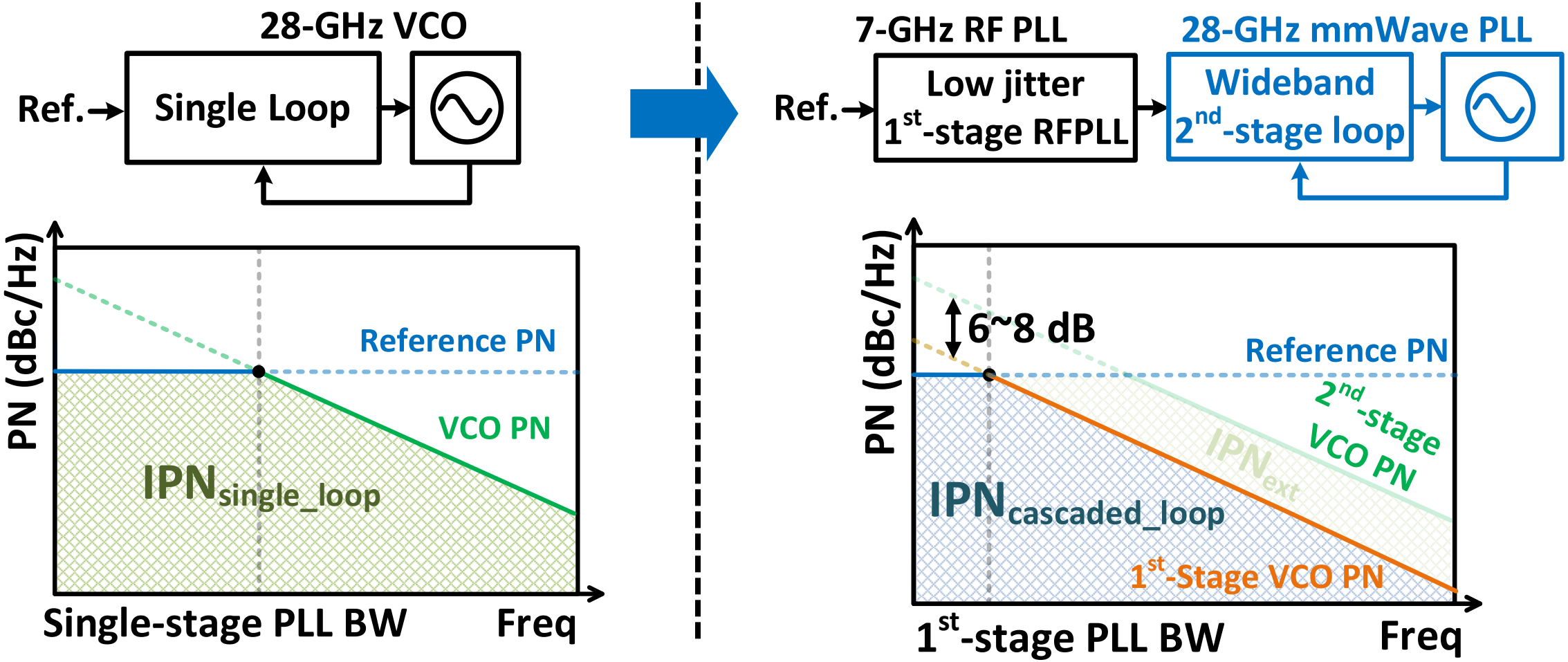
• Beamsteering Demo



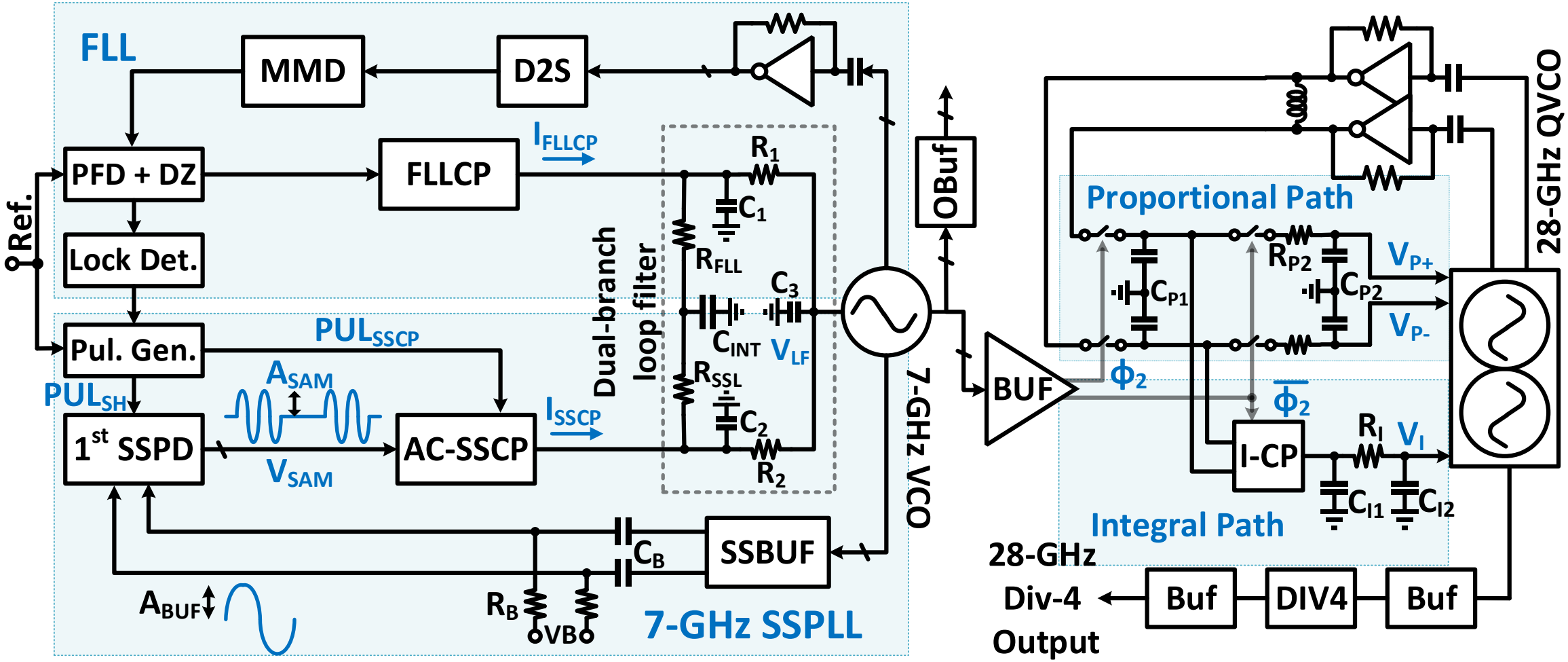




Ka-Band Cascaded QPLL



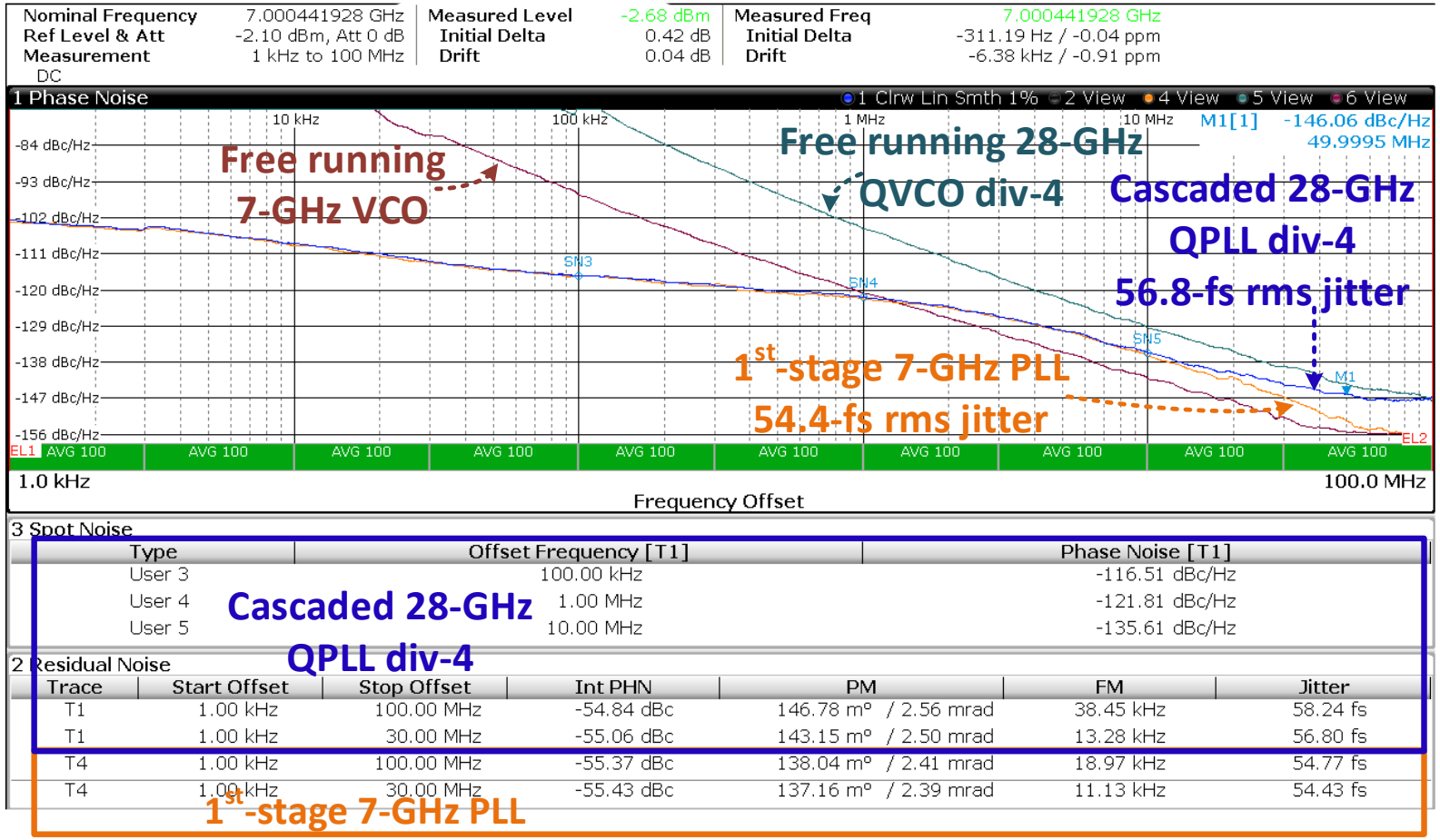
28GHz Dual-Loop PLL Architecture



[1] L. Wang, and **C. P. Yue**, VLSI 2023, Kyoto, Japan.

Experimental Results

- The 1st-stage RF SSPLL dominates the overall jitter
  - 1st-stage contributes 54.4-fs out of 56.8-fs total rms jitter
  - High frequency VCO phase noise is sufficiently attenuated
  - Over 1 kHz to 100 MHz range, QVCO PN profile is well above QPLL



Performance Comparison

	Hu ISSCC20	EK JSSC18	Yang ISSCC22	Du VLSI21	Kim JSSC19	Liao JSSC20	This work
Tech	28nm	28nm	7nm	28nm	65nm	45nm	40nm
Arch.	CS + Harmonic extraction	Single-stage	Harmonic mixing	Harmonic extraction	Cascaded SS+QILO	Cascaded RSPLL+ ILFM	Cascaded SS+DP-SS
Freq. (GHz)	21.71~ 26.49	23.3~ 30.2	25~28	24~31	28~31	33.6~36	24.0~ 29.8
Freq. range	19.3%	25.8%	11.3%	25%	10.1%	6.9%	**21.4%**
Ref. (MHz)	250	491.5	74	50	100	80	250
Jitter (fs)	75.89 (10k~30M)	114	88	199 (10k~30M)	76 (1k~30M)	251 (10k~10M)	**56.8 (1k~30M)**
Spur (dB)	-45	-65.1	-61	-65	-58	-60	-55.6
Pdc (mW)	16.5	31	12.9	11.5	41.8	20.6	42. 1
FoM_{jitter} (dB)	-250.2	-244	-250	-243.3	-246.1	-238.9	**-248.6**
$FoM_{jitter-N}$ (dB)	-270.4	-261.2	-275.8	-270.9	-270.7	-265.3	-269.1
Area	0.5	N. M.	0.24	0.3	0.32	0.41	0.4

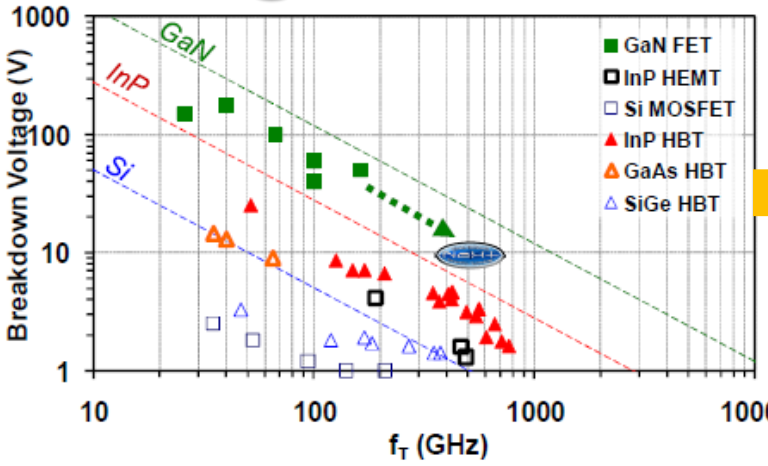
High-SPLIQ IC Needed for the New Era

High-Speed + High-Power

K. Shinohara, "III-Nitride millimeter wave transistors", Chapter 4 in *III-Nitride Electronic Devices*, Elsevier (2019).

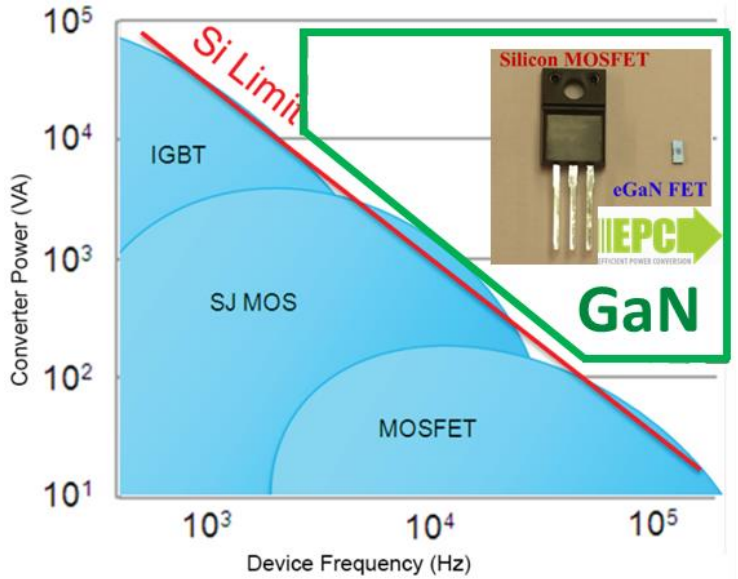
GaN for mmWave

J. Albrecht *et al.*, IEEE CSICS (2010).



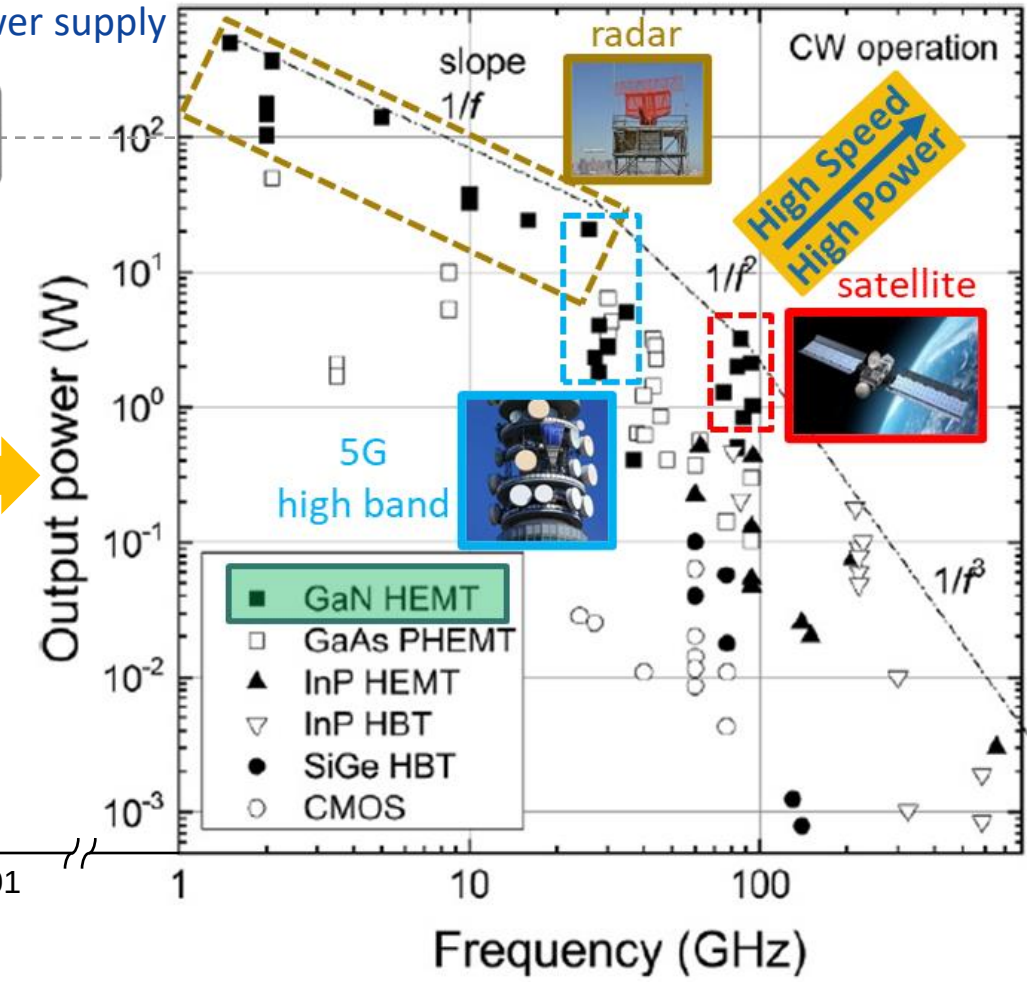
GaN for power management

I. C. Kizilyalli *et al.*, "Wide band-gap semiconductor based power electronics for energy efficiency" (ARPA-E, Washington DC, 2018)

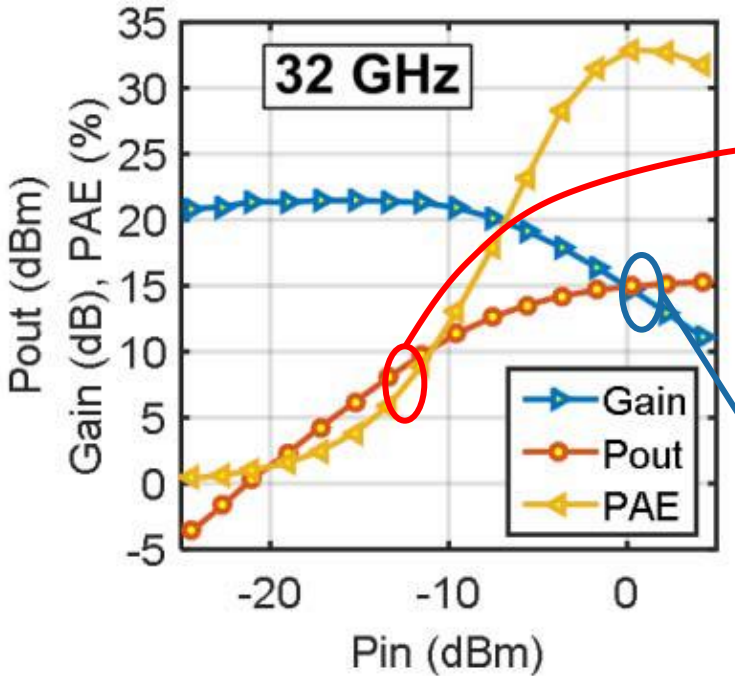


Charger and power supply

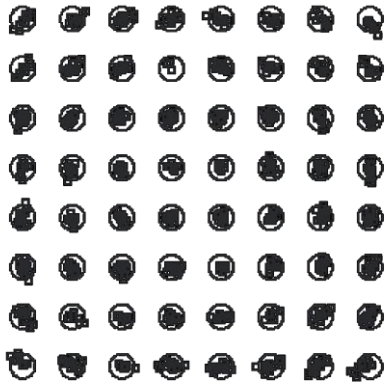
HIGH5 SEMI



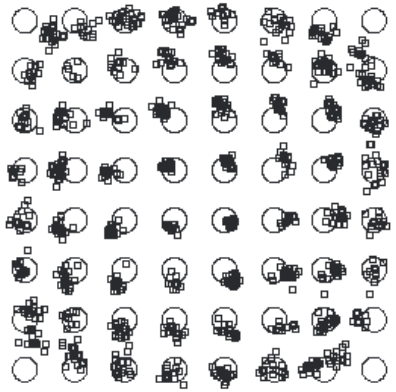
High-Linearity



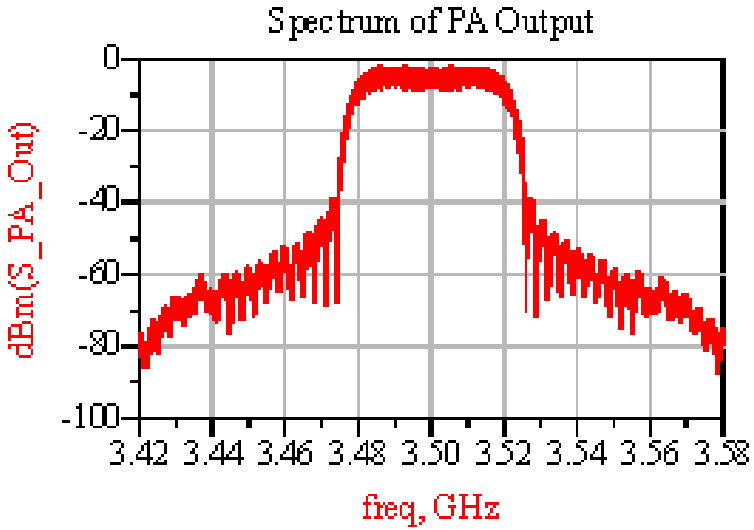
Large signal performance of a mmWave power amplifier (PA), including P_{out}, Gain and PAE



QAM-64 constellation with low EVM



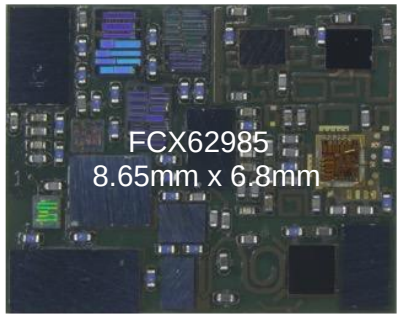
QAM-64 constellation with high EVM (bad linearity)



ACPR from ISEE (Integrated System Engineering Evaluator), a simulation platform developed by OWL)

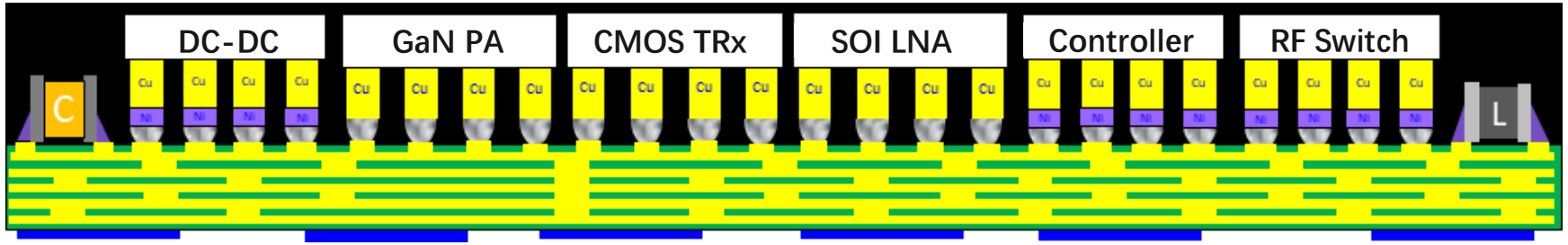
https://github.com/HKUST-ECE-IC-Design-Center-OWL/ISEE-Complex-Signal-Co-simulation-Platform-For-Intergrated-Circuit-and-System-Design

High-Integration



Compact Package

- Designed to achieve highest-level of integration in a small form-factor and includes multiple functions IC with multiple processes
- This RFFE SiP includes 56 SMDs, 9 Acoustic filters, 4 HBT PAs, 2 SOI Switches, 1 SOI LNA, and 1 CMOS controller



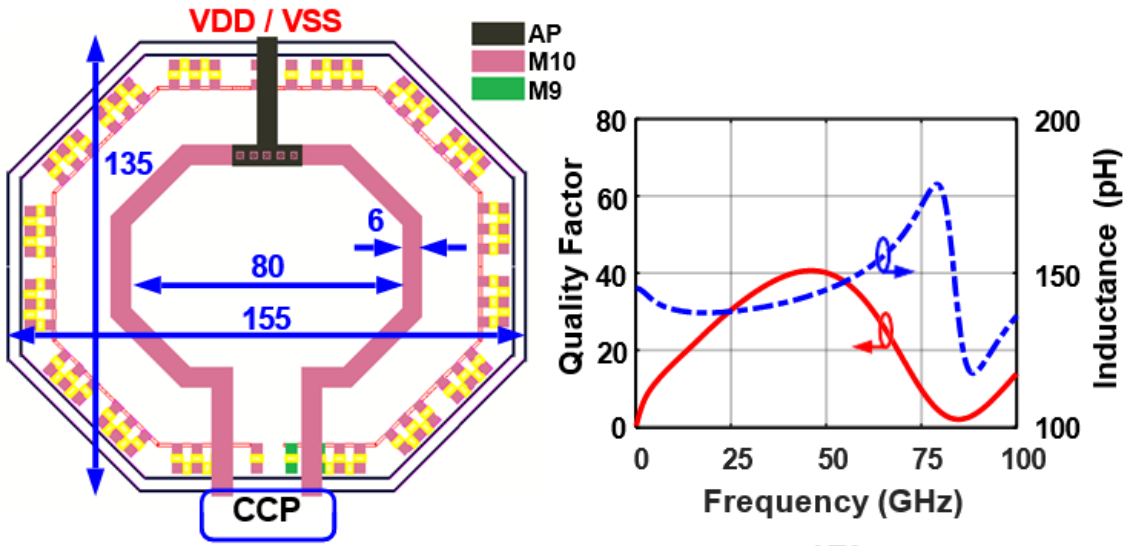
System-in-Package

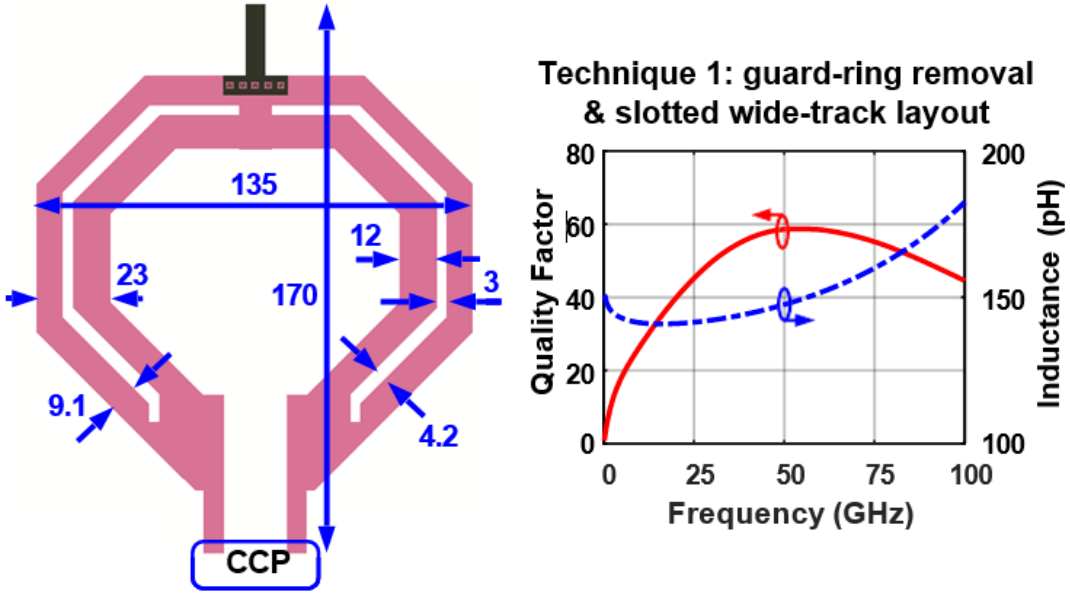
- High power dissipation device like DC-DC converter and GaN PA in the same package
- Multiple-tech chips in a single package

High-Voltage High-Power Buck Boost Converter

- EPC 140W Micro SmartPower
- Type-C Bidirectional PD3.1/Max 140W
- Type-A multi-channel fast charging
- Intelligent power allocation for multi-port high-power charging
- Built-in dual DC-DC
- Supports 2C1A independent fast charging
- Supports dual PD3.1 simultaneous charging and discharging
- Solar energy charging
- 28V-5A discharge; 28V-2A charge
- Multiple over-voltage, over-current, and over-temperature protection

High-Quality Factor Passives





Directly using PDK inductor

- L = 138 pH
- Q = 33

Custom-design optimized inductor

- L = 153 pH
- Q = 47 (42% higher)

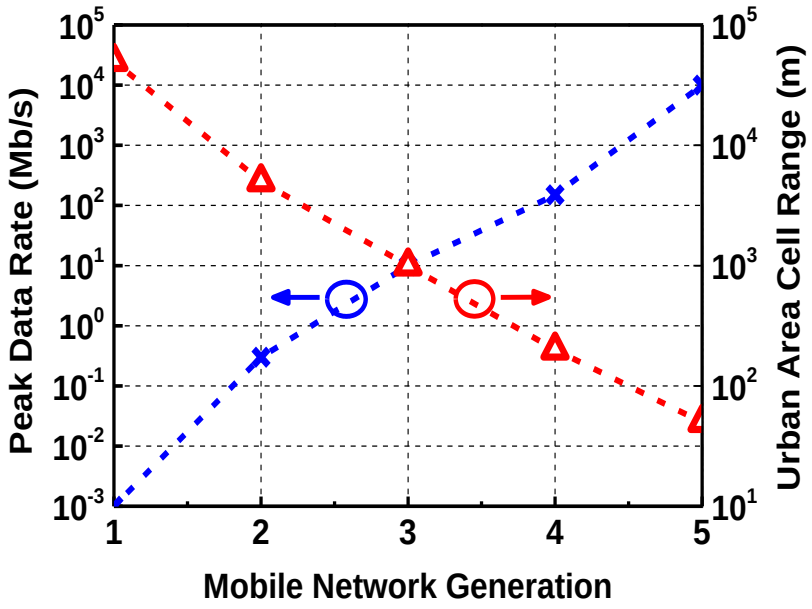
Trade-off between Q factor, inductance density, and power handling capability

New Potential Applications in the 6G Era

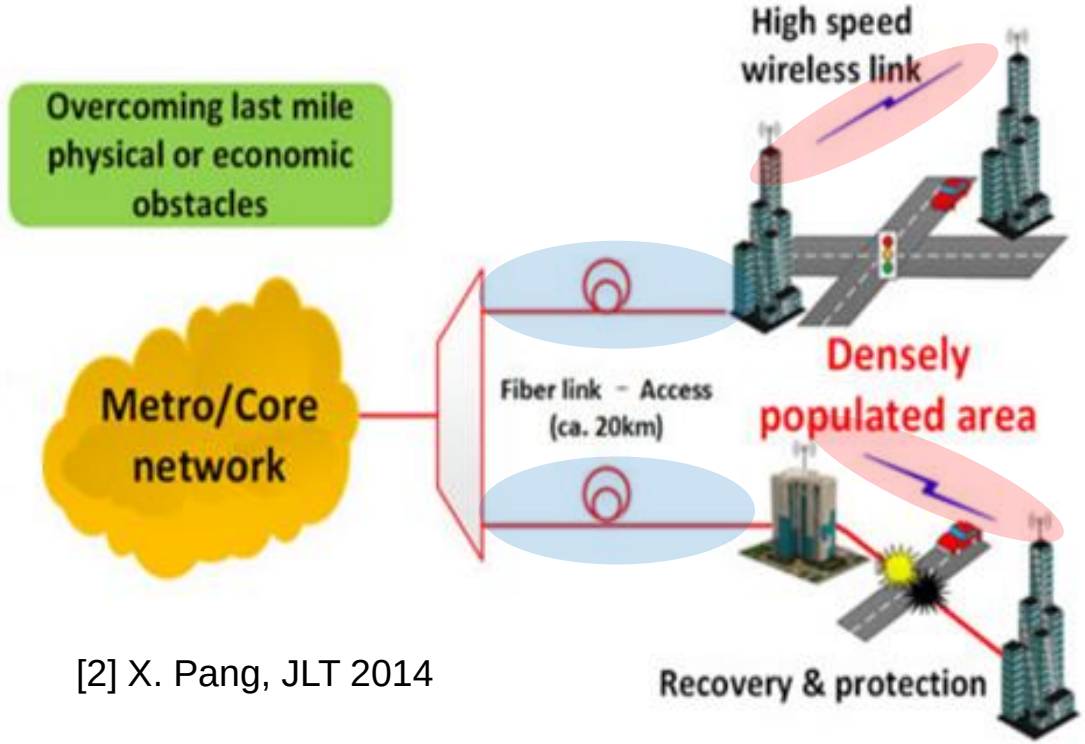
New Opportunities: Optical-Wireless Hybrid Link

- **Fiber-Wireless Hybrid Network: Cascaded Topology**

Evolution of Cellular Networks



Fiber-Wireless Network

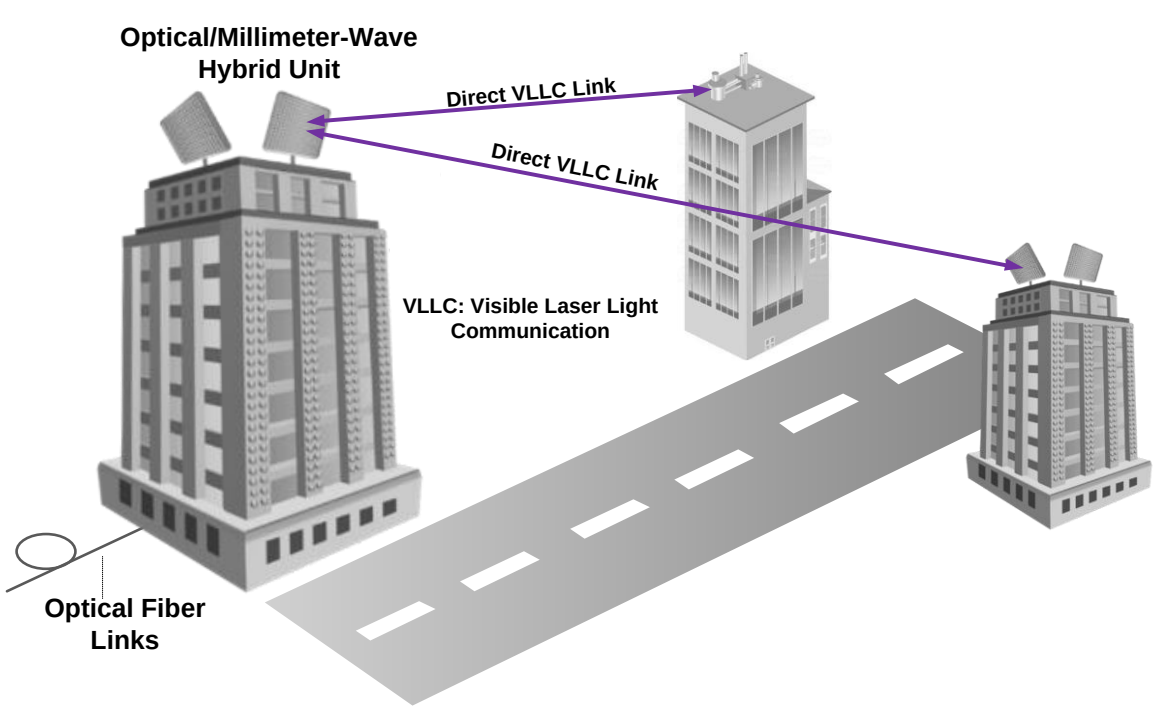


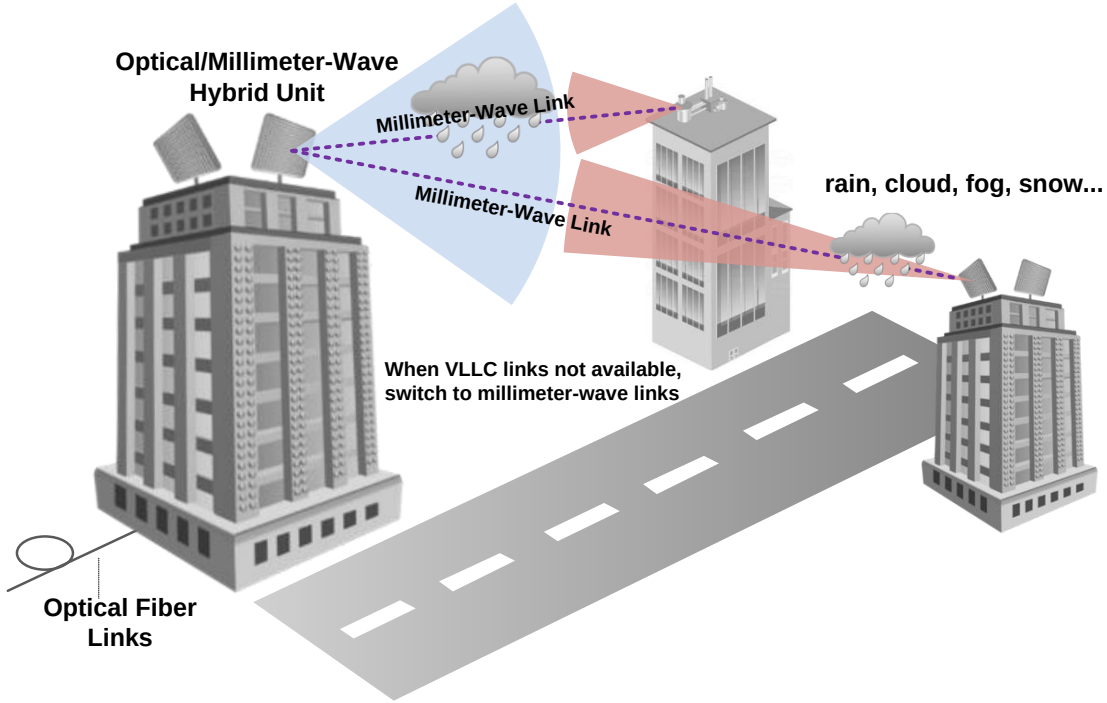
[2] X. Pang, JLT 2014

- **5G mobile network requires ultra-dense cellular cells**
- **Backhaul links deployment is challenging**
- **Fiber-wireless networks provide high performance and flexible backhaul link connections**

New Opportunities: Optical-Wireless Hybrid Link

- **Fiber-Wireless Hybrid Network: Parallel Topology**





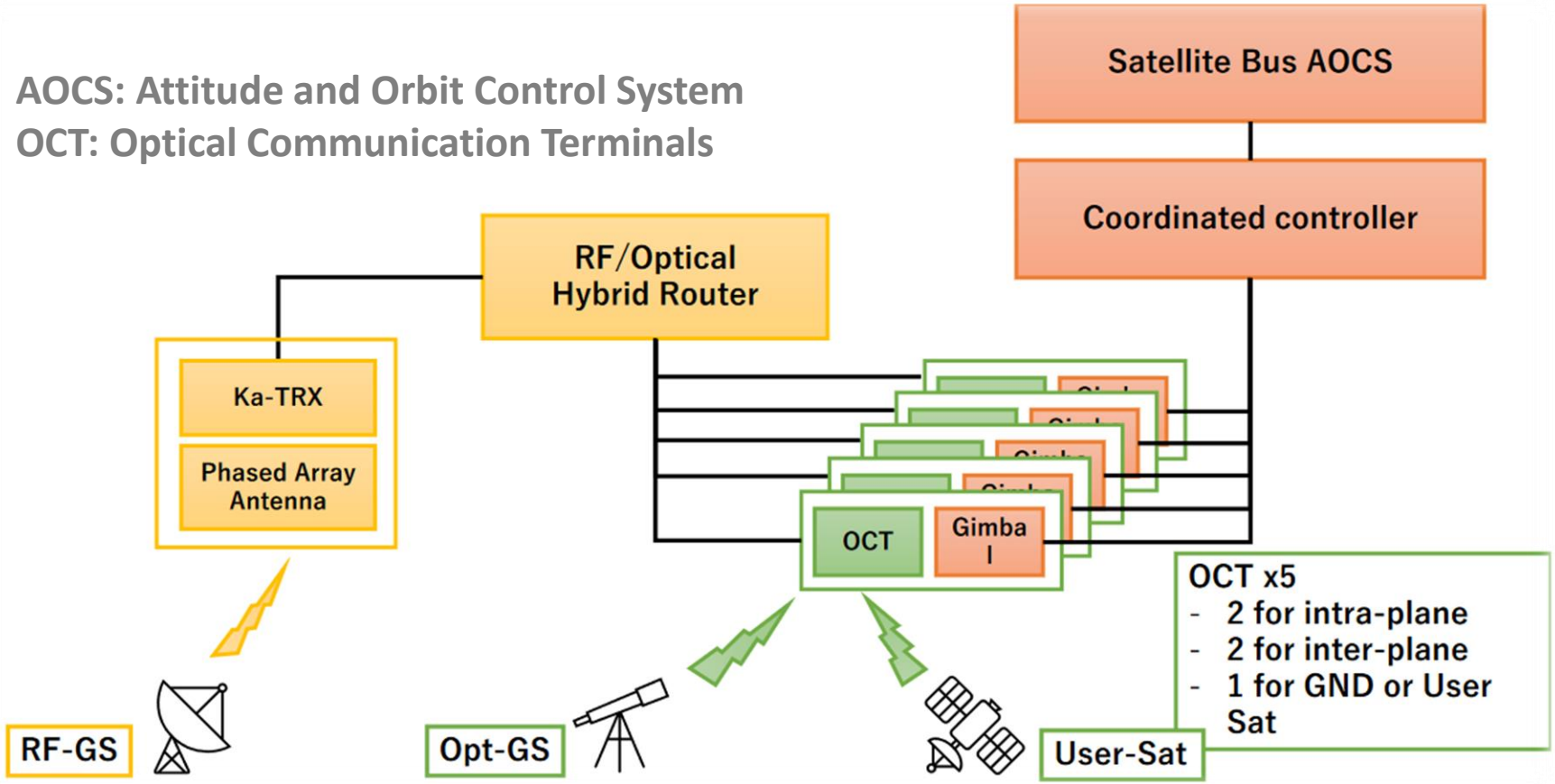
- Under good weather condition: mmWave + Optical in parallel
- Under bad weather condition: mmWave only

Optical-Wireless Hybrid Link for SatCom

Mixed usage of OWC and mmWave links for LEO SatCom

- Optical: communication between satellites
- mmWave: between satellite and ground base station

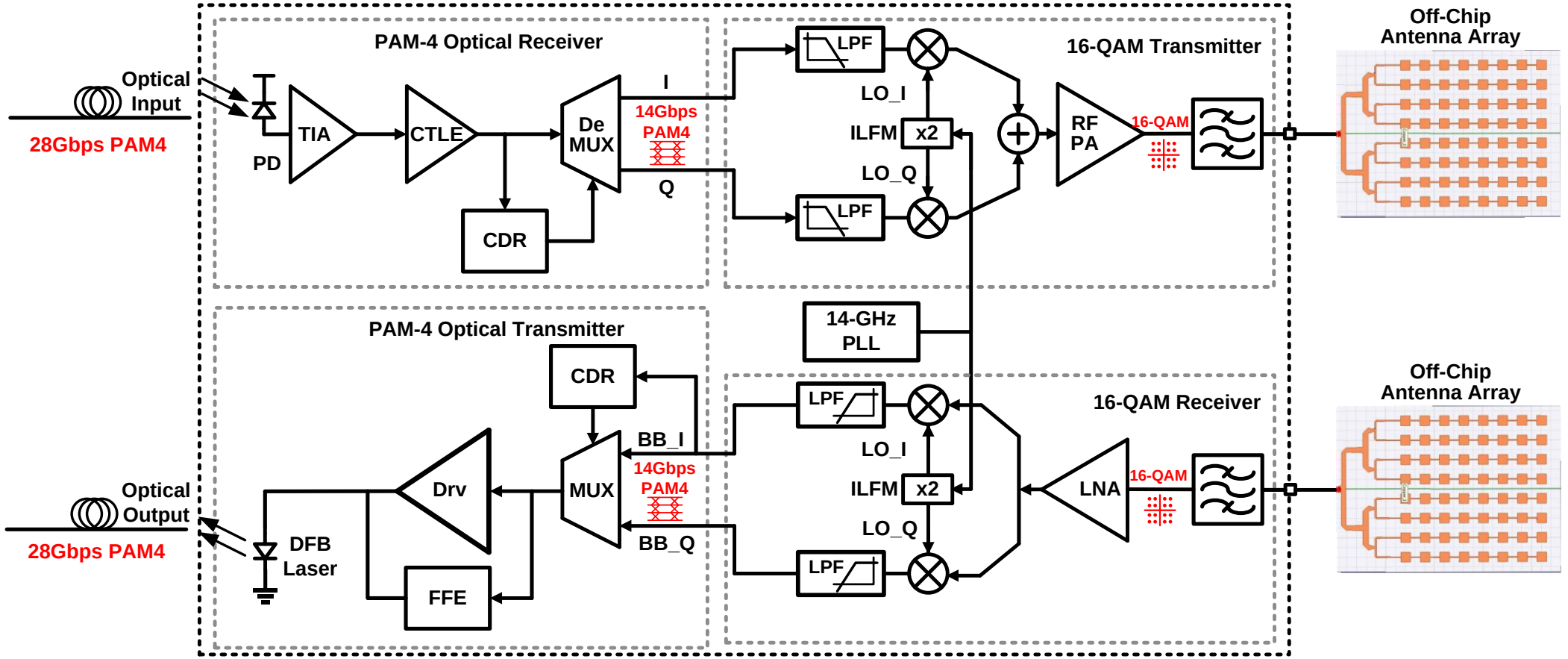
AOCS: Attitude and Orbit Control System
OCT: Optical Communication Terminals



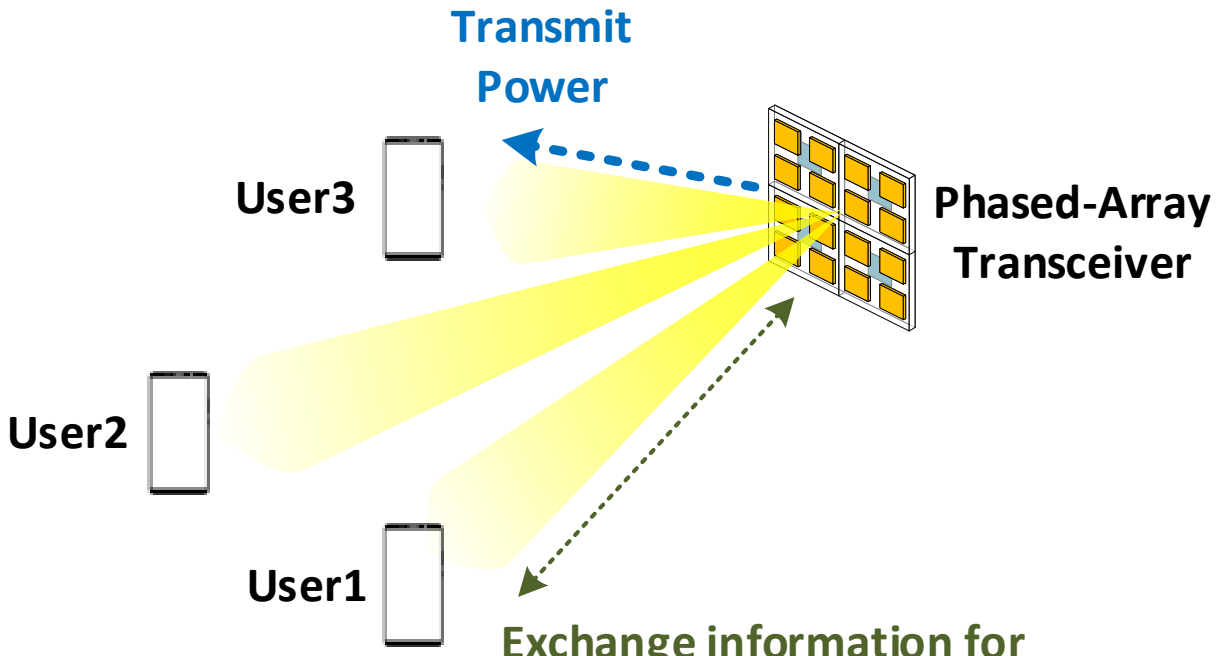
[Okada. Tokyo Tech]

Optical-Wireless Hybrid Transceiver Architecture

- **Optical-In-mmWave-Out + mmWave-In-Optical-Out**



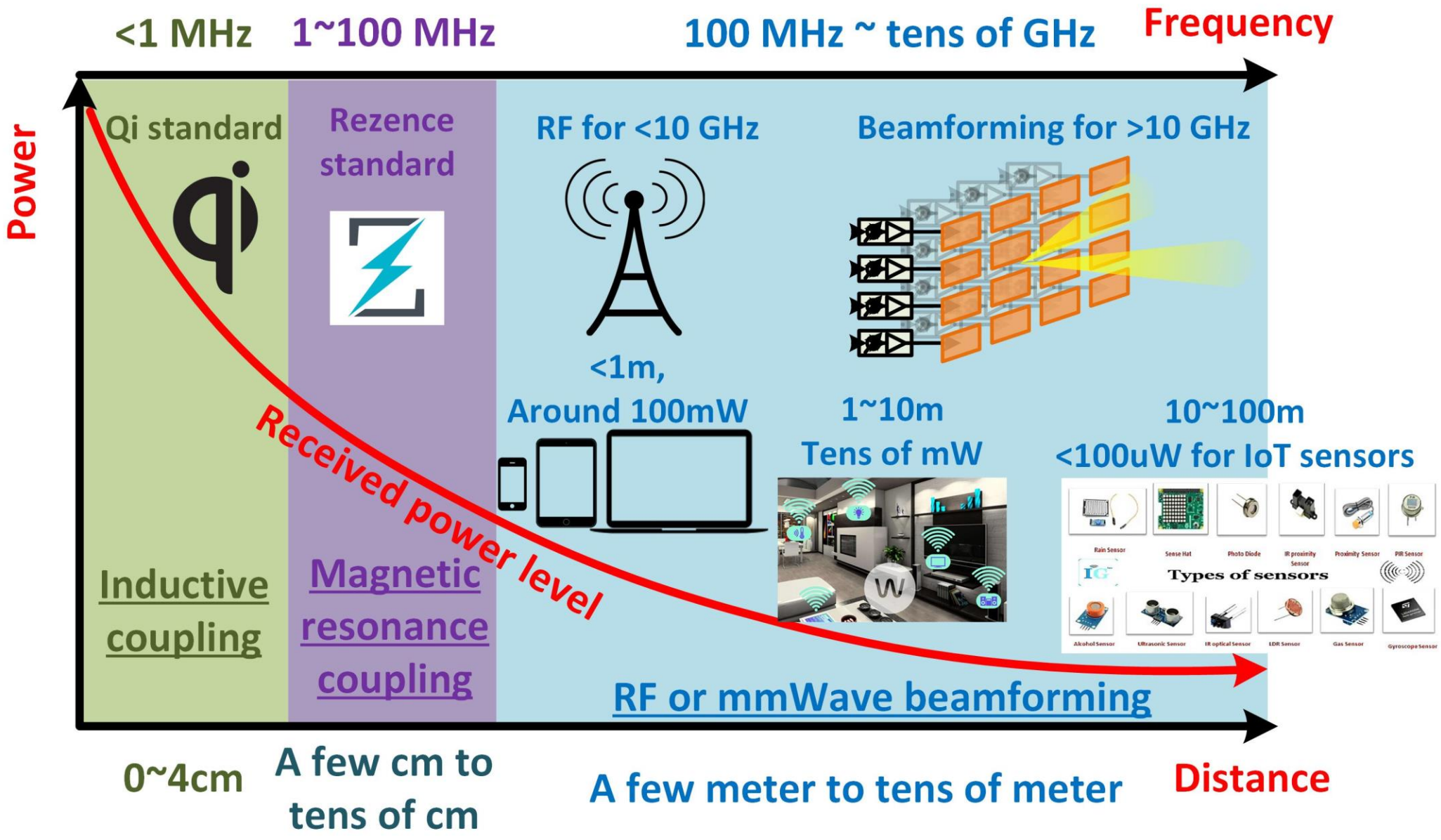
Simultaneous Wireless Information and Power Transfer (SWIPT)



Exchange information for

- Adjust beamforming angle
- Adaptive power level control

[Hajimiri, Caltech & Guru]


<1 MHz
1~100 MHz
100 MHz ~ tens of GHz
Frequency
Power
Qi standard
Rezence standard
RF for <10 GHz
Beamforming for >10 GHz
<1m,
Around 100mW
1~10m
Tens of mW
10~100m
<100uW for IoT sensors
Received power level
Inductive coupling
Magnetic resonance coupling
RF or mmWave beamforming
Types of sensors
0~4cm
A few cm to tens of cm
A few meter to tens of meter
Distance

6G Technologies & IC Design Research @ HKUST

OWL ICDC ECE HKUST

An Area of Excellence Project (AoE/E-601/22-R)

6G: Wireless Access and Connectivity for an Intelligent and Sustainable World

Project Coordinator:

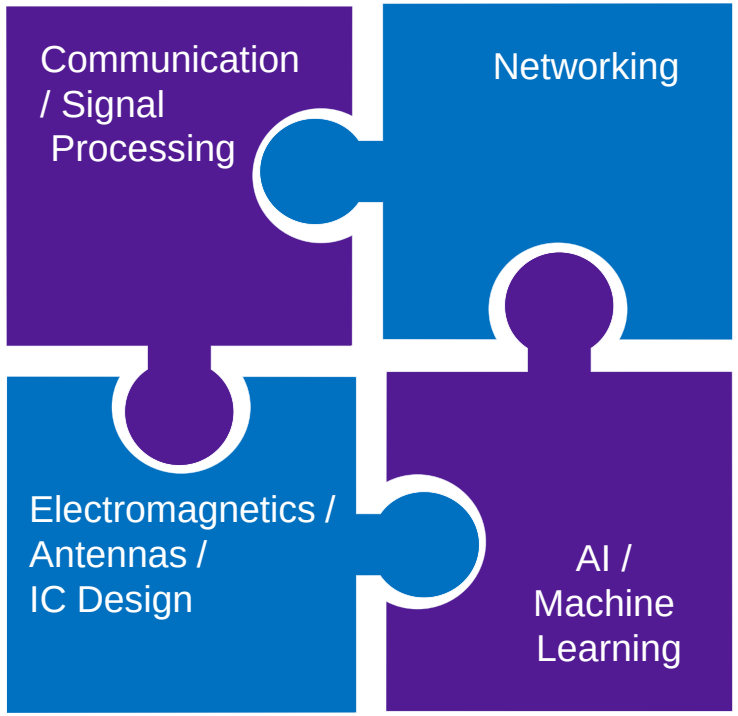
Khaled B. LETAIEF
New Bright Professor of Engineering
Chair Professor
Department of Electronic and Computer Engineering
The Hong Kong University of Science and Technology

Coordinating University:

香港科技大學
THE HONG KONG UNIVERSITY OF SCIENCE AND TECHNOLOGY

Started Jan. 2023 and Supported by the Hong Kong Research Grant Council

The AoE Team



MULTIDISCIPLINARY TEAM WITH COMPLEMENTARY STRENGTHS

香港科技大學
THE HONG KONG UNIVERSITY OF SCIENCE AND TECHNOLOGY

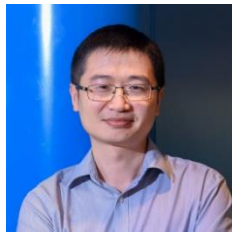

K. B. LETAIEF


R. MURCH


Qian ZHANG


V. N. LAU


Patrick YUE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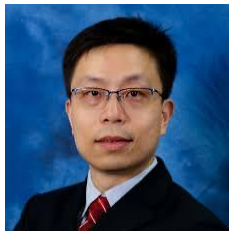
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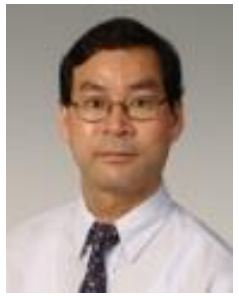

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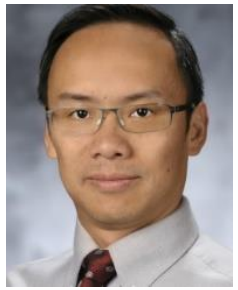

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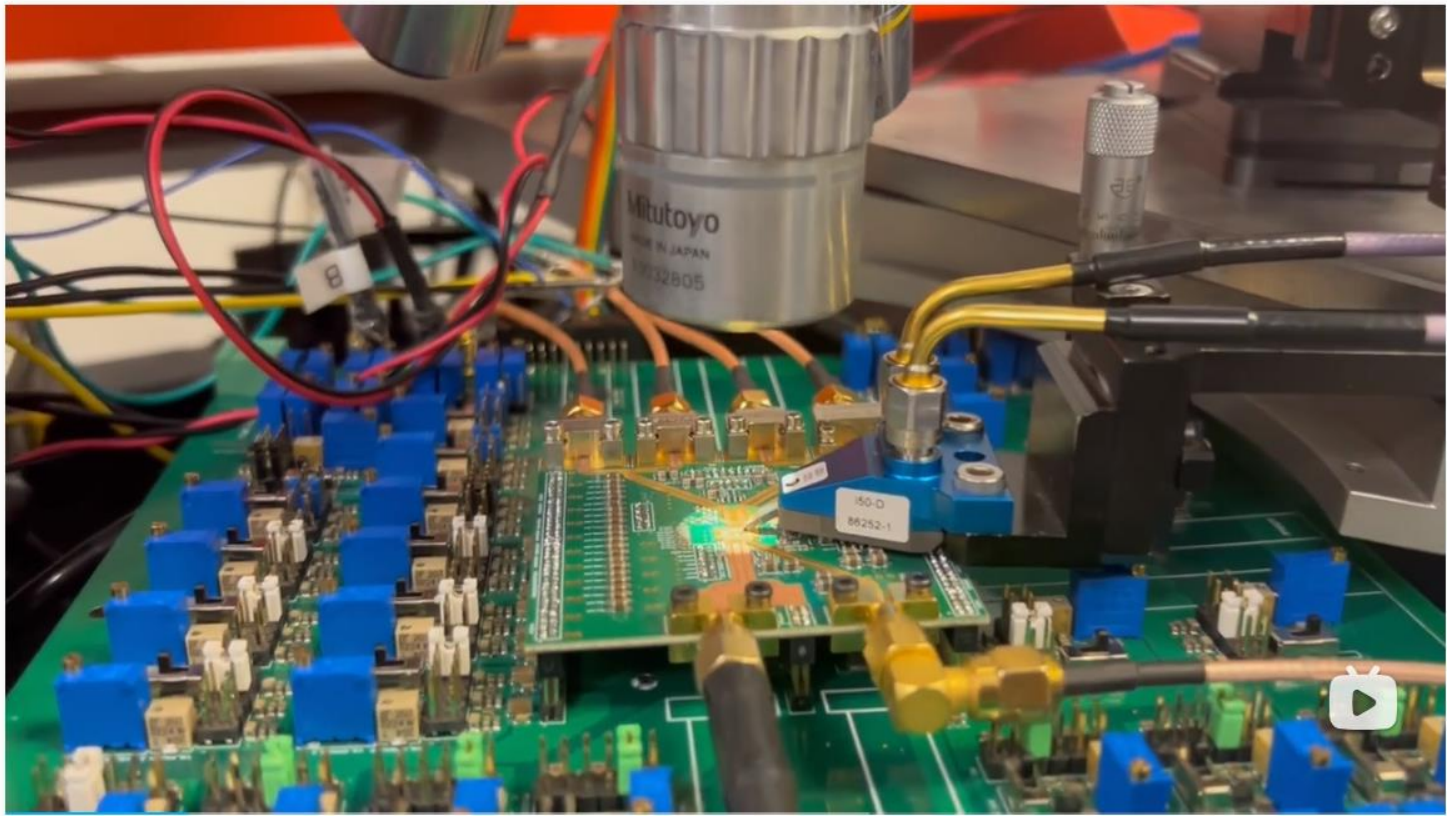

谢谢!

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