

Optical, Wireless, and Optical Wireless Communication and a **Brave Startup**

光、无线、及光无线通信，和一个**勇敢的初创公司**

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Hong Kong University of Science and Technology

OWL



ICDC



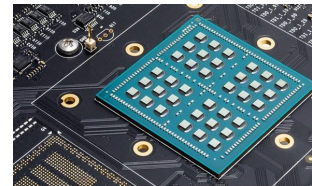
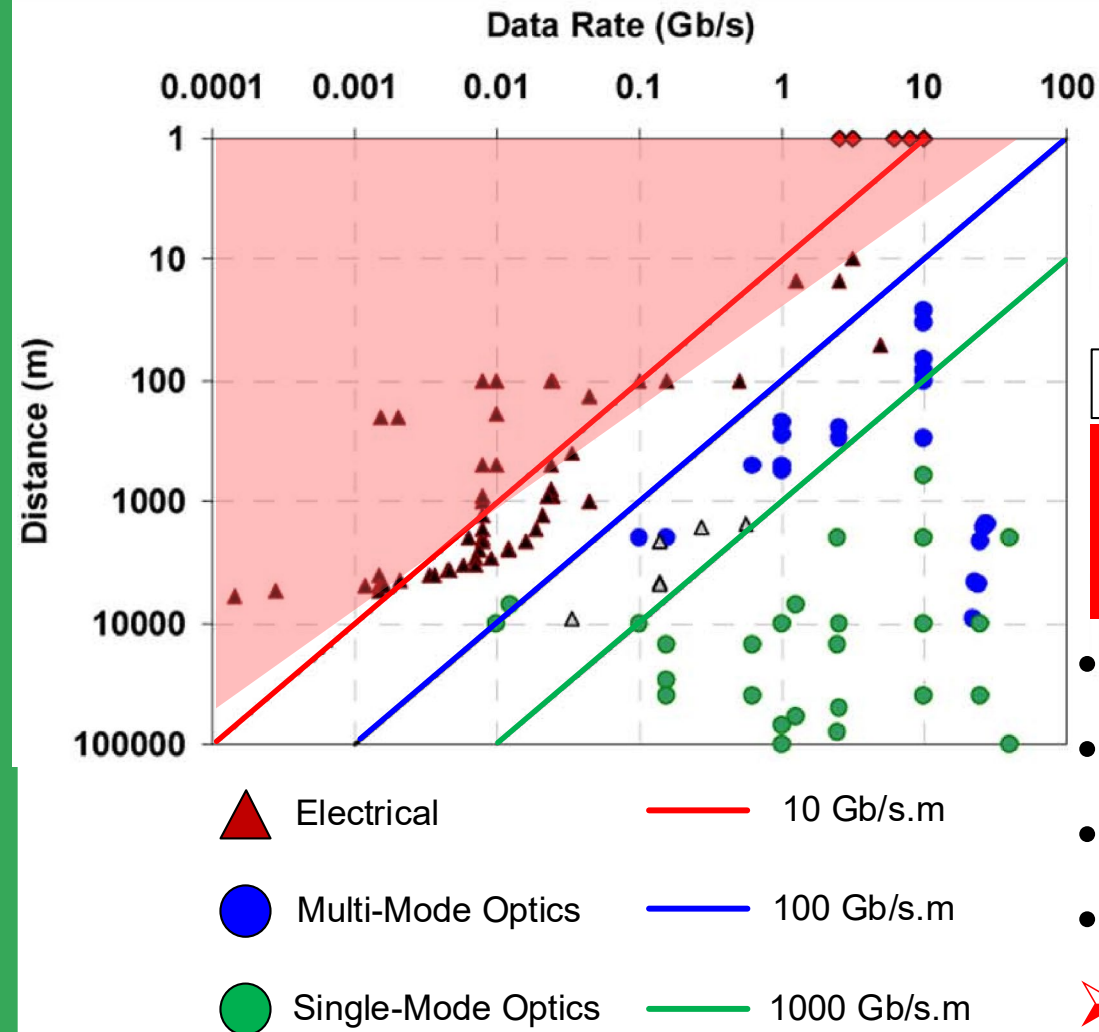
ECE



Outline

- **Optical, Wireless, and Optical Wireless – What? Why?**
- **Optical-Electronic Integrated Circuit (OEIC)**
- **CMOS mmWave Phased-Array IC**
- **High-SPLIQ IC for 6G Era**
- **New Potential Applications in the 6G Era**
- **Summary**

Optical, Wireless, and Optical Wireless



1 cm

Module/Package



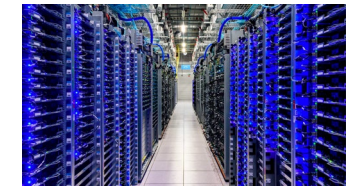
10 cm

Intra-Board



1 m

Intra-Rack



10 m

100 m

Inter-Rack

Electrical

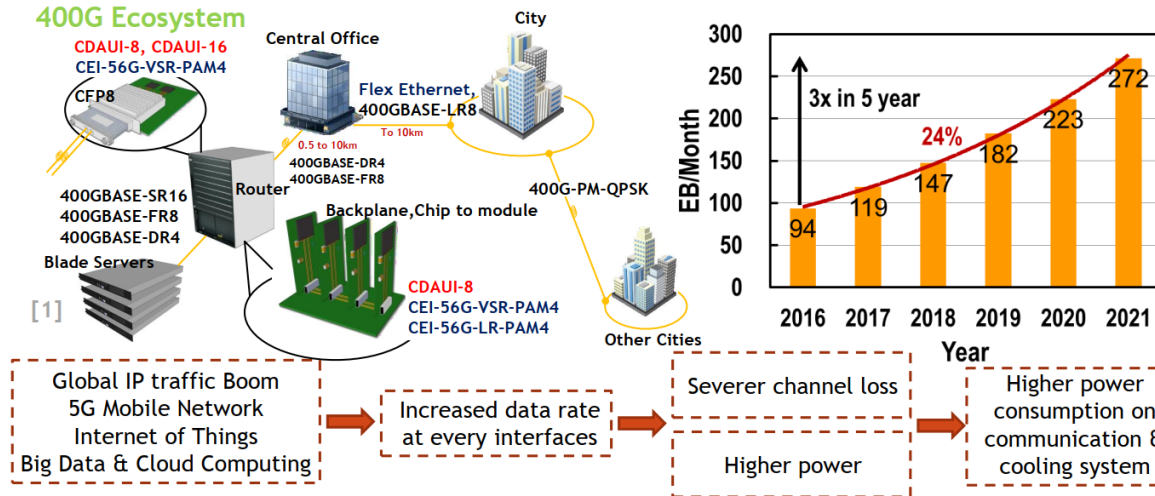
Optics

Multi-mode optics

Single-mode optics

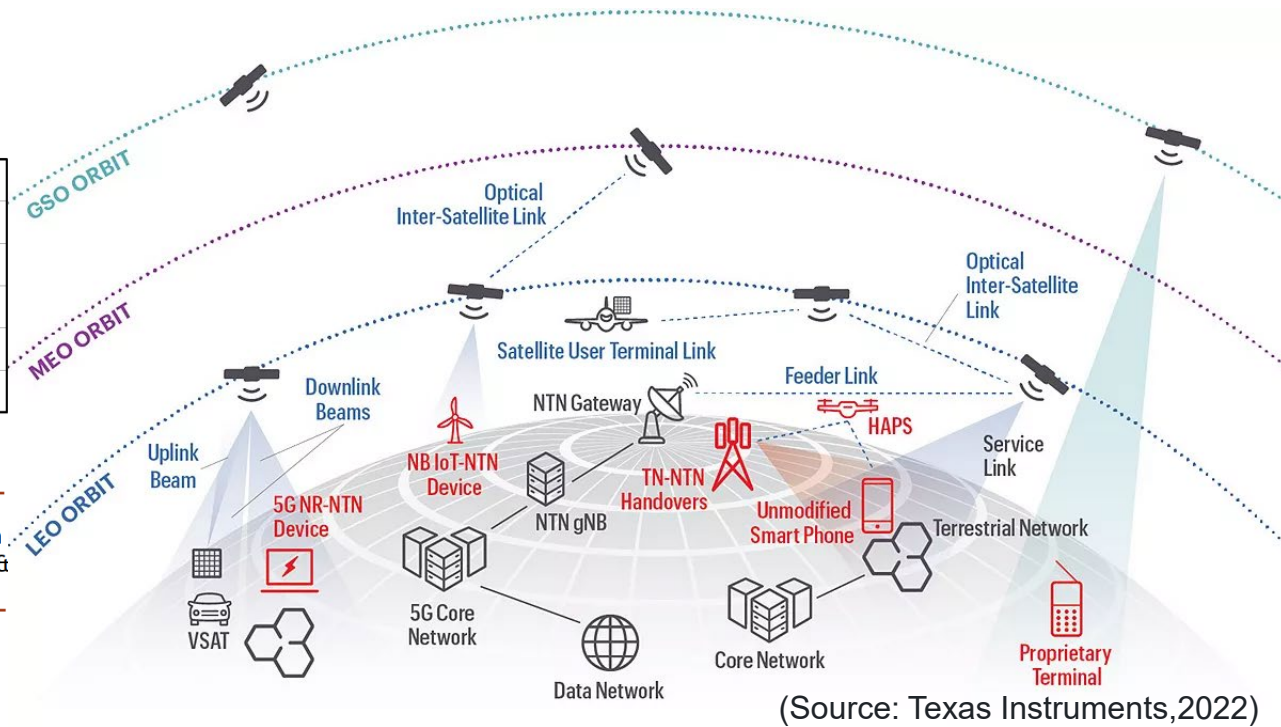
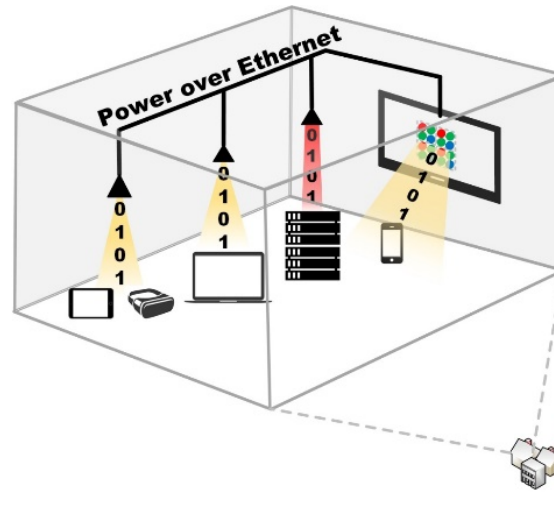
- Copper: high loss, low bandwidth
 - Fibers: low loss, high bandwidth, need OE-EO
 - Optical for Distance X Data Rate $> 100 \text{ Gb/s-m}$
 - Cross-over opportunities!!
- High-Speed OWC, Short-Reach Optical

Ethernet Wireline Link



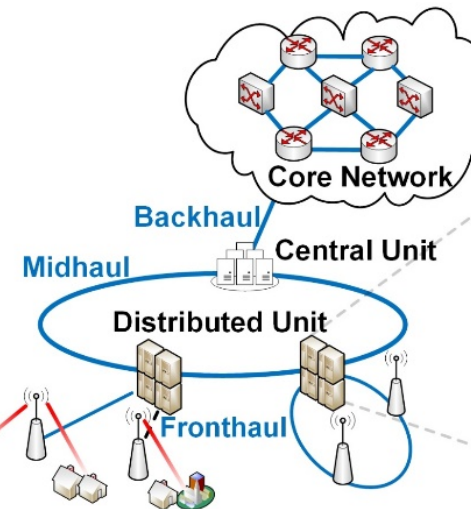
Motivation: Energy efficient high-speed data communication

High-SPLIQ IC and SiP required in advanced enterprise communication applications



Non-terrestrial networks (NTN)

Optical fiber network for 5G network back-, mid-, front-haul connectivity



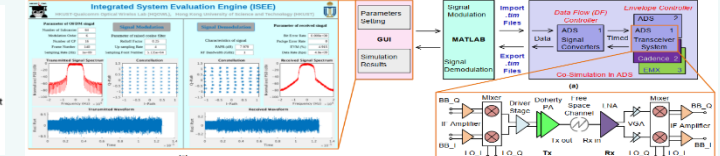
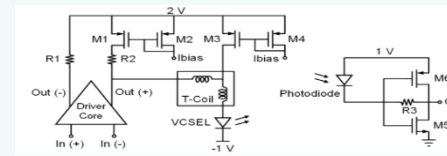


Optical-Electronic Integrated Circuit (OEIC)

CMOS Optoelectronic Interconnect Chip: Architecture Design

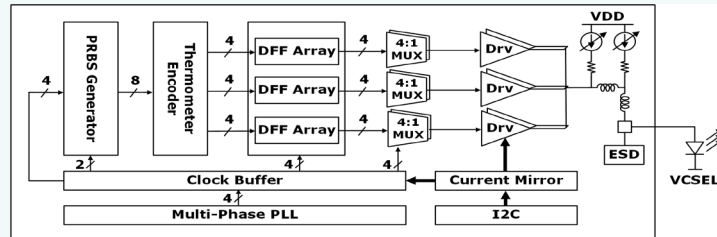
Fully-Integrated System Architecture Design and Verification

1. Top-down system simulation to clarify specifications for each module
2. Multi-chip system simulation throughout the entire design cycle
3. Support complex modulation scheme, like PAM-4, OFDM, QAM



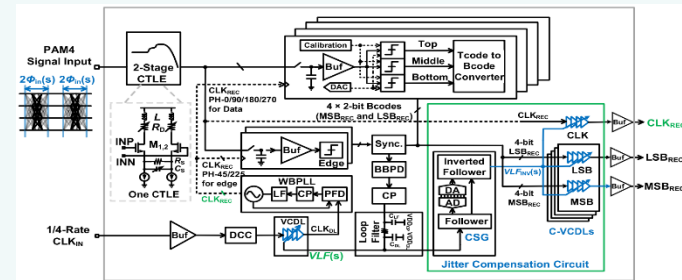
56-Gb/s PAM4 TX

- Data path implements VCSEL nonlinearity compensation
- Clock path has on-chip PLL



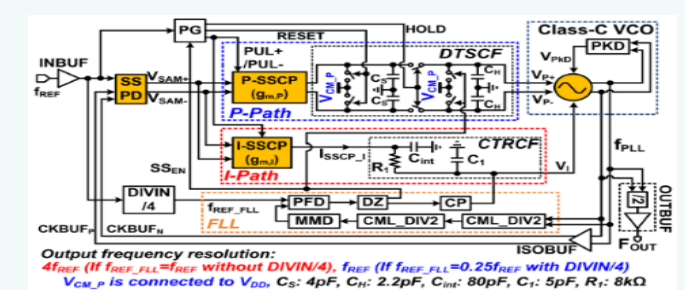
56-Gb/s PAM4 RX

- Signal equalization in frequency domain
- PAM4 signal decoding and clock recovery



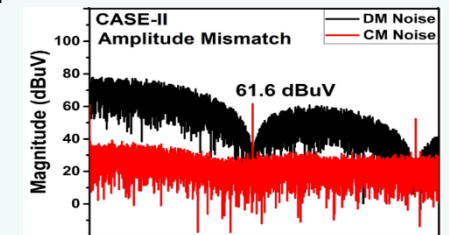
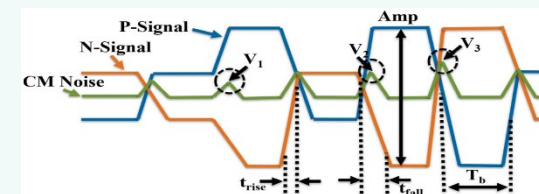
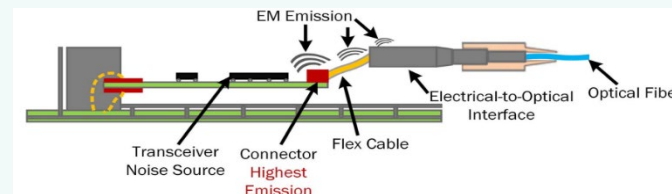
14-GHz PLL

- Sub-sampling PLL achieves low jitter
- Low supply voltage to decrease power



PAM4 Optoelectronic Interconnect Chip EMI Analysis and Cancellation

- Clarify radiation theory of CM noise
- Propose close-loop controlling of CM noise
- Propose CM noise cancellation circuit





广东省重点领域研发项目验收会

面向下一代以太网采用四电平脉冲幅度调制的CMOS全集成光电互联芯片的研究与设计

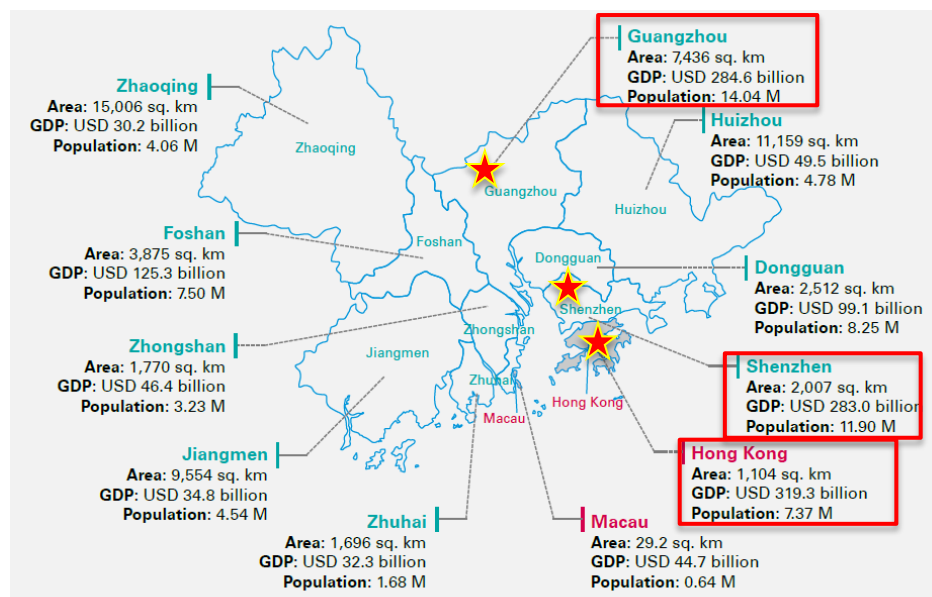
课题负责人：俞捷

课题汇报单位：香港科技大学

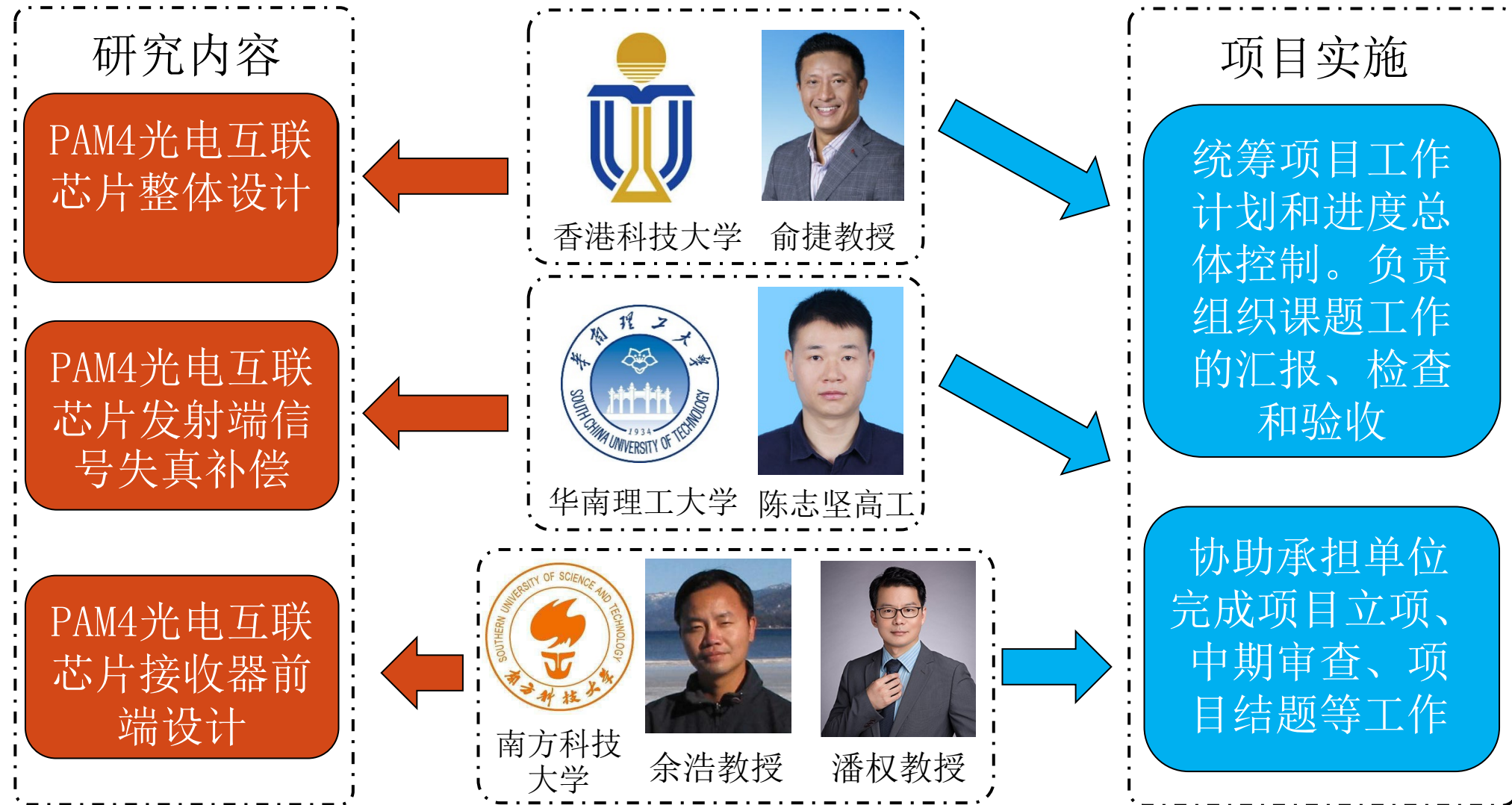
参与单位：

华南理工大学、南方科技大学

2024. 01. 22

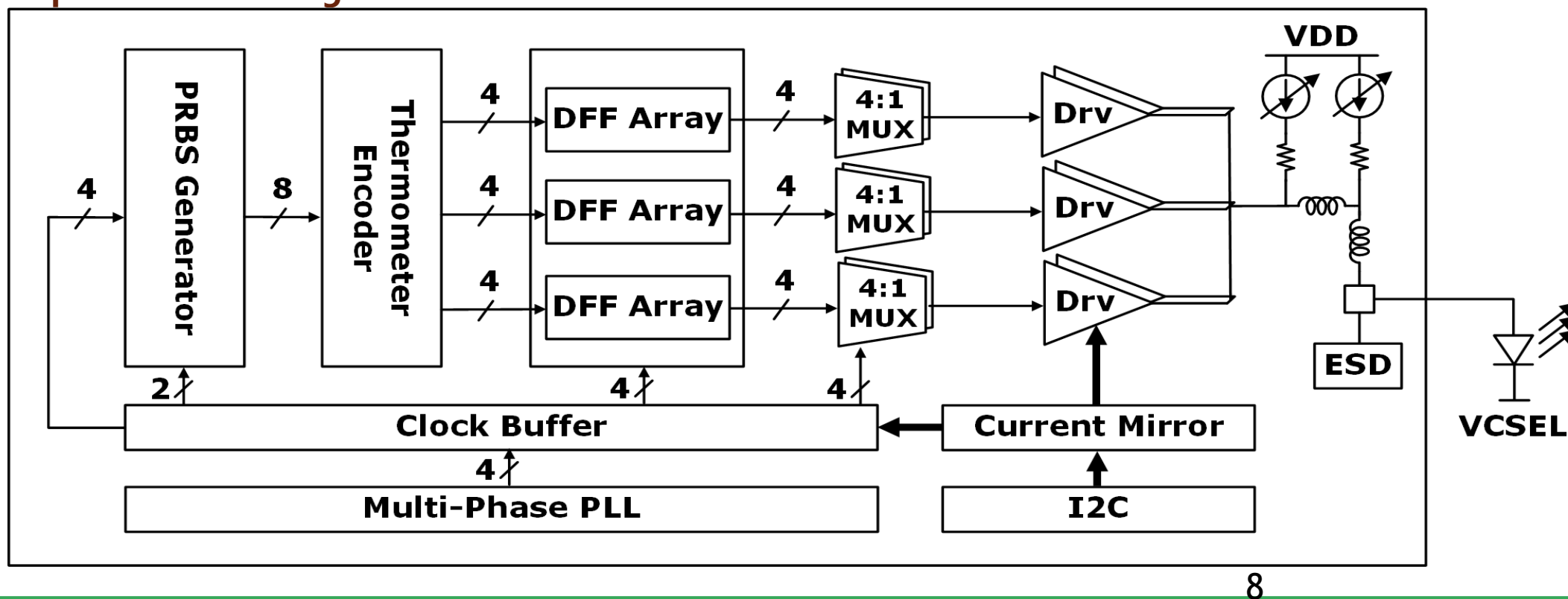


项目分工



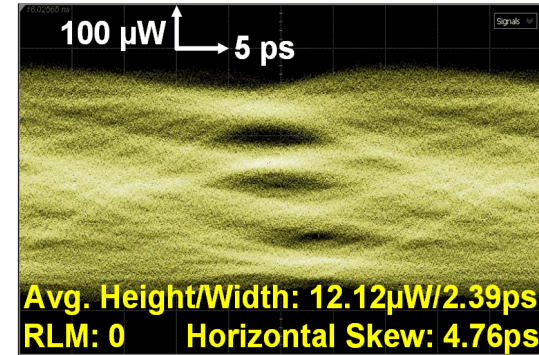
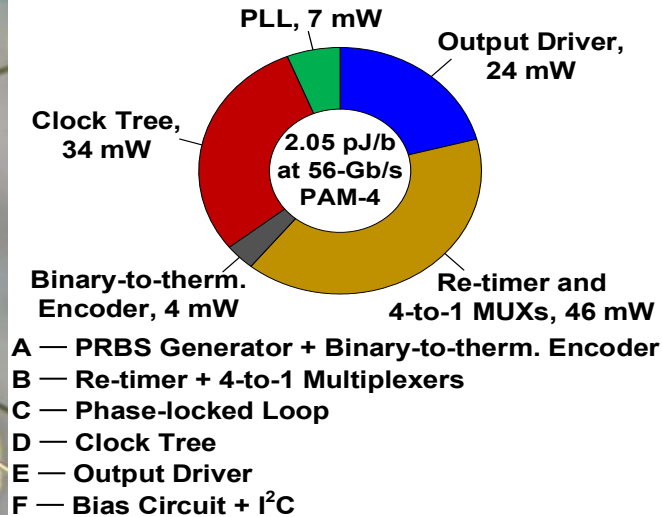
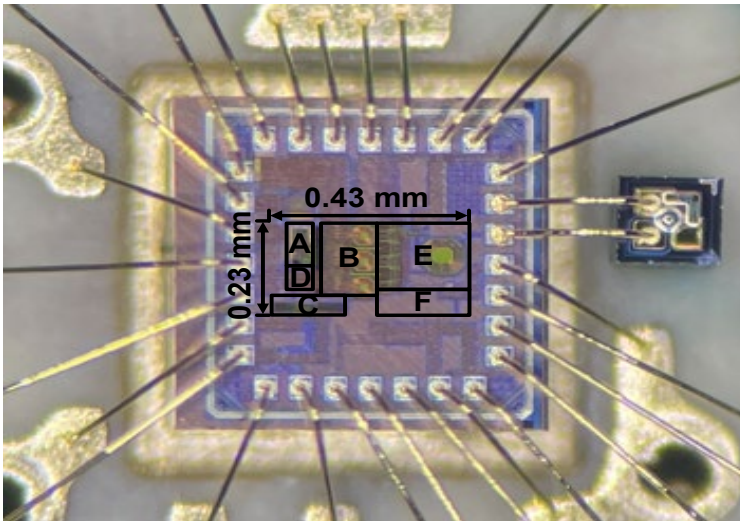
High-linearity 56-Gb/s PAM4 TX chip

- Based on 4-to-1 MUX, including data path, clock path, and bias and control part
- Data path: adopting thermometer code-based architecture for piecewise compensating E/O gain and bandwidth nonlinearities
- Clock path: multi-phase PLL to generate 8-phase clock
- On-chip PRBS for testing

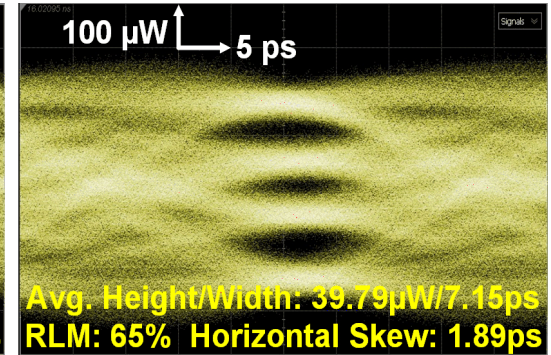


High-linearity 56-Gb/s PAM4 TX chip: 4-2-1 MUX design

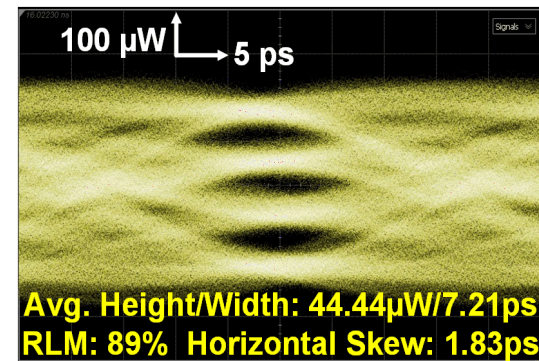
- Implemented in 40nm CMOS, 0.1 mm² of core area
- Tuned slice EQ and slice gain to compensate for the VCSEL nonlinearity



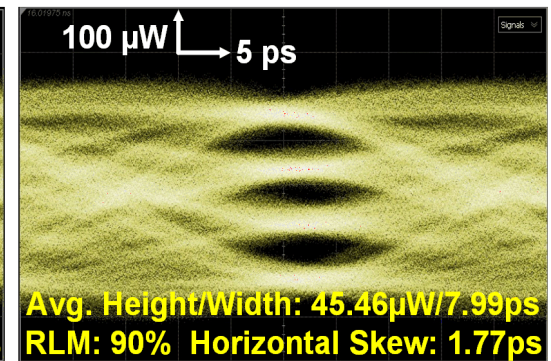
(a) EQ OFF, Equal Slice Gain



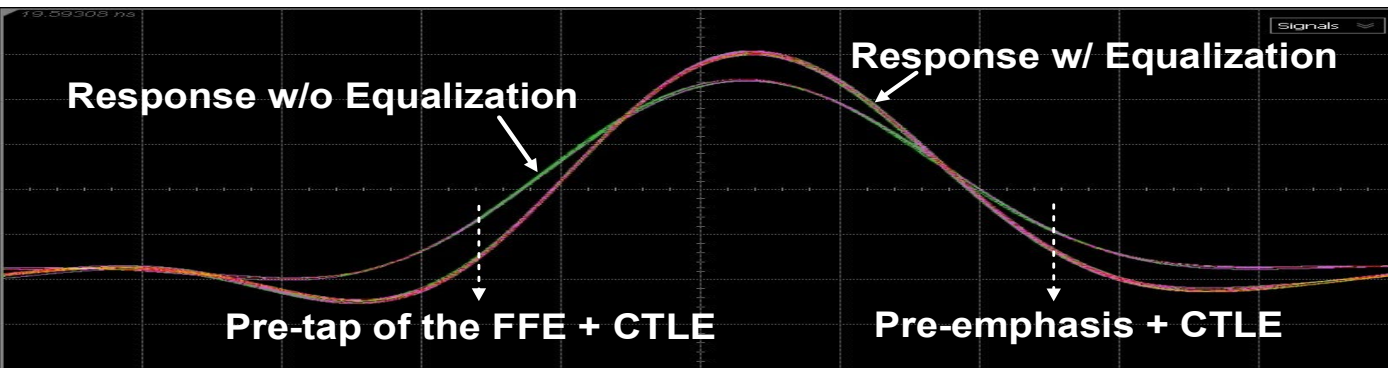
(b) Equal Slice EQ and Slice Gain



(c) Equal Slice EQ, Piecewise Tuned Slice Gain



(d) Piecewise Tuned Slice EQ and Slice Gain



• **测试指标** (经第三方检测报告认定) 与**任务书指标**对比

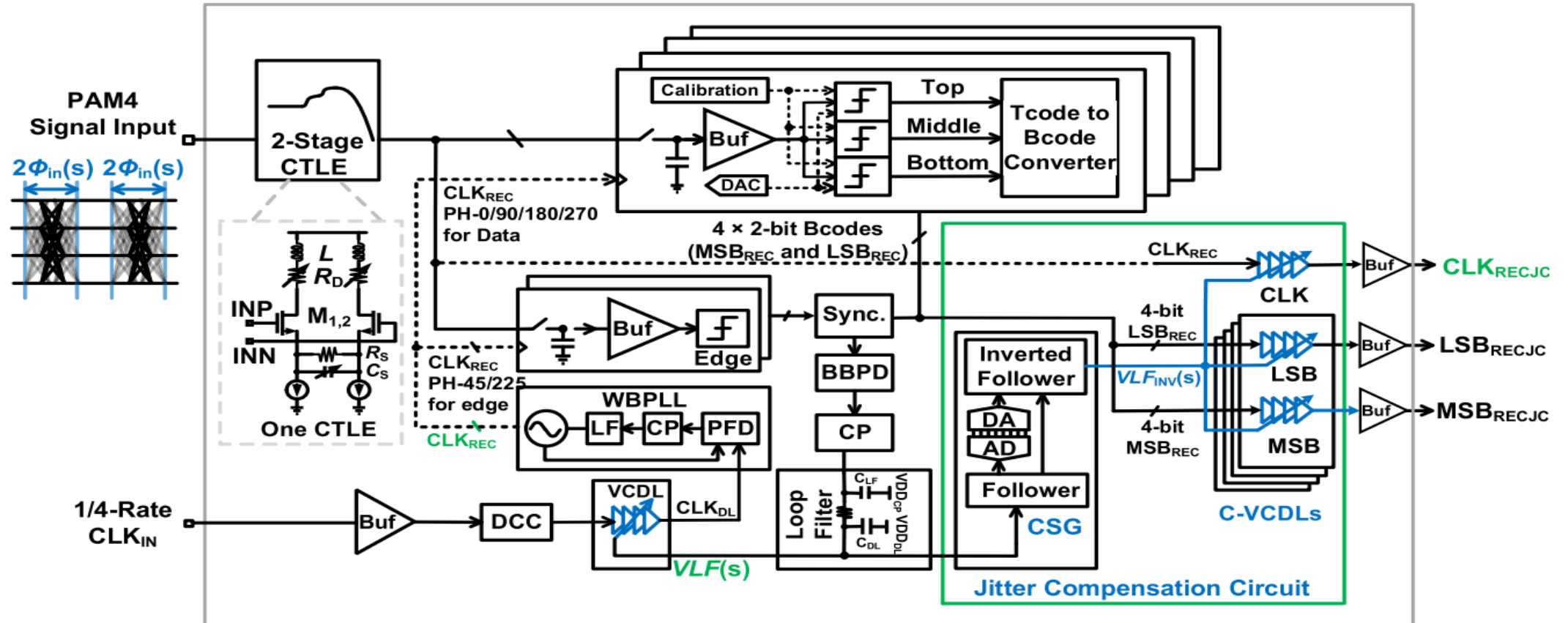
技术指标名称	任务书指标	实测指标	是否满足
速率	≥ 56 Gbps	56 Gb/s	完成
功耗	< 400 mW	152 mW	完成

• **测试指标** (经第三方检测报告认定) 与**国内外领先技术**对比

	PTL'18	JSSC'22	VLSI'19	ASSCC'21	This work
Technology [nm]	65	40	65	40	40
Signalling scheme	1/2-rate PAM-4	1/4-rate PAM-4	1/4-rate PAM-4	1/4-rate PAM-4	1/4-rate PAM-4
Date rate [Gbps]	50	56	64	64	56
OMA [mW]	2.00	0.81	2.50	1.08	1.18
Power effi. [pJ/b]	5.12	1.73	2.69	2.09	2.05
Core area [mm ²]	0.31	0.47	0.28	0.16	0.10
Asymmetric equalization	2.5-tap DAC-based FFE	2-tap DAC-based FFE	3-tap LSB/MSB-based Asymmetric FFE	3-tap LSB/MSB-based Asymmetric FFE	2-tap FFE + CTLE + Pre-emphasis
Nonlinearity compensation	Full	Full	Partial	Partial	Full
Method type	Digital	Digital	Analog	Analog	Analog

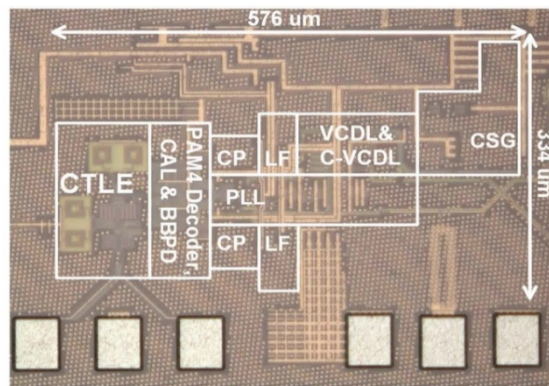
PAM4 RX: signal equalization, decoding, and clock recovery

- Two-stage CTLE to compensate signal in frequency domain
- $\frac{1}{4}$ rate architecture, 3 comparators to adjust top, middle, and bottom eyes separately
- Clock generated by DLL CDR, adopts jitter compensation to improve quality of output data

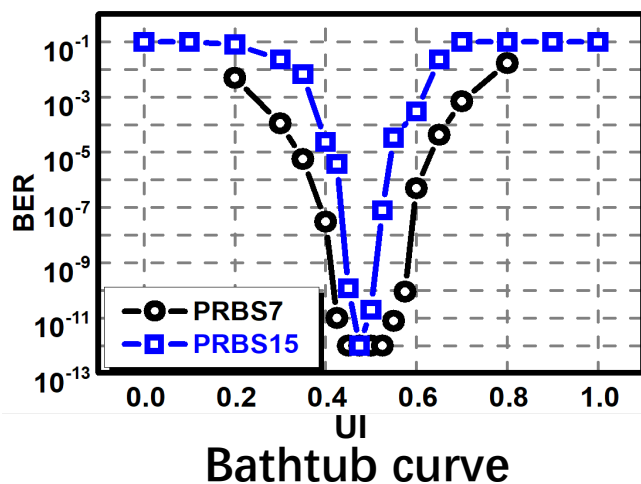


PAM4 RX: signal equalization, decoding, and clock recovery

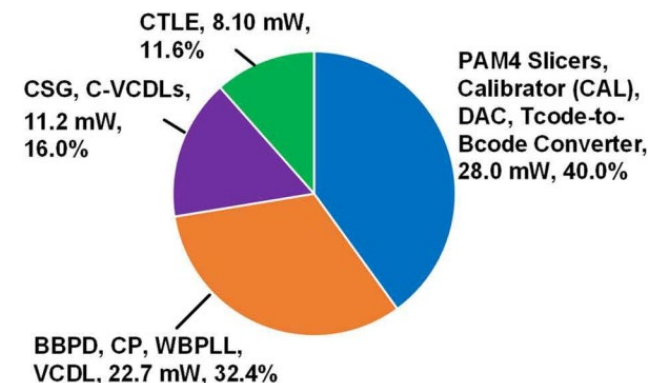
- Implemented in 40nm CMOS technology, 0.58 x 0.34 mm² of core area
- Error-free under 60-Gb/s with PRBS7/15, 70.8 mW of total power



Die photo

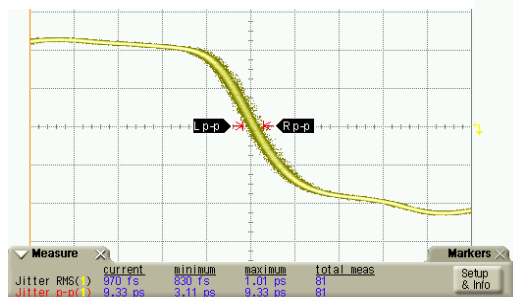


Bathtub curve



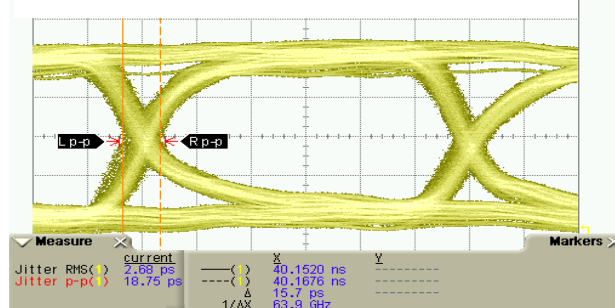
Power breakdown

7.5 GHz CLK_{RECJC}
Jitter_{RMS}: 0.97 ps



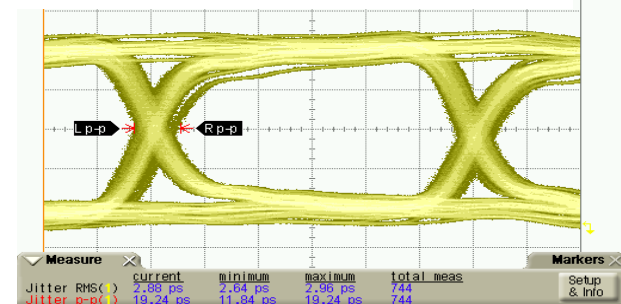
Eye diagram of output clock under 1/4 rate

7.5 Gb/s MSB_{RECJC}
Jitter_{RMS}: 2.68 ps



Eye diagram of output MSB under 1/4 rate

7.5 Gb/s LSB_{RECJC}
Jitter_{RMS}: 2.88 ps



Eye diagram of output LSB under 1/4 rate

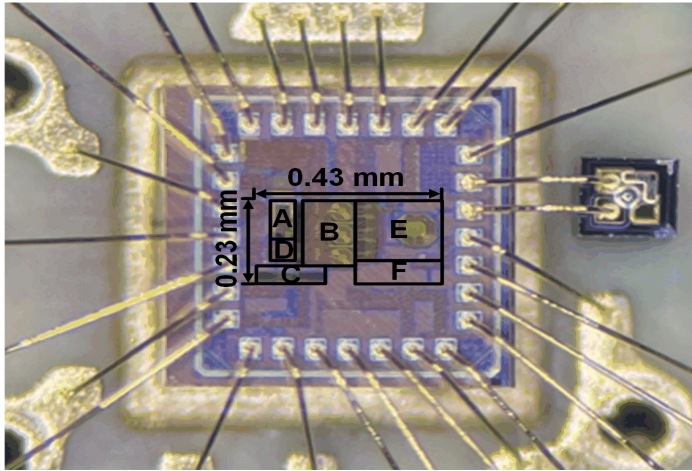
测试指标 (经第三方检测报告认定) 与任务书指标对比

技术指标名称	任务书指标	实测指标	是否满足
速率	≥ 56 Gbps	60 Gb/s	超额完成
功耗	< 400 mW	70.8 mW	超额完成

测试指标 (经第三方检测报告认定) 与国内外领先技术对比

	JSSC'19	JSSC'19	VLSI'14	JSSC'17	VLSI'14	This work
Technology	28-nm	40-nm	65-nm	65-nm	28nm	40-nm
Architecture	1/4-Rate NRZ	1/4-rate NRZ	1/4-rate NRZ	1/4-rate NRZ Adaptive LPF BW in CDR	1/4-rate NRZ Split path CDR	1/4-rate PAM4, JCCDR
JTOL [UI _{pp}] @ 3dB bandwidth	None @ 1 MHz	0.22 UIPP** @ 4 MHz	0.1 UIPP @ 1 MHz	0.41 UIPP @ 20 MHz	0.2 UIPP @ 8 MHz	0.2 UIPP 40 MHz
JTRAN [dB] @ 3dB bandwidth	None	0 ~ -3 dB @DC ~ 4 MHz	0 ~ -3 dB @DC ~ 1 MHz	0 ~ -3 dB @DC ~ 4 MHz	0 ~ -3 dB @DC ~ 3MHz	<-8 dB @All band
Data rate [Gb/s]	2-pairs × 16	25	14	40	4-lanes × 40	60
Power [mW]	2-pairs × 16.06	27***	7.8	225	4-lanes × 175	70.8
Power efficiency [pJ/bit]	1.004*	1.08***	0.56	5.625	4.375	1.18
Supply voltage (V)	0.9	None	0.8	1.2	None	1.0

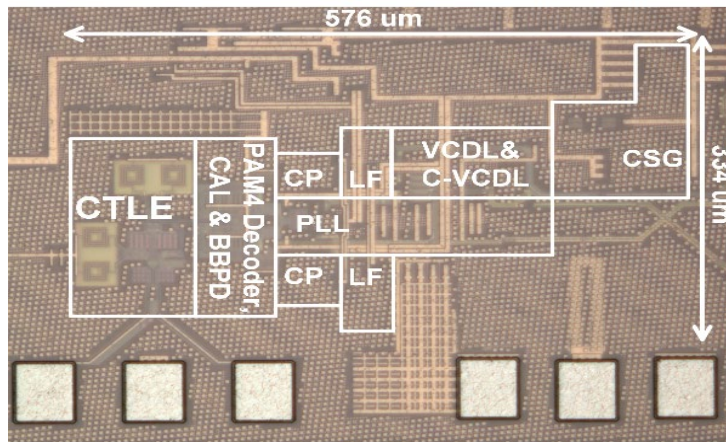
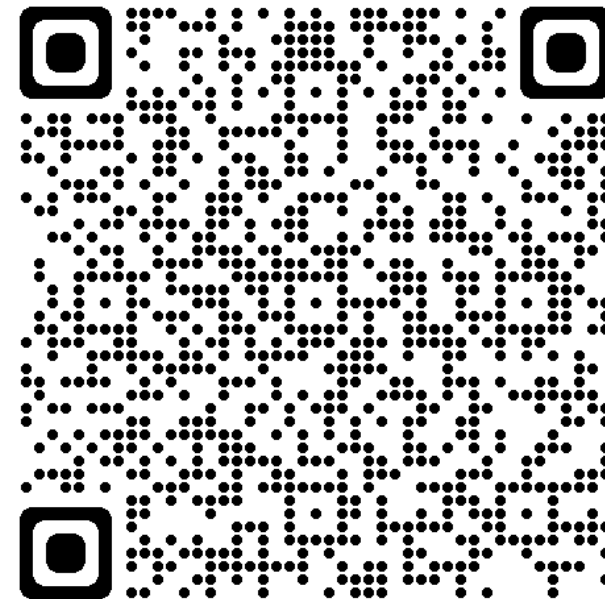
VCSEL TRX Demo: 56-Gb/s PAM-4 VCSEL TX and RX



Link

[PAM4收发机芯片演示视频 ESSCIRC 2023+VLSI2021 Fuzhan Li_哔哩哔哩_bilibili](#)

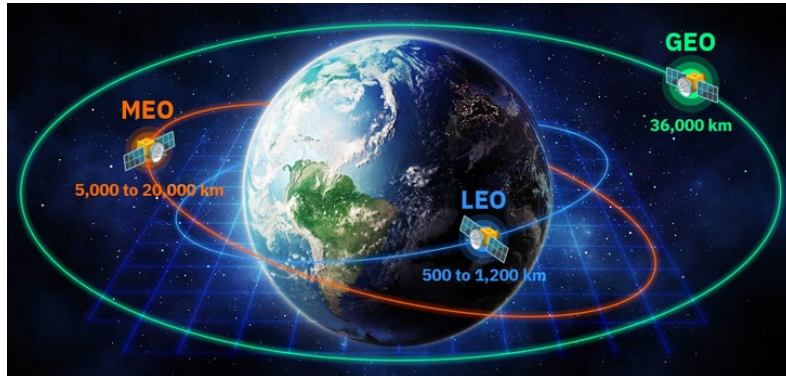
QR code



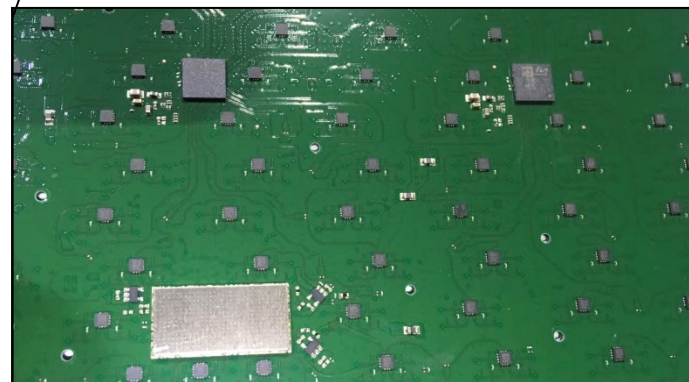
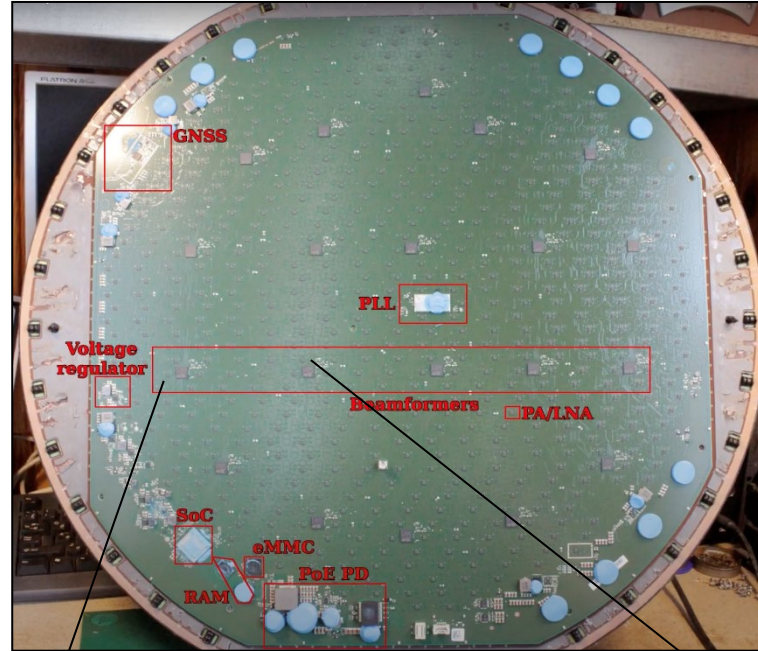


CMOS mmWave Phased-Array IC

Starlink Satcom

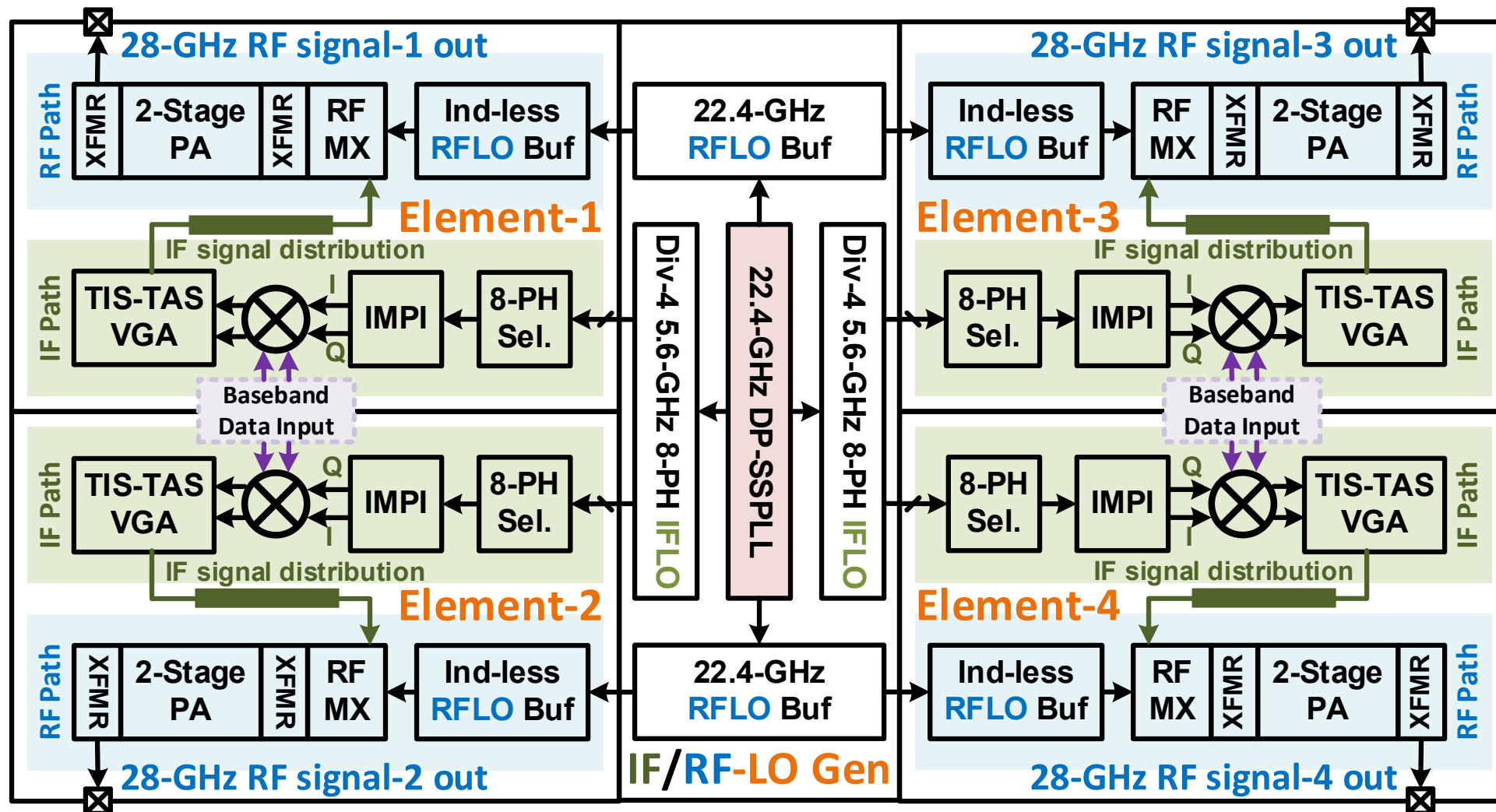


Starlink Ground Dish

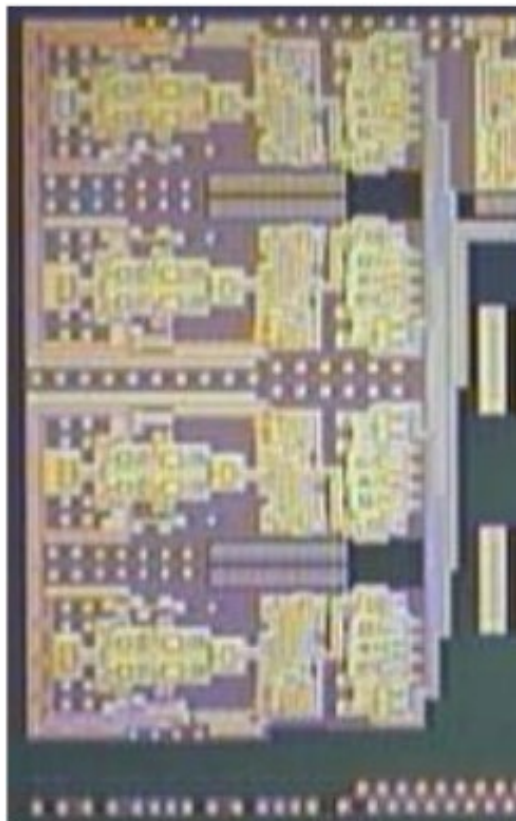


- Mechanical satellite tracking employed
- Utilization of electrical and digital beamforming
- Architecture designed to minimize beamforming IC usage
- Focus on combining individual PAs and LNAs for gain enhancement

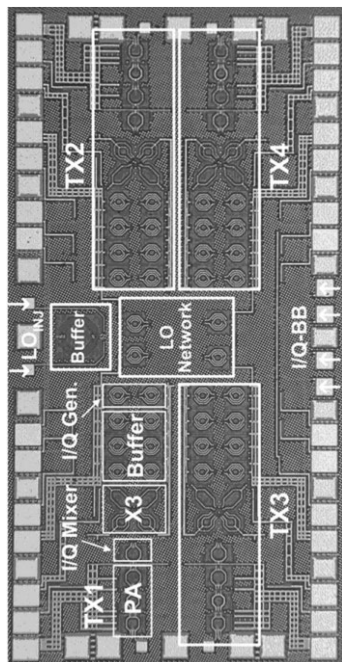
A Ka-Band Phased-Array Tx SoC in 40nm CMOS



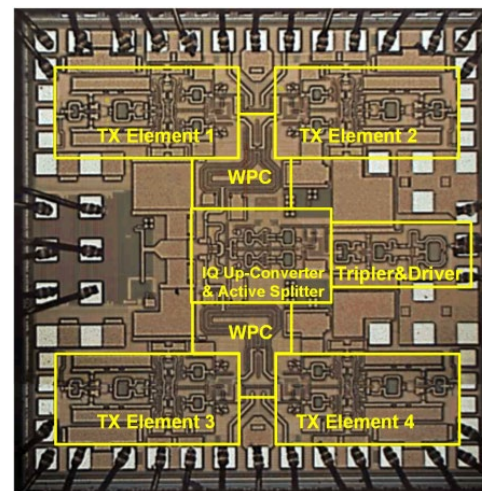
Area Efficiency Comparison



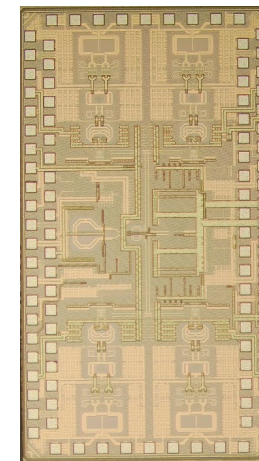
TMTT 2021, 38 GHz
4.3 x 2.2 mm²
w/o LO Gen.



JSSC 2010, 60 GHz
2.9 x 1.4 mm²
w/o LO Gen.

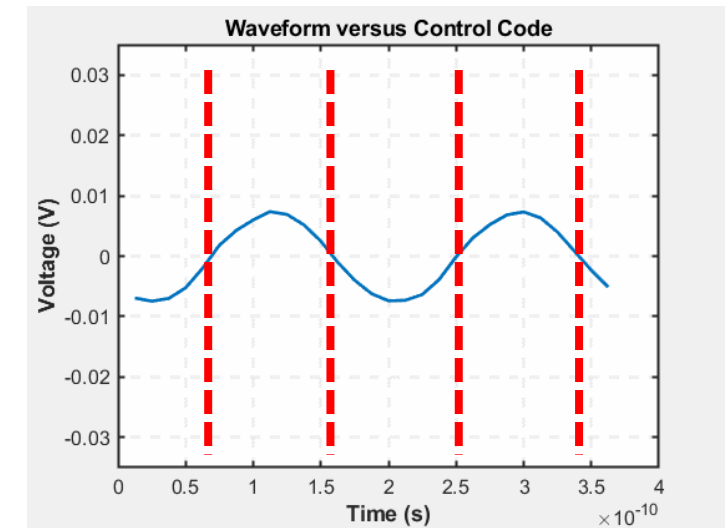
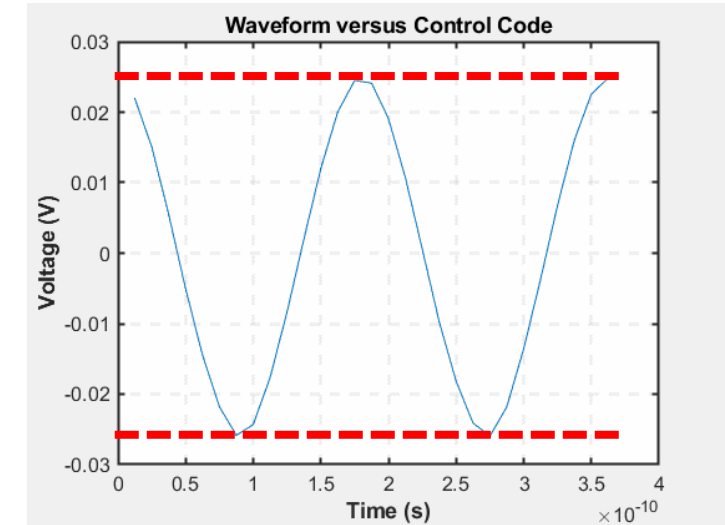
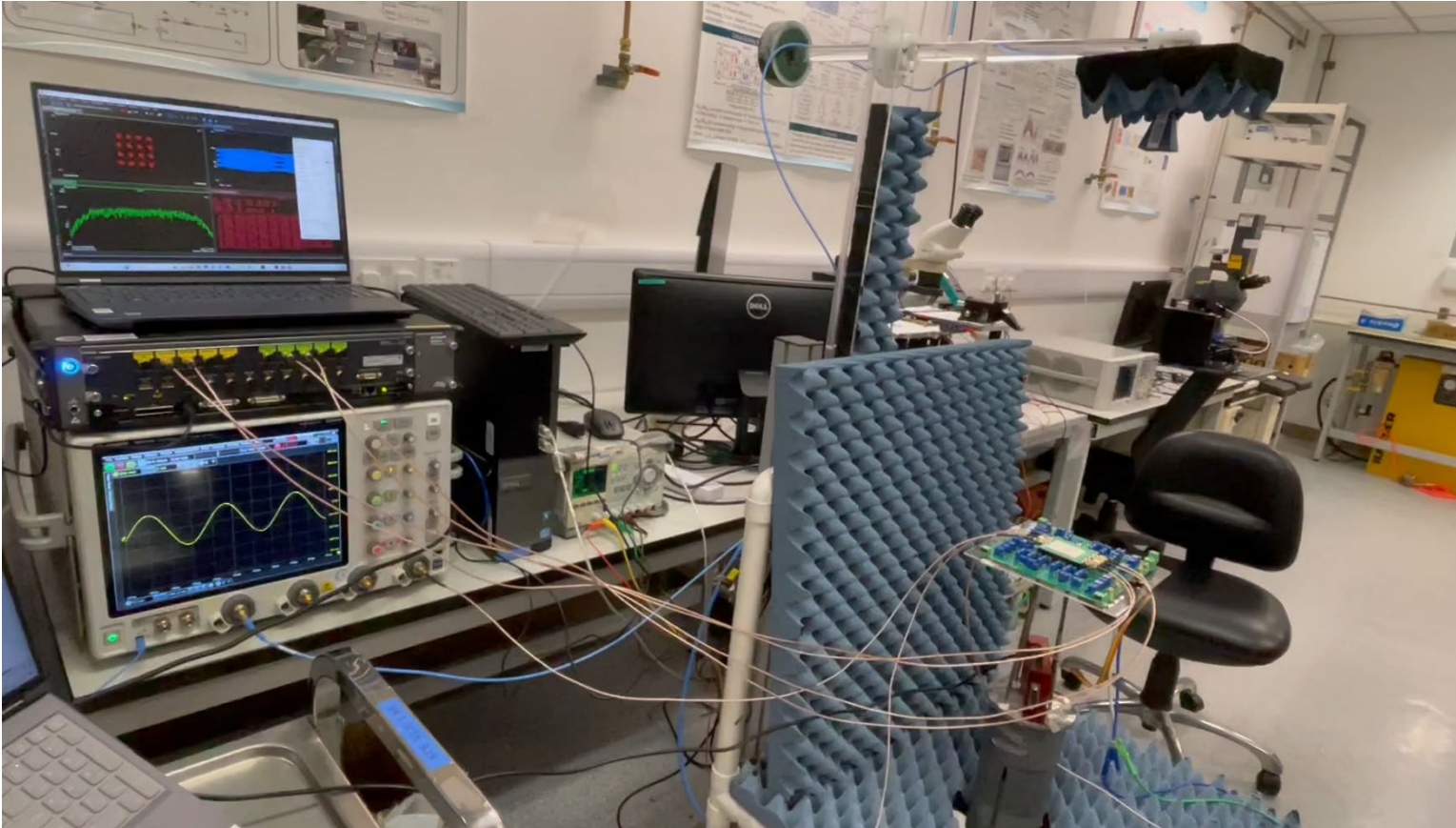


JSSC 2022, W band
2 x 2 mm²
w/o LO Gen.

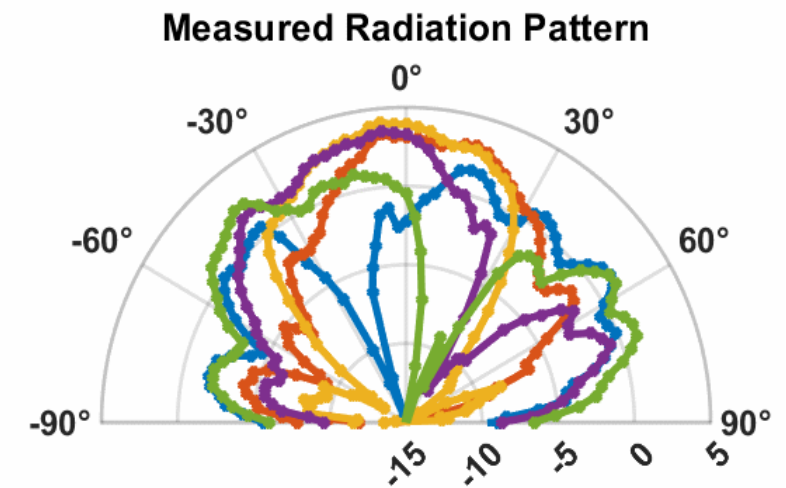
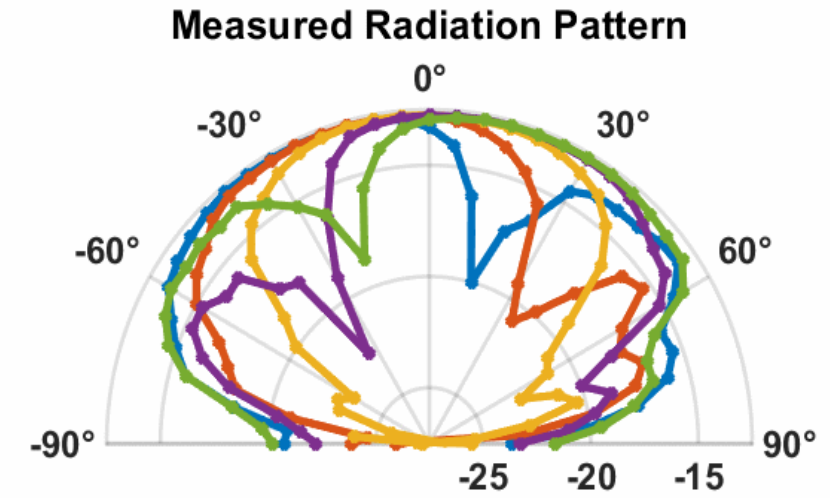
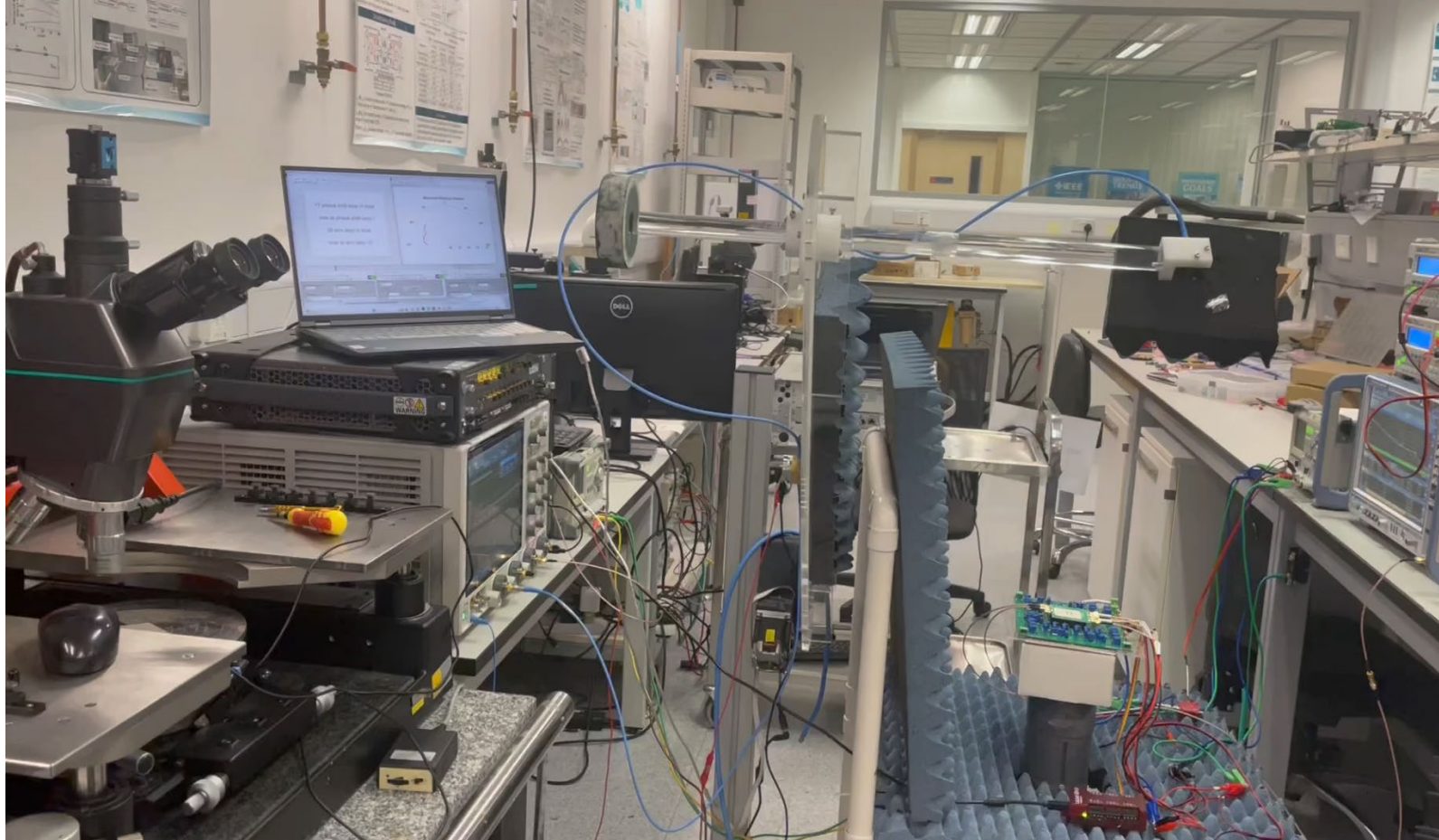


This work, 28 GHz
1.87 x 1.16 mm²
with LO Gen

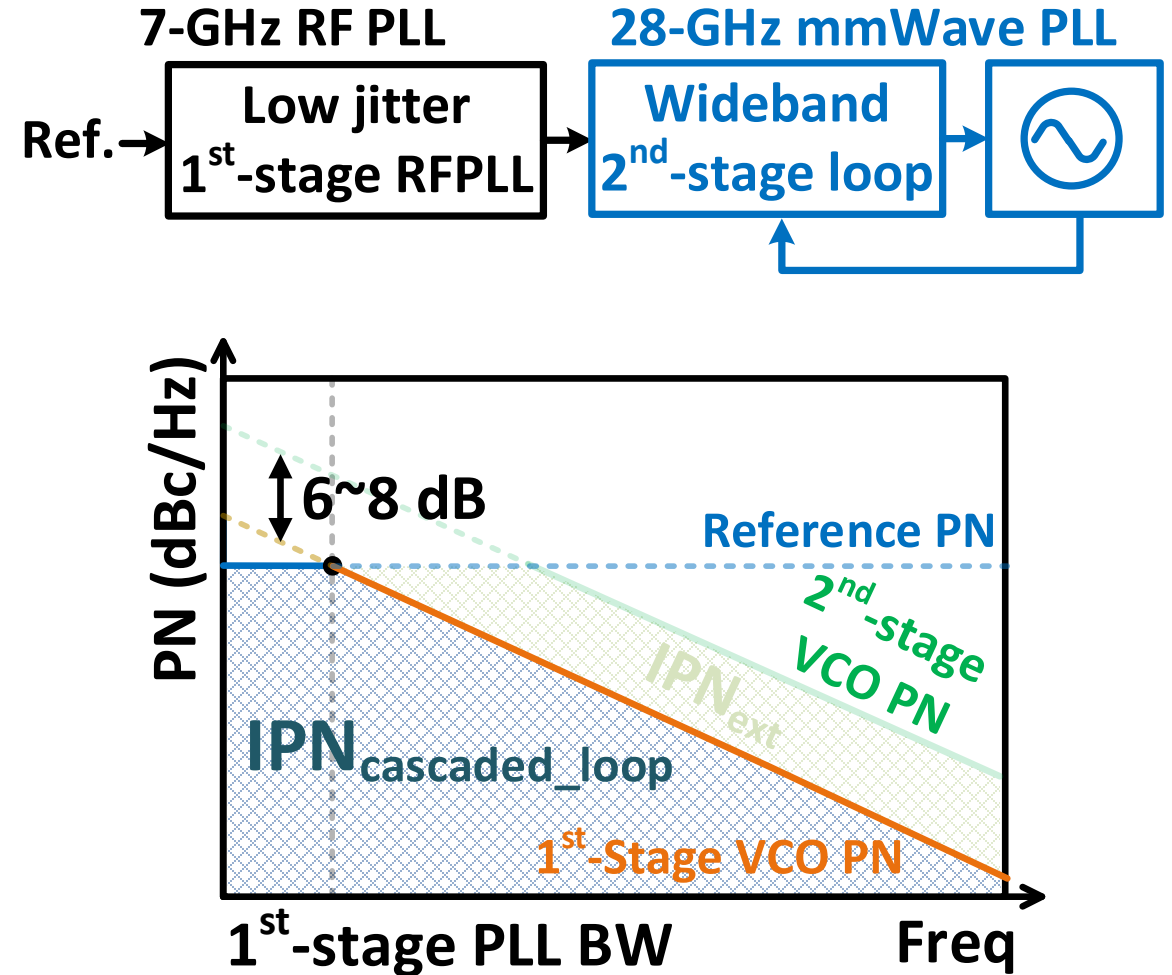
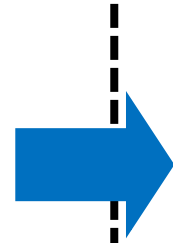
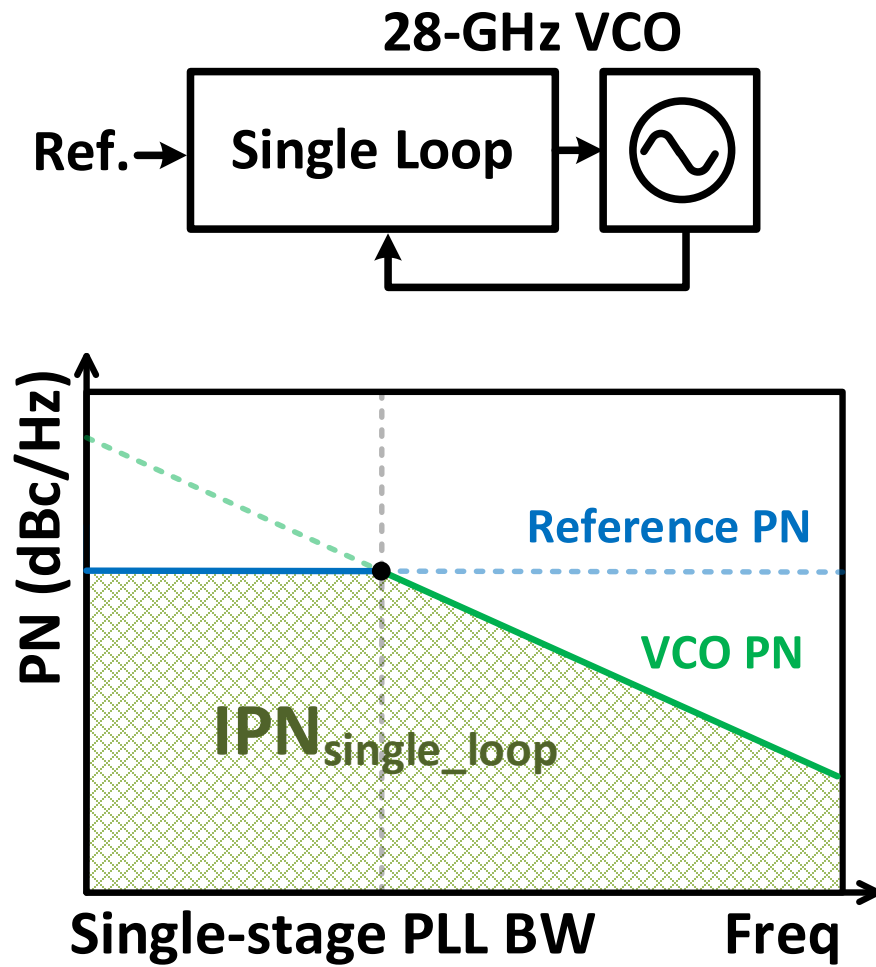
- Phase Shift and Gain Control Demo
 - Orthogonal phase shift and gain control



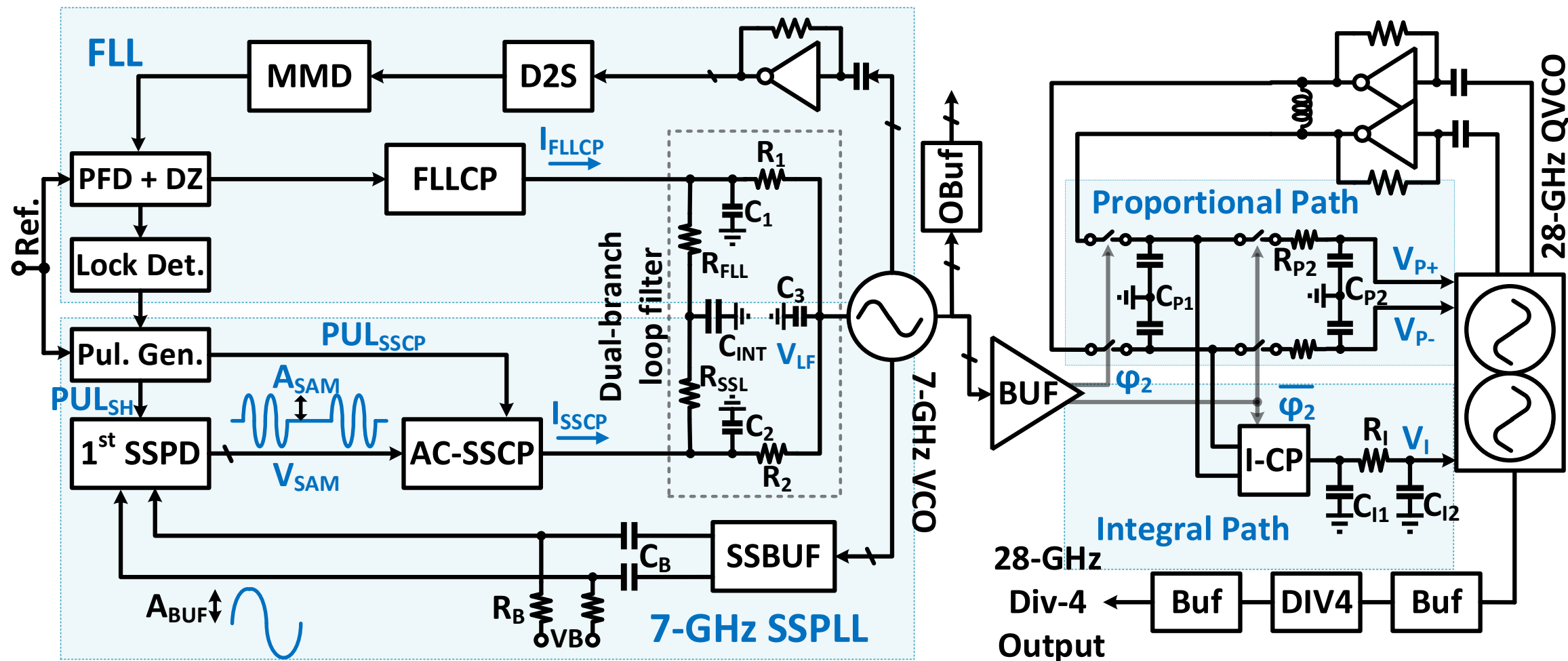
- Beamsteering Demo



Ka-Band Cascaded QPLL

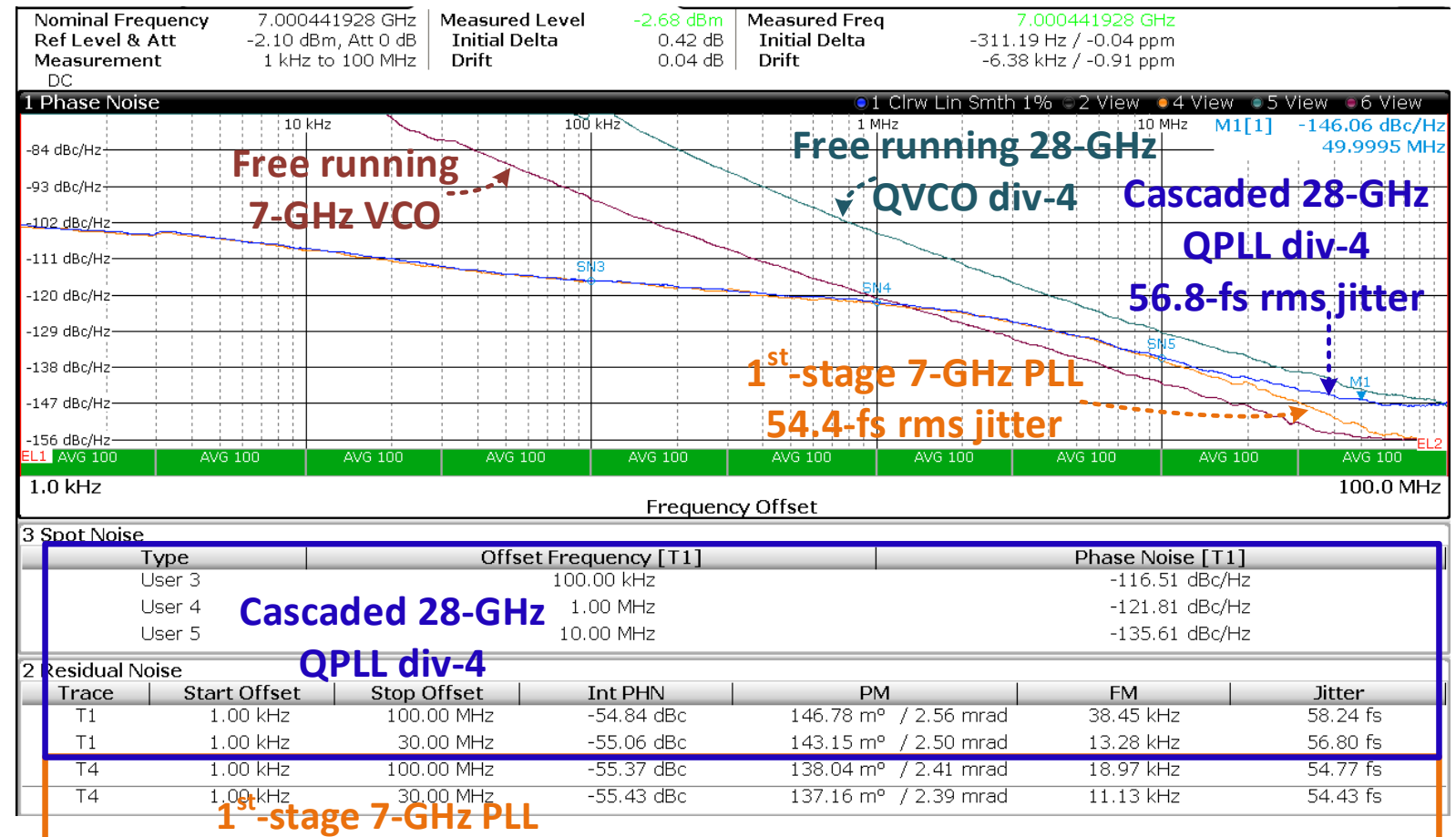


28GHz Dual-Loop PLL Architecture



Experimental Results

- The 1st-stage RF SSPLL dominates the overall jitter
 - 1st-stage contributes 54.4-fs out of 56.8-fs total rms jitter
 - High frequency VCO phase noise is sufficiently attenuated
 - Over 1 kHz to 100 MHz range, QVCO PN profile is well above QPLL



Performance Comparison

	Hu ISSCC20	EK JSSC18	Yang ISSCC22	Du VLSI21	Kim JSSC19	Liao JSSC20	This work
Tech	28nm	28nm	7nm	28nm	65nm	45nm	40nm
Arch.	CS + Harmonic extraction	Single-stage	Harmonic mixing	Harmonic extraction	Cascaded SS+QILO	Cascaded RSPLL+ ILFM	Cascaded SS+DP-SS
Freq. (GHz)	21.71~ 26.49	23.3~ 30.2	25~28	24~31	28~31	33.6~36	24.0~ 29.8
Freq. range	19.3%	25.8%	11.3%	25%	10.1%	6.9%	21.4%
Ref. (MHz)	250	491.5	74	50	100	80	250
Jitter (fs)	75.89 (10k~30M)	114	88	199 (10k~30M)	76 (1k~30M)	251 (10k~10M)	56.8 (1k~30M)
Spur (dB)	-45	-65.1	-61	-65	-58	-60	-55.6
Pdc (mW)	16.5	31	12.9	11.5	41.8	20.6	42.1
FoM _{jitter} (dB)	-250.2	-244	-250	-243.3	-246.1	-238.9	-248.6
FoM _{jitter-N} (dB)	-270.4	-261.2	-275.8	-270.9	-270.7	-265.3	-269.1
Area	0.5	N. M.	0.24	0.3	0.32	0.41	0.4

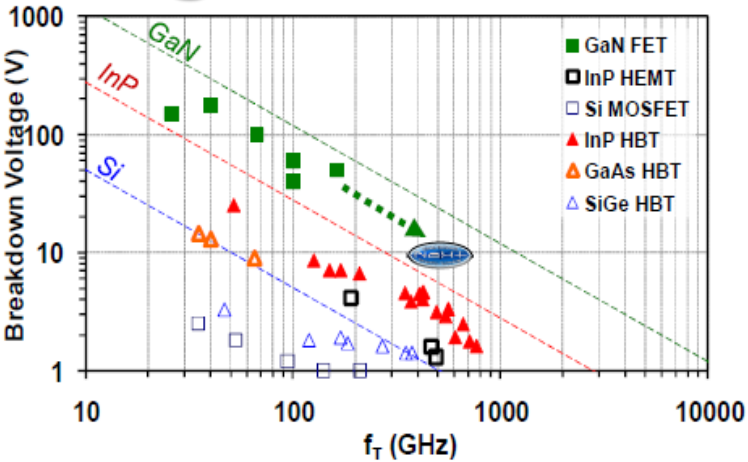


High-SPLIQ IC Needed for the New Era

High-Speed High-Power

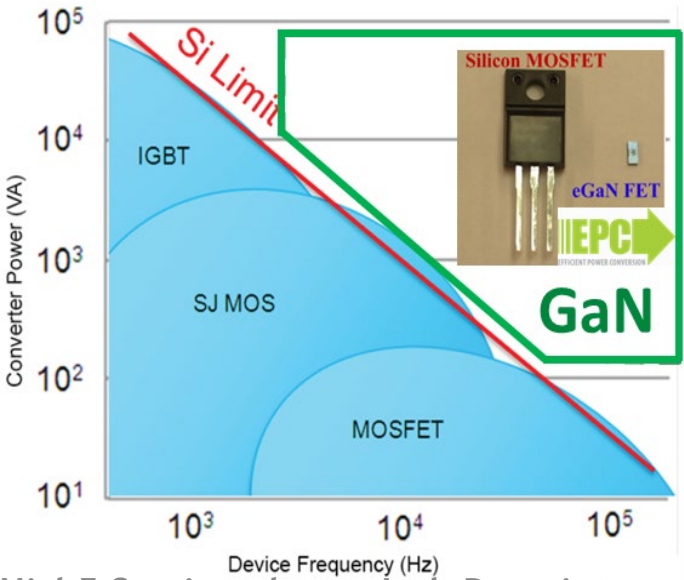
GaN for mmWave

J. Albrecht *et al.*, IEEE CSICS (2010).



GaN for power management

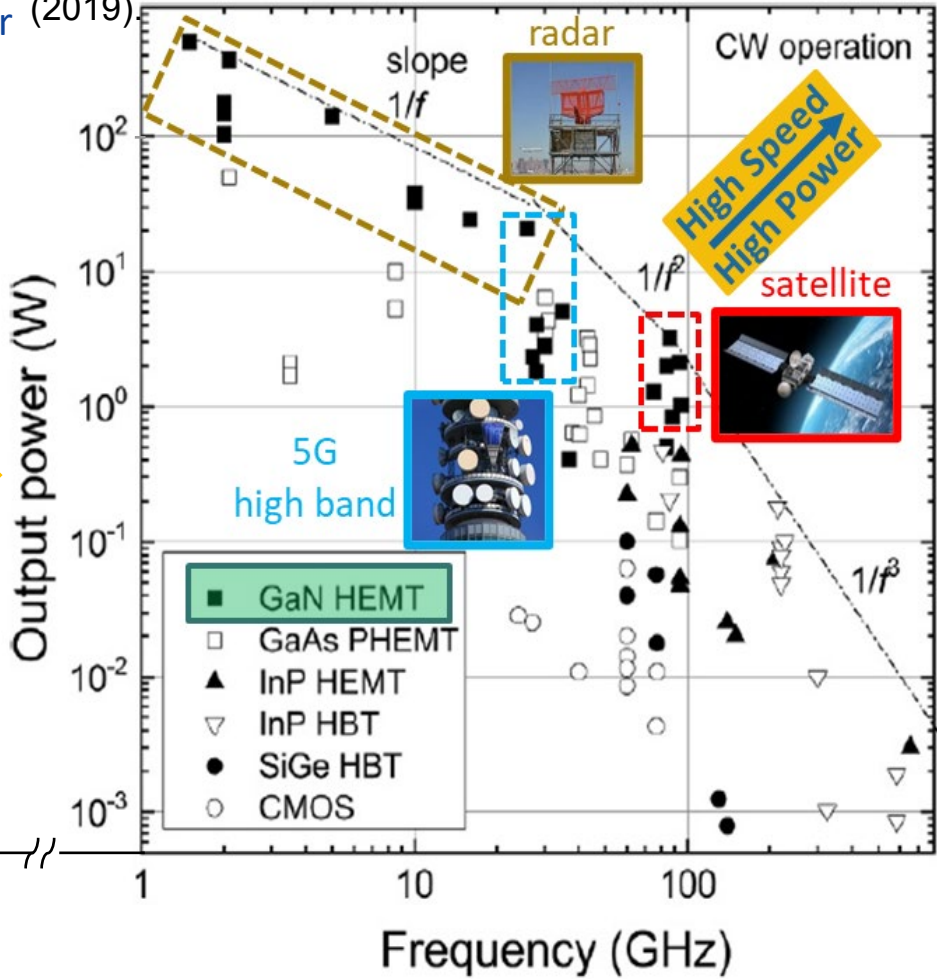
I. C. Kizilyalli *et al.*, "Wide band-gap semiconductor based power electronics for energy efficiency" (ARPA-E, Washington DC, 2018)



Charger and power supply



K. Shinohara, "III-Nitride millimeter wave transistors", Chapter 4 in *III-Nitride Electronic Devices*, Elsevier (2019)

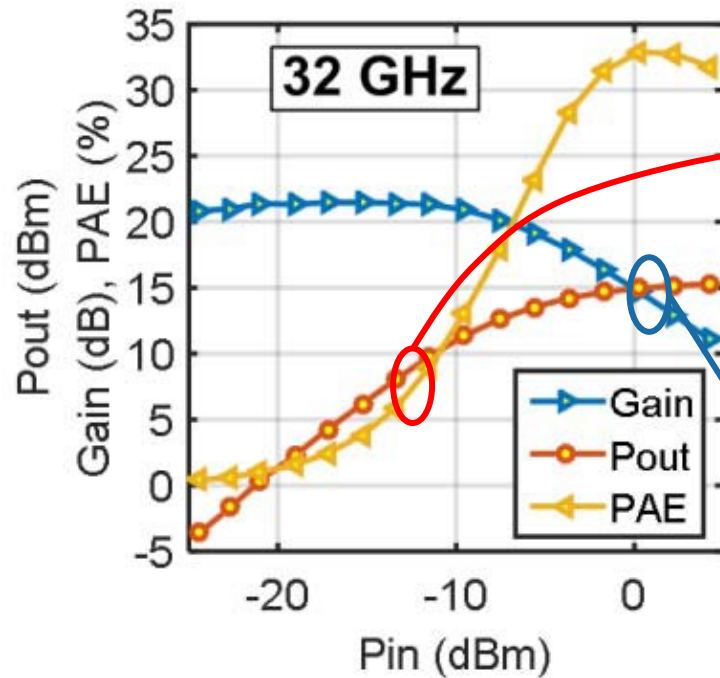


2025/10/22

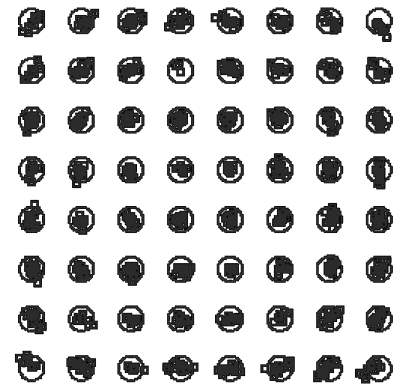
High5 Semiconductor Ltd. Proprietary and Confidential. Protected under NDA.
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26

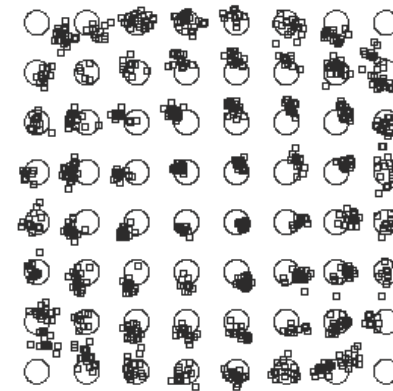
High-**L**inearity



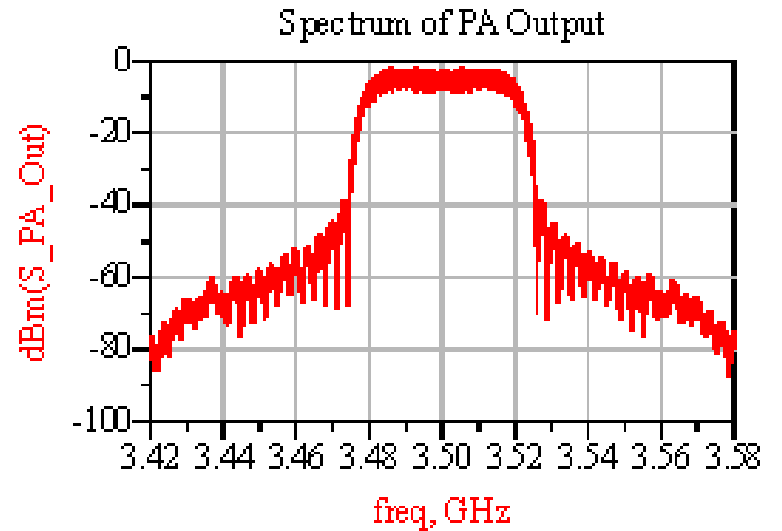
Large signal performance of a mmWave power amplifier (PA), including P_{out} , Gain and PAE



QAM-64 constellation with **low** EVM



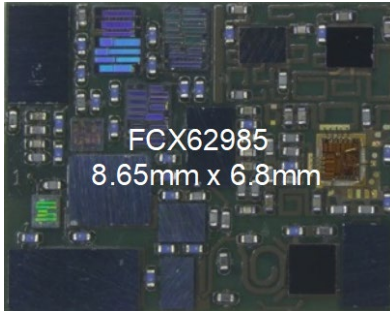
QAM-64 constellation with **high** EVM (bad linearity)



ACPR from ISEE
(Integrated System Engineering Evaluator),
a simulation platform developed by OWL)

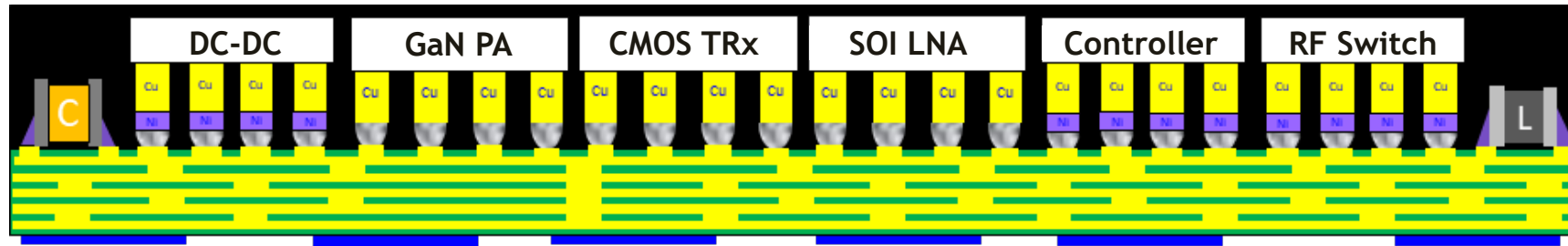
<https://github.com/HKUST-ECE-IC-Design-Center-OWL/ISEE-Complex-Signal-Co-simulation-Platform-For-Integrated-Circuit-and-System-Design>

High-Integration



Compact Package

- Designed to achieve highest-level of integration in a small form-factor and includes multiple functions IC with multiple processes
- This RFFE SiP includes 56 SMDs, 9 Acoustic filters, 4 HBT PAs, 2 SOI Switches, 1 SOI LNA, and 1 CMOS controller



System-in-Package

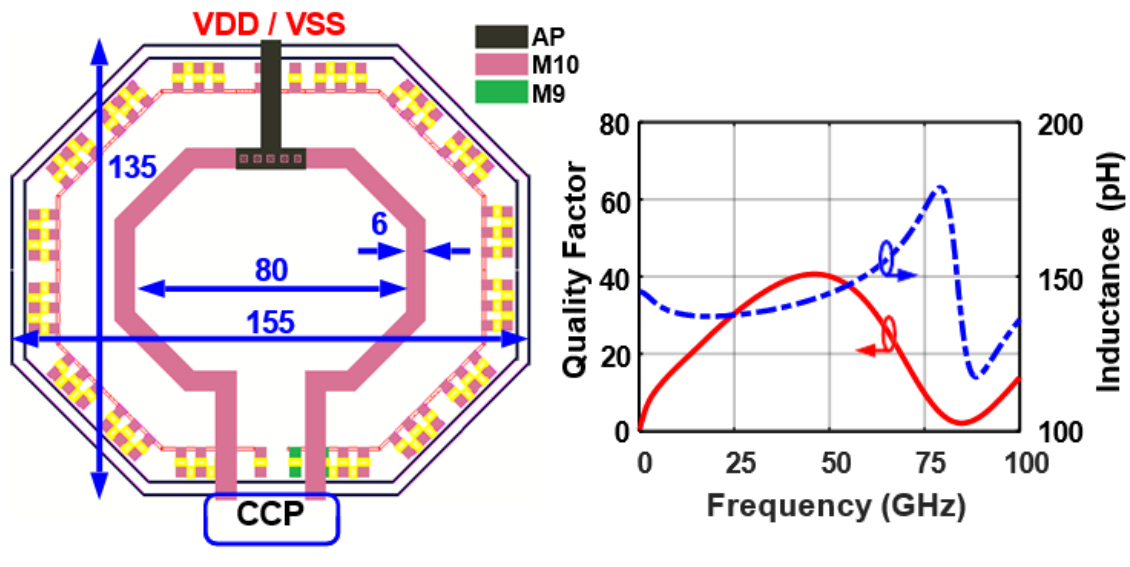
- High power dissipation device like DC-DC converter and GaN PA in the same package
- Multiple-tech chips in a single package

High-Voltage High-Power Buck Boost Converter



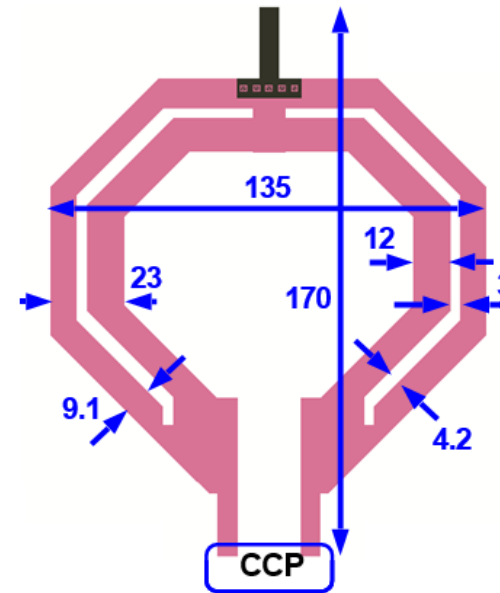
- EPC 140W Micro SmartPower
- Type-C Bidirectional PD3.1/Max 140W
- Type-A multi-channel fast charging
- Intelligent power allocation for multi-port high-power charging
- Built-in dual DC-DC
- Supports 2C1A independent fast charging
- Supports dual PD3.1 simultaneous charging and discharging
- Solar energy charging
- 28V-5A discharge; 28V-2A charge
- Multiple over-voltage, over-current, and over-temperature protection

High-Quality Factor Passives



Directly using PDK inductor

- $L = 138 \text{ pH}$
- $Q = 33$



Custom-design optimized inductor

- $L = 153 \text{ pH}$
- $Q = 47$ (42% higher)



Trade-off between Q factor, inductance density, and power handling capability

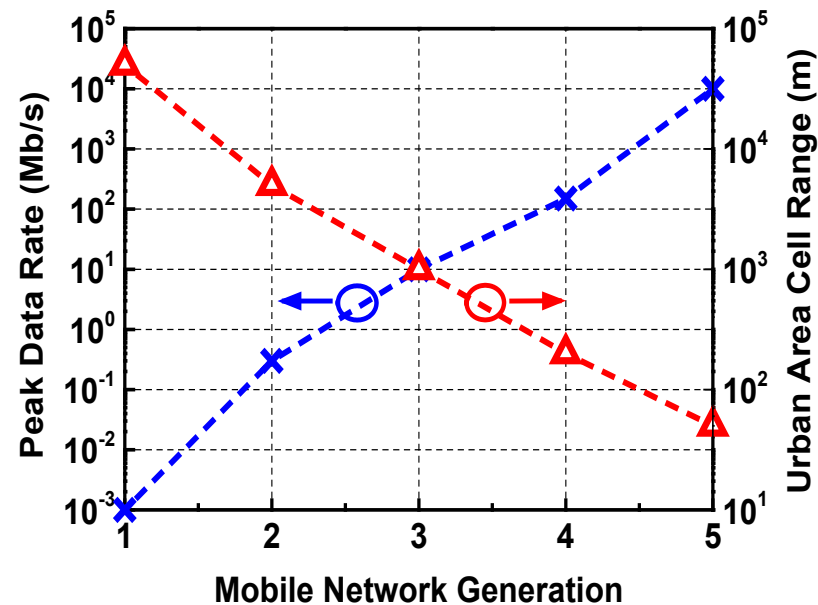


New Potential Applications in the 6G Era

New Opportunities: Optical-Wireless Hybrid Link

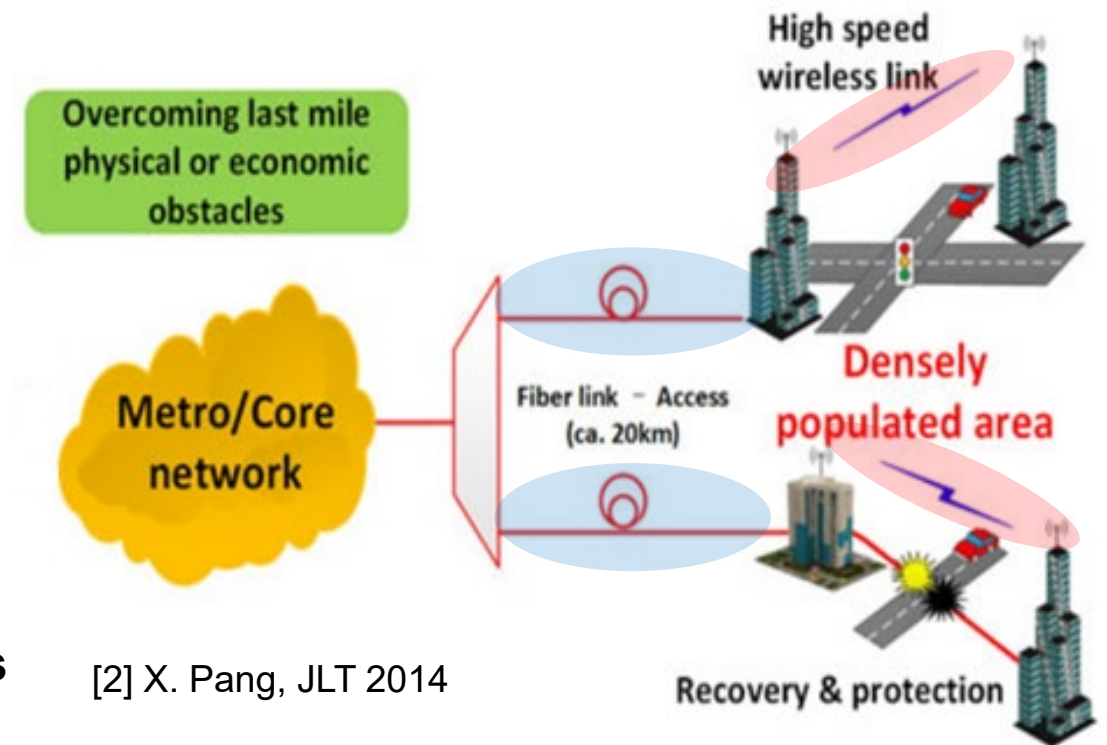
- Fiber-Wireless Hybrid Network: **Cascaded Topology**

Evolution of Cellular Networks



- 5G mobile network requires ultra-dense cellular cells
- Backhaul links deployment is challenging
- Fiber-wireless networks provide high performance and flexible backhaul link connections

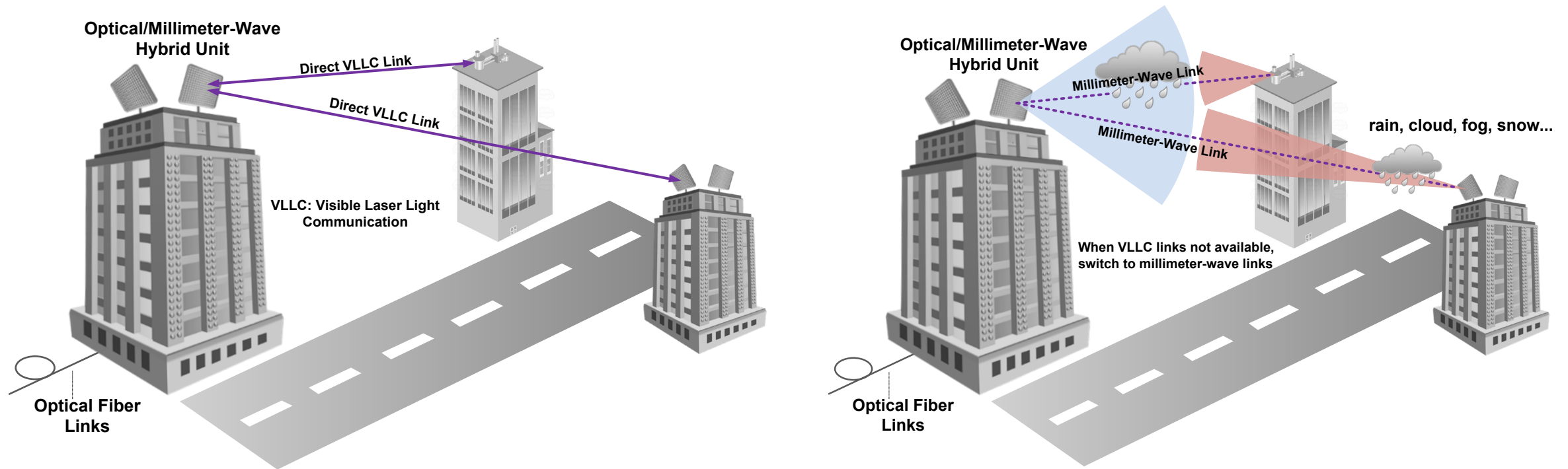
Fiber-Wireless Network



[2] X. Pang, JLT 2014

New Opportunities: Optical-Wireless Hybrid Link

- Fiber-Wireless Hybrid Network: **Parallel Topology**



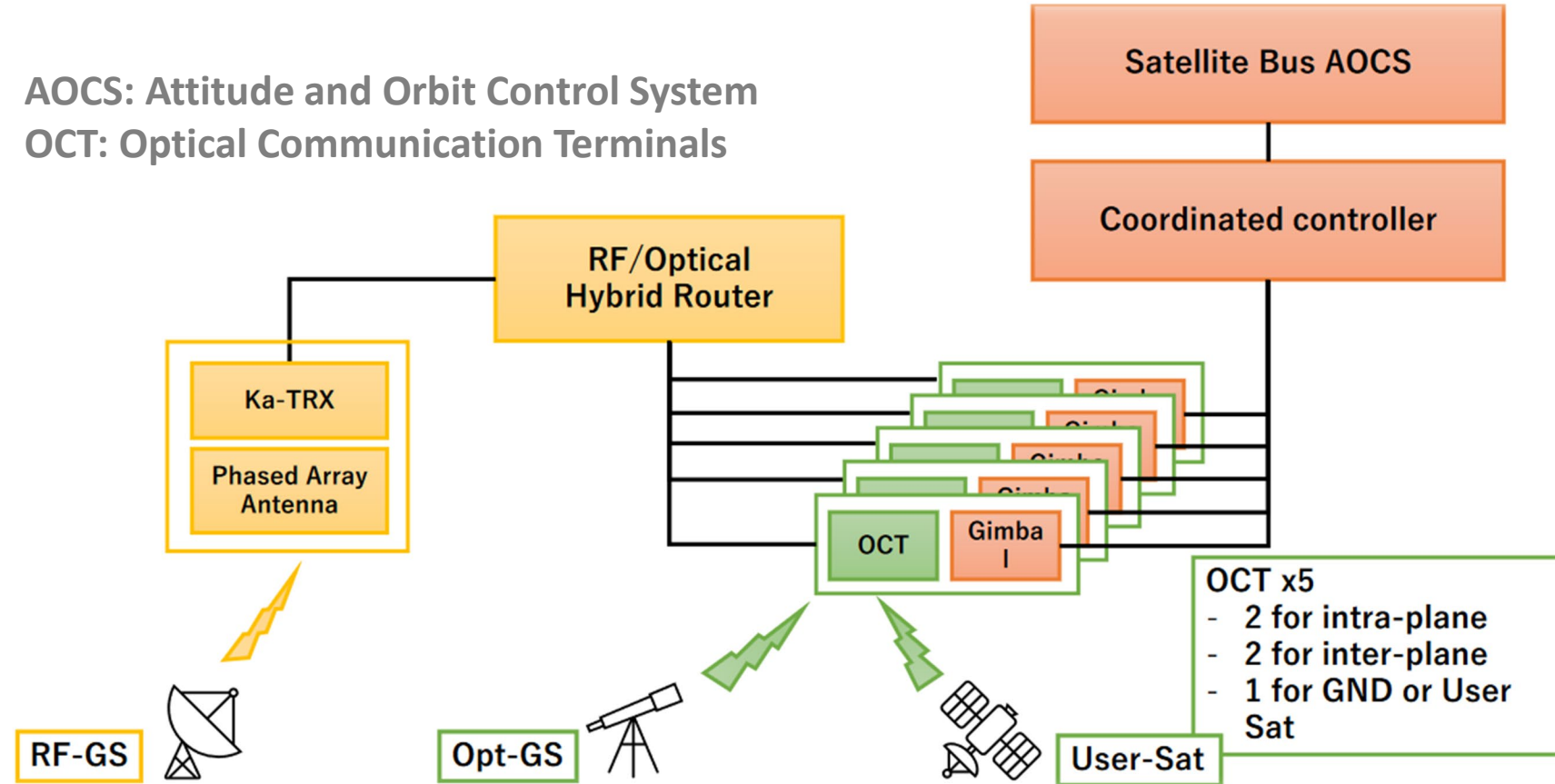
- Under good weather condition: mmWave + Optical in parallel
- Under bad weather condition: mmWave only

Optical-Wireless Hybrid Link for SatCom

Mixed usage of
OWC and mmWave
links for LEO SatCom

- Optical: communication between satellites
- mmWave: between satellite and ground base station

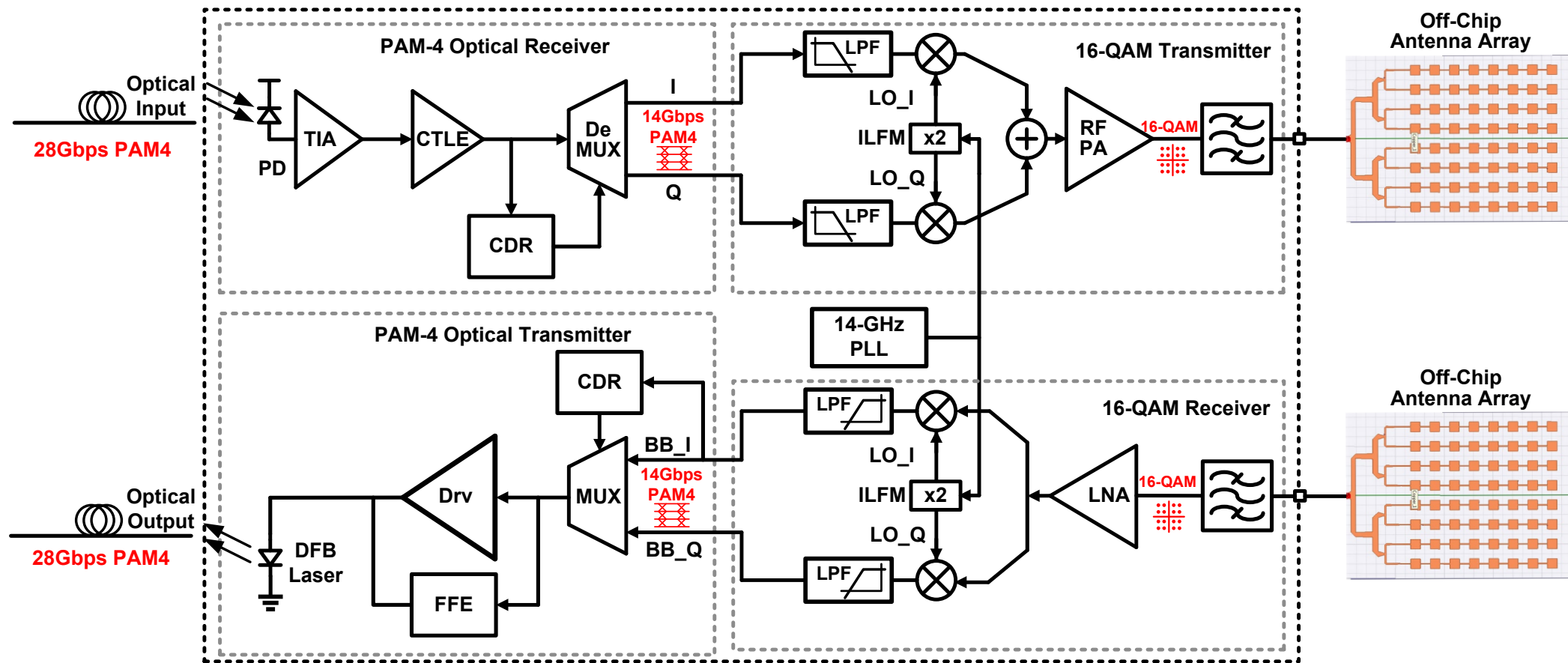
AOCS: Attitude and Orbit Control System
OCT: Optical Communication Terminals



[Okada. Tokyo Tech]

Optical-Wireless Hybrid Transceiver Architecture

- Optical-In-mmWave-Out + mmWave-In-Optical-Out





6G Technologies & IC Design Research @ HKUST

An Area of Excellence Project (AoE/E-601/22-R)

6G: Wireless Access and Connectivity for an Intelligent and Sustainable World

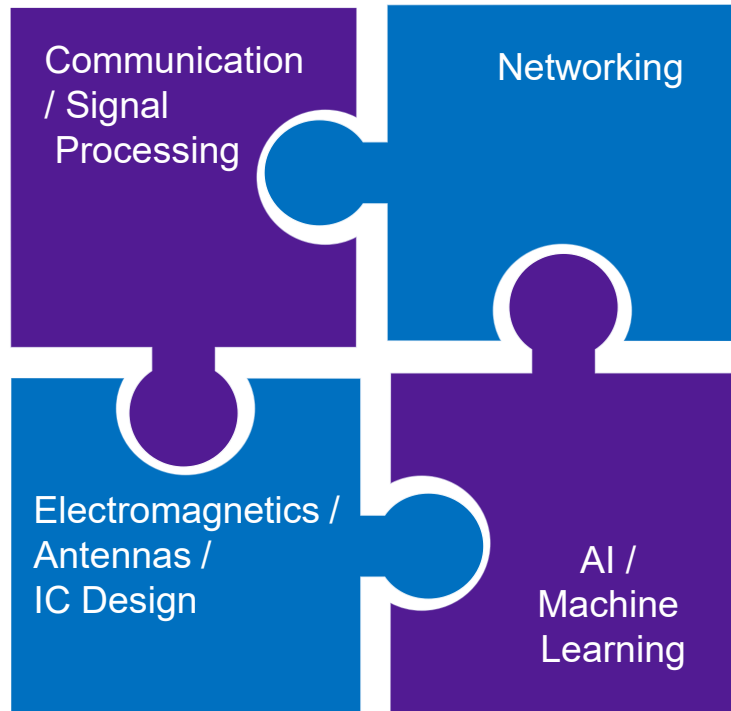


**Coordinating
University:**



**Started Jan. 2023 and
Supported by the Hong
Kong Research Grant
Council**

The AoE Team



**MULTIDISCIPLINARY TEAM
WITH COMPLEMENTARY STRENGTHS**



K. B. LETAIEF



R. MURCH



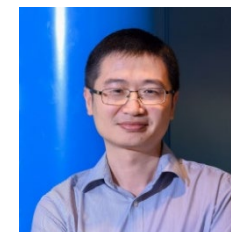
Qian ZHANG



V. N. LAU



Patrick YUE



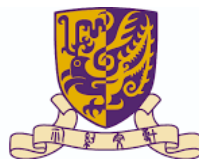
Jun ZHANG



C. Y. TSUI



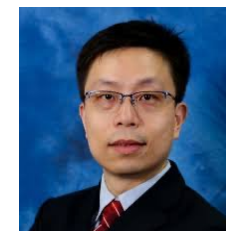
Song GUO



香港中文大學
The Chinese University of Hong Kong



A. ZHANG



Jiaya JIA



香港大學
THE UNIVERSITY OF HONG KONG



K. HUANG

Optical Wireless Lab (OWL) Chip Gallery



2007~2013

2014

2015

2016

2017

2018

2019

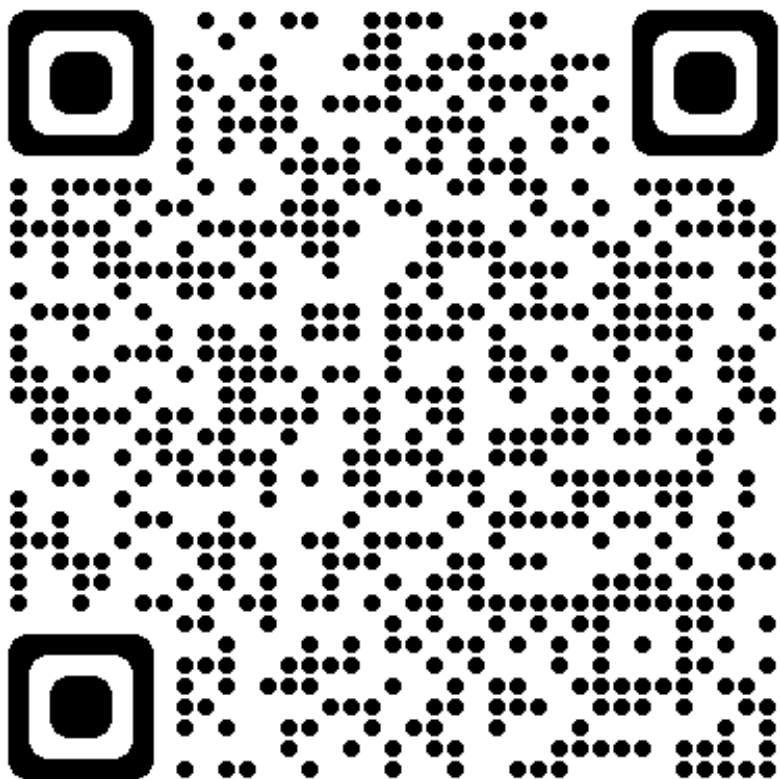
2020

2021

2022

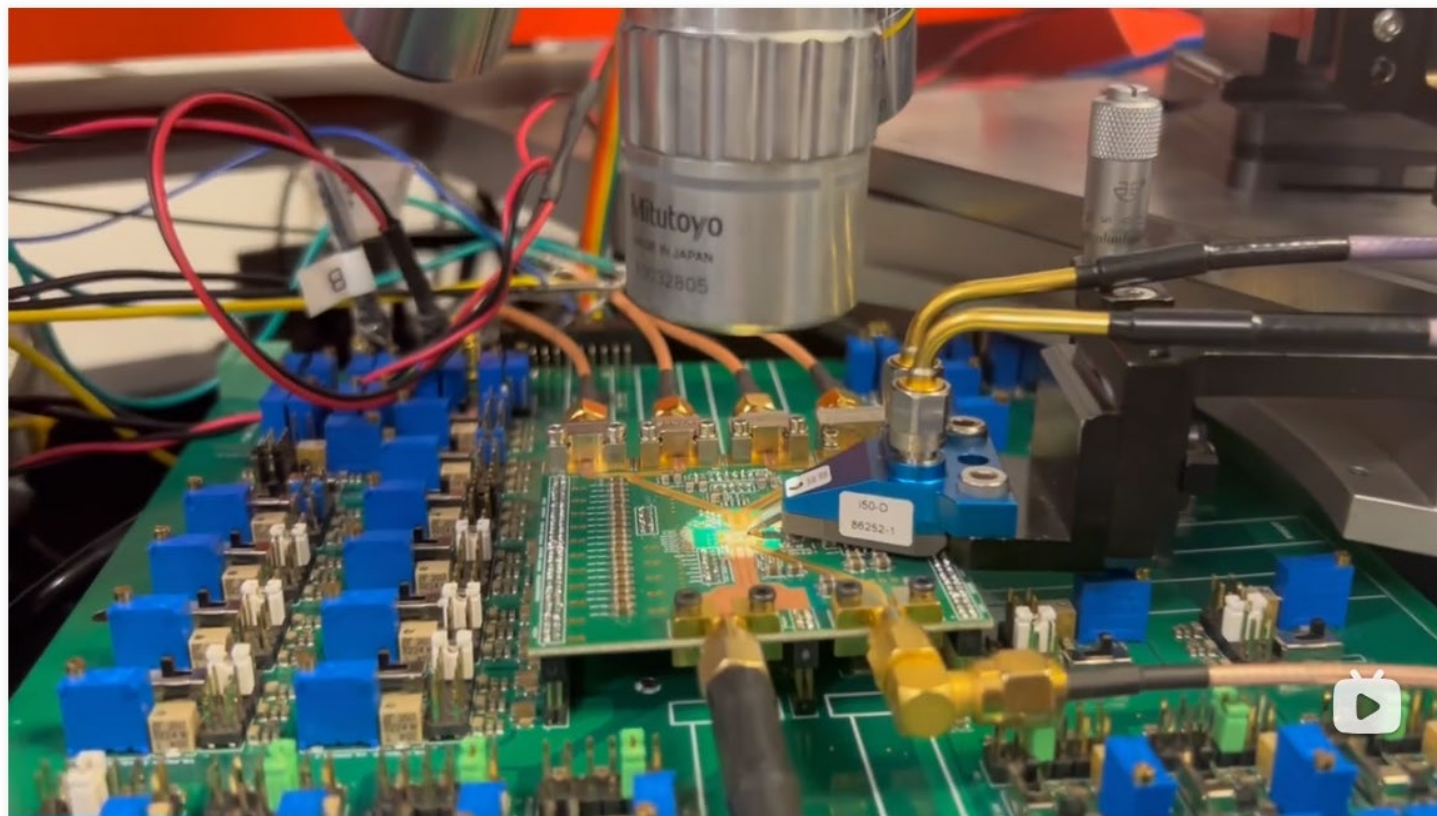
2023

港科大光电无线实验室个人主页-哔哩哔哩视频 (bilibili.com)



28-GHz 中频移相相控阵芯片演示

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谢谢!

Thank you!