香港科技大學
THE HONG KONG UNIVERSITY OF SCIENCE AND TECHNOLOGY

HKUST OWL

Advanced Wireline and Optical Communication IC Design
高级有线及光通信 IC 设计

Prof. C. Patrick Yue 俞捷教授

ECE ICDC OWL

芯动力人才计划®第 125 期国际名家讲堂

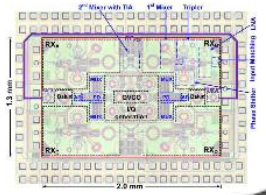
Integrated Circuit Design Center

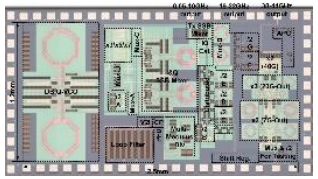
芯 片 設 計 研 究 中 心

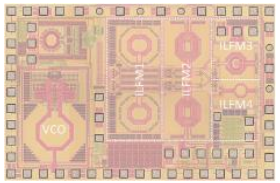
Key Research Areas

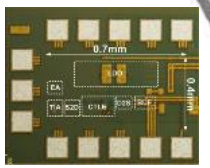
RF Integrated Circuits and Systems

➟ mm-wave/sub-THz IC, visible light communication and optical transceiver



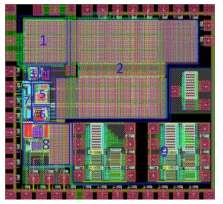


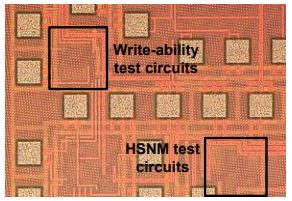




VLSI System

➟ VLSI architectures for deep learning and digital baseband applications

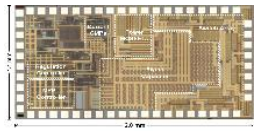


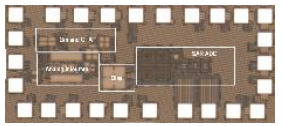


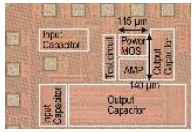
Source: Qualcomm

Analog & Mixed-signal IC

➟ low-voltage and low-power analog IC for IoT

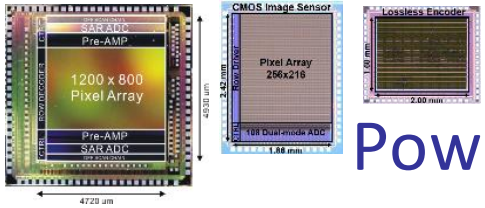






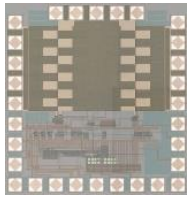
Smart Sensors and Microsystems

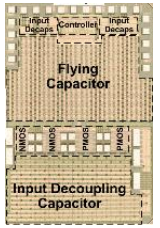
➟ vision, temperature, humidity and gas sensors

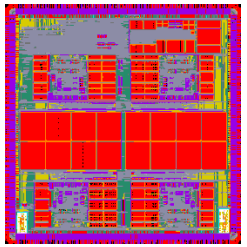


Reconfigurable Computing System

➟ embedded system security, performance and power efficient multicore system

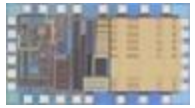






Power Management and Display Driver

➟ wireless power transfer and energy harvesting IC



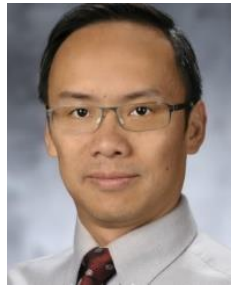
HKUST ICDC Faculty Profiles

- 14 faculty (6 Fellows of IEEE, 1 Fellow of Optica, ACM & FAAAS)
- 100 post-docs, RAs, PhD and MPhil students

Patrick YUE
Stanford
FIEEE, FOptica

Wing Hung KI
UCLA

Tim CHENG
UC Berkeley
FIEEE



Yuan XIE
Princeton
FIEEE, FACM, FAAAS

Mansun CHAN
UC Berkeley
FIEEE

Ricky LEE
Purdue
FIEEE

Yihan ZHANG
Columbia

Wei ZHANG
Princeton

Howard LUONG
UC Berkeley
FIEEE

Chi Ying TSUI
USC

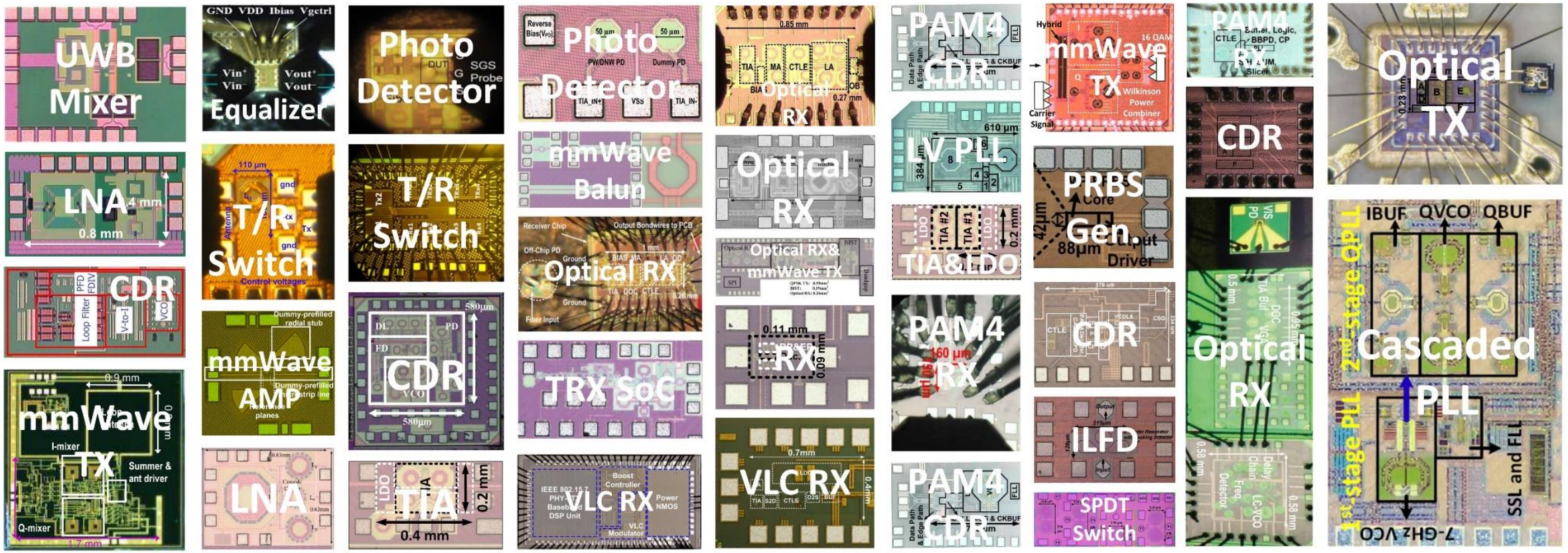
George YUAN
UPenn

Khawar SARFRAZ
HKUST

Zhiyao XIE
Duke

Fengbin TU
Tsinghua

Optical Wireless Lab (OWL) Chip Gallery

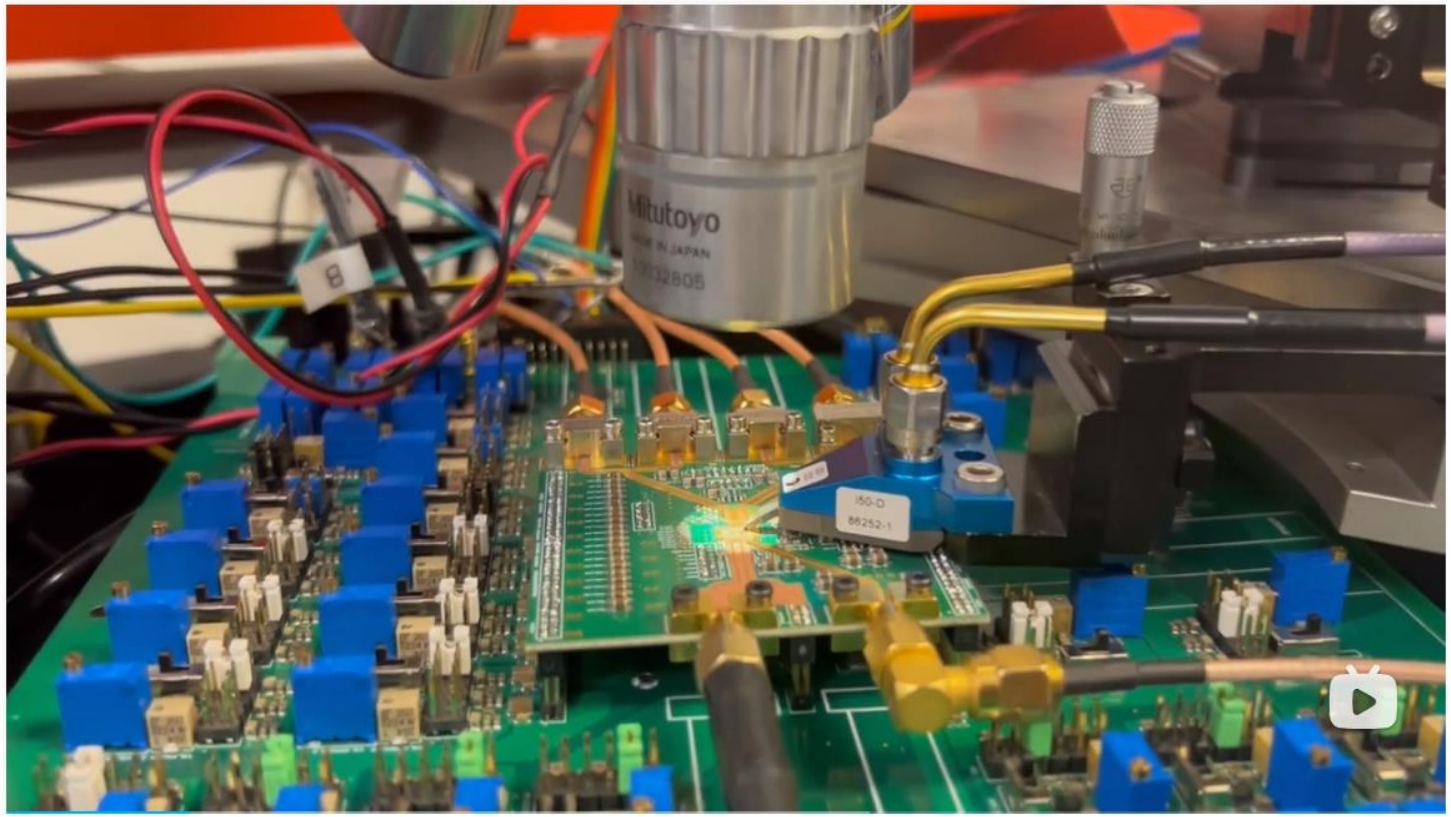


Chip Testing Demo

港科大光电无线实验室个人主页-哔哩哔哩视频 (bilibili.com)

28-GHz 中频移相相控阵芯片演示

179 0 2023-09-20 15:58:42 未经作者授权，禁止转载



Short Course Outline

- Background, Application, and Trend (BAT)
- Transmitter (Tx) [Tx Ref]
- Receiver (Rx) [Rx Ref]
- Clock & Data Recovery (CDR) [CDR Ref]
- Practical Implementation Techniques (PIT) [PIT Ref]

Acknowledgements (OWL Alumni)

Acknowledgements (OWL Current Members)

Background, Applications, and Trends for High-Speed Serial Links

- Applications
- Characteristics of the Architecture
- Technology Choices
- Performance Metric
- Trends

Wireline and Optical Transmitter

- Architecture
  - VCSEL Transmitter
  - MRM Transmitter
  - MZM Transmitter
  - Wireline Transmitter
- Key Circuits
  - Multiplexer (GitHub: 4-to1-MUX-for-28Gbaud-Optical-TX)
  - Output Driver
  - Pre-emphasis
- Practical Issues
  - EMI Suppression Due to CM Noise to Reduce Radiation Emissions

Wireline and Optical Receiver

- Motivation
  - Electrical vs Optical Link
- Architecture
  - Wireline vs Optical Receiver
  - ADC-Based Receiver
- Key Circuits
  - PD Interface
  - Multiple Peaking in TIA
  - Modified Cherry-Hooper Amplifier
  - FFE and DFE Implementation
- Practical Issues
  - On-Chip LDO for Improved Sensitivity
- Conclusion

Clock and Data Recovery and Clock Generation

- Architecture
  - Overview of CDR and PLL Loop Configuration
  - Why Single Loop? How to Achieve Wide Capture Range Via Single Loop
  - Why Dual Loop? Cascaded or Parallel? How Loop Parameters Are Determined
  - Why Dual Path? Decoupling JTRAN and JTOL
- Key Circuits
  - PAM-n PD(Github: Jabdekhoda (github.com))
  - VCO (Github: https://github.com/WANG-Li-lwangbk)
  - AC-Coupled Sub-Sampling Charge Pump
  - R2R Comparator (Github: Jabdekhoda (github.com))

Practical Implementation Techniques

- Motivation
  - Practical Implementation Techniques
- Example 1
  - A Performance Study of Layout and Vt Options for Low Noise Amplifier Design in 65-nm CMOS [RFIC'12]
- Example 2
  - Differential Stacked Spiral Inductor and Transistor Layout Designs for Broadband High-Speed Circuits [RFIT'14]
- Example 3
  - Package Design for a 10 Gigabit Ethernet Transceiver [DesignCon'2004]
- Conclusion

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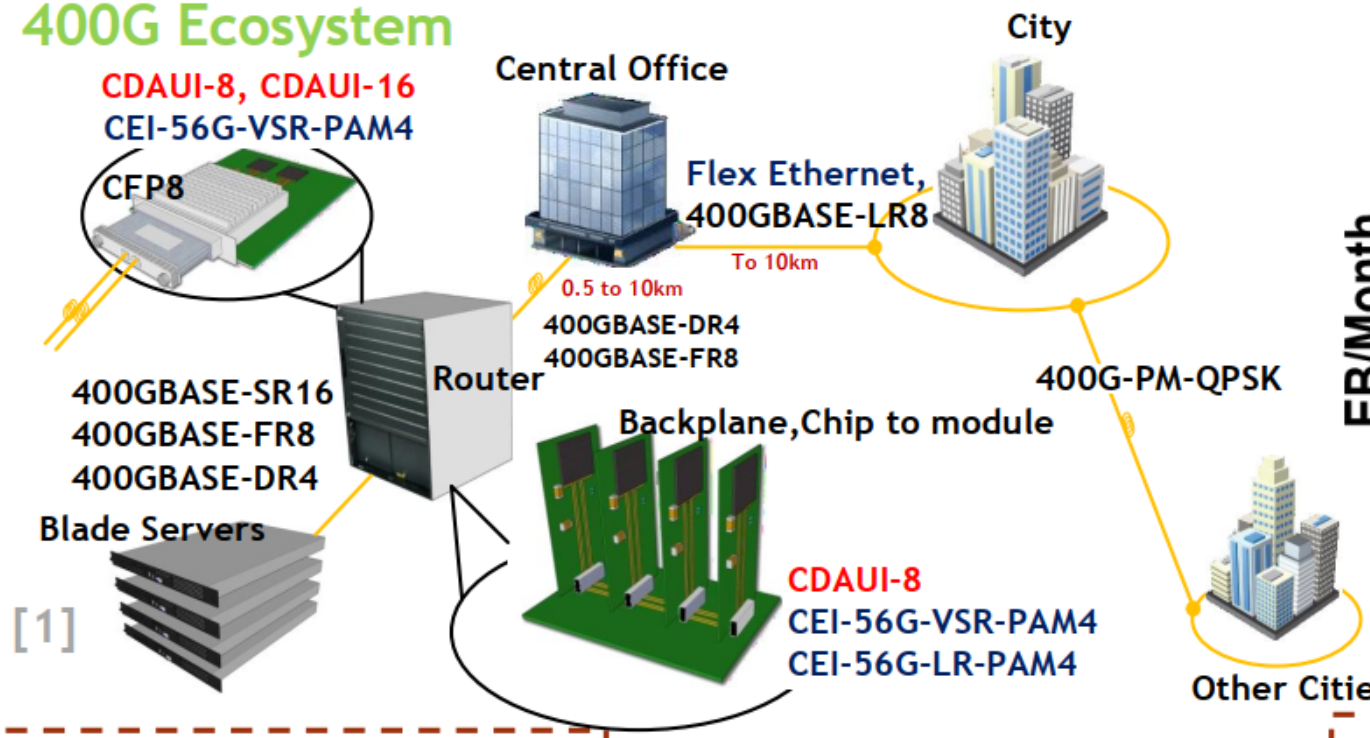
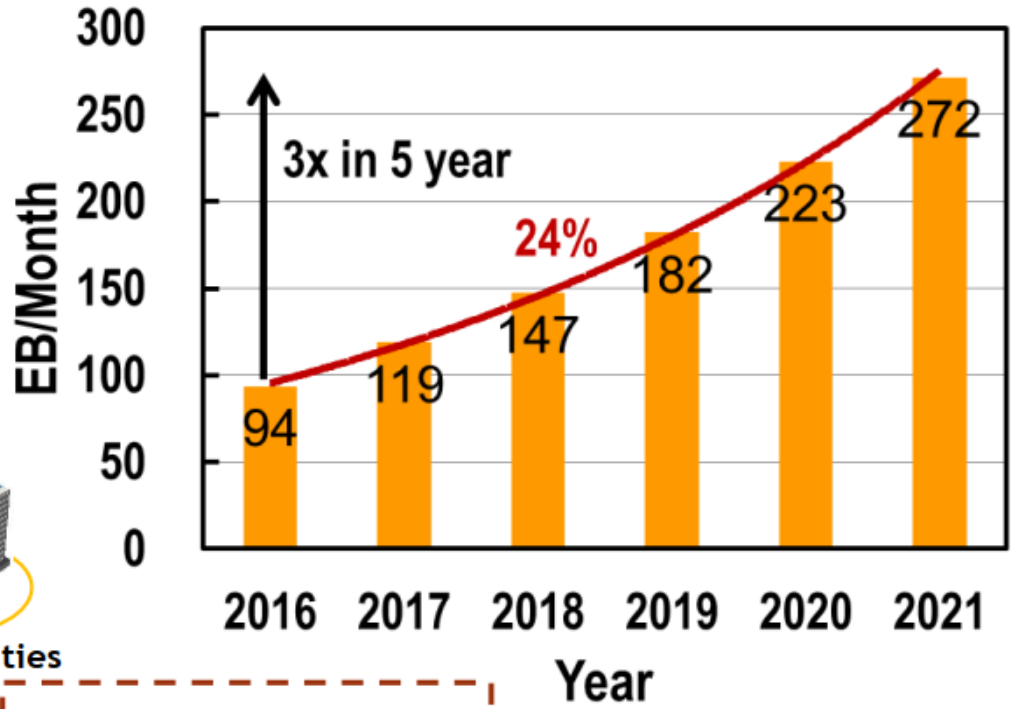
Background of Wireline and Optical Links
有线和光通信链路的研究背景

Prof. C. Patrick Yue 俞捷教授

芯动力人才计划®第 125 期国际名家讲堂

Wireline Link for Next Generation Ethernet





Global IP traffic Boom
5G Mobile Network
Internet of Things
Big Data & Cloud Computing

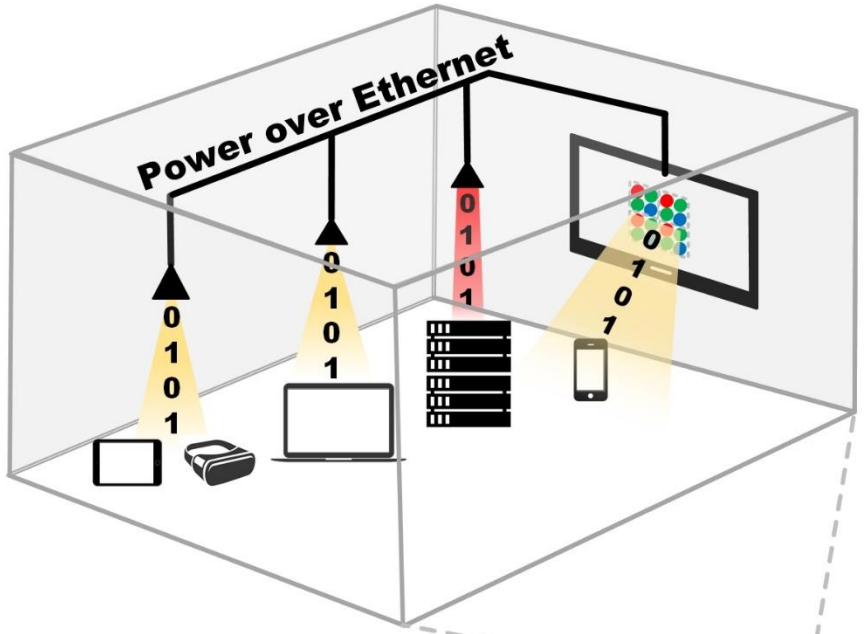
→ Increased data rate at every interfaces

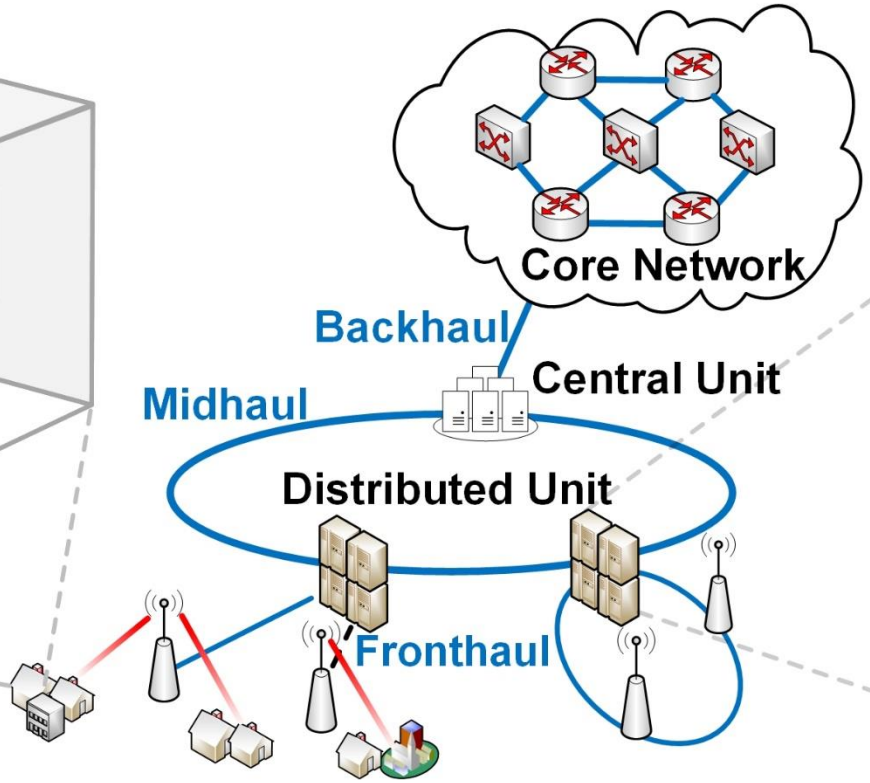
→ Severer channel loss
Higher power

→ Higher power consumption on communication & cooling system

Motivation: Energy efficient high-speed data communication

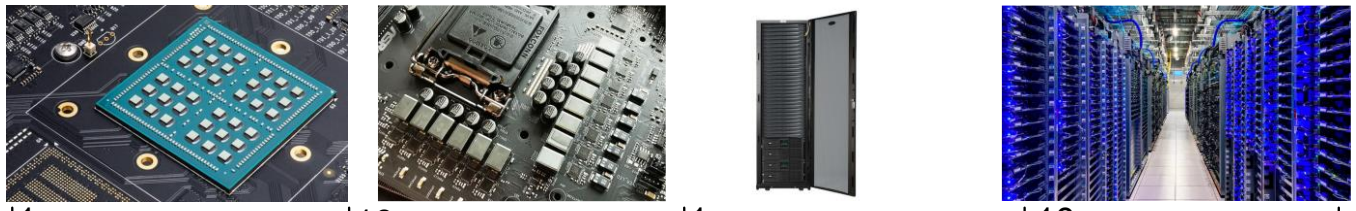
Optical Interconnections for 5G Network





- Optical links for long-distance inter data center communication
- Recently, optical I/O is also evolving towards short-reach and even with package communications

VCSEL and Silicon-Photonic Optical Transmitter

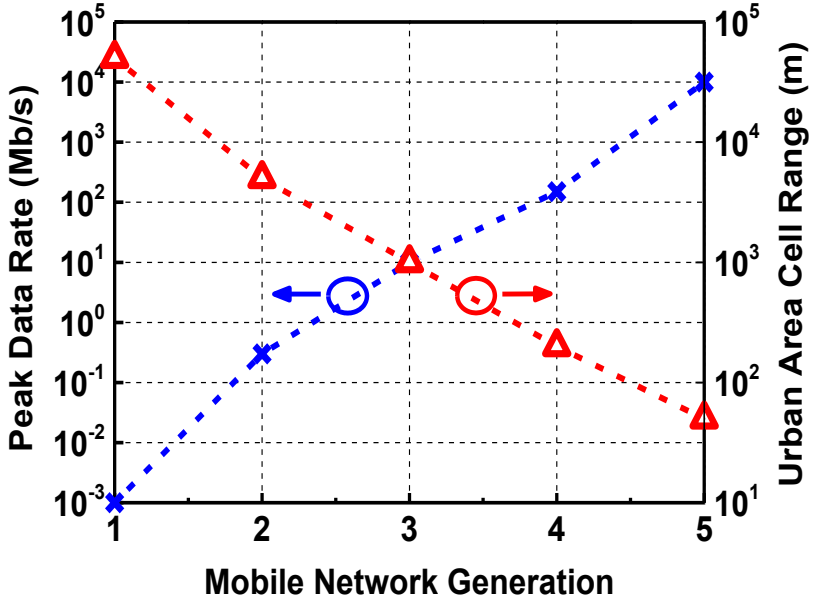


	Data Rate	Ethernet Standard	Channels	Modulation Scheme
VCSEL	400G	400GBASE-SR8	8	25Gbps NRZ
	400G	400GBASE-SR8	8	50Gbps PAM-4
Single-mode optics, e.g. Si-PH MRM	400G	400GBASE-PSM16	16	25Gbps-λ: NRZ
	400G	400GBASE-PSM8	8	50Gbps-λ: NRZ or PAM-4

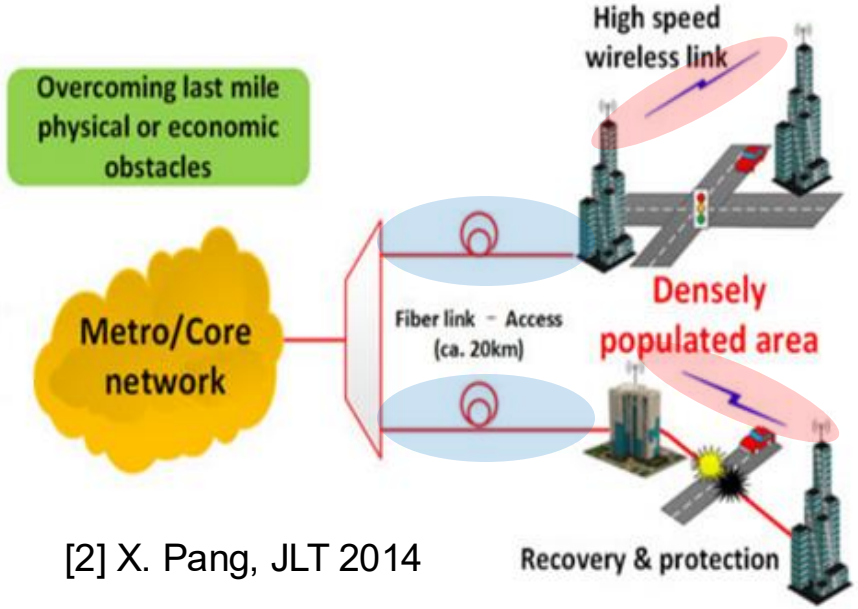
Beyond Optical and Wireline

- Fiber-Wireless Network

Evo. of Cellular Networks



Fiber-Wireless Network

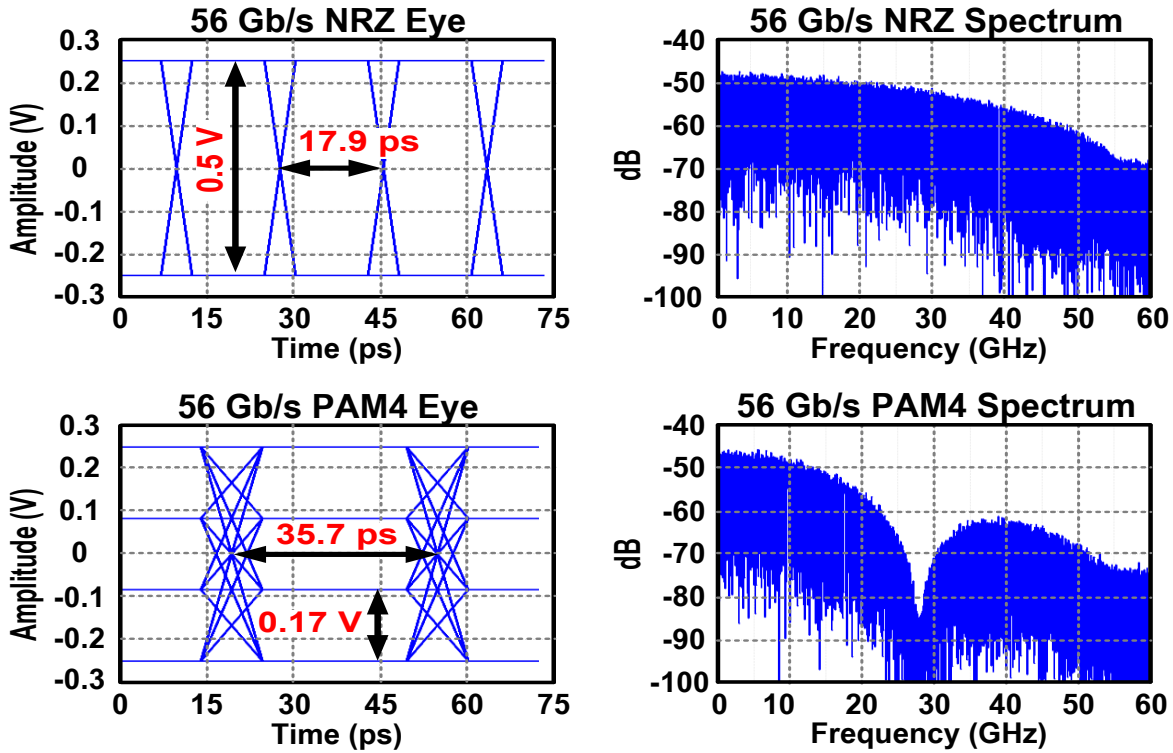


[2] X. Pang, JLT 2014

- 5G mobile network requires ultra-dense cellular cells
- Backhaul links deployment is challenging
- Fiber-wireless networks provide high performance and flexible backhaul link connections

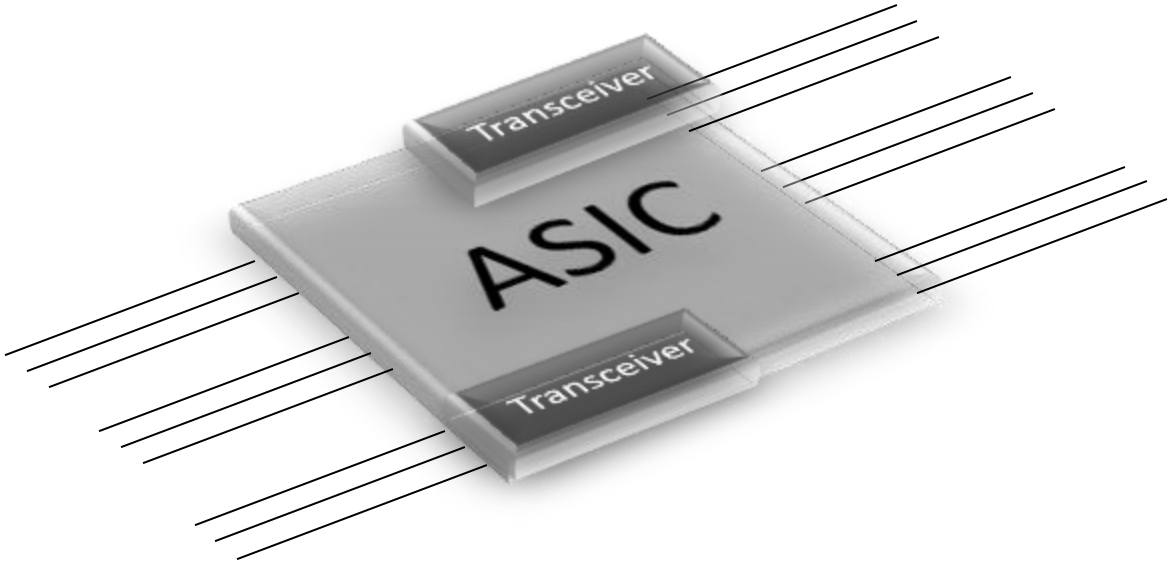
Wireline Rx: PAM4 vs. NRZ

- PAM4 Rx trades SNR for time/frequency efficiency
- PAM4 Rx meets new design issues
  - PAM4-to-NRZ decoding for DSP
  - CDR and equalizer with complicated data levels/transitions



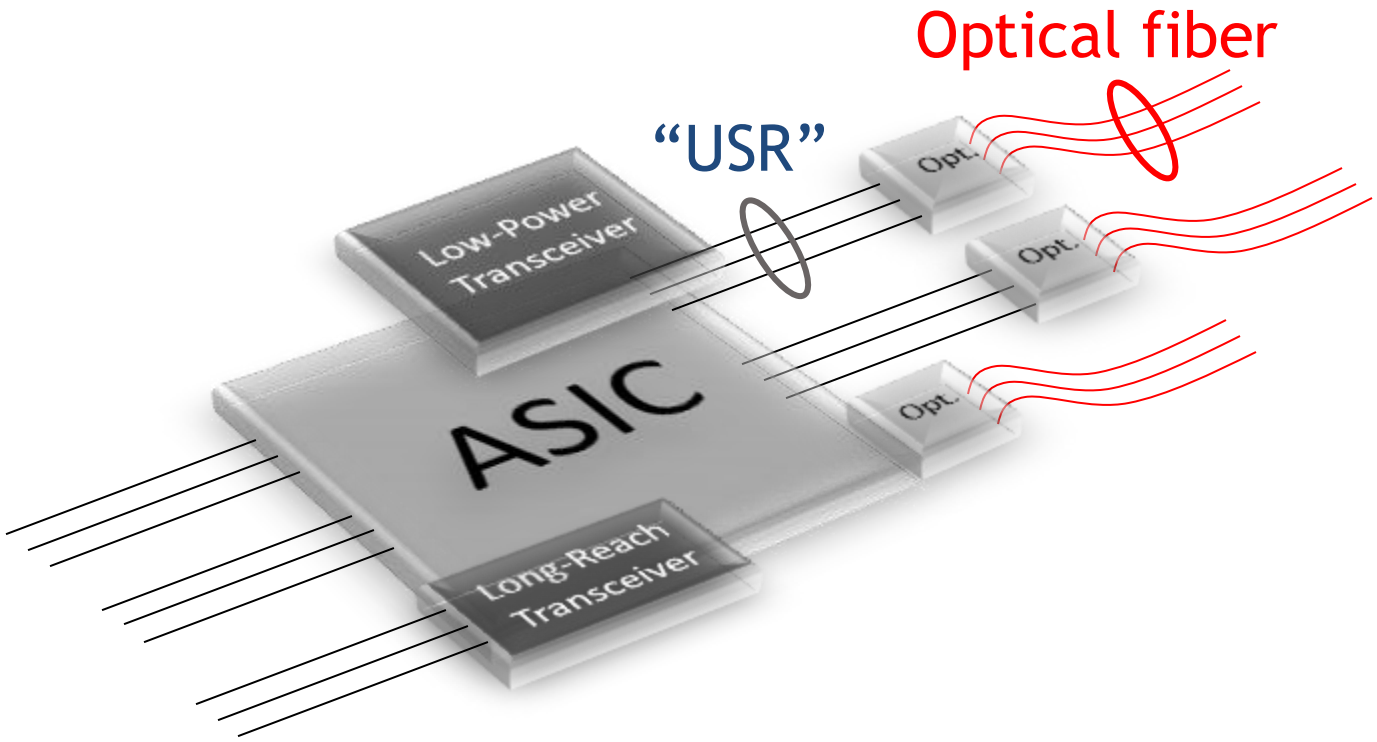
Modern Wireline Transceivers

- Low-power across a wide range of channel losses for copper interconnect
- Transceivers for optical modules focusing on low-cost and low-power
- Relatively simple 2-PAM and 4-PAM modulation with linear and/or decision-feedback equalization
- Forward error control coding



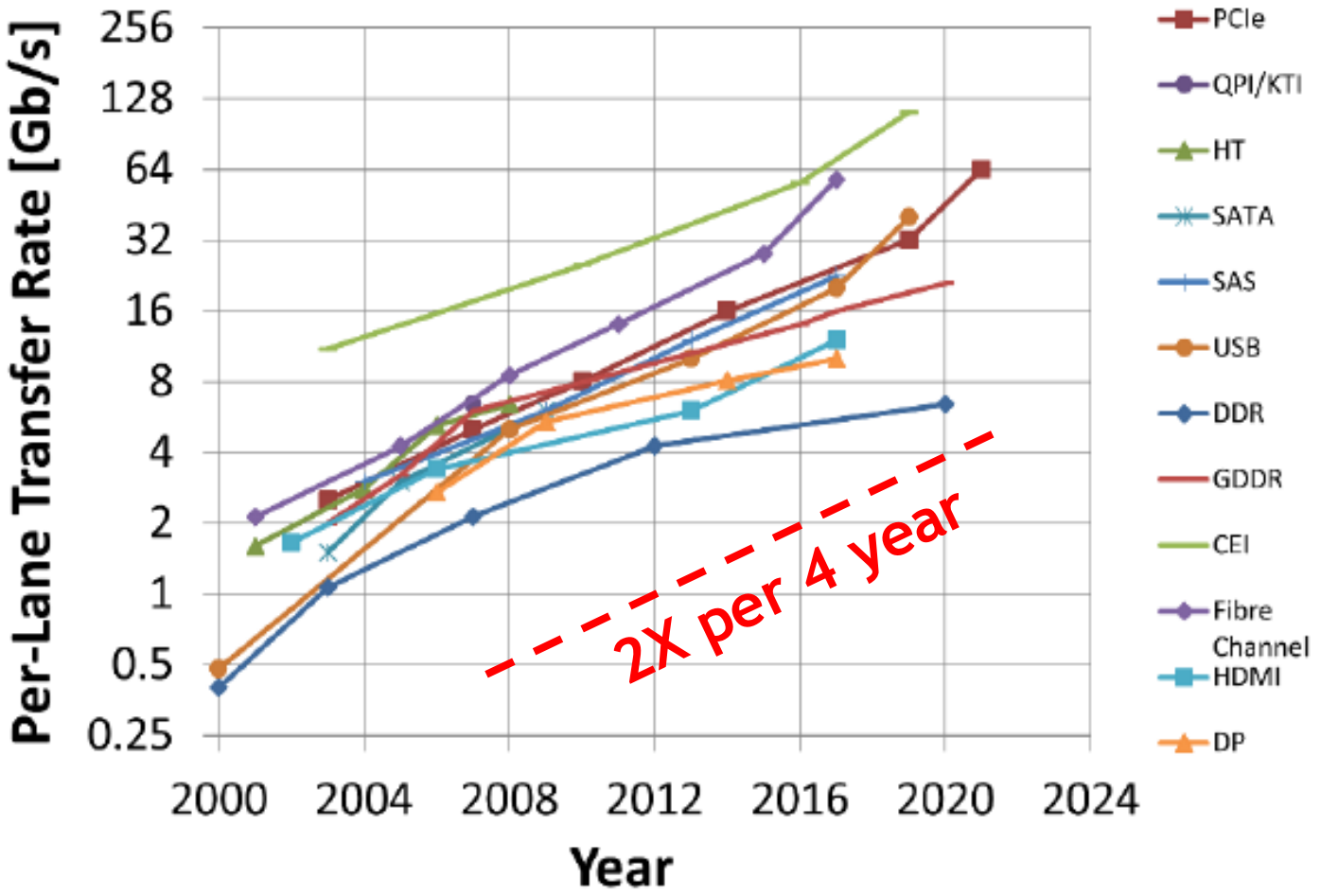
Paving the Way to 200Gb/s Transceivers

- Optical Transceivers that are Compact and Co-Optimized
- Modulation and Coding with Increasingly Co-Optimized DSP for Long-Reach Transceivers
- Extremely Short and Within-Package Transceivers Focusing on Low Power



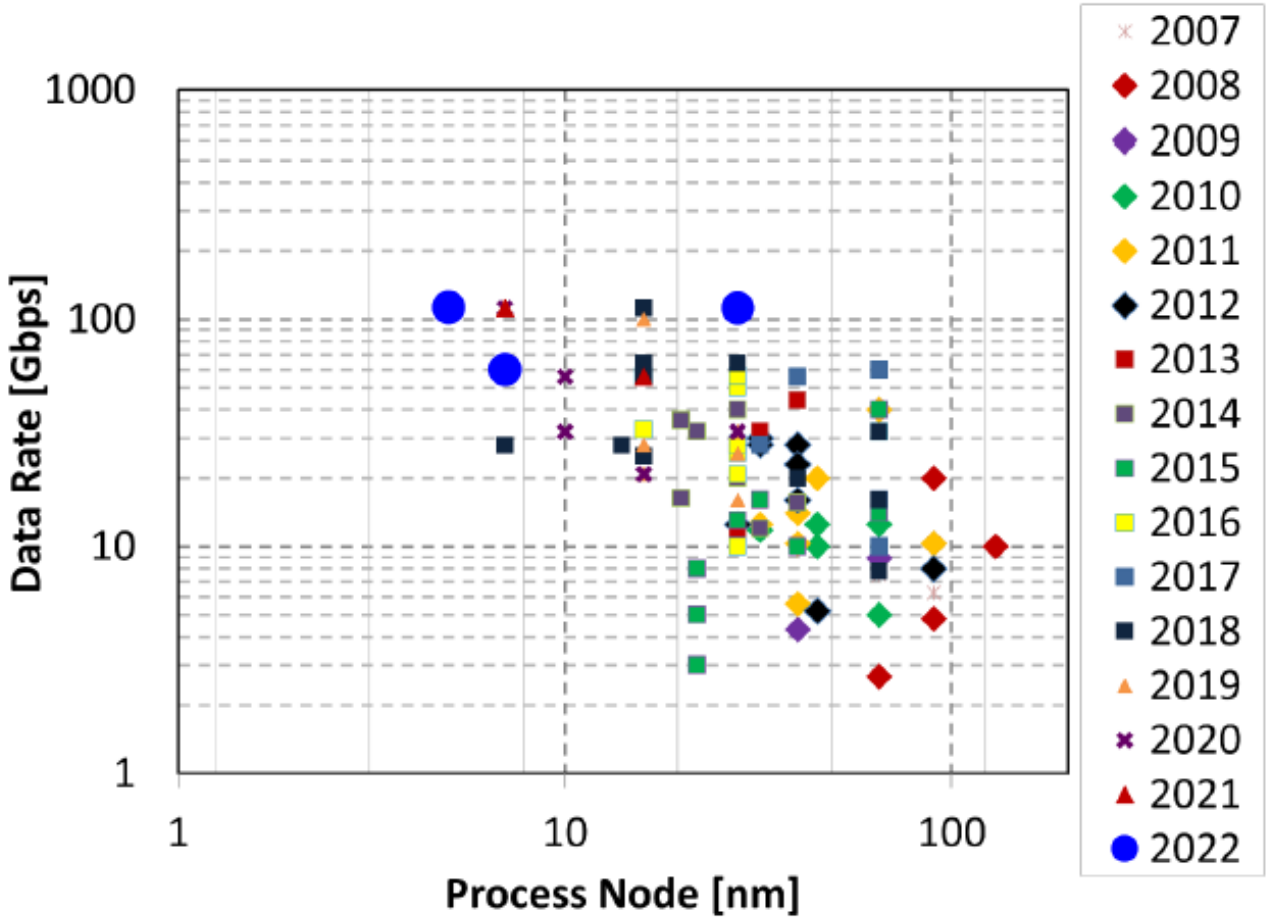
Trend: Per-Lane Data Rate Growth vs. Year

- Data-rate per pin has approximately doubled every four years across various I/O standards ranging from DDR, to graphics, to high-speed Ethernet.



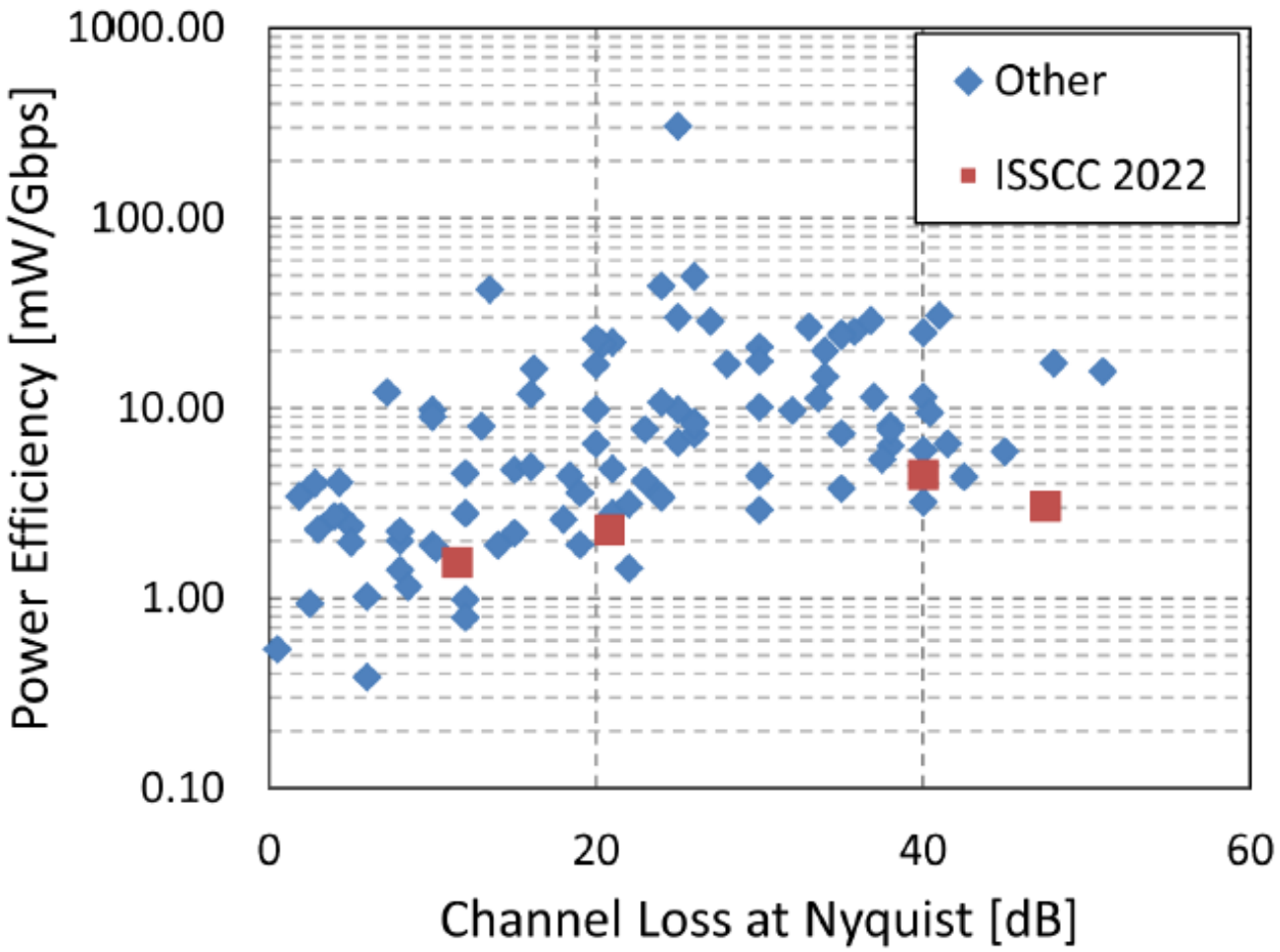
Trend: Data Rate vs. Process Node

- PAM4 transceivers have kept pace at 56Gb/s and 112Gb/s while taking advantage of CMOS scaling down to 5 nm for more aggressive channel loss compensation



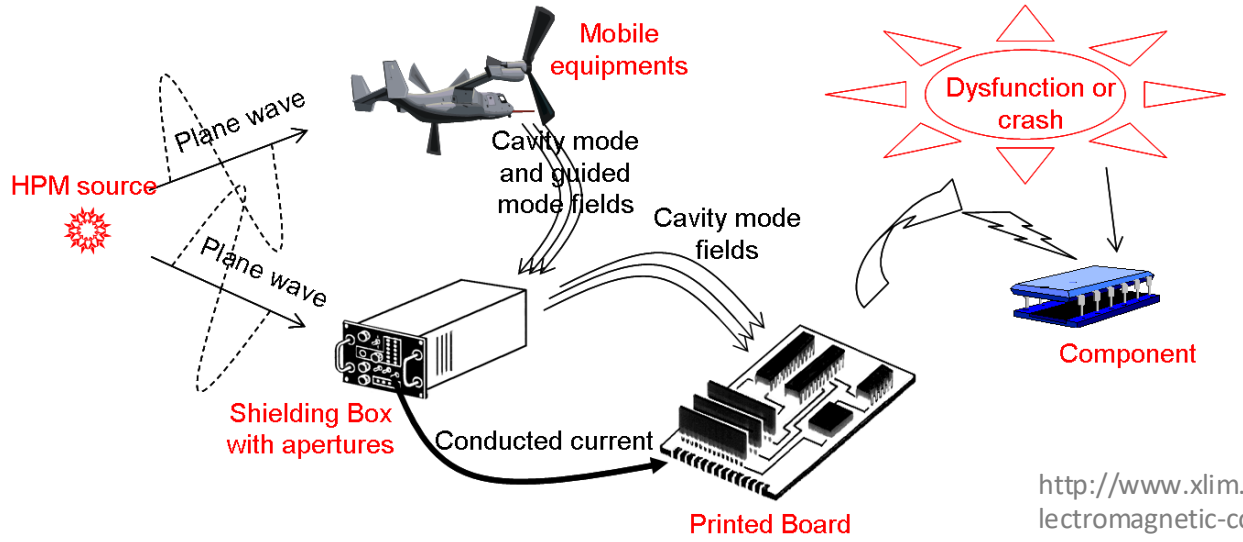
Trends: Bit Efficiency vs. Channel Loss

- Channel loss compensation by different equalization techniques
- Power efficiency better than ~1-2 pJ/bit only for Short Reach with < 20 dB loss
- Power efficiency ~5-10 pJ/bit for Long Reach with up to 50 dB loss



EMI Issues in Advanced Data Center

- Most electronics generate electromagnetic emission



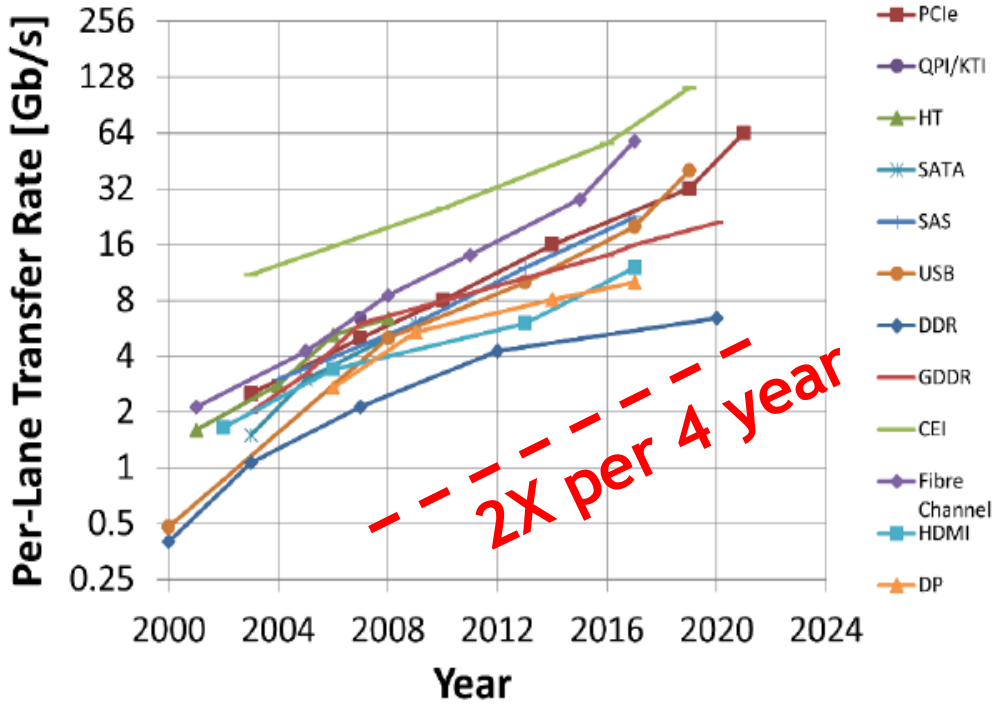
http://www.xlim.fr/en/osa/electromagnetic-compatibility

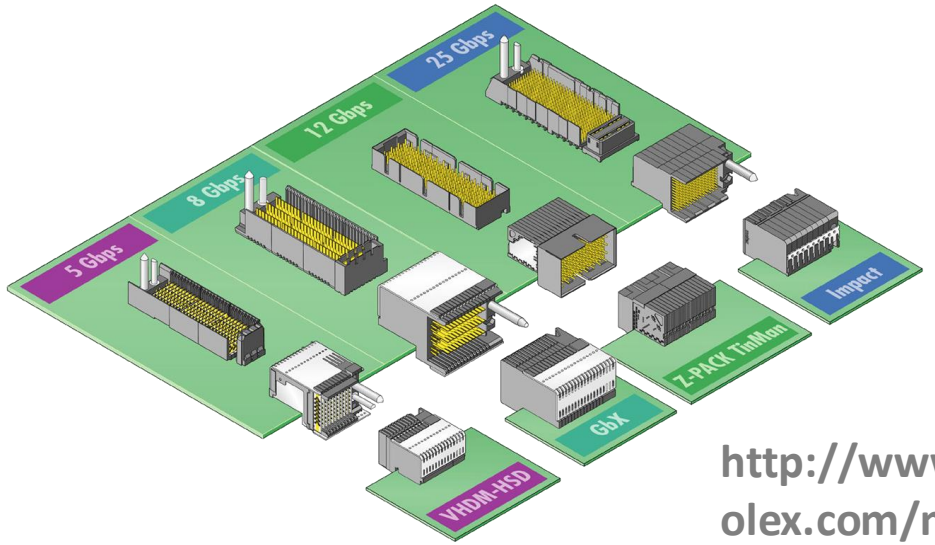
- Electromagnetic interference (EMI) causes malfunction of the victim electronics
- How to solve?
  - Keep enough distance, be robust, and keep quiet

EMI Issues in Advanced Data Center

- Front-side haven, but back-side disaster
- Thousands of paralleled communication modules
  - Data rate of each module > 10 Gbps
- Complicated electromagnetic environment

EMI Issues in Advanced Data Center

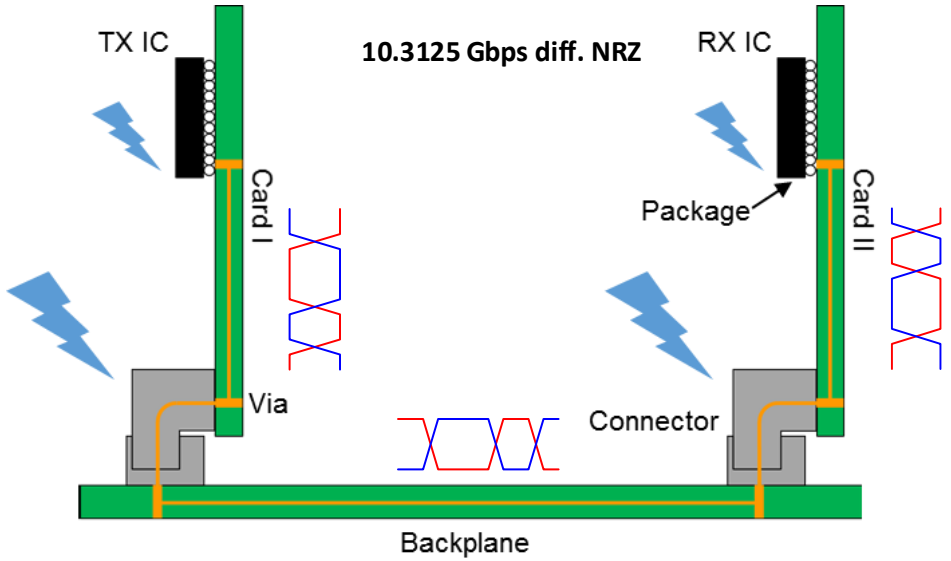


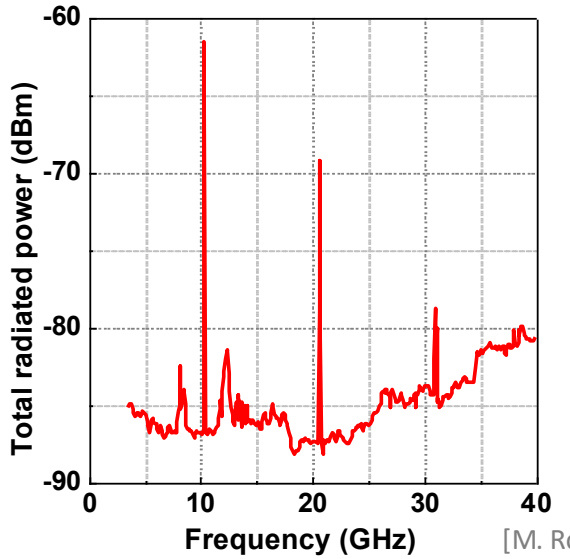


http://www.molex.com/mx_upload/family//NEW_BP_Roadmap.pdf

- **High-speed backplane connectors roadmap**
  - Higher data rate↑, higher data density↑
- **For each backplane link**
  - Smaller physical dimension, closer distance
  - Be more robust and quieter

EMI Case Study in Backplane Link





[M. Rowlands, DesignCon 2015]

- **EMI radiation of backplane communication module**
  - EMI radiations at $2f_{Nyquist}$, $4f_{Nyquist}$, … (e.g., 10 Gbps NRZ, $f_{Nyquist}$ = 5 GHz)
  - Ideal NRZ* data has no frequency component @ $2f_{Nyquist}$, $4f_{Nyquist}$, $6f_{Nyquist}$ …
    - NRZ = non-return-to-zero
- **Distorted differential NRZ signals**

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Wireline and Optical Transmitters
有线和光发射机

Prof. C. Patrick Yue 俞捷教授

芯动力人才计划®第 125 期国际名家讲堂

Section Outline

- Architecture
  - VCSEL Transmitter
  - MRM Transmitter
  - MZM Transmitter
  - Wireline Transmitter
- Key Circuits
  - Multiplexer

    (Now Opensource: https://github.com/HKUST-ECE-IC-Design-Center-OWL/SHARE-by-OWL-HKUST-4to1-MUX-for-28Gbaud-Optical-TX)
  - Output Driver
  - Pre-emphasis
- Practical Issues
  - EMI Suppression Due to CM Noise to Reduce Radiation Emissions

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香港科技大學
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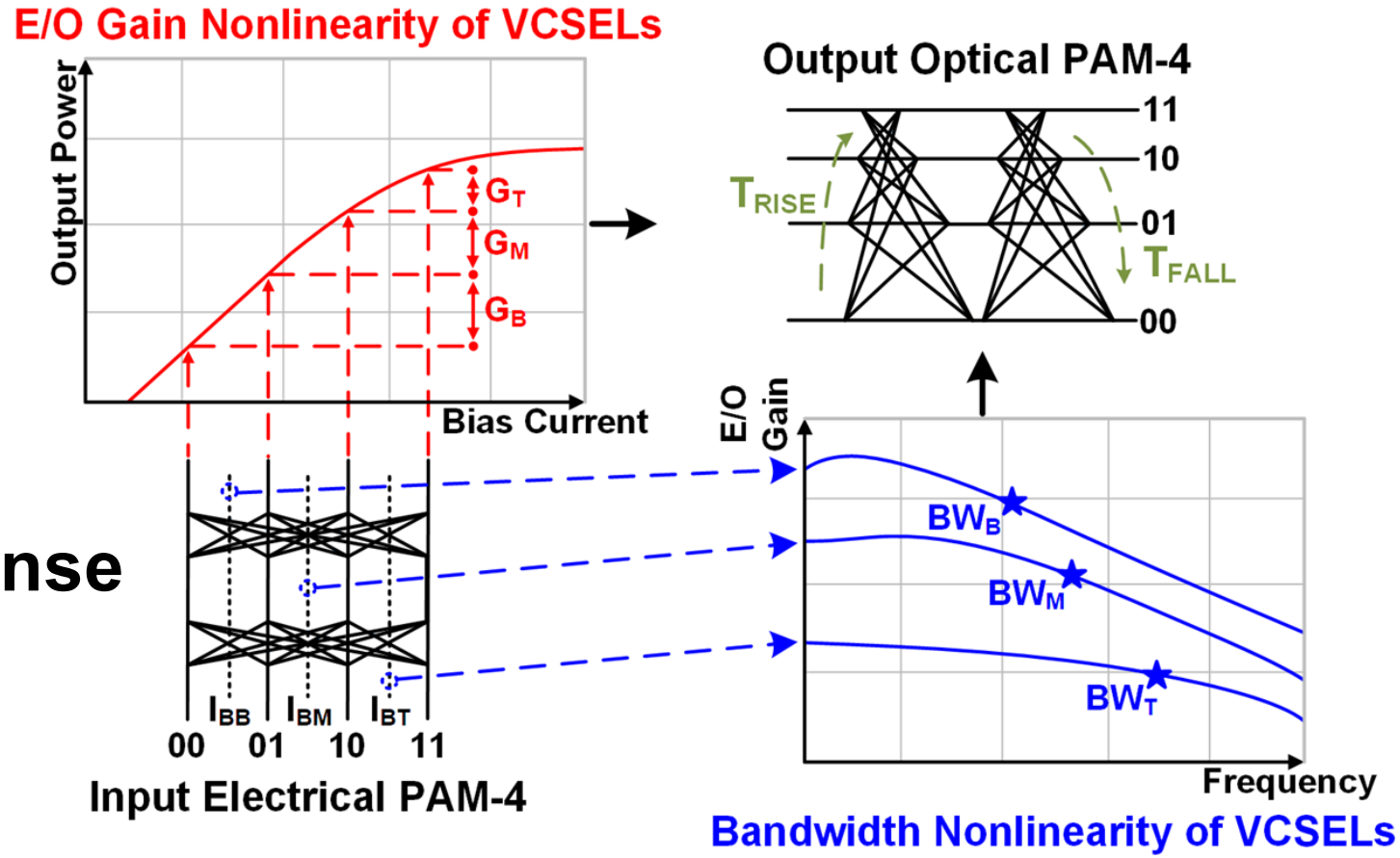
HKUST OWL

A 56-Gb/s PAM-4 VCSEL Transmitter with Piecewise Nonlinearity Compensation and Asymmetric Equalization

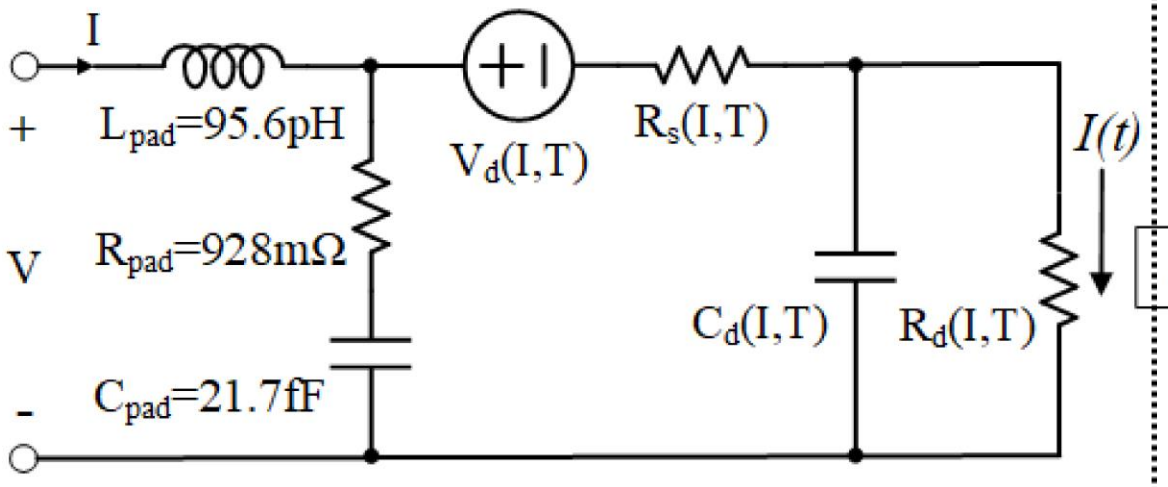
Non-idealities of VCSEL

- **Bias current ↑, E/O gain ↓**
  - $G_B > G_M > G_T$
- **Bias current ↑, E/O BW ↑**
  - $BW_B < BW_M < BW_T$
- **Asymmetric rise/fall response**
  - $T_{RISE} < T_{FALL}$



VCSEL Modeling

R-L-C Part



Verilog-A Part

$$\frac{dN(t)}{dt} = \frac{I(t)}{qV_a} - \frac{N(t)}{\tau_n} - g_0(T)\frac{N(t)-N_0}{1+\varepsilon(T)S(t)}S(t)$$

$$\frac{dS(t)}{dt} = \Gamma g_0(T)\frac{N(t)-N_0}{1+\varepsilon(T)S(t)}S(t) - \frac{S(t)}{\tau_p} + \frac{\Gamma\beta N(t)}{\tau_n}$$

$$P_{opt} = \frac{S(t)V_a h\nu}{2\Gamma\lambda}k\eta(T)$$

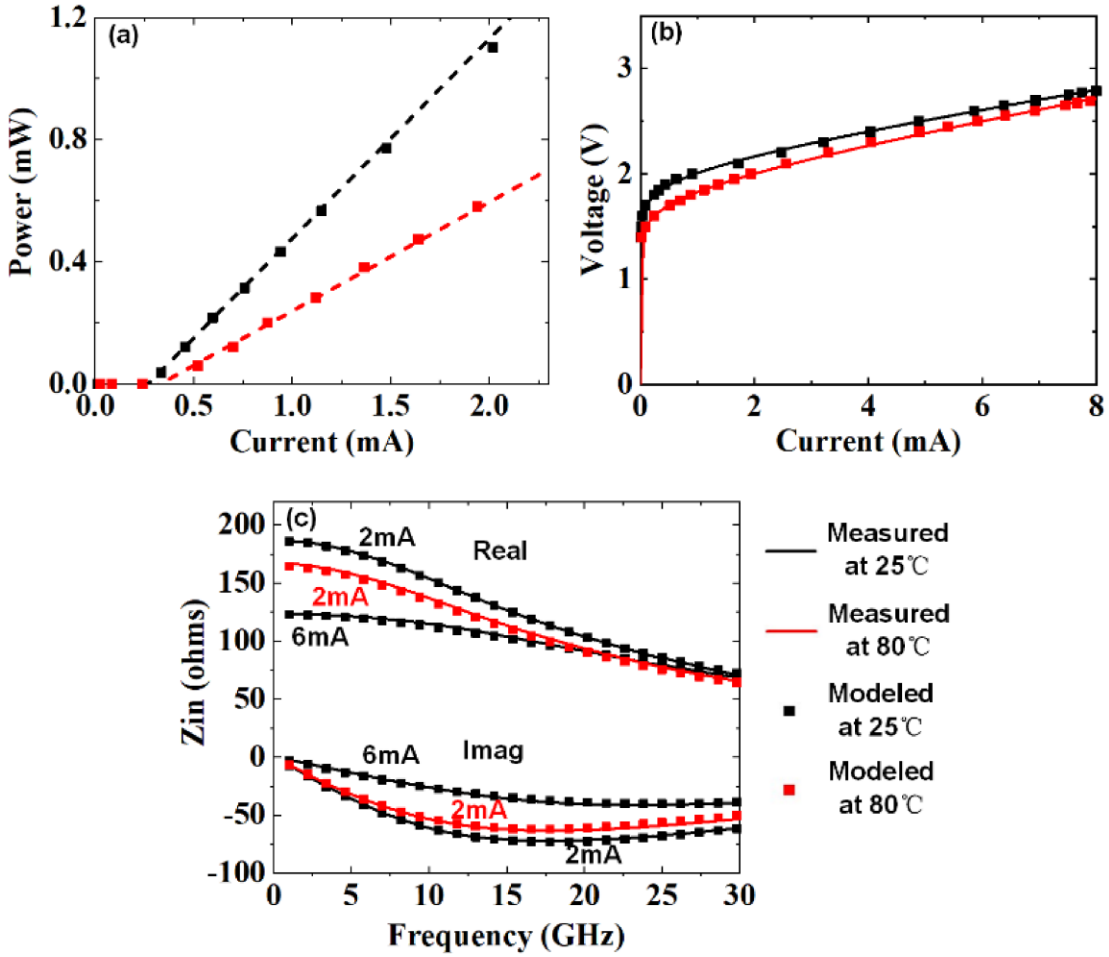
N(t): Carrier density
S(t): Photon density

I(t) → P_{opt}

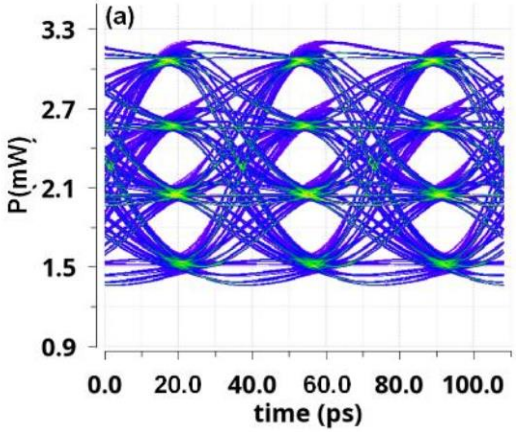
- V_a: volume of active region,
- τ_n: carrier lifetime,
- g_0: gain slope coefficient,
- N_0: transparency carrier density,
- τ_p: photon lifetime,
- ε: gain compression factor,
- Γ: optical confinement factor,
- β: spontaneous capture efficiency,
- q: electron charge.

VCSEL Modeling

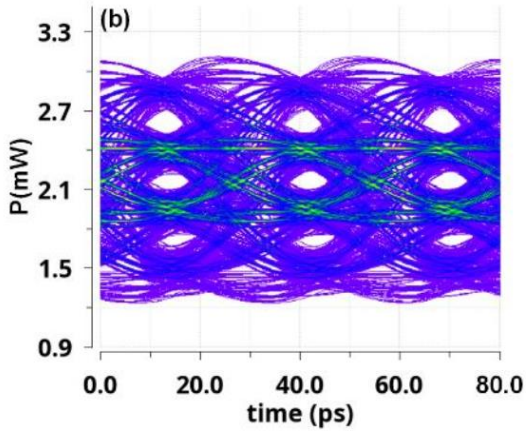
Simulation vs. Measurement



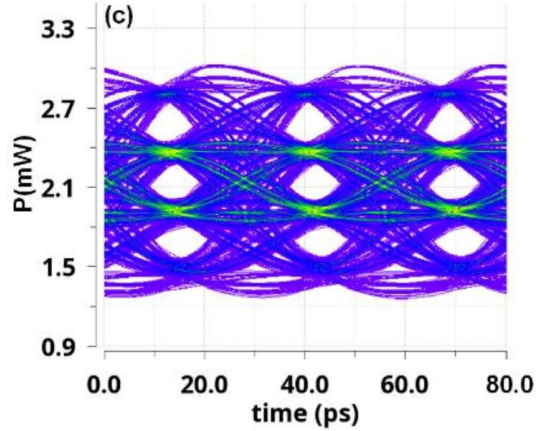
Simulated Eye Diagrams



56 Gb/s, 25 °C

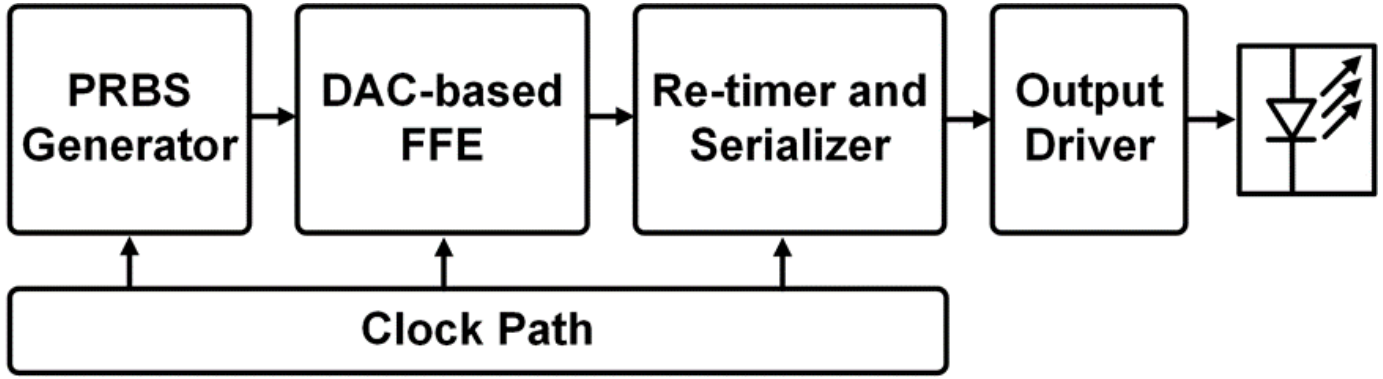


72 Gb/s, 80 °C

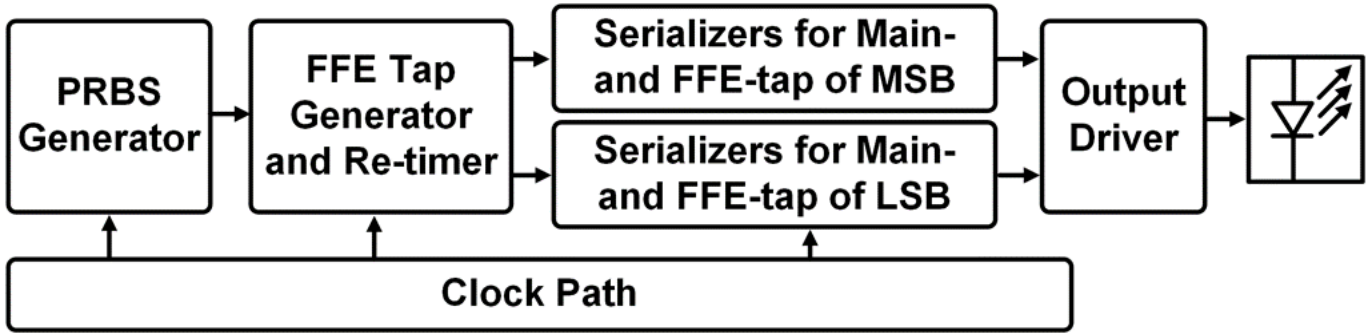


72 Gb/s, 80 °C, FFE ON

Prior VCSEL TX Works



- **DAC-based FFE**[1][2]
  - Large die area
  - High link latency

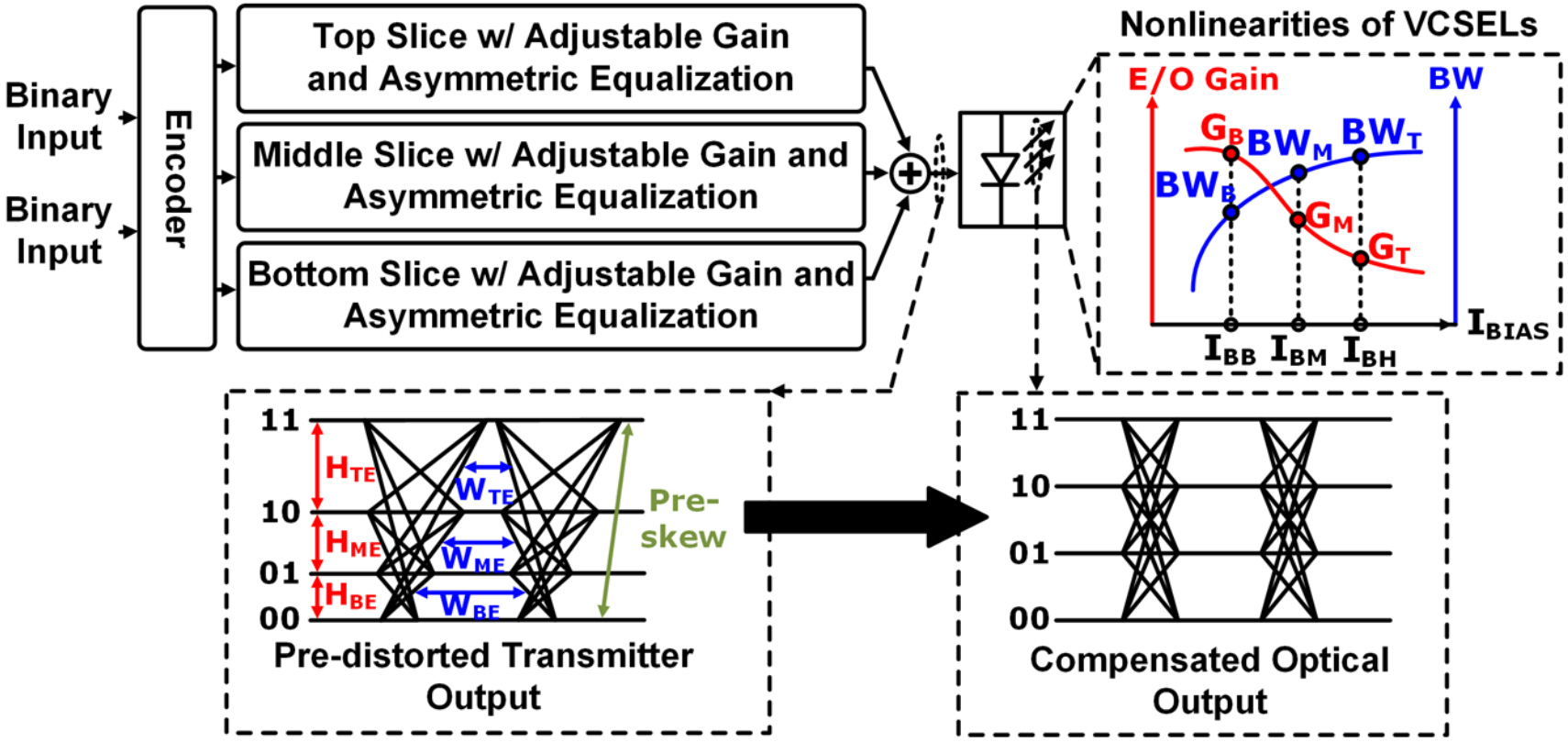


- **Analog asymmetric FFE**[3][4]
  - Cannot fully compensate for VCSEL non-idealities

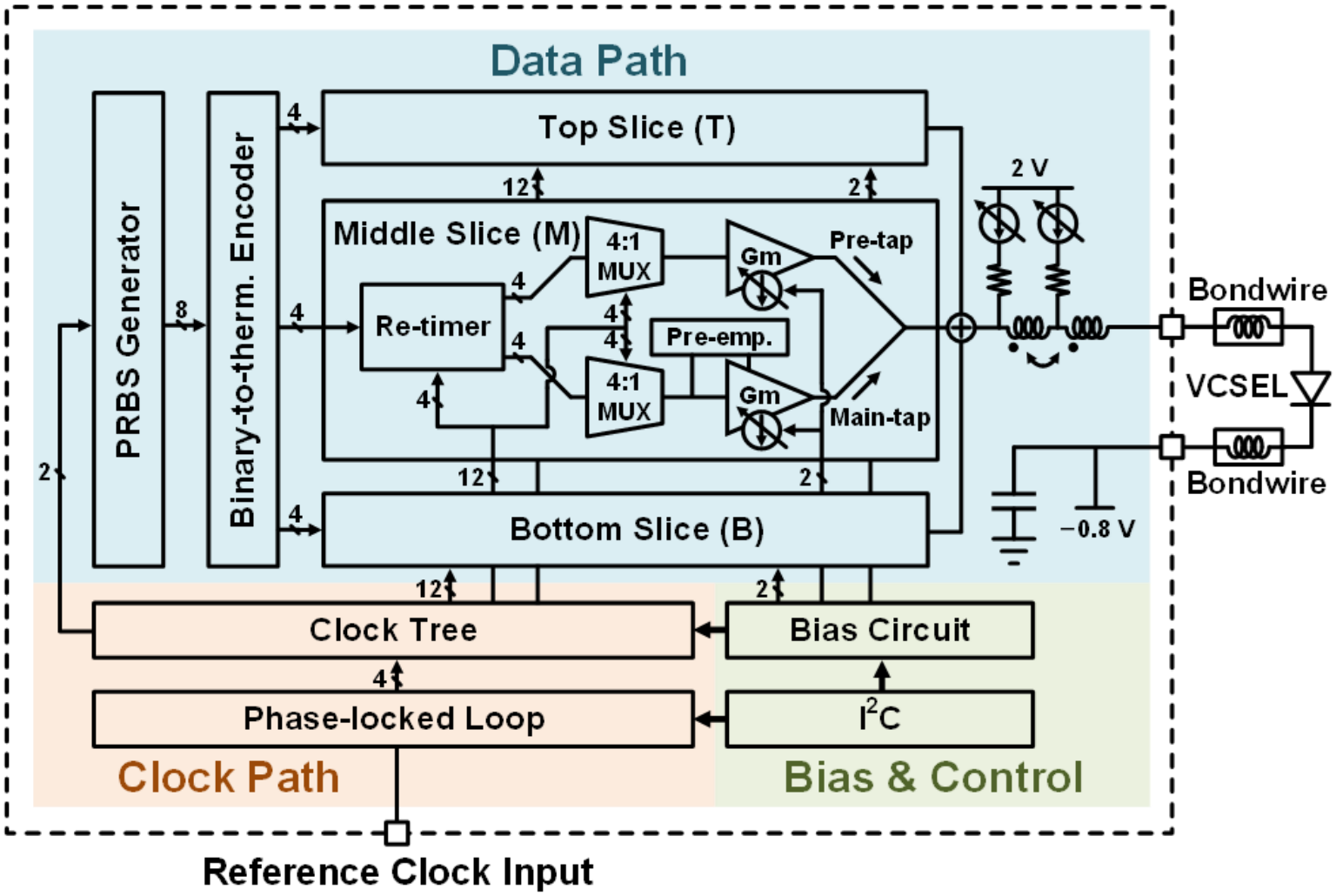
[1] A. Tyagi *et al.*, *PTL,* 2018 [2] P.-J. Peng *et al.*, *JSSC,* 2022 [3] J. Hwang *et al.*, *VLSI*, 2019 [4] H. Do *et al.*, *ASSCC*, 2021

Proposed Compensation Methods

- Thermometer code-based architecture for piecewise compensating E/O gain and E/O BW nonlinearities
- Asymmetric pre-emphasis for relieving asymmetric optical response

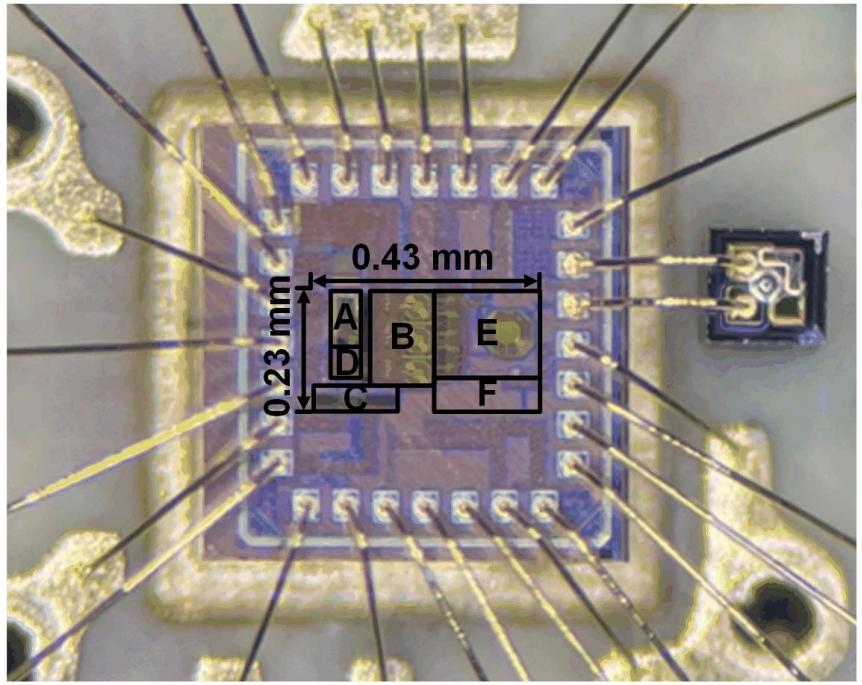


VCSEL TX Architecture



- **Data path**
  - 2-tap FFE
  - Gm cell-merged CTLE
  - Pre-emphasis circuit
- **Clock path**
  - Wideband PLL
  - Clock tree with VCDLs
- **Optical part**
  - Wide-bonded anode-driven VCSEL

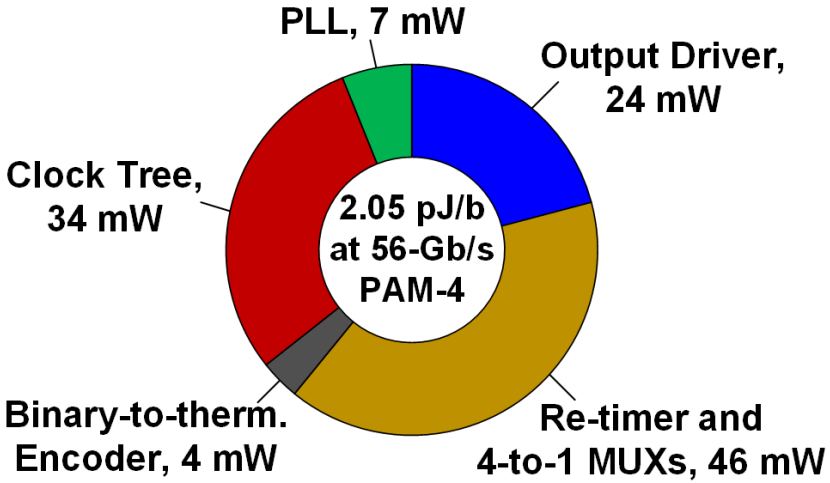
Measurement Overview



- Fabricated in 40-nm bulk CMOS
- Transmitter core occupies ~0.1 mm^2
- Consumes 115 mW at 56-Gb/s PAM-4

A — PRBS Generator + Binary-to-therm. Encoder
B — Re-timer + 4-to-1 Multiplexers
C — Phase-locked Loop
D — Clock Tree
E — Output Driver
F — Bias Circuit + I^2C

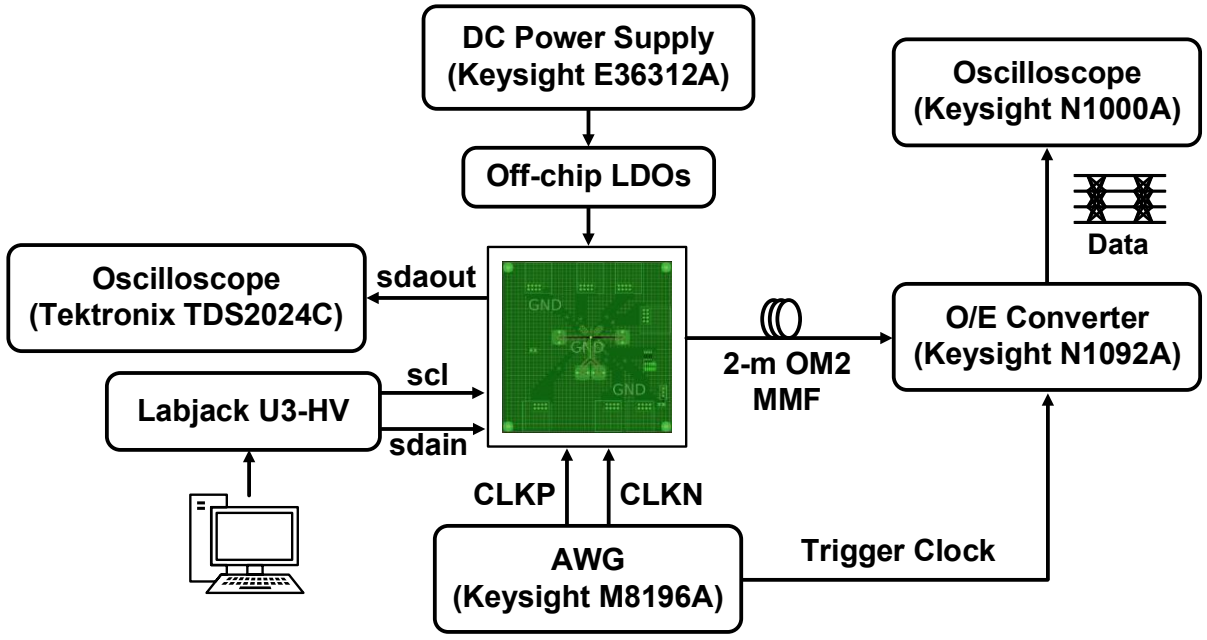
Power Breakdown



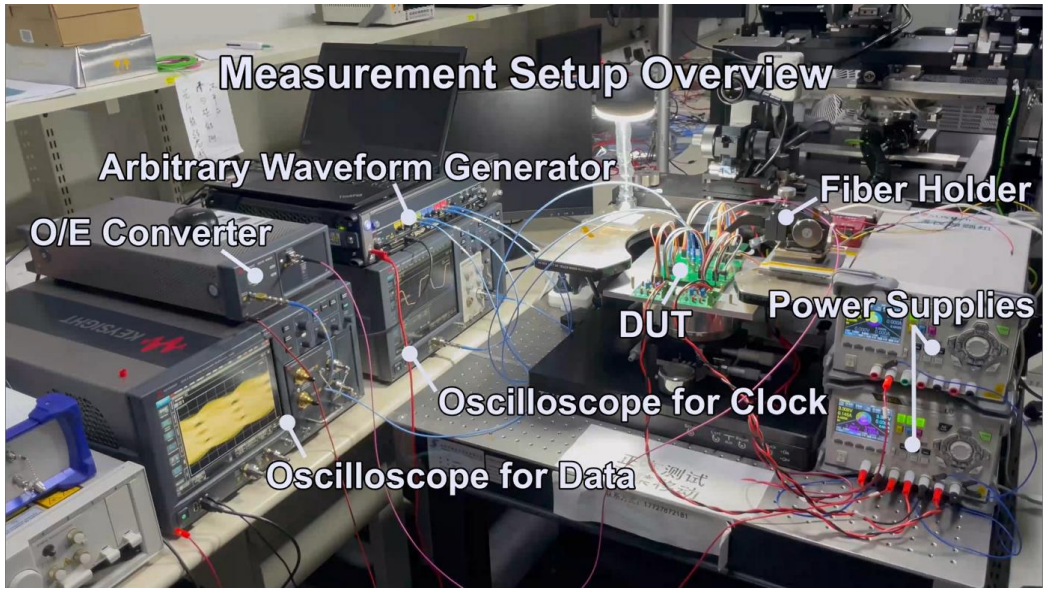
Measurement Setup

- A commercial VCSEL wire-bonded with the TX for optical measurements
- The optical signal is butt-coupled to the multi-mode fiber

Scan to Watch Measurement Video

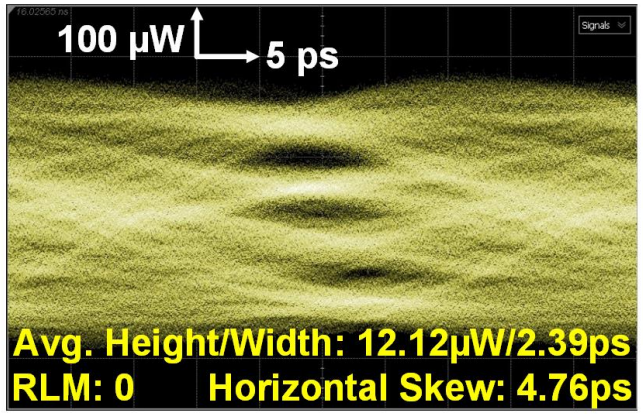


Measurement Setup

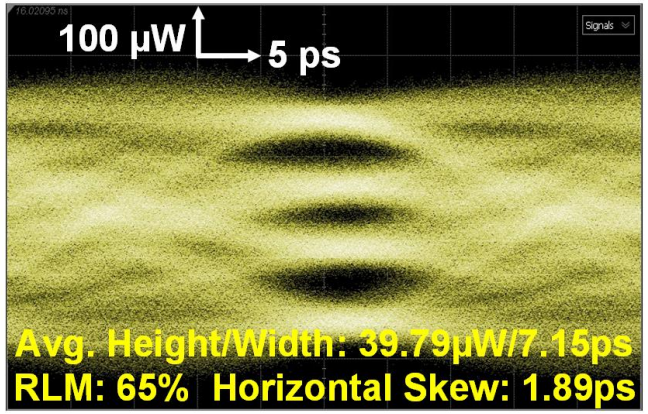


Measurement Environment

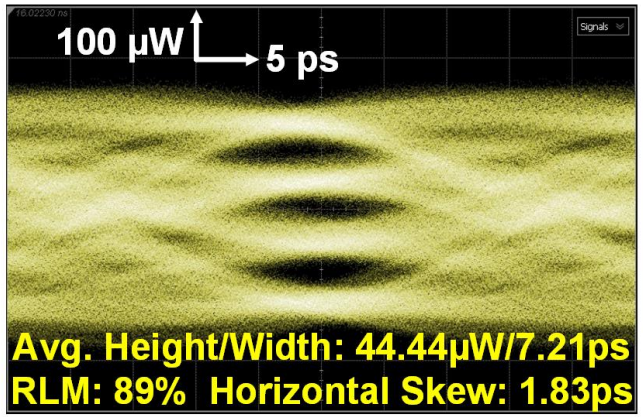
Measurement Results



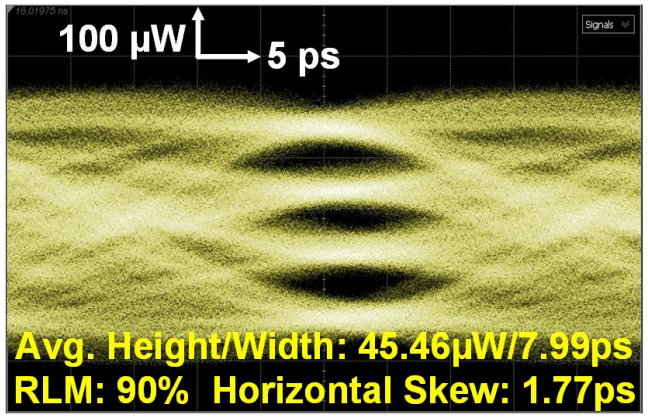
(a) EQ OFF, Equal Slice Gain



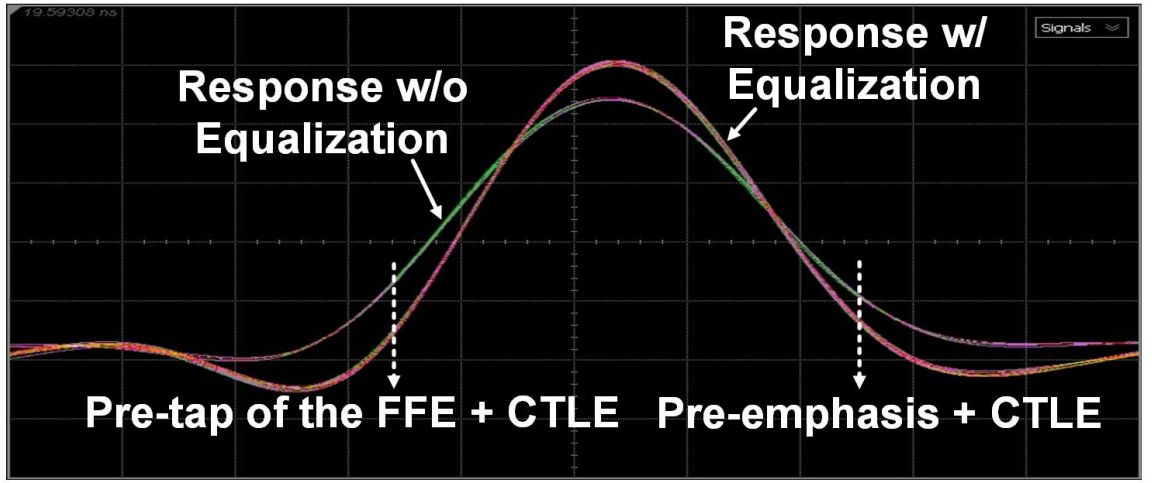
(b) EQ ON, Equal Slice EQ, Equal Slice Gain

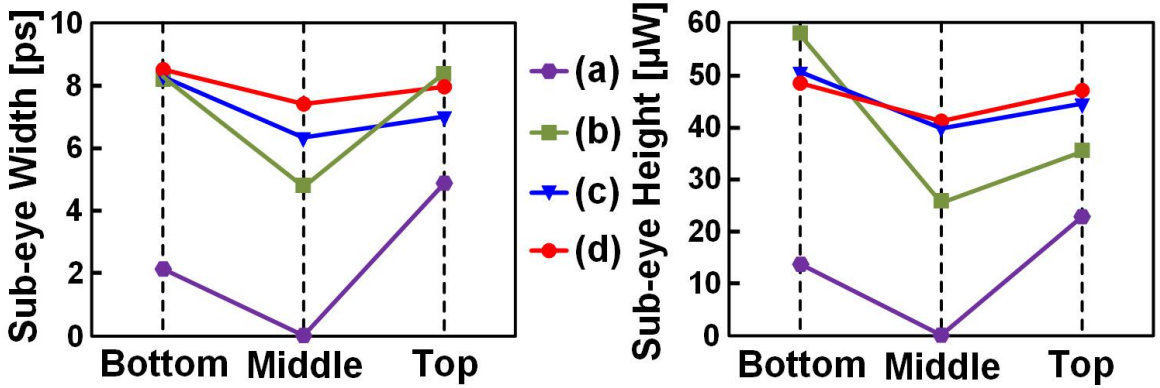


(c) EQ ON, Equal Slice EQ, Piecewise Tuned Slice Gain



(d) EQ ON, Piecewise Tunned Slice EQ and Slice Gain





Comparison with Prior Works

	PTL'18 A. Tyagi *et al.*	JSSC'22 P.-J. Peng *et al.*	VLSI'19 J. Hwang *et al.*	ASSCC'21 H. Do *et al.*	This work
CMOS Node [nm]	65	40	65	40	40
Architecture Signaling Scheme	1/2-rate PAM-4	1/4-rate PAM-4	1/4-rate PAM-4	1/4-rate PAM-4	1/4-rate PAM-4
Data Rate [Gbps]	50	56	64	64	56
OMA [mW]	2.00	0.81*	2.50*	1.08*	1.18*
Power effi. [pJ/b]	5.12	1.73	2.69#	2.09	2.05#
Core Area [mm^2]	0.31	0.47	0.28	0.16	0.10
Asymmetric Equalization	2.5-tap DAC-based FFE	2-tap DAC-based FFE	3-tap LSB/MSB-based Asym. FFE	3-tap LSB/MSB-based Asym. FFE	2-tap FFE + CTLE + Pre-emphasis
Nonlinearity Compensation	Full	Full	Partial	Partial	Full
Method Type	Digital	Digital	Analog	Analog	Mixed-signal

*3-dB butt coupling loss de-embedded
#Includes on-chip PLL

Conclusion

A PAM-4 VCSEL transmitter in 40-nm CMOS

- The piecewise nonlinearity compensation improves optical eye height/width and RLM by 14%/12% and 38%, respectively
- The asymmetric equalization scheme reduces the horizontal optical eye skew by 63%
- The transmitter achieves a power efficiency of 2.05 pJ/b at 56-Gb/s PAM-4
- The core occupies a die area of 0.1 mm^2

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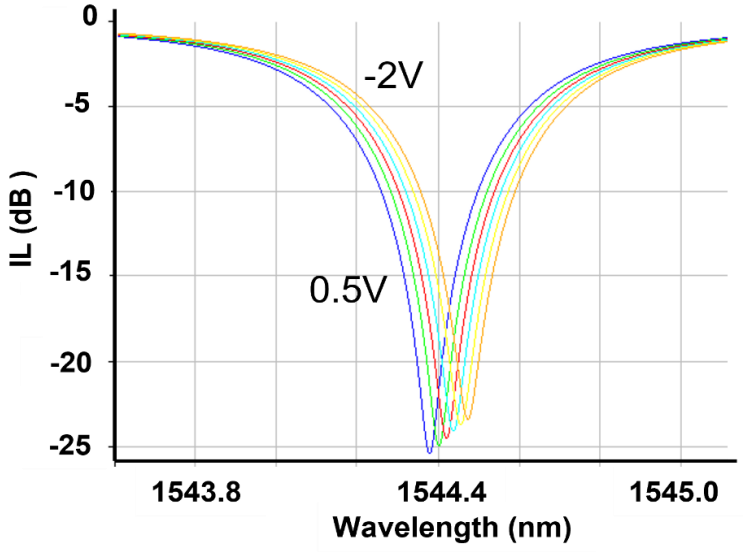
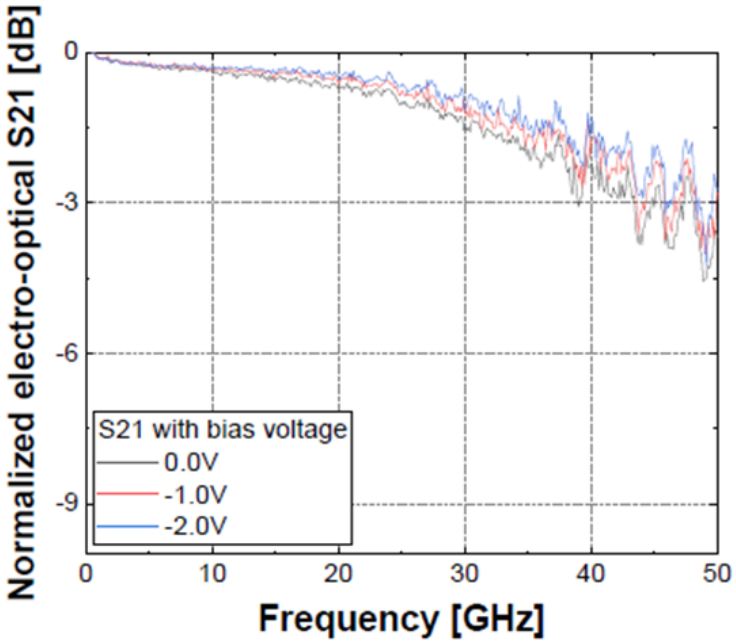
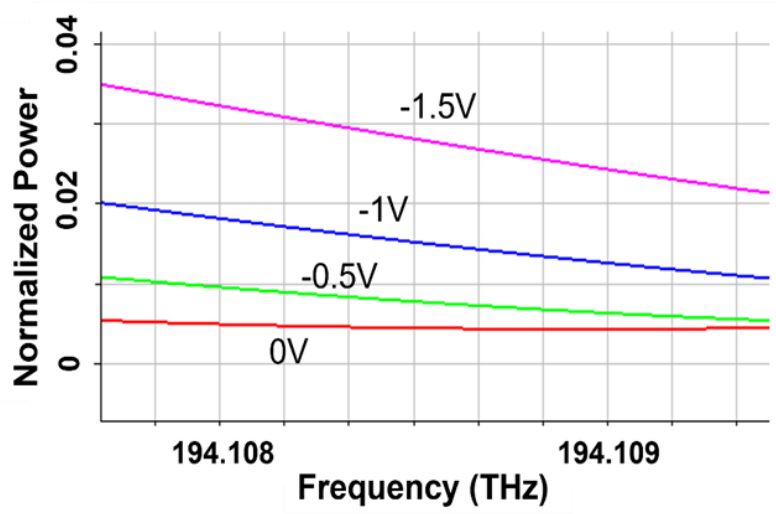
A 56-Gb/s PAM-4 Transmitter Using Silicon Photonic MRM in 40nm CMOS

MRM Characteristics







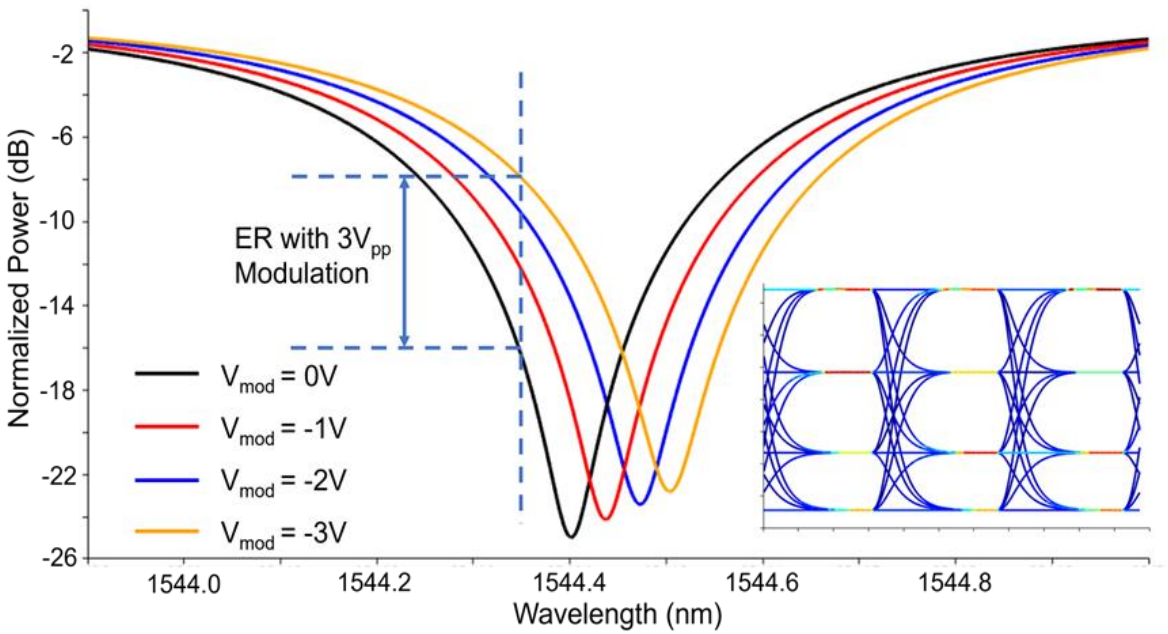
[M. Pantouvaki, JLT'17]

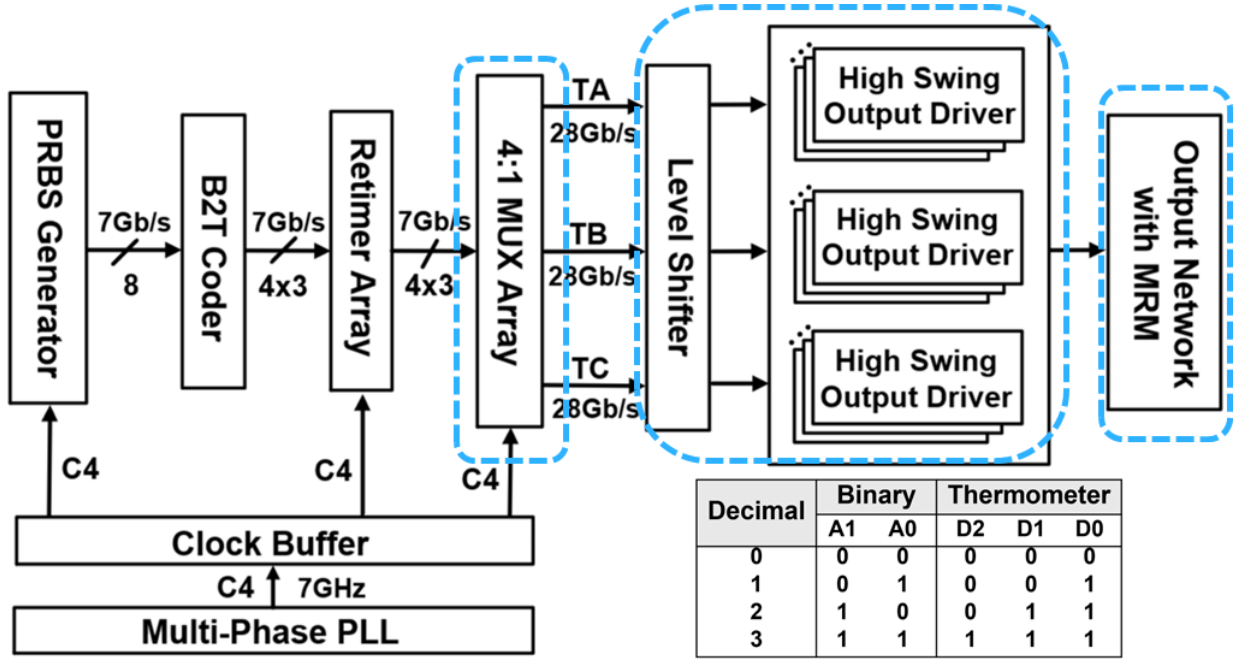
- High voltage swing for large extinction ratio (ER)
- High-swing voltage mode driver needed

- Bias-dependent E-O BW
- Equalization needed

- Nonlinear E-to-O conversion
- Independent level adjustment

Transmitter Architecture

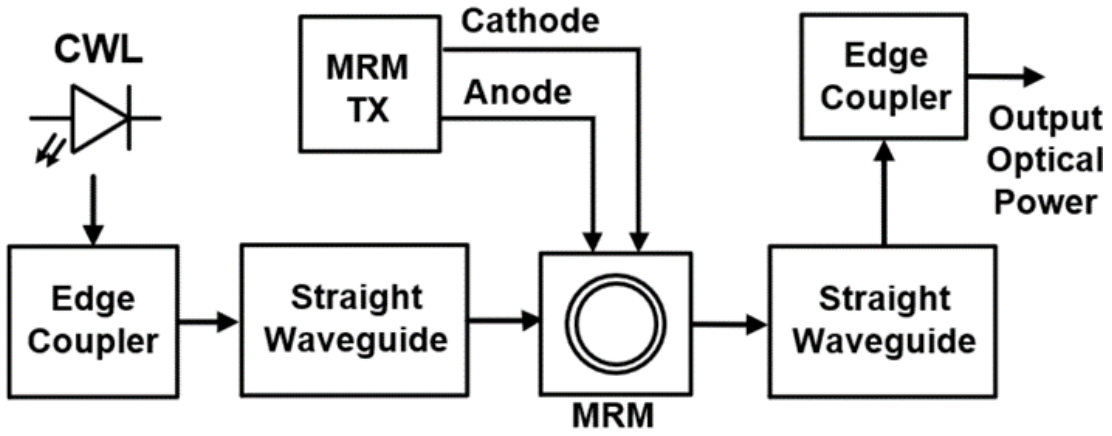


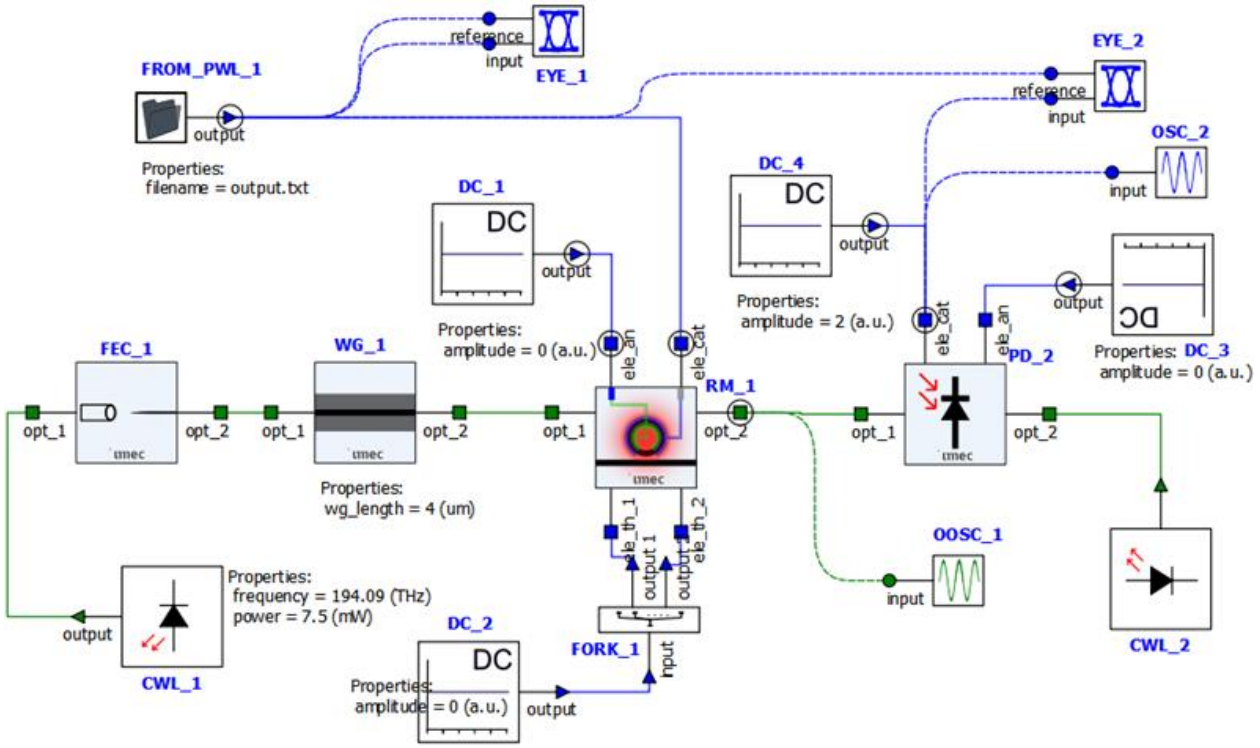


Decimal	Binary		Thermometer		
	A1	A0	D2	D1	D0
0	0	0	0	0	0
1	0	1	0	0	1
2	1	0	0	1	1
3	1	1	1	1	1

- For PAM-4 implementations, nonlinear E-to-O conversion results in unequal eye-heights
- Quarter-rate structure to balance the power and complexity
- Thermometer-coded topology is used for independent single-eye-height adjustment

Optical Simulation Setup

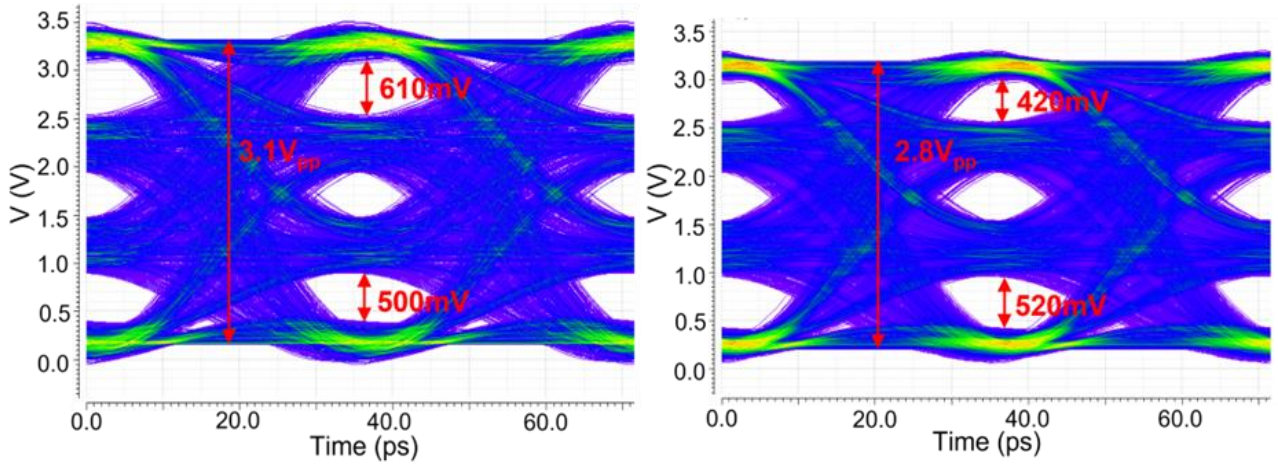




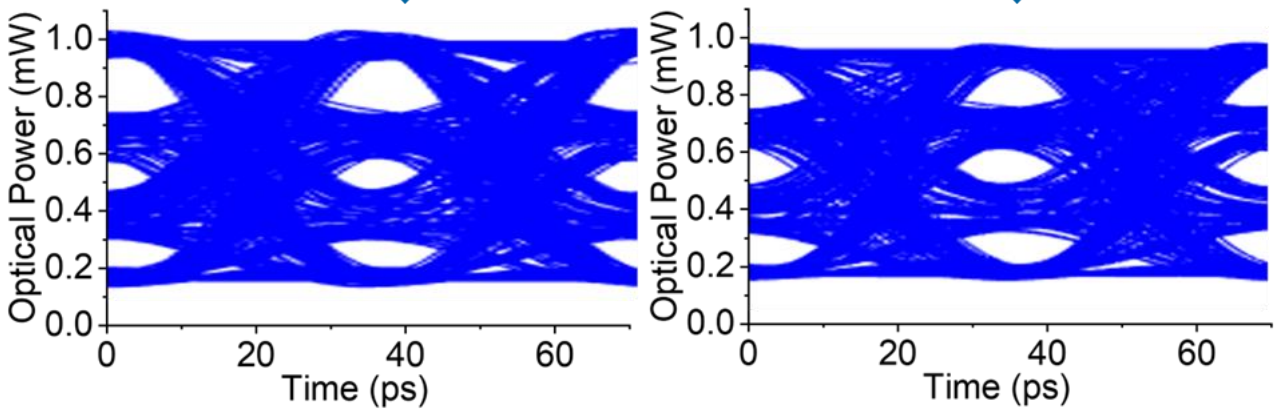
- Custom-designed Verilog-A model is replaced by the model provided by the foundry
- Commercial software Ansys Lumerical INTERCONNECT is used for simulation
- CW lasers, edge couplers, and straight waveguides are included in the simulation

Simulation Results

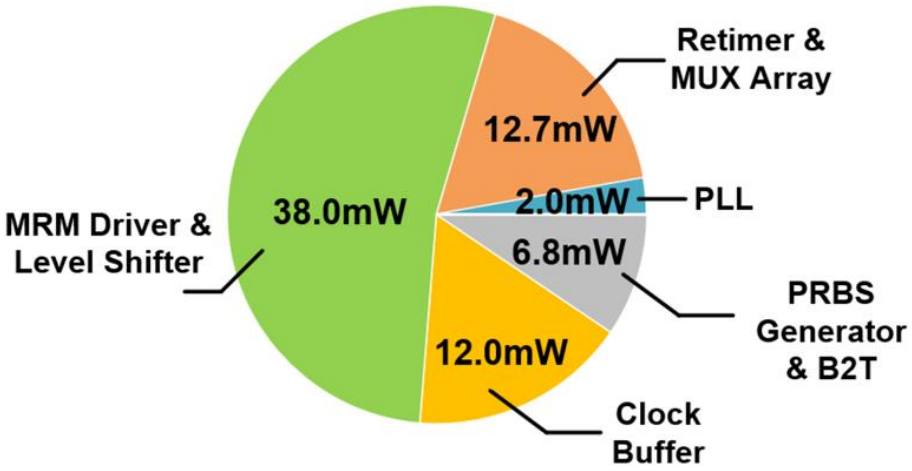
Before swing adjustment After swing adjustment



Simulated electrical PAM-4 eye diagram at 56 Gb/s



Simulated optical PAM-4 eye diagram at 56 Gb/s



- The electrical output can result in unequal optical eyes due to nonlinearities of MRM
- Single-eye-height adjustment combined with accurate optical simulation is necessary
- Power consumption: 71.5mW

Performance Summary

	PTL'18	JSSC'15	MWSCAS'19	JSSC'20	This Work
Data Rate (Gb/s)	56	25	25	10	56
Modulation Scheme	NRZ	NRZ	PAM-4	BPSK	PAM-4
Output Swing (V)	1	4.4	2.4	1.55	3.1
Electronic IC Process	28nm FDSOI CMOS	65nm CMOS	65nm CMOS	45nm SOI CMOS	40nm CMOS
Optical Simulation	N/A	Verilog-A	imec ISIPP50G	N/A	imec ISIPP50G
Energy Efficiency (pJ/bit)	0.71	4.54	1.6	2.3	1.28
FOM[a] (pJ/(bit·V))	0.71	1.03	0.67	1.48	0.41

Conclusions

A 56-Gb/s PAM-4 optical transmitter using a silicon photonic MRM

- Thermometer-coded topology used for independent single-eye-height adjustment
- Pulsed tri-state inverter-based 4:1 MUX releases the bandwidth constraint
- High-swing voltage-mode driver with swing adjustability achieves large ER
- E-O co-simulations are performed using device models from the foundry to optimize the TX design

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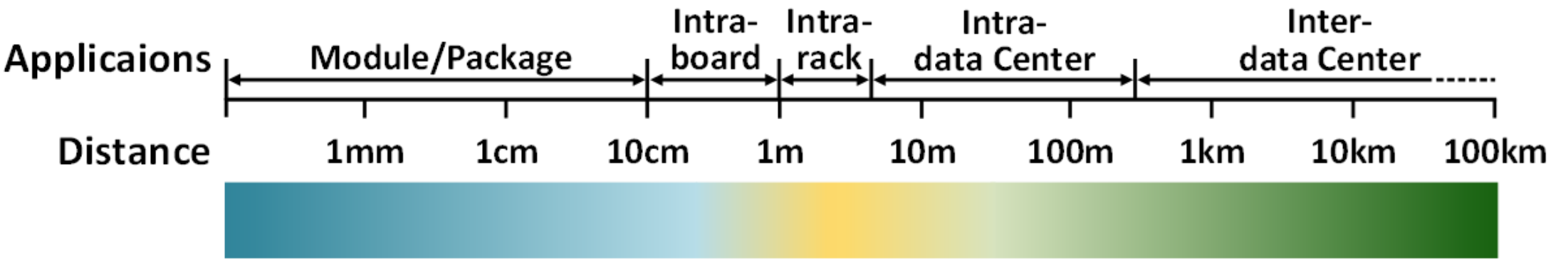
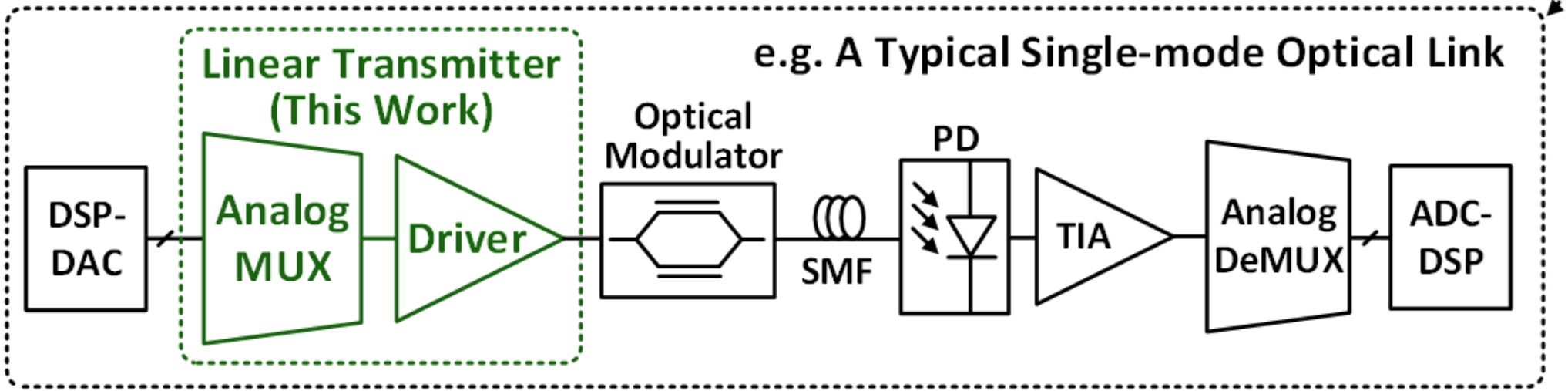
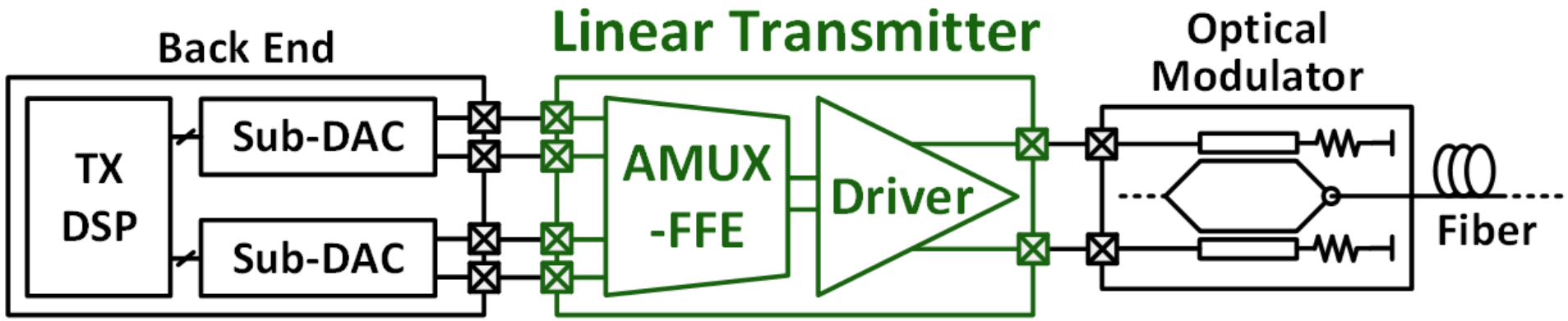
A 56-Gbaud 7.3-V_{ppd} Linear Transmitter for MZM in 130-nm SiGe BiCMOS

Motivation


Applicaions
Module/Package
Intra-board
Intra-rack
Intra-data Center
Inter-data Center
Distance
1mm
1cm
10cm
1m
10m
100m
1km
10km
100km
Medium
Electrical
Data Rate (DR) & Distance Limited by Channel Loss
Multi-mode Optics
DR & Distance Limited by MMF Dispersion
Single-mode Optics
Low fiber dispersion and thus longer distance

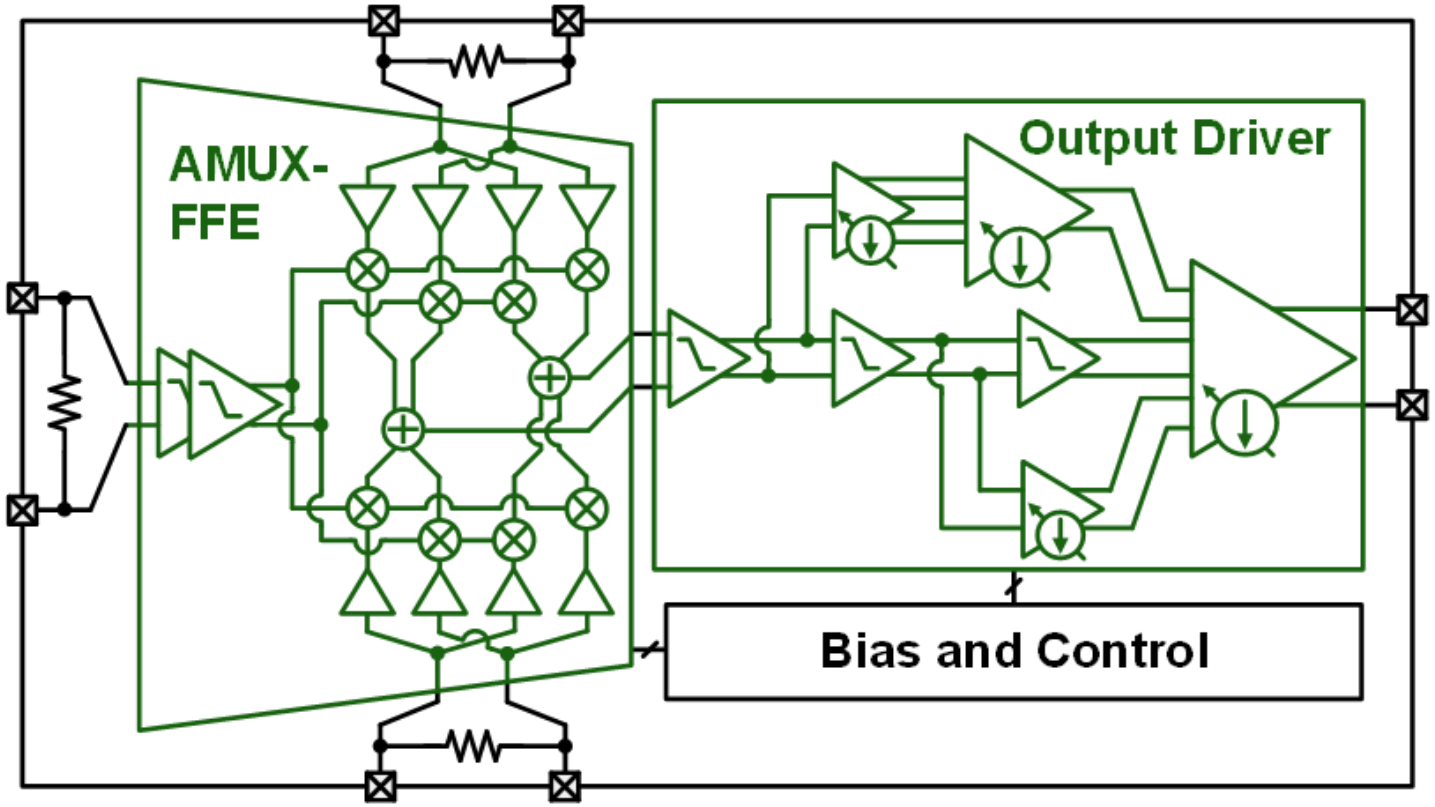

e.g. A Typical Single-mode Optical Link
Linear Transmitter (This Work)
DSP-DAC
Analog MUX
Driver
Optical Modulator
SMF
PD
TIA
Analog DeMUX
ADC-DSP

Design Challenges for Linear TX



- **Large output swing** for high optical extinction ratio
- **High linearity** to support advanced modulation schemes for high data rate
- **Equalization** to compensate for high-frequency loss from E/E and E/O interfaces
- **Analog serialization** to relieve BW requirements for DACs

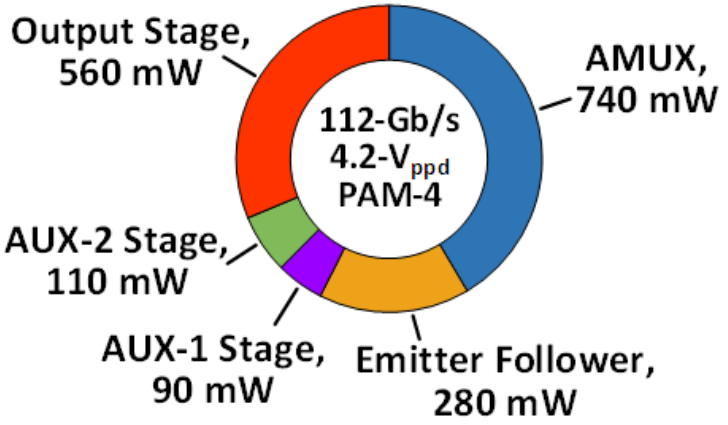
Transmitter Architecture

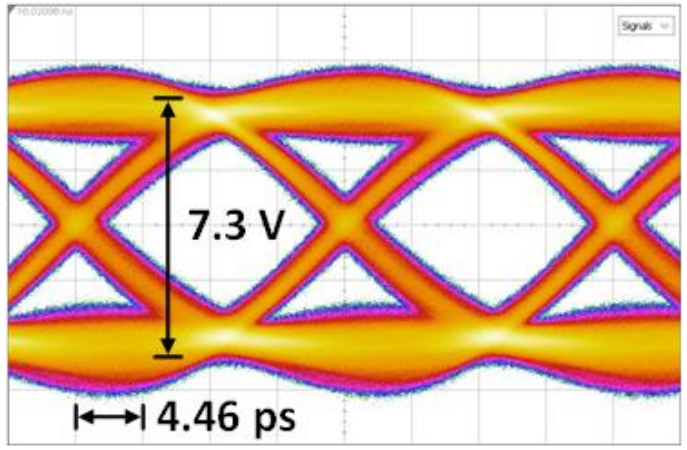


- **AMUX-FFE**
  - Serializes data streams from half rate to full rate
  - Generates equalized signal with a tap generator-less re-config. FFE
- **Output Driver**
  - Linearly amplifies signal swing using a dynamic triple-stacked topology

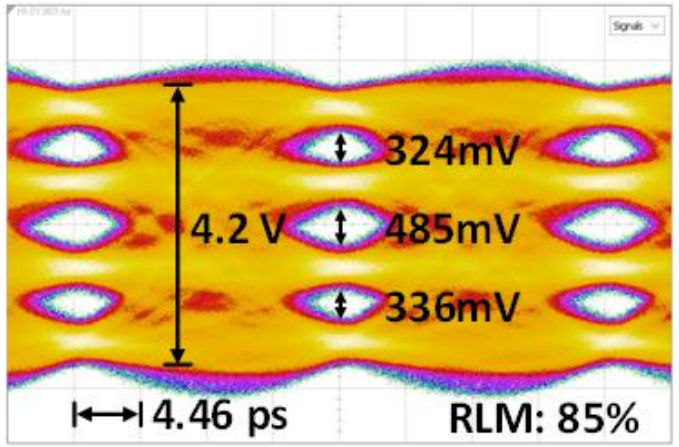
Measurement Results

- The whole transmitter supports a maximum output swing of **7.3-Vppd @ 56-Gbaud NRZ**
- With FFE, **56-Gbaud 4.2-Vppd PAM-4** is also achieved, with 1.78-W power consumption

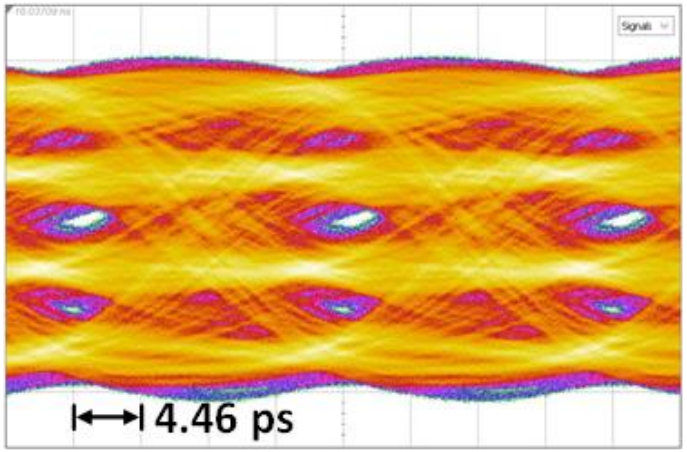




56 Gbaud with FFE Off



56 Gbaud with FFE On



56 Gbaud with FFE Off

Performance Summary

		TMTT'17 P. Rito *et al.*	JSSC'20 A. H. Ahmed *et al.*	BCICTS'21 A. Fatemi *et al.*	BCICTS'22 F. Iseini *et al.*	This Work
Technology		130-nm SiGe BiCMOS	130-nm SiGe BiCMOS	130-nm SiGe BiCMOS	130-nm SiGe BiCMOS	130-nm SiGe BiCMOS
f_T / f_{MAX} [GHz]		300/500	250/NA	300/500	380/520	250/340
Output Impedance Matching [Ω]		100	100	100	100	100
Equalization		NA	NA	1-tap FFE	NA	Reconfig. FFE
Serialization		NA	NA	NA	NA	2:1 Analog
Maximum Ouput Swing [V_{ppd}]		4 @90-Gb/s PAM-4	6 @64-Gb/s NRZ	4 @64-Gb/s Duobinary	2 (estimated by P1dB)	7.3 @56-Gb/s NRZ
Maximum Data Rate [Gb/s]		120 @3-V_{ppd} NRZ	138 @2.4-V_{ppd} PAM-4	64 @4-V_{ppd} Duobinary	128 @1.2-V_{ppd} PAM-4	112 @4.2-V_{ppd} PAM-4
Data Rate-Output Swing Product [V·Gb/s]		360	384	256	256	470
Driver THD		3.8% @1GHz, 3V_{ppd}	3.6% @1GHz, 6V_{ppd}	5.5% @1GHz, 4V_{ppd}	6% @5GHz, 2V_{ppd}	1.6% @1GHz, 6V_{ppd}
Driver Gain [dB]		12.5	30 (with VGA)	24	18	17
Power Consumption [mW]	Driver	550	1000	1030	280	1040
	AMUX	NA	NA	NA	NA	740
FoM# [bit/s/Hz]		0.00818	0.00397	0.00414	0.00217	0.00867*

$$^{\#}\text{FoM} = \frac{\text{Maximum Data Rate}}{f_T} \cdot \frac{(\text{Output Swing @ Maximum Data Rate})^2}{8 \cdot \text{Output Impedance Matching} \cdot \text{Power Consumption}}$$

Conclusion

A linear transmitter in 130-nm SiGe BiCMOS for optical modulators

- Tap generator-less re-configurable AMUX-FFE
- Dynamic triple-stacked driver topology
- Demonstrates 7.3-Vppd maximum output swing @56-Gbaud NRZ
- Supports 56-Gbaud 4.2-Vppd PAM-4
- Achieves the best FoM among linear TX/drivers in the same node

香港科技大學
THE HONG KONG UNIVERSITY OF SCIENCE AND TECHNOLOGY

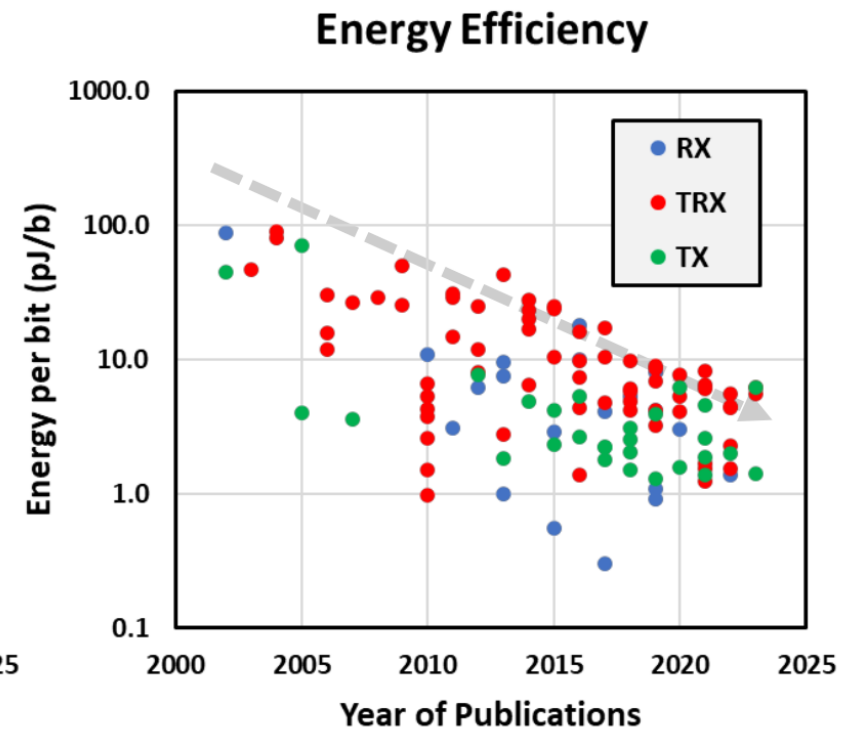
HKUST OWL

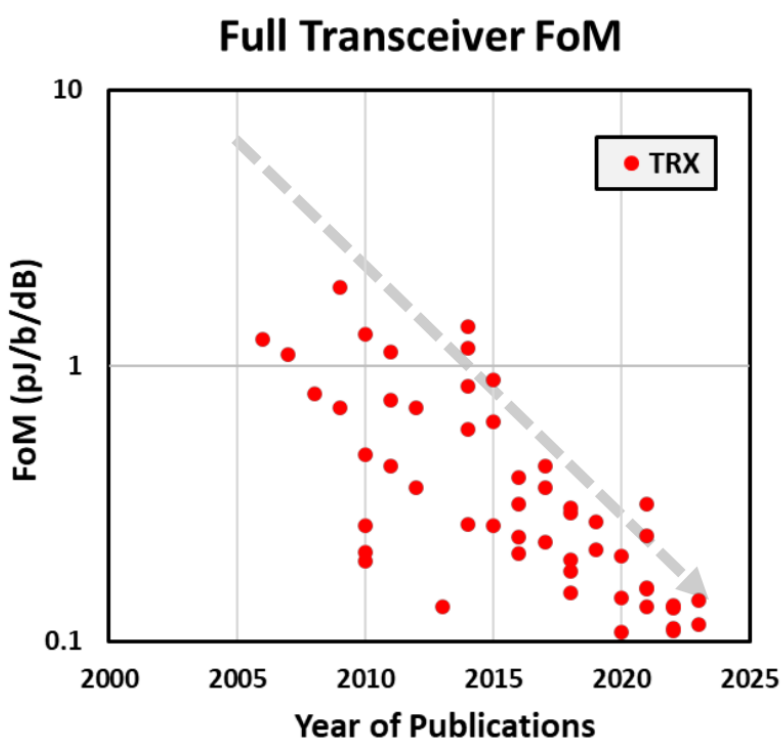
Beyond 200Gb/s Wireline Transceiver

Source: ISSCC Forum 2024-Forum 6.3, Intel

CMOS Electrical Links in the Past 21 Years

- Both speed and efficiency have scaled by >21x in the past 21 years!



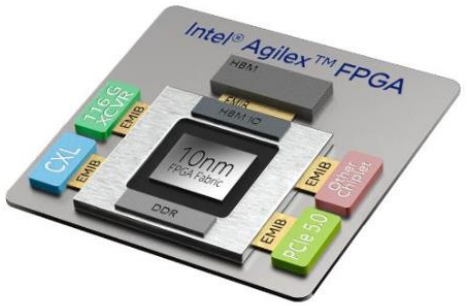


From ISSCC/VLSI (2002-2022) [1-40]

100+Gb/s SerDes PHY Examples

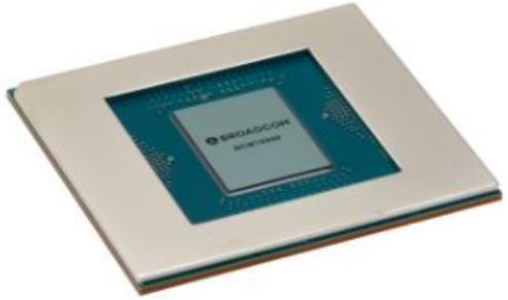
FPGAs, NW-SW SOCs, ASICs, IPs, …

intel



- Agilex-I™ FPGA
- 116Gb/s PAM-4 LR
- 4.2 Tb/s Max BW

BROADCOM



- Tomahawk™ 5
- 51.2 Tb/s
- 64x800GbE
- 8x106Gb/s PAM4 LR

AMD XILINX Rambus SYNOPSYS .....

MEDIATEK

- 28.8 Tb/s SW 800GbE
- 288x112G SerDes in 7nm

HUAWEI

- 25.6 Tb/s SW
- 128x100G SerDes

MARVELL

- Alaska™
- Dual 400GbE w/ 100G PAM4 SerDes in 5nm

etopus we accelerate

- EPHY™
- 112G LR SerDes in 7nm

Alphawave IP

- AlphaCORE™
- 112G LR SerDes IP

cadence

112G-ELR PAM4 SerDes PHY in 5nm

Modulation for Wireline TRX

- Modulation → PAM-4
  - Best SNR SNR and power performing at tested channel
  - Backward compatibility
  - Electrical to optical compatibility
  - Testing methodology and equipment maturity/availability

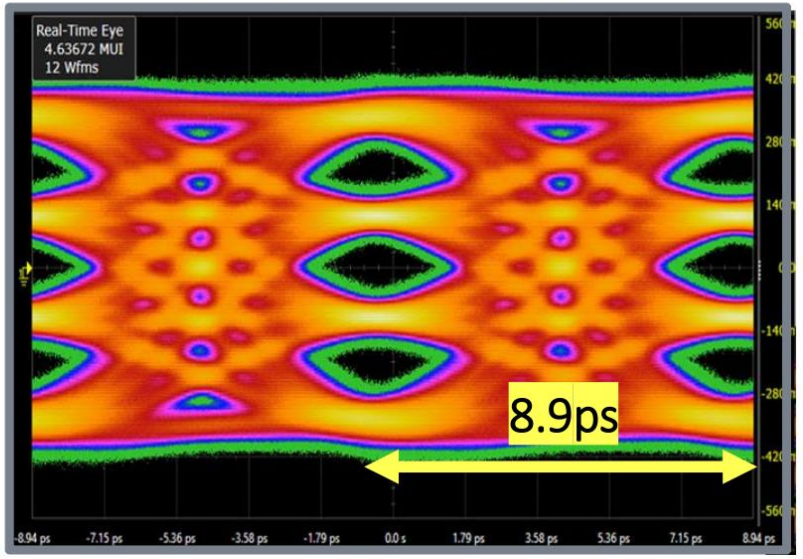
Data Ratem Gb/s	224	224	224	224	224	224
PAMn Levels	4	5	6	7	8	16
Bit per symbol	2.00	2.32	2.58	2.81	3.00	4.00
Symboe Rate (GS/s)	112.00	96.47	86.66	79.79	74.67	56.00
UI (ps)	8.93	10.37	11.54	12.53	13.39	17.86
Nyquist Freq	56.00	48.24	43.33	39.90	37.33	28.00
SNR Delta	0.00	-2.50	-4.44	-6.02	-7.36	-13.98

Source: "PAMn vs Channel and FEC investigation for 224 Gb/s", IEEE P802.3df Ethernet Task Force

Key Challenges of 224-Gb/s PAM-4 Wireline TRX

- Ultra high circuit BW > 56Ghz
- UI=8.9ps -> extra-low random jitter < 100fs
- Developing Analog to Digital converter sampling in 112GS/s (like high end scope)
- Developing Digital to Analog Converter working in 112GS/s with low noise (like high end signal generator)
- Package, channels IL and reflections

224Gb/s PAM-4



J. Kim et al., ISSCC 2021

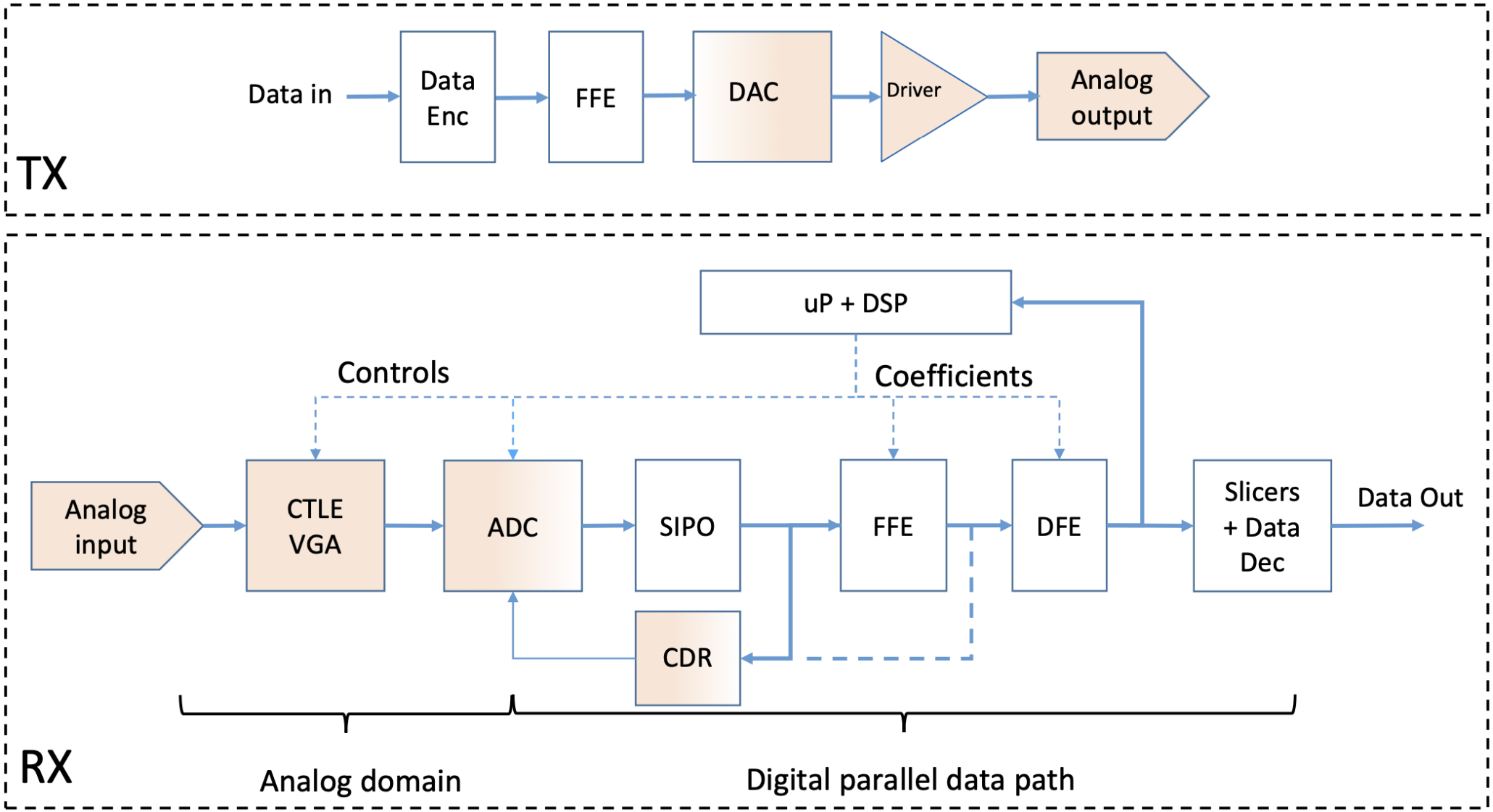
Why DAC-ADC TRX for 224Gb/s

At 224Gb/s data-rate, we need to deal with

- **Tough channels with higher 56GHz Nyquist**
  - Higher insertion loss (package, board, connector, etc.)
  - Critical reflections at many UIs later than the cursor (large package and short UI)
  - Sharp roll-offs or some notches
  - Non-ideal smoothness (ripples in insertion loss)
- **Implementation**
  - Analog DFE loop timing in RX can not be done with a UI=8.9ps

Need more powerful and flexible channel equalization for good BER
→ Need many-tap TX/RX FFE, continuous time EQ, DFE, sometimes advanced equalization (sliding-block DFE, MLSD, etc)

112/224 Gb/s DAC-ADC TRX Architecture



E.g., A 224-Gb/s DAC-TX Architecture

9-Tap FFE
NRZ
PAM-4
PAM-6

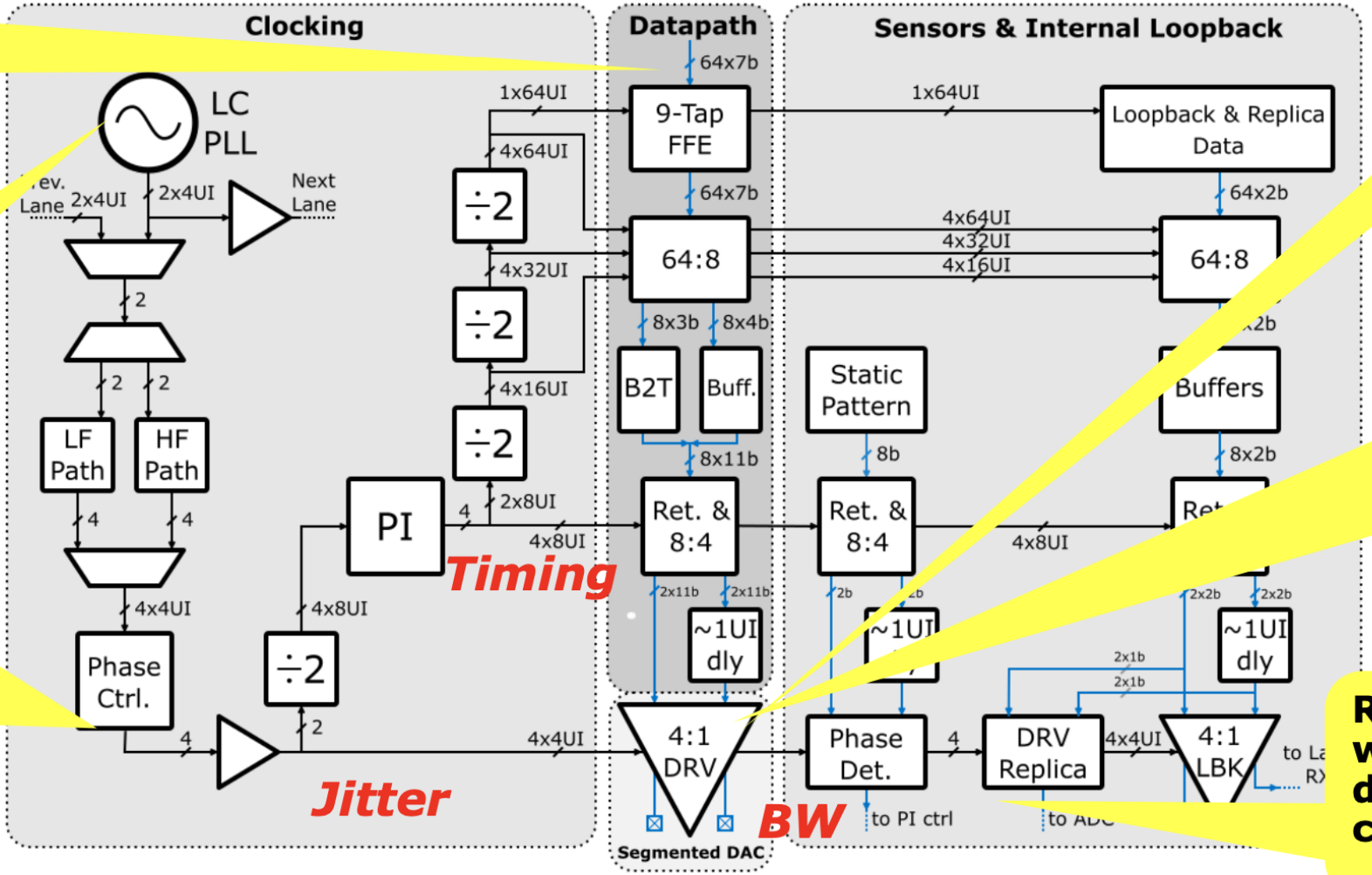
LC D-PLL
<-99dBc/Hz
@1MHz

CMOS w/without inductors
<RJ 62fs
<DJ 110fs

7b-segmented DAC

4:1 serializer directly at the output
>36dB SNDR
>0.97 RLM
>1Vpp swing

Replica based DRV with phase detector for phase calibration



Beyond 200Gbps Electrical transceivers – Circuit

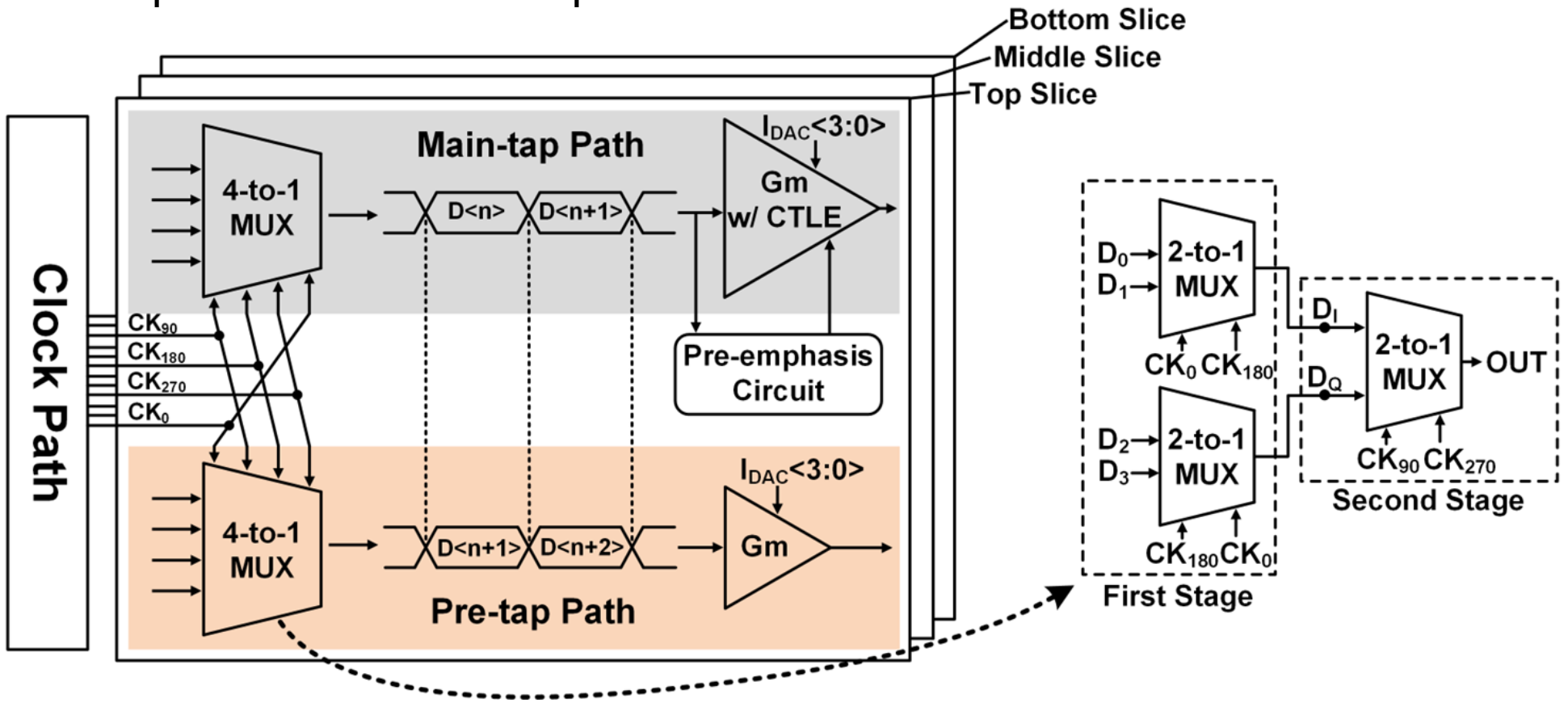
Section Outline

- Architecture
  - VCSEL Transmitter
  - MRM Transmitter
  - MZM Transmitter
  - Wireline Transmitter
- **Key Circuits**
  - **Multiplexer**

    (Now Opensource: https://github.com/HKUST-ECE-IC-Design-Center-OWL/SHARE-by-OWL-HKUST-4to1-MUX-for-28Gbaud-Optical-TX)
  - **Output Driver**
  - **Pre-emphasis**
- Practical Issues
  - EMI Suppression Due to CM Noise to Reduce Radiation Emissions

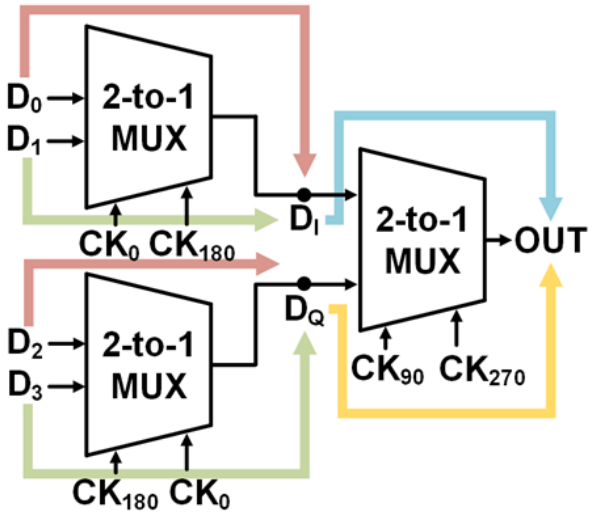
4-to-1 Multiplexer

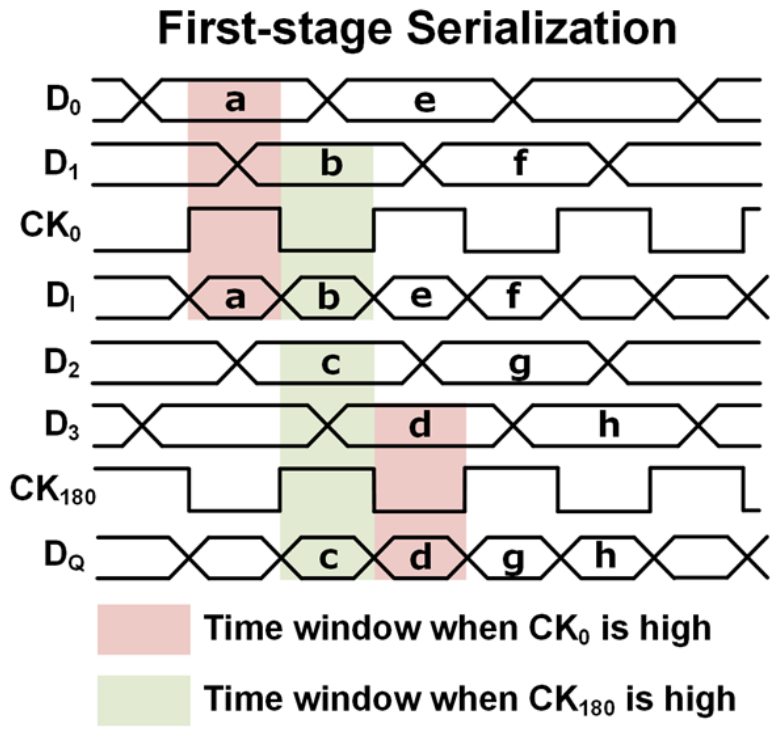
- **Functions**
  - 4 quarter-rate data streams → 1 full-rate data stream
  - Controls tap interval of the 2-tap FFE

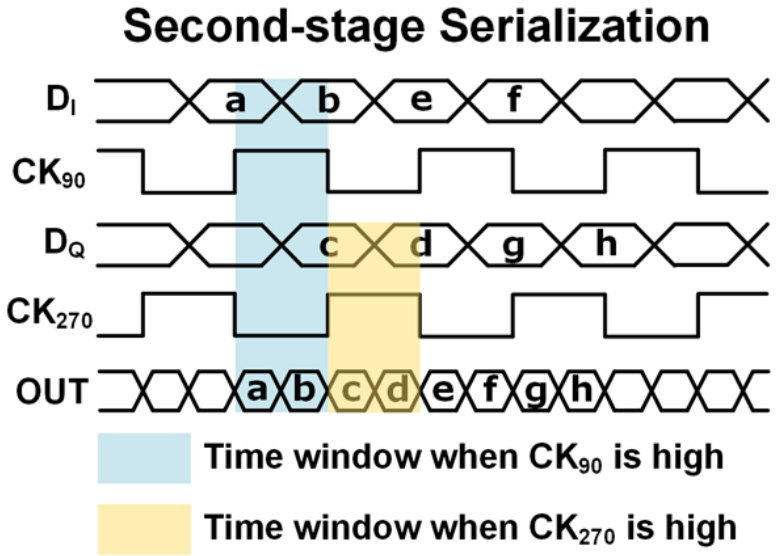


4-to-1 Multiplexer

- **Principle**
  - Implemented by cascading two-stages of 2-to-1 MUXs
  - 1st-stage 2-to-1 MUX serializes D_0~D_3 to D_I and D_Q
  - 2nd-stage 2-to-1 MUX further serializes D_I and D_Q to OUT

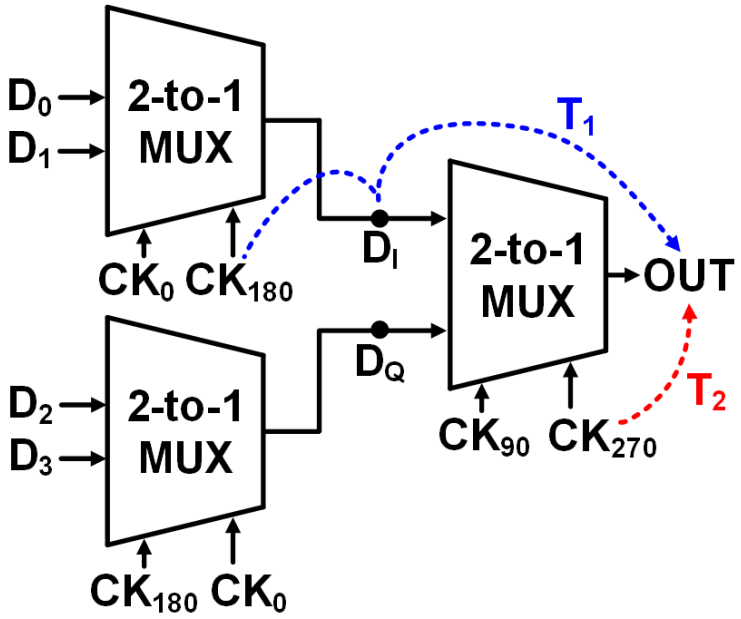


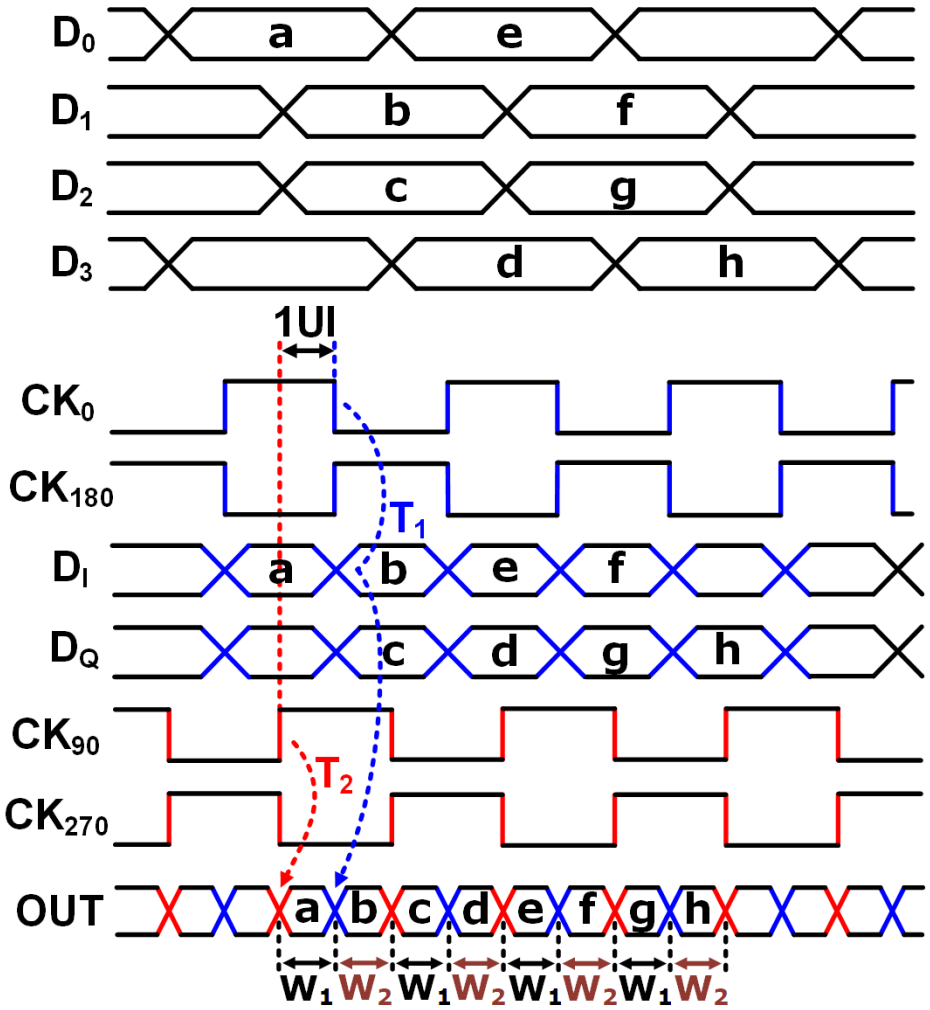




4-to-1 Multiplexer

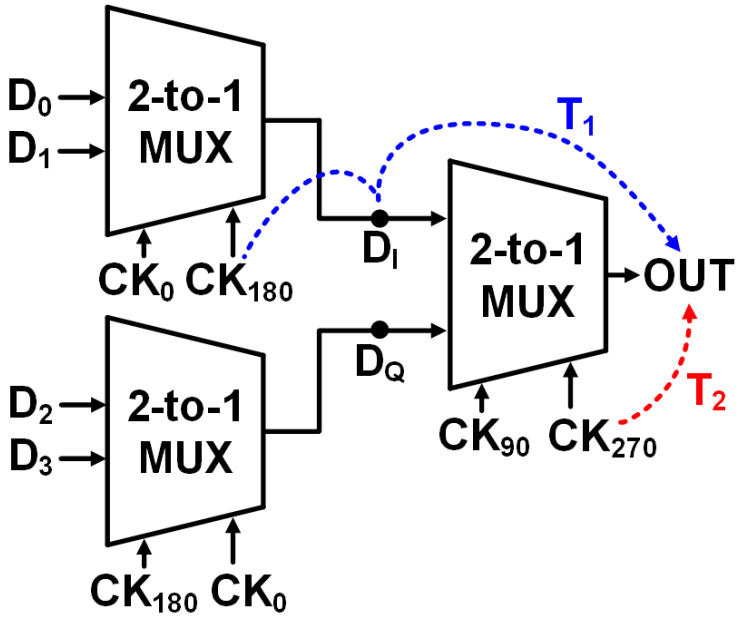
- **Output distortion issue**
  - T1: delay from CK_0 (CK_{180}) to OUT
  - T2: delay from CK_{90} (CK_{270}) to OUT
  - T1 ≠ T2 → duty cycle distortion of the output

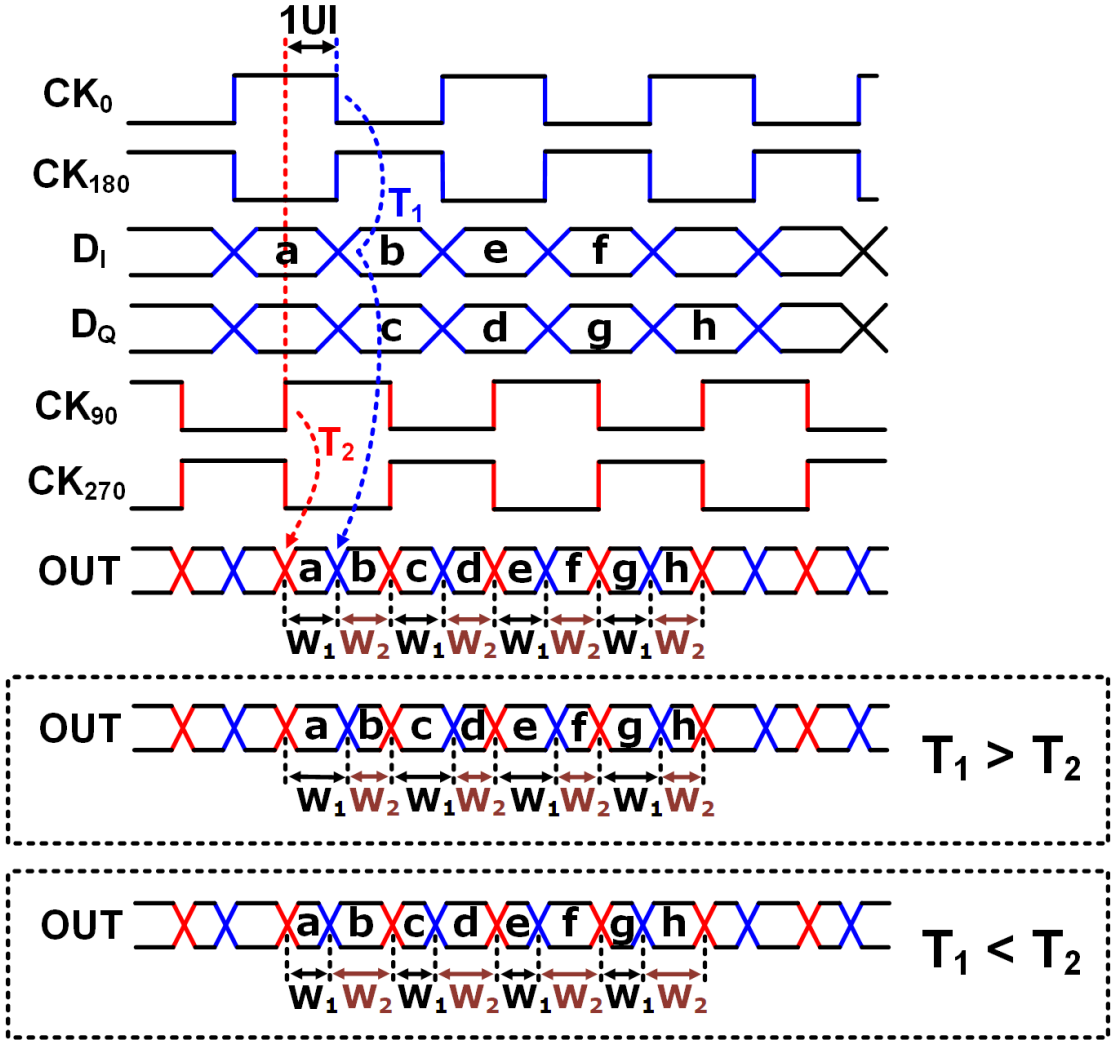




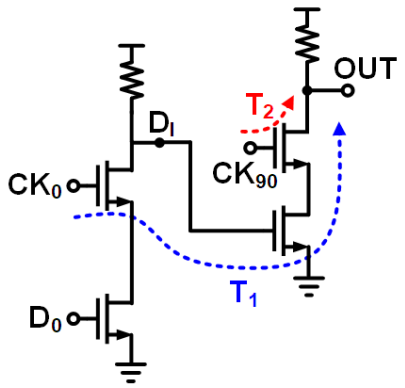
4-to-1 Multiplexer

- **Output distortion issue**
  - T1: delay from CK_0 (CK_{180}) to OUT
  - T2: delay from CK_{90} (CK_{270}) to OUT
  - T1 ≠ T2 → duty cycle distortion of the output

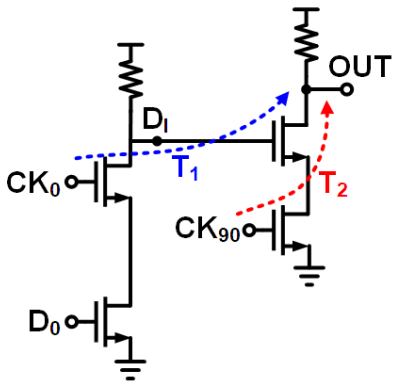




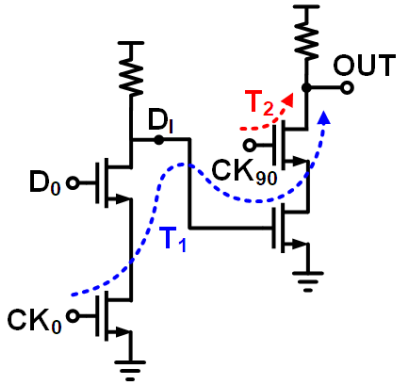
4-to-1 Multiplexer



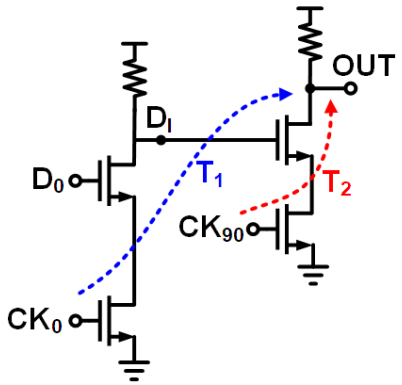
☹ Clock Up-Clock Up
($T_1 > T_2$)



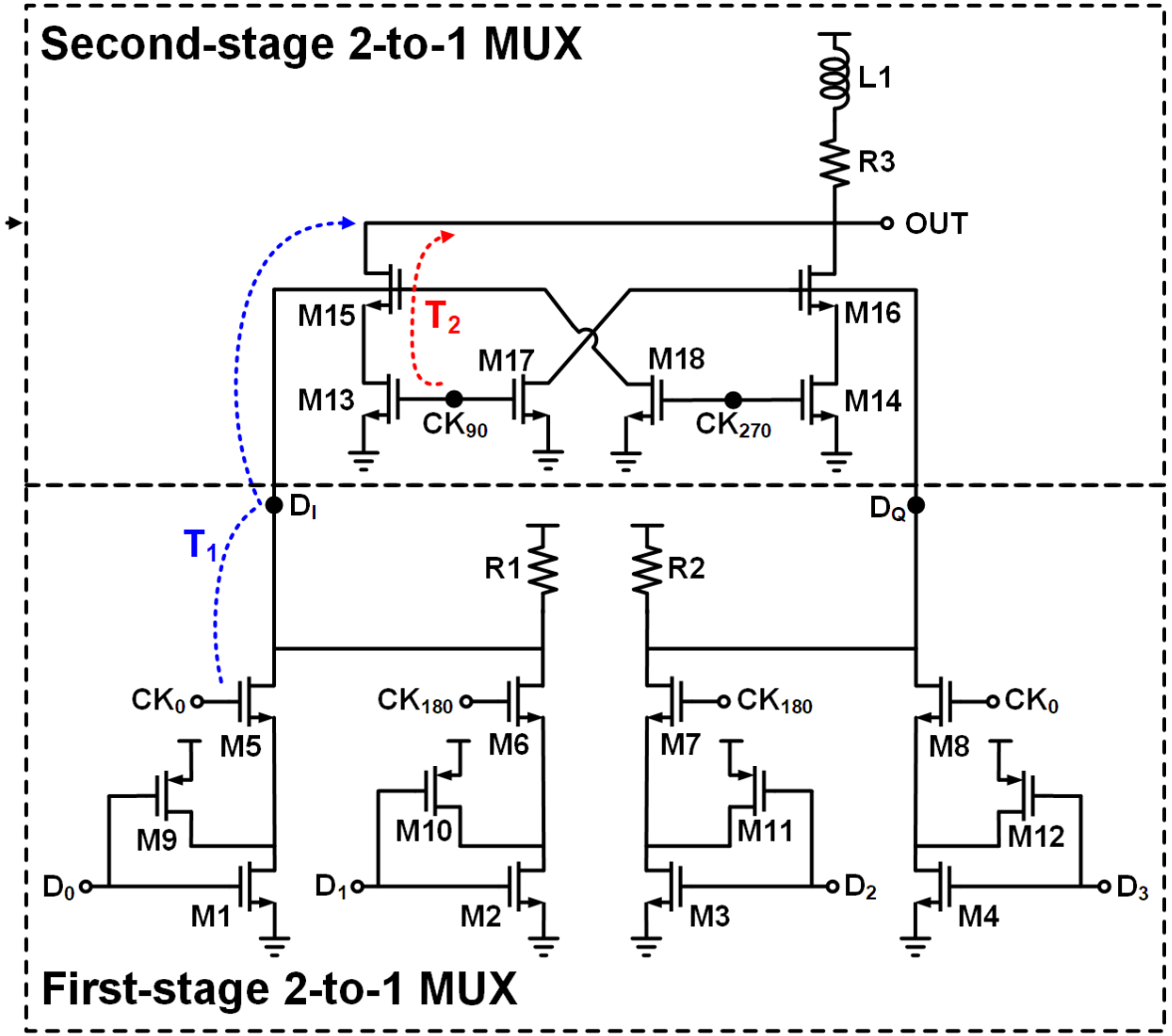
☺ Clock Up-Clock Down
($T_1 \approx T_2$)



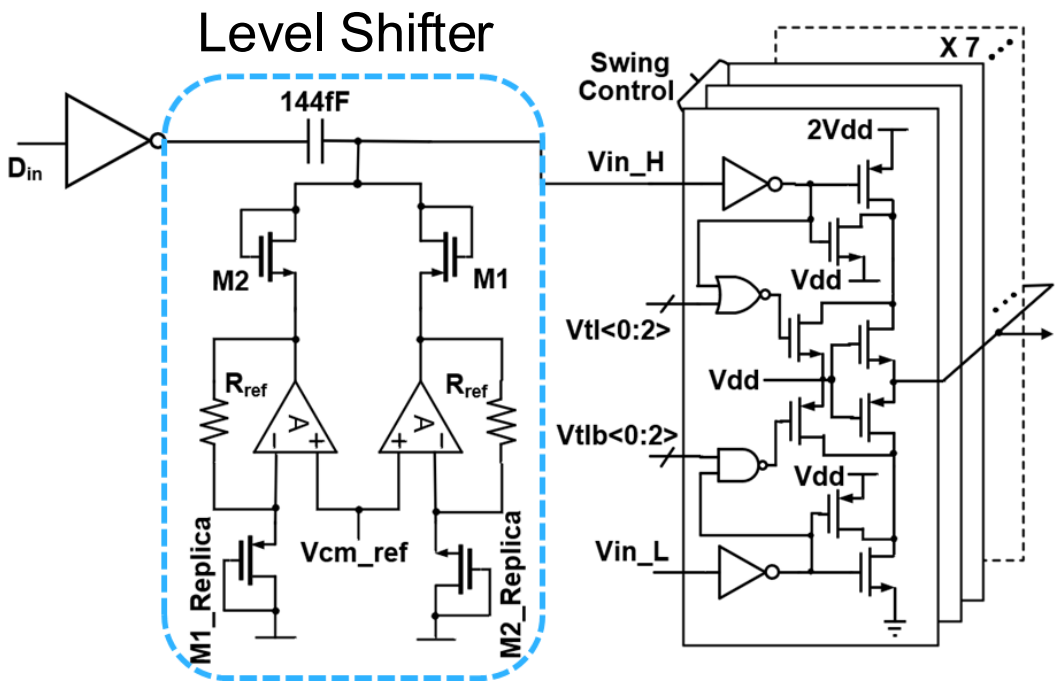
☹ Clock Down-Clock Up
($T_1 >> T_2$)

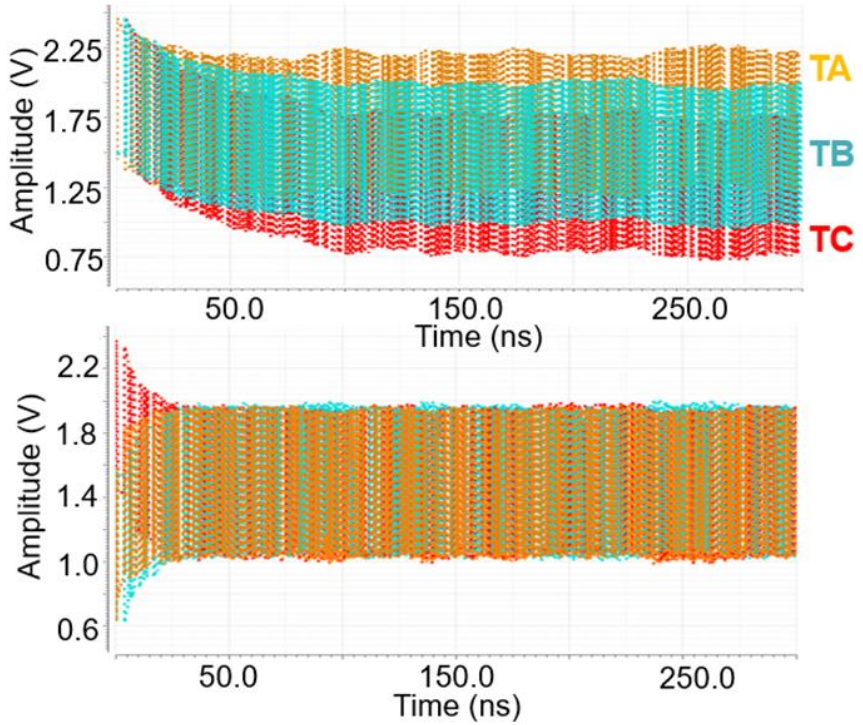


☹ Clock Down-Clock Down
($T_1 > T_2$)



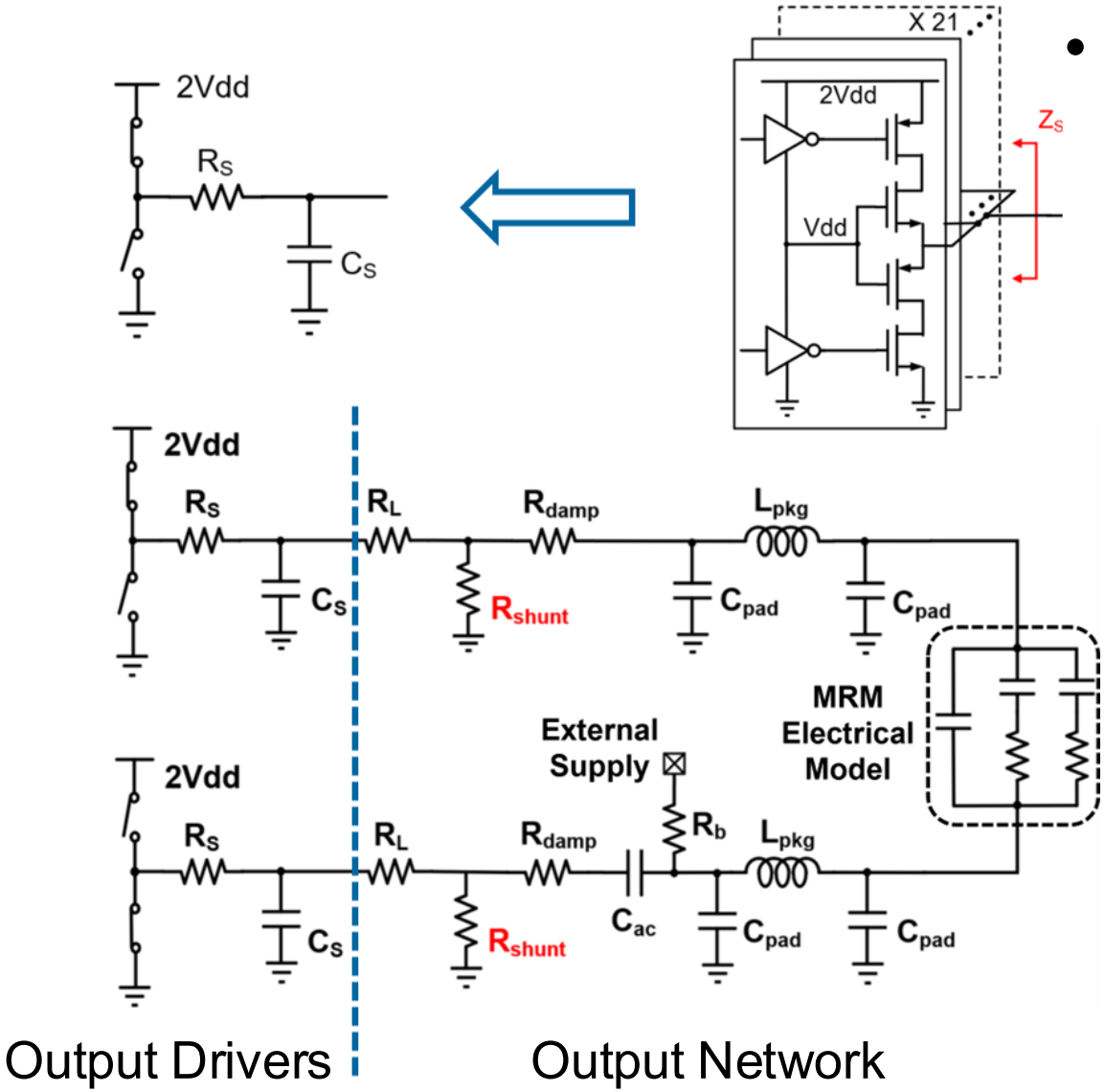
Output Driver for MRM and MZM



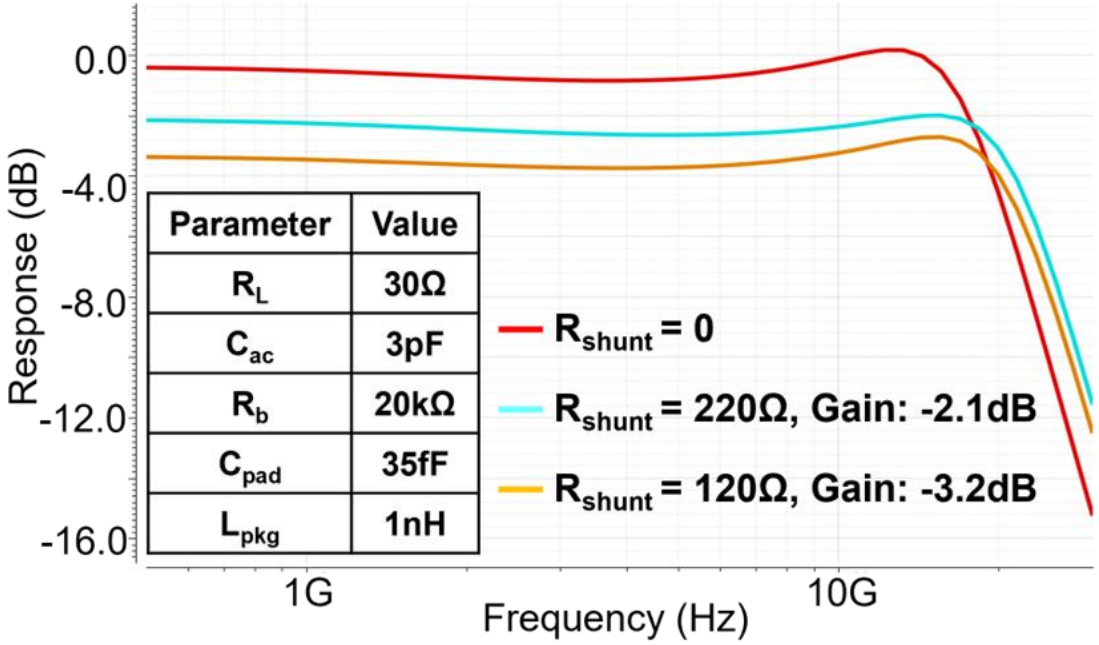


- Multiple transistors are stacked with the middle devices biased at Vdd to achieve 2xVdd output swing
- 3-bit swing adjustability is achieved by combination of binary-weighted driver slices
- Resistors of ac-coupled level shifter are replaced by diode-connected transistors and their replicas
- By tuning Vcm_ref, the average output voltage can be adjusted and set equally

Output Driver for MRM and MZM



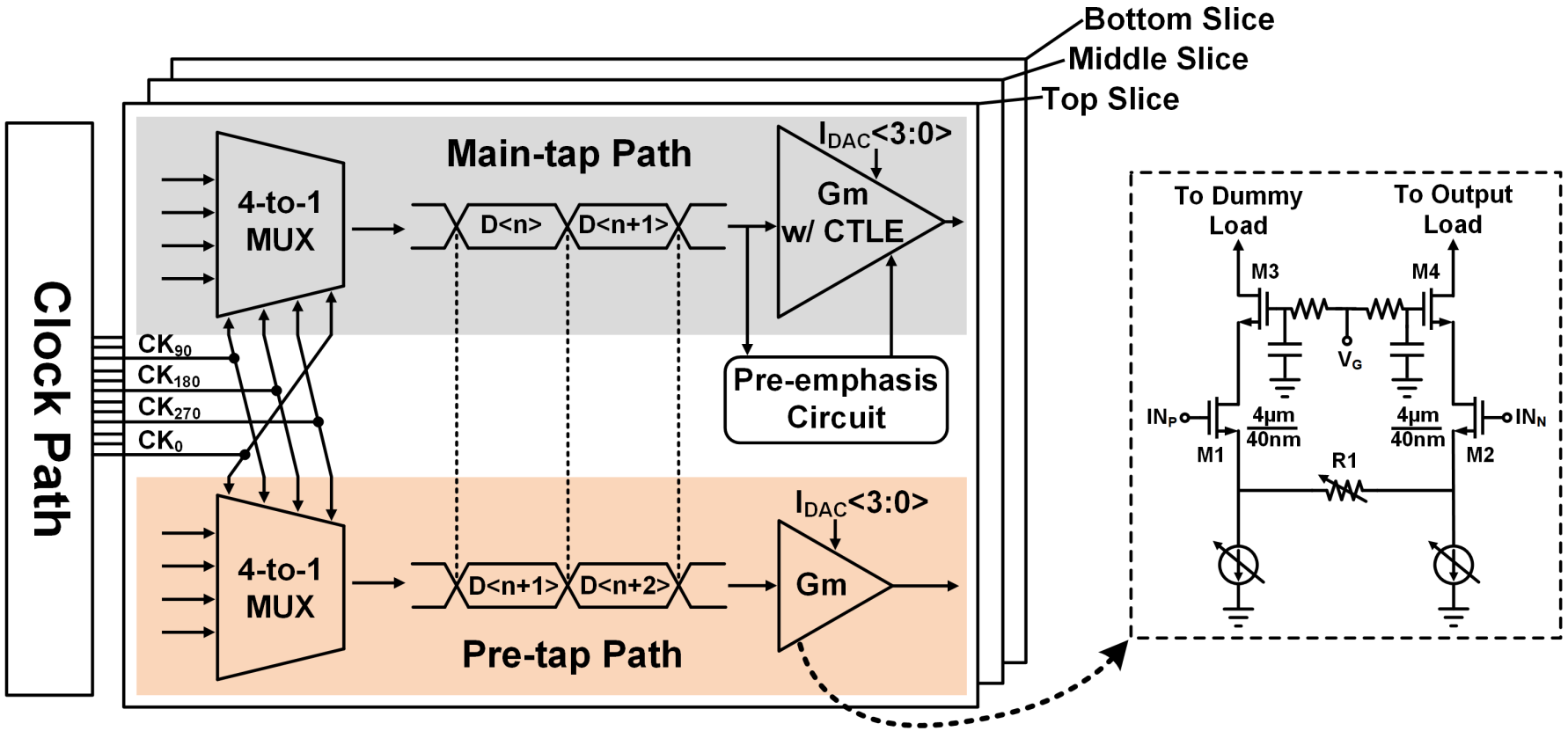
- **Output network**
  - MRM driver represented by a first-order RC and optimized with the output network
  - With a 220Ω-Rshunt, BW is extended from 18.6 to 22.4 GHz with a 3.2-dB dc gain reduction



Parameter	Value
R_L	30Ω
C_{ac}	3pF
R_b	20kΩ
C_{pad}	35fF
L_{pkg}	1nH

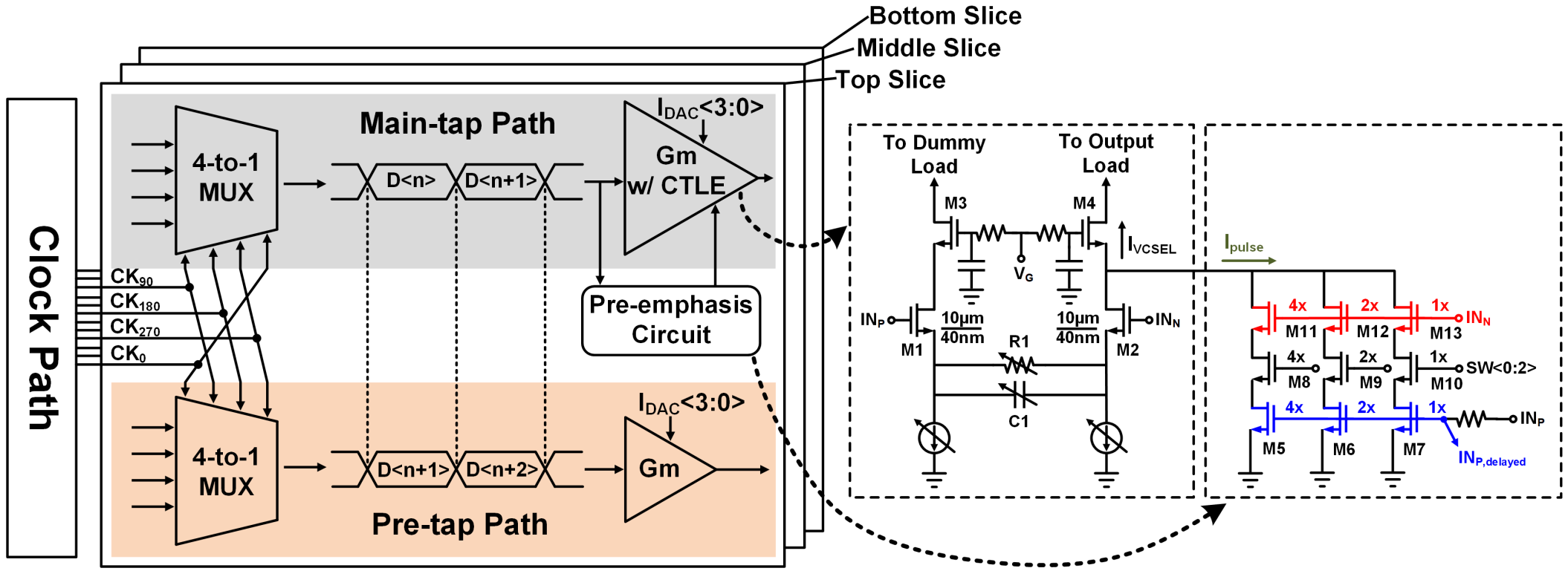
Output Driver for VCSEL Embedded in a 2-Tap FFE

- **Pre-tap gm cell**
  - Cascode structure for preventing breakdown issue
  - Tunable tail current source and degenerated variable resistor for gain adjustment



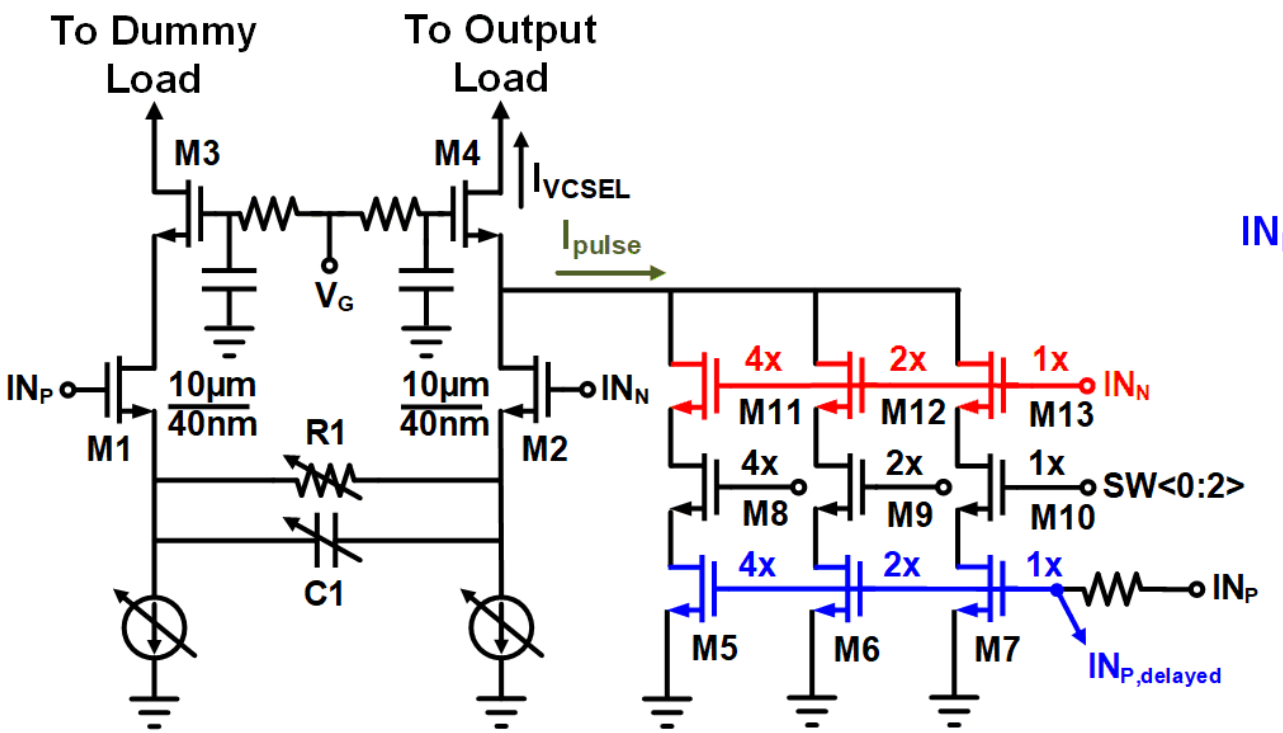
Output Driver for VCSEL Embedded in a 2-Tap FFE

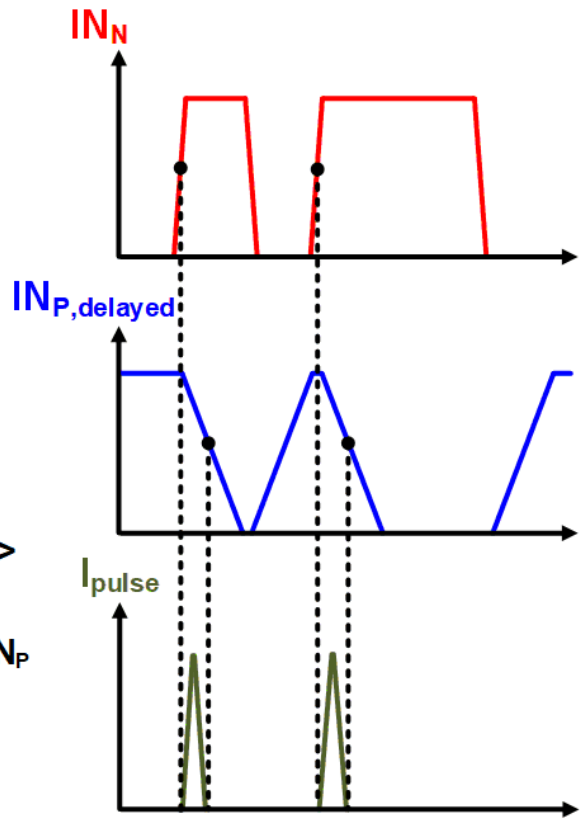
- **Main-tap gm cell**
  - Transistors size 2.5 times larger than pre-tap gm cell
  - Source-degenerated capacitor for BW extension
  - Pre-emphasis circuit for optical eye skew mitigation



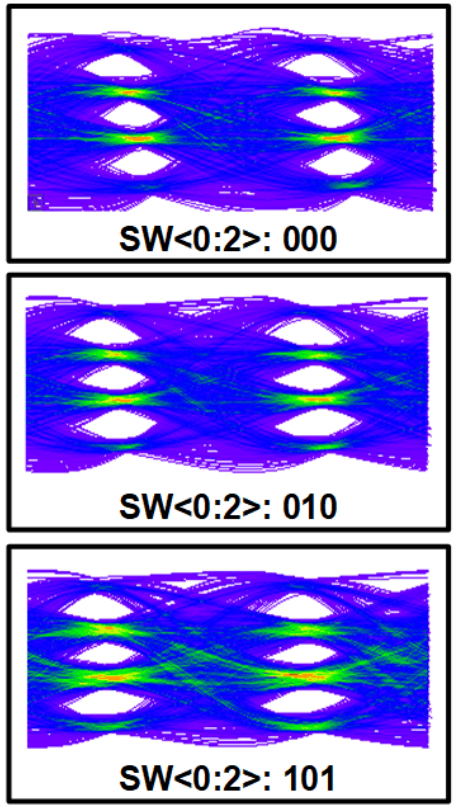
Pre-emphasis Circuit

- **Principle**
  - $IN_N \uparrow \rightarrow I_{VCSEL} \downarrow \rightarrow IN_N$ & $IN_{P,delayed}$ both high → A sharp current pulse I_{pulse} generated





Simulated Optical Eye Diagrams



Section Outline

- Architecture
  - VCSEL Transmitter
  - MRM Transmitter
  - MZM Transmitter
  - Wireline Transmitter
- Key Circuits
  - Multiplexer
  - Output Driver
  - Pre-emphasis
- **Practical Issues**
  - **EMI Suppression Due to CM Noise to Reduce Radiation Emissions**

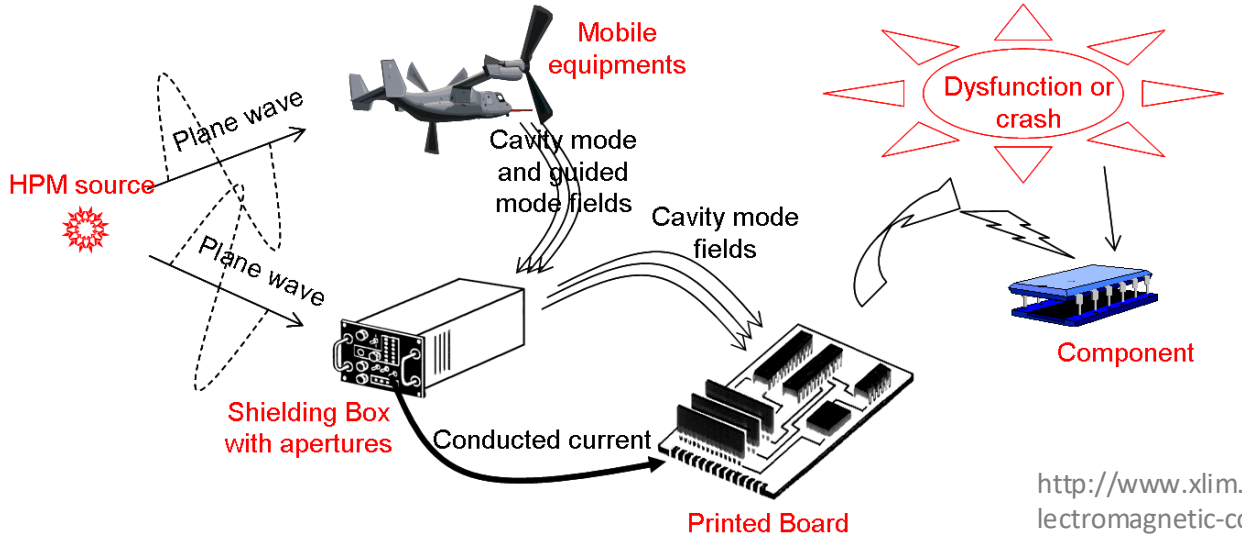
香港科技大學
THE HONG KONG UNIVERSITY OF SCIENCE AND TECHNOLOGY

HKUST OWL

Analysis on EMI Related Common-Mode Noise of Serdes Transmitter

What is EMI?

- Most electronics generate electromagnetic emission



http://www.xlim.fr/en/osa/electromagnetic-compatibility

- Electromagnetic interference (EMI) causes malfunction of the victim electronics
- How to solve?
  - Keep enough distance, be robust, and keep quiet

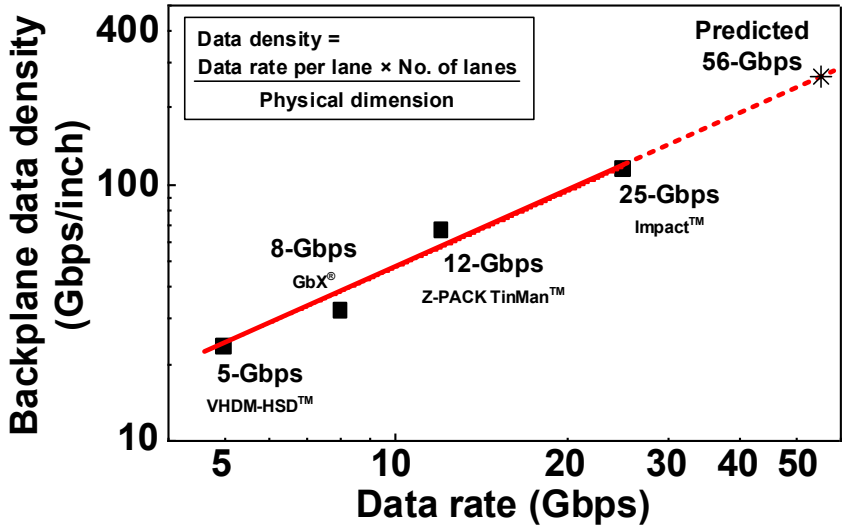
EMI in Modern Data Center

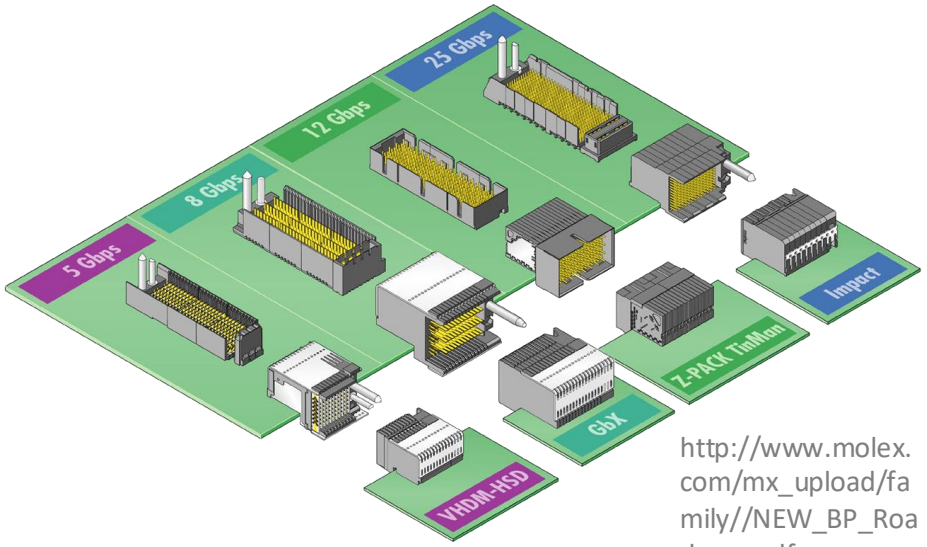
www.cisco.com/c/r/en/us/internet-of-everything-ioe/data-center/vision/index.html

https://avi.alkalay.net/2015/08/cloud-enabling-innovation-in-the-third-platform-era.html

- Front-side haven, but back-side disaster
- Thousands of paralleled communication modules
  - Data rate of each module > 10 Gbps
- Complicated electromagnetic environment

Increase of Data Density

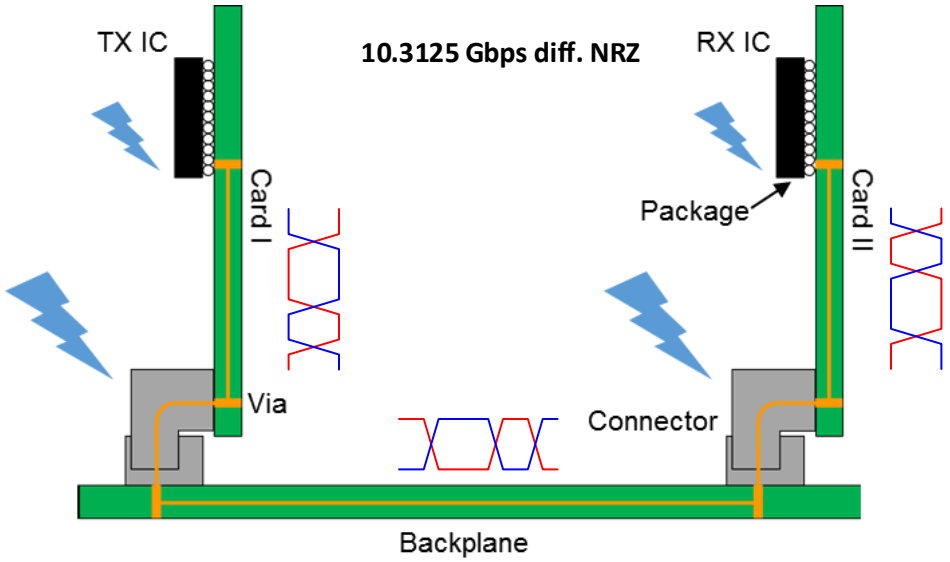


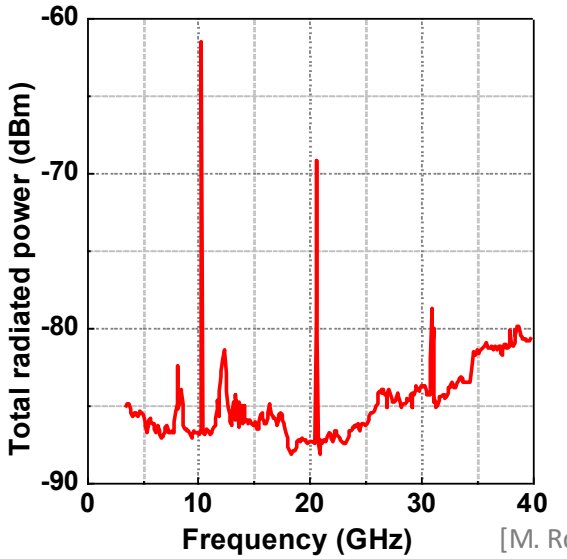


http://www.molex.com/mx_upload/family//NEW_BP_Roadmap.pdf

- High-speed backplane connectors roadmap (Molex®)
  - Higher data rate↑, higher data density↑
- For each backplane link
  - Smaller physical dimension, closer distance
  - Be more robust and quieter

EMI Case Study in Backplane Link

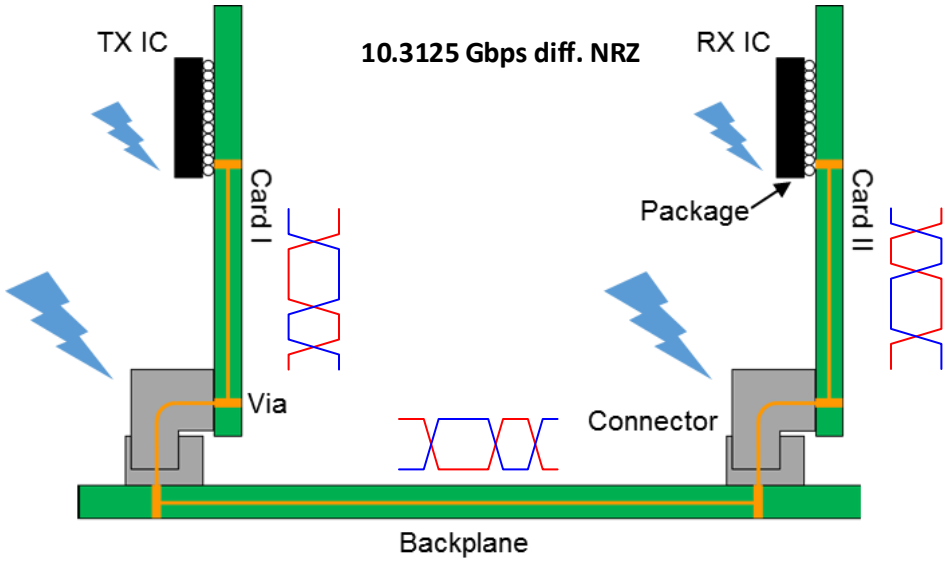


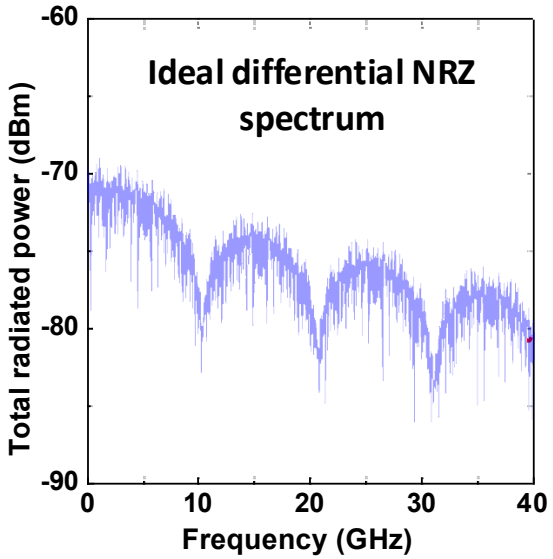


[M. Rowlands, DesignCon 2015]

- EMI radiation of backplane communication module
  - EMI radiations at $2f_{Nyquist}$, $4f_{Nyquist}$, … (e.g., 10 Gbps NRZ, $f_{Nyquist}$ = 5 GHz)
  - Ideal NRZ* data has no frequency component @ $2f_{Nyquist}$, $4f_{Nyquist}$, $6f_{Nyquist}$ …
    - NRZ = non-return-to-zero
- Distorted differential NRZ signals

EMI Case Study in Backplane Link





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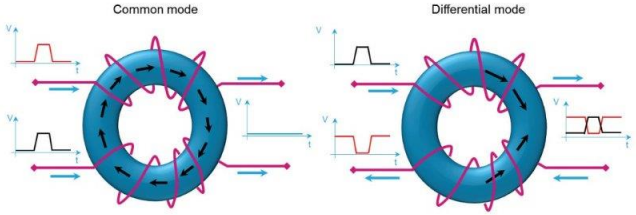
- Distorted differential NRZ signals

Previous Works

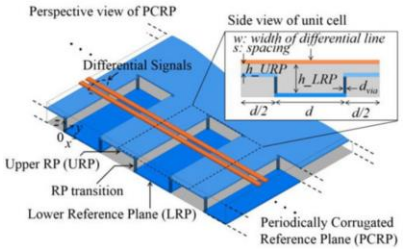
- CM noise dominates EMI radiation [1][6][7]
  - "Passive" solutions for CM noise suppression

CM Filter/Choke, BW < 5 GHz



[Murata, CM choke]

PCB structures (CM band-stop 5-10 GHz)

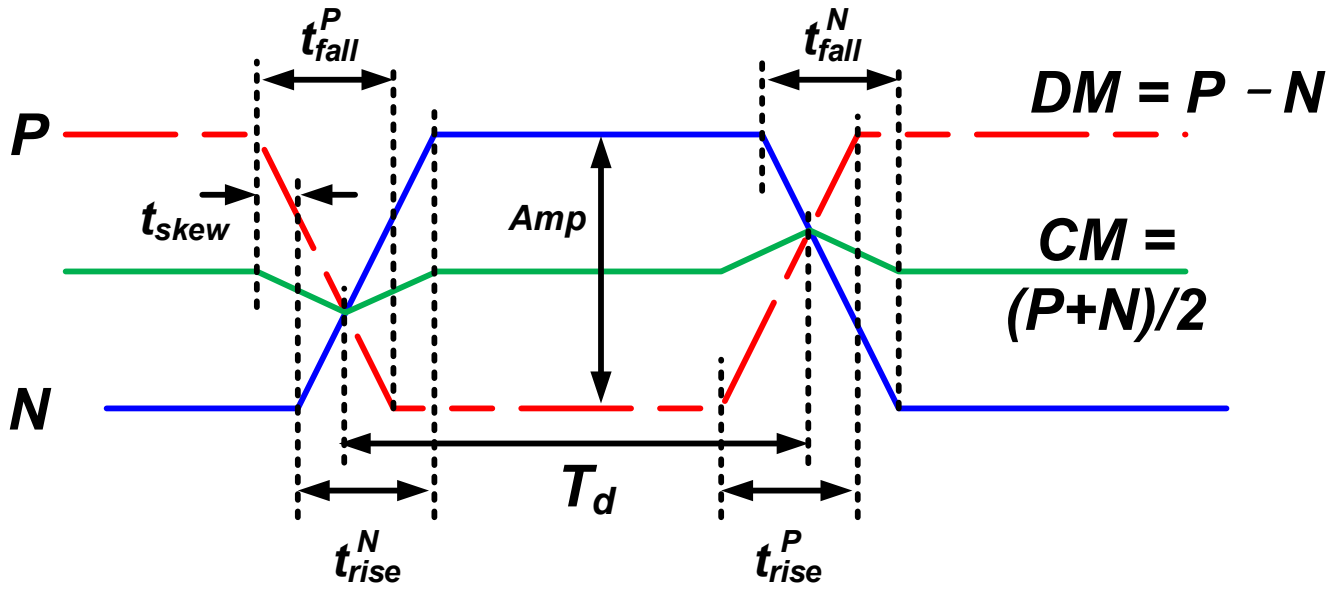


[Kim, TEMC 2016]

  - Current solutions: "find and patch"
  - How about eliminating the CM noise source of EMI radiation?
- Pioneer: Acimovic
  - In *DesignCon* 2007, he first described the CM noise at $2f_{Nyquist}$
  - No detailed analysis or verification
  - Passive CM filter solution
    - "Novel Band-Stop Common Mode Filter For High-Speed Digital Data Transmission"

What is the signal distortion that causes EMI radiation?

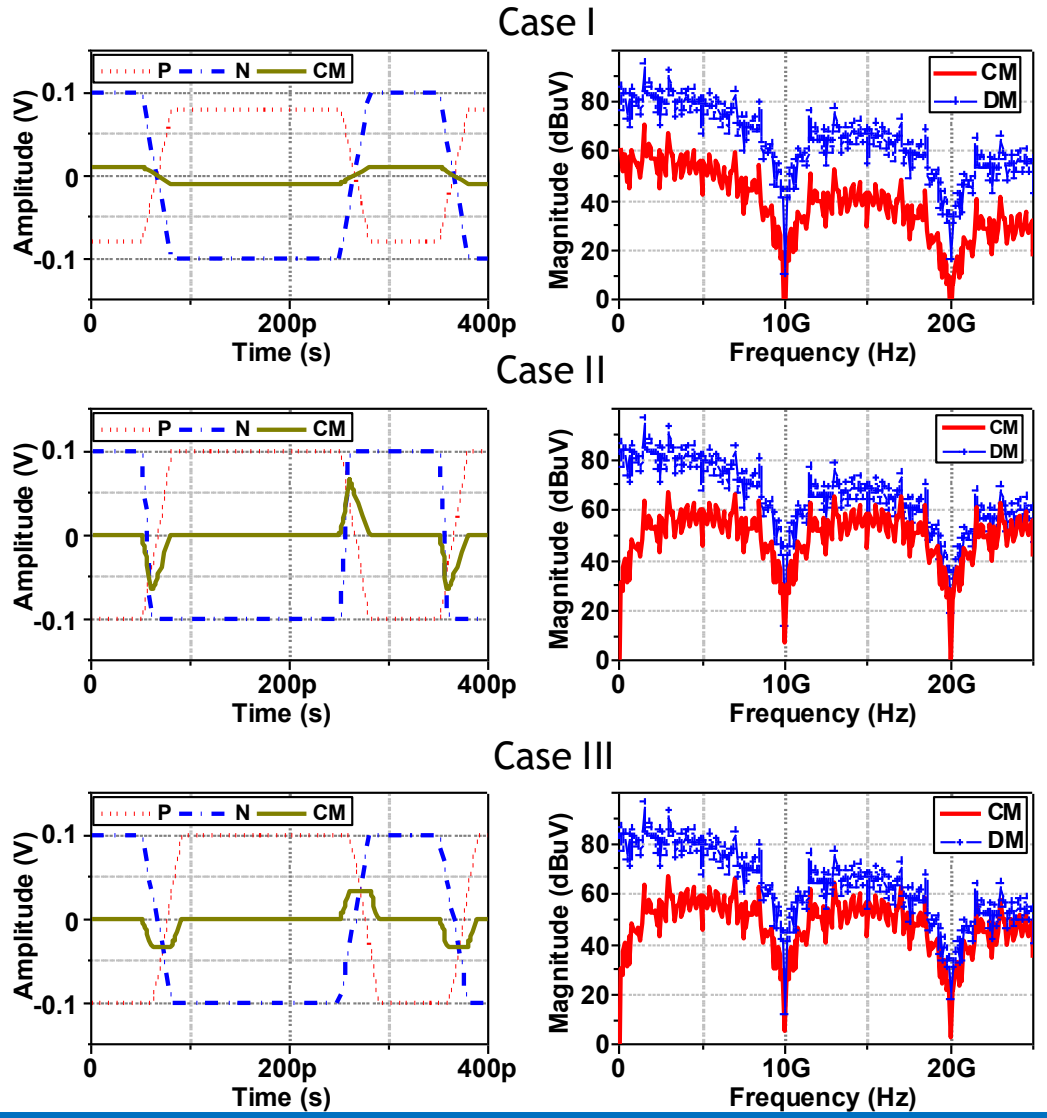
Distorted Differential NRZ Signals



- 4 types of distortions in differential (diff.) NRZ data
  - Case I: Inter-channel amplitude mismatch
  - Case II: Inter-channel skew
  - Case III: Inter-channel bandwidth mismatch (rise time / fall time)
  - Case IV: Intra-channel edge mismatch (rise time / fall time)

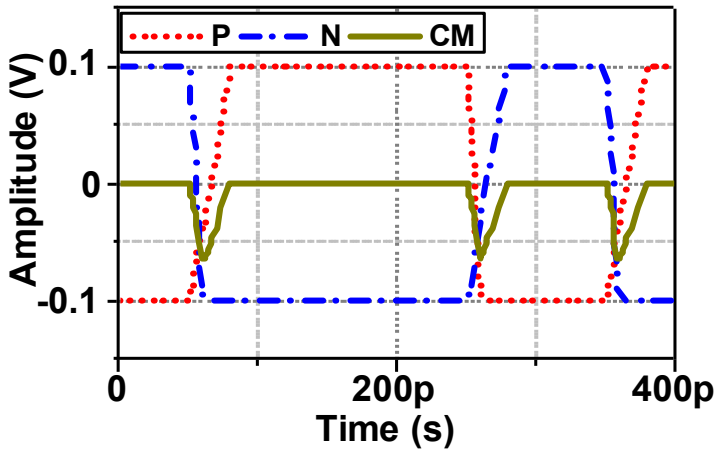
NRZ Signal Distortion: Case I/II/III

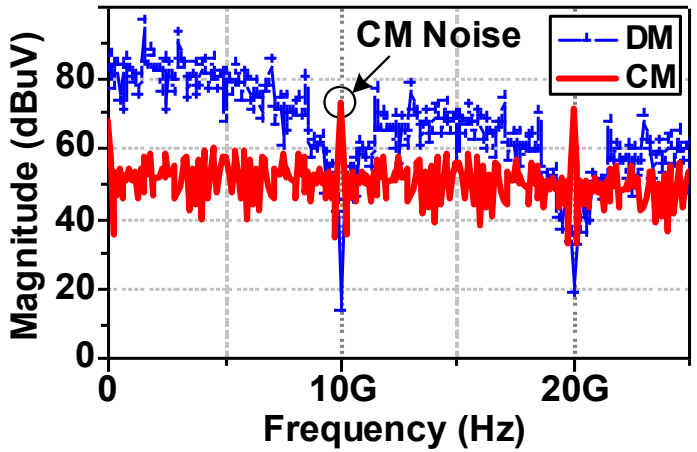
- Amplitude mismatch
  - $Amp_P = 0.8 \cdot Amp_N$
- Channel Skew
  - $t_{skew} = 10ps$
- Inter-channel bandwidth mismatch
  - $BW_P < BW_N$
  - $t_{rise}^P = t_{fall}^P > t_{rise}^N = t_{fall}^N$
- Similarity
  - Polarity of CM signal is data-dependent
  - Broadband CM signal spectrum
  - Linear distortion

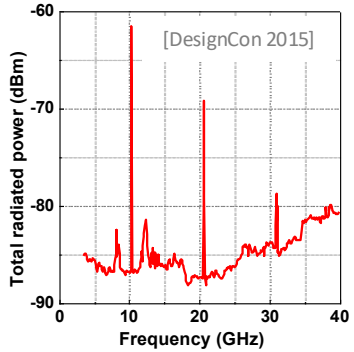


NRZ Signal Distortion: Case IV

- Case IV







- Intra-channel edge mismatch
  - $t^P_{rise} = t^N_{rise} > t^P_{fall} = t^N_{fall}$
  - Polarity of CM signal is data-independent
  - Large noise tone @ 10 GHz ($2f_{Nyquist}$)

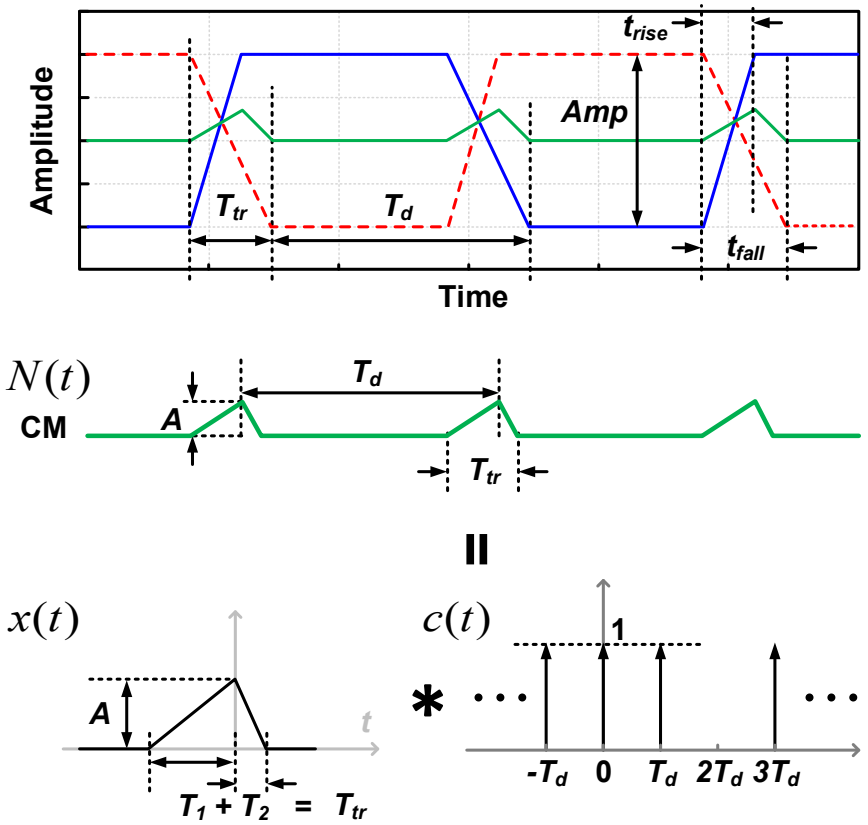
- **Non-linear distortion**
- **New noise tone @ 2fNyquist**
- **'CM noise' is specified to be the noise at $2f_{Nyquist}$**

Calculate the CM Noise @ $2f_{Nyquist}$

- Fourier transform of CM signal, *F(N(t))*
  - $F(N(t)) = F(x(t) * c(t)) = F(x(t)) \cdot F(c(t))$

- CM noise @ $2f_{Nyquist}$
  - $F(2f_{Nyquist}) = F(\frac{1}{T_d})$

- *A* and T_{tr} is calculated as
  - $A = \frac{Amp}{2} \cdot \frac{|t_{rise} - t_{fall}|}{T_{tr}}$
  - $T_{tr} = \max(t_{rise}, t_{fall})$

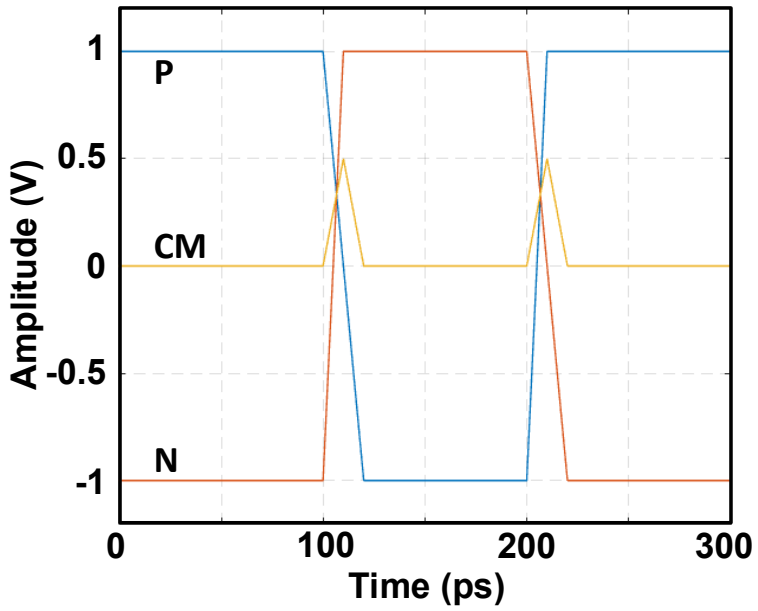


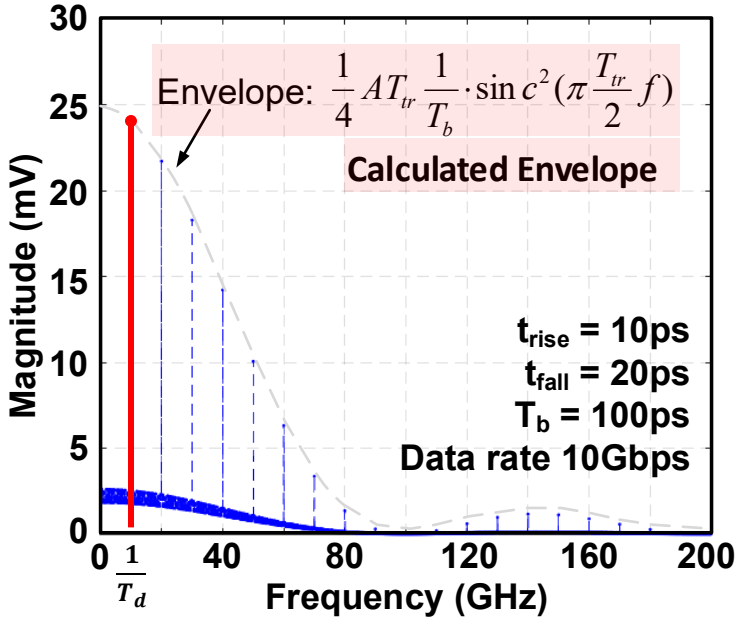
Fourier Transform of CM Signal

- CM signal

$$\|F_N(f)\| = \|X(f)\cdot F_c(f)\| = X(f)\cdot\|F_c(f)\| = \begin{cases} \frac{1}{4}AT_{tr}\frac{1}{T_d}\sin c^2(\frac{\pi}{2}T_{tr}f), & f=\frac{n}{T_d} \\ \frac{1}{4}AT_{tr}\sqrt{\frac{1}{T_d}}\sin c^2(\frac{\pi}{2}T_{tr}f), & f\neq\frac{n}{T_d} \end{cases}, n\in Z$$

- MATLAB simulation (data rate: $1/T_d >> 1$) vs. calculation results





Calculation of CM Noise @ $2f_{Nyquist}$

- $F_N(2f_{Nyquist}) = \frac{1}{4} A \frac{T_{tr}}{T_d} \sin c^2(\frac{\pi}{2} \cdot \frac{T_{tr}}{T_d}) = \frac{Amp}{8} \cdot \frac{|t_{rise} - t_{fall}|}{T_d} \cdot \sin c^2(\frac{\pi}{2} \cdot \frac{T_{tr}}{T_d})$
- $A = \frac{Amp}{2} \cdot \frac{|t_{rise} - t_{fall}|}{T_{tr}}$ $\quad 2f_{Nyquist}, = \frac{1}{T_d}$

When $T_{tr} << T_d$

This term is about 1

- The CM noise is positively correlated with
  - Data rate (10 years ago, Acimovic's work in *DesignCon* 2007 did not draw much attention)
  - Signal swing
  - Mismatch of rising and falling edges

$$F_N(2f_{Nyquist}) \propto A \cdot \frac{1}{T_d} \cdot T_{tr} \propto Amp \cdot |t_{rise} - t_{fall}| \cdot \frac{1}{T_d}$$

Conclusion

- CM noise dominates the EMI radiation
- Non-linear distortion generates the CM noise tone @$2f_{Nyquist}$, $4f_{Nyquist}$, $6f_{Nyquist}$ …
- The CM noise at $2f_{Nyquist}$ is largest
- The CM noise increases noise floor
- The CM noise is a data-dependent random process

$$F_N(2f_{Nyquist}) \propto A \cdot \frac{1}{T_d} \cdot \boxed{T_{tr}} \propto Amp \cdot \left| t_{rise} - t_{fall} \right| \cdot \frac{1}{T_d}$$

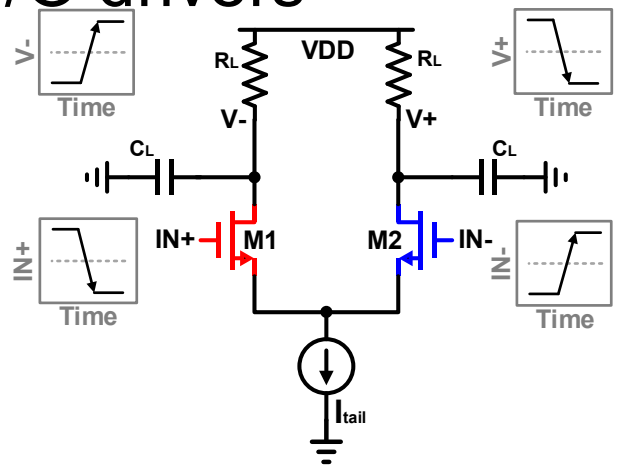
- Sharp data edge (smaller T_{tr}) reduces the EMI-related CM noise

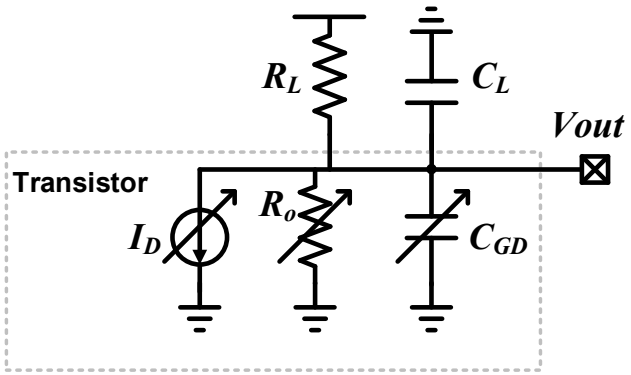
How is the distortion generated?

Non-linearity of high-speed I/O driver

CM Noise in CML Driver

- Current mode logic (CML) circuit are widely used for high-speed I/O drivers





- Equivalent circuits of M1 and M2
  - Rising/falling edge calculation: $V_{out} = V_{initial} + I_D \cdot R_{total}(1 - e^{-\frac{1}{R_{total}C_{total}}t})$
  - I_D, R_o and C_{GD} varies with biasing voltage (V_{GS} and V_{DS})
  - Mismatch of rising and falling edges is a function of V_{GS} and V_{DS}

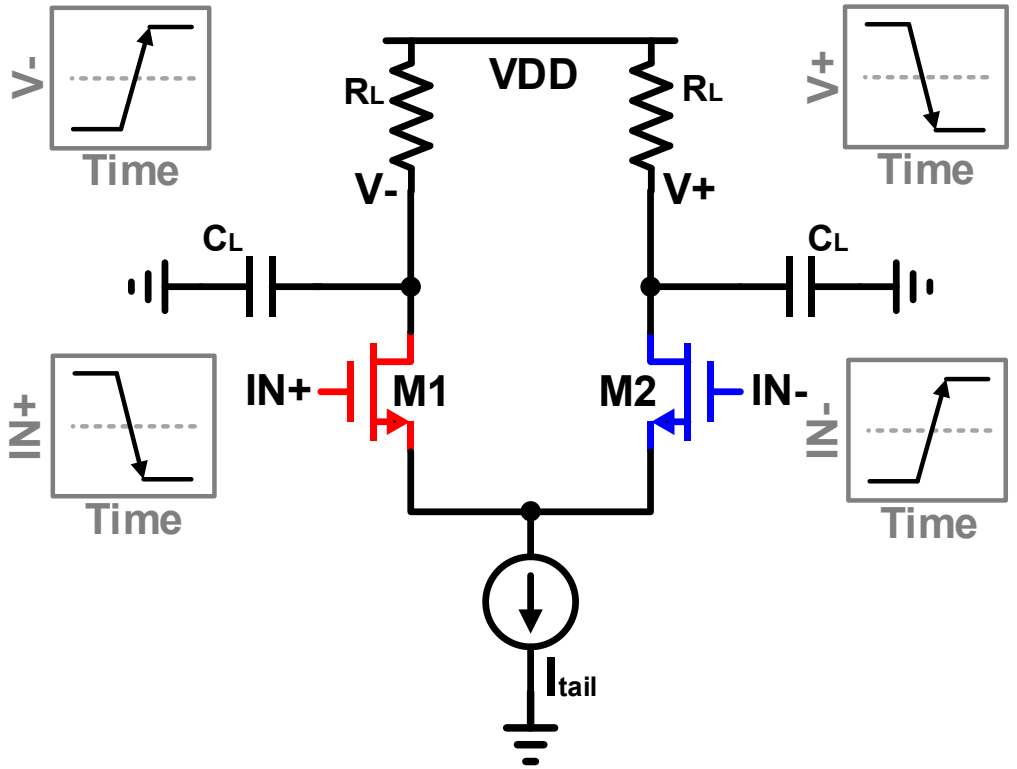
$$\left|t_{rise} - t_{fall}\right| = t(\Delta V_{GS}, \Delta V_{DS})$$

CM Noise in CML Driver

$$\left|t_{rise} - t_{fall}\right| = t(\Delta V_{GS}, \Delta V_{DS})$$

$$F_N(2f_{Nyquist}) \propto Amp \cdot \left|t_{rise} - t_{fall}\right| \cdot \frac{1}{T_d}$$

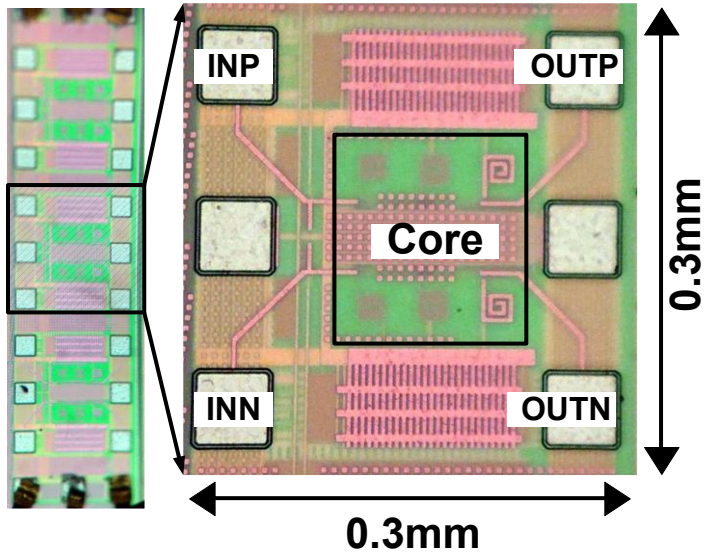
- Completely reversed voltage variations
  - M1: $V_{GS}\downarrow$, $V_{DS}\uparrow$
  - M2: $V_{GS}\uparrow$, $V_{DS}\downarrow$
- Intrinsic mismatch of rising and falling edges
  - Not able to eliminate the CM noise
  - Optimize V_{GS} to minimize $\left|t_{rise} - t_{fall}\right|$?
  - Reduce the amplitude *Amp* ?

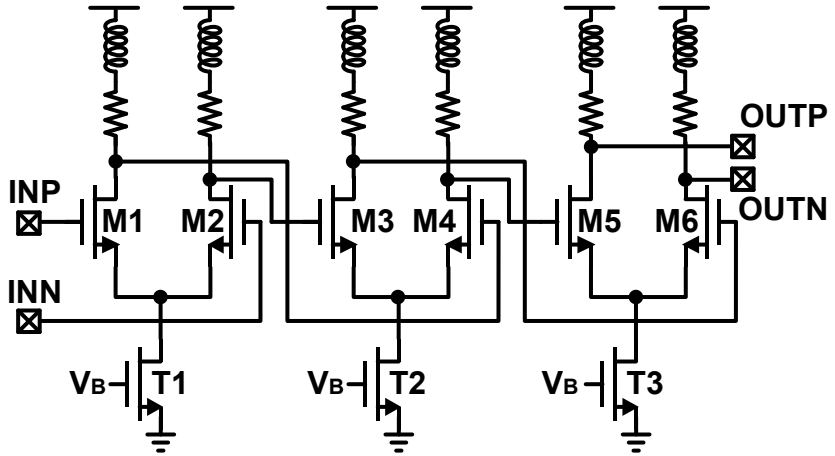


Measurement & Verification

A test chip in a 65nm CMOS process

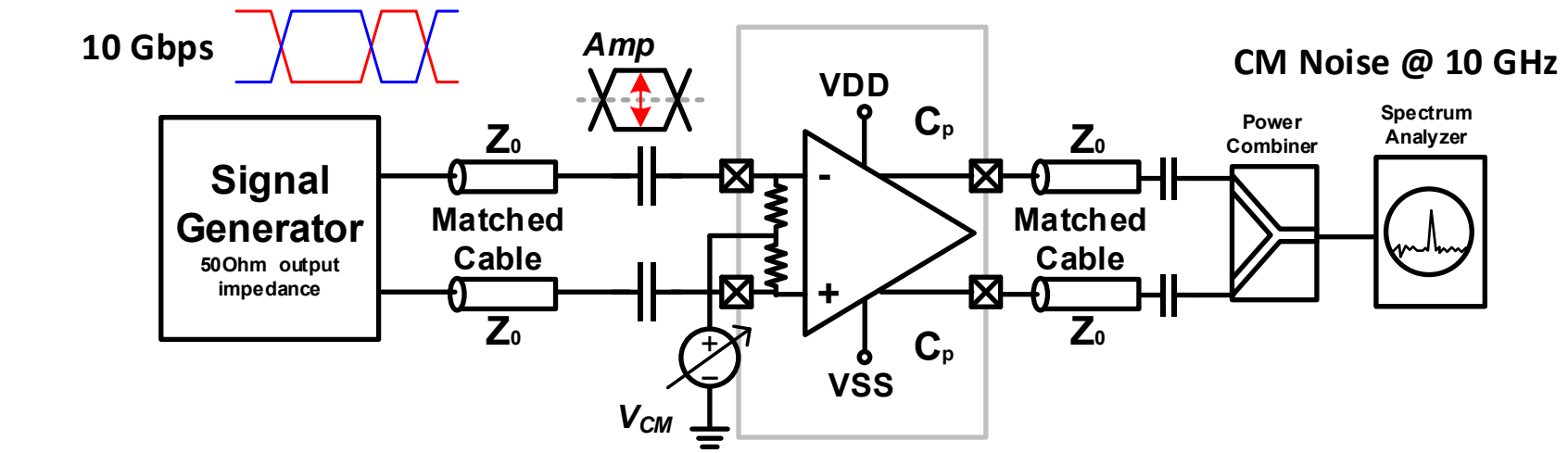
Test Chip: CML Driver Circuit

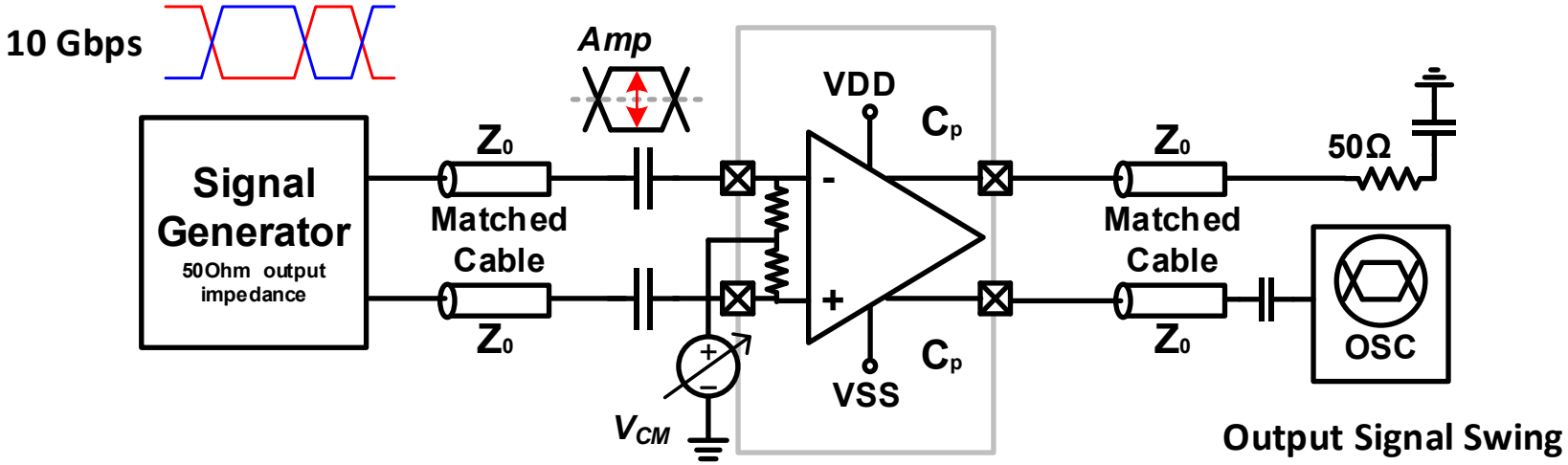




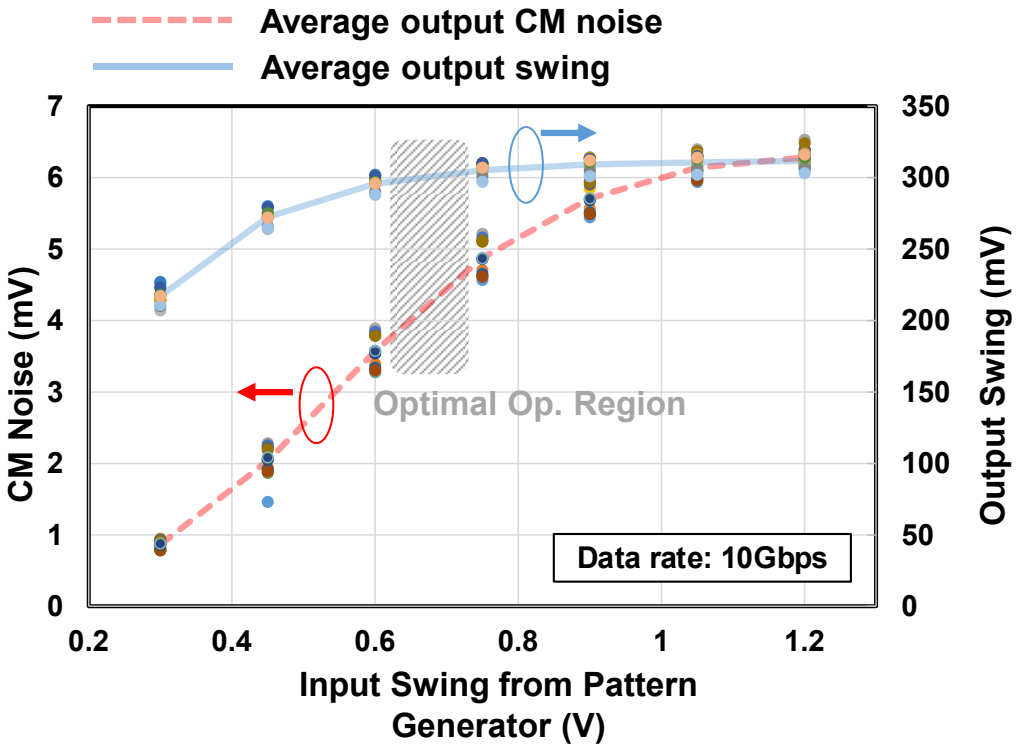
- Test chip information
  - 3-stage cascaded CML driver in a 65nm CMOS process
- Measurements
  - Output CM noise & output signal

Measurement: CM Noise & Output Signal





CM Noise vs. Signal Amplitude



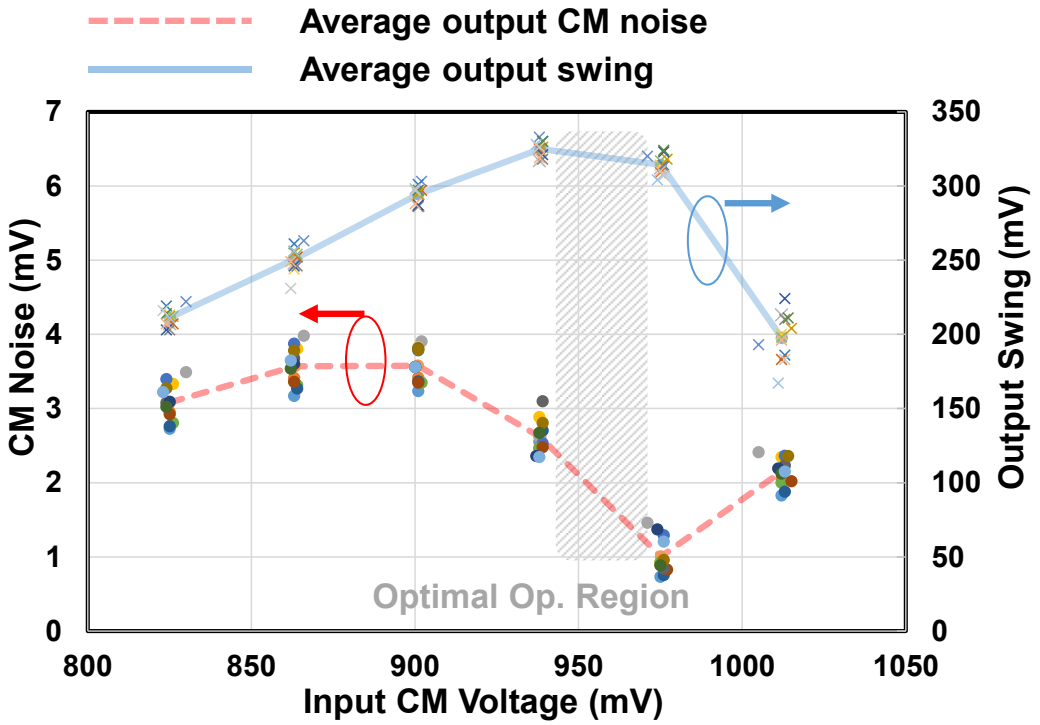
- 13 chip samples
- Averaged CM noise
- Averaged output swing
- Power supply 1.2 V
- V_{CM} = 0.9 V

- Positive correlation: $F_N(2f_{Nyquist}) \propto Amp$
- Input swing ↑, output swing saturates faster than CM noise

$$\left|t_{rise} - t_{fall}\right| = t(\Delta V_{GS}, \Delta V_{DS})$$

  - 90% amplitude → 57% CM noise (amplitude back-off)

CM Noise vs. Biasing Voltage



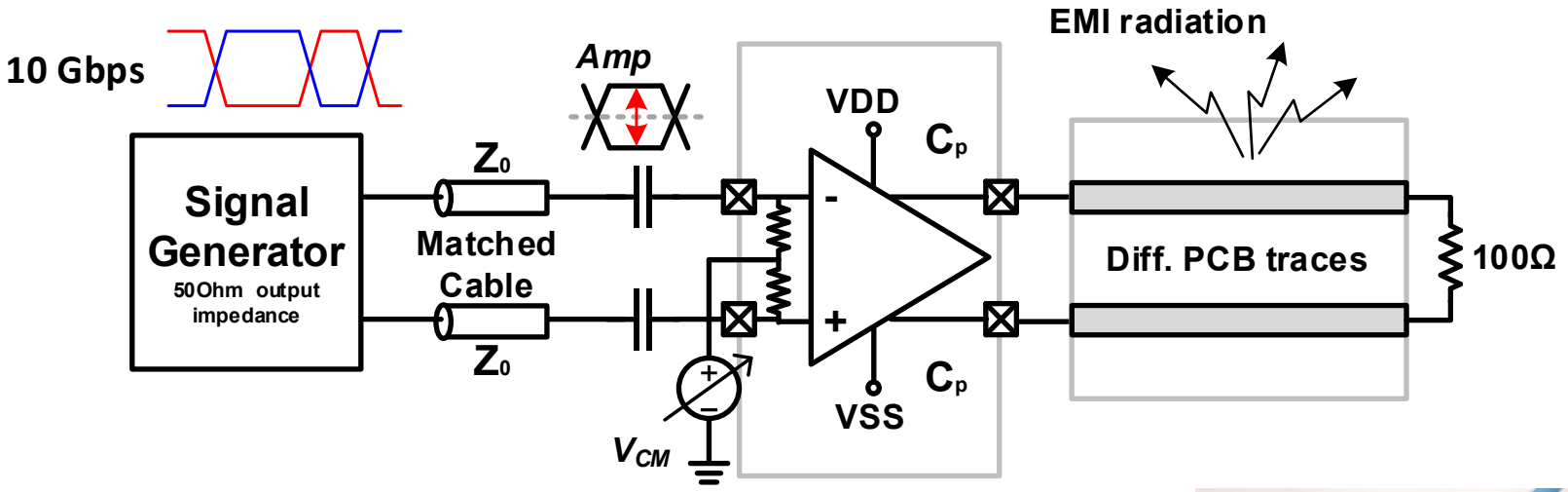
- 13 chip samples
- Averaged CM noise
- Averaged output swing
- Power supply 1.2 V
- Amp = 0.6 V

- $|t_{rise} - t_{fall}| = t(\Delta V_{GS}, \Delta V_{DS})$, $F_N(2f_{Nyquist}) \propto |t_{rise} - t_{fall}|$
- Optimal Input biasing voltage (V_{GS}) to reduce CM noise
  - Balancing the rising and falling edge: $|t_{rise} - t_{fall}| \downarrow$
  - Providing sufficient output swing for communication quality

Is the EMI radiation reduced?

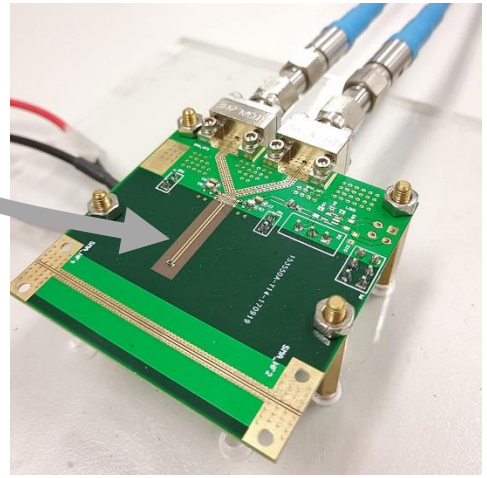
Definitely, it is.

EMI Radiation Measurement



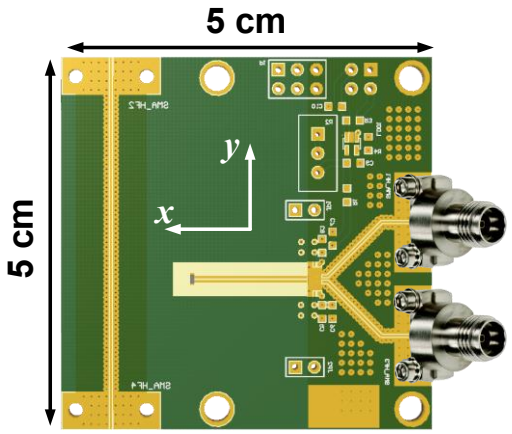
- EMI Measurement setup
  - 10 Gbps diff. PRBS input
  - Differential output PCB traces
    - PCB trace Z_0 = 50 Ohm
    - 100 Ohm far-end termination resistor

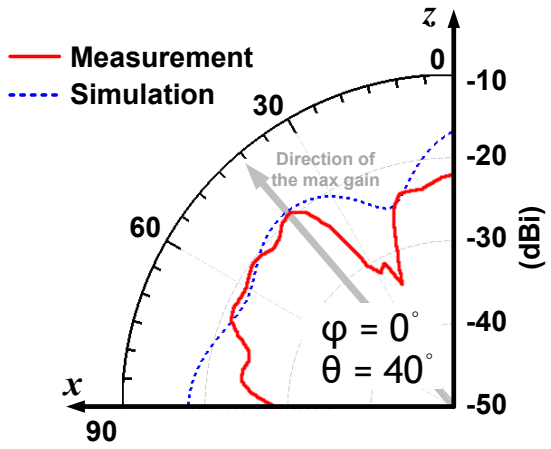
Output diff. traces (radiator)

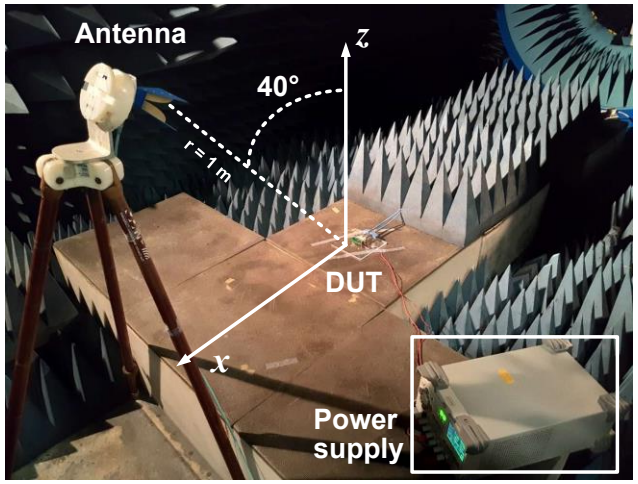


Where to Place the Antenna?

- **Antenna is used to collect radiated EMI emission**



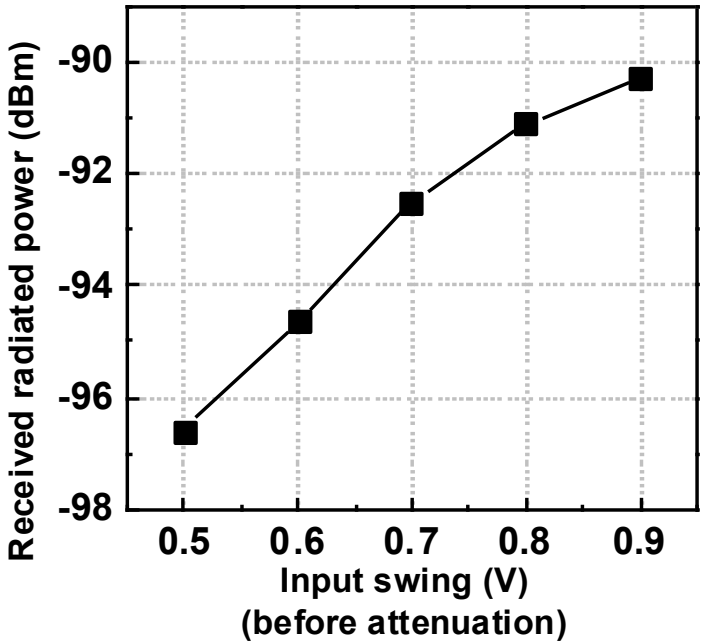


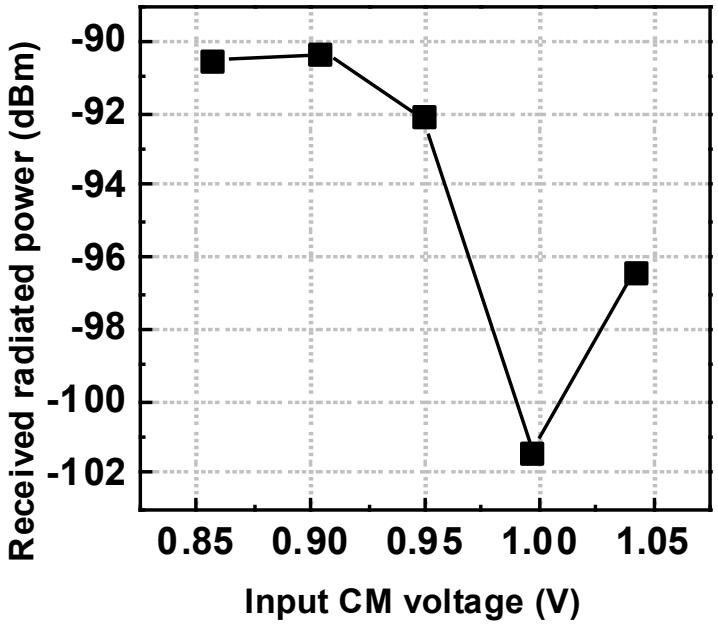


Testing site in an anechoic chamber

- Maximum far-field radiation
  - CM radiation pattern, maximum gain: **φ = 0° , θ = 40°**
  - Far-field Fraunhofer distance: $r \geq \frac{2d^2}{\lambda} = 72cm$, so $r = 1m$
    - d = 10.4 cm, the maximum dimension of antenna; λ = 3 cm, 10 GHz wavelength

EMI Radiation Measurement Result





- Signal swing vs. EMI radiation

$$EMI \propto F_N(2f_{Nyquist}) \propto Amp$$

- **Biasing voltage vs. EMI radiation**
  - **Optimal biasing condition**

$$|t_{rise} - t_{fall}| = t(\Delta V_{GS}, \Delta V_{DS})$$

$$EMI \propto F_N(2f_{Nyquist}) \propto |t_{rise} - t_{fall}|$$

- **CM noise dominates EMI radiation**

Conclusion

- CM noise is intrinsically existed in I/O buffers
  - Non-linear variation during large-signal operation in transistors

- Given a certain data rate, CM noise is positively correlated to
  - Signal swing
  - Edge mismatch

$$F_N(2f_{Nyquist}) \propto Amp$$
$$F_N(2f_{Nyquist}) \propto |t_{rise} - t_{fall}|$$

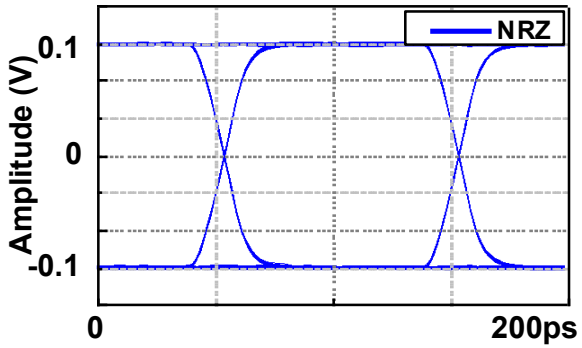
- Suppress CM noise to reduce EMI radiation
  - Limit the signal swing and do not over drive the circuit
  - Optimize the biasing voltage to balance data edges

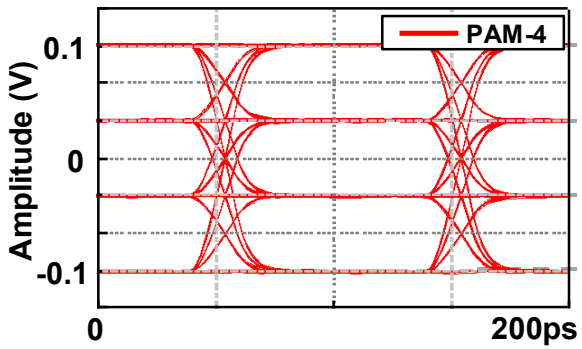
A more complicated case: PAM-4

From NRZ to PAM-4

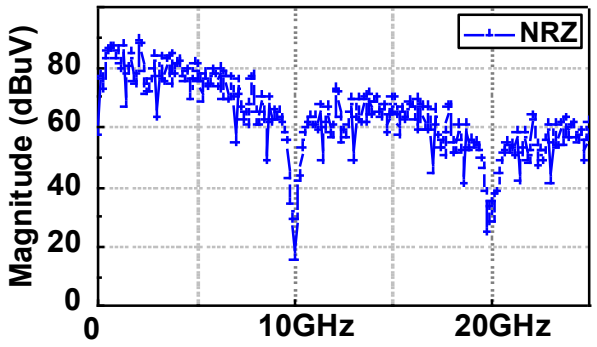
- **Eye-diagram of 10 GB PAM-4**
  - **Doubled data rate: 20 Gbps**
  - **4 data levels (00, 01, 10 ,11)**
  - **16 data transitions**
  - **Higher bandwidth efficiency**

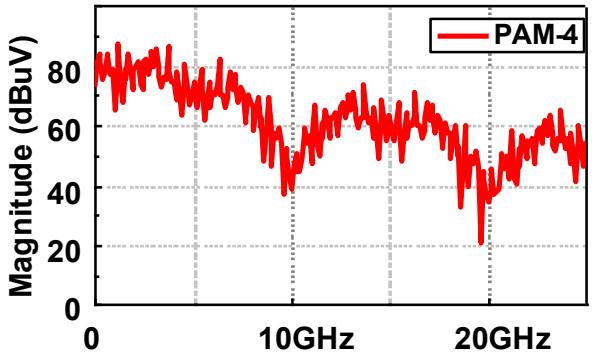
- Eye-diagram of 10 GB NRZ
  - 10 Gbps
  - 2 data levels (0, 1)
  - 4 data transitions





11 Level 3
10 Level 2
01 Level 1
00 Level 0

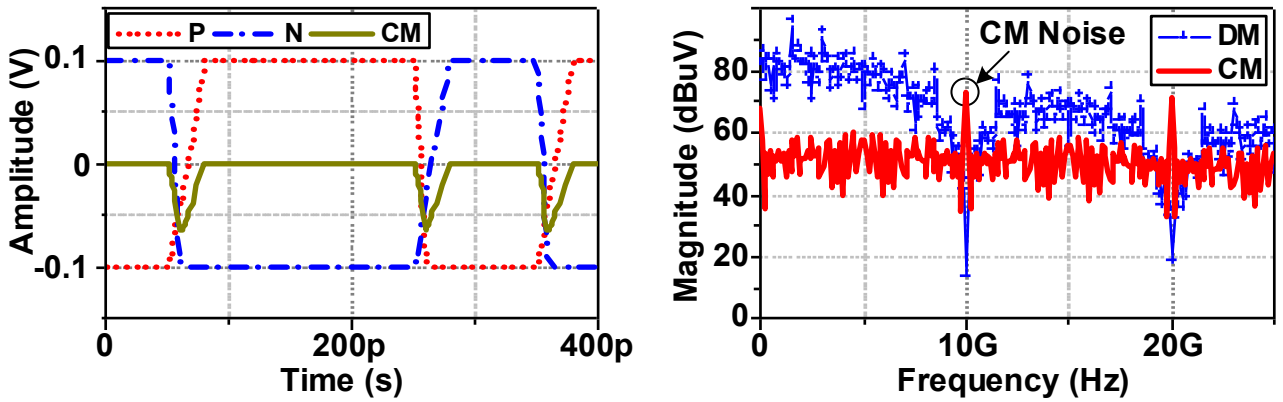




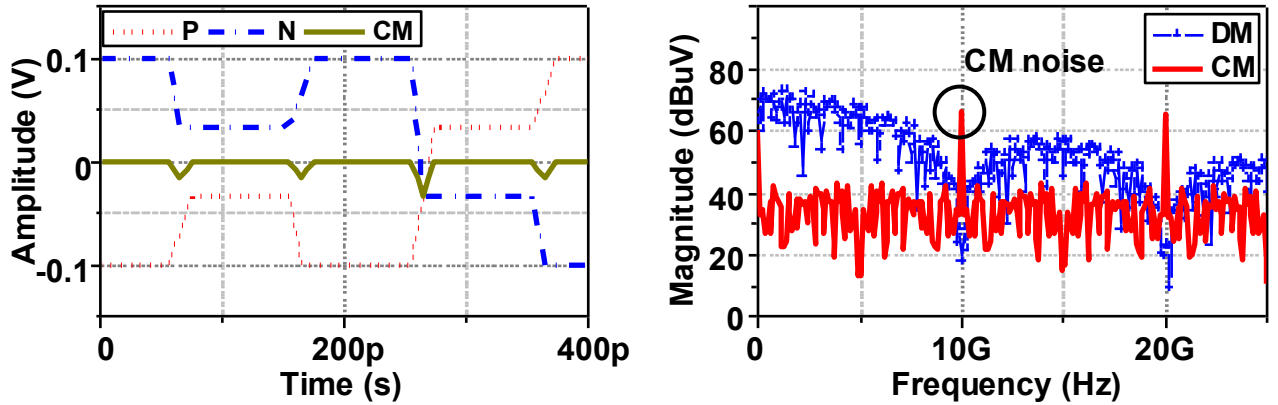
- **Eye-diagram: 10Gbps NRZ vs. 20Gbps PAM-4**
  - **<u>Four</u> possible data levels per symbol, data rate is doubled**
  - **Higher bandwidth efficiency**
  - **Key solution for next 200/400 GbE communication**

EMI Issue in Diff. PAM-4 Signals

- NRZ



- PAM-4



- Intra-Channel edge mismatch
  - Similar to differential NRZ signals
  - $t_{rise}^{P} = t_{rise}^{N} = 25\text{p} > t_{fall}^{P} = t_{fall}^{N} = 10\text{ps}$

How to describe the CM noise in PAM-4 systems?

From NRZ to PAM-4

- Equation for NRZ

$$F_N(2f_{Nyquist}) = \frac{Amp}{8} \cdot \frac{|t_{rise} - t_{fall}|}{T_d} \cdot \sin c^2\left(\frac{\pi}{2} \cdot \frac{T_{tr}}{T_d}\right)$$

- Upgraded equation for PAM-4
  - Data period T_d → Symbol period T_s
  - Mismatch of rise and fall time depends on circuit physical structure
  - *Amp* → expected value of amplitude, *E(Amp)*

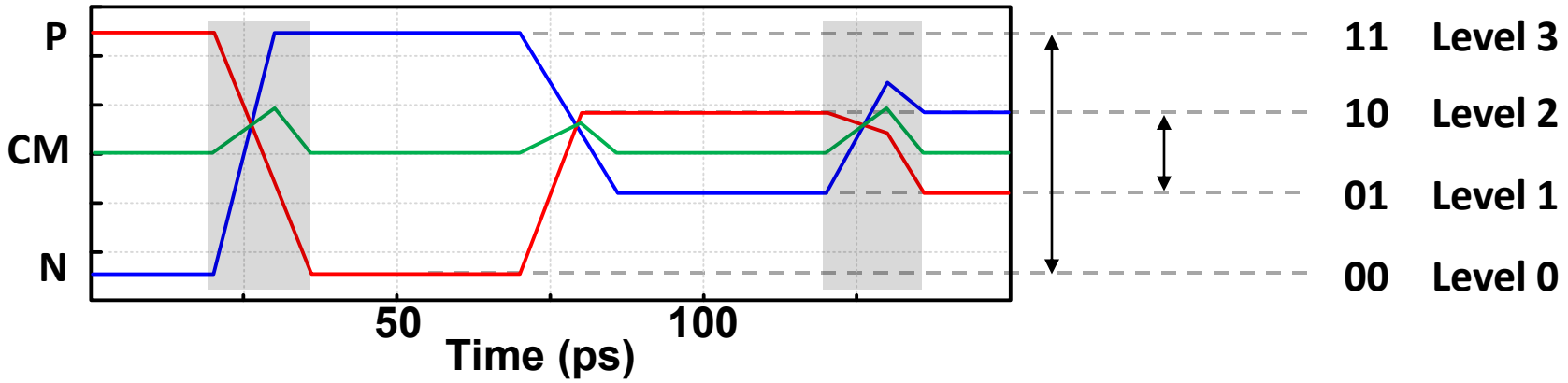
$$F_N(2f_{Nyquist}) = \frac{E(Amp)}{8} \cdot \frac{|t_{rise} - t_{fall}|}{T_s} \cdot \sin c^2\left(\frac{\pi}{2} \cdot \frac{T_{tr}}{T_s}\right)$$

- How to calculate *E(Amp)*?

CM Noise vs. “Amplitude”

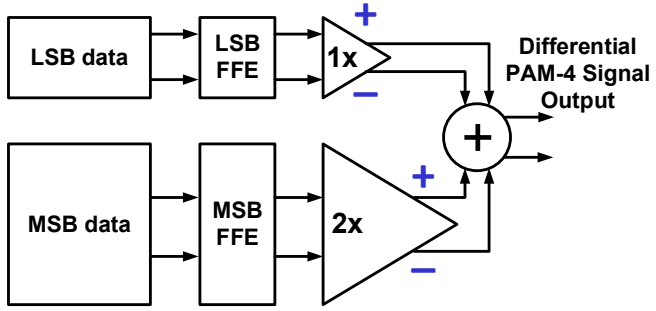
- Conclusions for NRZ
  - CM noise is positively correlated to amplitude $F_N(2f_{Nyquist}) \propto Amp$

- PAM-4
  - CM noise is not positively correlated to amplitude
    - Data transition between Level 0 and Level 3
    - Data transition between Level 1 and Level 2

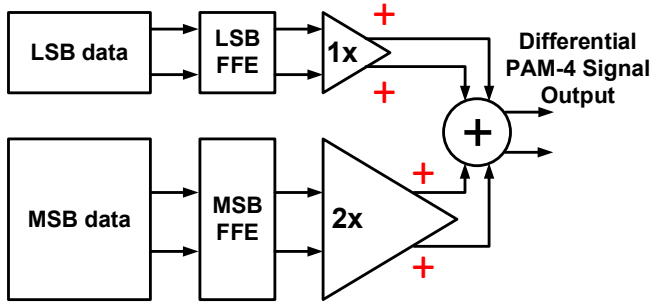


CM Noise of PAM-4 Signals

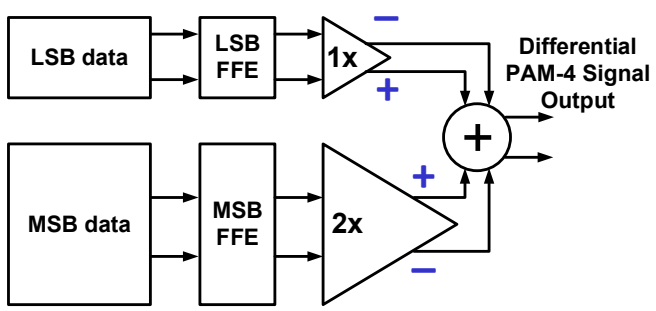
- Data transition: 00 → 11
  - MSB: 0 → 1
  - LSB: 0 → 1
- DM: $+DM_{MSB} + DM_{LSB}$



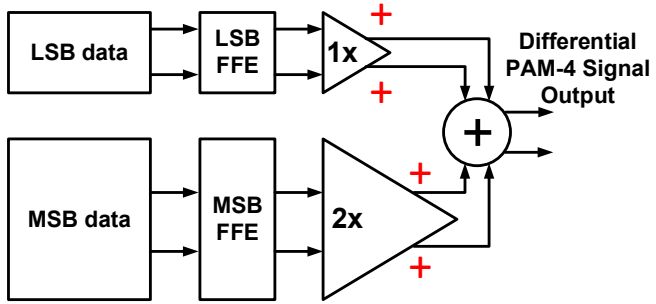
- CM: $+CM_{MSB} + CM_{LSB}$



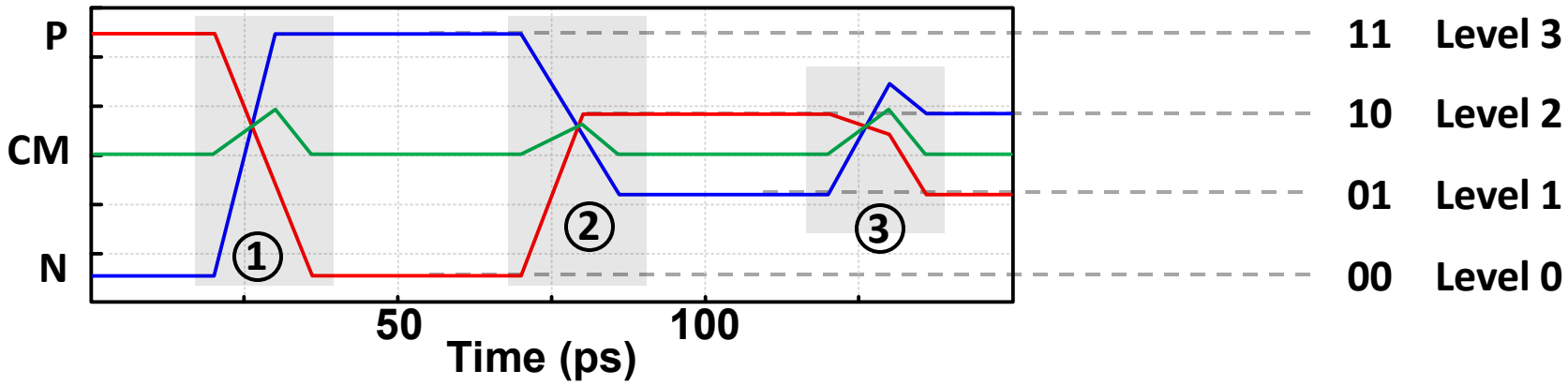
- **Data transition: 01 → 10**
  - **MSB: 0 → 1**
  - **LSB:1 → 0**
- **DM: $+DM_{MSB} - DM_{LSB}$**



- **CM: $+CM_{MSB} + CM_{LSB}$**



CM Noise of PAM-4 Signals



- CM noise is correlated to data transitions
- Switching distance (SD) to describe <u>how many bits are switched</u>

$$SD(A,B)=\sum_k W_k\cdot(A[k]\oplus B[k]),\ W_k=2^{k-1}$$

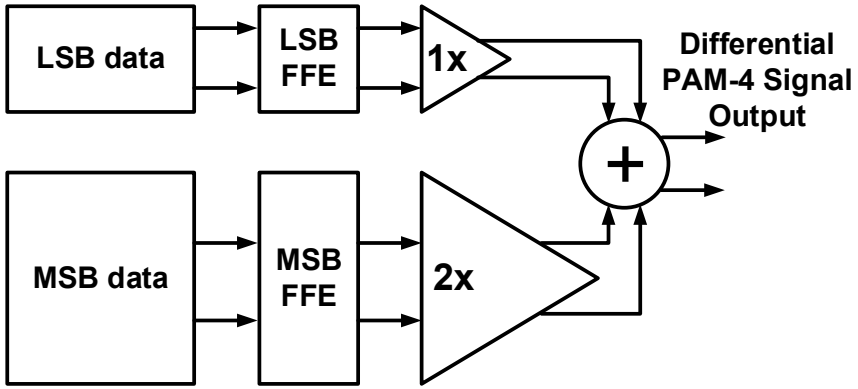
$$\boxed{N_{CM}\propto SD} \qquad SD(00,11)=SD(01,10)=MSB+LSB$$

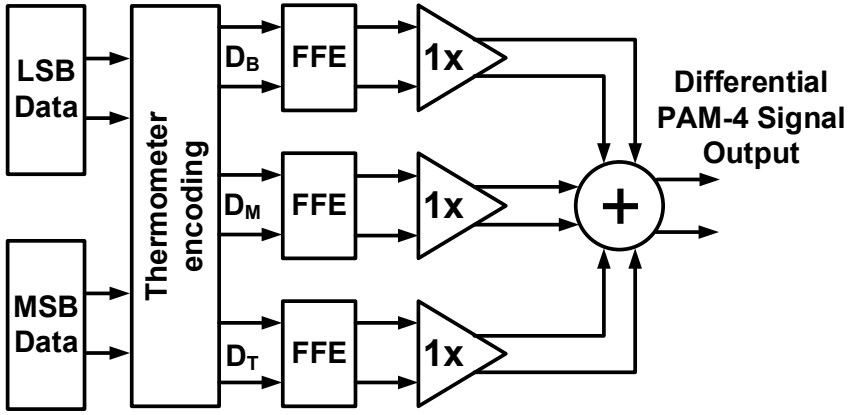
- CM noise is positively correlated to SD

$E(Amp) \longrightarrow E(SD)$

Look back to the generation of PAM-4 signals

E(SD) in Different PAM-4 Architectures





- Binary-scaled (BS)

MSB	LSB
0	0
0	1
1	0
1	1

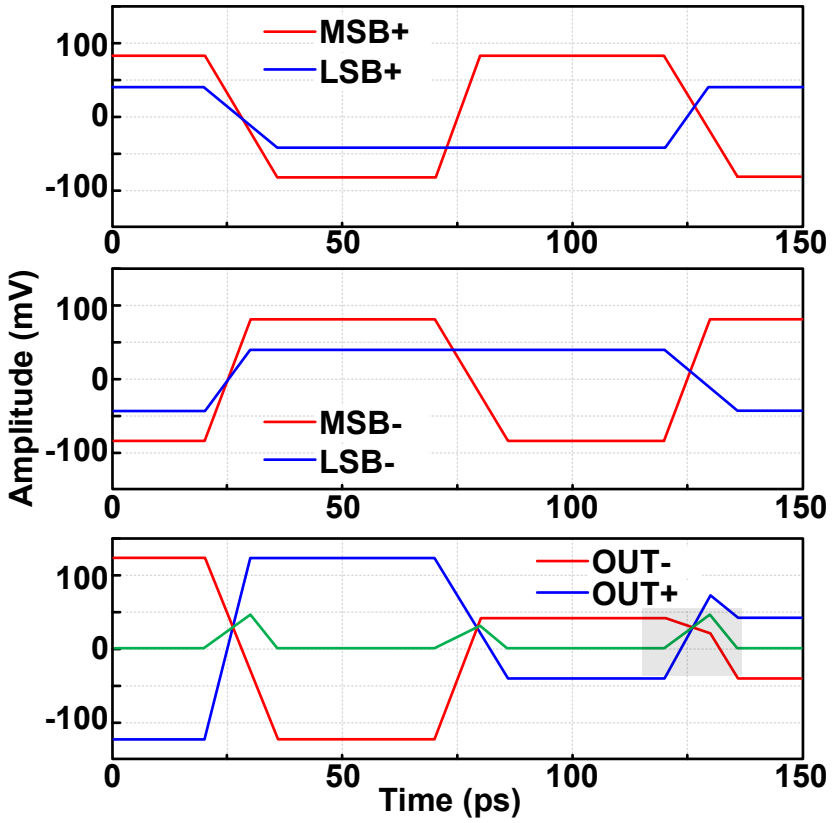
$$V_{PAM-4} = 2V_{MSB} + V_{LSB}$$

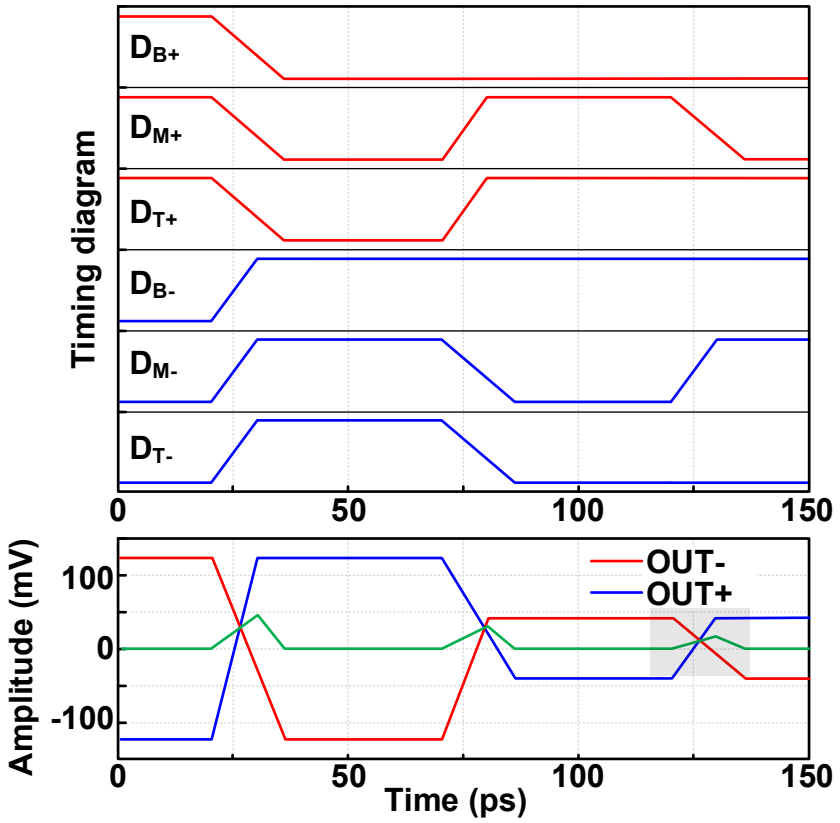
- **Thermometer-coded (TC)**

D_B	D_M	D_T
0	0	0
1	0	0
1	1	0
1	1	1

$$V_{PAM-4} = V_{DT} + V_{DM} + V_{DB}$$

Transient Waveform: BS vs. TC





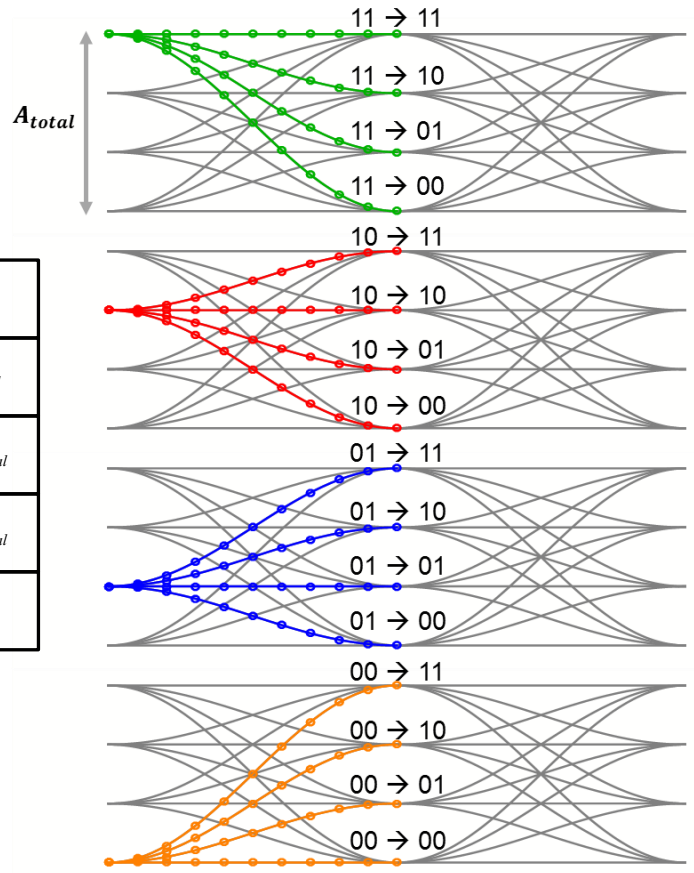
- Binary-scaled (BS)

$$-V_{PAM-4} = 2V_{MSB} + V_{LSB}$$

- **Thermometer-coded (TC)**
  - $V_{PAM-4} = V_{DT} + V_{DM} + V_{DB}$
  - **Smaller CM noise?**

E(SD) of Binary-Scaled PAM-4

SD: S_y / S_x	S_0 00	S_1 01	S_2 10	S_3 11
S_0 00	0	$\frac{1}{3}A_{total}$	$\frac{2}{3}A_{total}$	A_{total}
S_1 01	$\frac{1}{3}A_{total}$	0	A_{total}	$\frac{2}{3}A_{total}$
S_2 10	$\frac{2}{3}A_{total}$	A_{total}	0	$\frac{1}{3}A_{total}$
S_3 11	A_{total}	$\frac{2}{3}A_{total}$	$\frac{1}{3}A_{total}$	0



$$\frac{1}{16}\left(0+\frac{1}{3}A_{total}+\frac{2}{3}A_{total}+\frac{3}{3}A_{total}\right)$$

$$+$$

$$\frac{1}{16}\left(\frac{1}{3}A_{total}+0+\frac{3}{3}A_{total}+\frac{2}{3}A_{total}\right)$$

$$+ \qquad = \frac{1}{2}A_{total}$$

$$\frac{1}{16}\left(\frac{2}{3}A_{total}+\frac{3}{3}A_{total}+0+\frac{1}{3}A_{total}\right)$$

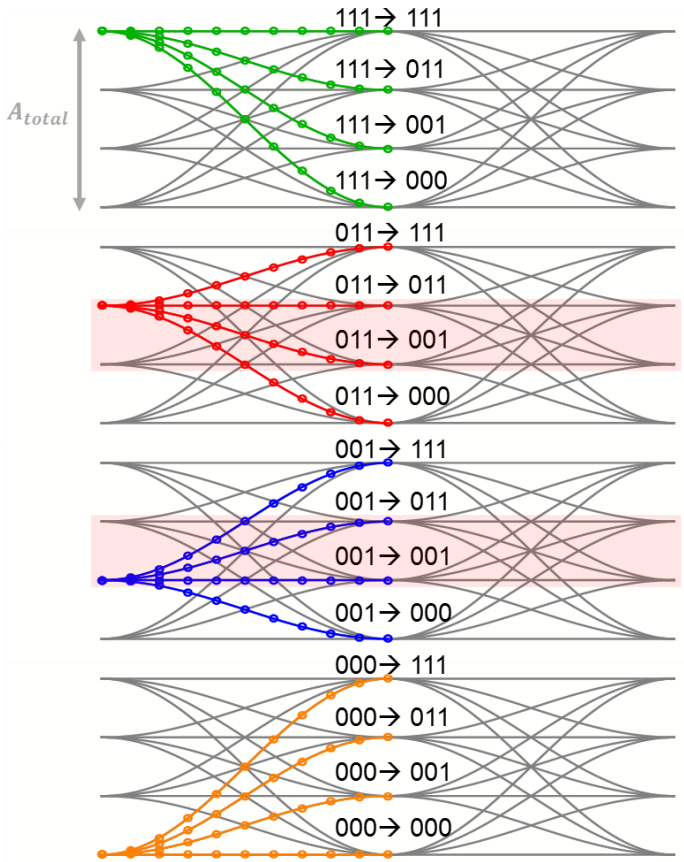
$$+$$

$$\frac{1}{16}\left(\frac{3}{3}A_{total}+\frac{2}{3}A_{total}+\frac{1}{3}A_{total}+0\right)$$

- $$E(SD)=\sum_{n=0}^{3}\sum_{m=0}^{3}p_{n,m}\cdot SD(S_n,S_m)=\frac{1}{16}\cdot\sum_{n=0}^{3}\sum_{m=0}^{3}SD(S_n,S_m)=\frac{1}{2}A_{total}$$

E(SD) of Thermometer-Coded PAM-4

S_y \ S_x	S_0 000	S_1 001	S_2 011	S_3 111
S_0 000	0	$\frac{1}{3}A_{total}$	$\frac{2}{3}A_{total}$	A_{total}
S_1 001	$\frac{1}{3}A_{total}$	0	$\frac{1}{3}A_{total}$	$\frac{2}{3}A_{total}$
S_2 011	$\frac{2}{3}A_{total}$	$\frac{1}{3}A_{total}$	0	$\frac{1}{3}A_{total}$
S_3 111	A_{total}	$\frac{2}{3}A_{total}$	$\frac{1}{3}A_{total}$	0



$$\frac{1}{16}\left(0+\frac{1}{3}A_{total}+\frac{2}{3}A_{total}+\frac{3}{3}A_{total}\right)$$

$$+$$

$$\frac{1}{16}\left(\frac{1}{3}A_{total}+0+\frac{1}{3}A_{total}+\frac{2}{3}A_{total}\right)$$

$$+ \qquad = \frac{5}{12}A_{total}$$

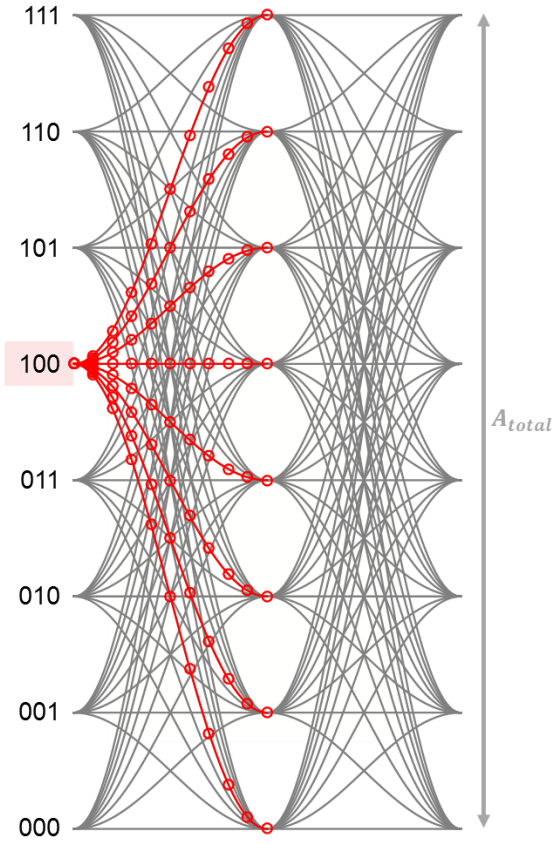
$$\frac{1}{16}\left(\frac{2}{3}A_{total}+\frac{1}{3}A_{total}+0+\frac{1}{3}A_{total}\right)$$

$$+$$

$$\frac{1}{16}\left(\frac{3}{3}A_{total}+\frac{2}{3}A_{total}+\frac{1}{3}A_{total}+0\right)$$

- $$E(SD)=\sum_{n=0}^{3}\sum_{m=0}^{3}p_{n,m}\cdot SD(S_n,S_m)=\frac{1}{16}\cdot\sum_{n=0}^{3}\sum_{m=0}^{3}SD(S_n,S_m)=\frac{5}{12}A_{total}$$

E(SD) of Binary-Scaled PAM-8

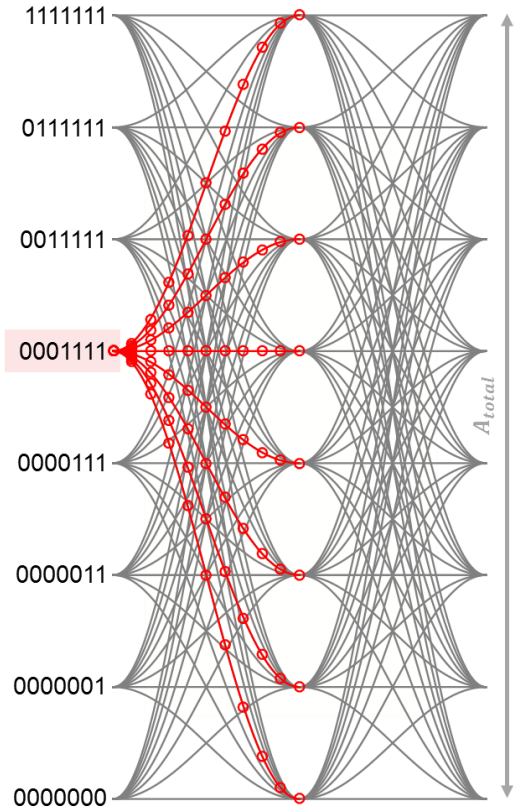


	111	110	101	100	011	010	001	000
111	0	$\frac{1}{7}$	$\frac{2}{7}$	$\frac{3}{7}$	$\frac{4}{7}$	$\frac{5}{7}$	$\frac{6}{7}$	$\frac{7}{7}$
110	$\frac{1}{7}$	0	$\frac{3}{7}$	$\frac{2}{7}$	$\frac{5}{7}$	$\frac{4}{7}$	$\frac{7}{7}$	$\frac{6}{7}$
101	$\frac{2}{7}$	$\frac{3}{7}$	0	$\frac{1}{7}$	$\frac{6}{7}$	$\frac{7}{7}$	$\frac{4}{7}$	$\frac{5}{7}$
100	$\frac{3}{7}$	$\frac{2}{7}$	$\frac{1}{7}$	0	$\frac{7}{7}$	$\frac{6}{7}$	$\frac{5}{7}$	$\frac{4}{7}$
011	$\frac{4}{7}$	$\frac{5}{7}$	$\frac{6}{7}$	$\frac{7}{7}$	0	$\frac{1}{7}$	$\frac{2}{7}$	$\frac{3}{7}$
010	$\frac{5}{7}$	$\frac{4}{7}$	$\frac{7}{7}$	$\frac{6}{7}$	$\frac{1}{7}$	0	$\frac{3}{7}$	$\frac{2}{7}$
001	$\frac{6}{7}$	$\frac{7}{7}$	$\frac{4}{7}$	$\frac{5}{7}$	$\frac{2}{7}$	$\frac{3}{7}$	0	$\frac{1}{7}$
000	$\frac{7}{7}$	$\frac{6}{7}$	$\frac{5}{7}$	$\frac{4}{7}$	$\frac{3}{7}$	$\frac{2}{7}$	$\frac{1}{7}$	0

$$SD = \sum_{n=0}^{7}\sum_{m=0}^{7} p_{n,m} \cdot SD(S_n, S_m) = \frac{1}{64}\sum_{n=0}^{7}\sum_{m=0}^{7} \frac{m}{7} A_{total} = \frac{1}{2} A_{total}$$

- 3-bit binary weighted
  - $V_{PAM-8} = 4V_{B2} + 2V_{B1} + V_{B0}$

E(SD) of Thermometer-Coded PAM-8



	1111111	0111111	0011111	0001111	0000111	0000011	0000001	0000000
1111111	0	$\frac{1}{7}$	$\frac{2}{7}$	$\frac{3}{7}$	$\frac{4}{7}$	$\frac{5}{7}$	$\frac{6}{7}$	$\frac{7}{7}$
0111111	$\frac{1}{7}$	0	$\frac{1}{7}$	$\frac{2}{7}$	$\frac{3}{7}$	$\frac{4}{7}$	$\frac{5}{7}$	$\frac{6}{7}$
0011111	$\frac{1}{7}$	$\frac{2}{7}$	0	$\frac{1}{7}$	$\frac{2}{7}$	$\frac{3}{7}$	$\frac{4}{7}$	$\frac{5}{7}$
0001111	$\frac{1}{7}$	$\frac{2}{7}$	$\frac{3}{7}$	0	$\frac{1}{7}$	$\frac{2}{7}$	$\frac{3}{7}$	$\frac{4}{7}$
0000111	$\frac{1}{7}$	$\frac{2}{7}$	$\frac{3}{7}$	$\frac{4}{7}$	0	$\frac{1}{7}$	$\frac{2}{7}$	$\frac{3}{7}$
0000011	$\frac{1}{7}$	$\frac{2}{7}$	$\frac{3}{7}$	$\frac{4}{7}$	$\frac{5}{7}$	0	$\frac{1}{7}$	$\frac{2}{7}$
0000001	$\frac{1}{7}$	$\frac{2}{7}$	$\frac{3}{7}$	$\frac{4}{7}$	$\frac{5}{7}$	$\frac{6}{7}$	0	$\frac{1}{7}$
0000000	$\frac{1}{7}$	$\frac{2}{7}$	$\frac{3}{7}$	$\frac{4}{7}$	$\frac{5}{7}$	$\frac{6}{7}$	$\frac{7}{7}$	0

$$SD = \sum_{n=0}^{7}\sum_{m=0}^{7} p_{n,m} \cdot SD(S_n, S_m) = \frac{1}{64}\sum_{k=0}^{7}\left(\sum_{x=0}^{k}\frac{x}{7}A_{total} + \sum_{y=k}^{7}\frac{y-k}{7}A_{total}\right) = \frac{3}{8}A_{total}$$

- 7 data eyes → 7-bit thermometer code

$$-V_{PAM-8} = V_{D6} + V_{D5} + V_{D4} + V_{D3} + V_{D2} + V_{D1} + V_{D0}$$

E(SD) Calculation Summary

	PAM-4		PAM-8		PAM-16	
Topology	**BS***	**TC#**	**BS**	**TC**	**BS**	**TC**
Baud rate (GB)	10	10	10	10	10	10
Data rate (Gbps)	20	20	30	30	40	40
Double Nyquist frequency (GHz)	10	10	10	10	10	10
Total Signal Amplitude	A_{total}	A_{total}	A_{total}	A_{total}	A_{total}	A_{total}
Average SD	$\frac{1}{2}A_{total}$	$\frac{5}{12}A_{total}$	$\frac{1}{2}A_{total}$	$\frac{3}{8}A_{total}$	$\frac{1}{2}A_{total}$	$\frac{17}{48}A_{total}$
Normalized CM Noise	1	0.83	1	0.75	1	0.71

* BS stands for binary-scaled

TC stands for thermometer-coded

- With same symbol rate (same T_s)
  - BS PAM-4/8/16 have same *E(SD)* and same CM noise
  - TC PAM-4/8/16 have intrinsically smaller CM noise

Upgraded CM Noise Equation

$$N(2f_{Nyquist}) = \frac{1}{8}\beta_S \cdot Amp\frac{\left|t_{rise} - t_{fall}\right|}{T_s} \cdot \sin c^2(\frac{\pi}{2} \cdot \frac{T_{tr}}{T_s})$$

- Introducing system-architecture coefficient (SAC),

$$\beta_S = \frac{SD^T_{PAM-2^k}}{SD^B_{PAM-2^k}} = \frac{\frac{1}{2^{2k}}\sum_{n=0}^{2^k-1}(\sum_{x=0}^{n}\frac{x}{2^k-1} + \sum_{y=n}^{2^k-1}\frac{y-n}{2^k-1})A_{total}}{\frac{1}{2}A_{total}}$$

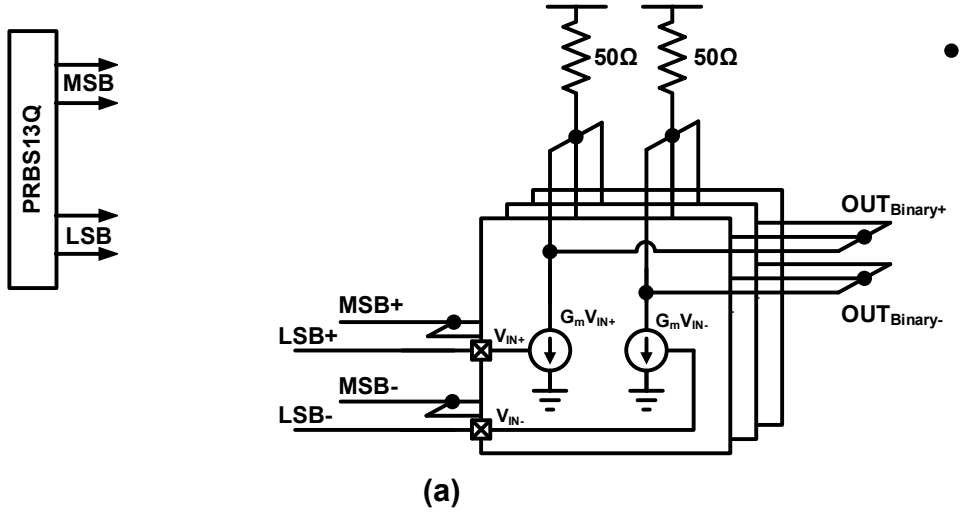
  - Normalized CM noise to the CM noise in binary-scaled systems

β_S	PAM-4	PAM-8	PAM-16
Binary-scaled	1	1	1
Thermometer-coded	0.83	0.75	0.71

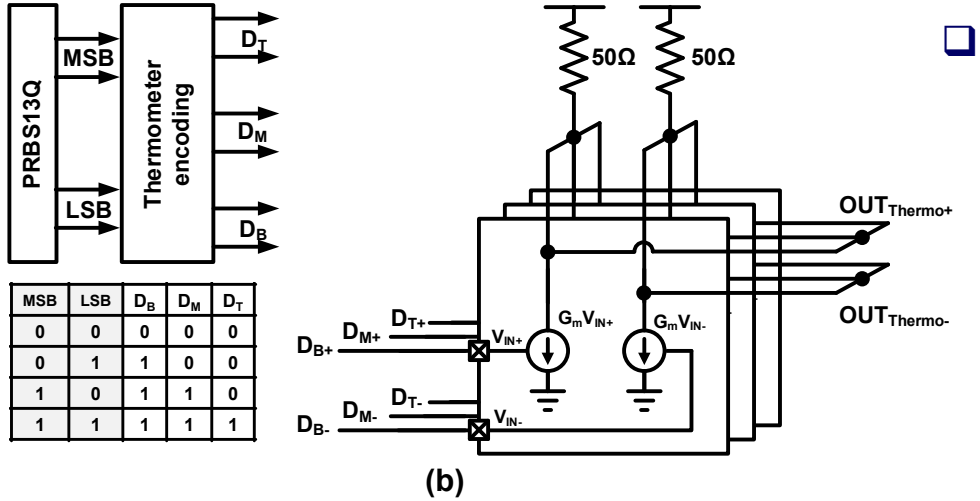
Behavior- and transistor-level simulation results

PAM-4 and PAM-8 CML Drivers

PAM-4 Behavior-Level Simulations



- Binary-scaled PAM-4
  - 3 identical slices
  - 2 for MSB, 1 for LSB
  - $V_o = G_m R_o (2V_{MSB} + V_{LSB})$

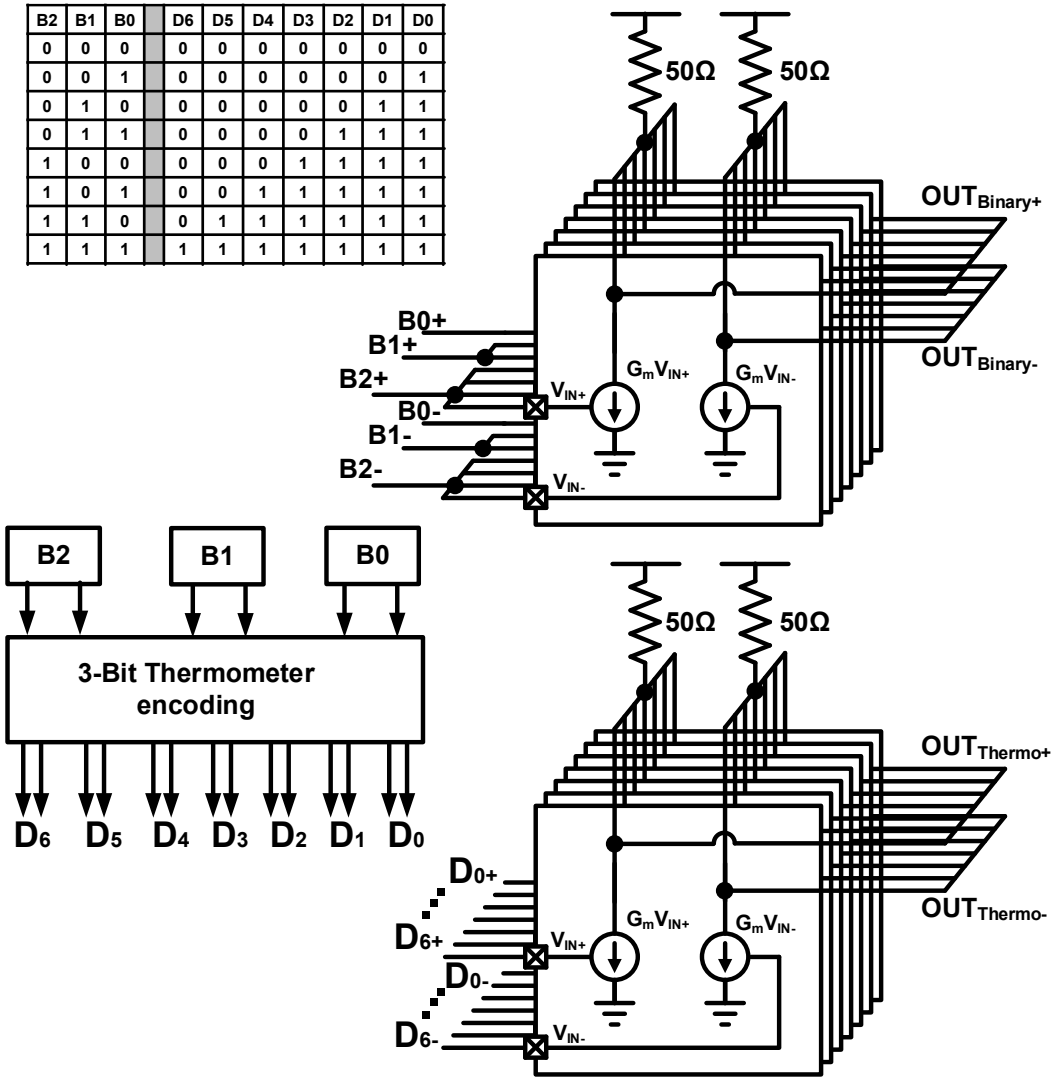


MSB	LSB	D_B	D_M	D_T
0	0	0	0	0
0	1	1	0	0
1	0	1	1	0
1	1	1	1	1

- **Thermometer-coded PAM-4**
  - **3 identical slices**
  - **1 for D_T, 1 for D_M, and 1 for D_B**
  - $V_o = G_m R_o (V_{DT} + V_{DM} + V_{DB})$

PAM-8 Behavior-Level Simulations

B2	B1	B0		D6	D5	D4	D3	D2	D1	D0
0	0	0		0	0	0	0	0	0	0
0	0	1		0	0	0	0	0	0	1
0	1	0		0	0	0	0	0	1	1
0	1	1		0	0	0	0	1	1	1
1	0	0		0	0	0	1	1	1	1
1	0	1		0	0	1	1	1	1	1
1	1	0		0	1	1	1	1	1	1
1	1	1		1	1	1	1	1	1	1



- Binary-scaled PAM-8
  - 7 identical slices
  - 4 for B2, 2 for B1, and 1 for B0
  - $V_o = G_m R_o(4V_{B2} + 2V_{B1} + V_{B0})$

❑ **Thermometer-coded PAM-8**

- **7 identical slices**
- **Evenly distributed**
- $V_o = G_m R_o(V_{D6} + V_{D5} + \cdots V_{D0})$

Summary of Simulation Results

	PAM-4		PAM-8	
Topology	**BS***	**TC#**	**BS**	**TC**
Baud rate (GB)	10	10	10	10
Data rate (Gbps)	20	20	30	30
Double Nyquist frequency (GHz)	10	10	10	10
Simulation time (nS)	800	800	800	800
Total amplitude (mV)	252	252	252	252
Rising/falling edge (ps)	11/10	11/10	11/10	11/10
Simulated CM noise @ 20GHz (mV)	2.41	1.99	2.41	1.81
Normalized CM noise	1	0.826	1	0.751

* BS stands for binary-scaled

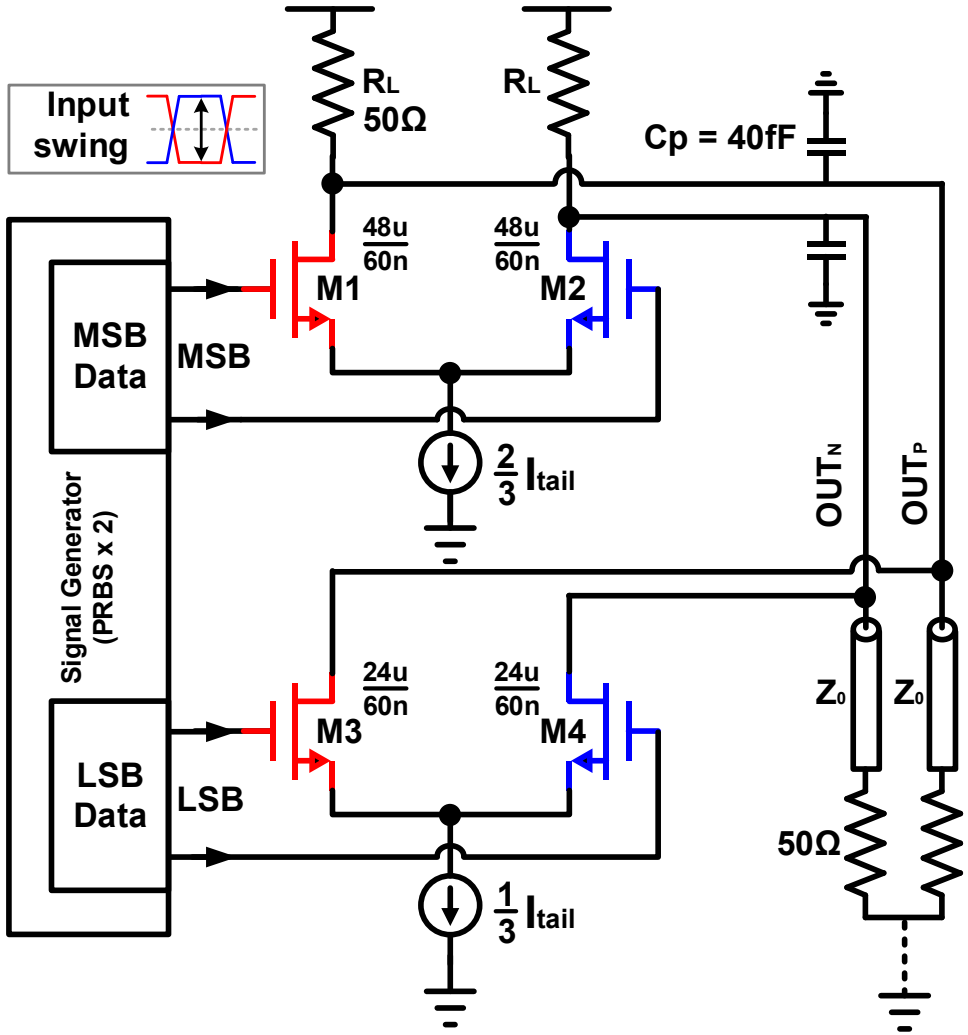
TC stands for thermometer-coded

β_S	PAM-4	PAM-8	PAM-16
Binary-scaled	**1**	**1**	**1**
Thermometer-coded	**0.83**	**0.75**	**0.71**

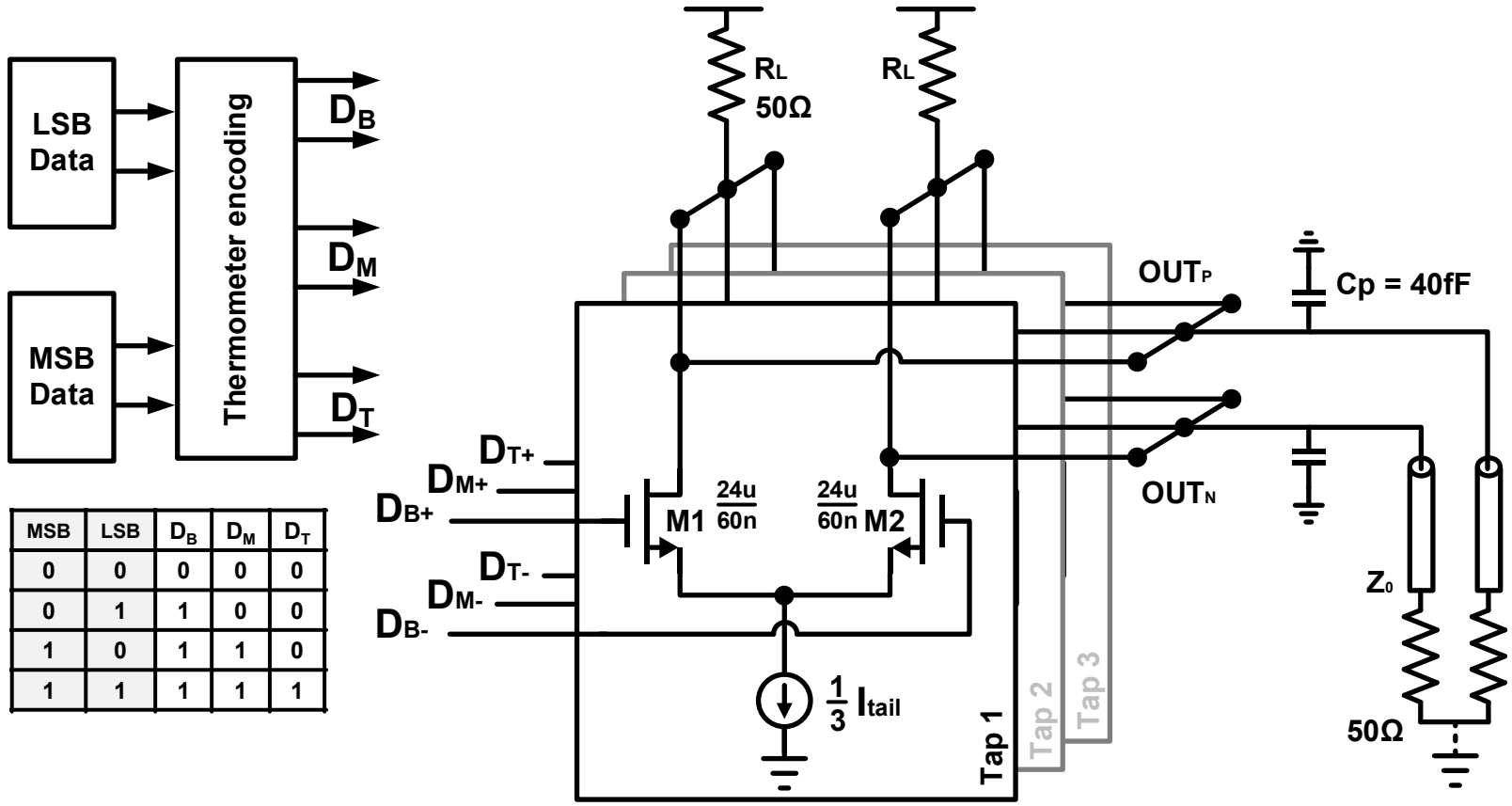
- Consistent with the previous calculations
  - Error is caused by the pseudo-randomness of PRBS13Q

BS PAM-4 Circuit Simulation Setup

- Verilog-A signal generator
  - Ideal non-distorted input MSB and LSB signals
- CML core circuit
  - 65nm CMOS process
- Output transmission line
  - S-parameter 2-port blocks
- Current ratio
  - MSB:LSB = 2:1



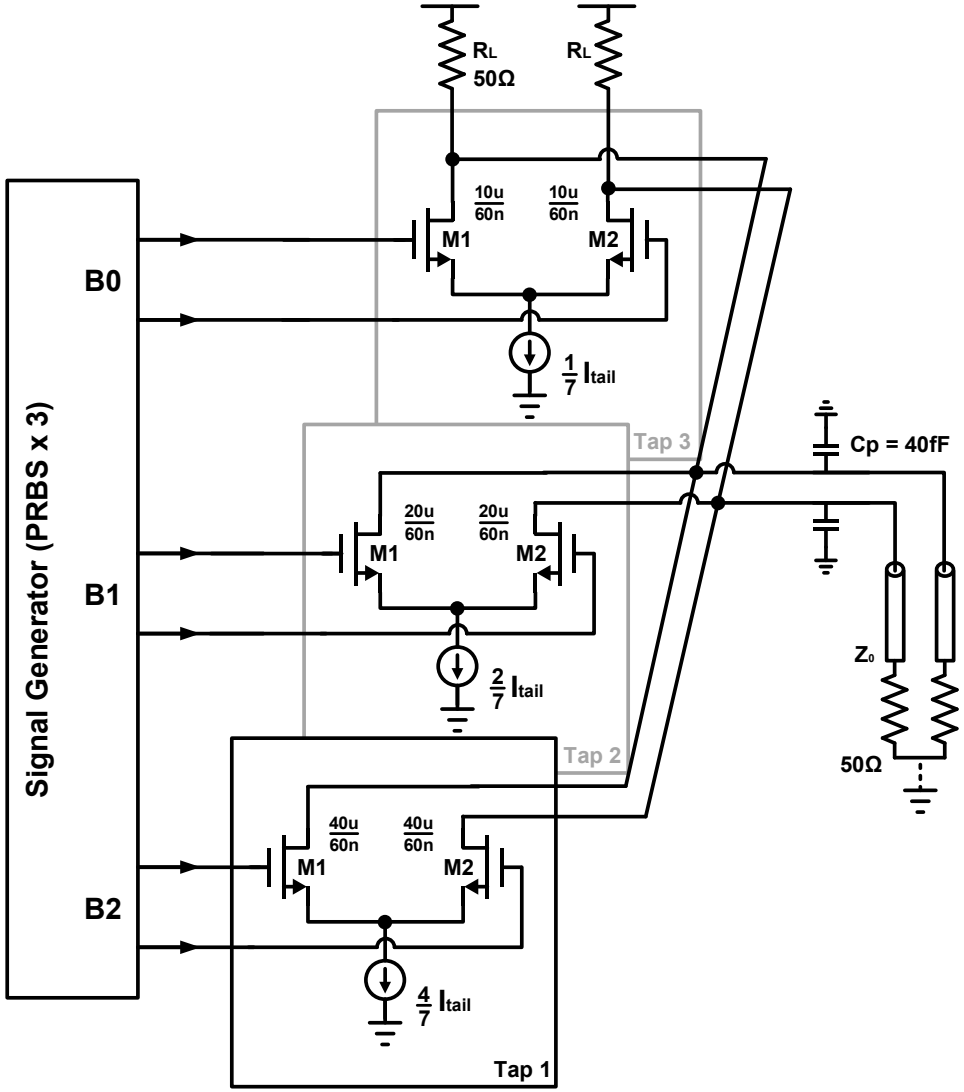
TC PAM-4 Circuit Simulation Setup

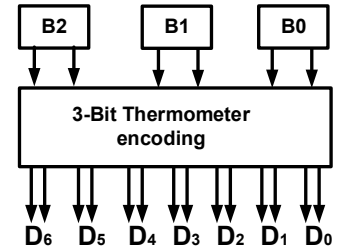


MSB	LSB	D_B	D_M	D_T
0	0	0	0	0
0	1	1	0	0
1	0	1	1	0
1	1	1	1	1

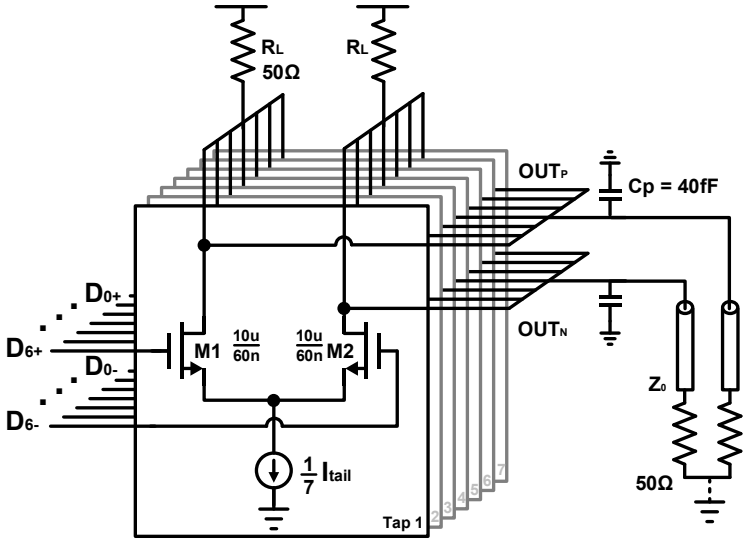
- Ideal input thermometer-code signals
- Current ratio, 1:1:1

BS & TC PAM-8 Circuit Simulation Setups





B2	B1	B0	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	1	1
0	1	1	0	0	0	0	1	1	1
1	0	0	0	0	0	1	1	1	1
1	0	1	0	0	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1



Transistor-Level Simulation Results

	PAM-4 BS*			PAM-4 TC#			PAM-8 BS			PAM-8 TC		
Baud rate (GB)	10			10			10			10		
Data rate (Gbps)	20			20			30			30		
Double Nyquist frequency	10 GHz			10 GHz			10 GHz			10 GHz		
Transistor sizing	48u+24u			24u x 3			40u+20u+10u			10u x 7		
Process corner	FF	TT	SS	FF	TT	SS	FF	TT	SS	FF	TT	SS
DC current (mA)	18.5	17.7	16.8	18.5	17.7	16.8	18.5	17.7	16.8	18.5	17.7	16.8
Input swing (V)	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2
Input biasing voltage (V)	0.85	0.85	0.85	0.85	0.85	0.85	0.85	0.85	0.85	0.85	0.85	0.85
Output swing (mV)	214.9	234.7	253.7	214.8	234.7	253.6	212.1	231.7	250.7	212.1	231.7	250.7
CM Noise @ 10GHz (mV)	1.34	1.86	3.01	0.92	1.39	2.13	1.41	1.93	3.04	0.96	1.32	2.11

- **Comparison results**
  - Same process corner, symbol rate, driver size, power, and signal swing
    - Binary-scaled drivers have same CM noise
    - Thermometer-coded systems drivers smaller CM noise
  - Consistent with prediction

Conclusions

$$N(2f_{Nyquist}) = \frac{1}{8}\beta_S \cdot Amp \frac{|t_{rise} - t_{fall}|}{T_s} \cdot \sin c^2(\frac{\pi}{2} \cdot \frac{T_{tr}}{T_s})$$

- Reduce EMI radiation of backplane links with a certain <u>data rate</u>
  - Limit amplitude and do not over drive the circuit $Amp \downarrow$
  - Optimize circuit biasing condition to balance rise and fall time $|t_{rise} - t_{fall}| \downarrow$
  - Use higher-order modulations to lower symbol rate $T_s \uparrow$
    - E.g., from NRZ to PAM-4, T_s is doubled
  - When designing PAM-4/8 systems, use thermometer-coded topology to reduce CM noise $\beta_S \downarrow$

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香港科技大學
THE HONG KONG UNIVERSITY OF SCIENCE AND TECHNOLOGY

HKUST OWL

Wireline and Optical Receiver
有线和光接收机

Prof. C. Patrick Yue 俞捷教授

芯动力人才计划®第 125 期国际名家讲堂

Outline

- Motivation
  - Electrical vs Optical Link
- RX Architecture
  - Wireline vs Optical Receiver
  - ADC-Based Receiver
- Circuit Implementations
  - PD Interface
  - Multi-peaking TIA
  - Modified Cherry-Hooper Amplifier
  - FFE and DFE Implementation
- Practical Issue
  - On-Chip LDO for Improved Sensitivity
- Conclusion

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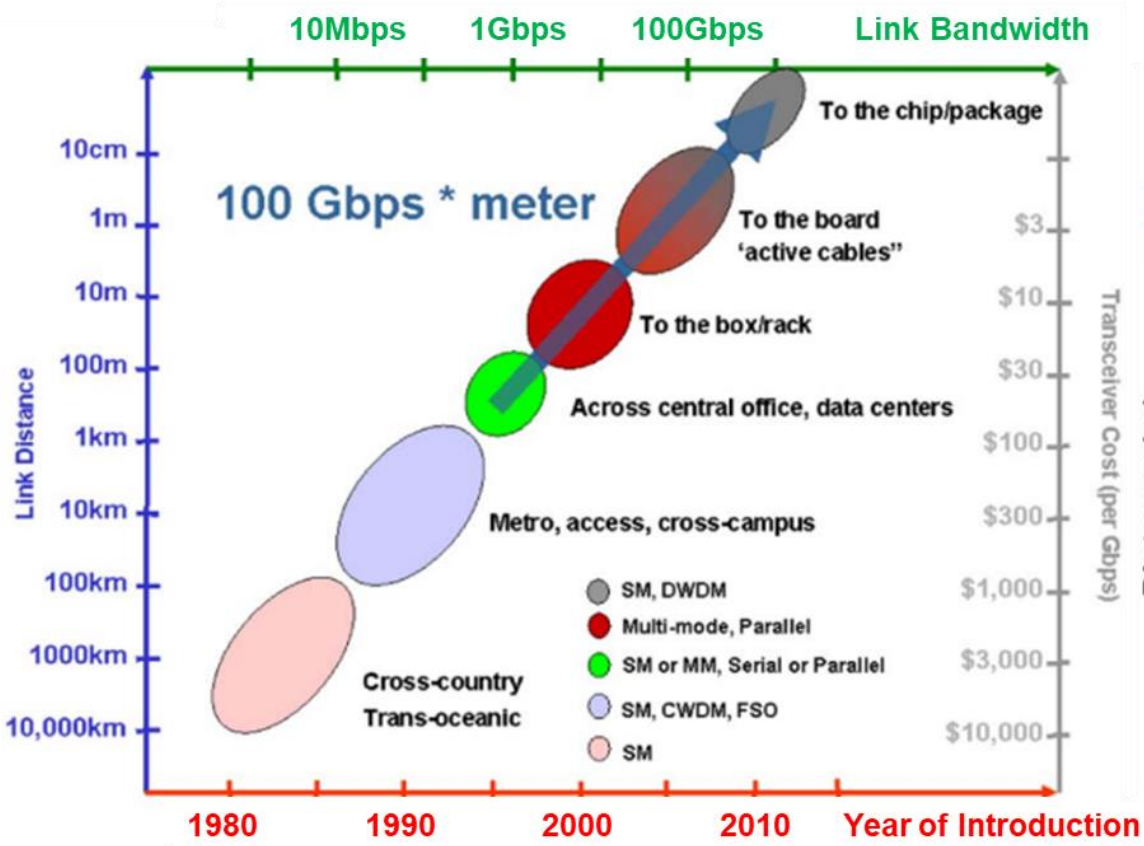
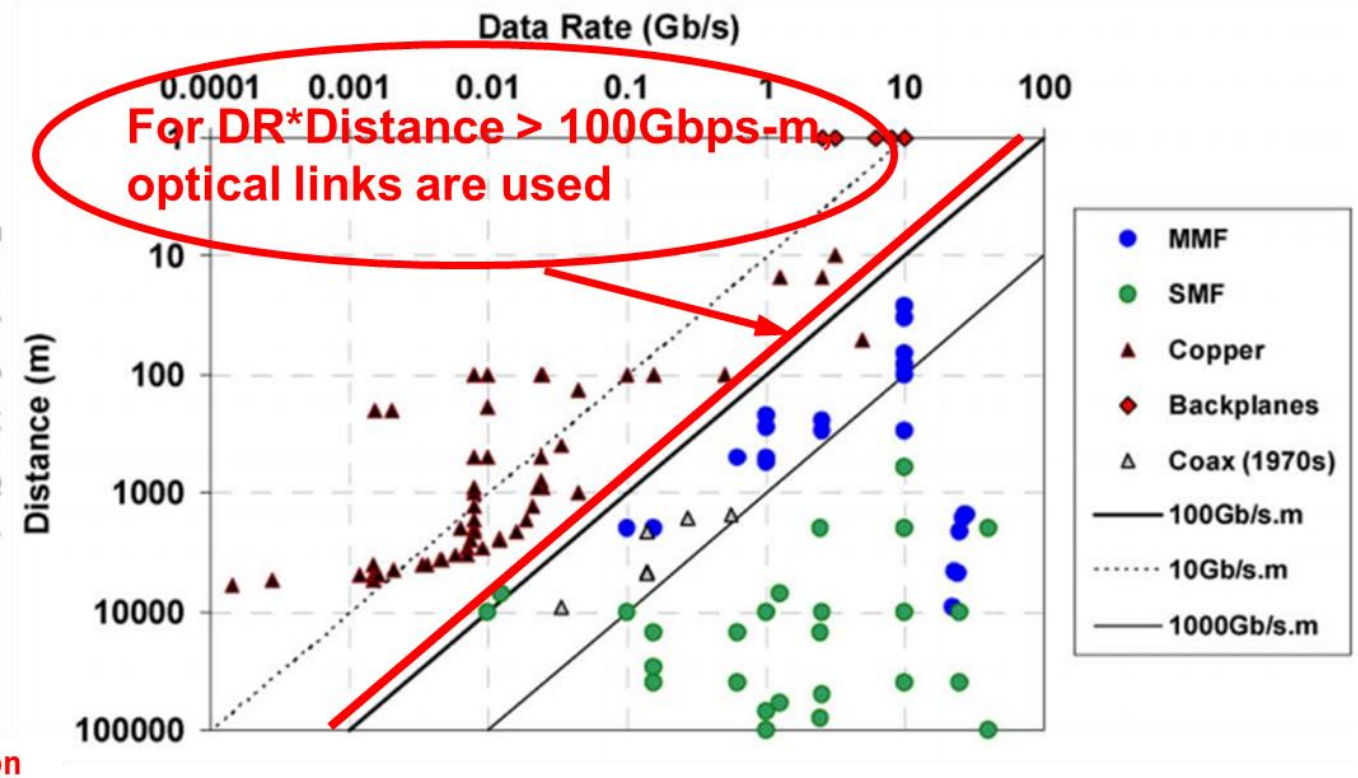
Electrical vs Optical Links



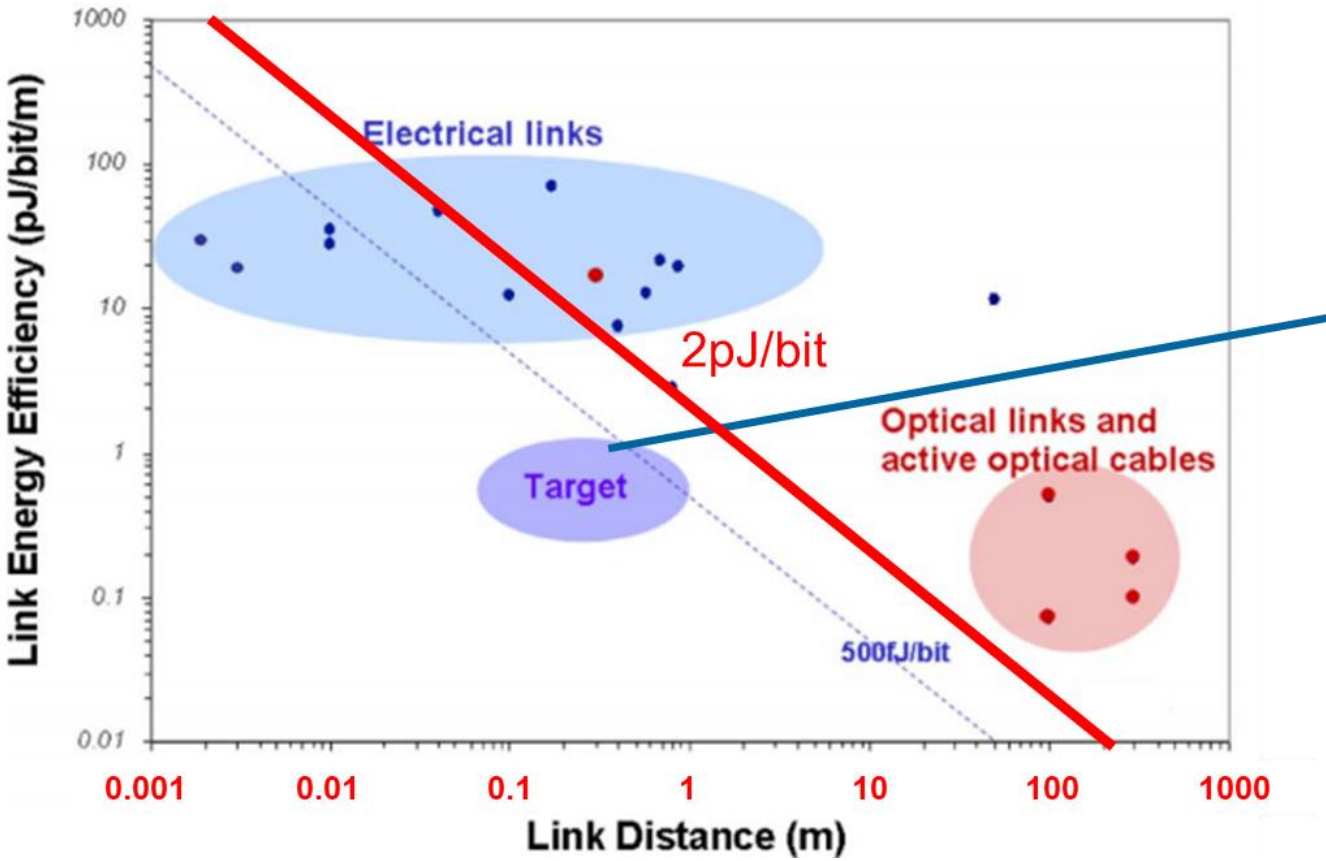
Penetration of optical links into communications.



- SMF: Single-Mode Fiber
- MMF: Multi-Mode Fiber

- Electrical links are bonded by the 100Gb/s-m bandwidth-distance product

Electrical vs Optical Links



Data center networks

- The potential exists to lower the energy of optical links to below a pJ/bit to the service link lengths ~1 m

Outline

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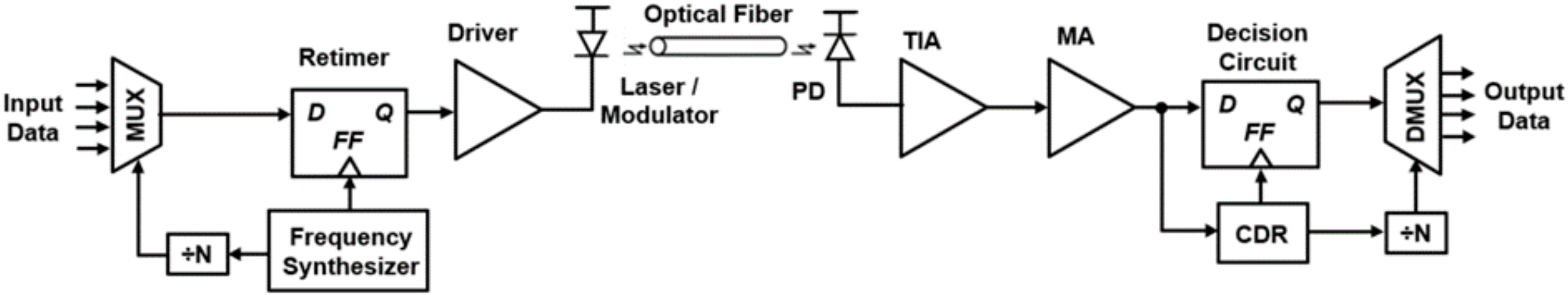
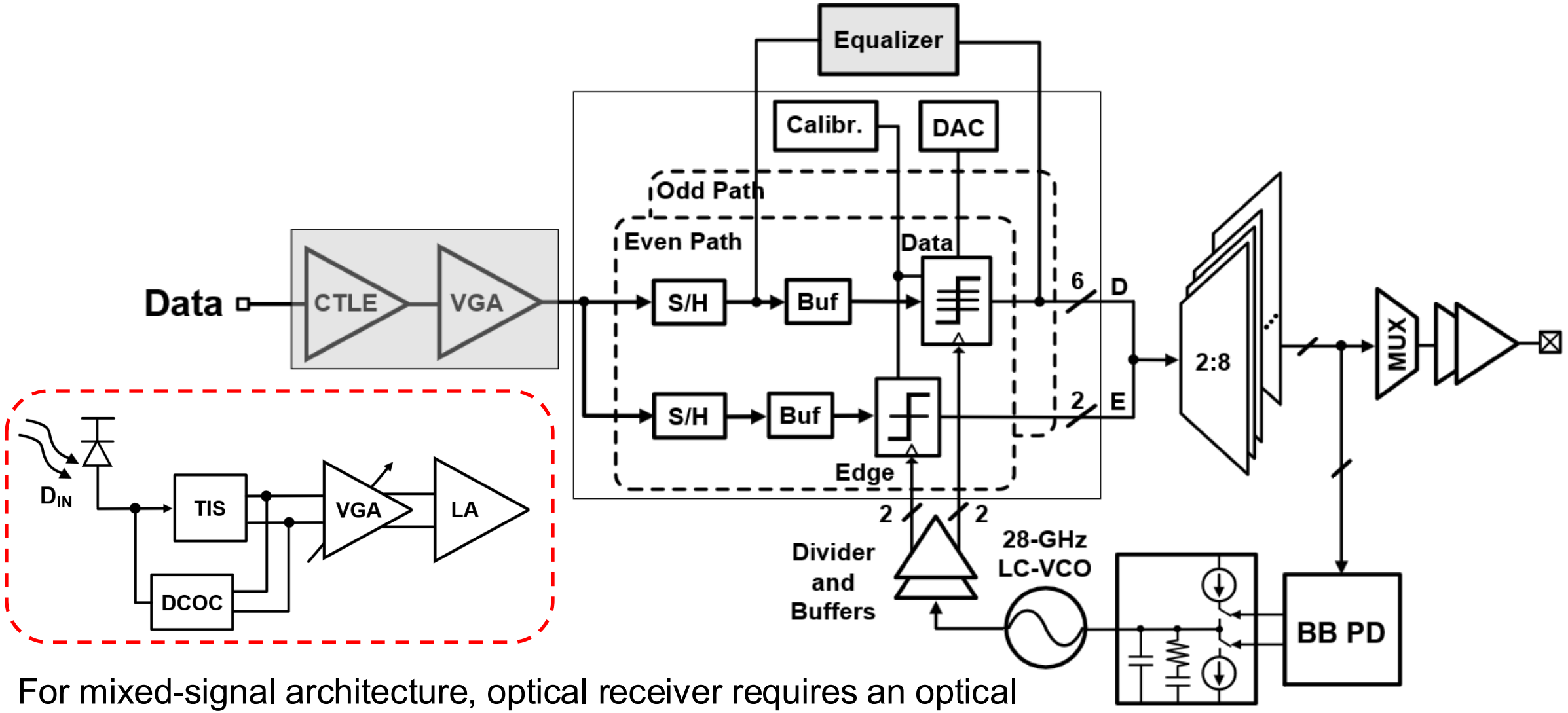
Intensity Modulation and Direct Detection Link



Typical system architecture of an intensity modulation and direct detection (IMDD) optical link

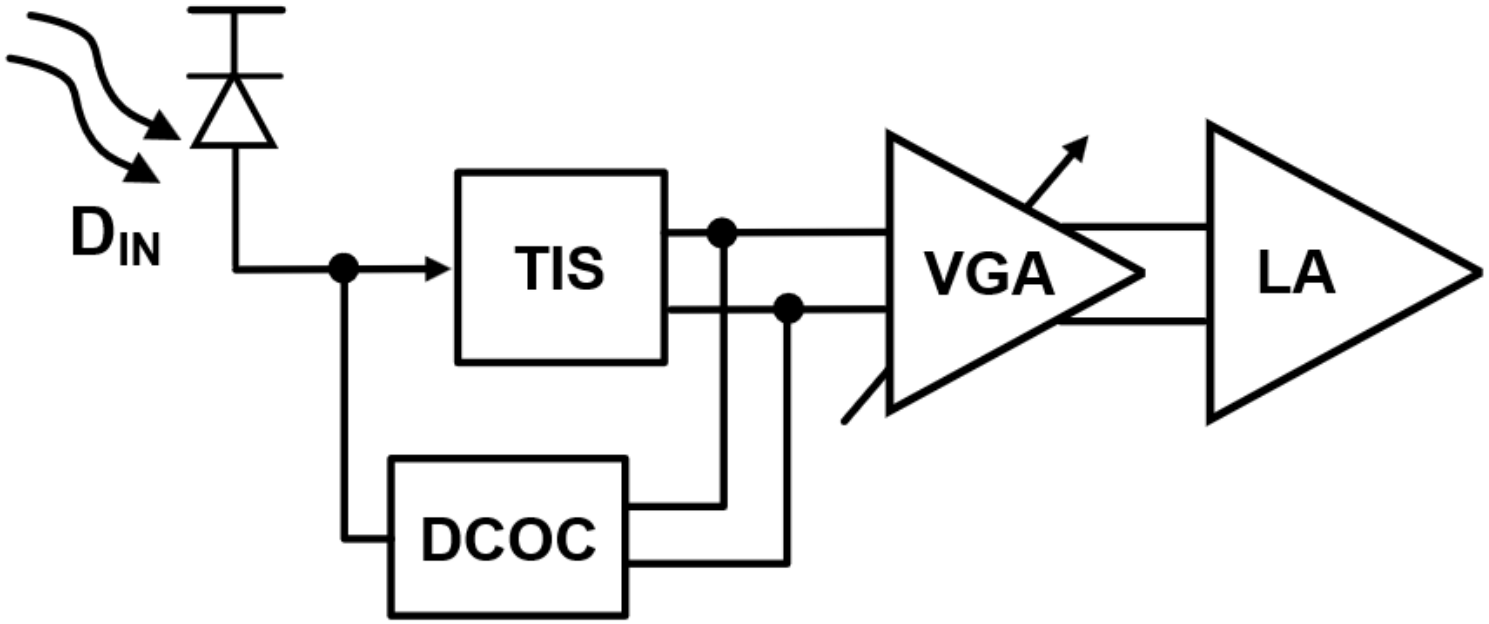
Distance/Optical Fiber	Modulation
100m MMF (400 GBASE-SR16)	25Gbaud NRZ, 16ch parallel
500m SMF (400 GBASE-PSM4)	1λ 50Gbaud PAM4
2km SMF (400 GBASE-FR8)	WDM 8λ WDM 25Gbaud PAM4

Comparison Between Wireline and Optical RX



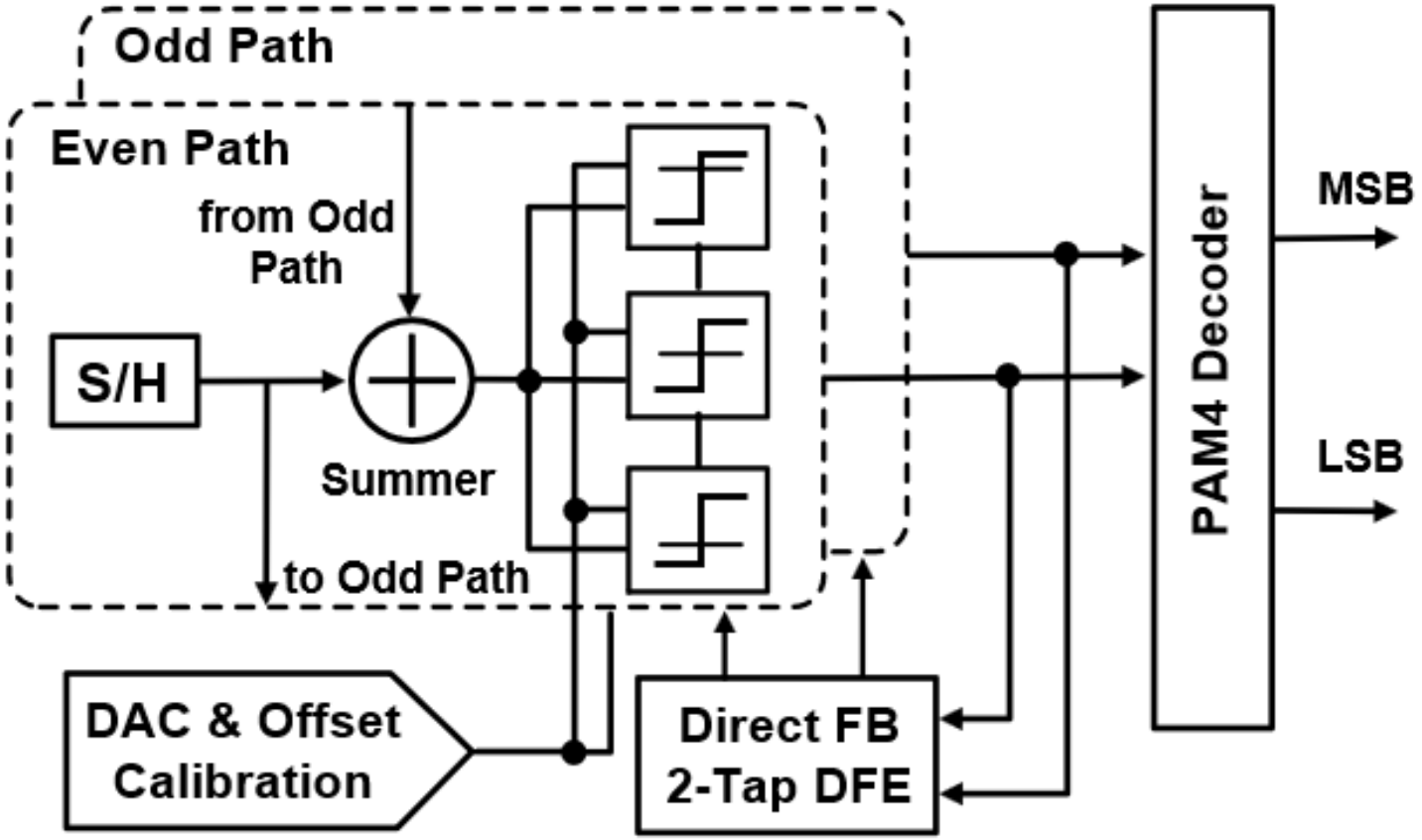
- For mixed-signal architecture, optical receiver requires an optical frontend to convert the input current from photodiode to voltage

Optical Frontend Architecture



- Optical frontend consists of a transimpedance amplifier (TIS), a variable amplifier (VGA), a limiting amplifier (LA), and a dc-offset cancellation (DCOC) block

Optical Frontend Architecture



- Half-rate structure
- 2-tap FFE
- 2-tap direct feedback DFE

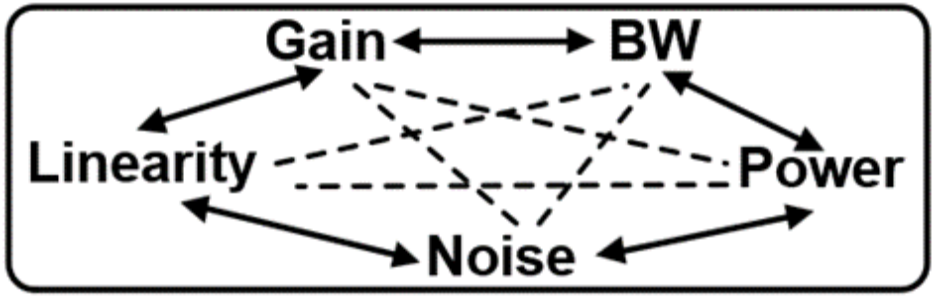
- Feedforward equalization and decision feedback equalization can be implemented to compensate for the ISI of TIA

Optical Receiver Design Tradeoffs

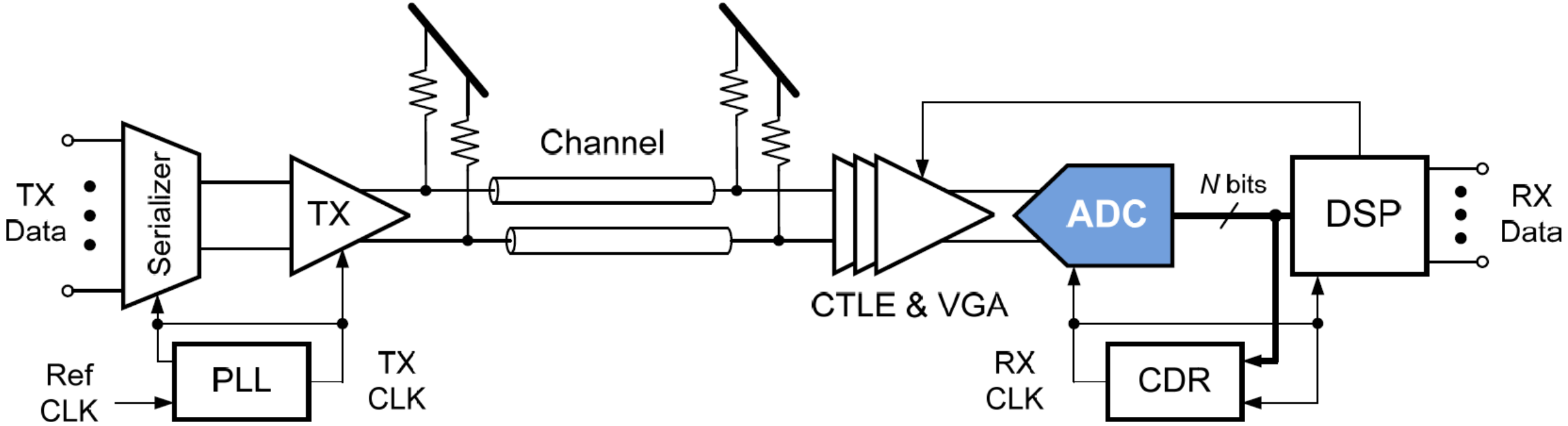
- Highly integrated optical communication system modules using silicon-based CMOS transceiver ICs with integrated AFE are highly desirable

- As the first stage of RX, the performance of TIA dictates the minimum input sensitivity and the maximum data rate of the entire RX

- TIA design tradeoff: by increasing the TIA gain, the noise can be reduced, and the sensitivity is improved, but the BW and data rate suffer



ADC-Based Receiver Front Ends

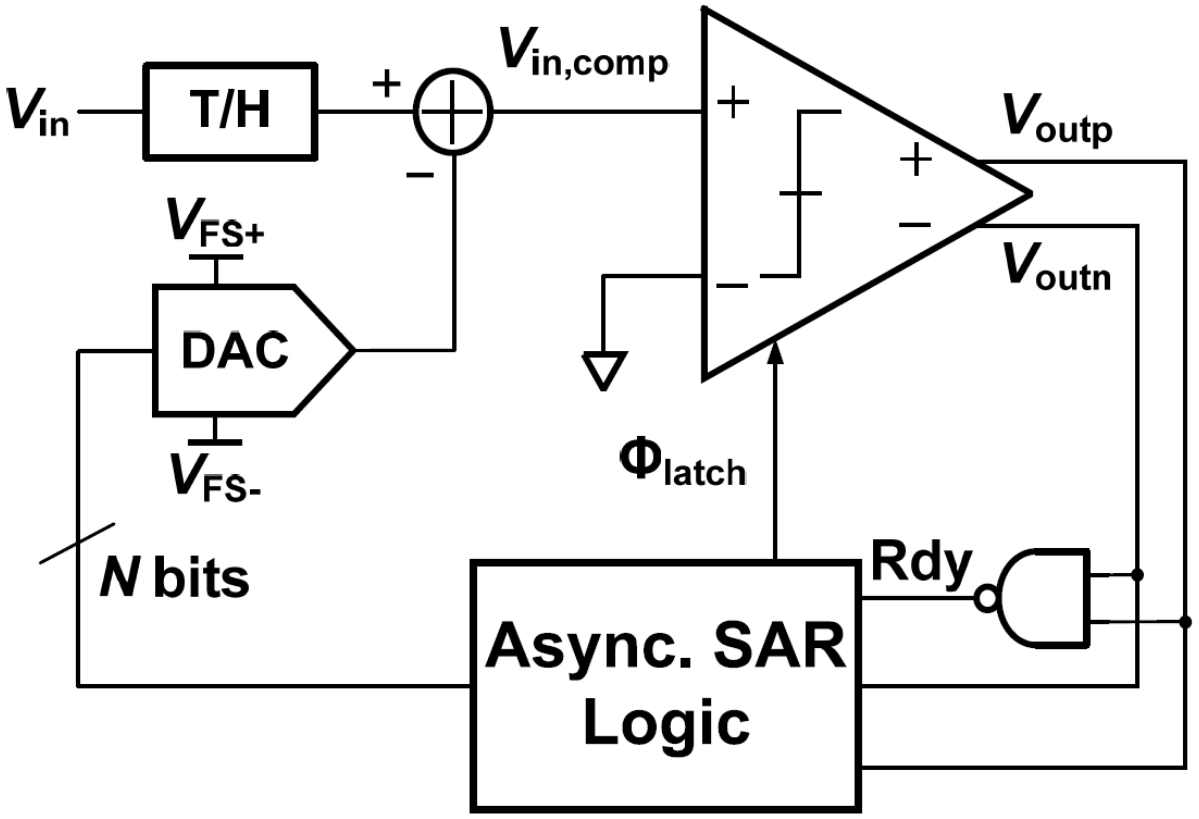


- ADC-based receivers perform ISI cancellation in digital domain, allowing for flexible advanced equalization and symbol detection
- Well-suited for more spectrally-efficient modulation schemes (PAM4)
- Benefit from improved area and power with CMOS scaling

Source: ISSCC 2018: ADC-Based Serial Links: Desig and Analysis, Samuel Palermo

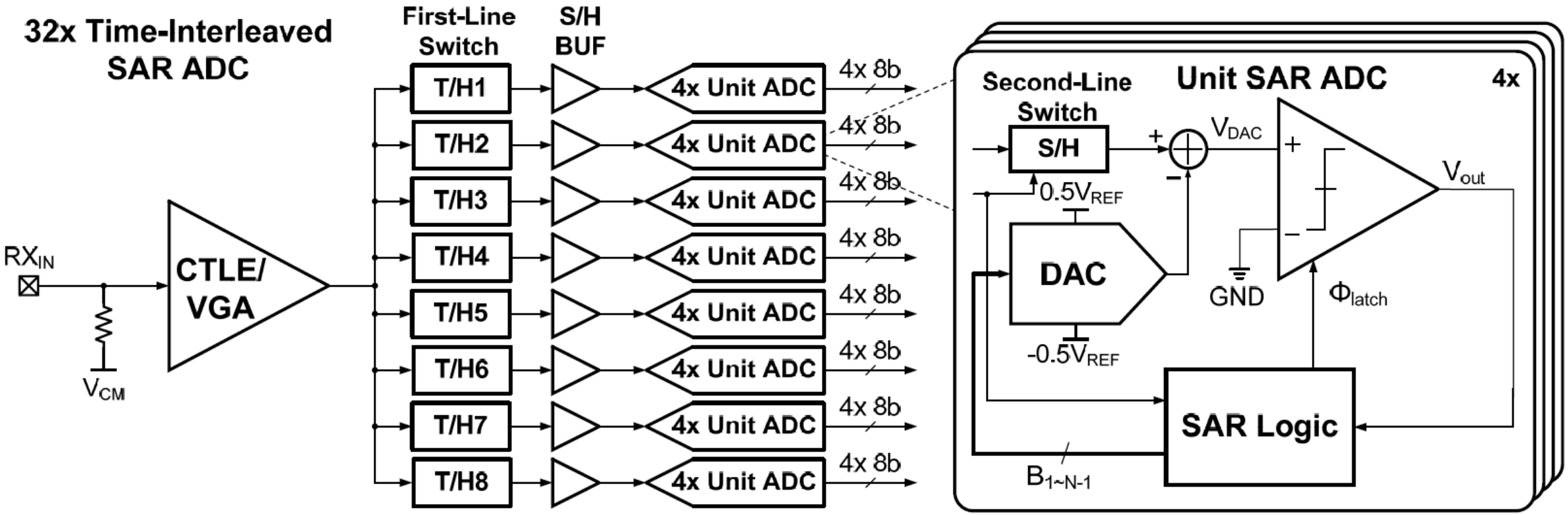
SAR ADC

- Performs a binary search conversion over multiple clock cycles
- Simplest implementations only require one comparator per unit ADC
- Slower unit ADC relative to flash/binary search
- Excellent choice for 6-8b resolution to support both PAM-2 and PAM-4
- The dominant architecture for PAM-4 ADC-based receivers



Source: ISSCC 2018: ADC-Based Serial Links: Desig and Analysis, Samuel Palermo

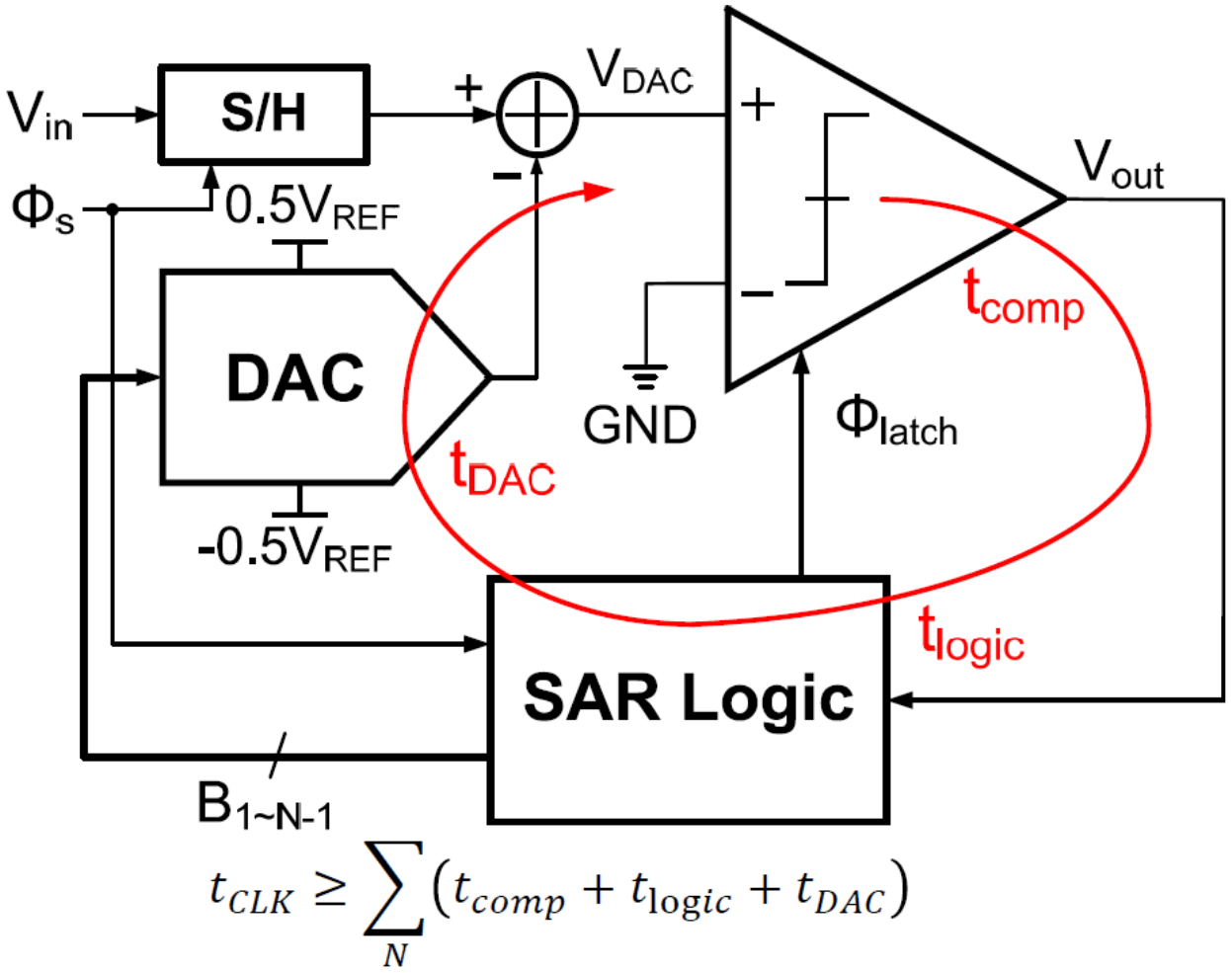
Time-Interleaved ADCs



- Wireline ADCs are time-interleaved to achieve high sample rates

Source: ISSCC 2018: ADC-Based Serial Links: Desig and Analysis, Samuel Palermo

Unit SAR ADC: Critical Timing Path



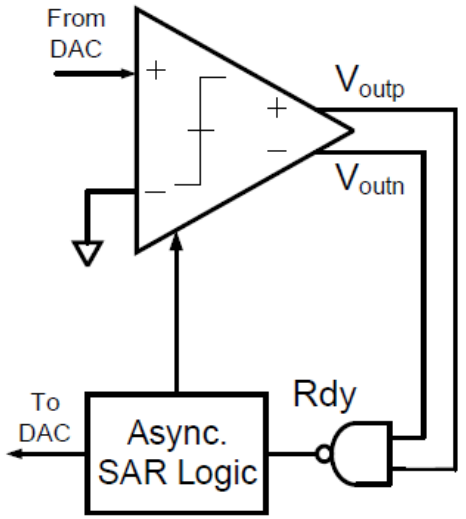
$$t_{CLK} \geq \sum_{N} \left(t_{comp} + t_{\log ic} + t_{DAC} \right)$$

- SAR ADC consists of S/H, DAC, comparator and SAR logic
- The conversion speed of SAR ADCs depends on the delay from comparator, logic and DAC in the critical timing path
- Various techniques to reduce the delay for faster SAR ADC speed

Source: ISSCC 2018: ADC-Based Serial Links: Desig and Analysis, Samuel Palermo

Unit SAR ADC: Advanced Techniques

- Asynchronous SAR operation

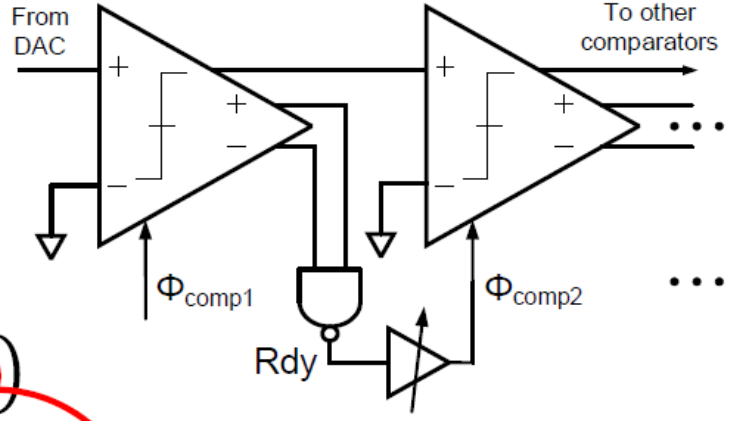


$$\sum_{i=0}^{N-1} \ln\left(\frac{V_{FS}}{V_{DAC}(i)}\right)$$

[S. Chen, JSSC'06]

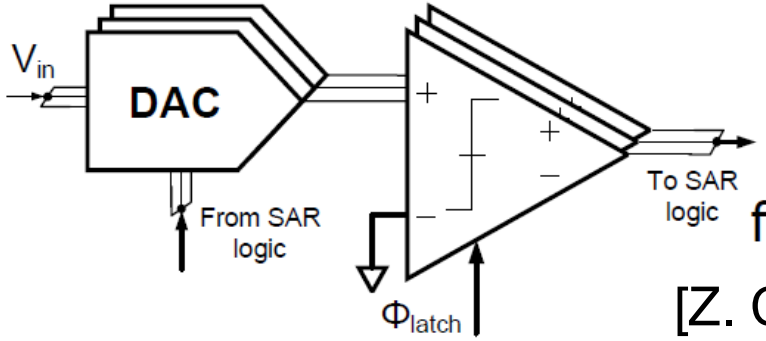
$$t_{CLK} \geq \sum_{N} \left(t_{comp} + t_{logic} + t_{DAC}\right)$$

- Loop-unrolled SAR



[T. Jiang, JSSC'12]

- Multi-bit/stage conversion

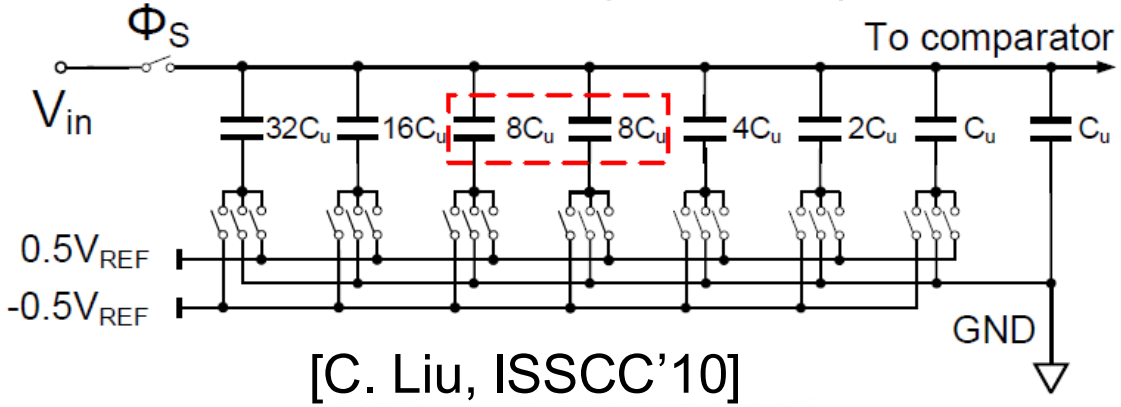


$$N' = \left\lceil \frac{N}{M} \right\rceil$$

for M-bit/stage

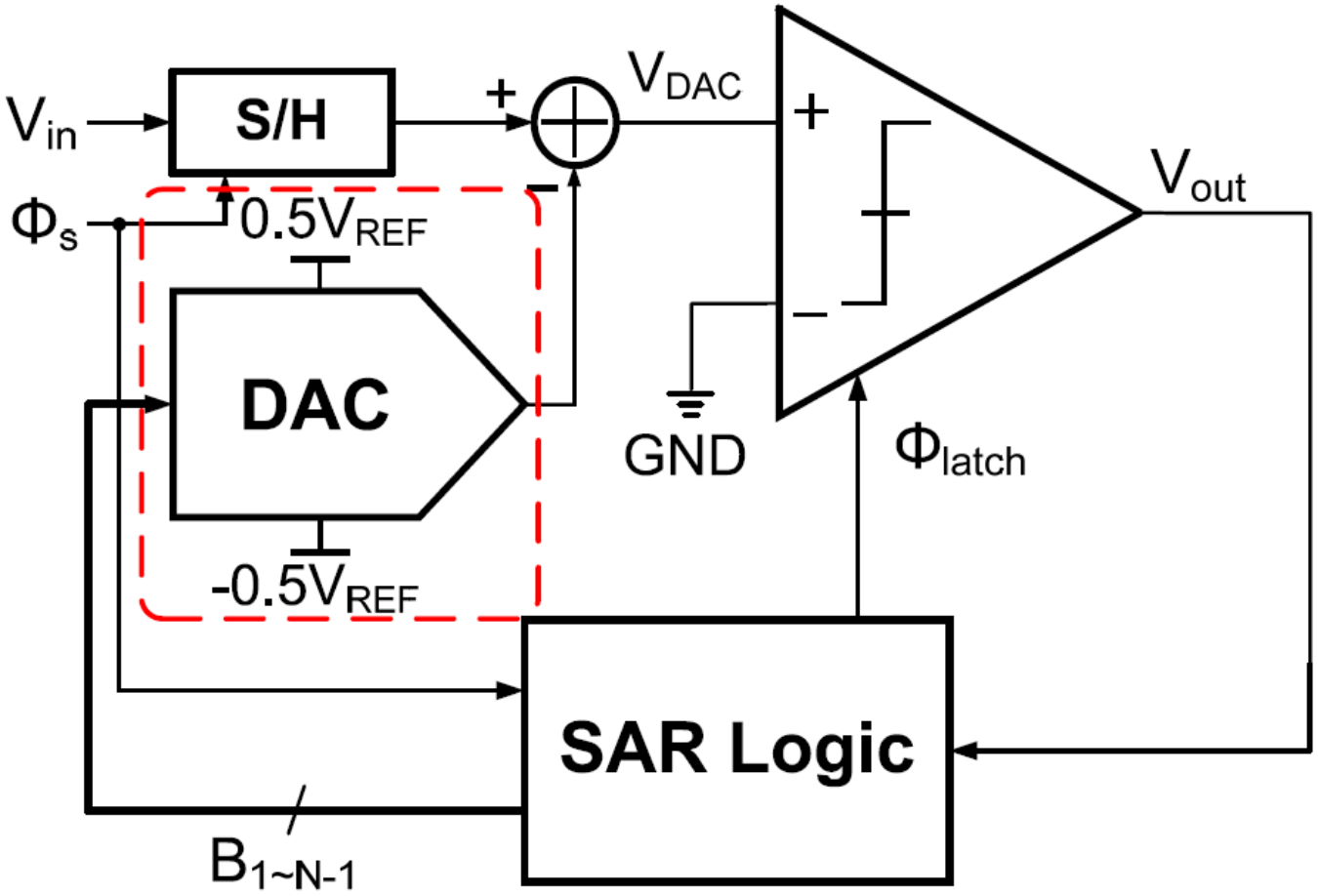
[Z. Cao, JSSC'09]

- Redundant SAR algorithm (trade-off N)



[C. Liu, ISSCC'10]

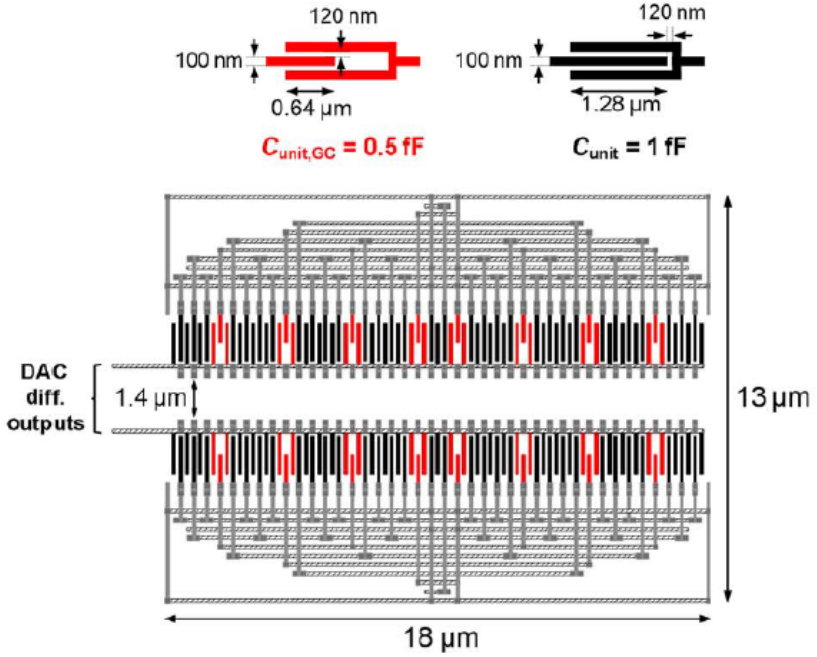
DAC

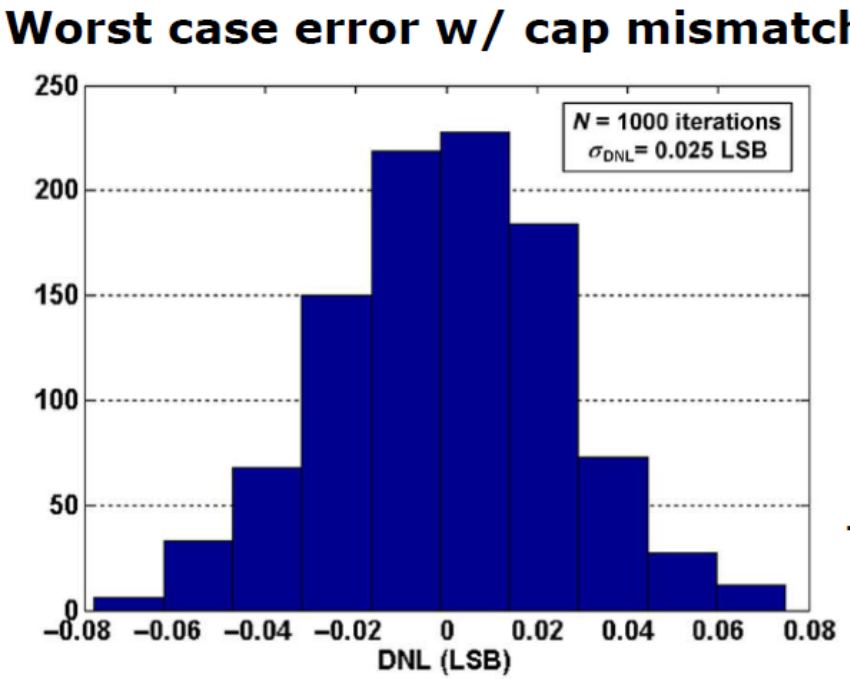


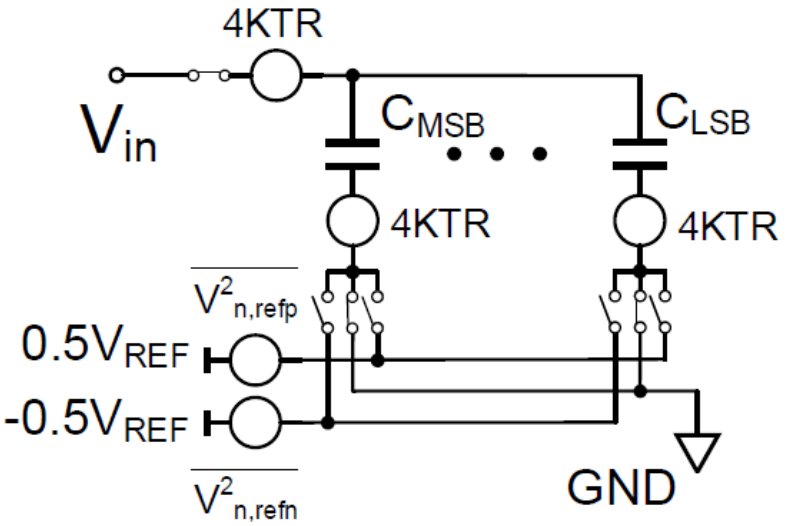
- DAC generates residue signals by subtracting binary weighted reference from input
- Capacitive DAC is the most popular DAC structure due to low power consumption

Source: ISSCC 2018: ADC-Based Serial Links: Desig and Analysis, Samuel Palermo

DAC Implementation



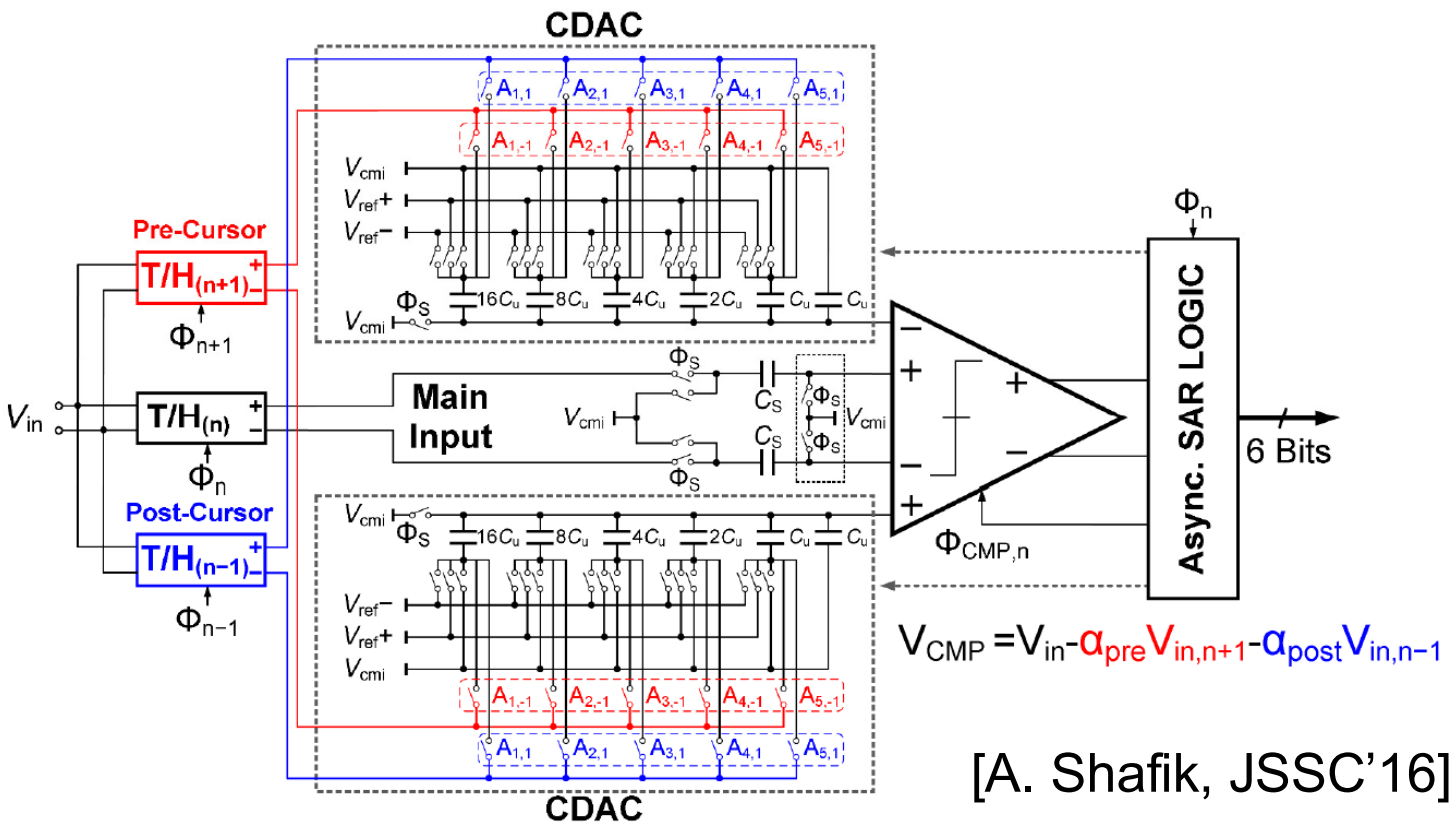




[A. Shafik, JSSC'16]

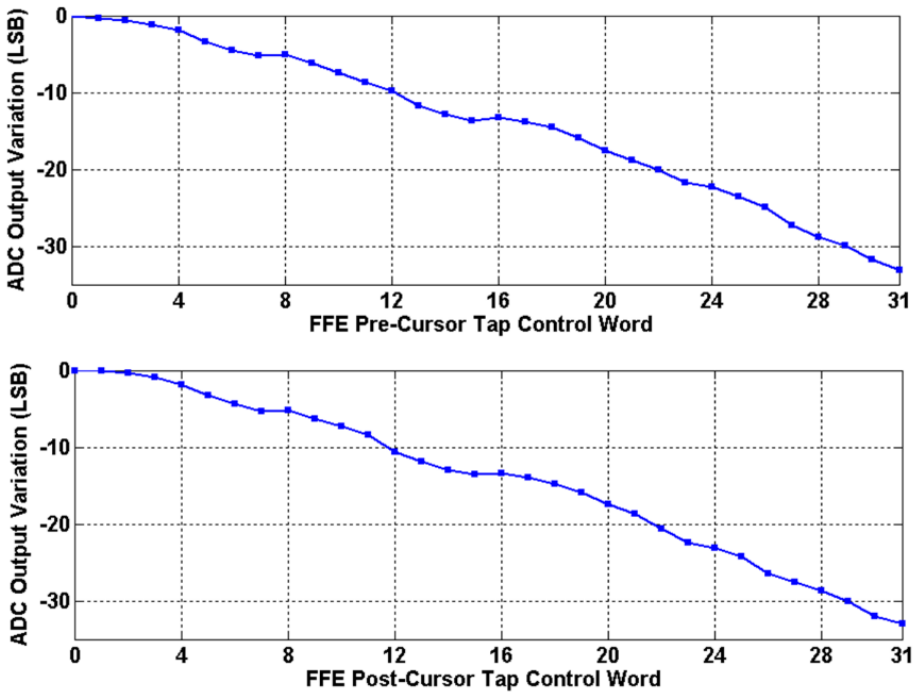
- Minimum unit cap size limited by matching requirement and KT/C noise (noise usually dominated by front-end and comparator)

Unit SAR ADC with Embedded FFE



$V_{CMP} = V_{in} - \alpha_{pre} V_{in,n+1} - \alpha_{post} V_{in,n-1}$

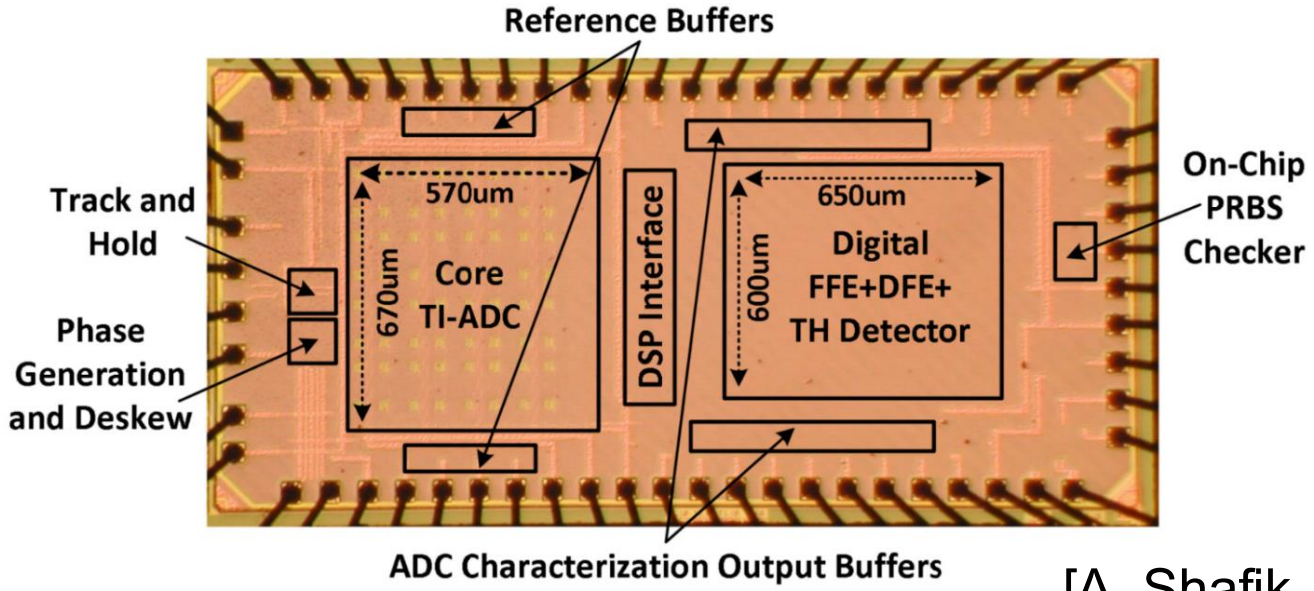
[A. Shafik, JSSC'16]



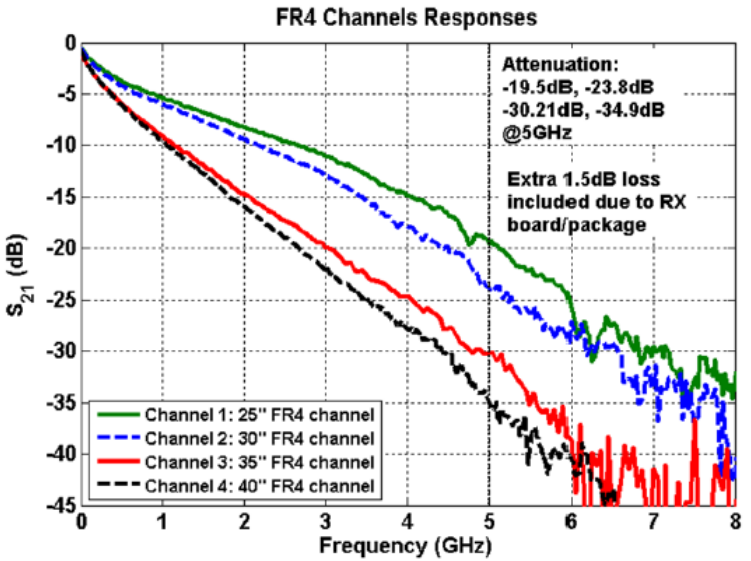
- 3-tap FFE efficiently embedded in the SAR CDAC
- Main trade-off is increased T/H loading (3X)

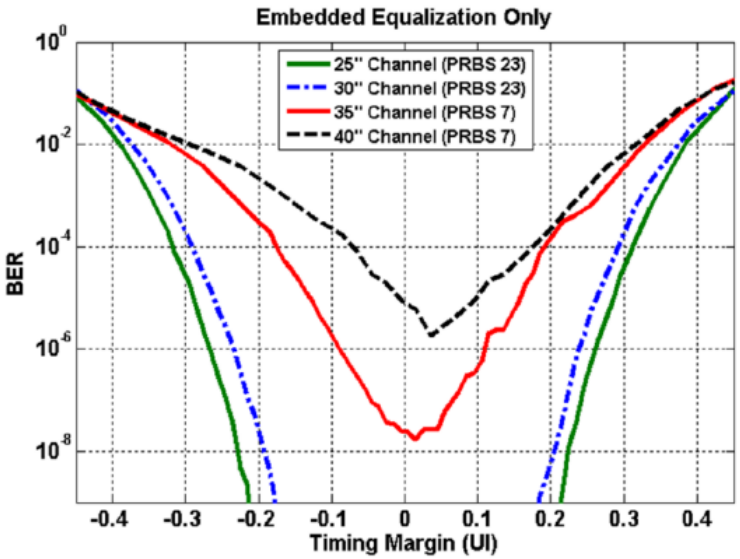
- Both pre- and post-cursor taps have ~33 LSB range and ~1.1 LSB resolution

10Gb/s NRZ ADC-Based RX Prototype in 65nm



[A. Shafik, JSSC'16]





- 10GS/s 32-way interleaved SAR ADC with embedded 3-tap FFE
- Embedded equalization alone is sufficient for the two lowest-loss (21, 25dB) channels
- Additional digital equalization is necessary for the two highest-loss (32, 36dB) channels

Outline

- Motivation
  - Electrical vs Optical Link
- RX Architecture
  - Wireline vs Optical Receiver
  - ADC-Based Receiver
- **Circuit Implementations**
  - **PD Interface**
  - **Multi-peaking TIA**
  - **Modified Cherry-Hooper Amplifier**
  - **FFE and DFE Implementation**
- Practical Issue
  - On-Chip LDO for Improved Sensitivity
- Conclusion

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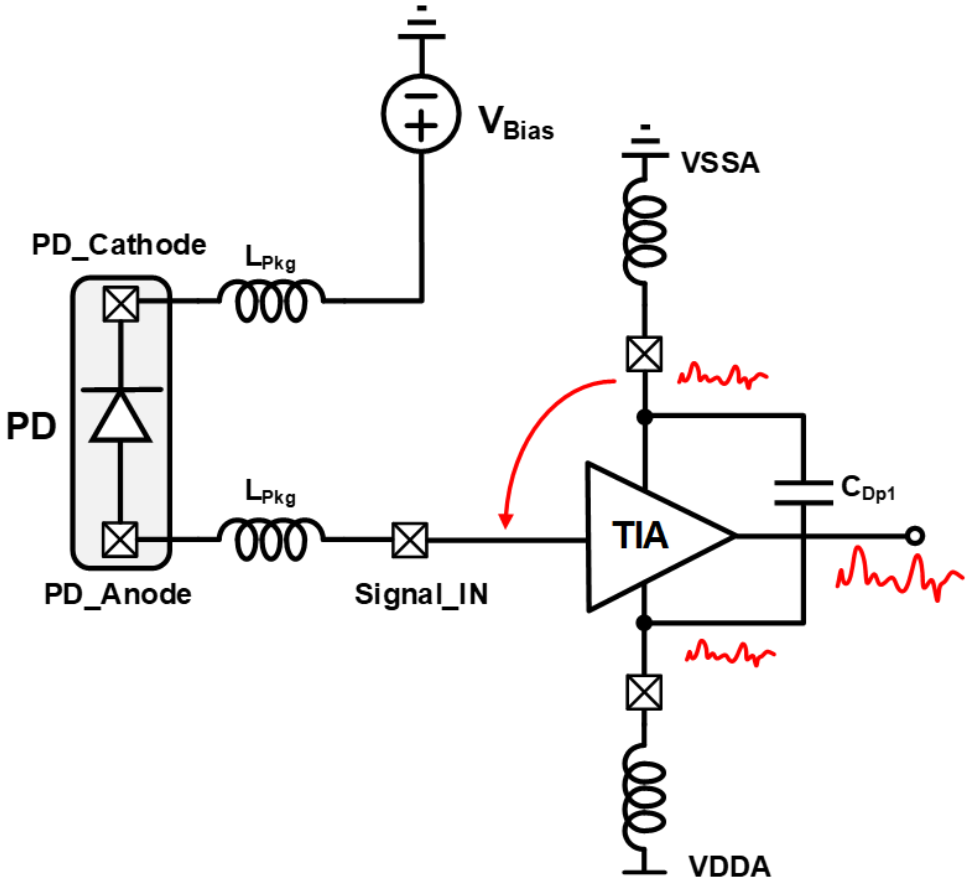
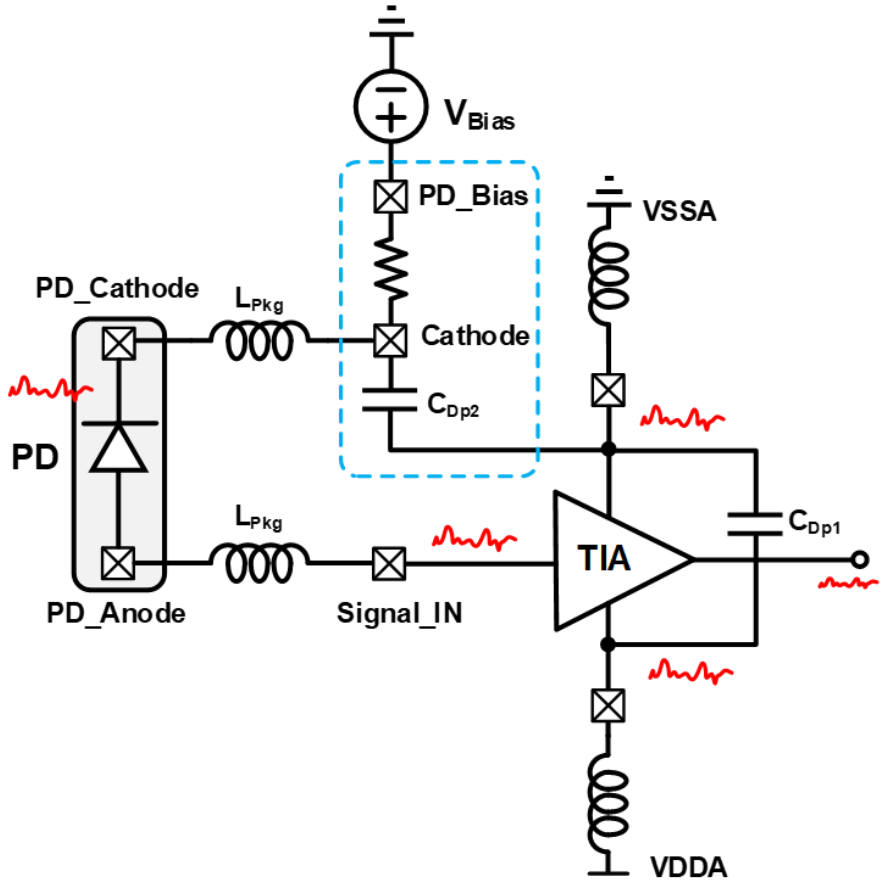
HKUST OWL

A 41-mW 30-Gb/s CMOS Optical Receiver with Digitally-Tunable Cascaded Equalization

PD Interface

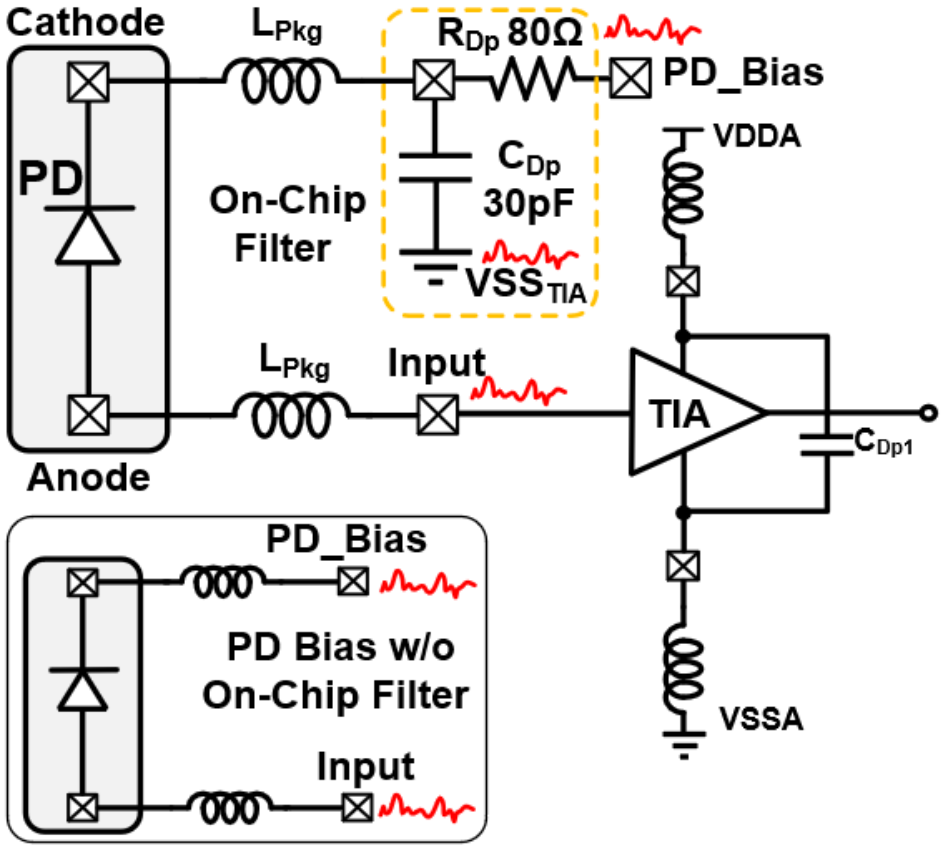


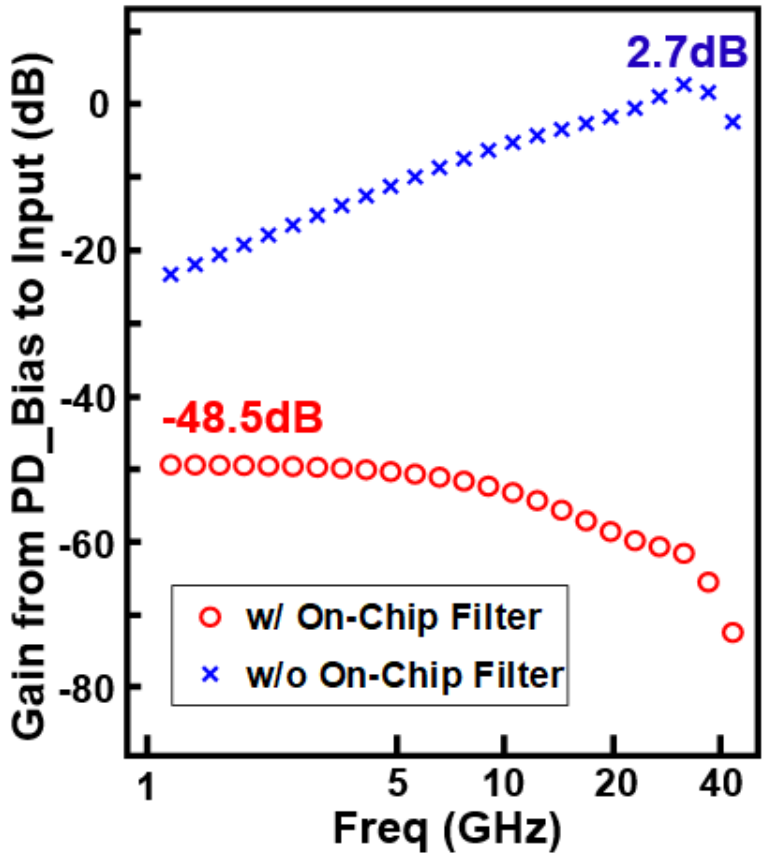
- External PD bias
- Transfer the supply noise to TIA output



- On-chip PD bias
- Prevent the supply noise to TIA output

PD-to-RX Interface with Bond Wire

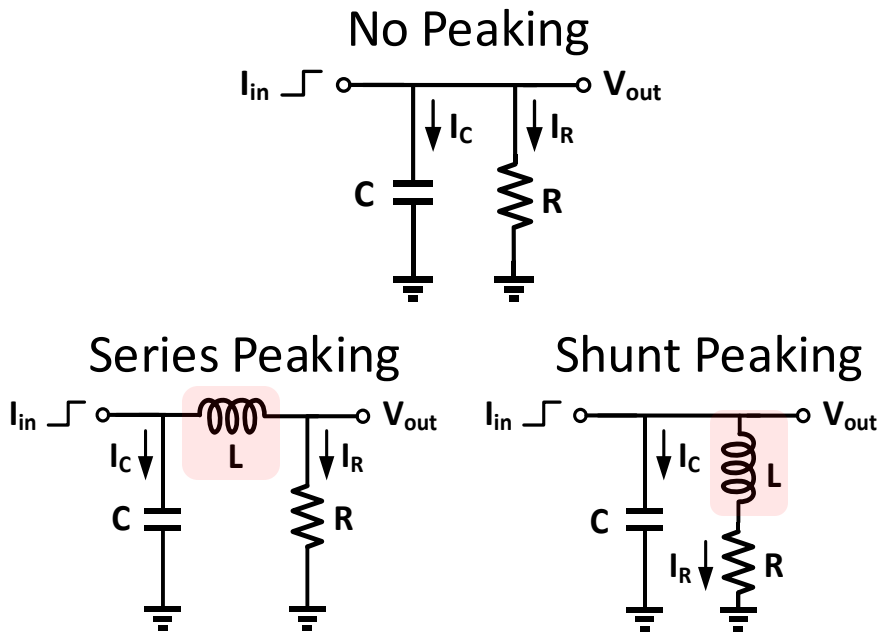


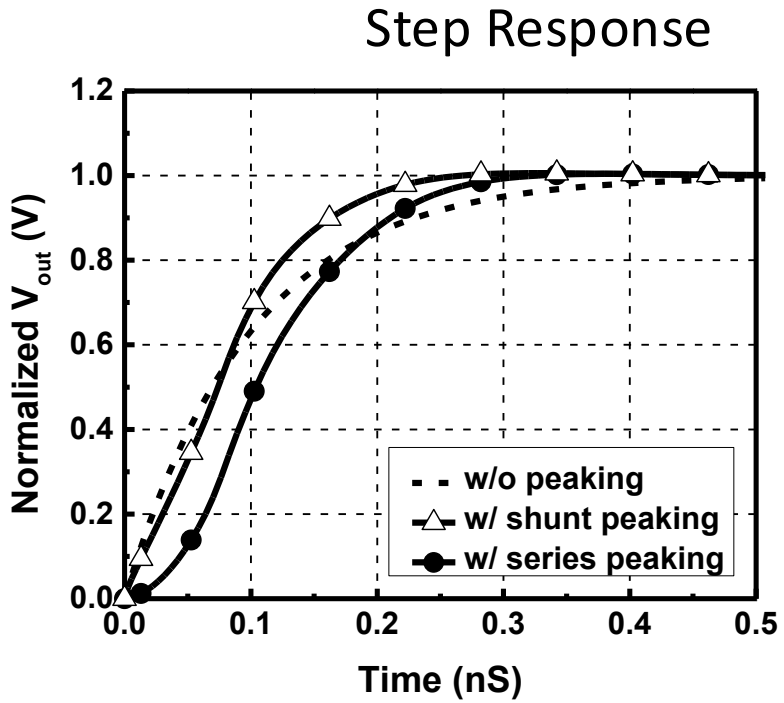


- On-chip PD bias and simulated conversion gain from PD bias to TIS input
- On-chip filtering prevents the noise at PD bias converting to TIA input

Bandwidth Enhancement Technique

- Inductive Peaking

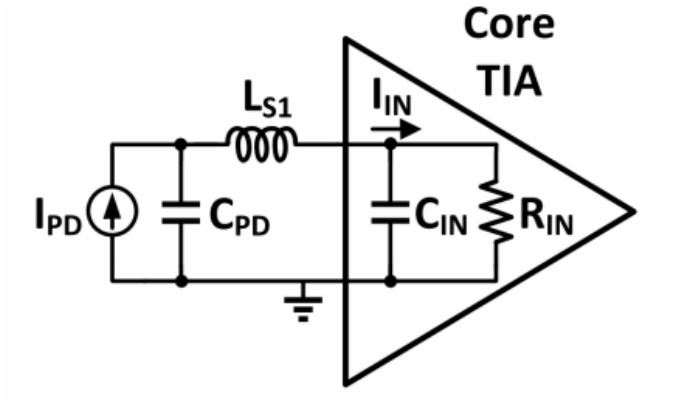




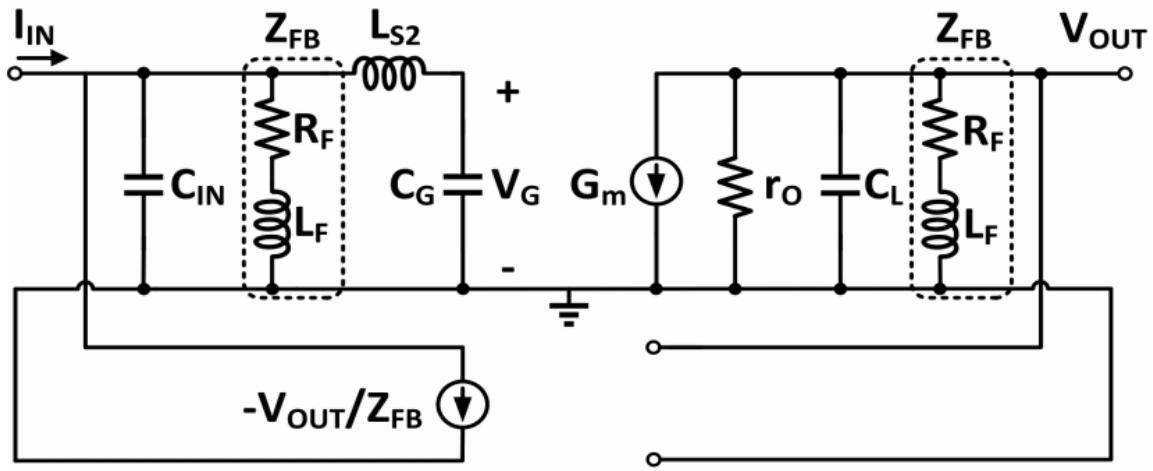
- Loading capacitor slows down output transition
- Series or shunt peaking inductor allows more high-frequency current to charge C -> Faster step response
- Faster response <-> Higher bandwidth

Bandwidth Enhancement Technique

- Multiple Inductive Peaking Technique



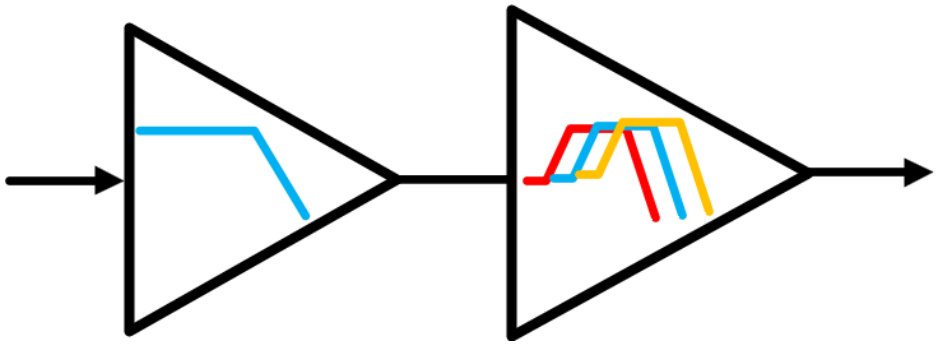
- Equivalent circuit of the input series peaking network
  - L_{S1}: bond-wire inductance

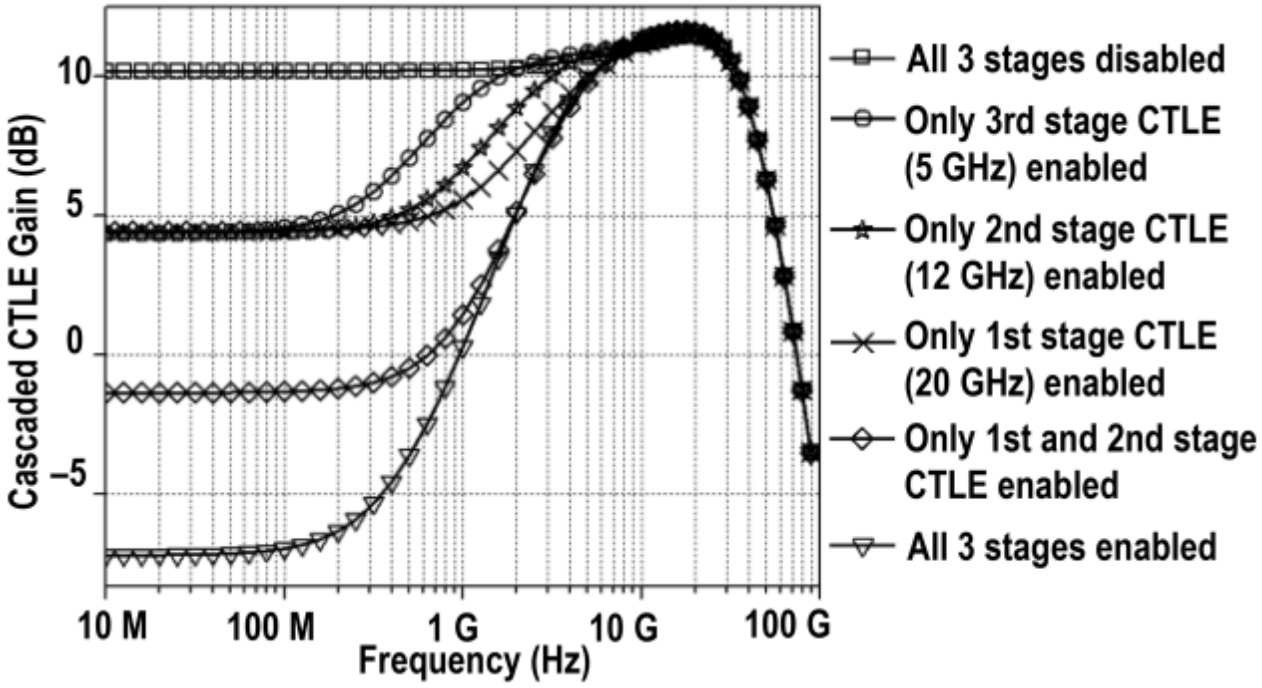


- Small-signal model of the core TIA
  - L_F and L_{S2} create the second and the third peaking

Bandwidth Enhancement Technique

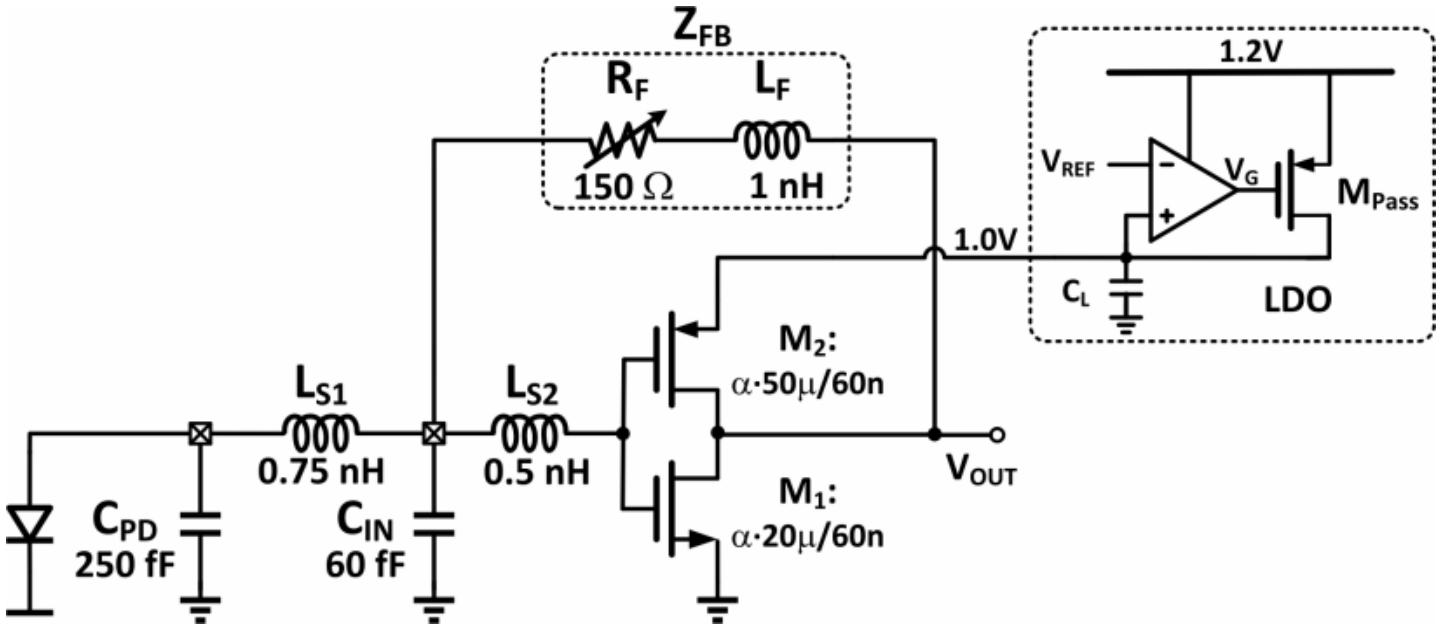
- Multi-Stage Cascaded CTLE

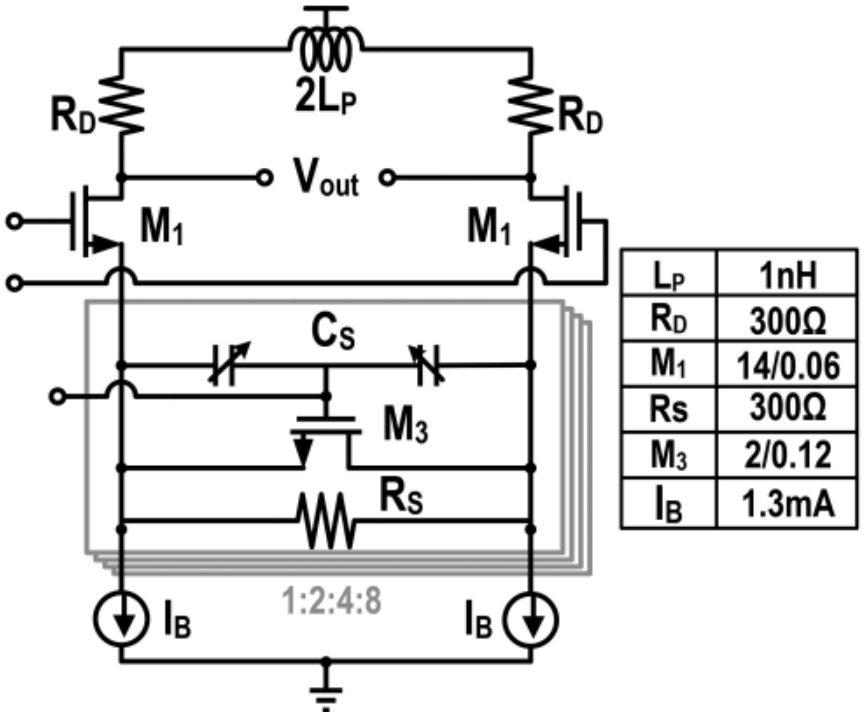




- Multi-stage CLTE provides different peaking at different frequencies
- Simulated frequency responses of the 3-stage cascaded CTLE

TIA and CTLE

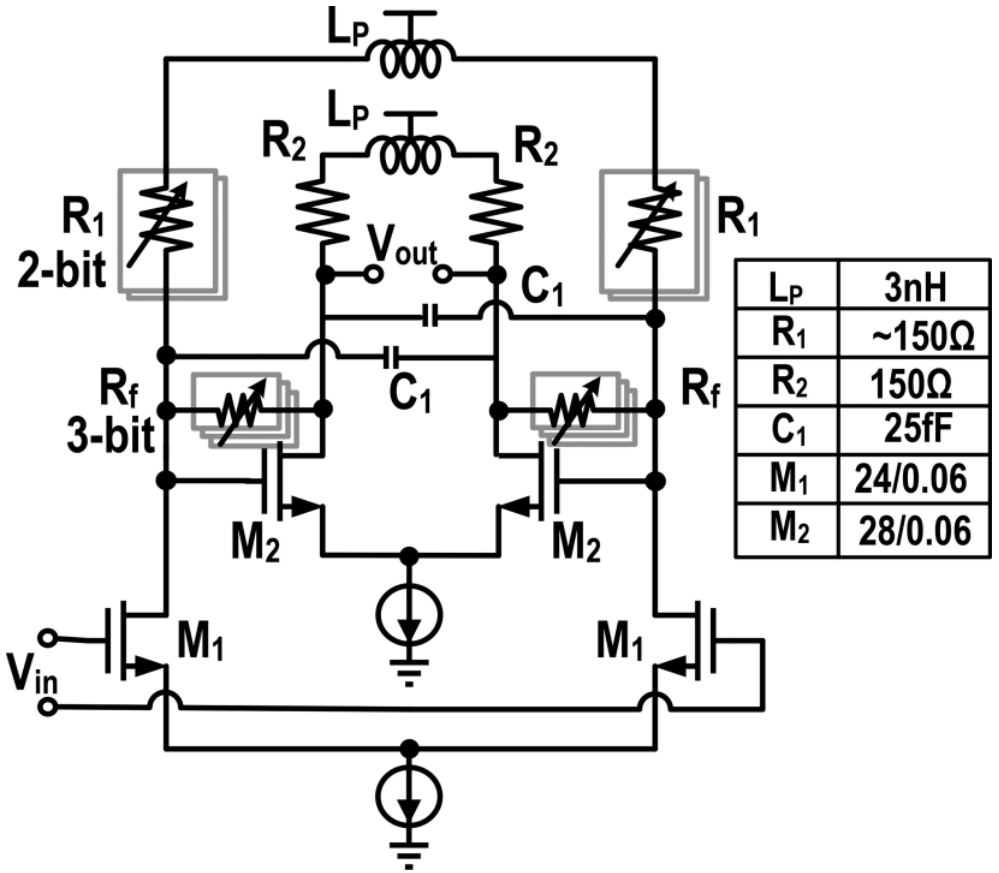




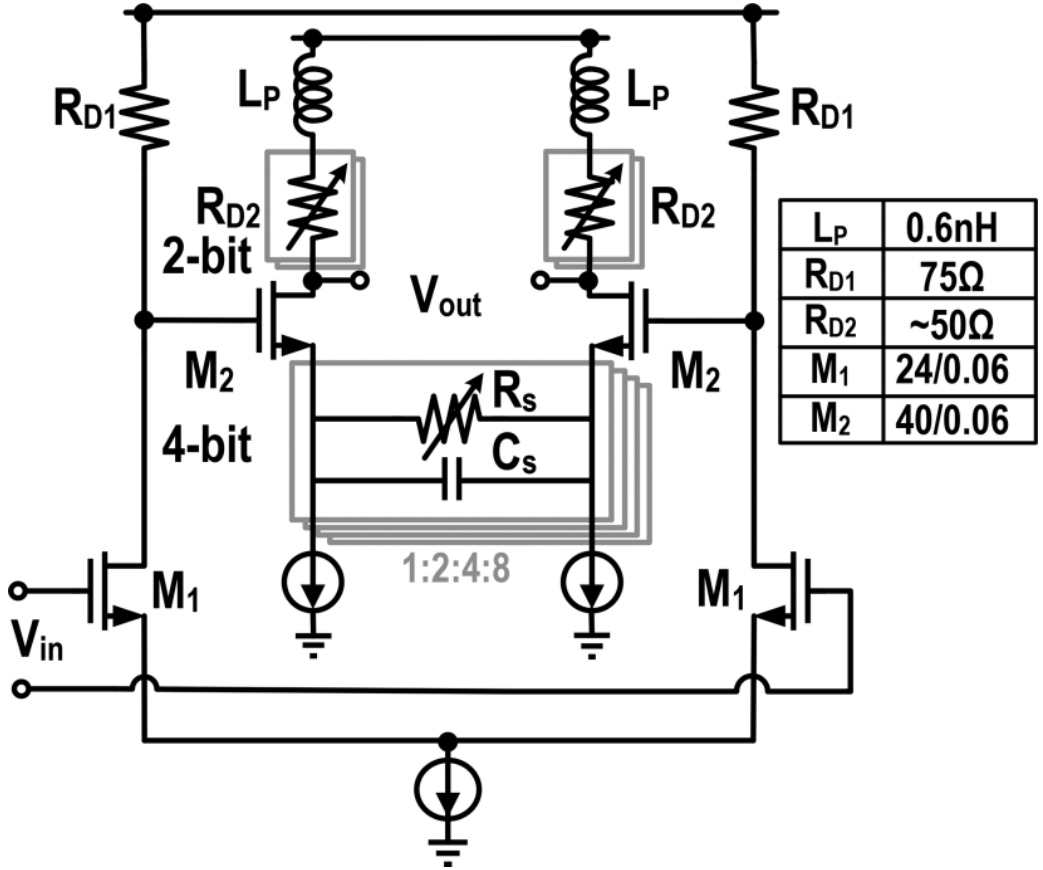
L_P	1nH
R_D	300Ω
M_1	14/0.06
Rs	300Ω
M_3	2/0.12
I_B	1.3mA

- Schematic of TIA with integrated LDO
- Schematic of the CTLE

Modified CH MA/LA and Output Driver



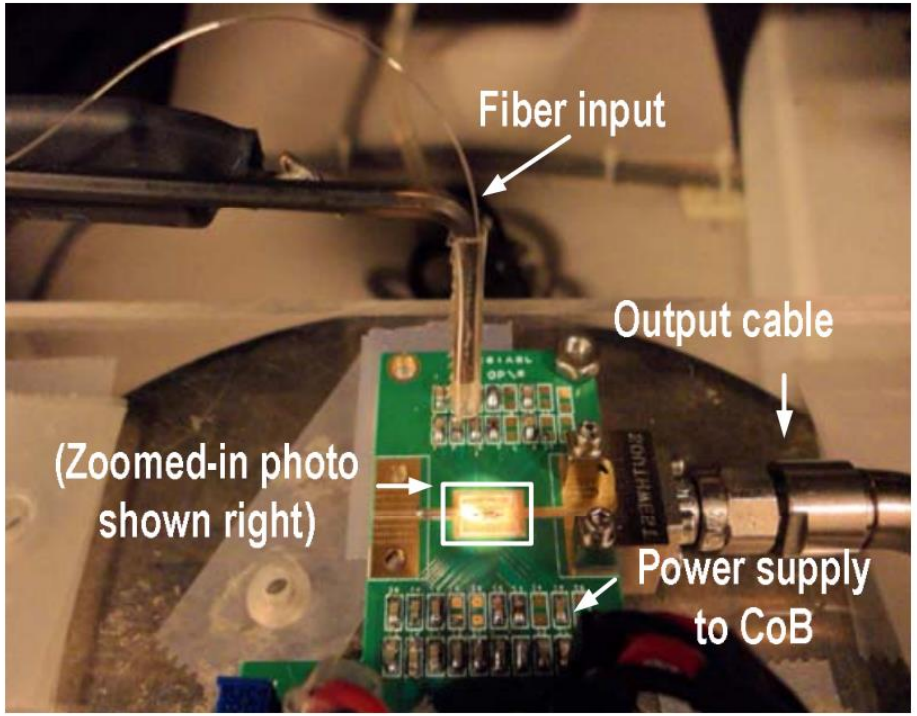
L_P	3nH
R_1	~150Ω
R_2	150Ω
C_1	25fF
M_1	24/0.06
M_2	28/0.06

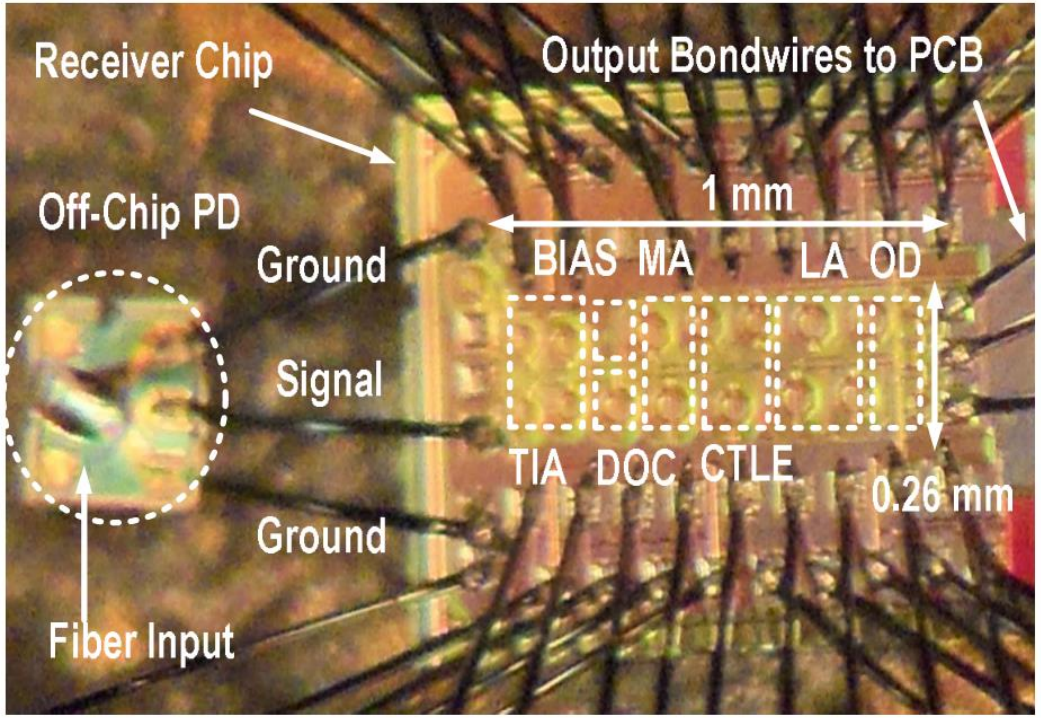


L_P	0.6nH
R_{D1}	75Ω
R_{D2}	~50Ω
M_1	24/0.06
M_2	40/0.06

- Schematic of the modified CH MA/LA
- Schematic of the output driver

Measurement Setup and Chip Micrograph

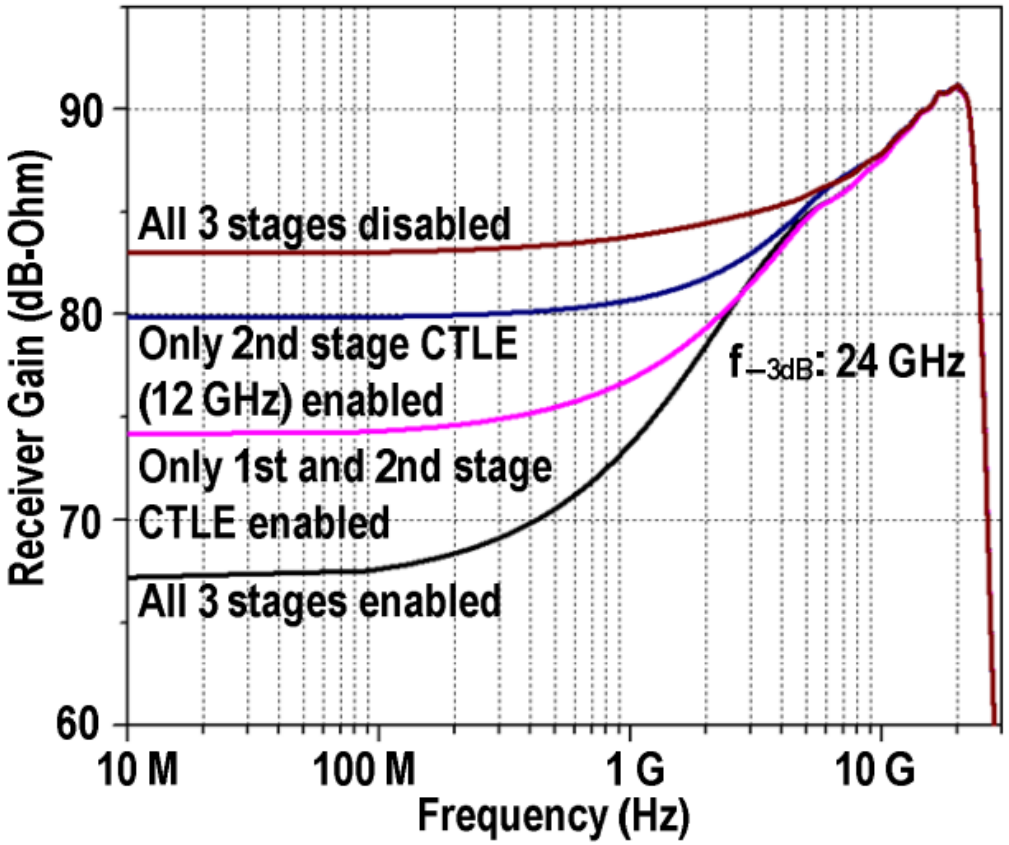


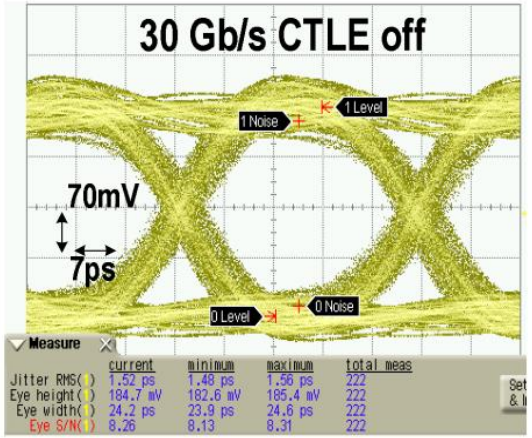


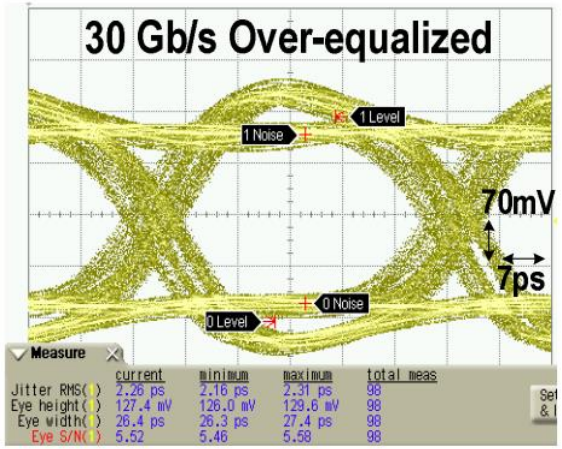
- Optical measurement setup
- Optical light is coupled through a single-mode fiber (SMF)

- Chip micrograph
- Fabricated in 65nm CMOS technology
- Wire-bonded with a commercial PD

Electrical Measurement Results



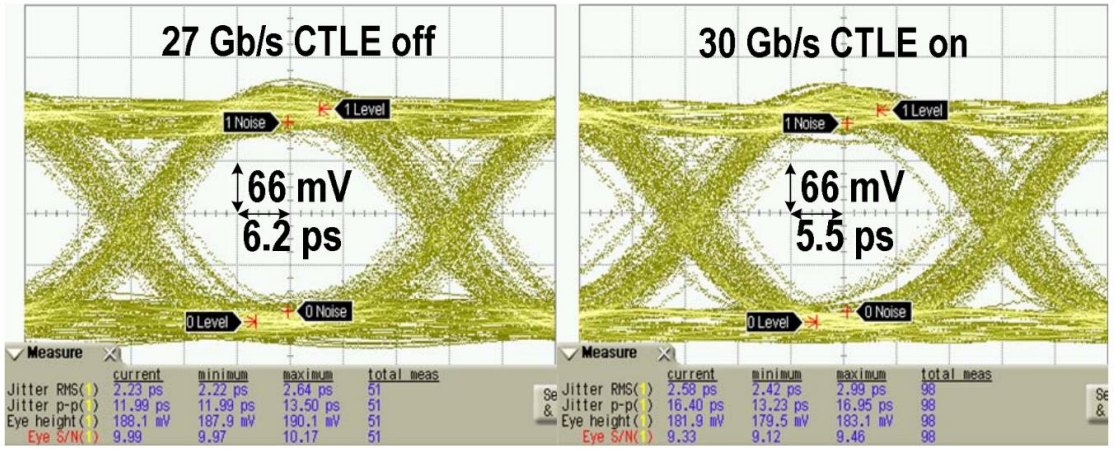


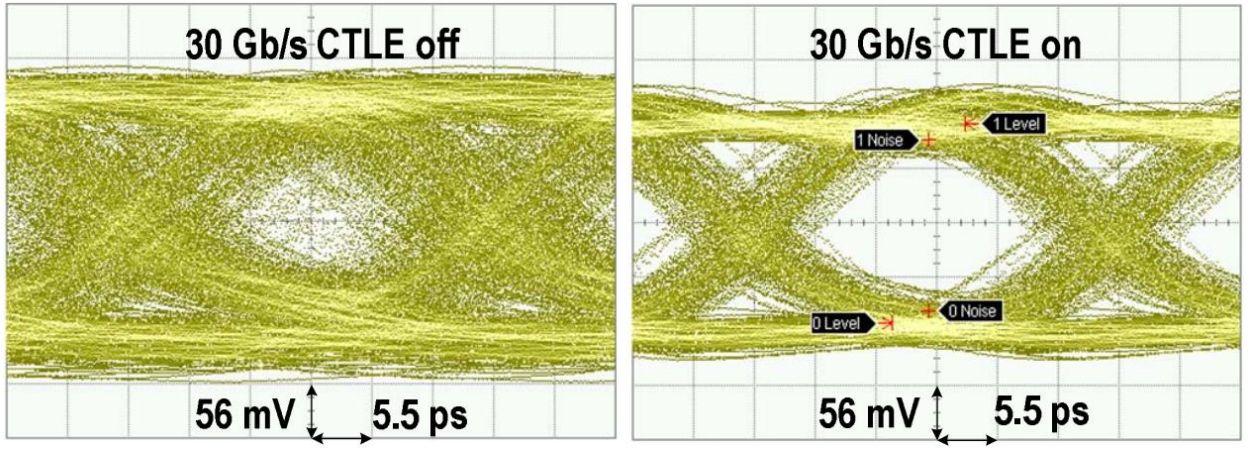


- Measured electrical frequency response
- 67-83 dBΩ, with 24-GHz bandwidth

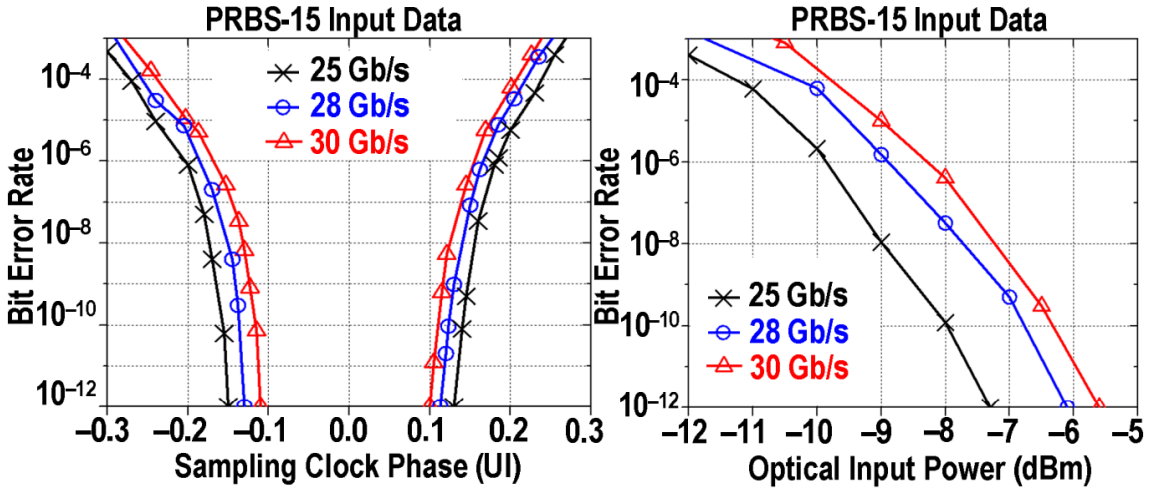
- Measured electrical eye diagram at 30 Gb/s with CTLE off and on

Measurement Results



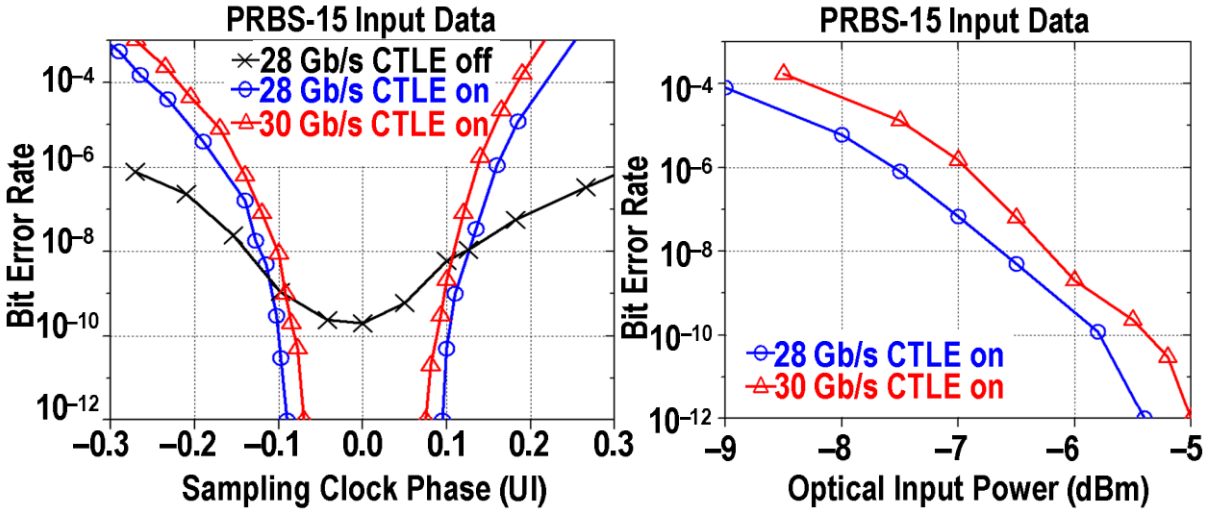


- Optical measurement results with a 30-Gb/s PD



- BER bathtub curves and input sensitivity

- Optical measurement results with a 14-Gb/s PD



- BER bathtub curves and input sensitivity

Performance Summary and Comparison

	[1] ISSCC'13	[2] ISSC'13	[3] ISSCC'12	This Work	
CMOS Technology	65nm	65nm	90nm	65nm	
Supply Voltage	1	3.3/1	1.2	1 (1.2 for LDO)	
Gain (dBΩ)	72.5	76.8	78.3	83	
Bandwidth (GHz)	21	21.4	20	24	
Power (mW)	48.8	90.9	44.4	41	
Data Rate (Gb/s)	25	25-28	25	30	
Sensitivity (dBm)	-6.8	-9.7	-4	-5.6	-5.0
Eye Opening (1-UI)	N/A	65%	22%	24%	18%
Efficiency (pJ/bit)	1.95	3.25	1.78	1.37	

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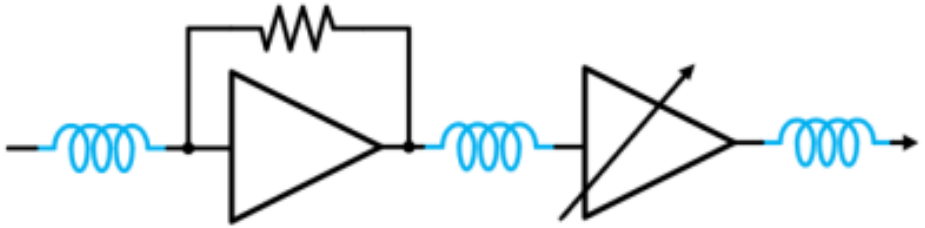
HKUST OWL

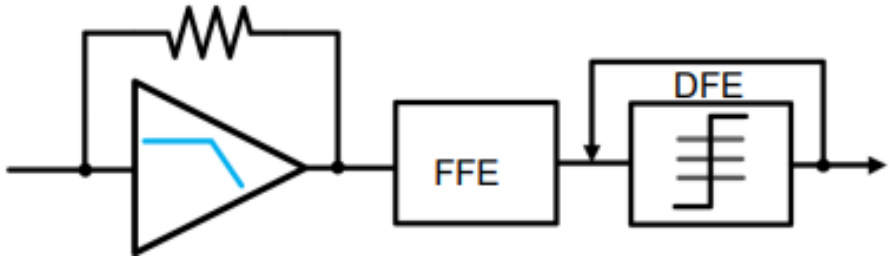
An Energy- and Area-Efficient Inductorless CMOS PAM4 Optical Receiver Achieving 700 Gb/s/mm^2 Towards Silicon Photonic Chiplet

Optical Receiver Architecture Comparison



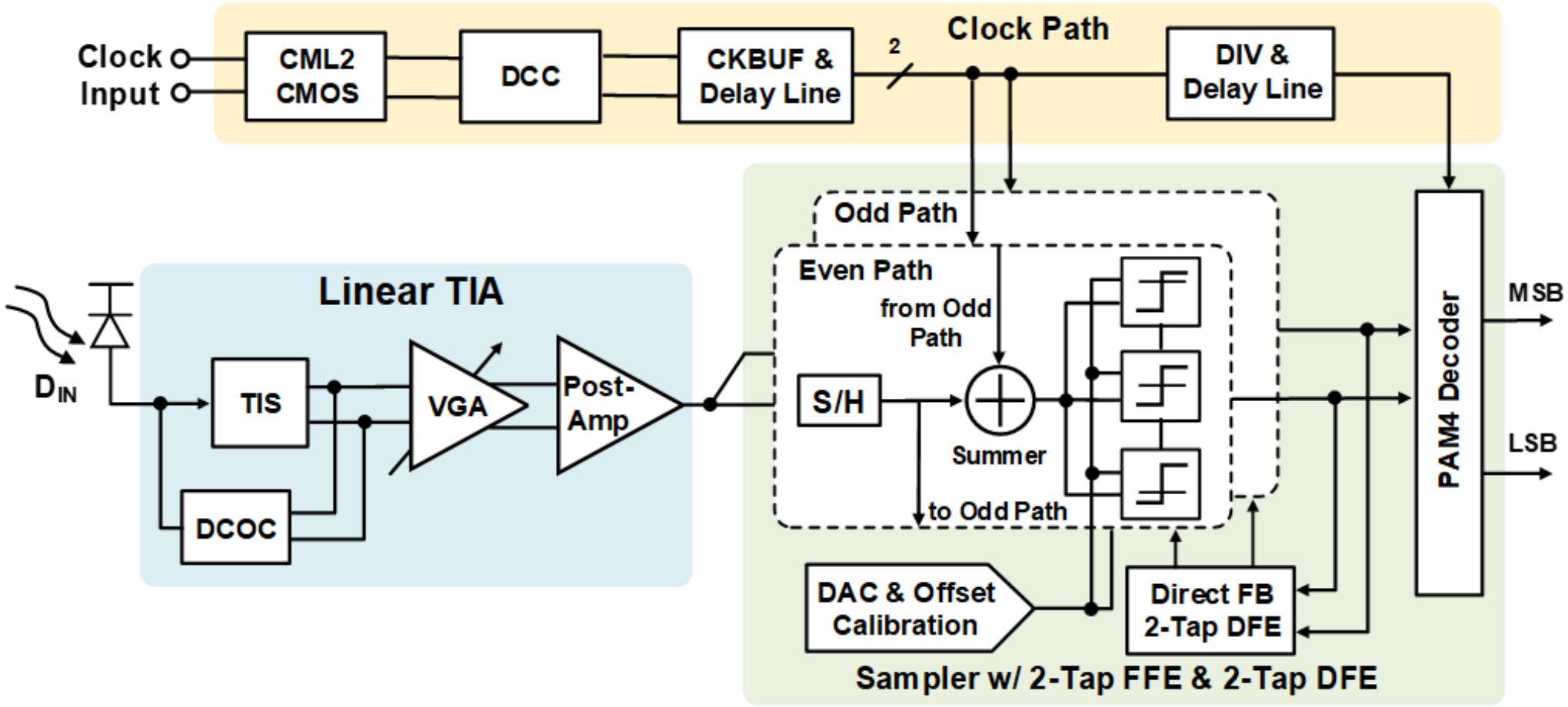
- Distributed inductive peaking
- Large area

- Low-BW TIA + CTLE
- Power hungry



- Inductorless TIA + FFE + DFE
- Compact and energy-efficient

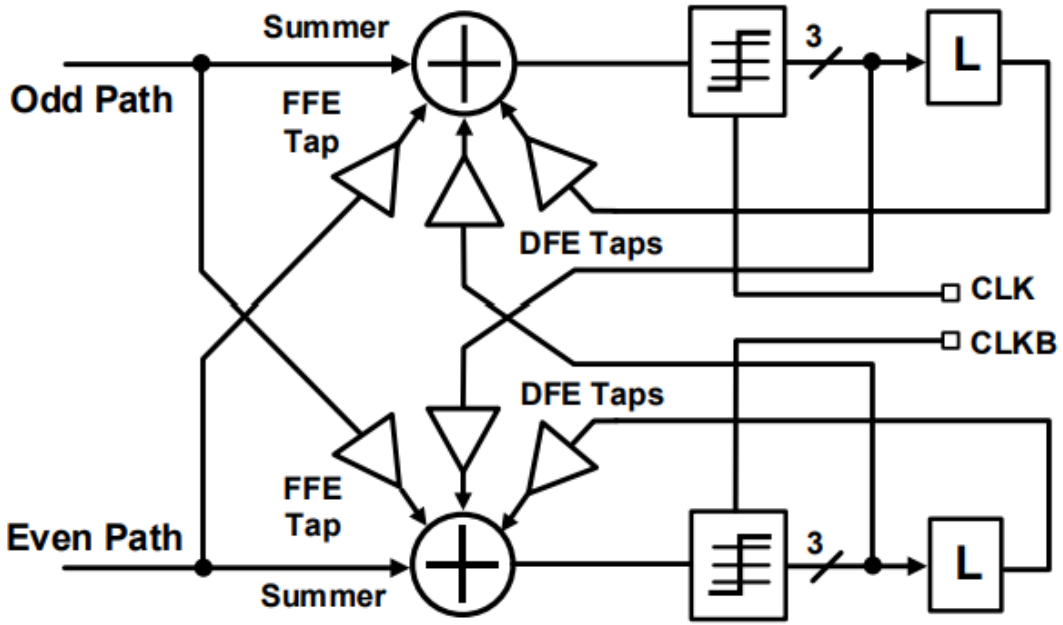
Proposed Architecture



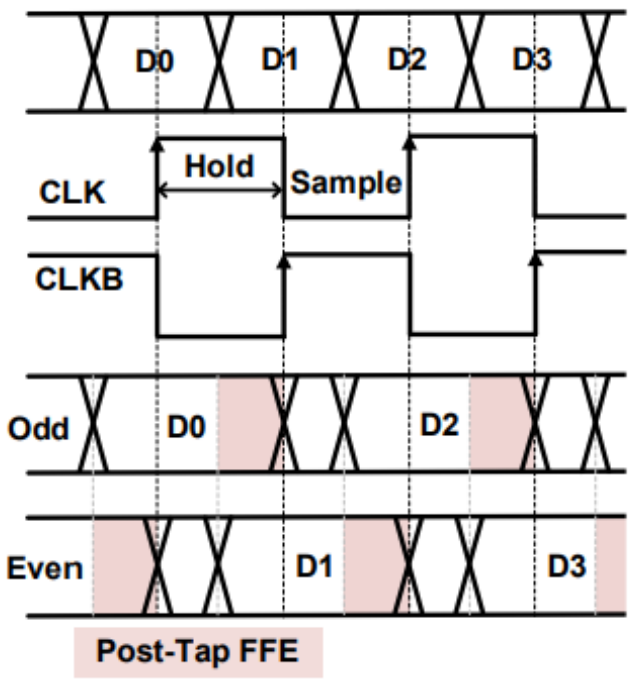
- Half-rate structure
- 2-tap FFE and 2-tap DFE integrated with sampler

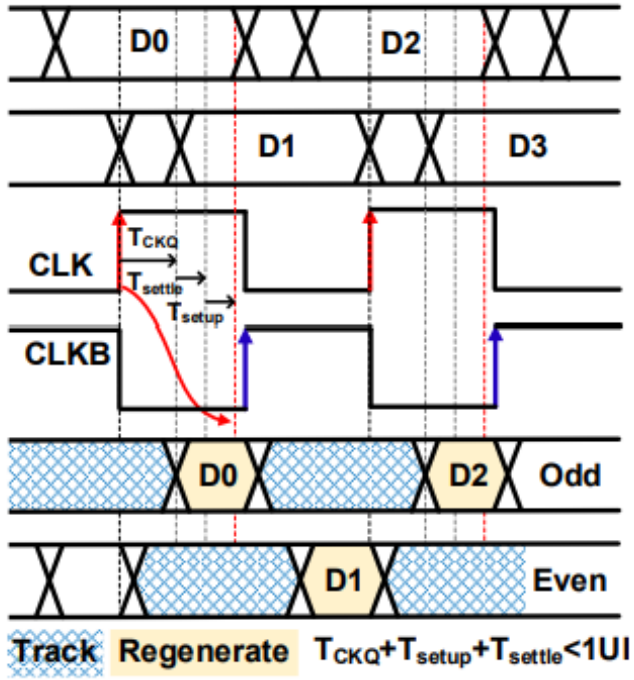
FFE and DFE

Half-rate FFE and DFE



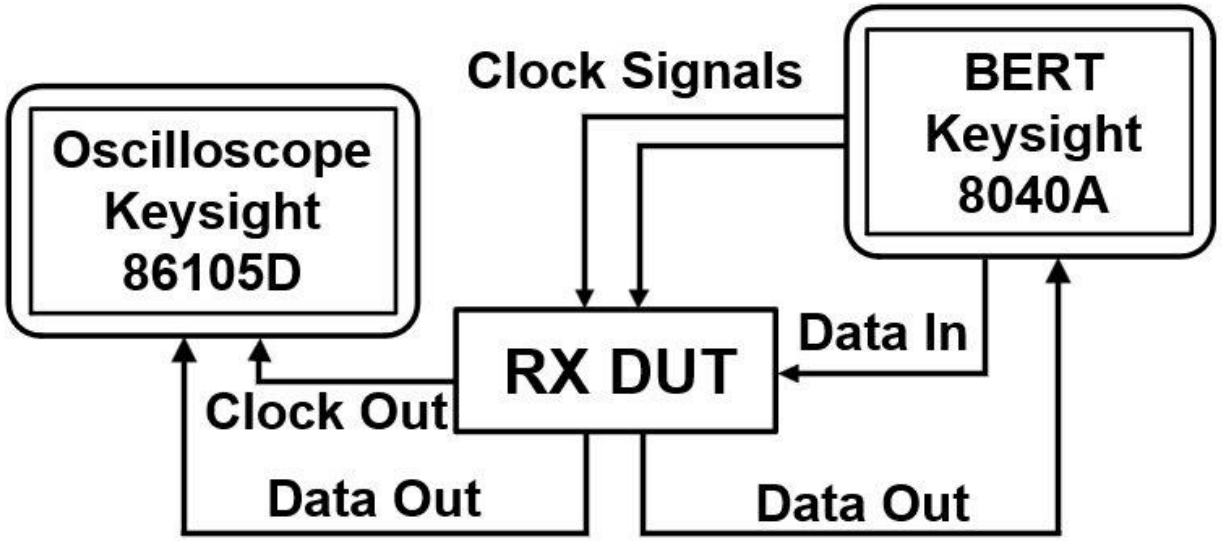
Timing Diagram of FFE and DFE



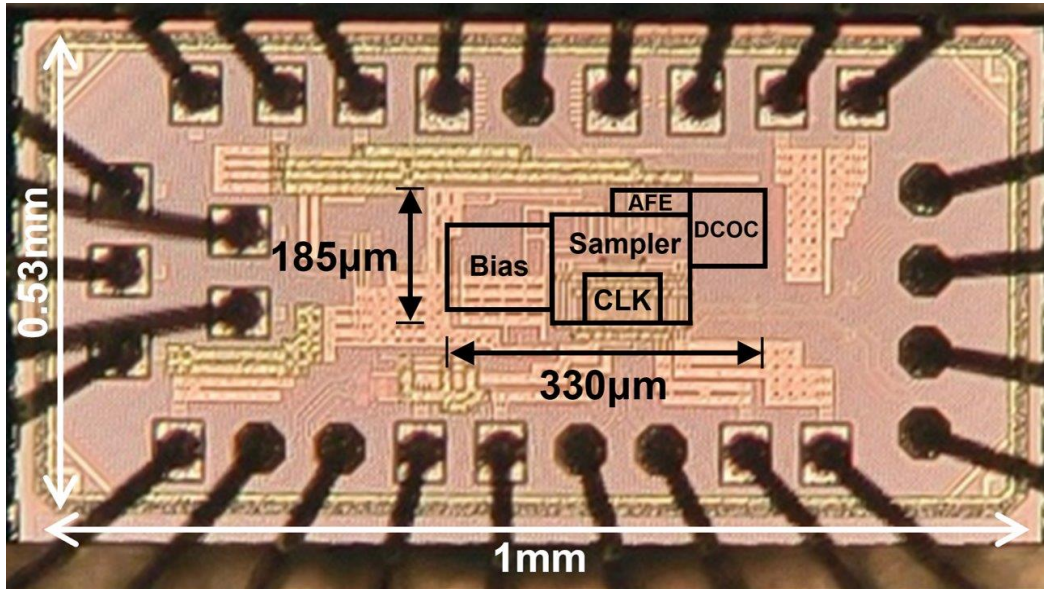


- Post-tap FFE can be achieved by summing the odd and even signal path
- 1-UI timing constrain should be met for the first tap direct DFE

Measurement Setup and Chip Micrograph

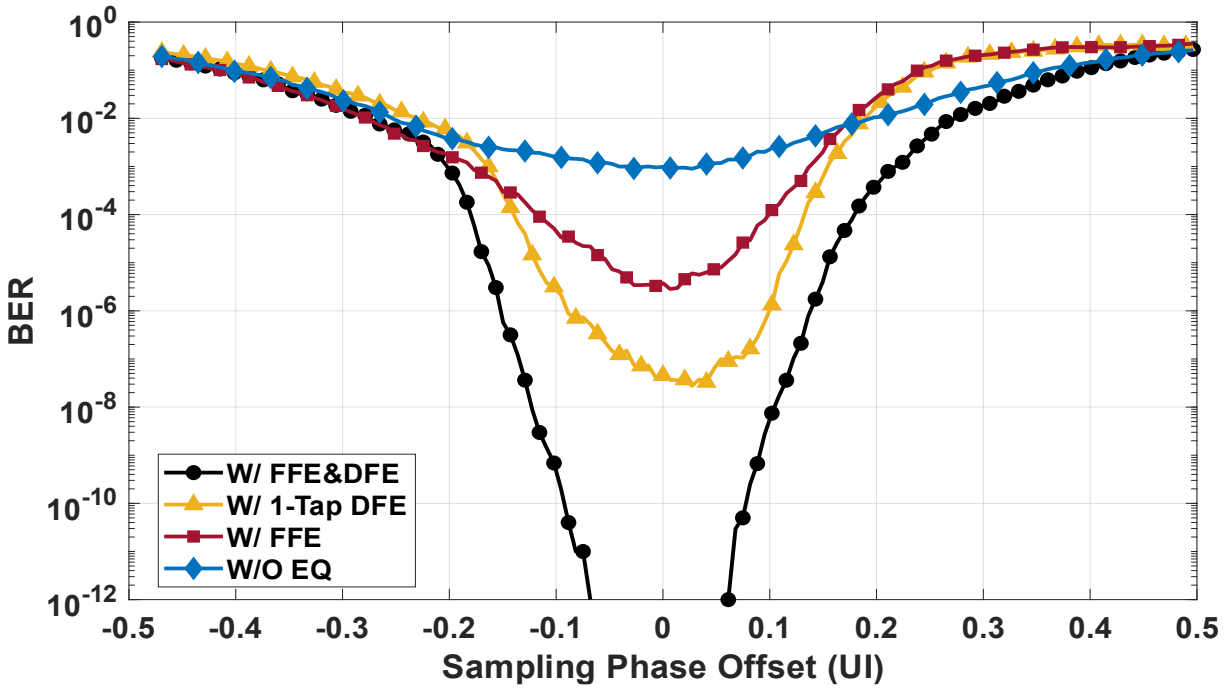


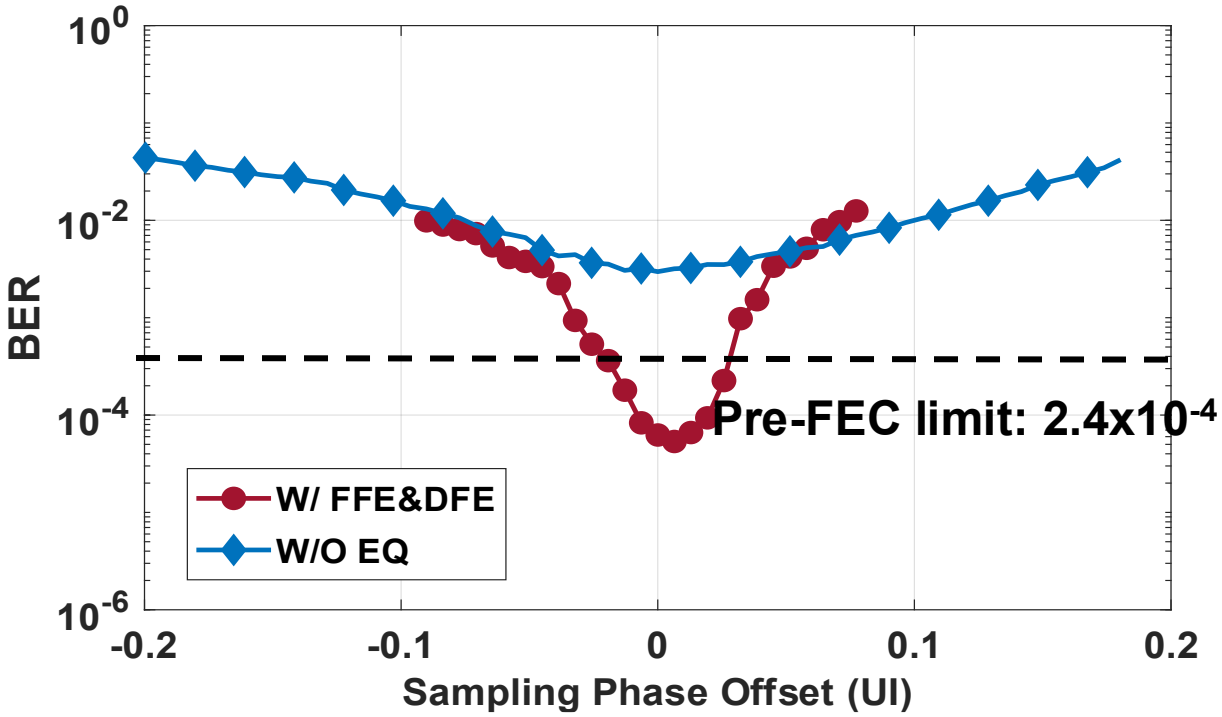
- Measurement setup



- Chip micrograph
- Core area: 0.06mm^2

Measurement Results





- Bathtub curve at 30 Gb/s NRZ
- Bathtub curve at 42 Gb/s PAM4

Performance Summary and Comparison

	JSSC'21	OJCS'21	ISSCC'21		RFIC'23	This Work	
Technology	65nm CMOS	40nm CMOS	28nm CMOS		28nm CMOS	28nm CMOS	
Data Rate (Gb/s)	16	36	100		42.7	42	
Signaling	Duobinary	PAM4	PAM4		NRZ	PAM4	
Number of Inductors	0	6	>16		3	0	
NRZ OMA Sens. at BER 1e-12 (dBm)	-16.8	N/A	-11.1 @56Gb/s		-3.6*	-8.2 @28Gb/s	
PAM4 OMA Sens. at 2.4e-4 (dBm)	N/A	-4.8*	-8.9		N/A	-5.1 @48Gb/s	
Rx EQ Capabilities	N/A	2-Tap DFE	2-Tap FFE + 2-Tap DFE		N/A	2-Tap FFE + 2 -Tap DFE	
Area (mm^2)	0.09	0.23	0.45		0.11**	0.06	
Power (mW)	23 (RX)	128.8 (RX)	117 (TIA)	381 (RX)	145.2** (RX)	13.1 (TIA)	57.3 (RX)
Efficiency (pJ/bit)	1.9	4.0	1.17	3.9	3.4	0.31	1.36
FoM (Gb/s/mm^2)	100	139	222		388	700	

*Estimated from the reported sensitivity curve **CDR included **FoM** = Data rate /

Outline

- Motivation
  - Electrical vs Optical Link
- RX Architecture
  - Wireline vs Optical Receiver
  - ADC-Based Receiver
- Circuit Implementations
  - PD Interface
  - Multi-peaking TIA
  - Modified Cherry-Hooper Amplifier
  - FFE and DFE Implementation
- **Practical Issue**
  - **On-Chip LDO for Improved Sensitivity**
- Conclusion

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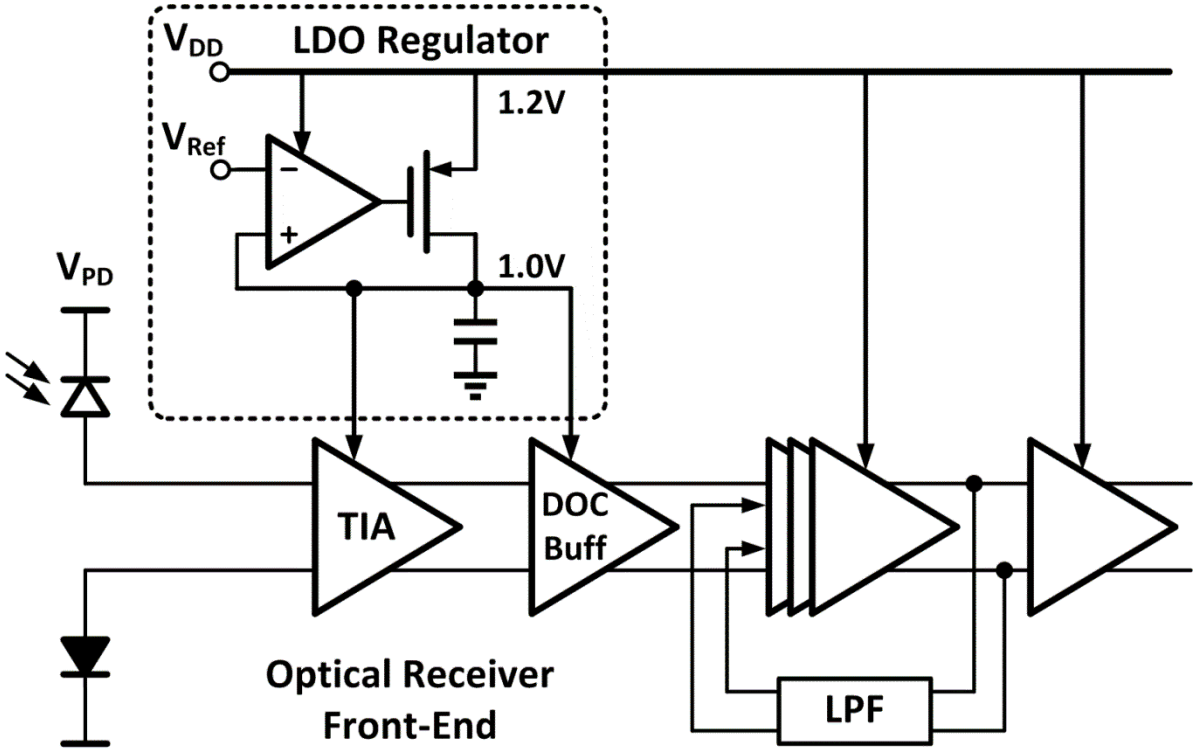
HKUST OWL

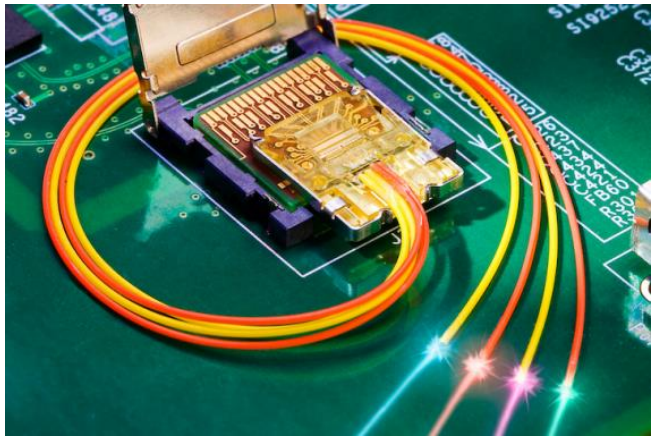
A Fully-Integrated Low-Dropout Regulator With Full-Spectrum Power Supply Rejection

Motivations

- **Fully-integrated** and **area-efficient** low dropout regulator (LDO) are highly desirable for point-of-load power delivery.
- LDOs with power supply rejection (PSR) up to **GHz range** are in demand for wideband communication systems.

[Harwood ISSCC 12]
[Takemoto ISSCC 13]





Light Peak Module - Intel

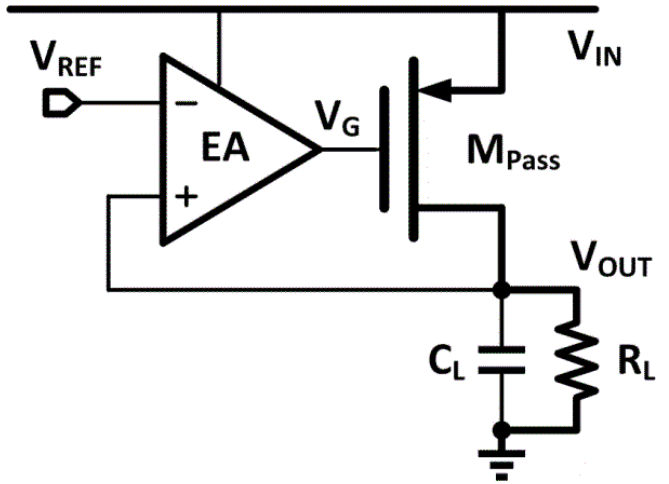
LDO Requirements

- To make a comparison, a figure-of-merit (FOM) of speed is defined

$$\text{FOM} = T_R \frac{I_Q}{I_{MAX}} = \frac{C \times \Delta V_{OUT}}{I_{MAX}} \times \frac{I_Q}{I_{MAX}}$$

[Hazucha JSSC 05]

  - Fast transient response
  - Small quiescent current (I_Q)



- Good PSR
- Area-efficient and scalable with process

LDOs with Off-/On-Chip Capacitor

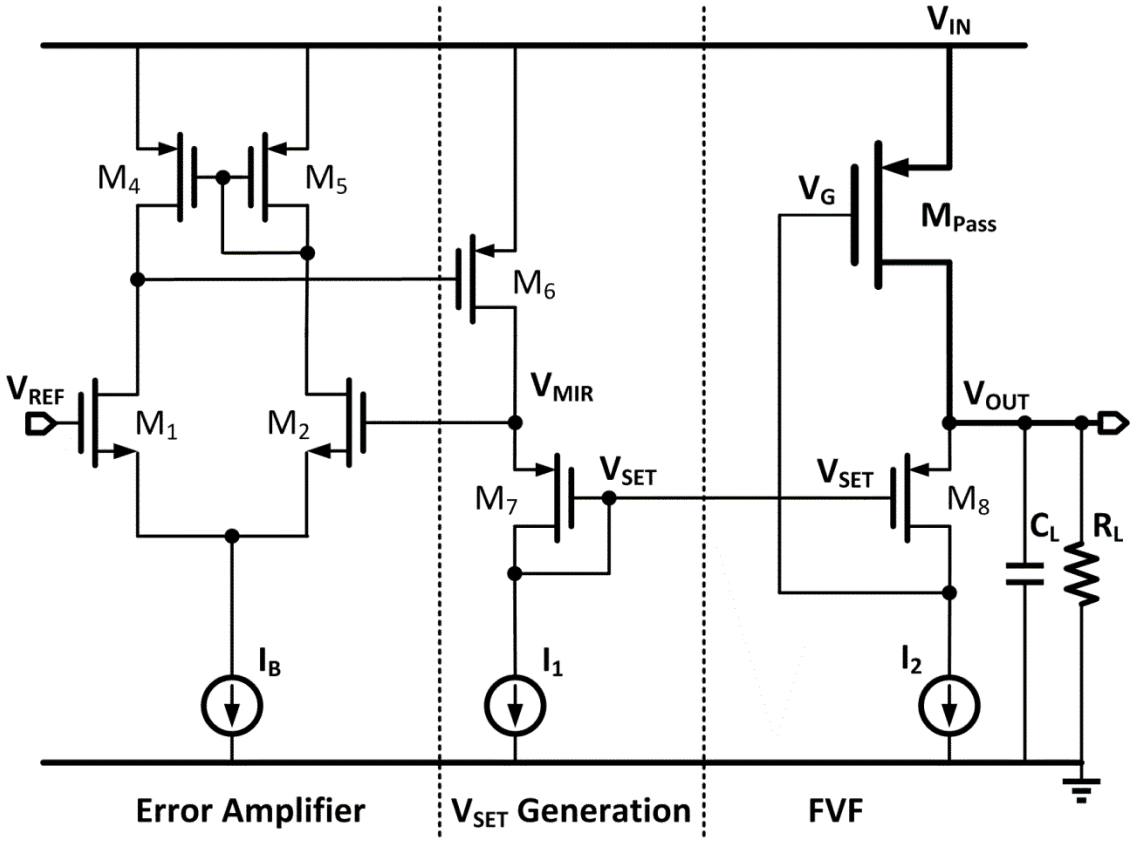
- LDO Regulators with **Off-Chip µF range** Capacitor
  - Off-chip cap is conventionally connected for filtering
  - Dominate pole located the output node
  - Small load transient glitches
  - High PSR

- LDO Regulators with **On-Chip sub-nF range** Capacitor
  - Dominate pole at the internal node (in previous designs)
  - Large undershoot and overshoot during load transient
  - Poor PSR

Improving the PSR and transient performances of the fully-integrated LDO is our key design issue

Schematic of the FVF Topology

- **Basic idea**: take the advantage of the advanced processes, push the internal poles to be higher than the UGF.
- **Technique**: Flipped Voltage Follower (FVF)



[Man TCAS-I 08]

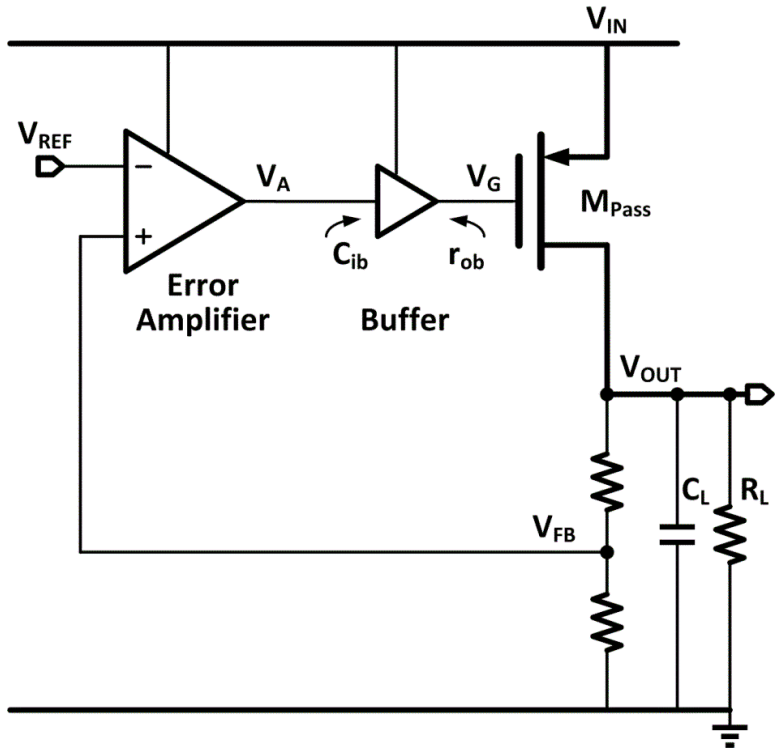
0.35μm CMOS

p_{Gate} Dominated

Poor DC Regulation

Schematic of the BIA Topology

- **Basic idea**: take the advantage of the advanced processes, push the internal poles to be higher than the unity-gain frequency (UGF).
- **Technique**:
  Buffer Impedance Attenuation (BIA)



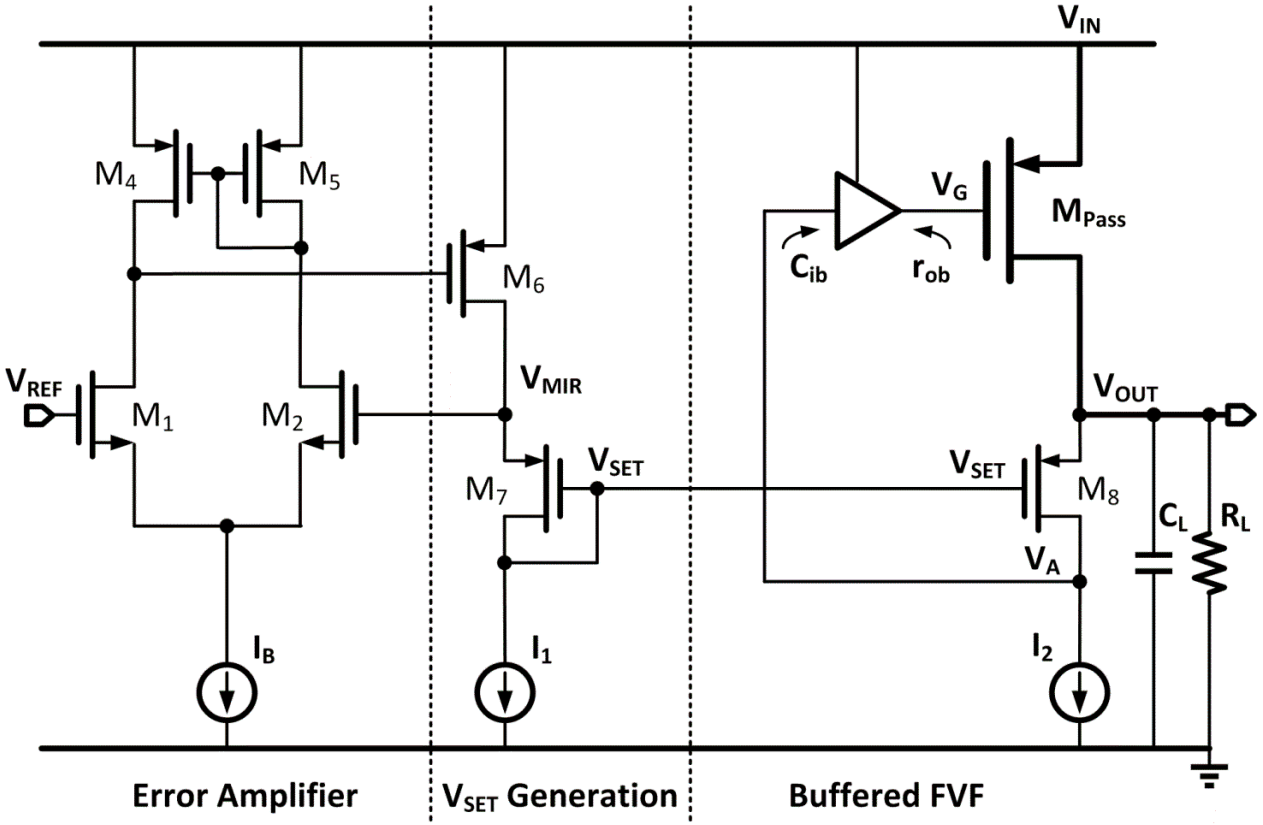
[Al-Shyoukh JSSC 07]

0.35µm CMOS

With 1µF Capacitor

Schematic of the FVF + BIA Topologies

- **Basic idea**: take the advantage of the advanced processes, push the internal poles to be higher than the UGF.
- **Techniques**: Flipped Voltage Follower (FVF) Buffer Impedance Attenuation (BIA)



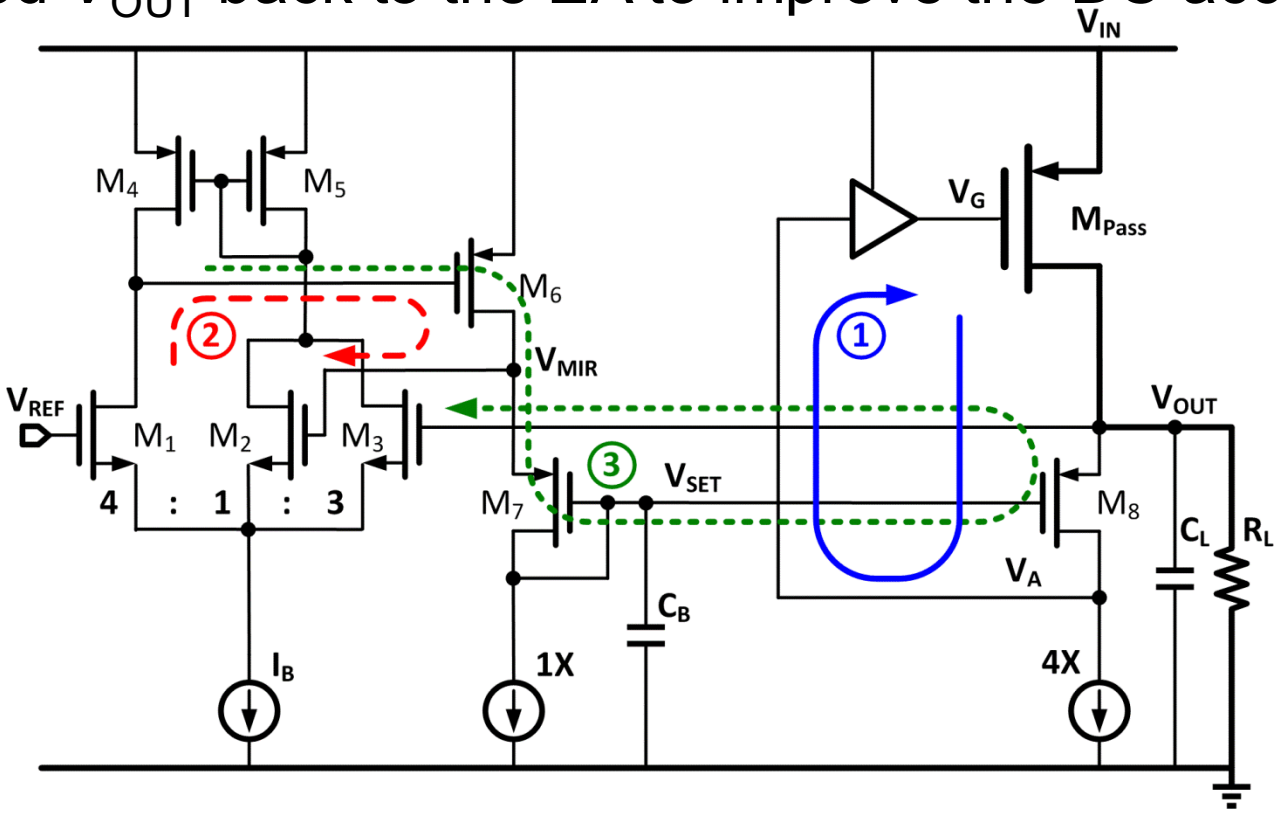
65nm CMOS

p_{Out} Dominated

Poor DC Regulation

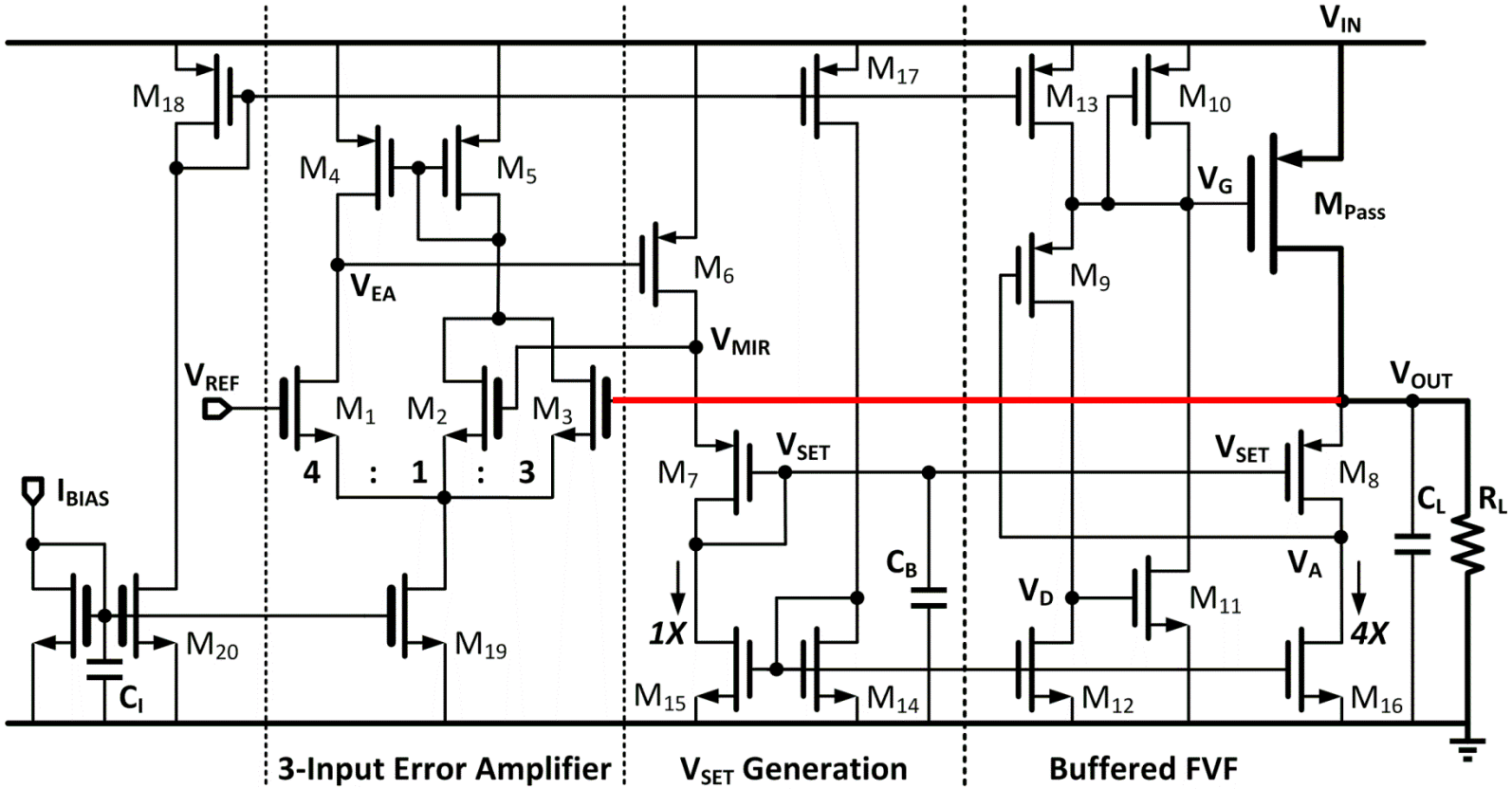
Tri-Loop in the Proposed LDO

- **Loop-1**: an ultra-fast low-gain loop with p_{Out} being its dominant pole and p_{Gate} be pushed to GHz range by BIA technique;
- **Loop-2**: a slow loop that generates V_{MIR} &V_{SET};
- **Loop-3**: feed V_{OUT} back to the EA to improve the DC accuracy.



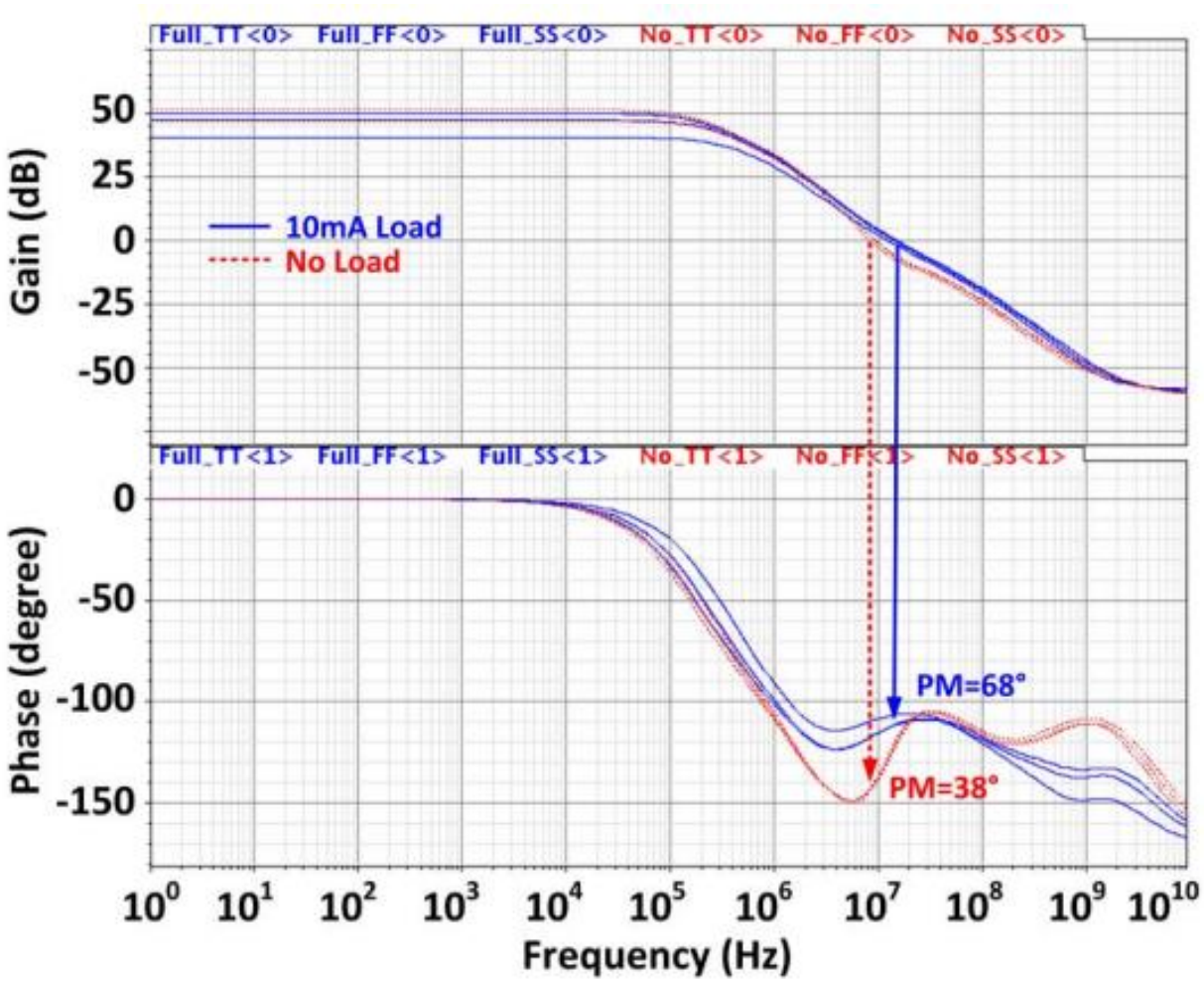
Schematic of the Proposed Tri-Loop LDO

- **Techniques**: Flipped Voltage Follower (FVF) and
  Buffer Impedance Attenuation (BIA)
- **Proposed 3-Input Error Amplifier (EA), and Tri-Loop Topology**

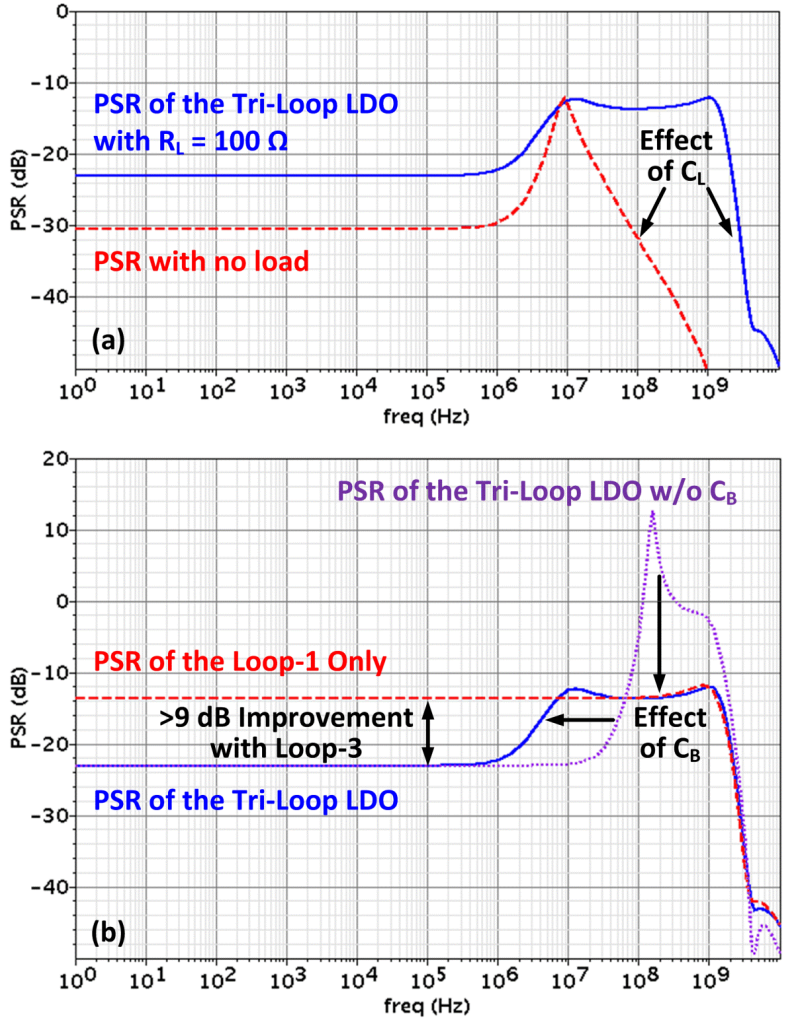


Simulated Bode Plot of LDO and PSR

- V_{IN} = 1.2V
- V_{OUT} = 1.0V
- R_L = 100Ω



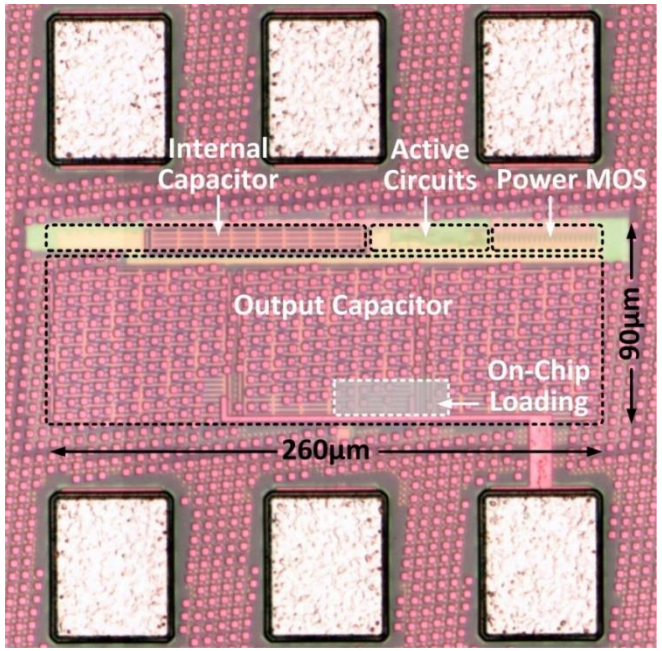
- Bode plot of the LDO

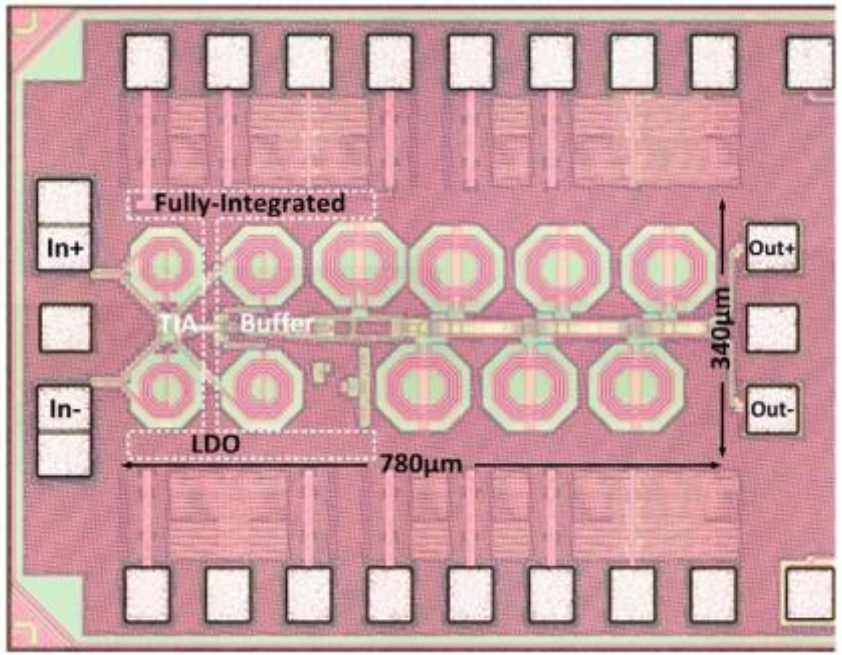


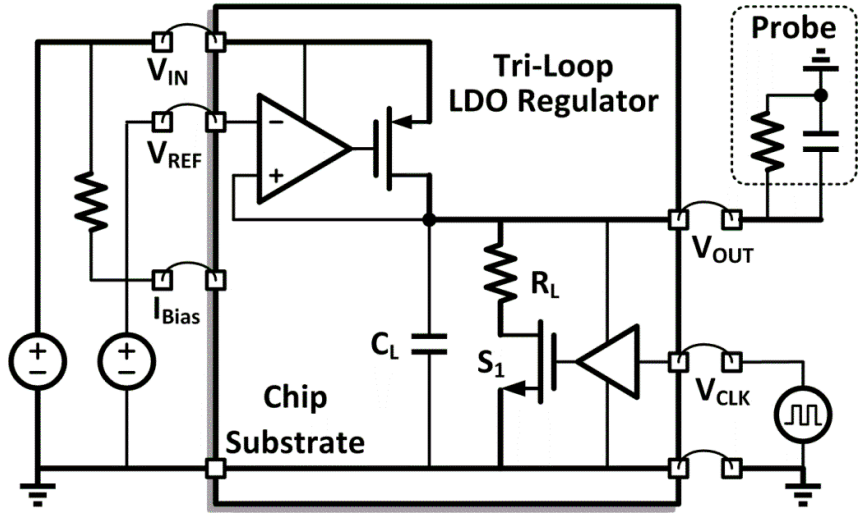
- PSR

Chip Micrograph of the LDO in 65nm

- Effective Area: 90 × 260 μm² (with on-chip loading)
- Total on-chip capacitance: 140 pF
  (stacked MOS and MIM capacitors)







- Stand-alone version
- Fully-integrated version

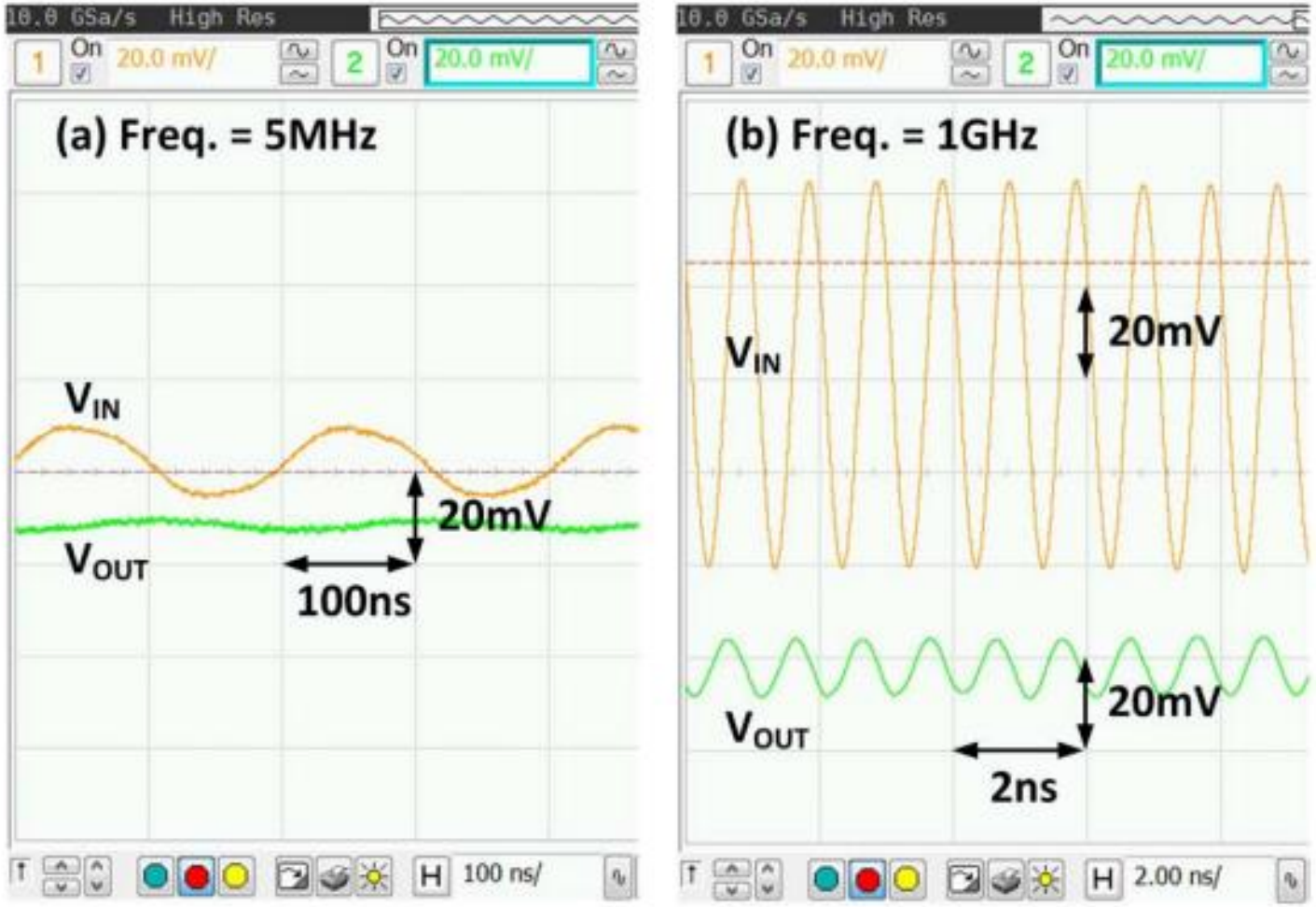
Ultra Fast Transient Response

- Rising/Falling edges of the load : < 200ps (0 mA to 10 mA)
- I_Q: 50µA; C_{Total}: 140 pF; ΔV_{OUT}: 43mV (undershoot)
- Response time T_R: 0.6 ns
- FOM: 3.01 fs

$$\text{FOM} = T_R \frac{I_Q}{I_{MAX}} = \frac{C \times \Delta V_{OUT}}{I_{MAX}} \times \frac{I_Q}{I_{MAX}}$$

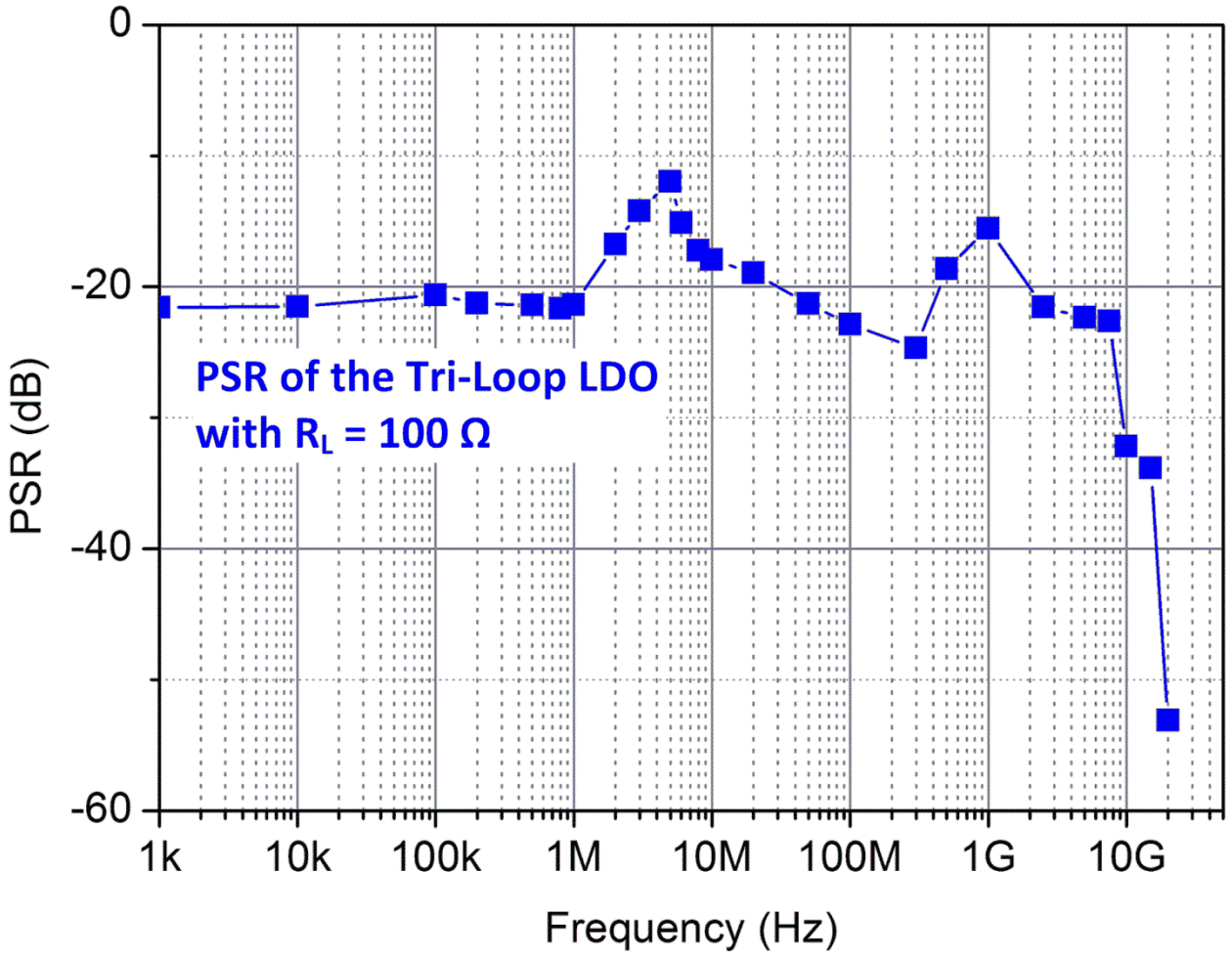
Measured PSR @ 5MHz and 1GHz

- V_{IN} = 1.2V, V_{OUT} = 1.0V, R_L = 100Ω

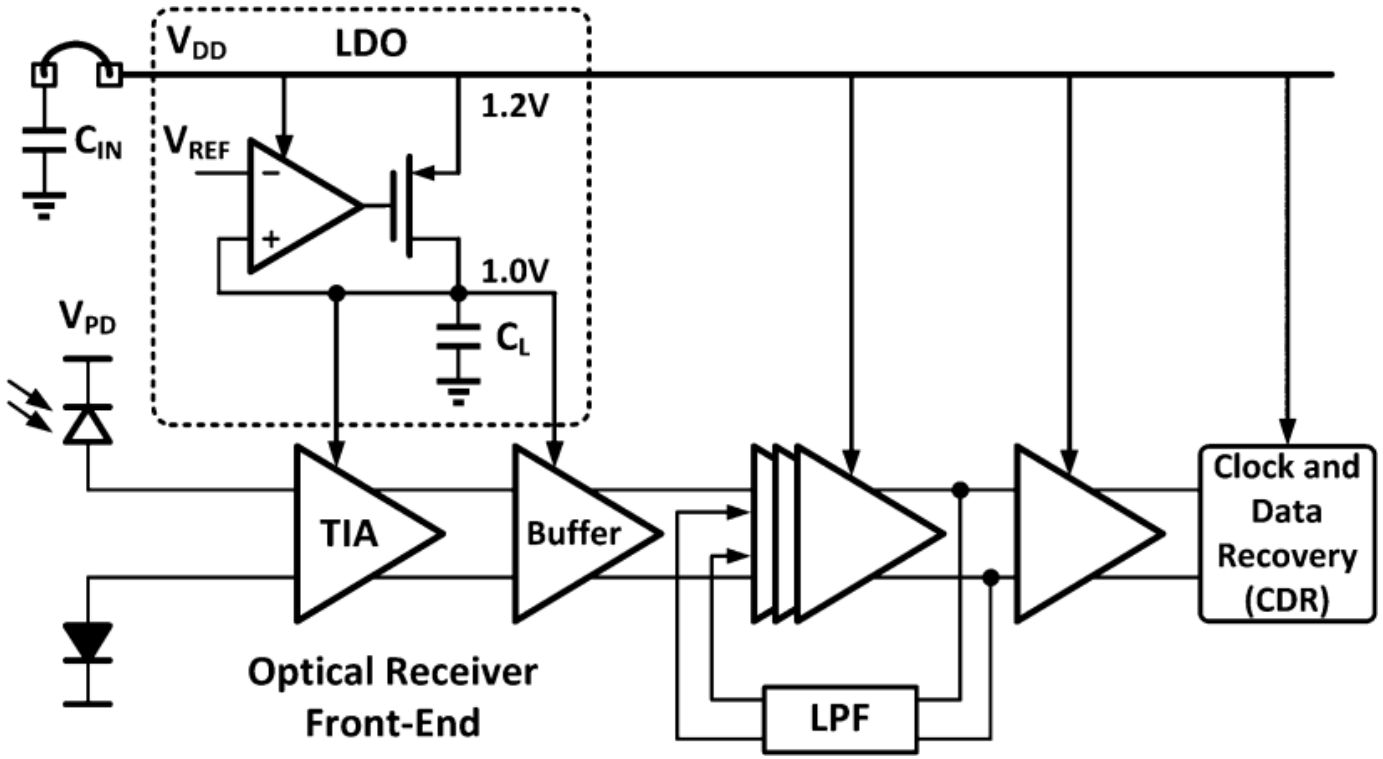


Measured PSR up to 20GHz

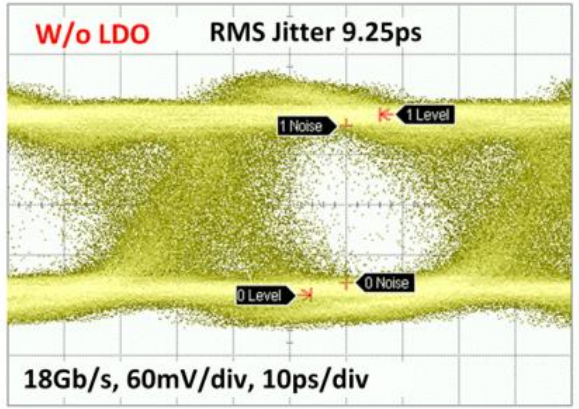
- V_{IN} = 1.2V, V_{OUT} = 1.0V, R_L = 100Ω
- -21.4dB @ 1MHz
- -12dB @ 5MHz
- -15.5dB @ 1GHz



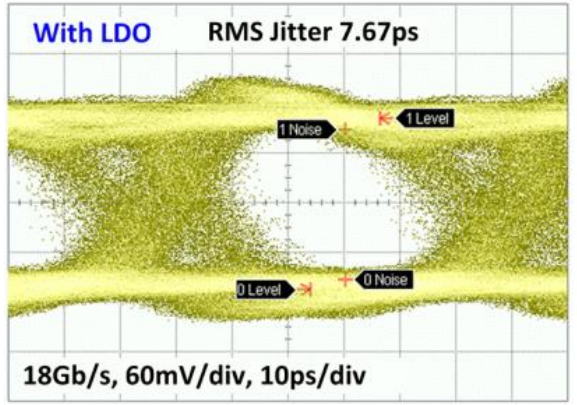
Optical Measurement Comparison



- On-chip LDO provides a clean supply for TIA



- Measured eye diagram without LDO



- Measured eye diagram with LDO

Comparison of State-of-the-Art LDOs

Publication	P. Hazucha JSSC 05'	J. Guo JSSC 10'	J. Bulzacchelli JSSC 12'	This Work
Output Cap.	**On-chip**			
Technology	90nm	90nm	45nm SOI	**65nm**
V_{OUT}	0.9V	0.5 to 1V	0.9 to 1.1V	**1V**
Drop out	300mV	200mV	85mV	**150mV**
I_Q	6mA	8μA	12mA	**50μA**
Io,max	100mA	100mA	42mA	**10mA**
Capacitance	600pF	50pF	1.46nF	**140pF**
PSR	N/A	0dB @1MHz	N/A	**-15.5dB @ 1GHz**
ΔV_{OUT} @T_{edge}	90mV @100ps	114mV @100ns	N/A	**43mV @200ps**
Load Reg.	90mV	10mV	3.5mV	**11mV**
T_R	0.54ns	N/A	0.288ns*	**0.6ns**
FOM	32ps	N/A	62.4ps*	**3.01fs**

*Simulated result

Outline

- Motivation
  - Electrical vs Optical Link
- RX Architecture
  - Wireline vs Optical Receiver
  - ADC-Based Receiver
- Circuit Implementations
  - PD Interface
  - Multi-peaking TIA
  - Modified Cherry-Hooper Amplifier
  - FFE and DFE Implementation
- Practical Issue
  - On-Chip LDO for Improved Sensitivity
- **Conclusion**

Conclusion

- Electrical reach is limited by a few meters, and it is getting shorter as data rates keep growing, and the transition to optical I/O links is beginning
- CMOS ADC-based receivers enable powerful digital equalization and symbol detection techniques for high data rate operation over electrical and optical wireline channels
- Multiple inductive peaking scheme and cascaded multi-stage CTLE can be used to achieve high gain of the TIA with high bandwidth
- FFE and DFE can be used to compensate for the residual ISI of the TIA
- By using a fully integrated LDO and on-chip filter for PD bias, the TIA jitters can be reduced for better sensitivity

Rx Reference (OWL)

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- Dr. PAN Quan's Thesis: Optoelectronic Receivers in Standard CMOS for Short-Range Optical Communications

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Clock and Data Recovery and Clock Generation
时钟数据恢复及时钟产生电路

Prof. C. Patrick Yue 俞捷教授

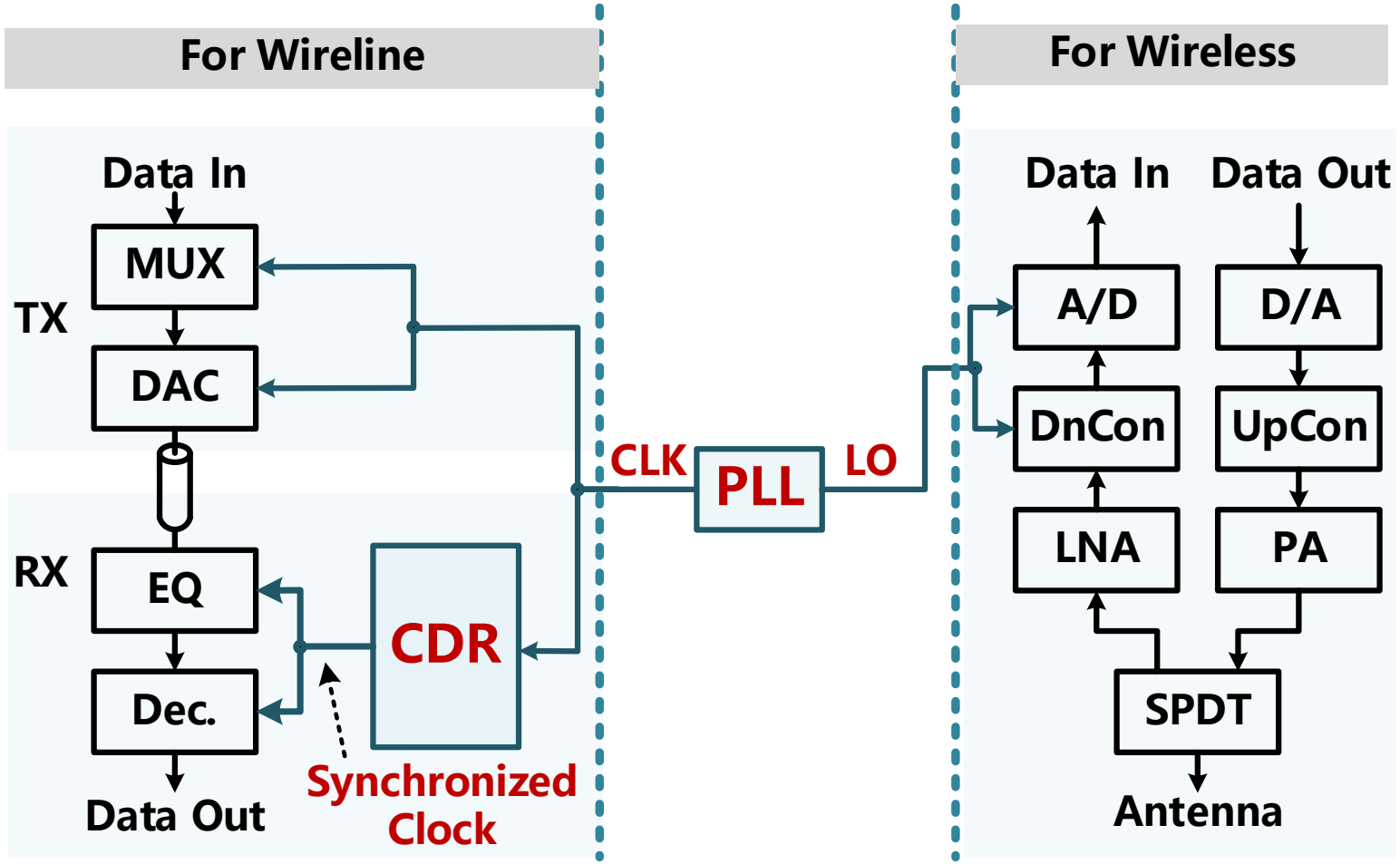
芯动力人才计划®第 125 期国际名家讲堂

Outline-Clock and Data Recovery and Clock Generation

- Architecture
  - Overview of CDR and PLL Loop Configuration
  - Why Single Loop? How to Achieve Wide Capture Range Via Single Loop
  - Why Dual Loop? Cascaded or Parallel? How Loop Parameters Are Determined
  - Why Dual Path? Decoupling JTRAN and JTOL
- Key Circuits
  - PAM-n PD (Github: Jabdekhoda (github.com))
  - VCO (Github: HKUST-OWL-WANG-Li/A-20-24-GHz-Class-C-VCO-with-186-dB-FoM (github.com))
  - AC-Coupled Sub-Sampling Charge Pump
  - R2R Comparator (Github: Jabdekhoda (github.com))

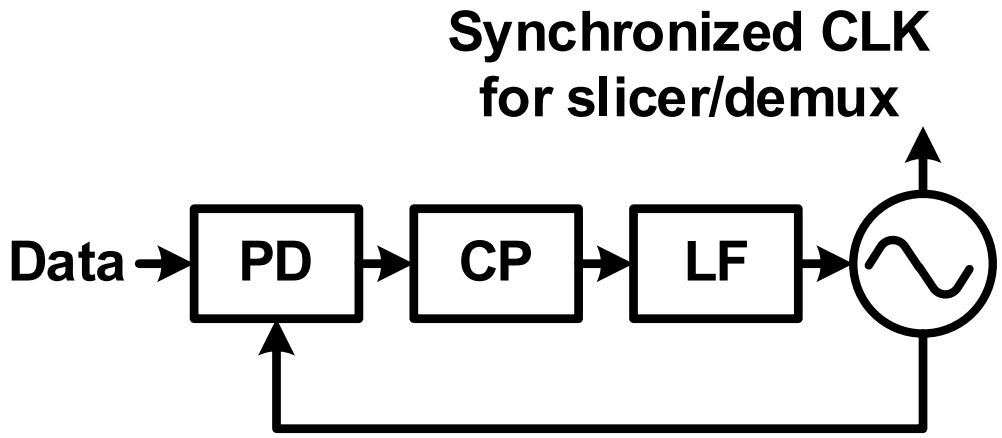
A General Overview of CDR/PLL

- PLL and CDR: Key building blocks in both wireline and wireless transceivers

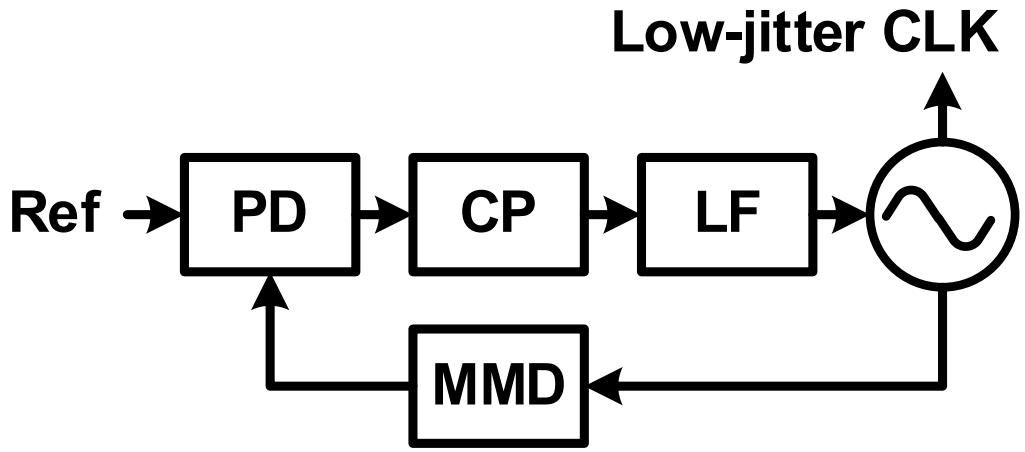


Why Single Loop

- Basic configuration:



Single-Loop CDR



Single-Loop PLL

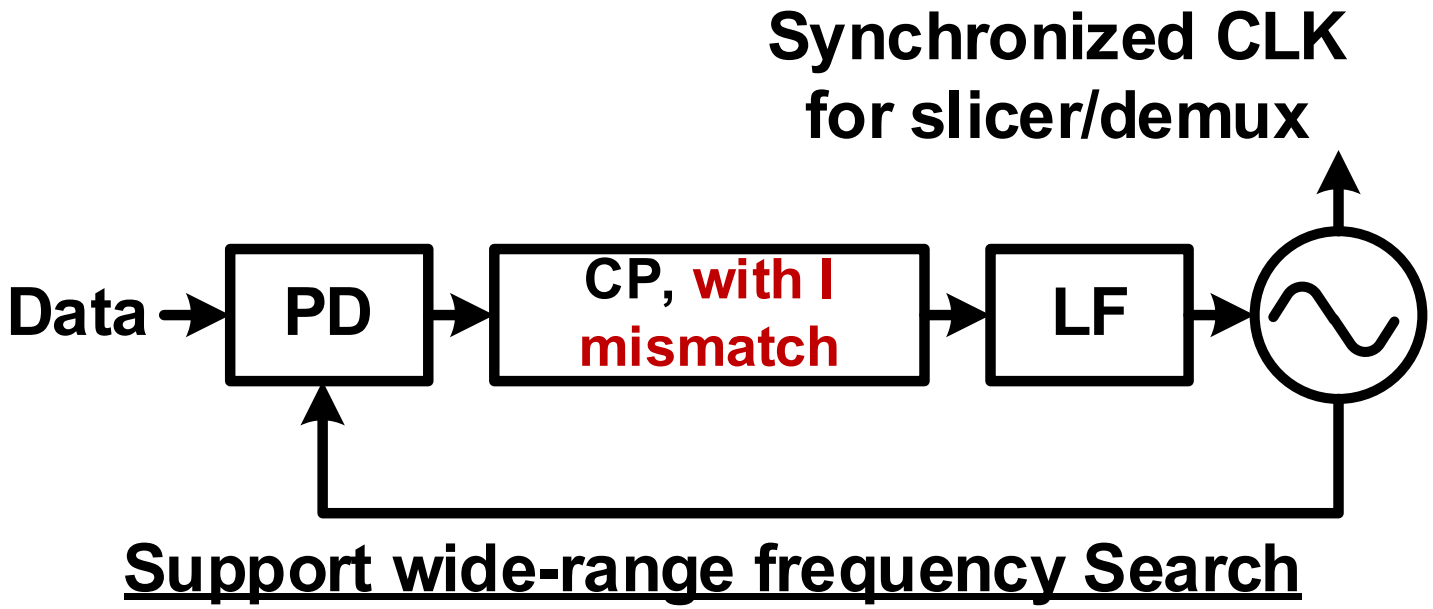
- Advantages: Concise and Low-cost
  - Simple circuit provides the best robustness, generally.

Beyond Single Loop Configuration

- But What If…
  - At high frequency (28 GHz, the quarter-rate clock for 200 GBE), the **VCO phase noise** is huge, limited by bad L-C tank quality factor, but a **low jitter clock** is still expected?
  - The CDR loop bandwidth is narrow, but a **wide frequency capture range** is needed?
  - In cascaded retimer, the jitter tracking in each stage causes **jitter accumulation**, and needs to be attenuated for better signal quality?

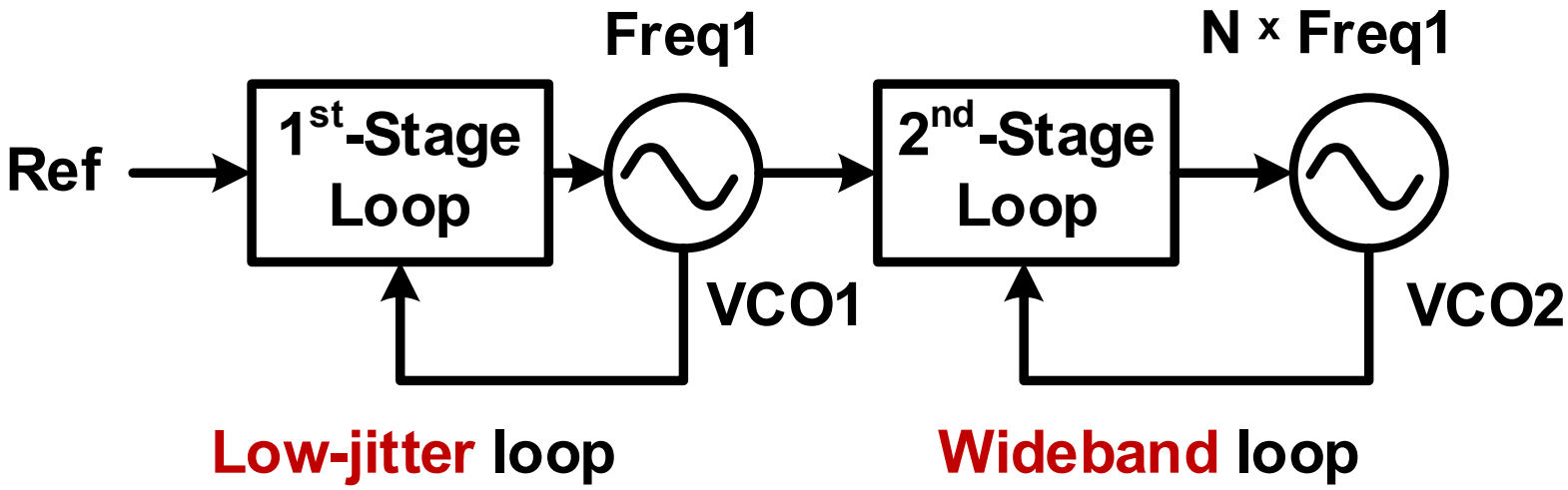
How A Single-Loop Achieves Wide Capture Range

- **A single loop with deliberate current mismatch in CP**: allows the single loop to cover a wide frequency capture range
  - The offset current drives the loop filter voltage, to **search** through the VCO tuning range



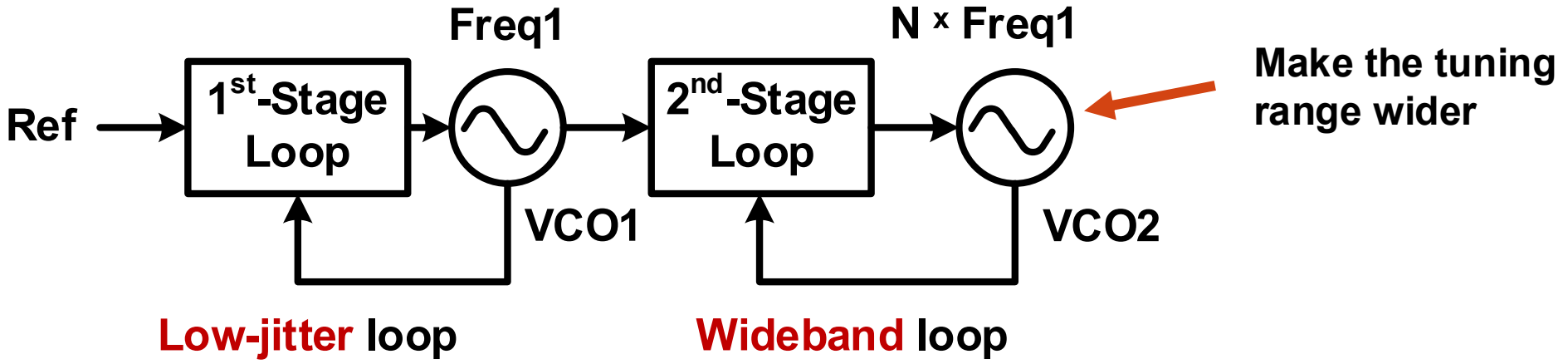
One More Loop? Cascaded or Parallel?

- **Cascaded two loop**: **One for low jitter, one for wideband**
- **How?**
  - First-stage **low jitter loop**: operating at sub-10-GHz Freq1, high-Q L-C tank
  - Second-stage **wideband** loop: operating at N×Freq1, high frequency loop, the wide bandwidth sufficiently attenuate the high-freq VCO phase noise



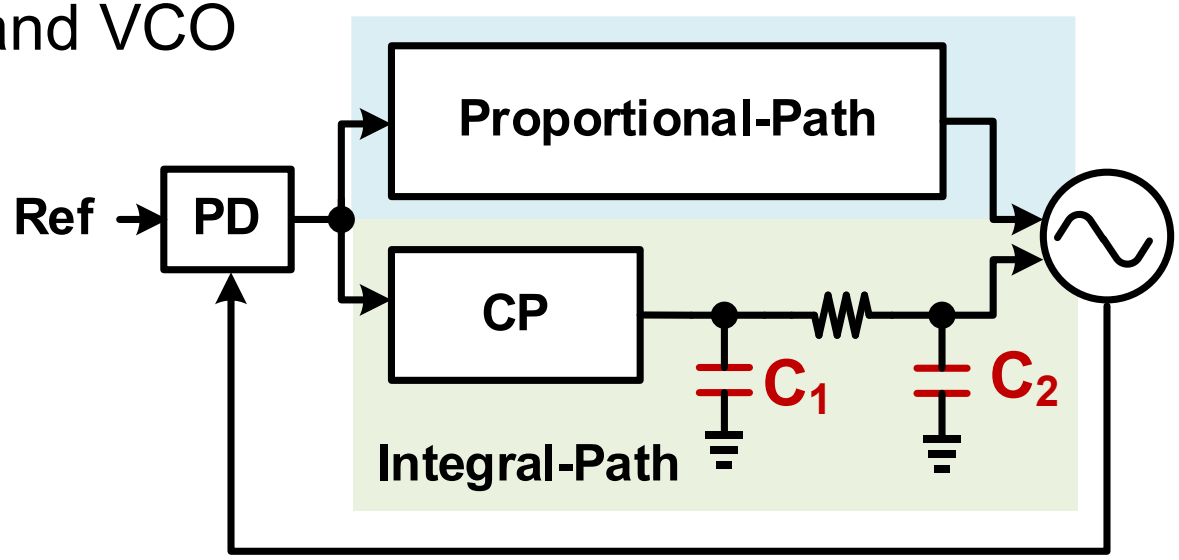
One More Loop? Cascaded or Parallel?

- **Disadvantage: cascaded two loop** provide narrow **tuning range**
  - Only then overlap portion between the two VCO's tuning range can be utilized for the overall PLL
- **Possible Solution:**
  - Design the second stage to have much wider tuning range than the first state
  - Why? The second stage does not suffer from tuning range-jitter tradeoff, **thanks to the wideband**



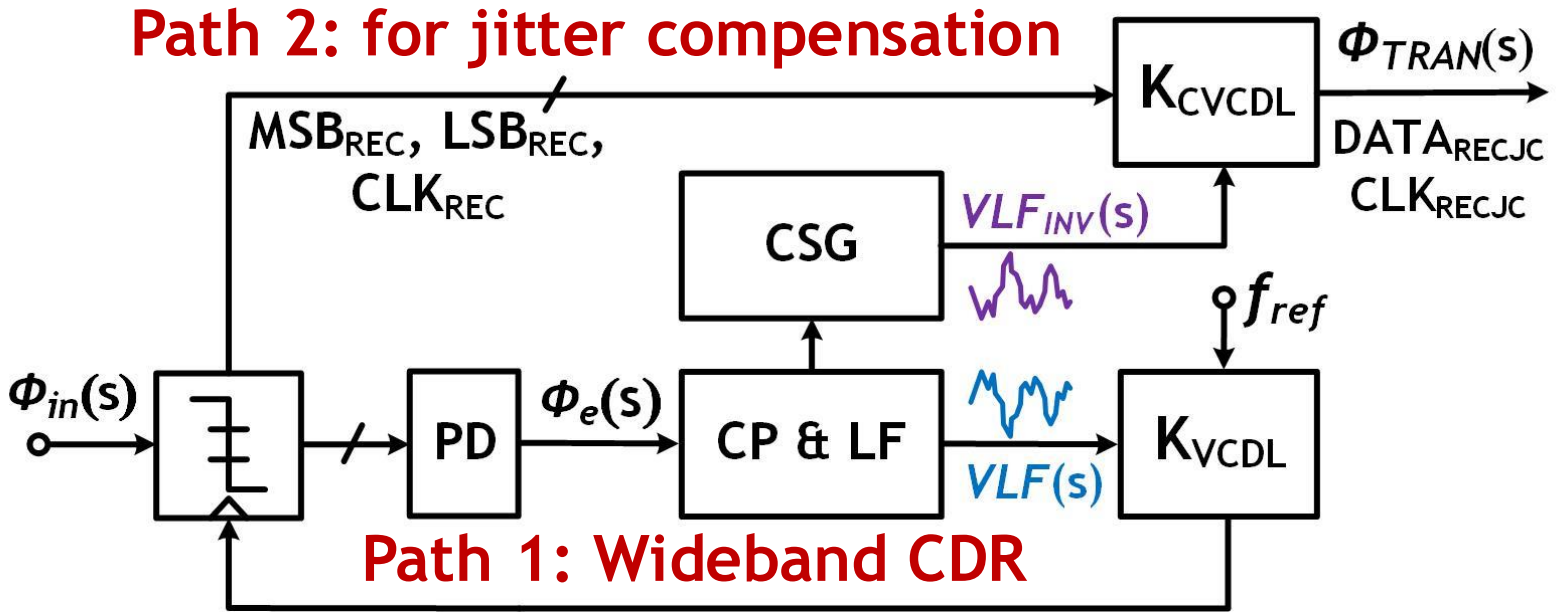
One More Loop? Cascaded or Parallel?

- **Parallel Two Loop**: **one for tracking frequency , one for tracking phase (& phase noise)**
- **How?**
  - **Integral path (I-Path):** ultra narrow bandwidth with little jitter contribution, just to capture the frequency error
  - **Proportional path (P-Path):** Optimal bandwidth with balanced jitter, balance the jitter from reference and VCO



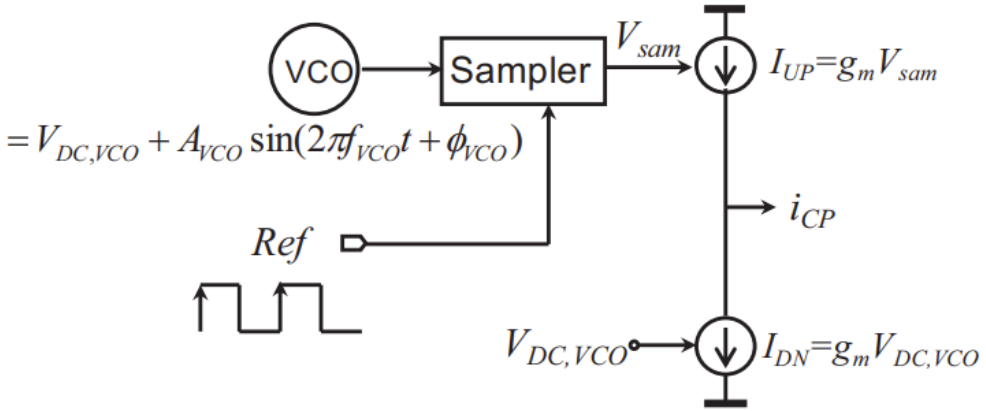
One More Loop? Dual Path

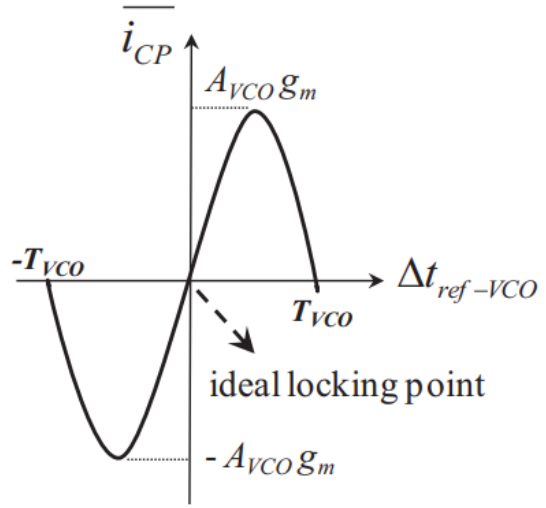
- **Dual Path**: **one loop for wideband JTOL, one path for jitter attenuation**
- **How?**
  - **Path 1**: a wideband CDR for wideband jitter tolerance
  - **Path 2**: jitter compensation path to attenuate the jitter transfer

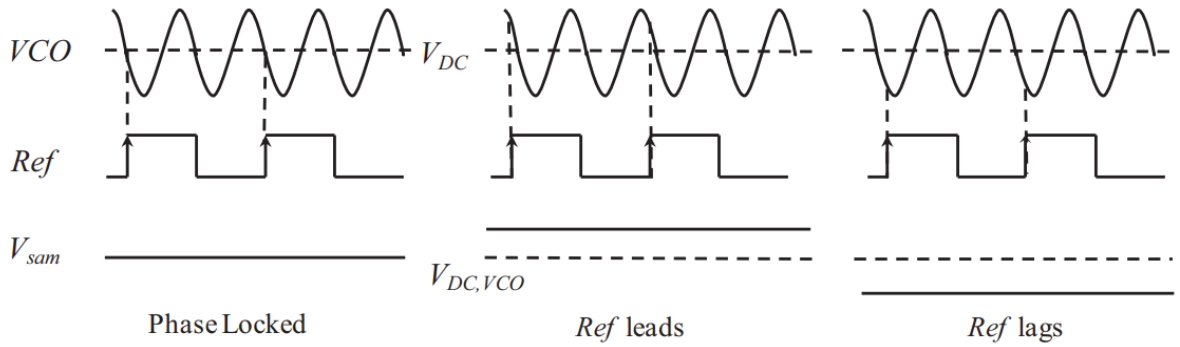


Subsampling

- Subsampling
  - Main feature: large gain
  - Reduce the contribution from other noise sources
  - Such as: charge pump, loop filter, or divider.







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  - R2R Comparator (GitHub Link by Johar)

香港科技大學
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HKUST OWL

An Improved Single Path Architecture:
For Wide-Capture-Range Clock and Data Recovery Circuit

模擬與混合信號超大規模集成電路
國家重點實驗室
State Key Laboratory of
Analog and Mixed-Signal VLSI

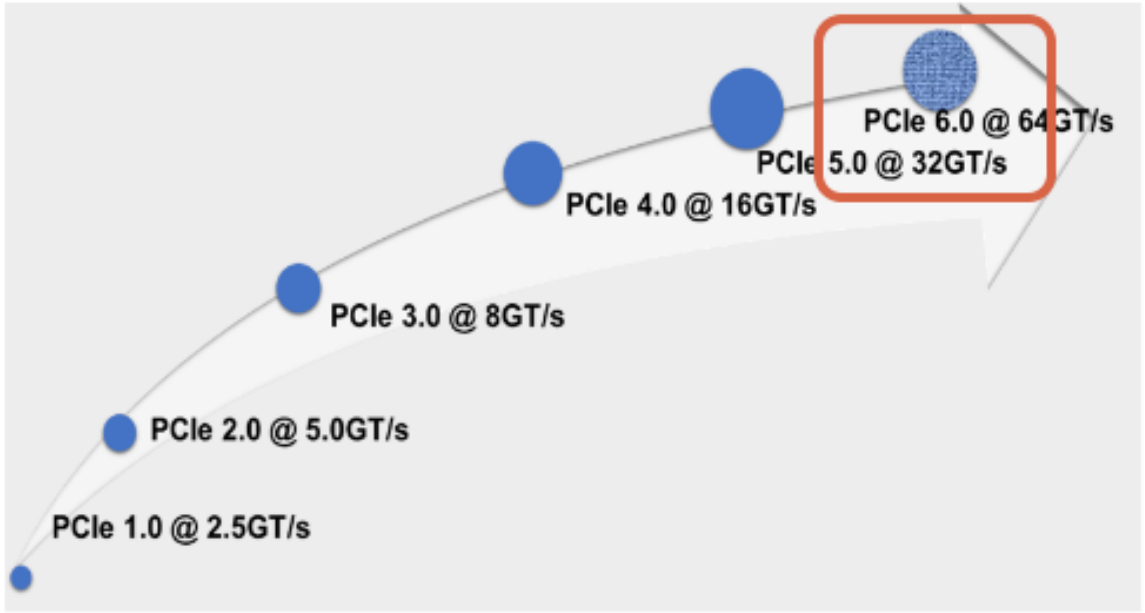
Outline

- Motivation
- Design Example 1
- Design Example 2
- Conclusion

Outline

- **Motivation**
- Design Example 1
- Design Example 2
- Conclusion

Design Motivation: Industry Standards

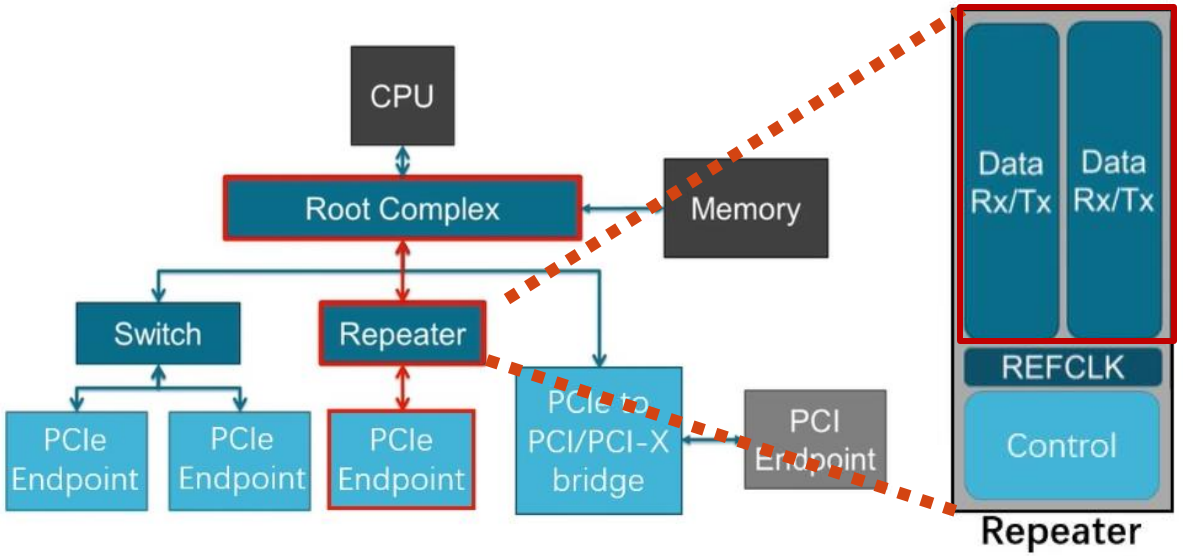


PCIe Specification	Data Rate(Gb/s) (Encoding)	x16 B/W per dirn*	Year
1.0	2.5 (8b/10b)	32 Gb/s	2003
2.0	5.0 (8b/10b)	64 Gb/s	2007
3.0	8.0 (128b/130b)	126 Gb/s	2010
4.0	16.0 (128b/130b)	252 Gb/s	2017
5.0	32.0 (128b/130b)	504 Gb/s	2019
6.0	64.0 (PAM-4, Flit)	1024 Gb/s (~1Tb/s)	2021

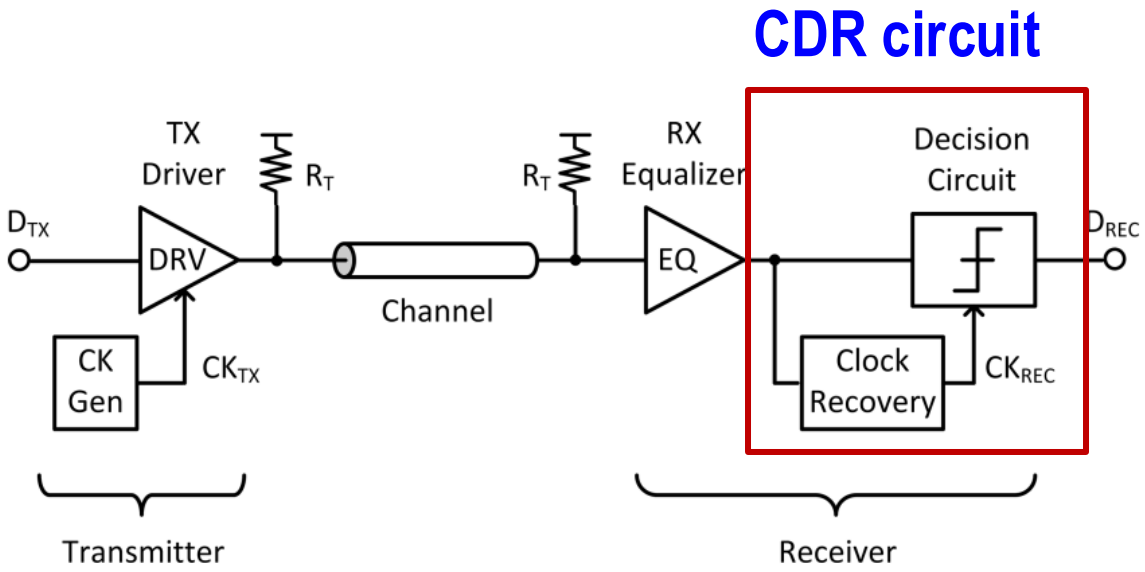
* - bandwidth after encoding overhead

- The rapid increment in data transport volume has pushed the development of the wireless/wireline communication system
- Several industry standards has been proposed for wired communication I/O interface: OIF CEI-56G/112G/224G and PCIe 6.0
- Each new generation of the standard has seen a doubling in the data rate (higher speed and lower power consumption)

Design Motivation: PCI Express-Rx Application



Signal transmission in PCIe

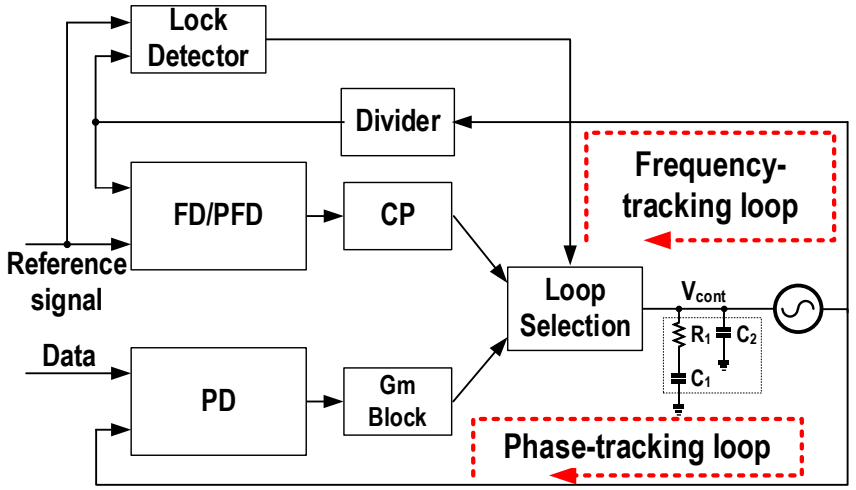


Block diagram of a wireline transceiver

- Repeater for redrive (signal equalization) and retime (clock and data recovery)
- The CDR circuit plays a key role in wireline data transport

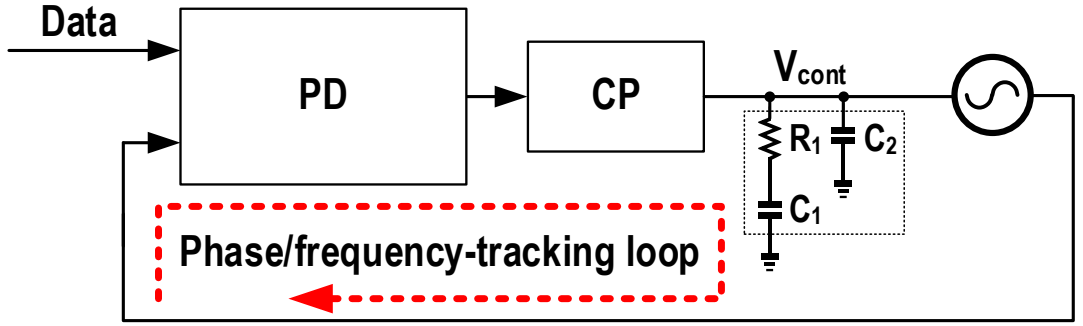
Design Motivation:
From Dual-Loop to Single-Loop CDR

Dual-Loop CDR with External Reference



- ✗ Complex structure
- ✗ High hardware cost
- ✗ Possibility to introduce undesired couple

Single-Loop Reference-Less CDR

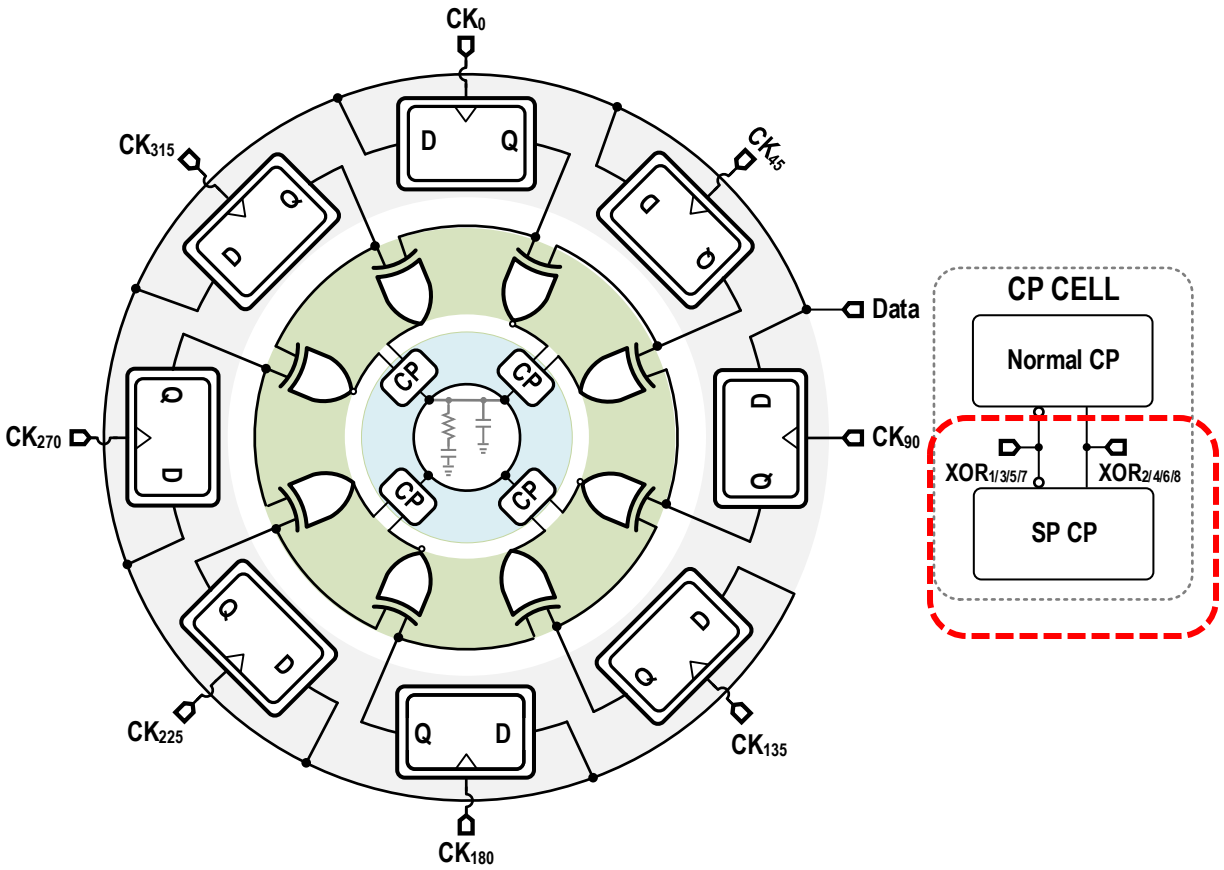


- ✓ Concise structure (single loop)
- ✓ Low hardware cost (single loop)
- ✓ Avoid nonideal couple from reference clock (reference-less)
- ✓ Flexibility to meet multi-standard application (wide capture range)

Outline

- Motivation
- **Design Example 1: A 10.8-to-37.4Gb/s Reference-Less FD-Less Single-Loop Quarter-Rate Bang-Bang Clock and Data Recovery Employing Deliberate-Current-Mismatch Wide-Frequency Acquisition Technique**
- Design Example 2
- Conclusion

Design 1: Proposed Quarter-Rate BBPD with FD

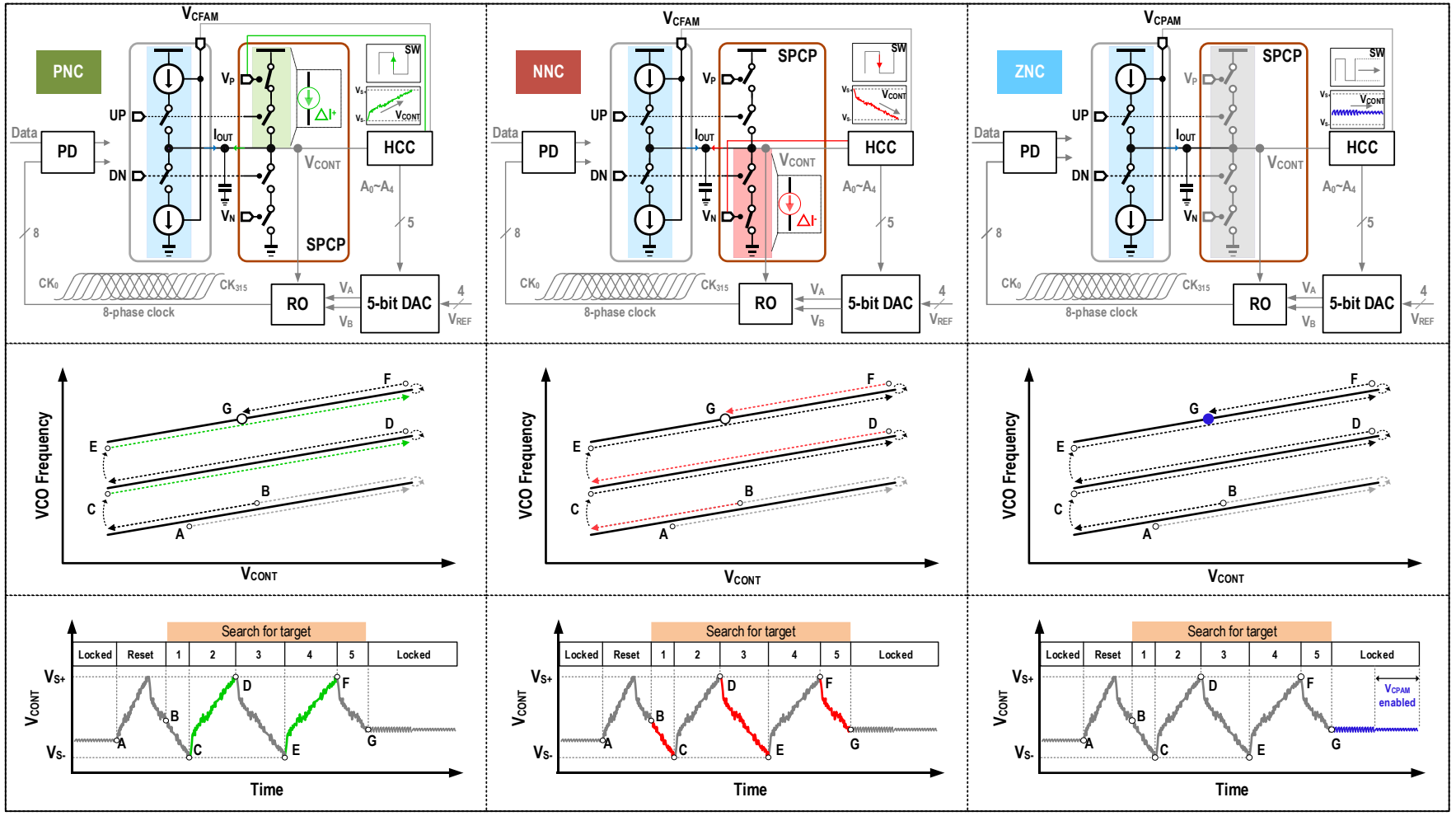


BBPD with modified CP

Main features

- Motivated by 8-phase clock to achieve quarter-rate sampling
- Extra tunable strobe point (SP) CP pairs are deliberately inserted for FD function
- $F_{Data} > 4F_{VCO}$ → CP offers a positive net current;
- $F_{Data} < 4F_{VCO}$ → CP offers a negative net current

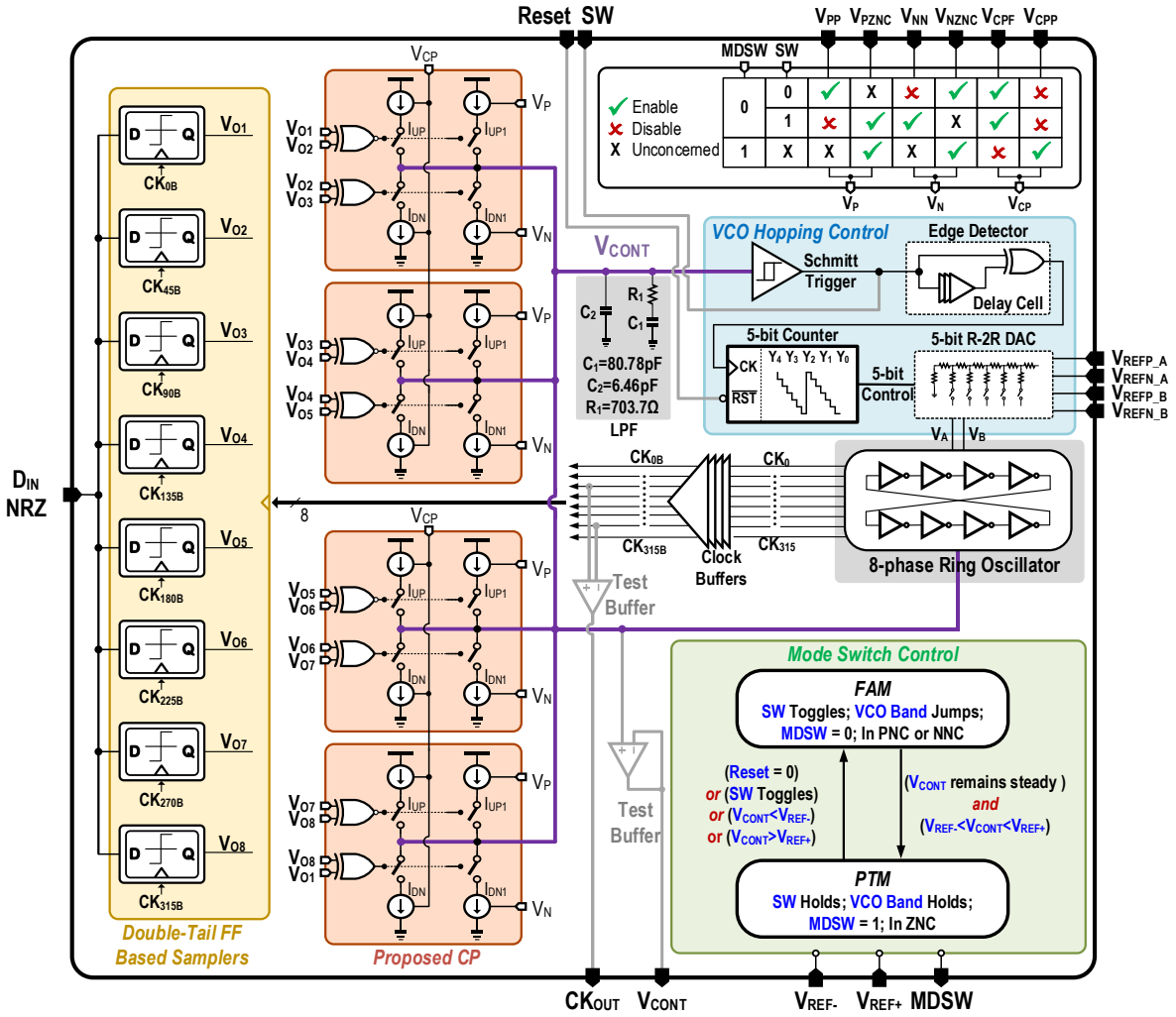
Design 1: Timing Diagram of Proposed BBPD



1. **VCO lag ($4f_{VCO} < f_{data}$):** SP CP operates as a current source and offer positive net current **(PNC)**
2. **VCO lead ($4f_{VCO} > f_{data}$):** SP CP works as a current outfall and offer negative net current **(NNC).**
3. **No frequency error:** SP CP is disabled and offer a zero net current **(ZNC)**

Illustration of operation mechanism under different mode

Design 1: Top Architecture of Proposed BBCDR

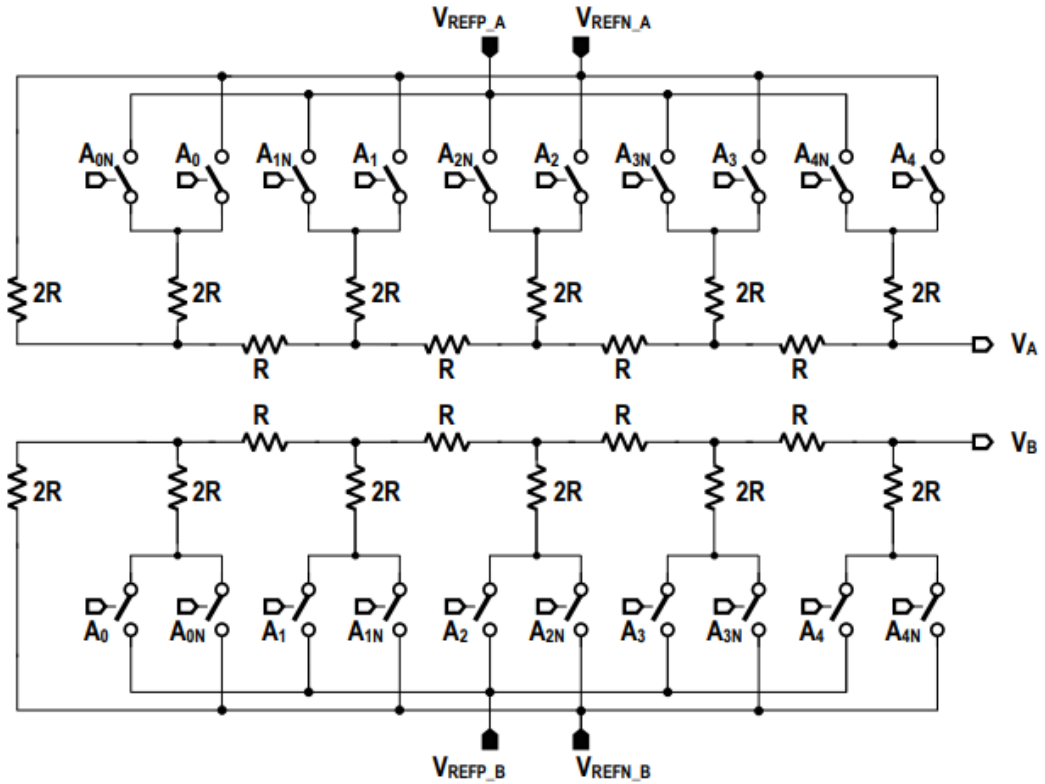


Top architecture

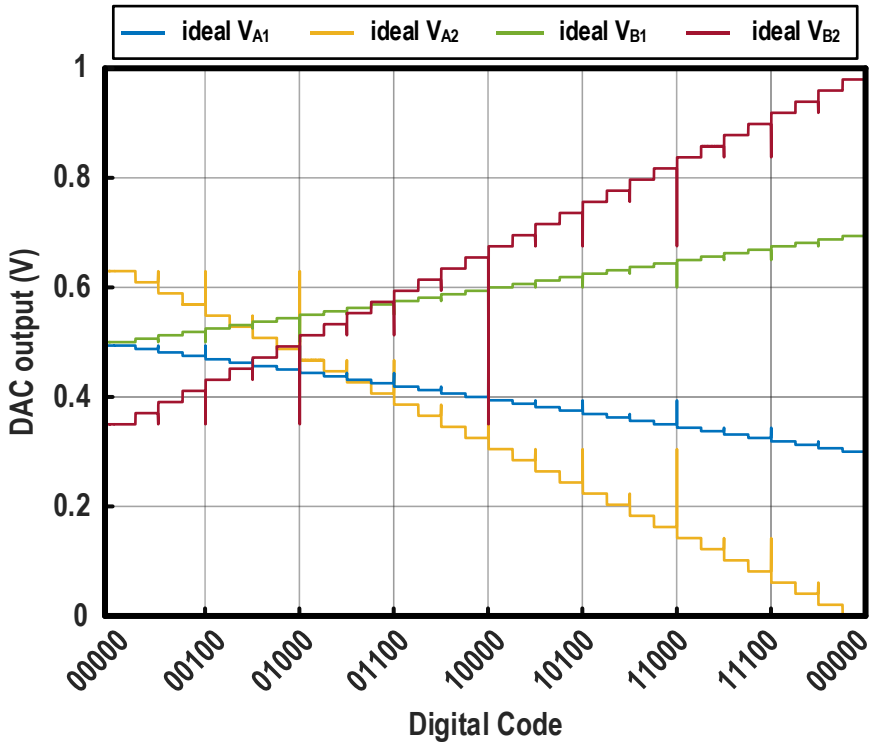
Main Block:

- Quarter-rate BBPD (for phase detection)
- Modified CP (for frequency locking)
- LPF (for control signal smoothing and bandwidth control)
- HCC (for mode switch and VCO band control)
- 5-bit RDAC (for VCO frequency control)
- 8-phase ring oscillator (for wide-tuning-range clock)

Design 1: 5-bit R-DAC



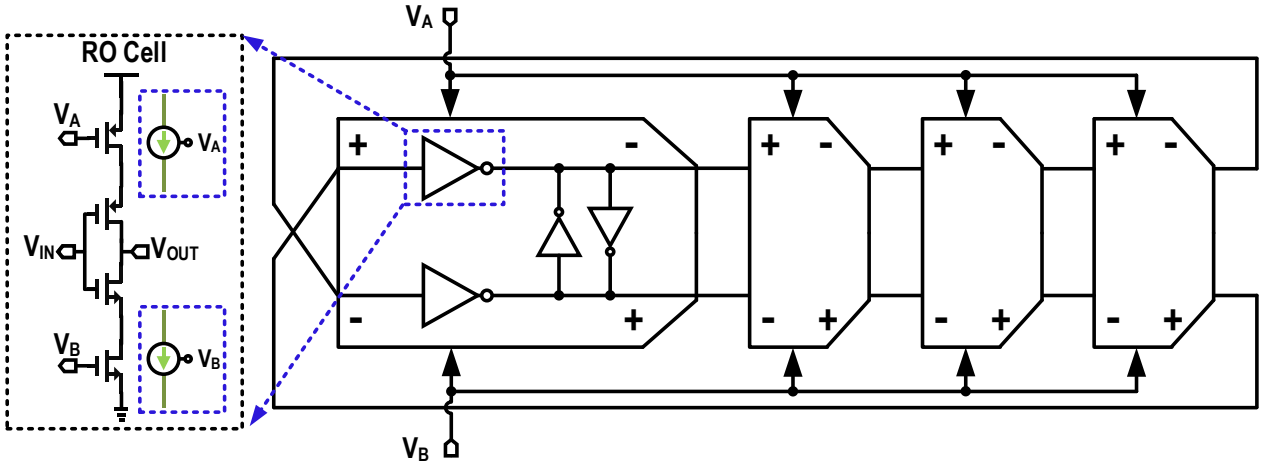
5-bit R-2R DAC



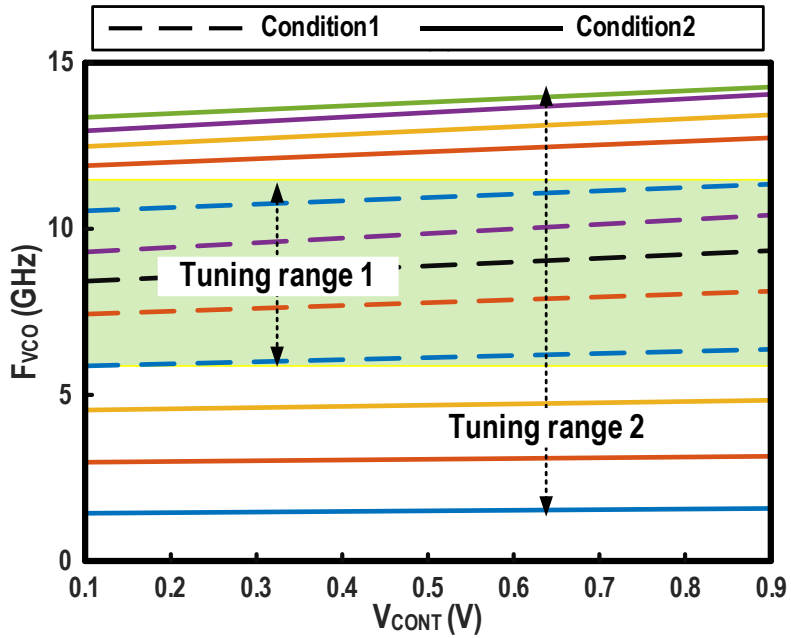
Simulated DAC output

1. Controlled by VCO band signal
2. Output varies between the upper and lower preset reference value

Design 1: 8-Phase Current-Starve Ring Oscillator



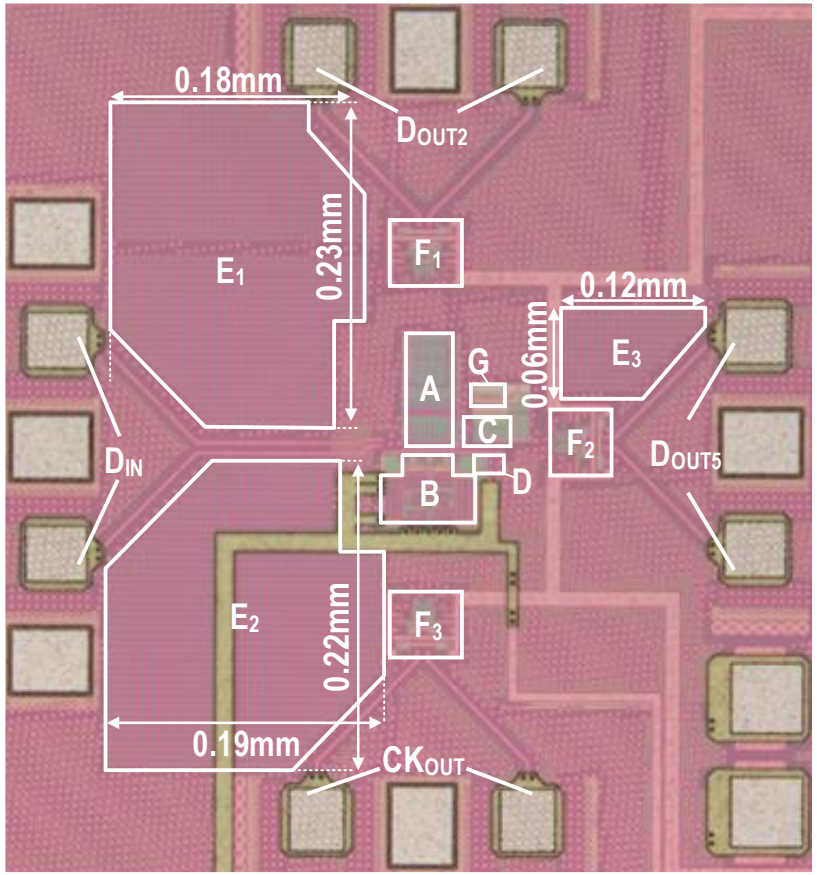
Current-starve ring oscillator



Tuning-range affected by external reference

- A current-starve based ring oscillator for a wide operating frequency
- The current strength directly controlled by the output of RDAC
- Entire tuning range is heavily affected by the external reference voltage of DAC

Design 1: Chip Photo and Area Breakdown



Chip Photo

Area Breakdown

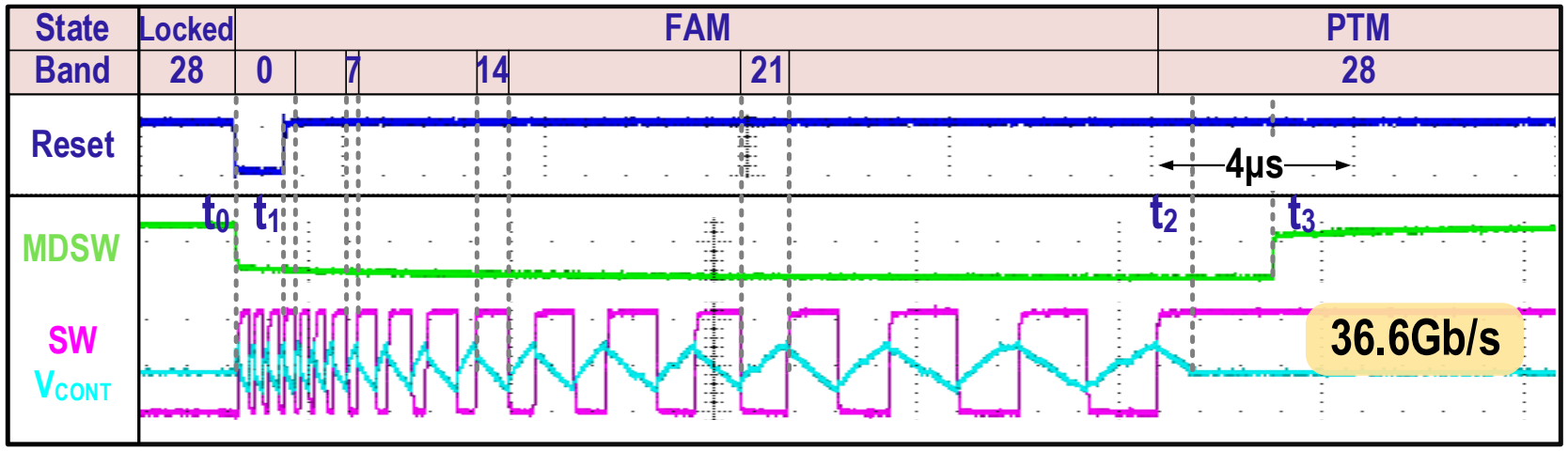
Main Circuits		Area	Auxiliary Circuits	
A	PD + CP+XOR	0.0026	F_1	D_{OUT2} Output Buffer
B	VCO	0.0035	F_2	D_{OUT5} Output Buffer
C	HCC	0.0005	F_3	Clock Output Buffer
D	DAC	0.0004	G	V_{CONT} Output Buffer
E	LPF	0.0757		
Total Core Area: 0.0827mm^2				

Power Breakdown

	Data Rate (Gb/s)	VCO (mW)	PD (mW)	CK Buffer (mW)	CP (mW)	HCC (mW)	Total Power (mW)	FOM (pJ/bit)
Band 0	10.8	16	2.29	1.54	1.98	0.63	22.4	2.08
Band 4	19.6	22.46	3.97	2.56	1.98	0.64	31.61	1.61
Band 12	29.8	29.6	5.58	3.5	1.92	0.72	41.32	1.39
Band 20	34.2	32.94	6.05	3.88	1.99	0.79	45.65	1.33
Band 28	36.6	34.7	6.13	4	1.99	0.79	47.61	1.30
Band 31	37.4	36	6.07	3.96	1.93	0.72	48.68	1.30

The current-starve oscillator consumes a large power at high operating speed

Design 1: Measured Dynamic Settling Process

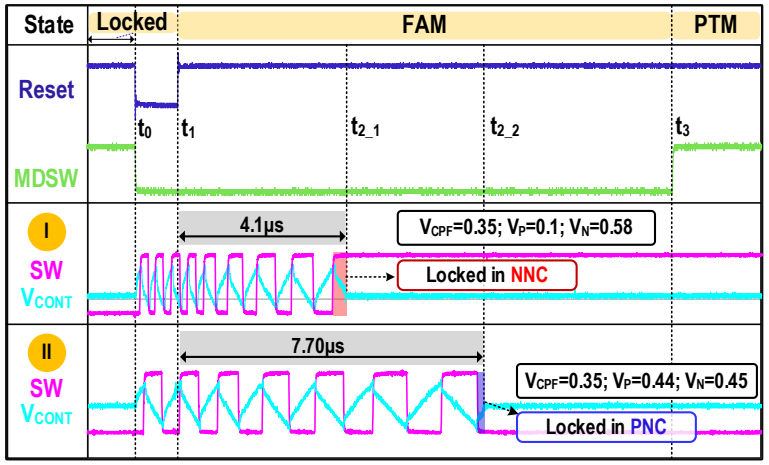


Measured HCC transient waveform

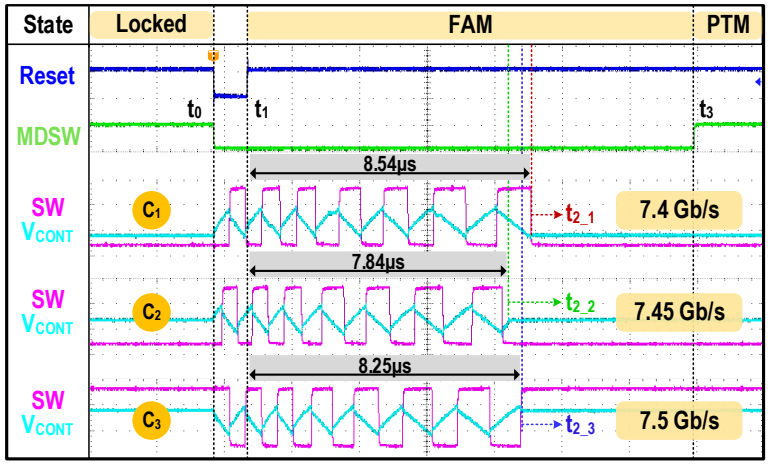
The loop operation :

- **At t_0 :** Reset signal is released
- **At t_1 :** frequency tracking mode (FAM) is released
- **At t_2 :** frequency is locked, and correct band is hunted
- **At t_3 :** phase tracking mode (PAM) is released for better jitter performance

Design 1: Measured Transient Waveforms and Spectrum

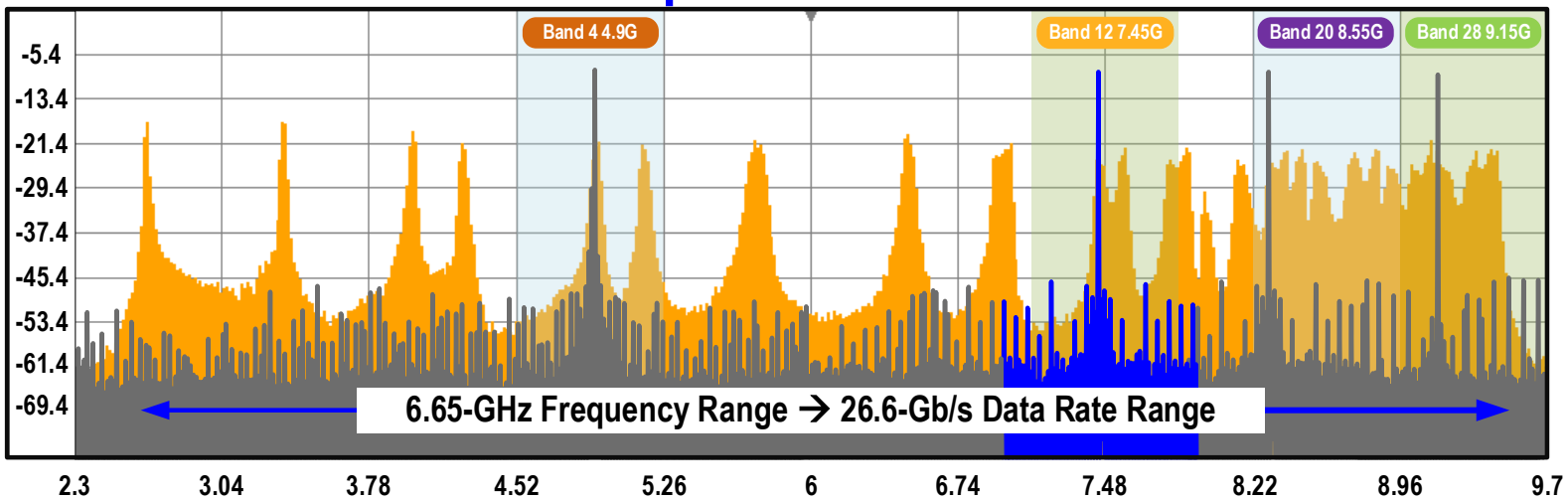


(a)



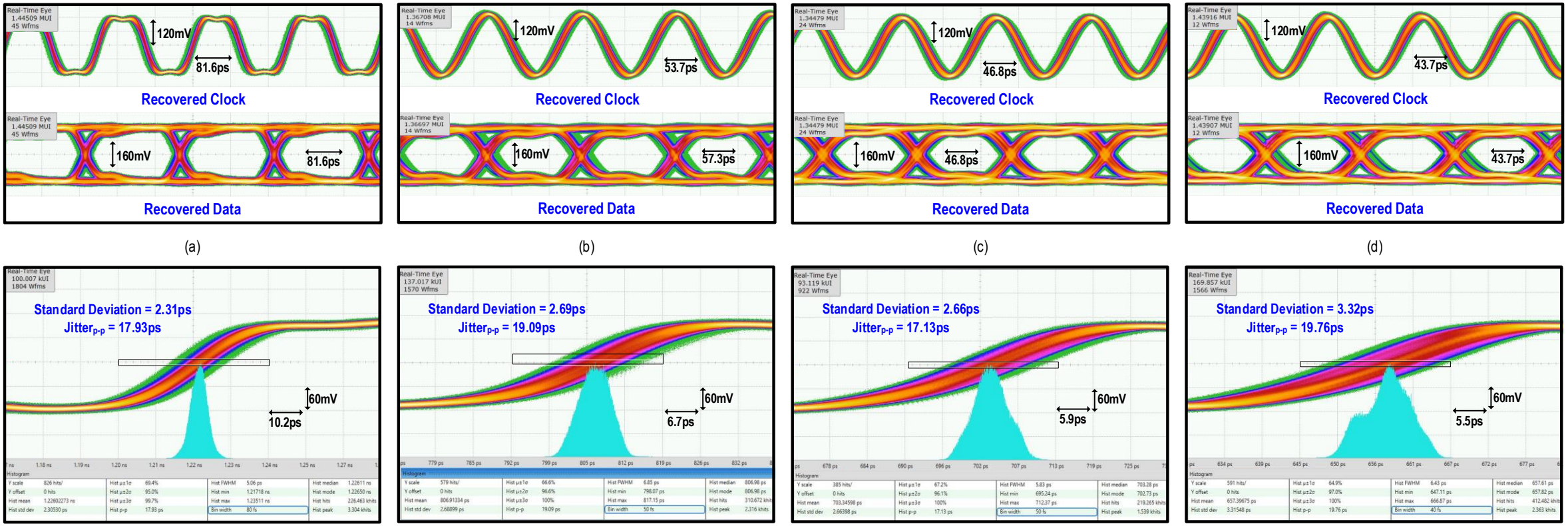
(b)

Measured waveforms when the loop locks in different sates and different V_{cont}



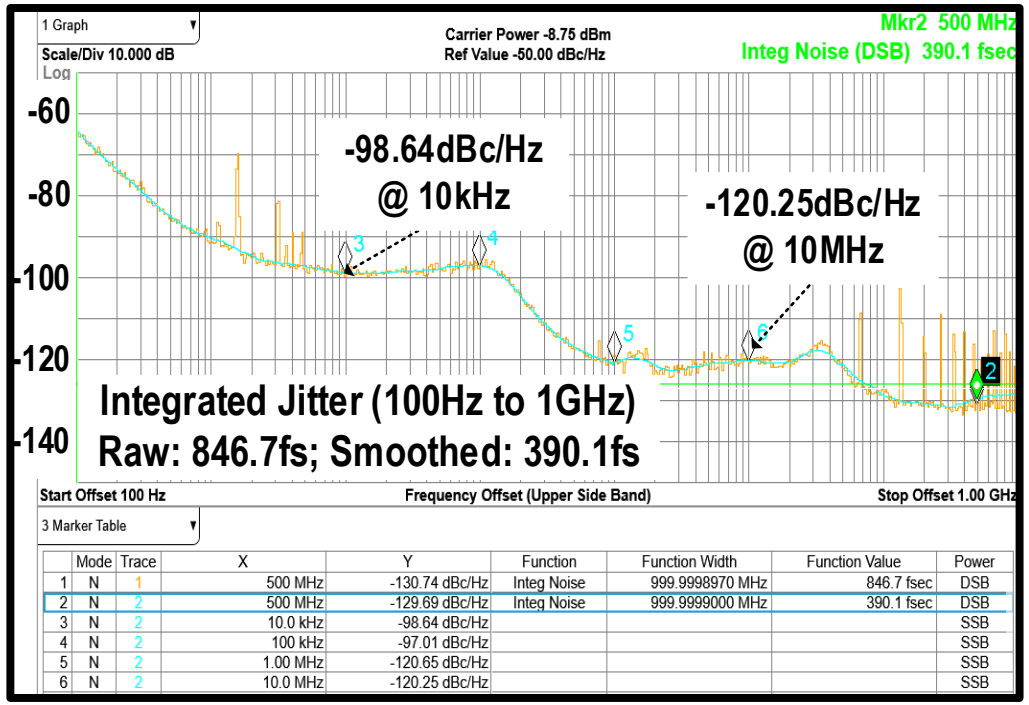
Measured overall spectra of the BBCDR's capture range

Design 1: Measured Eye Diagram and Histogram

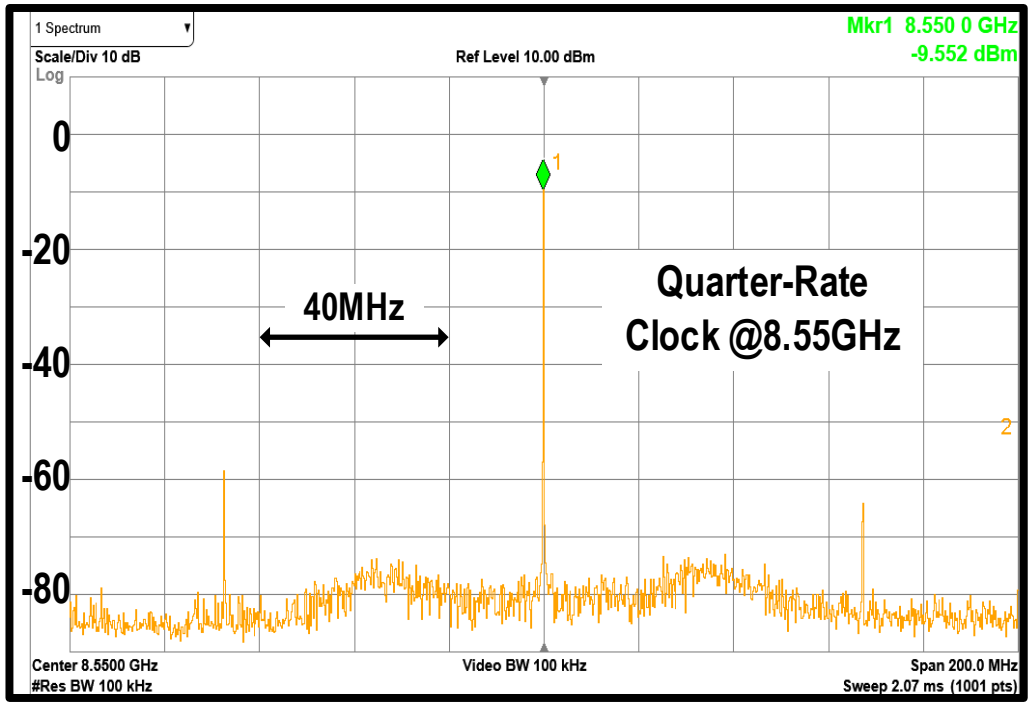


Eye diagram and histogram under multiple input data rates:
19.6Gb/s 29.8Gb/s 34.2Gb/s and 36.6Gb/s separately

Design 1: Measured Phase Noise (PN) of Recovered Clock

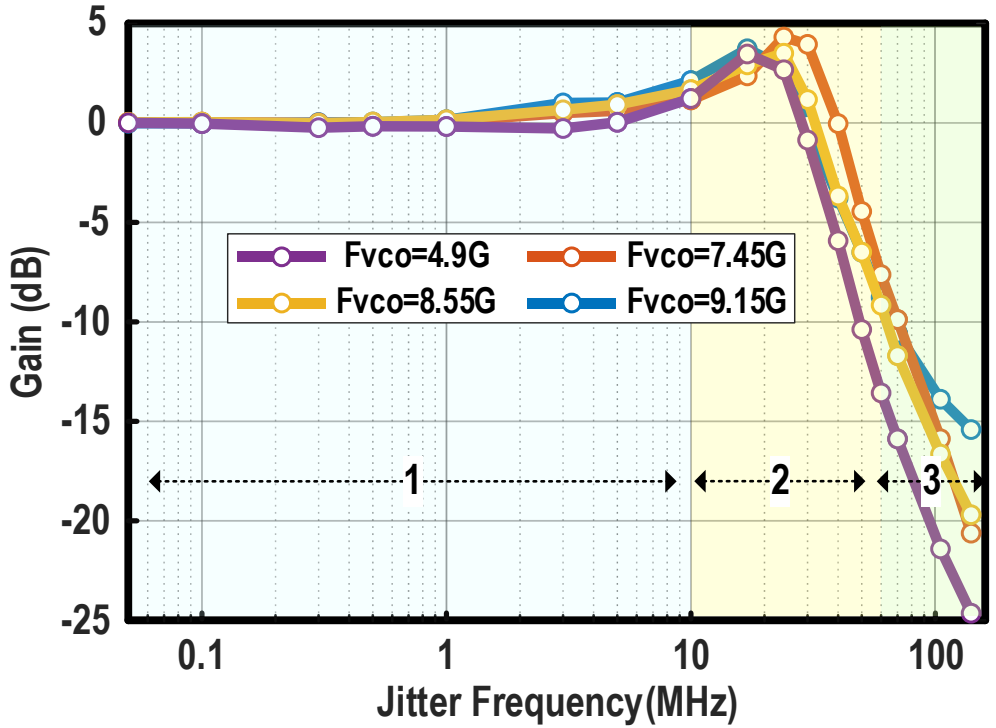


Measured integrated jitter

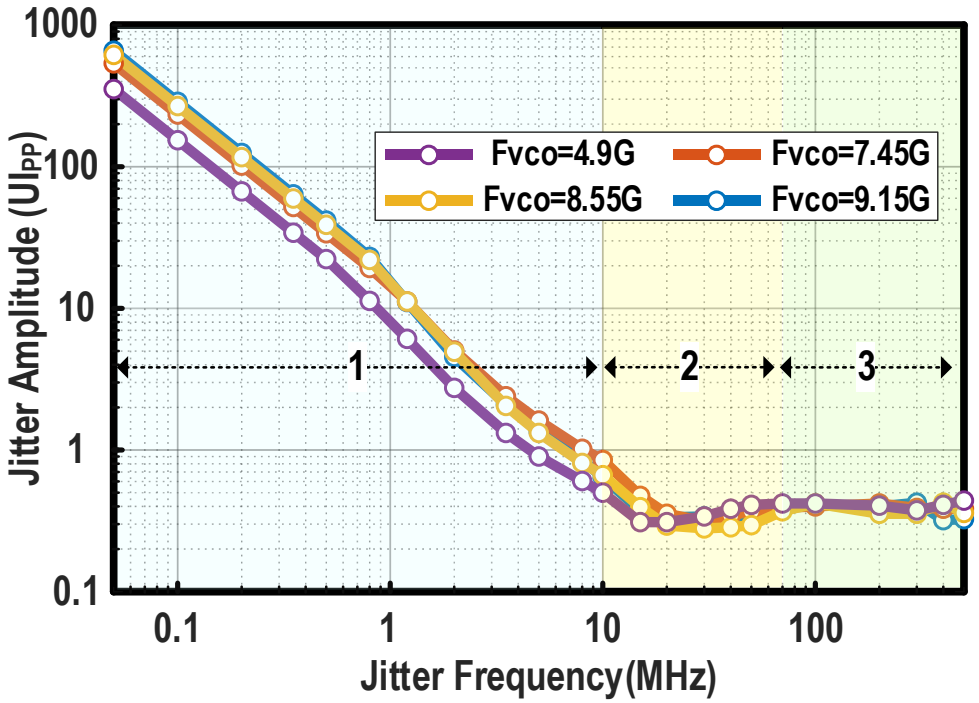


Measured spectrum at 8.55 GHz

Design 1: Measured JTF and JTOL Curves

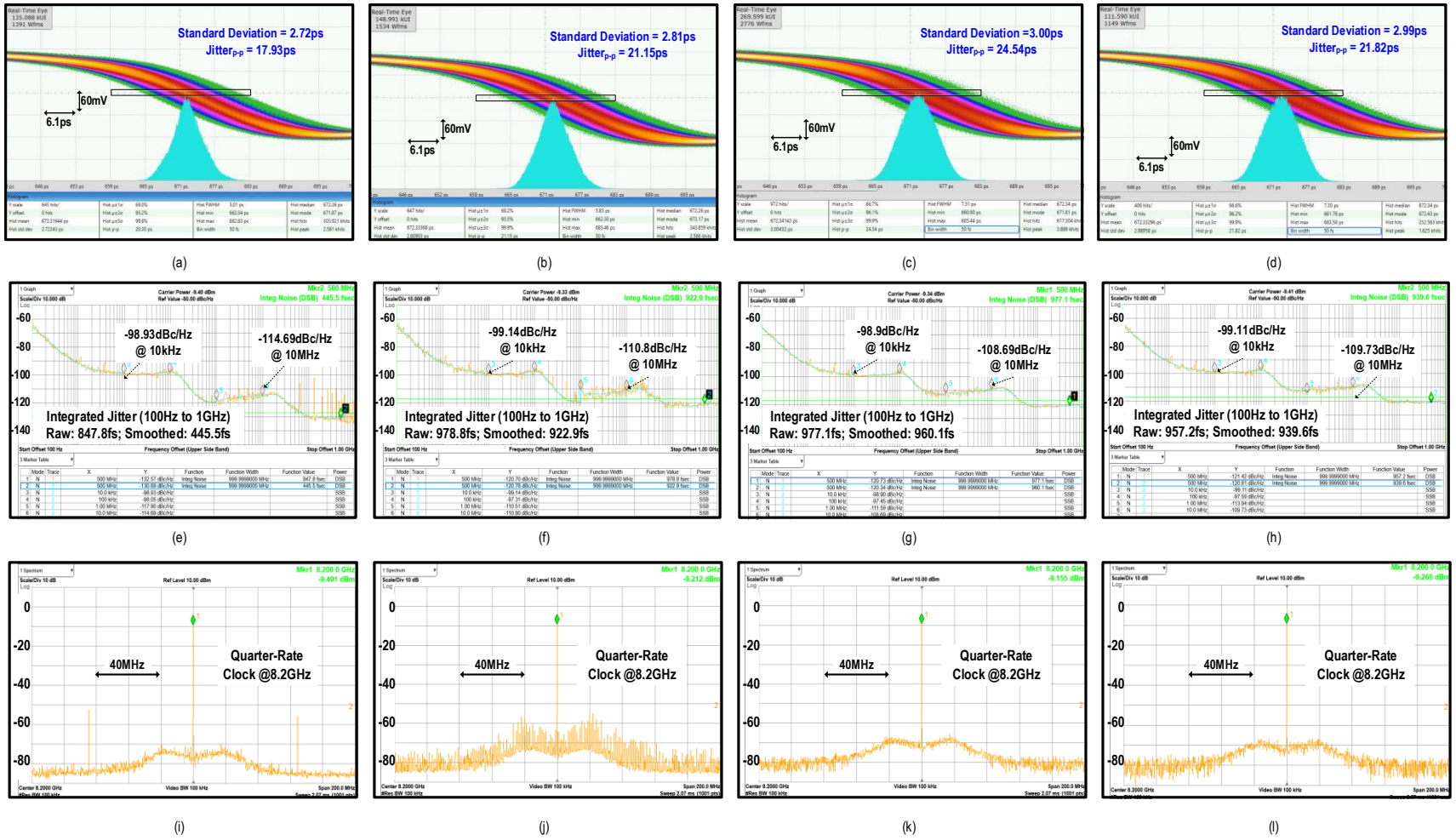


Measured jitter transfer function with 0.1-UI_{PP} input jitter



Measured jitter tolerance curve with BERT

Design 1: Measured Results Under Different Data Patterns



$PRBS2^{7}-1$ **$PRBS2^{15}-1$** **$PRBS2^{23}-1$** **$PRBS2^{31}-1$**

Design 1: Summary and Comparison with Prior Arts

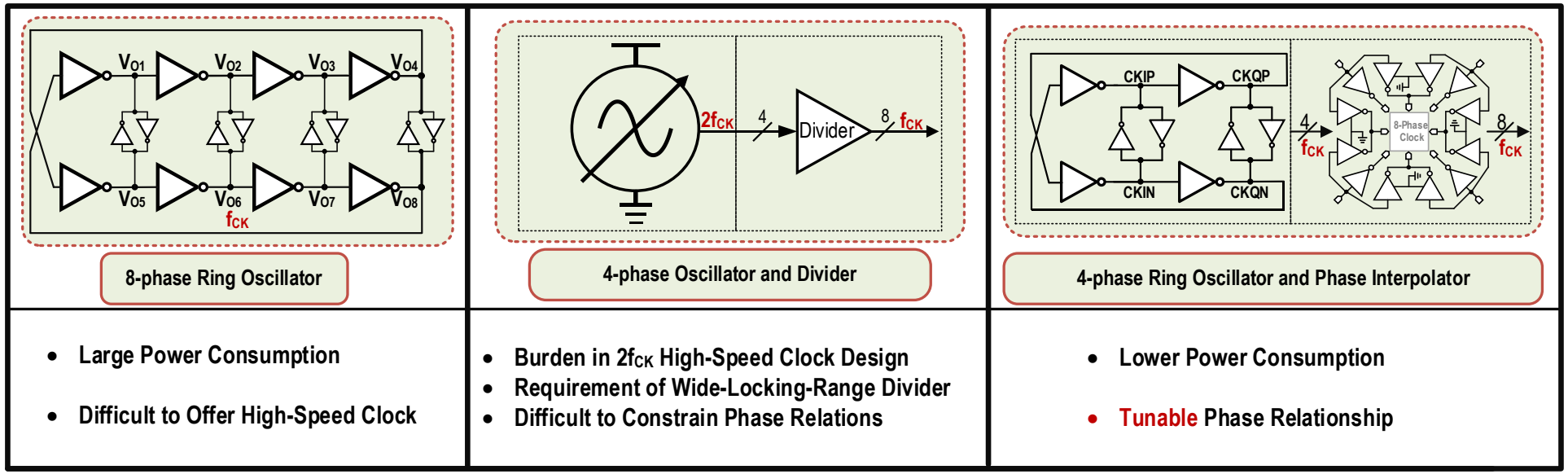
	This Work		ESSCIRC'18 [22]	JSSC'18 [32]	SSCL'20 [23]	JSSC'20 [24]	JSSC'21 [33]
Architecture	**Single-Loop Quarter-Rate BBPD**		Half-Rate CFD+DC-FD	Single-Loop Half-Rate BBPFD	Single-Loop Half-Rate Linear PD	Single-Loop Half-Rate Extended BBPD	Single-Loop Half-Rate BBPD
Oversampling Ratio	**2x**		2x	4x	N/A	2.5x	4x
Need FD?	**No**		Yes	Yes	No	Yes	Yes
Data Sampling Clock?	**No**		Yes	No	Yes	No	No
Data Rate (Gb/s)	**10.8 to 37.4**		4 to 10	6.7 to 11.2	6.4 to 11	6.5 to 12.5	4 to 20
Absolute Capture Range (Gb/s)	**26.6**		6	4.5	4.6	6	16
Acquisition Speed ((Gb/s)/μs)	**4.63**		0.26	4.18	0.29	2	1.6
Output RMS Jitter (ps)	**0.847* / 0.390* @8.55GHz**		1.05 @5GHz	1.8 @5GHz	1.66 @4GHz	1.15 @5.9GHz	1.95 @10GHz
JTOL (UI_{PP}) @ Jitter Frequency	**0.42 @100MHz**	**0.355 @200MHz**	N/A	0.505 @200MHz	0.14 @100MHz	0.34 @200MHz	0.42 @100MHz
Power Consumption (mW)	**45.65 @34.2Gb/s**		33 @10Gb/s	22.5 @10Gb/s	N/A	21.13 @10Gb/s	37.3 @20Gb/s
Energy Efficiency (pJ/bit)	**1.33**		3.3	2.25	2.7	2.11	1.87
Supply Voltage (V)	**1**		1	1.3	1	1	1.2
Core Area (mm^2)	**0.0827**		0.48	0.047	0.11	0.031	0.045
CMOS Technology (nm)	**65**		28	65	28	28	65

*Obtained from integrated phase noise from 100Hz to 1GHz.

Outline

- Motivation
- Design Example 1
- Design Example 2: A 6-to-38Gb/s Capture-Range Bang-Bang Clock and Data Recovery Circuit with Deliberate-Current-Mismatch Frequency Detection and Interpolation-Based Multi-Phase Clock Generation
- Conclusion

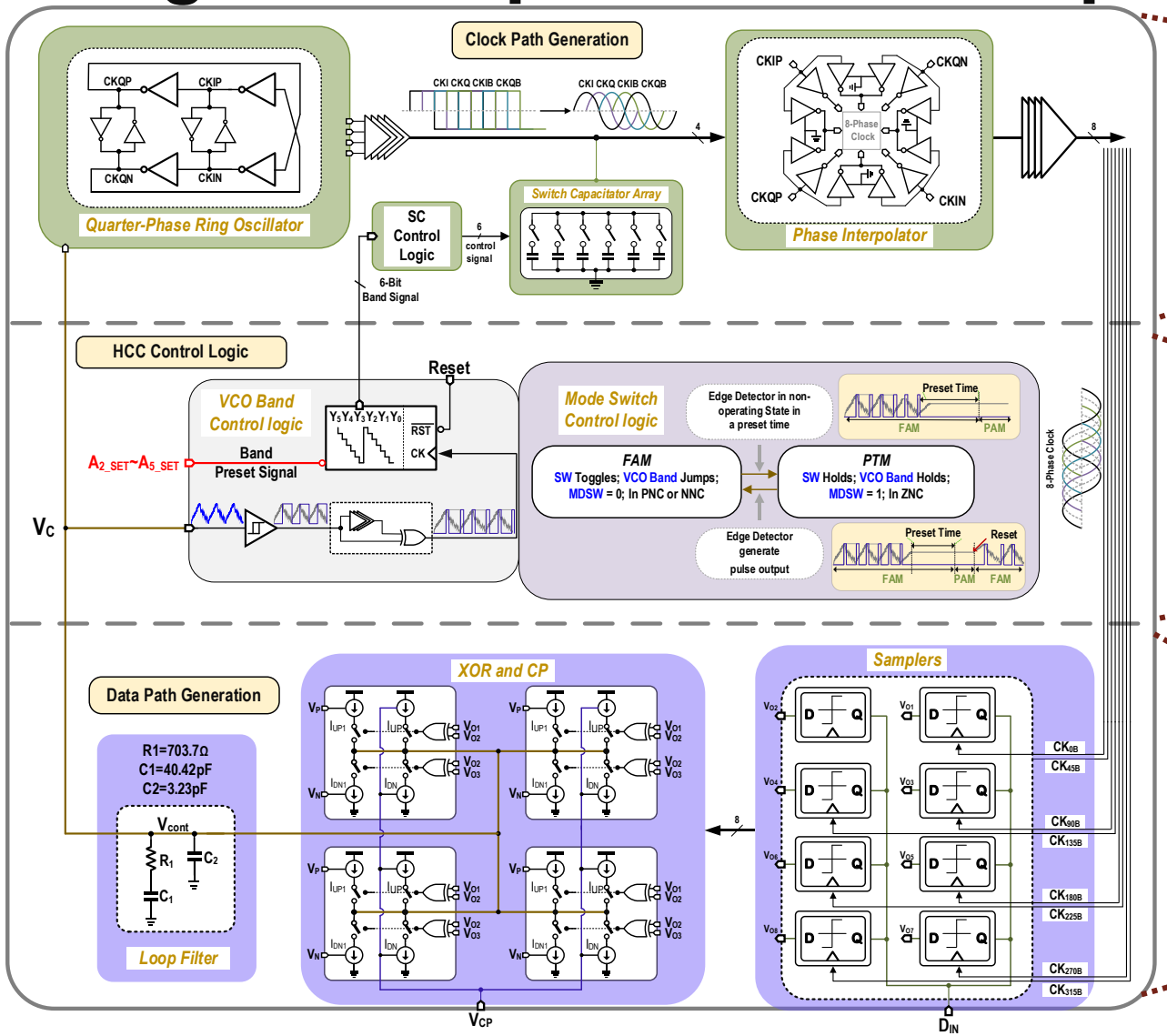
Design 2: Multi-phase Clock Generation



Commonly used eight-phase clock generation schemes: (a) eight-phase ring oscillator (b) the divider follows the quarter-phase oscillator and (c) the phase interpolator follows quarter-phase ring oscillator

- Half-rate or quarter-rate scheme to relieve high-speed clock design pressure
- These scheme requires multi-phase clock generation

Design 2: Proposed Wide-Capture-Range BBCDR

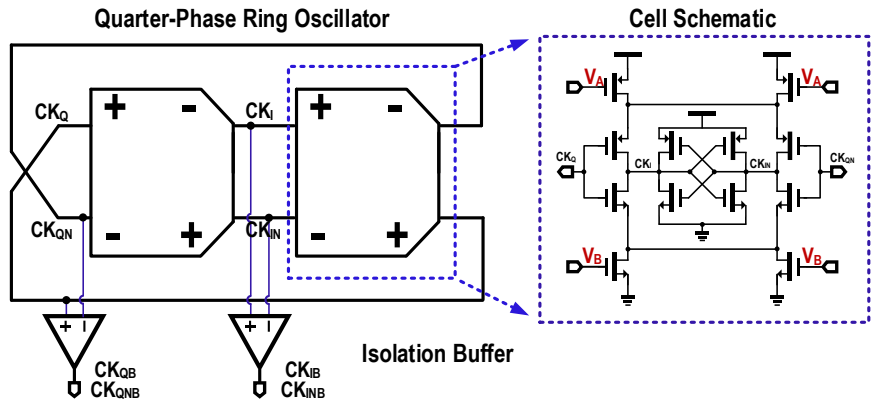


Clock Path (Multi-phase clock generation)

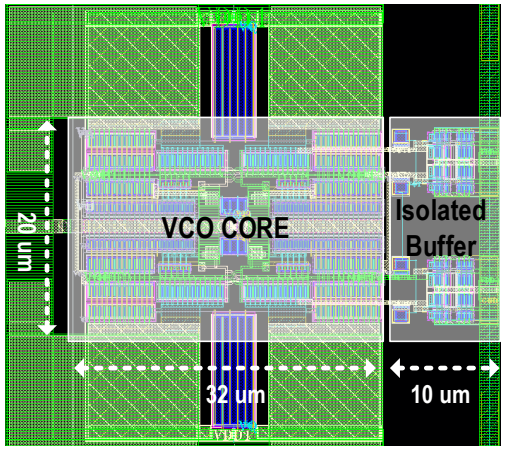
HCC (VCO band control and mode switch control)

Data Path (Data retiming and phase detection)

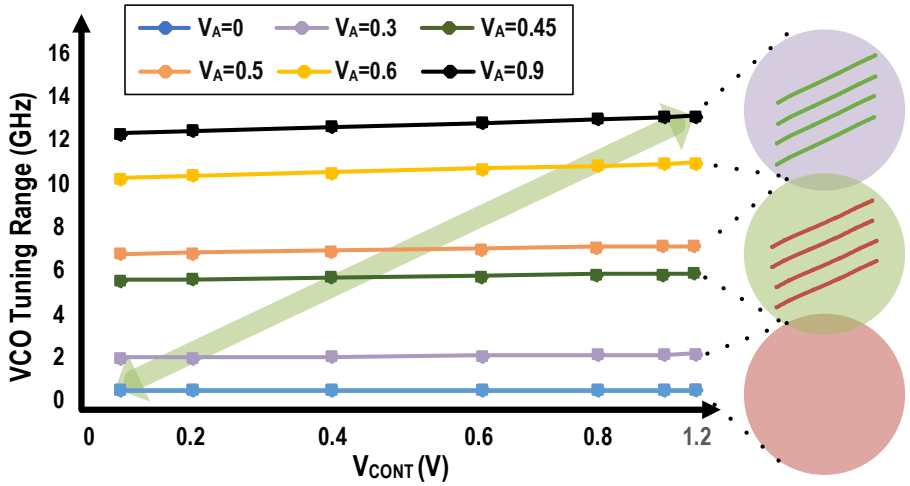
Design 2: Clock-path Generation



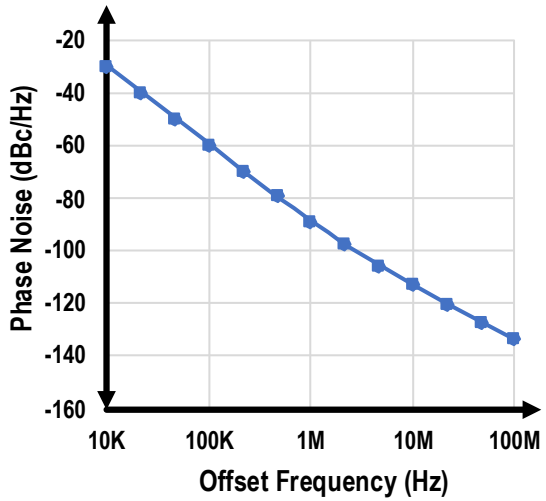
(a)



(b)



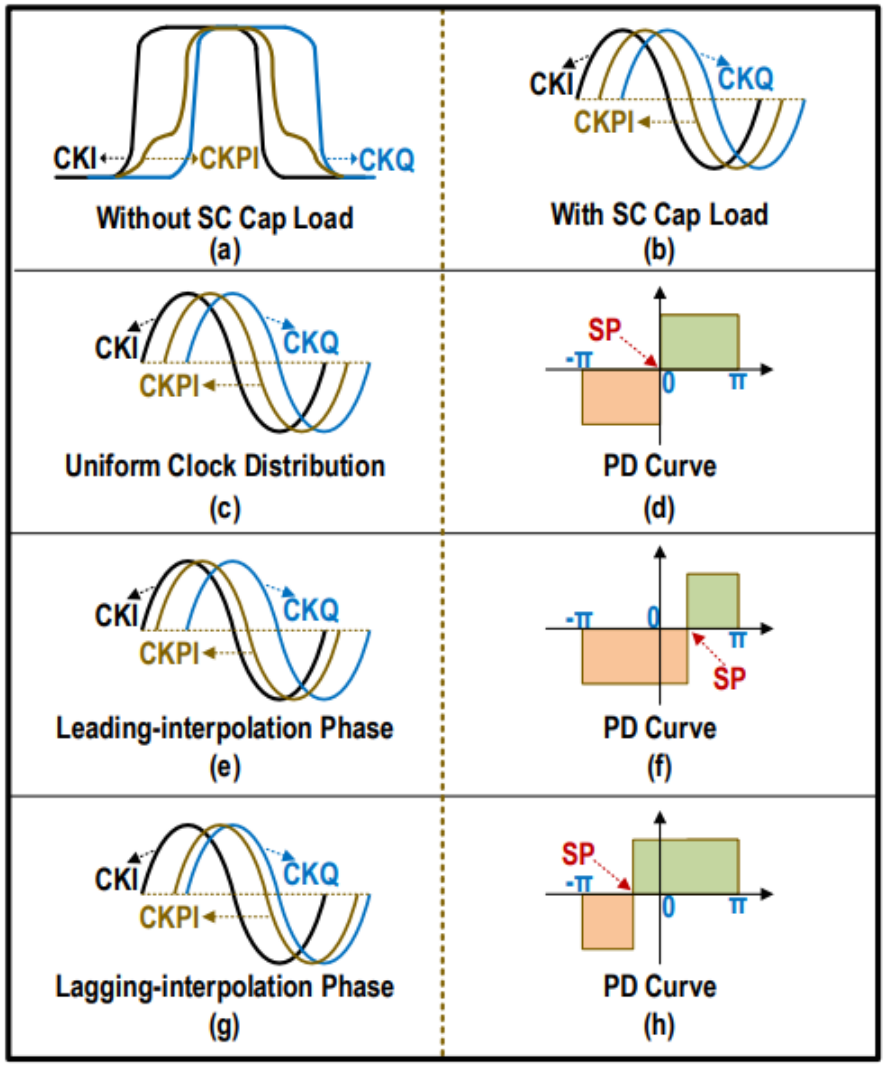
(c)



(d)

Quarter-phase RO design

Design 2: Nonideal Clock Phase Effect on PD Curve



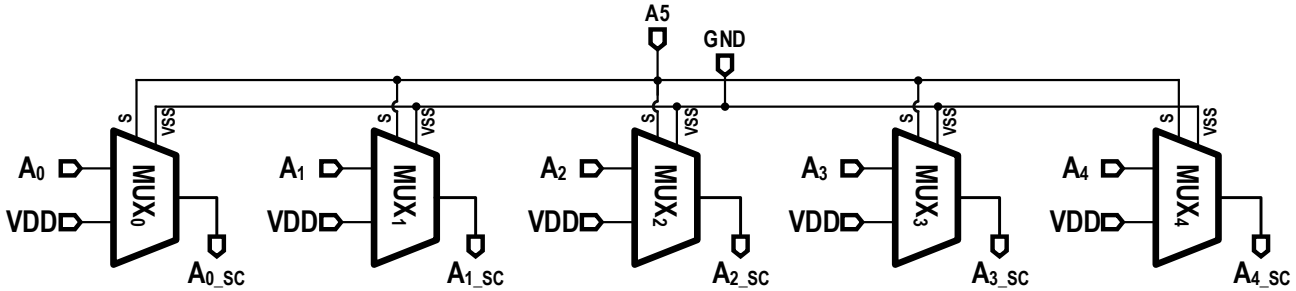
Use SC load to smooth quarter-phase clock for better interpolator

Ideal phase relationship

Leading phase result in a negative SP

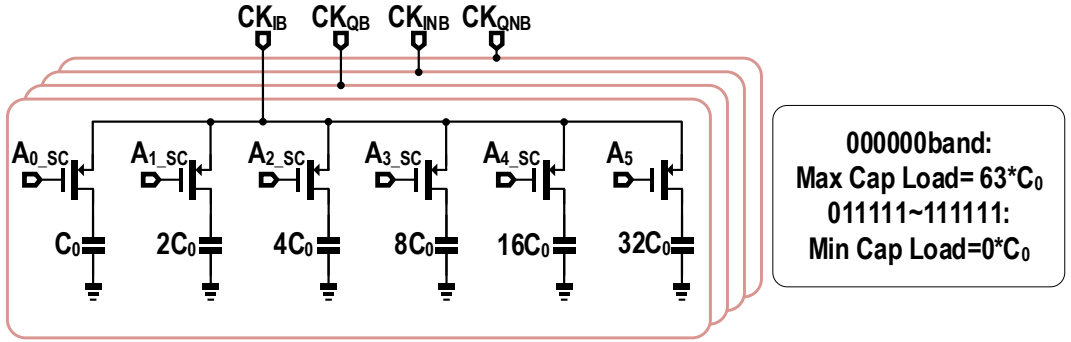
Lagging phase result in a positive SP

Design 2: Switched-capacitor Array



Truth Table					
A_5	A_{0_SC}	A_{1_SC}	A_{2_SC}	A_{3_SC}	A_{4_SC}
0	A_0	A_1	A_2	A_3	A_4
1	VDD				

(a)

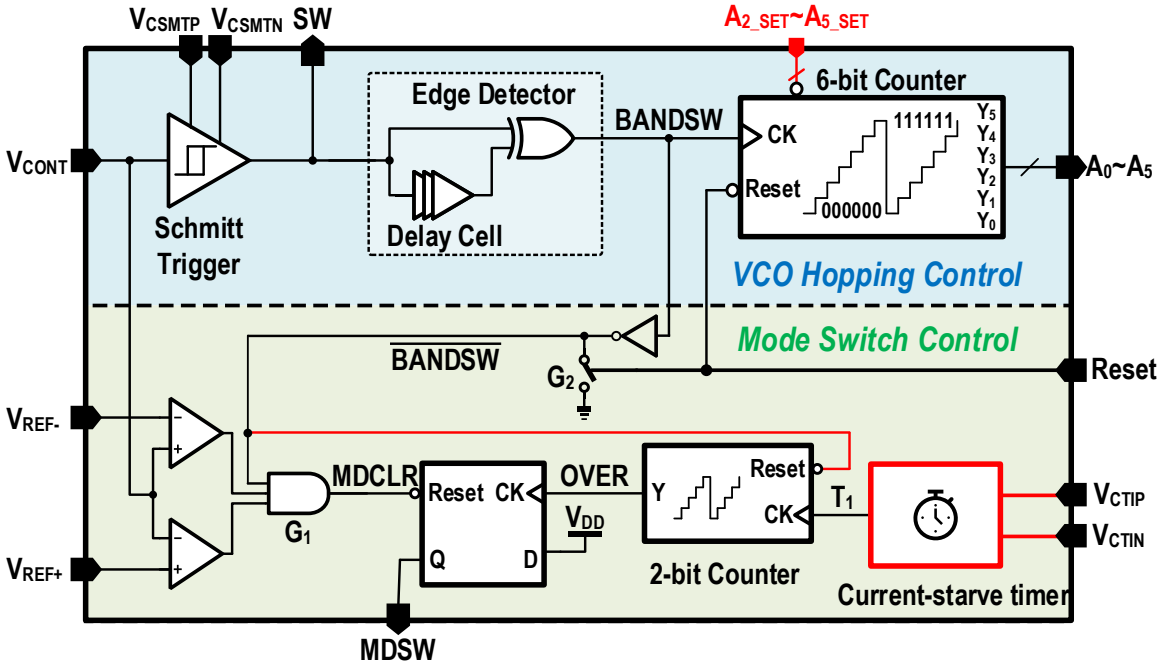


(b)

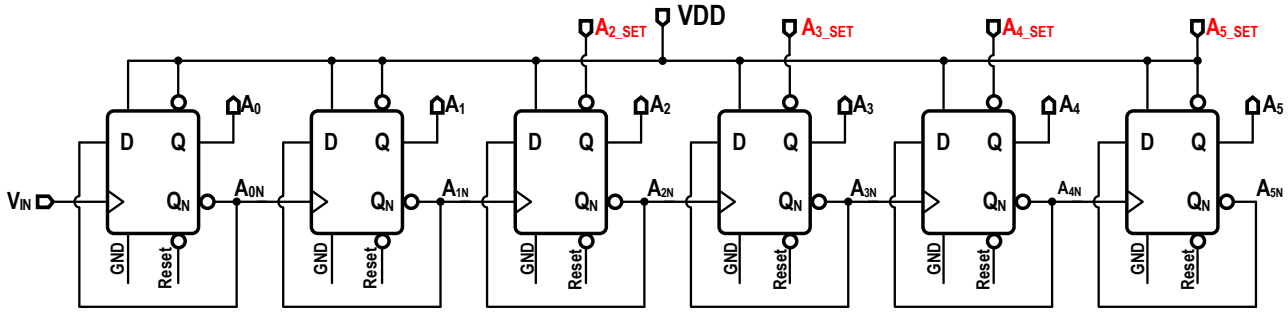
SC array control

- When the highest bit A5=1, SC load cap=0
- 000000band has max cap load=63*C_0
- The C_0 is determined by simulation

Design 2: HCC Block with Band Preset



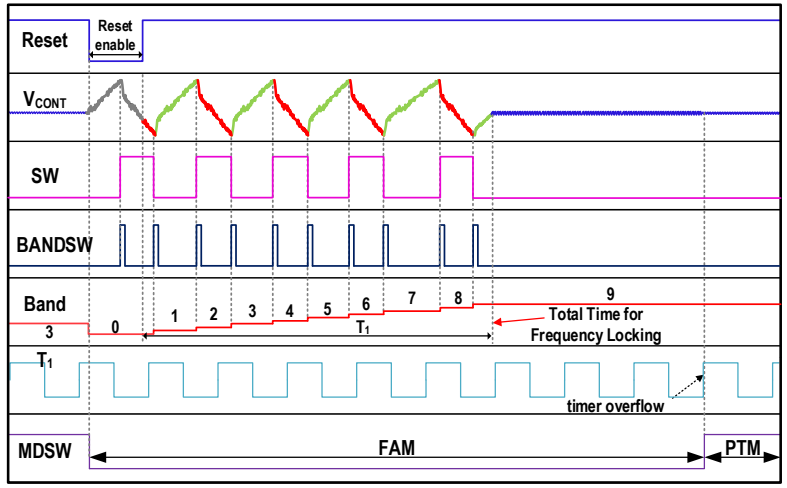
HCC block



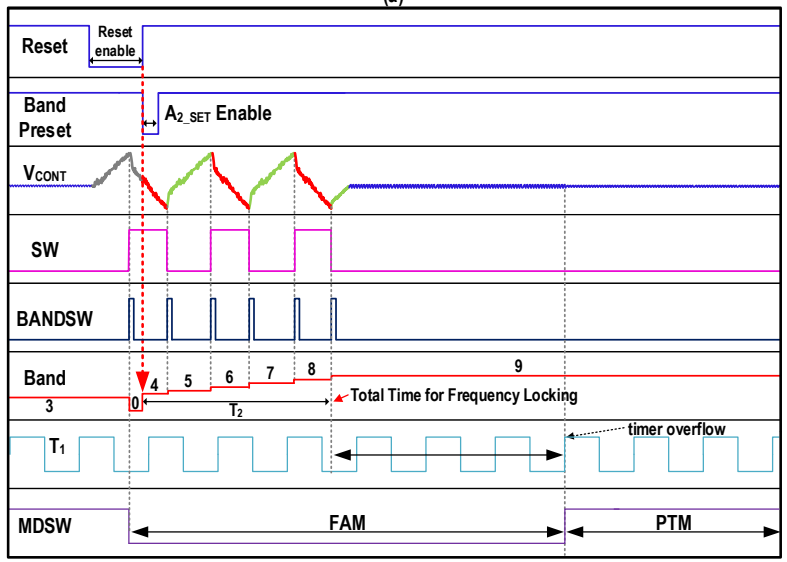
VCO band counter with band preset function

A2_SET~A5_SET enable, corresponding A2~A5 bit set to 1

Design 2: HCC Block with Band Preset

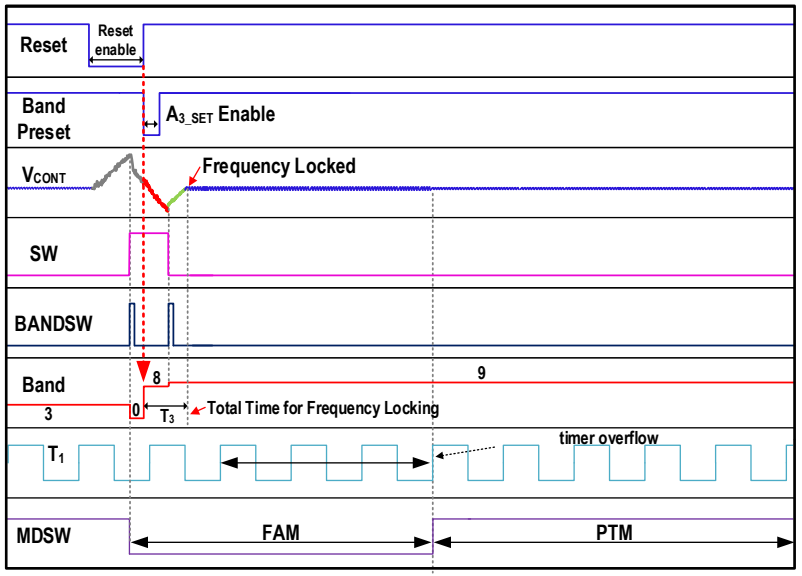


(a)



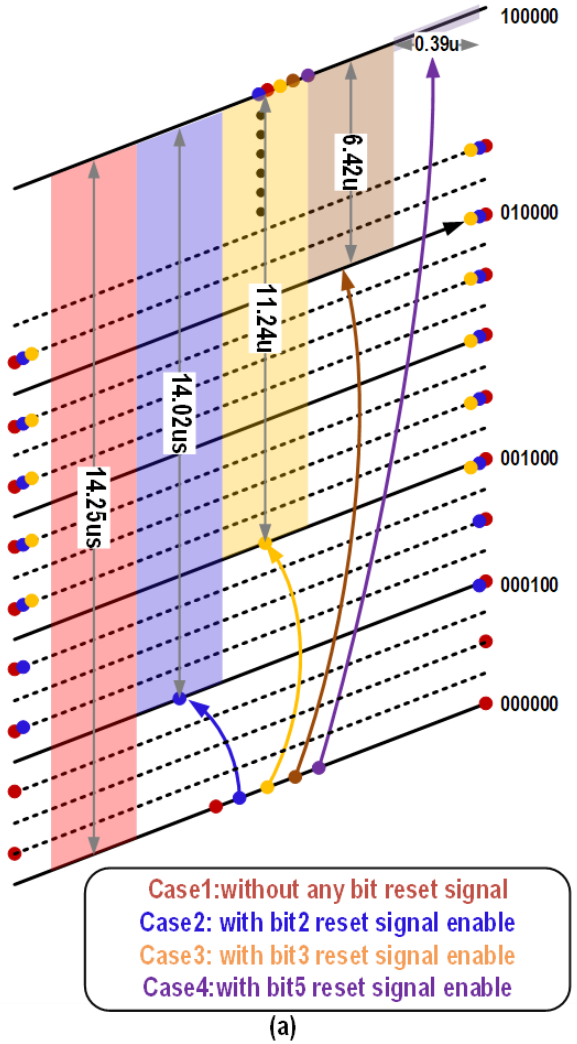
(b)

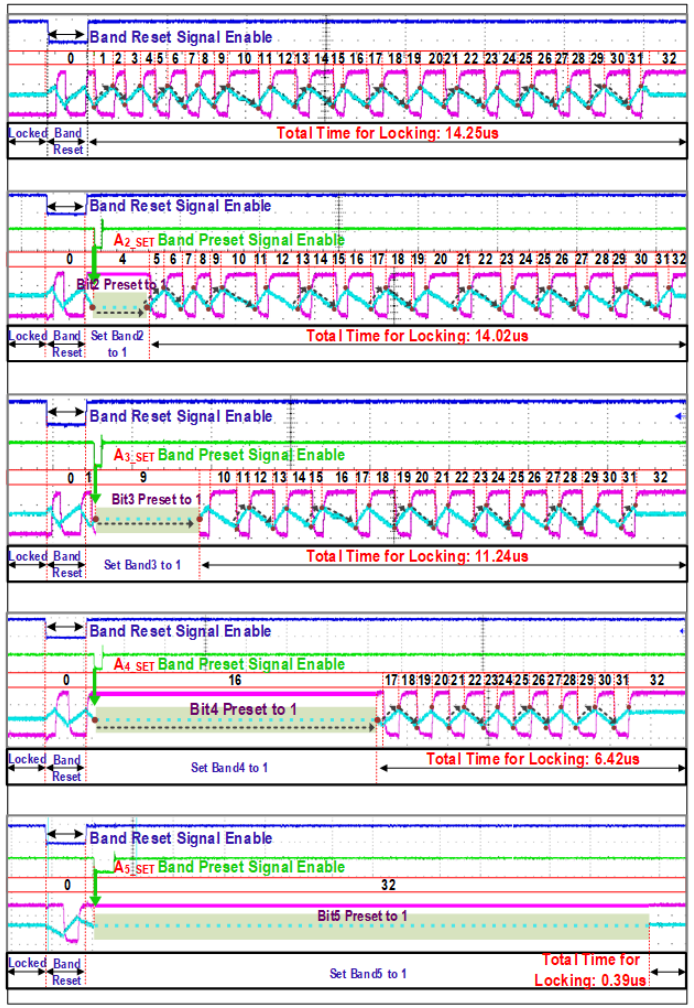
- Bit preset signal is generated by a pulse generator
- The bit preset signal follows band reset signal
- Preset bit to 1 will reduce frequency acquisition time



(c)

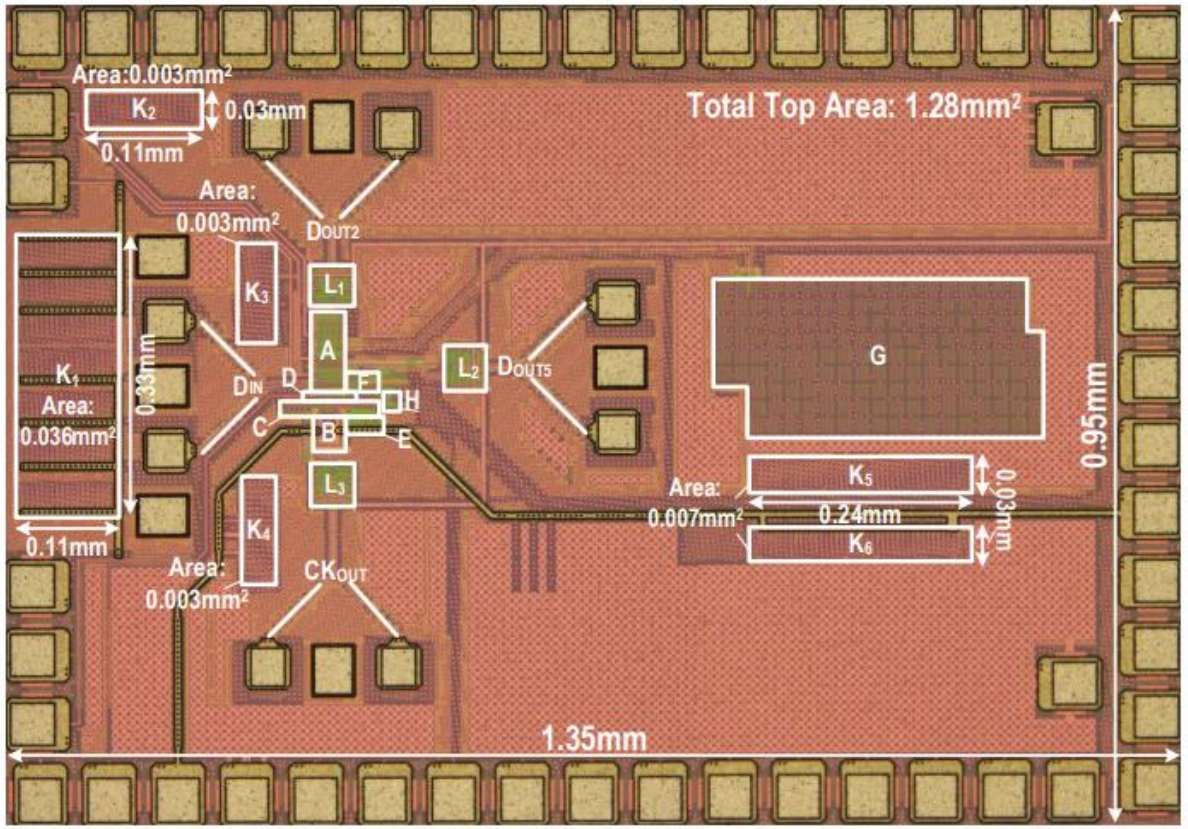
Design 2: Illustration of different band-jumping cases





- The preset signals do not impair the operation of the loop during the FAM period
- Input data rate is of 12 GHz ~ 14.3 GHz (band 4 to band 7), A2_SET will set bit 2 to 1
- In the frequency range of 14.3 GHz ~ 16.6 GHz (band 8 to band 15), A3_SET will set bit 3 to 1
- In the frequency range of 16.6 GHz ~ 28 GHz (band 16 to band 31), A4_SET will set bit 4 to 1
- In the frequency larger than 28 GHz (band32 to band63), A5_SET set bit 5 to 1

Design 2: Chip Photo and Area Breakdown



Area Breakdown (mm²)

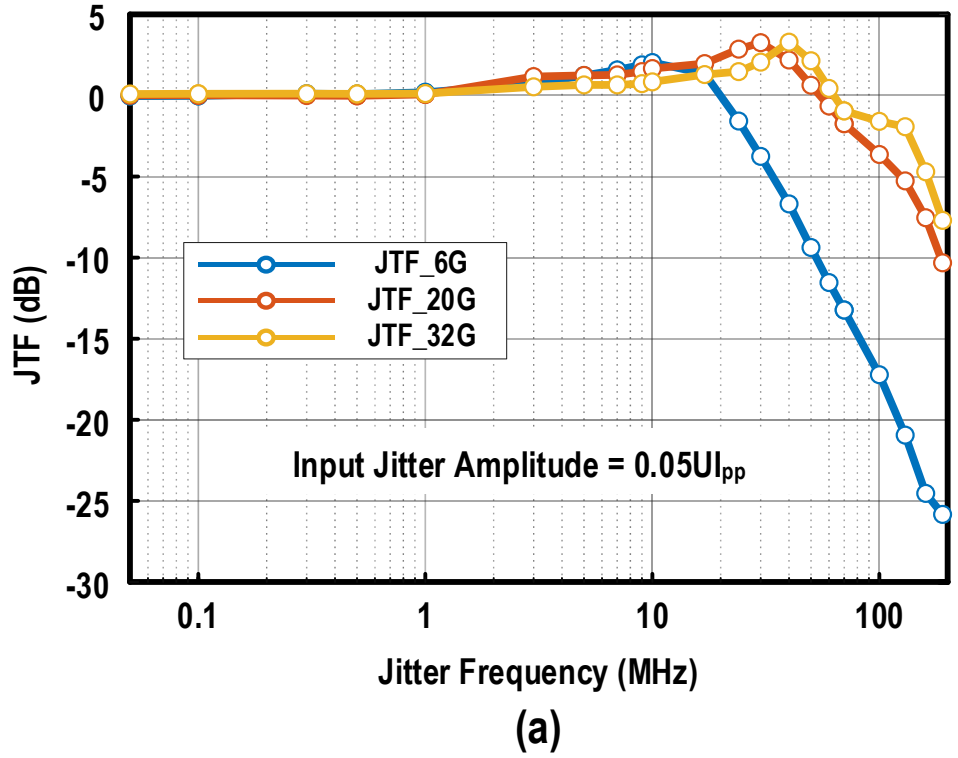
	Main Circuits	Area		Main Circuits	Area		Auxiliary Circuits		
A	PD + CP + XOR	0.0026	E	RDAC	0.0007	L_1	D_{OUT2} Output Buffer	K	Decoupling Capacitor
B	RO + VCO Buffer	0.0011	F	HCC	0.0005	L_2	D_{OUT5} Output Buffer		
C	SC Array	0.0011	G	LF	0.064	L_3	Clock Output Buffer		
D	PI + PI Buffer	0.0002				H	V_{CONT} Output Buffer		
Total Core Area: 0.07mm²									

Power Breakdown (mW)

Sub-Blocks	Power	Proportion	Sub-Blocks	Power	Proportion
VCO	10.37	42.1%	XOR	1.01	4.1%
CP	1.13	4.6%	PD	4.41	18.0%
PI	1.50	6.1%	HCC	0.47	1.9%
PI Buffer	5.72	23.2%	Energy Efficiency = 0.769 pJ/bit @ 32Gb/s		
Total Power Consumption: 24.61mW					

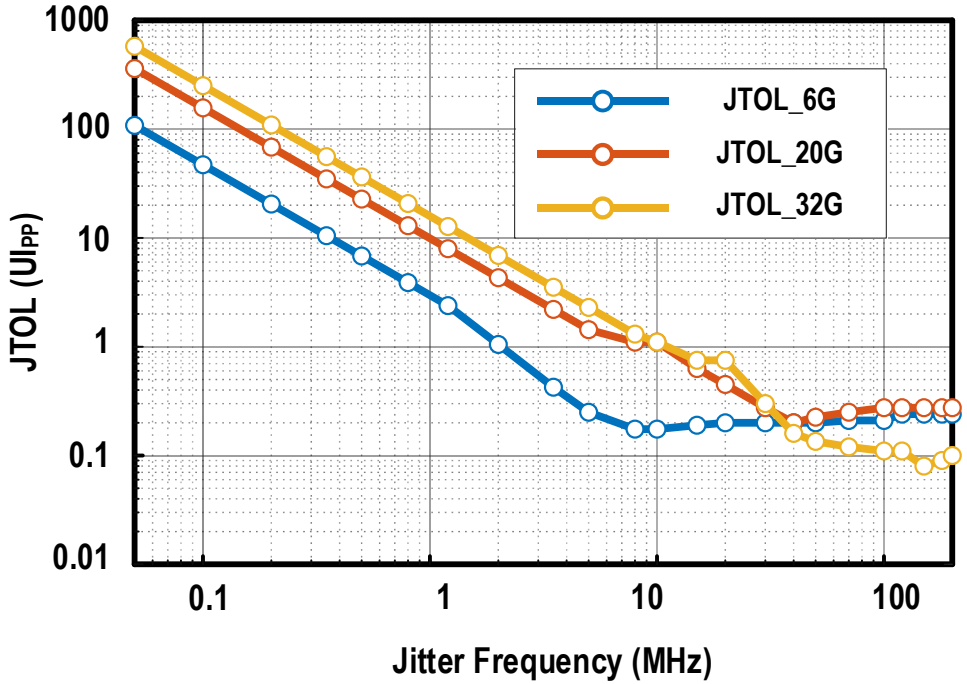
The total area of the PD, CP, and XOR modules enabling data retiming, phase detection, and frequency acquisition are just 0.0026 mm², i.e., 3.7% of the total core area

Design 2: Measured JTF and JTOL Curves



(a)

Measured jitter transfer function with 0.1-UI_{PP} input jitter

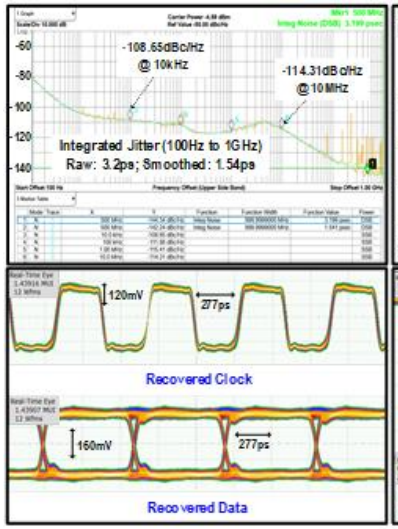


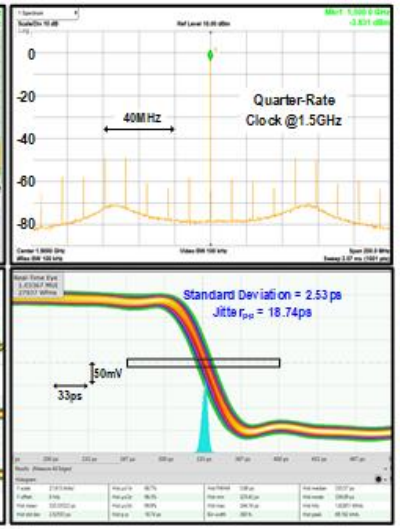
(b)

Measured jitter tolerance curve with BERT

Design 2: Measured Eye Diagram and Histogram

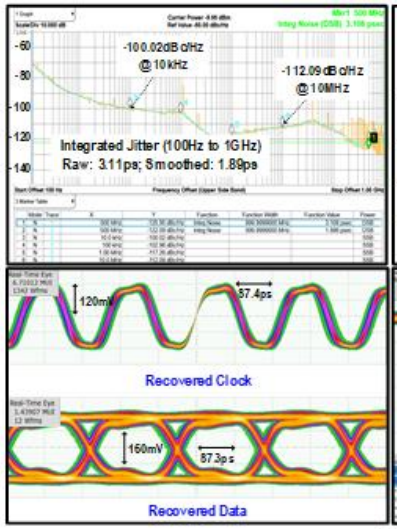
6Gb/s input

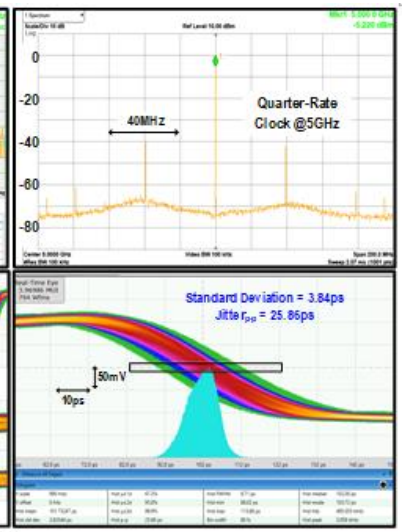




(a)

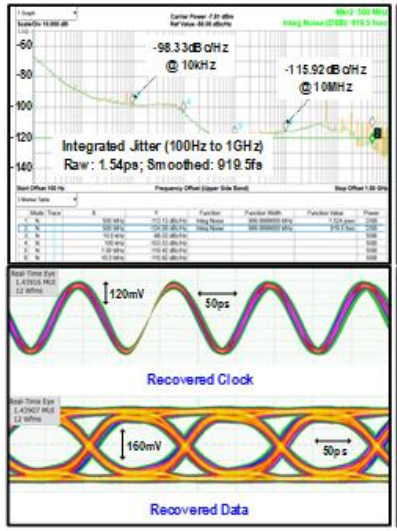
20Gb/s input

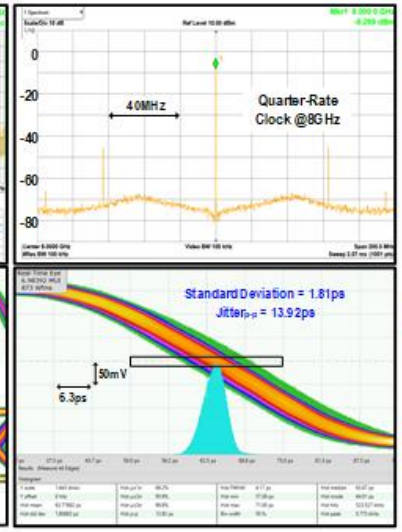




(b)

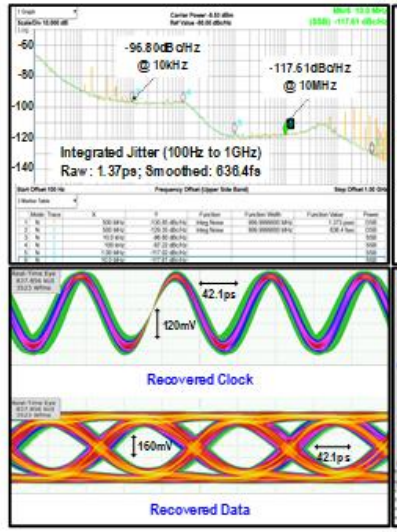
32Gb/s input

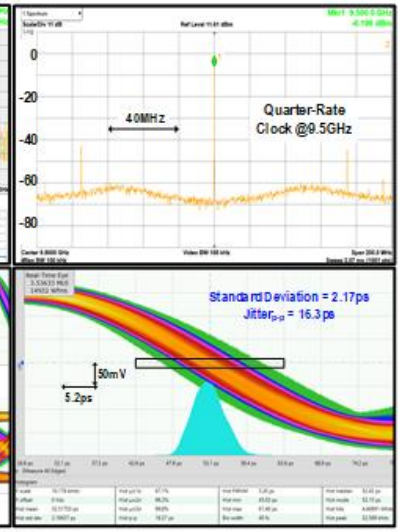




(c)

38Gb/s input





(d)

Design 2: Summary and Comparison with Prior Arts

		This Work		ESSCIRC'18 [13]	JSSC'21 [4]	JSSC'17 [23]	JSSC'20 [24]	JSSC'22 [34]	JSSC'22 [36]
Key Technologies		**Single-Loop Quarter-Rate BBPD**		Half-Rate CFD+DC-FD	Single-Loop Half-Rate BBPD	Single-Loop Half-Rate Baud-Rate PD	Single-Loop Half-Rate Extended BBPD	Single-Loop Full-Rate BBPD	Single-Loop Half-Rate BBPD
Oversampling Ratio		**2x**		2x	4x	1x	2.5x	2x	2x
Need FD?		**No**		Yes	Yes	Yes	Yes	No	No
Data Sampling Clock?		**No**		Yes	No	No	No	No	No
Data Rate (Gb/s)		**6 to 38**		4 to 10	4 to 20	22.5 to 32	6.5 to 12.5	23.4 to 29.1	47.6 to 58.8
Absolute Capture Range (Gb/s)		**32**		6	16	9.5	6	5.7	11.2
Acquisition Speed((Gb/s)/μs)		**3.19**		0.26	1.6	0.001	2	8.2	9.81
Output RMS Jitter (ps)		**1.81* / 0.919** @8GHz**		1.05 @5GHz	1.95 @10GHz	2.6 @12.5GHz	1.15 @5.9GHz	0.487@14GHz	0.416@13GHz
JTOL (UI_{PP}) @ Jitter Frequency	D_{IN} (NRZ)	**0.275 @100MHz**	**0.275 @200MHz**	N/A	0.42 @100MHz	0.2 @100MHz	0.34 @200MHz	N/A	0.45 @100MHz
	D_{IN} (PAM-4)	**N/A**	**N/A**	N/A	N/A	N/A	N/A	0.4 @200MHz	0.1 @100MHz
Power Consumption (mW)		**24.6 @32Gb/s**		33 @10Gb/s	37.3 @20Gb/s	87.61 @32Gb/s	21.13 @10Gb/s	19.16	11 to 13.1
Energy Efficiency (pJ/bit)		**0.769**		3.3	1.87	2.74	2.11	0.68	0.22 to 0.25
Supply Voltage (V)		**1**		1	1.2	0.9	1	1.2 / 0.6	1 / 0.6
Core Area (mm^2)		**0.07**		0.48	0.045	0.138	0.031	0.0285	0.056
CMOS Technology (nm)		**65**		28	65	28	28	28	28

Outline

- Motivation
- Design Example 1
- Design Example 2
- **Conclusion**

Conclusions

Design 1:

- Quarter-rate reference-less BBCDR without separate FD
- Achieve wide capture range (**10.8 to 37.4Gb/s**)
- Small core area (**0.0827 mm^2**)
- Low energy efficiency (**1.33 pJ/bit**)
- High jitter tolerance (**0.355 UIpp**)

Design 2:

- Current-mismatch-based frequency acquisition technique to achieve FD-less frequency acquisition
- Phase Interpolator-based multi-phase clock generation scheme
- Tunable clock phase
- Achieve wide capture range (**6 to 38Gb/s**)
- Small core area (**0.07 mm^2**)
- Low energy efficiency (**0.769 pJ/bit**)

香港科技大學
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UNIVERSITY OF SCIENCE
AND TECHNOLOGY

HKUST OWL

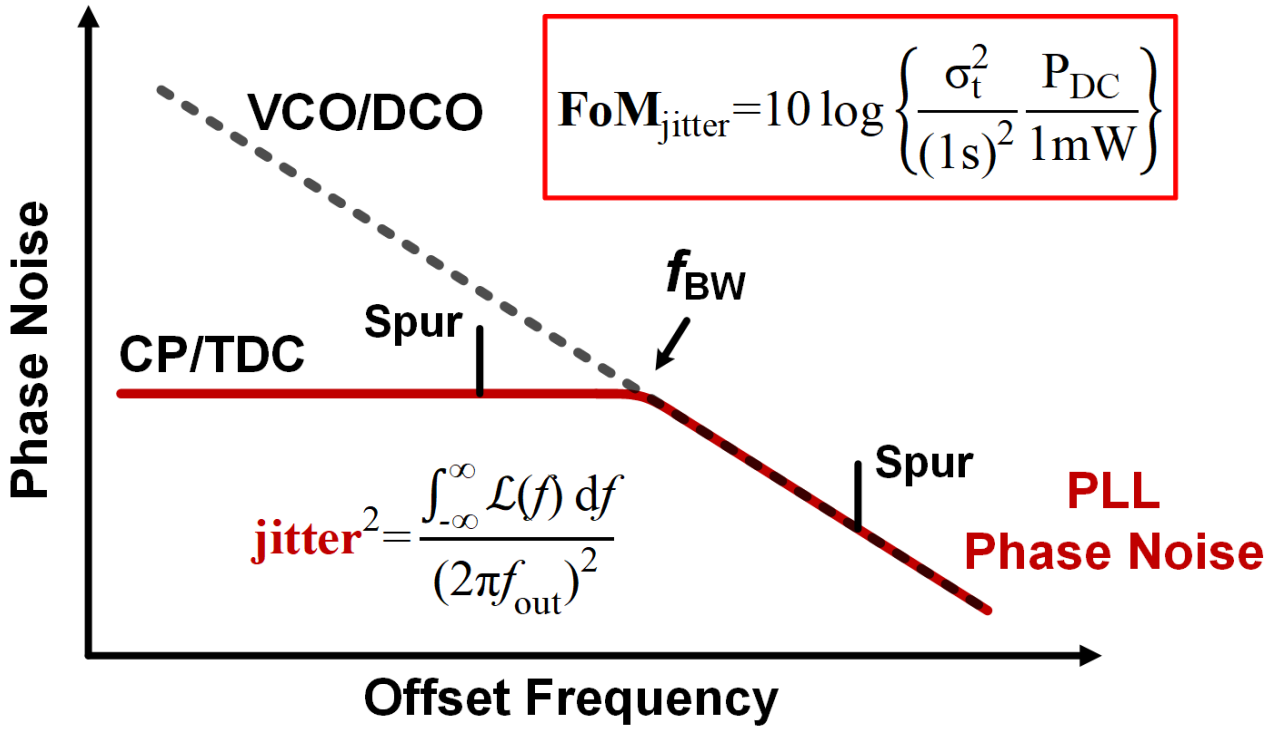
Cascaded Dual Loop:

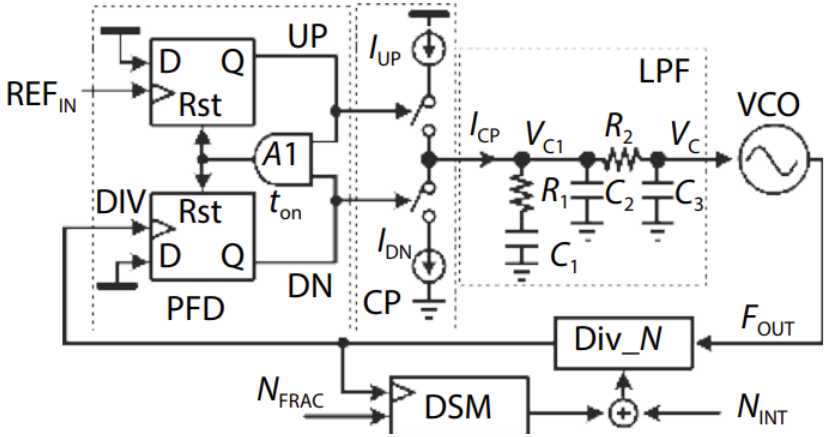
for Low-Jitter Frequency Synthesis Towards 200-GB/s Transceiver

Outline

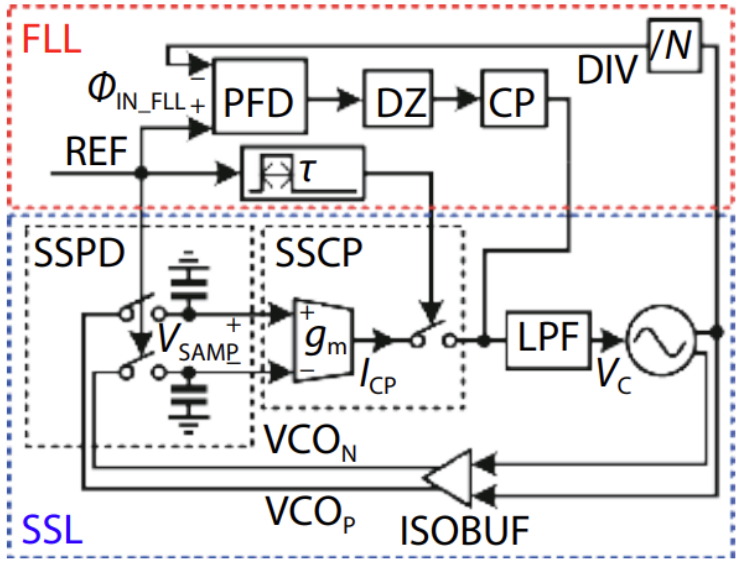
- Motivation
  - Background
  - PLL Architecture Choices and Frequency Planning
- Proposed Cascaded PLL Architecture
  - 1st-stage Low-Jitter Sub-sampling PLL (SSPLL)
  - 2nd-stage Dual-Path Sub-sampling PLL (DP-SSPLL)
- Measurement Results
- Conclusion

PLL General Background





PFD+CP-based PLL

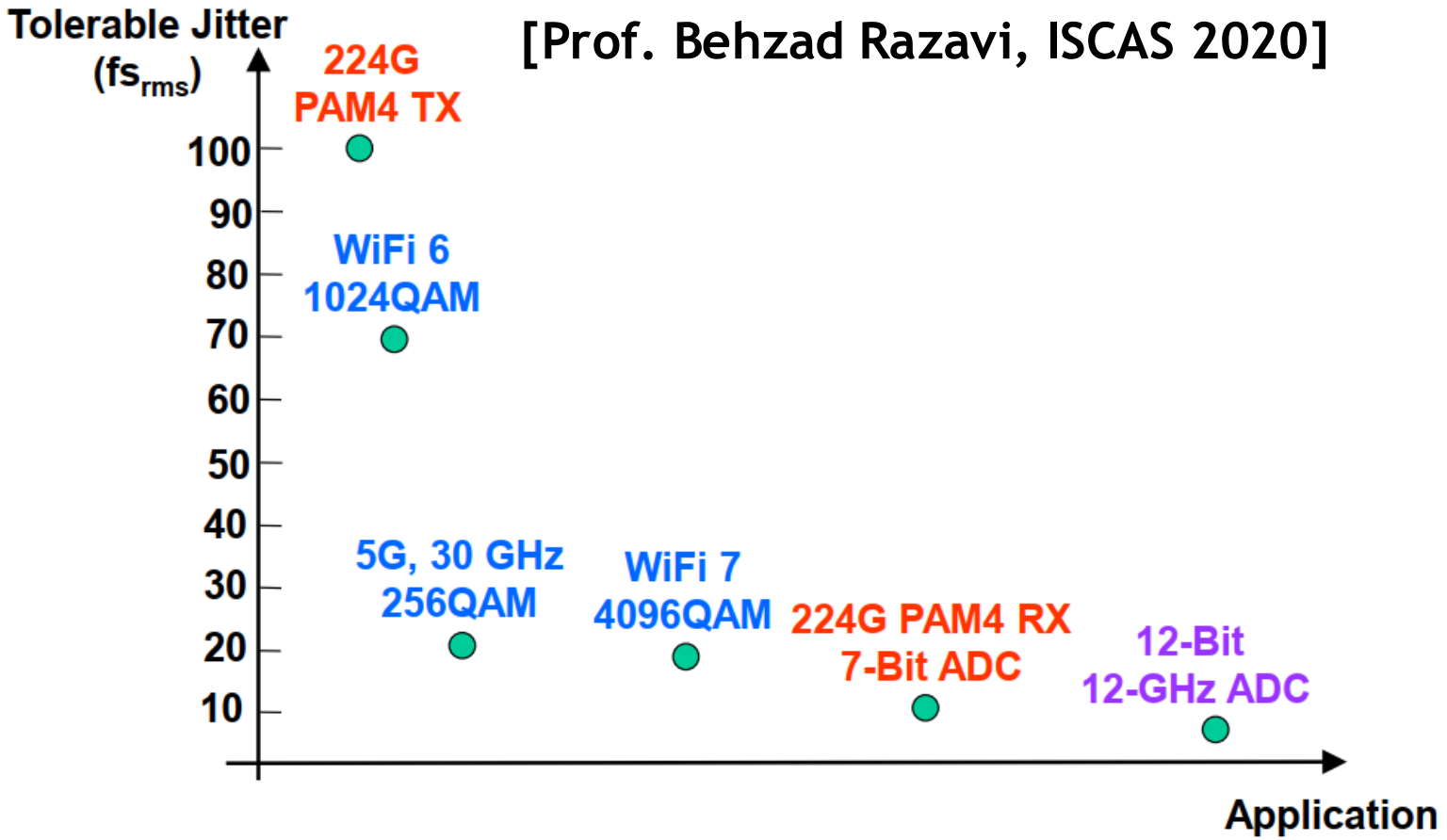


SSPLL

- To suppress the in-band phase noise, a large PD gain is necessary
- Sub-sampling technique provides the highest gain so far among different phase detector techniques

PLL Jitter Requirement

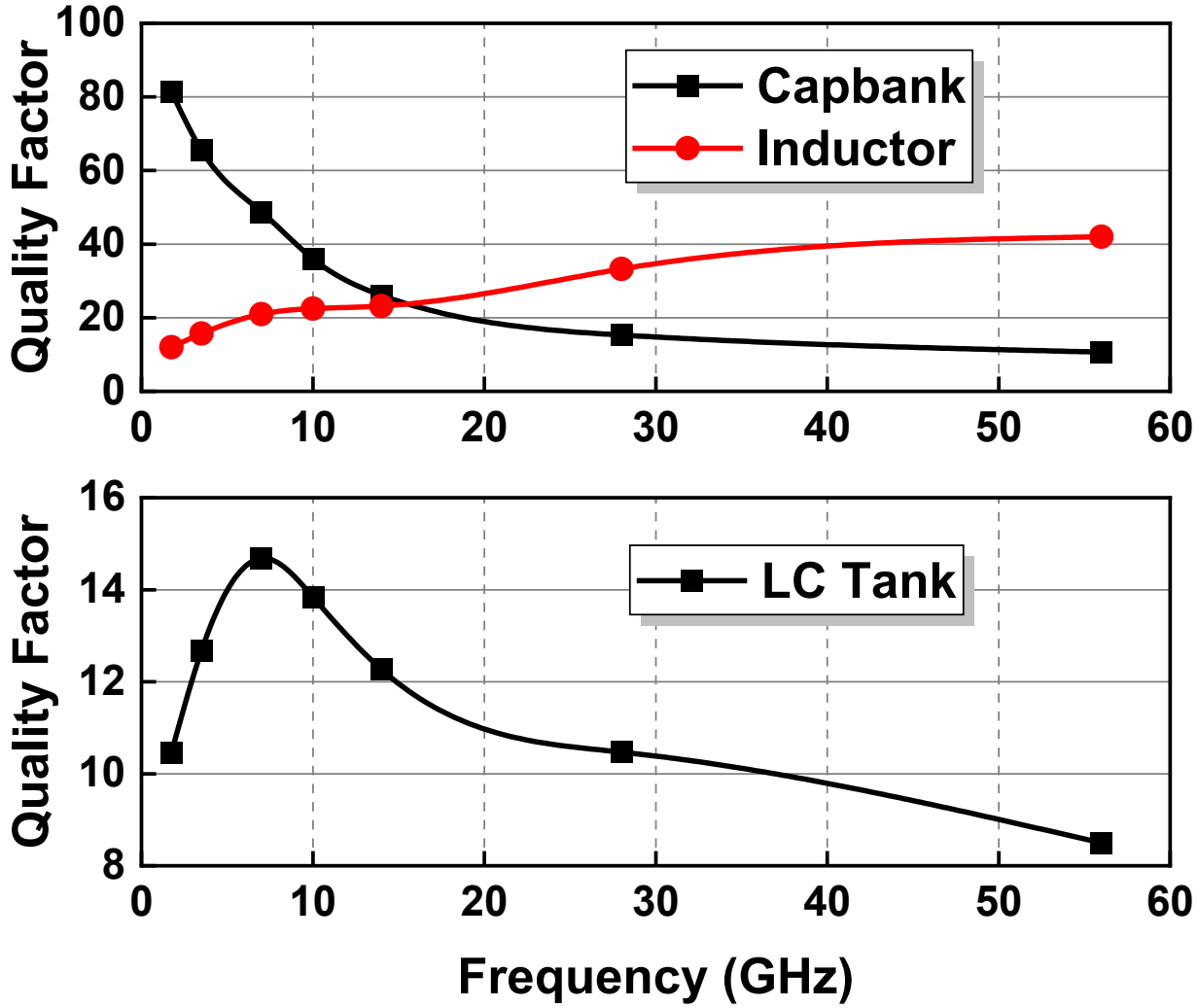
[Prof. Behzad Razavi, ISCAS 2020]



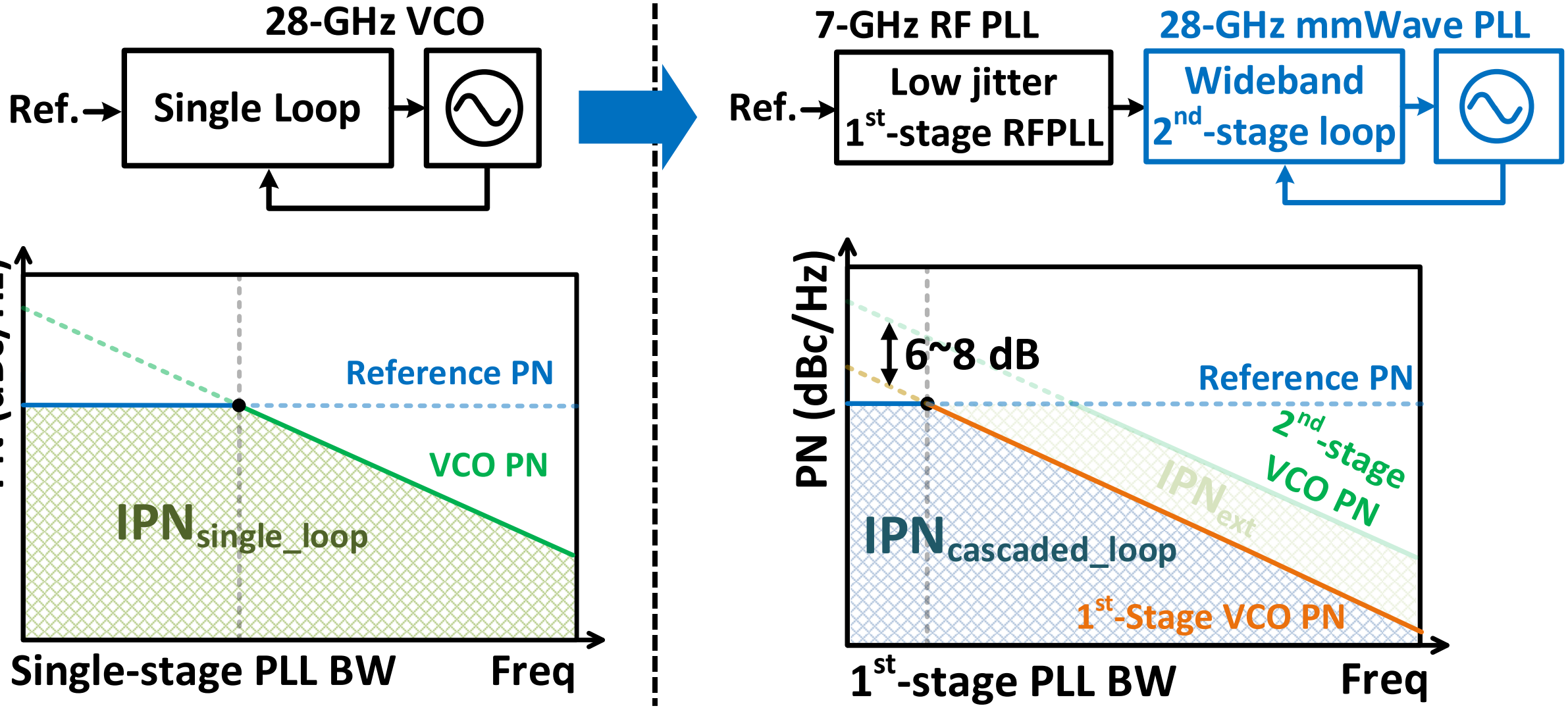
- <100-fs jitter required for PAM4 TX, < 20-fs jitter required for ADC-based PAM-4 Rx

Background: Application & Challenge

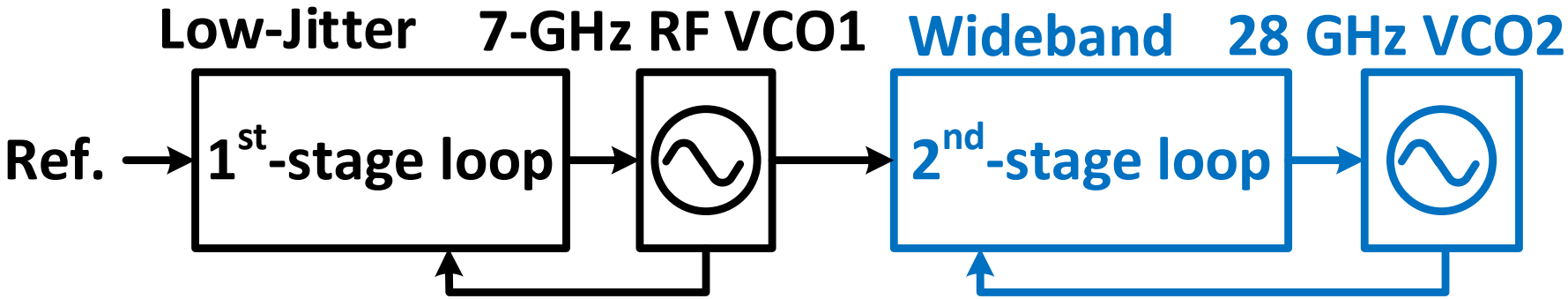
- Towards 224-Gb/s Transceiver, 28-GHz clock required for quarter-rate operation
- PLL jitter-power tradeoff due to degraded LC-tank Q
- At >10-GHz GHz, LC-tank Q degrades significantly

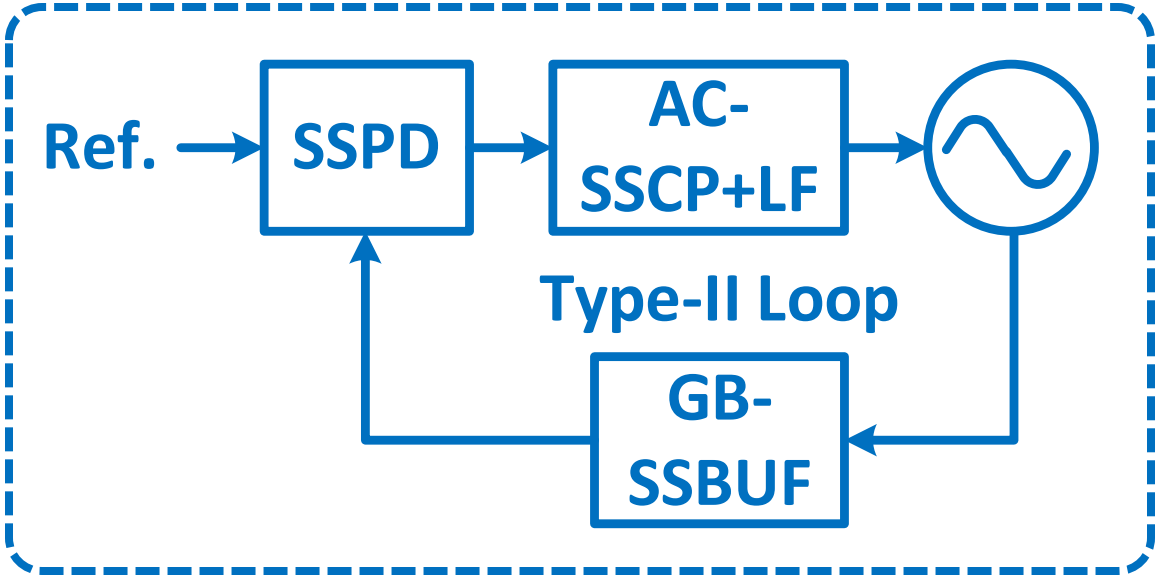


Advantage of Cascaded PLL Architecture



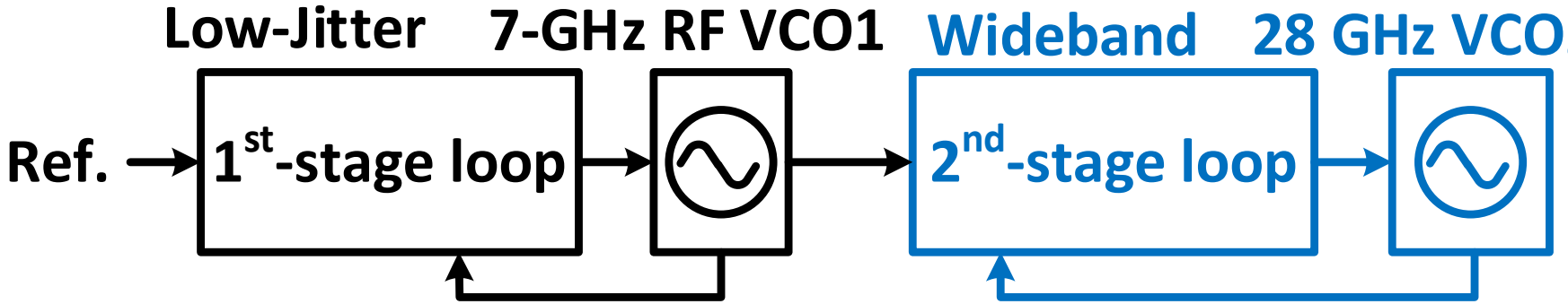
Architecture Planning: 1st-Stage RF PLL

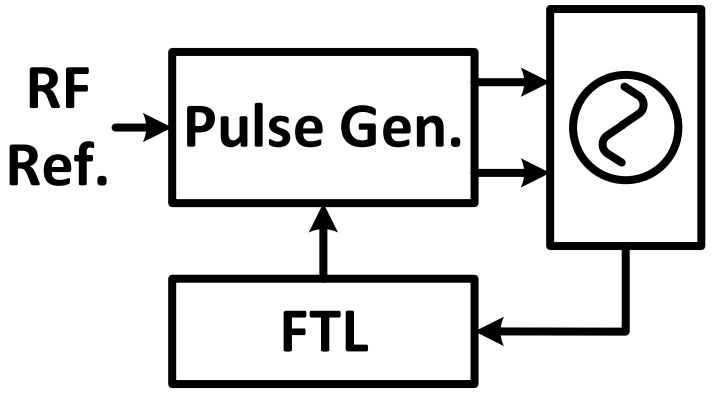




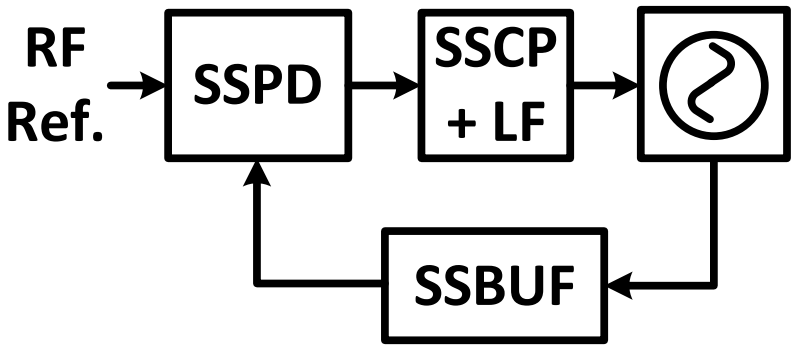
- ☑ Maximized PD gain suppresses in-band noise
  - AC-coupled SS-charge pump (AC-SSCP) and gain-boosted SS-buffer (GB-SSBUF)
- ☑ No divider-induced noise

Architecture Planning: 2nd-Stage 28-GHz PLL

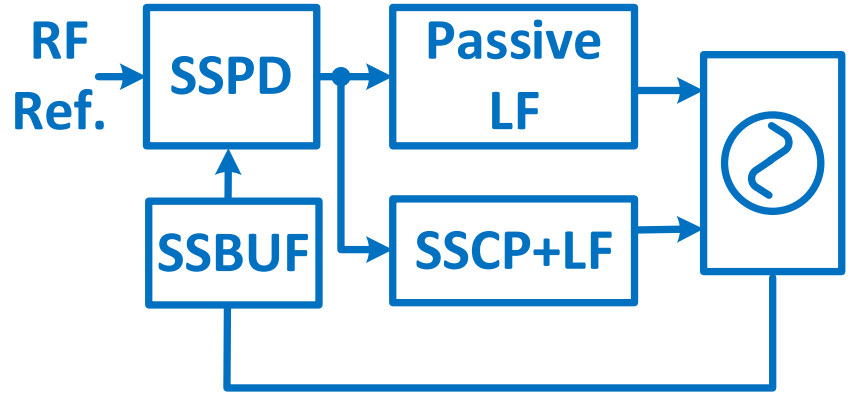




- Power hungry pulse generator (PG) at GHz range

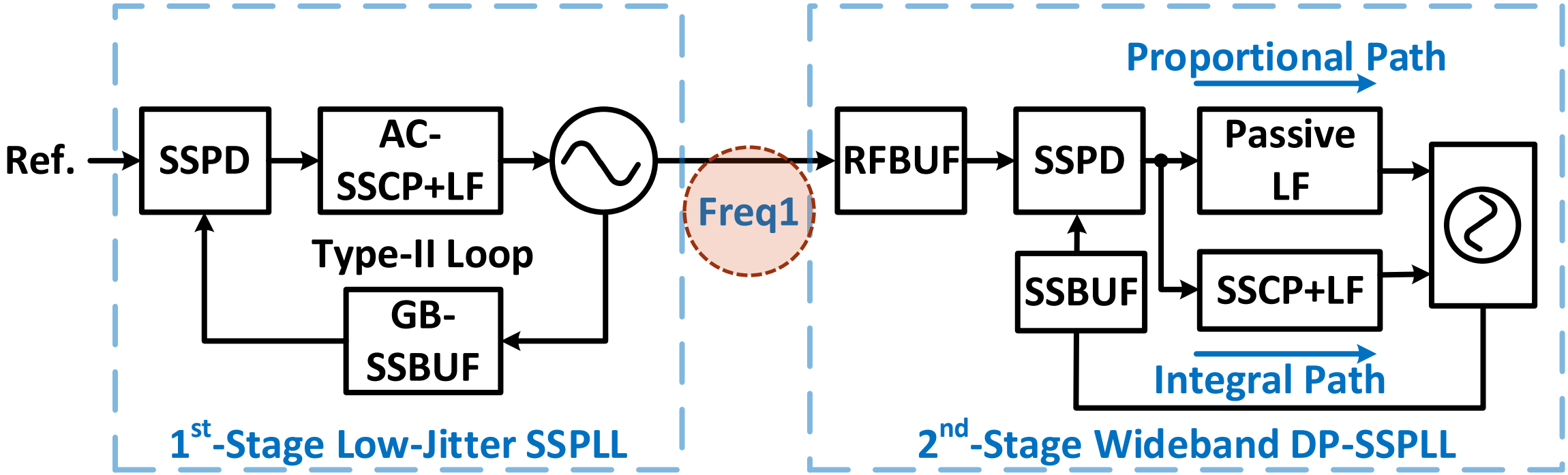


- PN from SSCP and LF
- Large SSCP power consumption at GHz



- Low in-band noise
- Negligible SSCP power consumption
- No off-chip LF capacitor

RF-PLL Frequency Planning



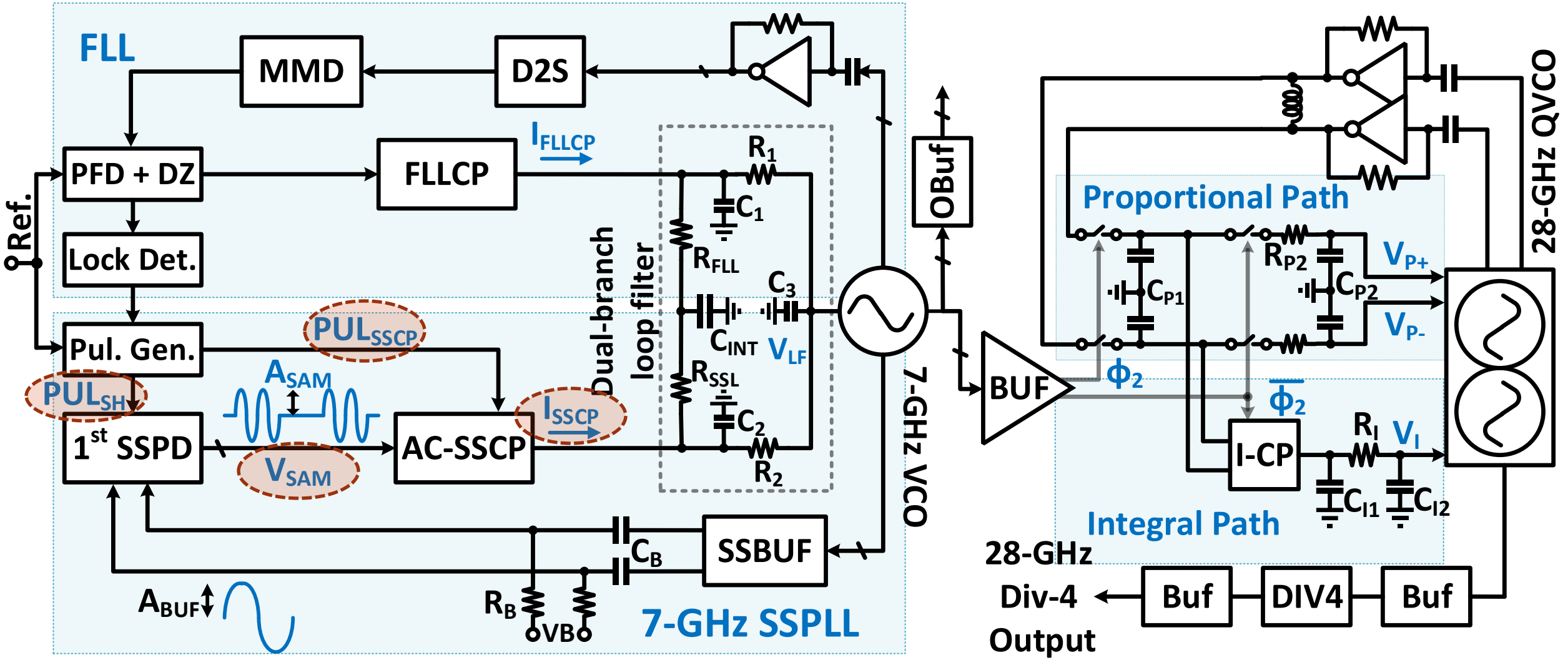
This work: RF-PLL freq at 7 GHz

- ☑ Close to maximum LC-tank Q
- ☑ Sufficient phase margin for 2nd-stage PLL loop filter at 100-MHz BW
- ☒ Higher power for buffer

RF-PLL freq at 1.75 or 3.5 GHz

- ☒ Lower tank Q, worse RF-VCO PN
- ☒ Causes phase margin-BW trade-off for 2nd-stage PLL
- ☑ Less power for GB-SSBUF and RF-BUF

Proposed Cascaded PLL



Outline

- Motivation
  - Background
  - PLL Architecture Choices and Frequency Planning
- Proposed Cascaded PLL Architecture
  - 1st-stage Low-Jitter Sub-sampling PLL (SSPLL)
  - 2nd-stage Dual-Path Sub-sampling PLL (DP-SSPLL)
- Measurement Results
- Conclusion

1st-Stage Low-Jitter RF SSPLL

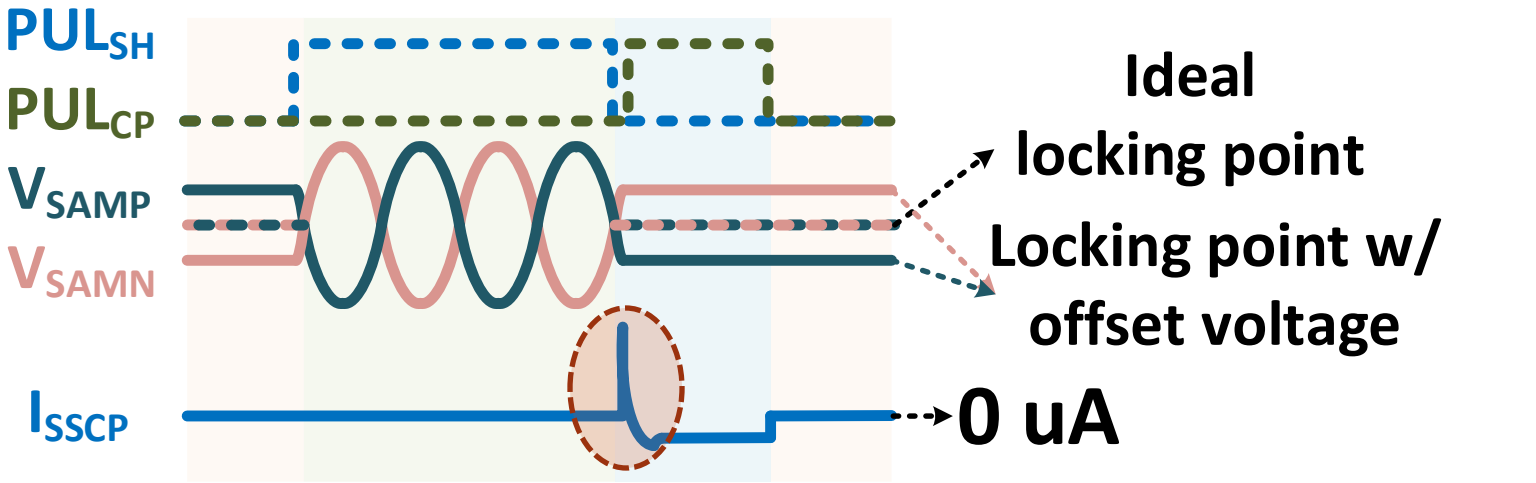
- 1st-Stage SSPLL
  - Increasing SSPD gain (GSSPD) to lower noise transfer function (NTF) of PD, CP, and LF
- Subsampling charge pump's offset current reduce the SSPD gain
  - An AC-coupled SSCP will be described later in the circuit technique section

$$\mathrm{NTF_{SSPD}} = \frac{\mathrm{Gain_{OL}}}{(1+\mathrm{Gain_{OL}})\mathrm{G_{SSPD}}} \downarrow$$

$\mathrm{G_{SSPD}} \uparrow$

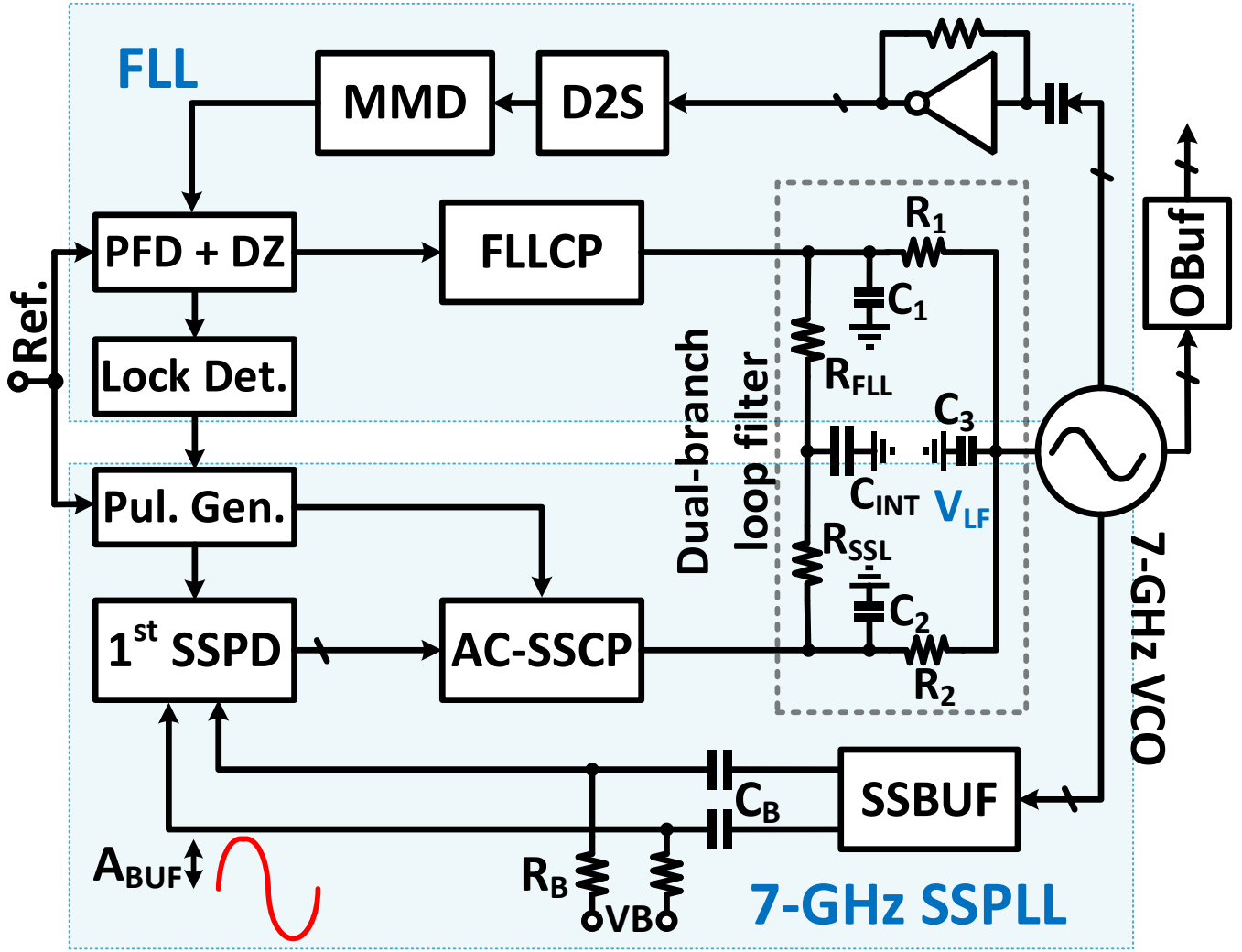
$$\mathrm{NTF_{SSCP}} = \frac{\mathrm{Gain_{OL}}}{(1+\mathrm{Gain_{OL}})\mathrm{G_{SSPD}}\mathrm{gm_{sscp}}} \downarrow$$

$$\mathrm{NTF_{LF}} = \frac{\mathrm{Gain_{OL}}}{(1+\mathrm{Gain_{OL}})\mathrm{G_{SSPD}}\tau_{\mathrm{PUL}}/\mathrm{T_{REF}}\mathrm{gm_{sscp}}\mathrm{R_{SSL}}} \downarrow$$



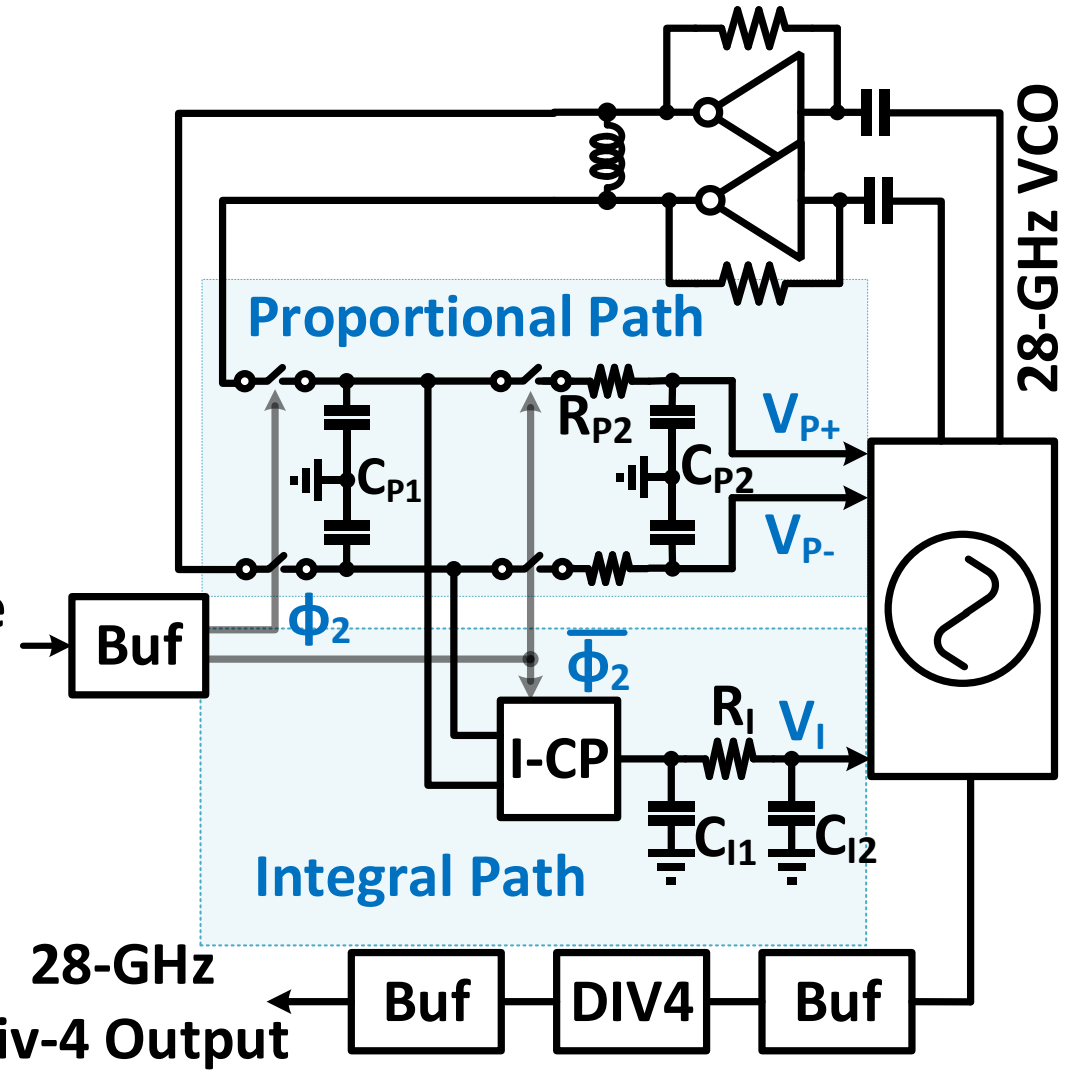
1st-Stage FLL

- FLL, an auxiliary loop
  - For initial frequency lock-in
- Interface between FLL and SSPLL: **Dual-branch loop filter**
  - Allows independent loop gain control for FLL and SSPLL



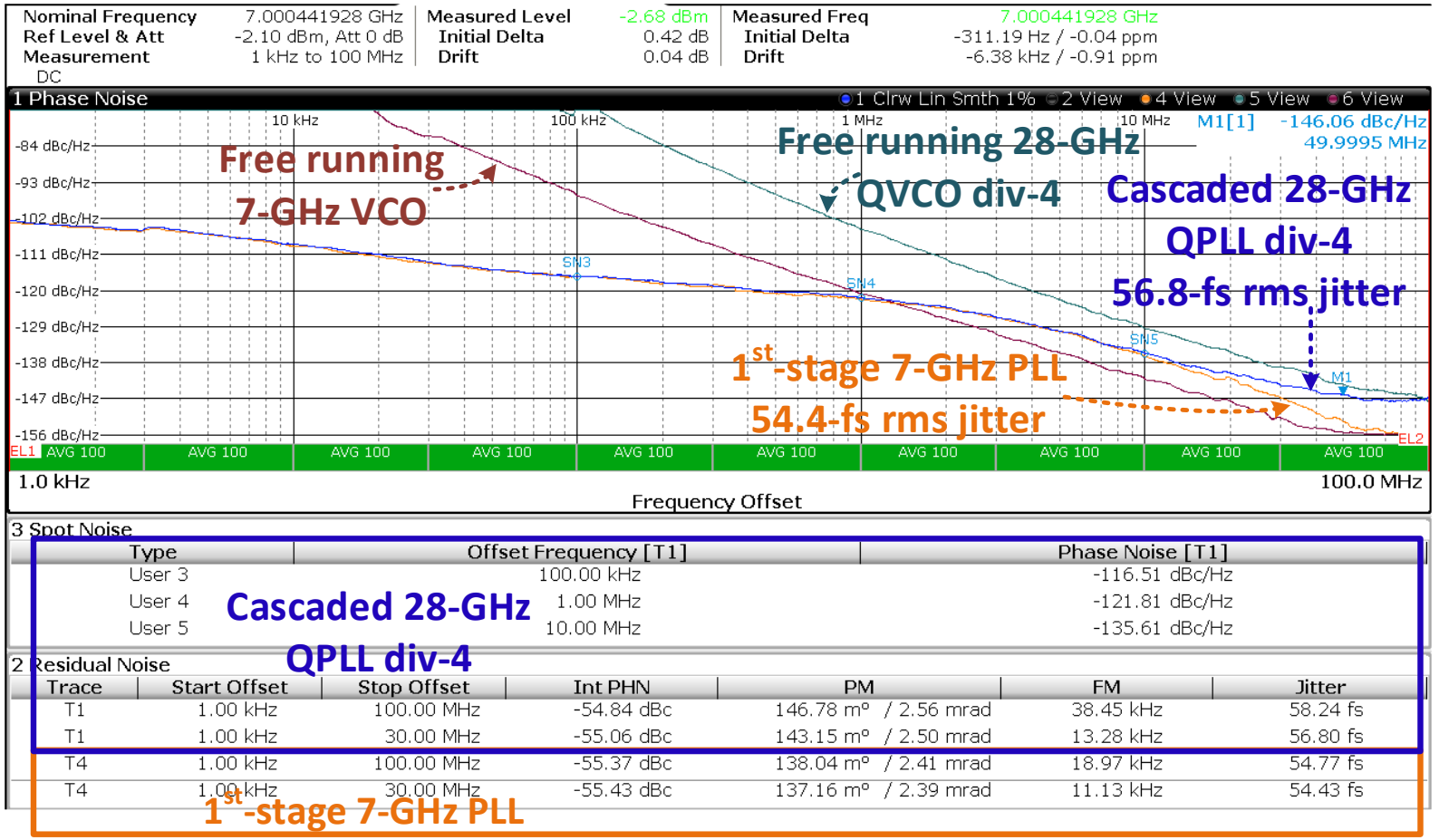
2nd-Stage High-Frequency DP-SSPLL

- The 2nd-stage, is a parallel **dual-loop architecture**
- Proportional path (P-path) dominates the overall loop dynamics, provides a wideband to regulate the VCO phase noise
- Integral path tracks frequency error
  - Enhances SSPD gain
  - ProvidesVCO close-in flicker noise suppression



Measured PLL Phase Noise Plot

- The 1st-stage RF SSPLL dominates the overall jitter
  - 1st-stage contributes 54.4-fs out of 56.8-fs total rms jitter
  - High frequency VCO phase noise is sufficiently attenuated
  - Over 1 kHz to 100 MHz range, QVCO PN profile is well above QPLL



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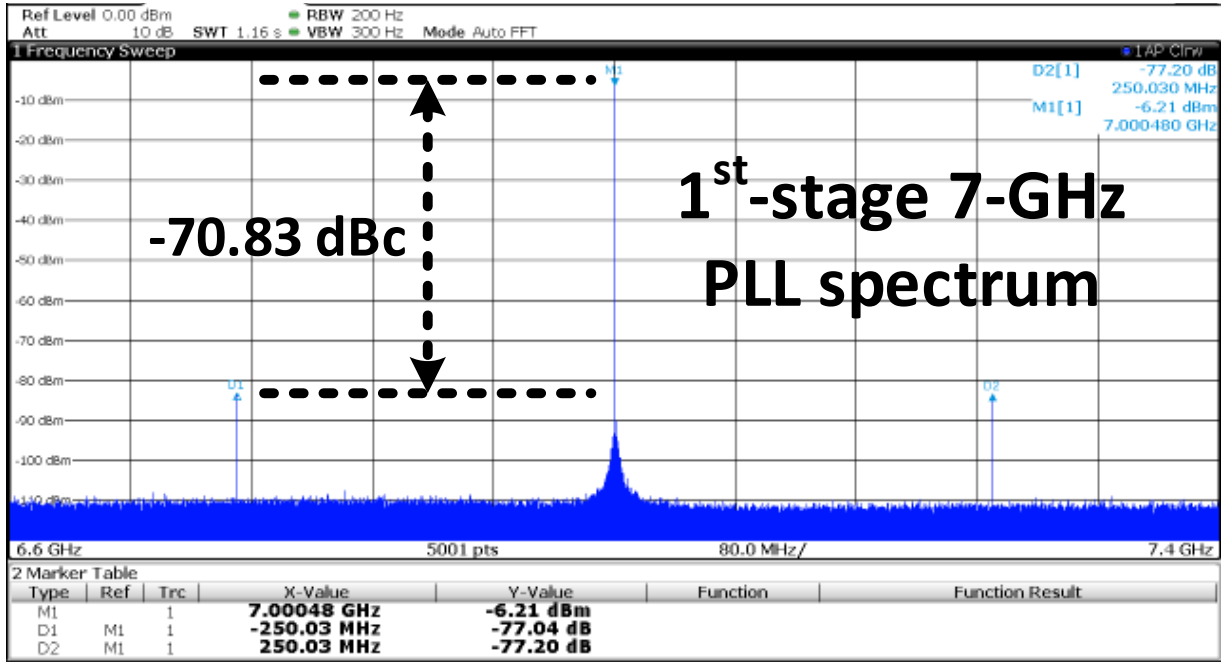
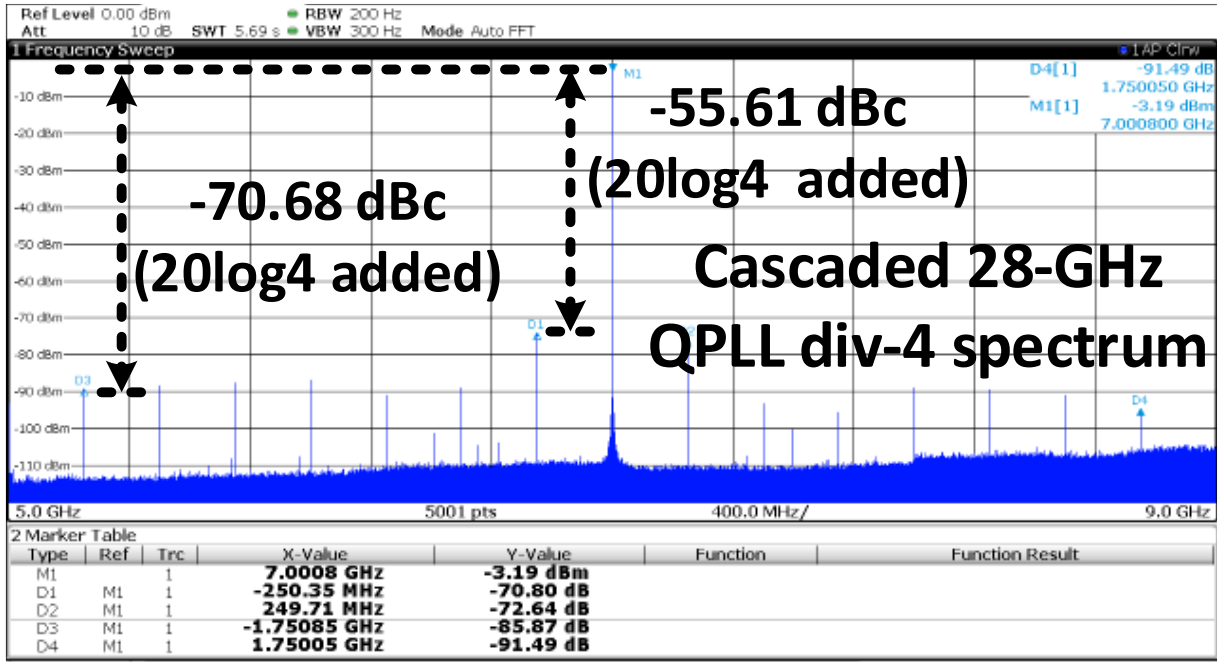
Measured Reference Spur

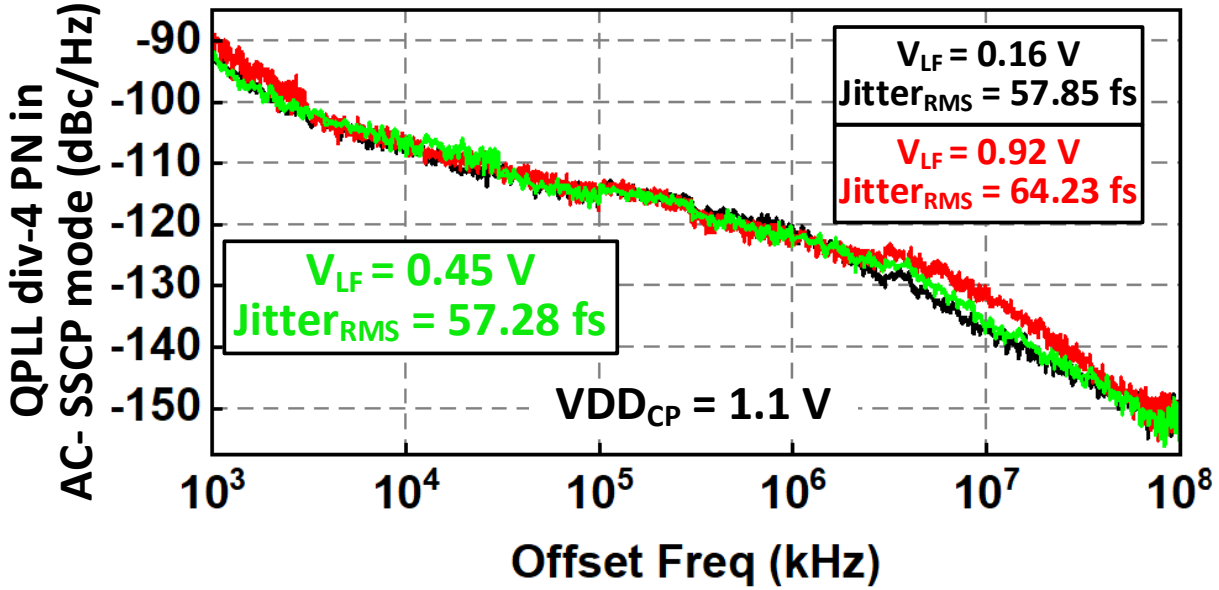


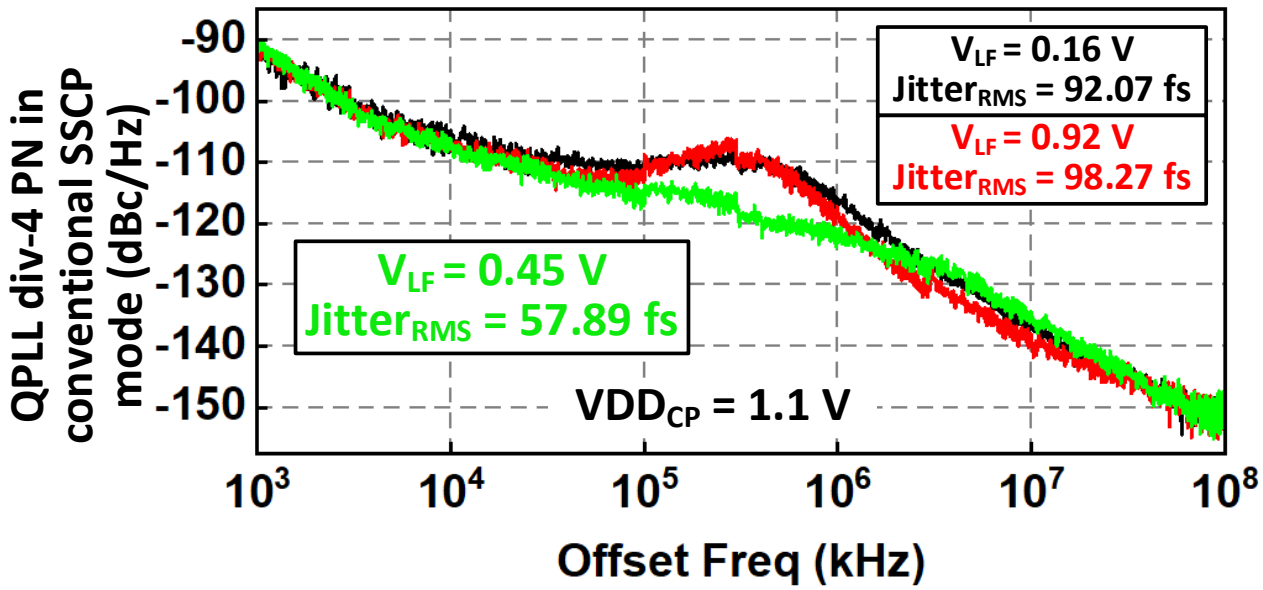


- 1st-stage RF SSPLL output spectrum, measured after an output buffer
- Cascaded 28-GHz PLL output spectrum, measured after a div-4 and output buffer

Measured Phase Noise Versus Loop Filter Voltage

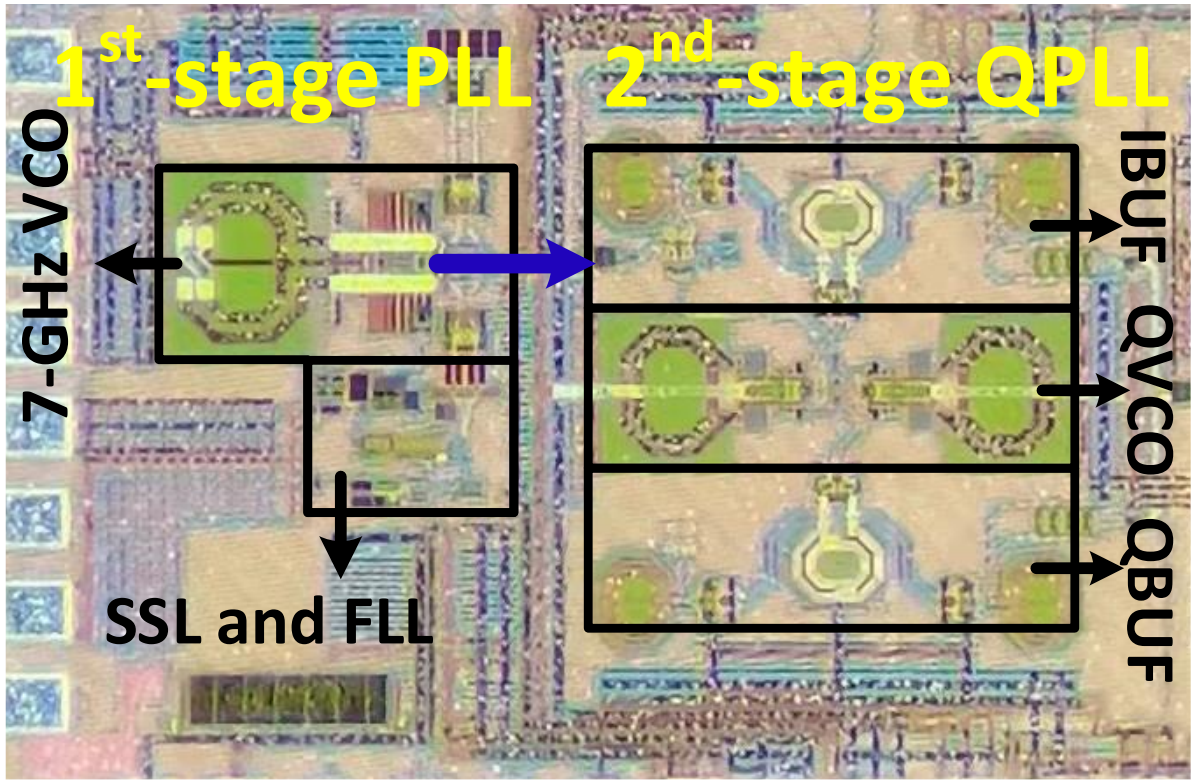
- By shorting the AC-coupling capacitor, and switching off the level alignment loop, the AC-SSCP is configured into a conventional SSCP
- By using the AC-SSCP, the phase noise and jitter performances remain robust over a loop filter voltage range from 0.16~0.92 V, under 1.1-V voltage supply

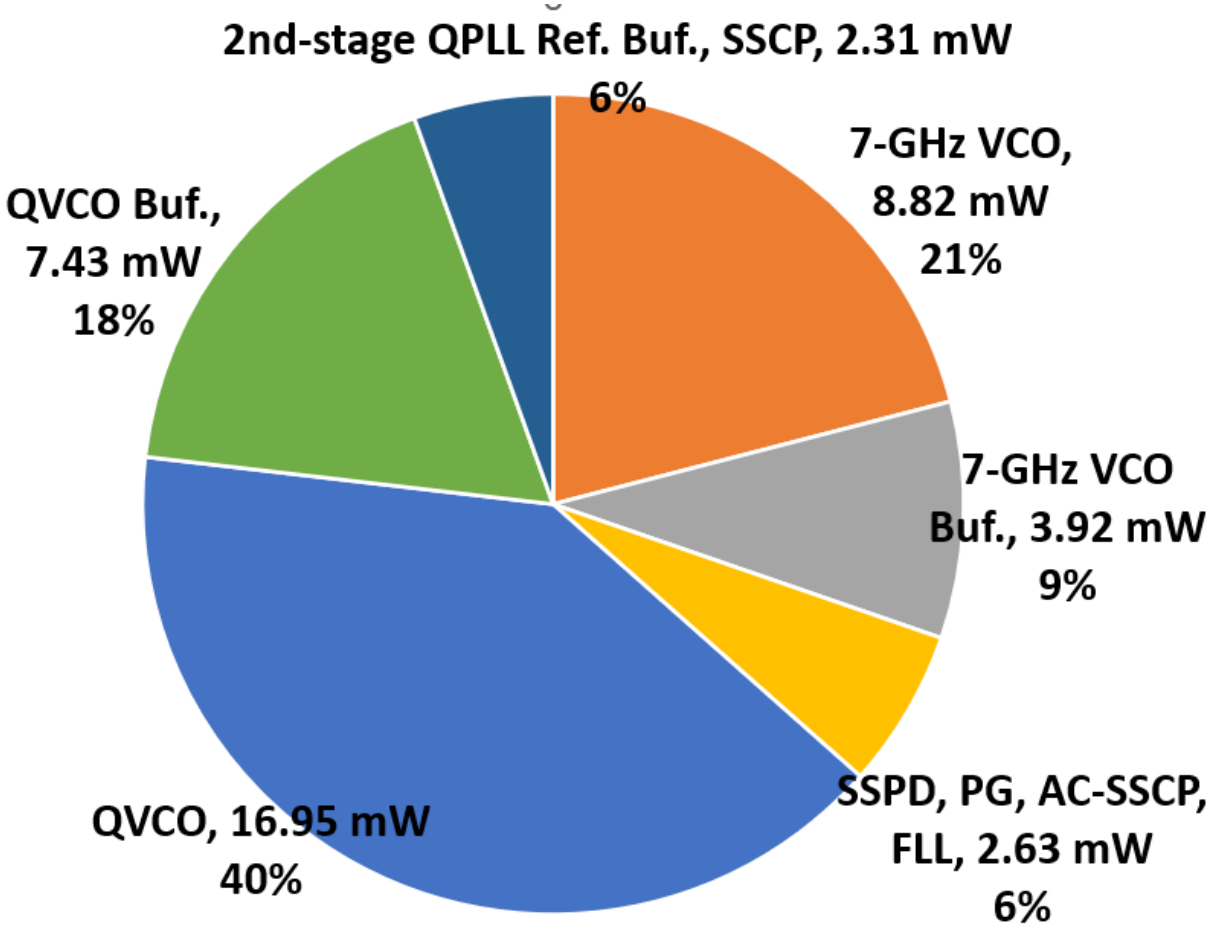




Die Micrograph and Power Breakdown

- Prototyped in 40-nm CMOS, core 0.4 mm^2





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Comparison Table

	Hu ISSCC20	EK JSSC18	Yang ISSCC22	Du VLSI21	Kim JSSC19	Liao JSSC20	This work
Tech	28nm	28nm	7nm	28nm	65nm	45nm	40nm
Arch.	CS + Harmonic extraction	Single-stage	Harmonic mixing	Harmonic extraction	Cascaded SS+QILO	Cascaded RSPLL+ ILFM	Cascaded SS+DP-SS
Freq. (GHz)	21.71~ 26.49	23.3~ 30.2	25~28	24~31	28~31	33.6~36	24.0~ 29.8
Freq. range	19.3%	25.8%	11.3%	25%	10.1%	6.9%	**21.4%**
Ref. (MHz)	250	491.5	74	50	100	80	250
Jitter (fs)	75.89 (10k~30M)	114	88	199 (10k~30M)	76 (1k~30M)	251 (10k~10M)	**56.8 (1k~30M)**
Spur (dB)	-45	-65.1	-61	-65	-58	-60	-55.6
Pdc (mW)	16.5	31	12.9	11.5	41.8	20.6	42. 1
FoM_{jitter} (dB)	-250.2	-244	-250	-243.3	-246.1	-238.9	**-248.6**
$FoM_{jitter-N}$ (dB)	-270.4	-261.2	-275.8	-270.9	-270.7	-265.3	-269.1
Area	0.5	N. M.	0.24	0.3	0.32	0.41	0.4

Conclusion

- A 24-30 GHz Cascaded PLL is designed and prototyped in 40nm CMOS for generating low-jitter clock
- The 1st-stage RF-SSPLL 6~7.5-GHz adopts an AC-SSCP and a GB-SSBUF to maximize the SSPD gain and hence suppress the in-band PN, yielding a low-jitter reference with 54.4-fs RMS jitter
- The 2nd-stage DP-SSPLL at 24-30 GHz uses a wide loop bandwidth (~100 MHz) to sufficiently suppressing the VCO phase noise
- The overall cascaded PLL achieves 56.8-fs RMS jitter, -55.6-dBc spur level, -248.6-dB FoM_{jitter} with 42.1-mW power consumption

Reference

- Y. Hu et al., "17.6 A 21.7-to-26.5GHz Charge-Sharing Locking Quadrature PLL with Implicit Digital Frequency-Tracking Loop Achieving 75fs Jitter and −250dB FoM," *2020 IEEE International Solid-State Circuits Conference - (ISSCC)*, San Francisco, CA, USA, 2020, pp. 276-278
- S. Ek et al., "A 28-nm FD-SOI 115-fs Jitter PLL-Based LO System for 24–30-GHz Sliding-IF 5G Transceivers," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 7, pp. 1988-2000, July 201
- D. Yang et al., "A Sub-100MHz Reference-Driven 25-to-28GHz Fractional-N PLL with −250dB FoM," *2022 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2022, pp. 384-386
- J. Du et al., "A 24–31 GHz Reference Oversampling ADPLL Achieving FoMjitter−N of -269.3 dB," *2021 Symposium on VLSI Circuits*, Kyoto, Japan, 2021, pp. 1-2
- J. Kim et al., "An Ultra-Low-Jitter, mmW-Band Frequency Synthesizer Based on Digital Subsampling PLL Using Optimally Spaced Voltage Comparators," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 12, pp. 3466-3477, Dec. 2019

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HKUST OWL

A Dual-Path Architecture: Motivation and Design Methodology

Outline

- Motivation
- System Architecture
- Measurement Results
- Conclusion

Outline

- **Motivation**
- System Architecture
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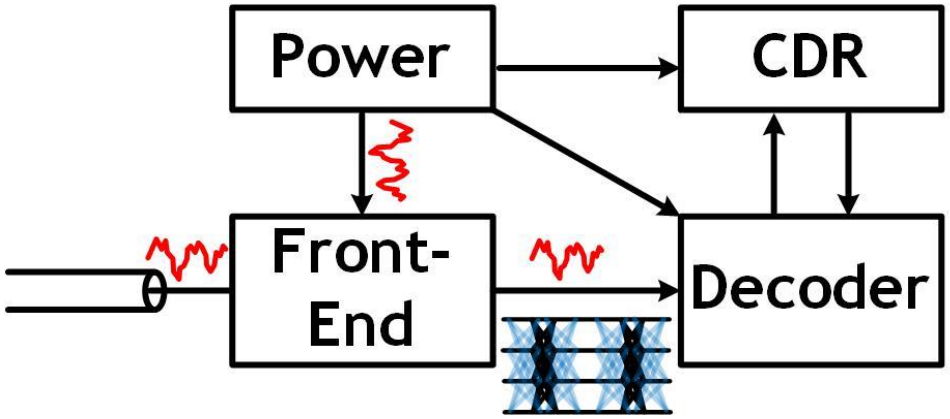
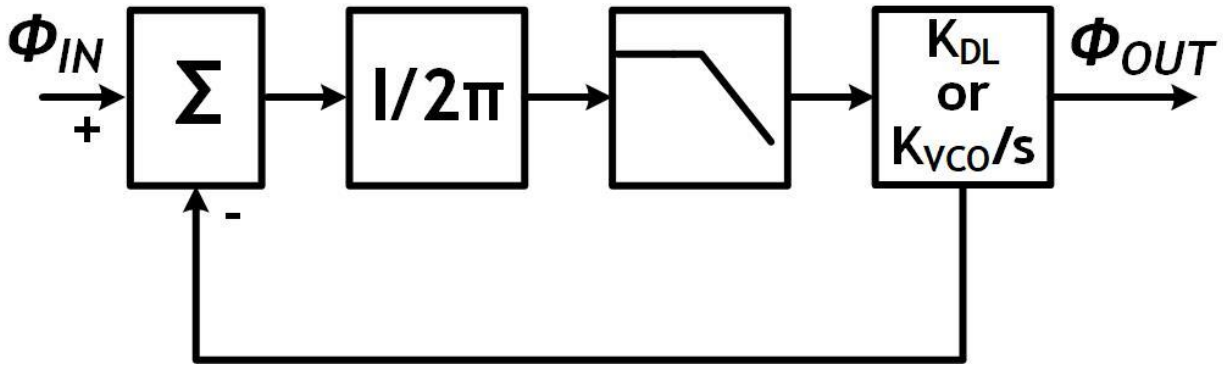
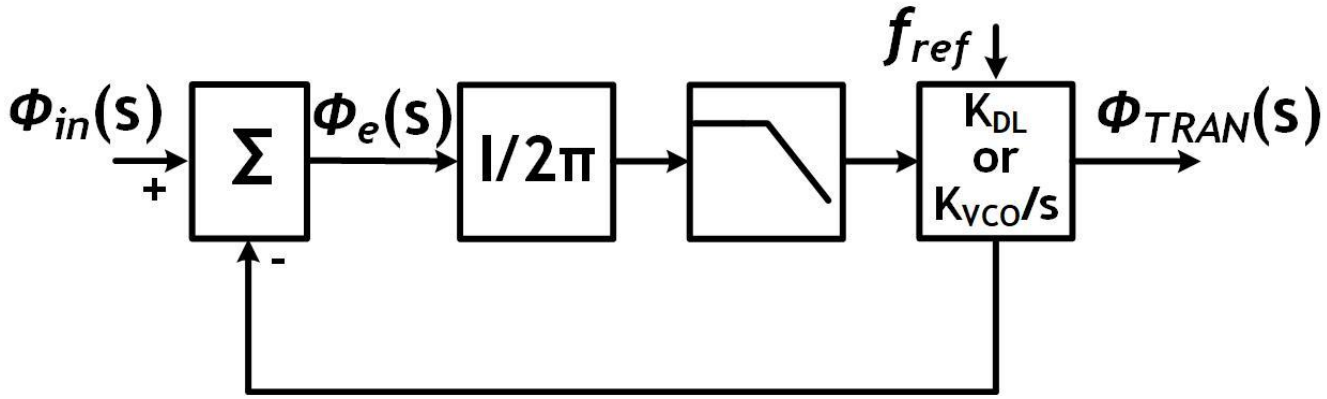
CDR in High-Speed I/O

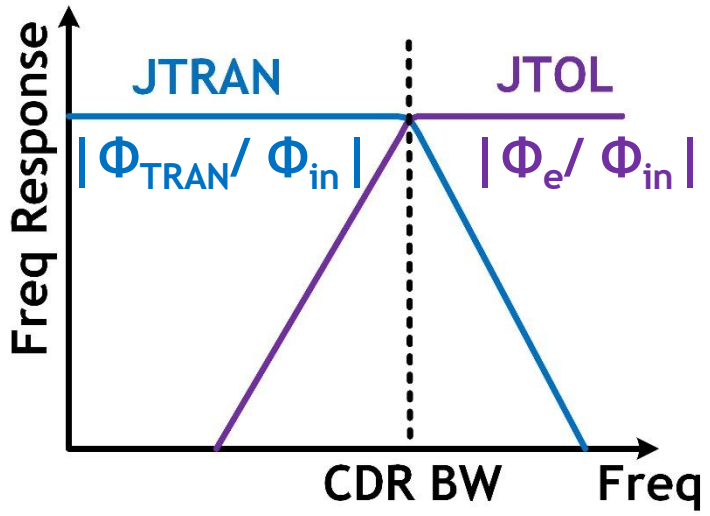




- Various sources introduce jitter through AM-PM conversion
  - Channel, circuit, supply noises
  - Temperature and supply variation
- Clock and data recovery (CDR) ensures robust jitter tracking and decoding

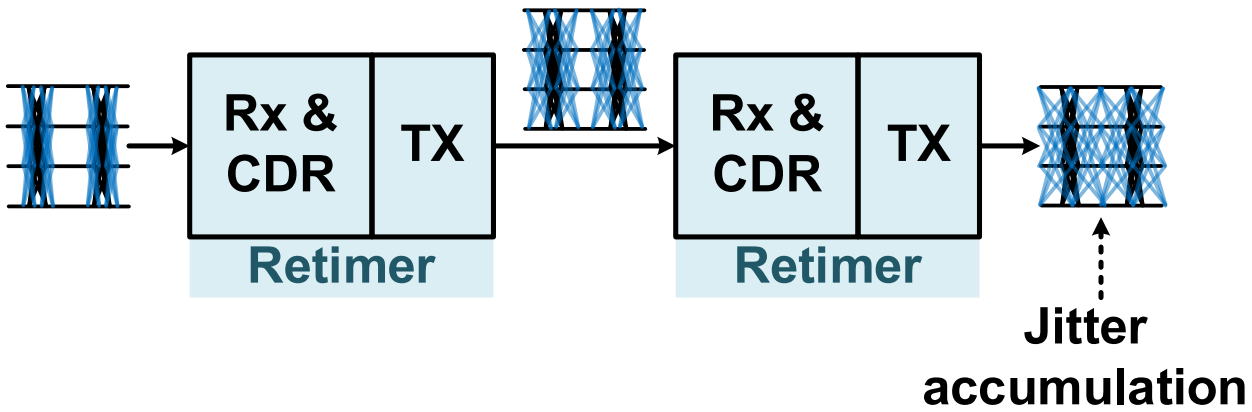
Tradeoff between JTRAN and JTOL

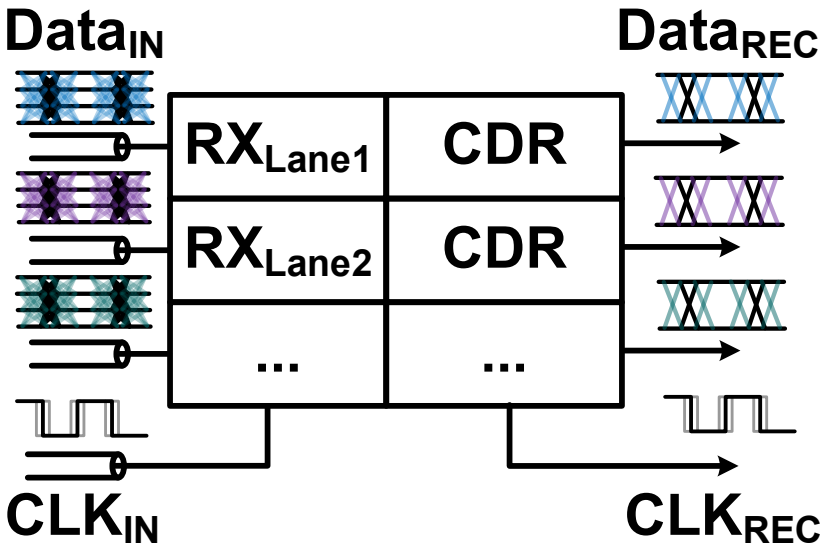




- **Expected:** Wide jitter tolerance bandwidth (JTOL BW) with narrow jitter transfer bandwidth (JTRAN BW).
  - Lower probability of generating error
  - Lower jitter on recovered data and clock
- Both JTOL and JTRAN BW are fixed by the CDR loop BW.

Issues of Large Jitter Transfer

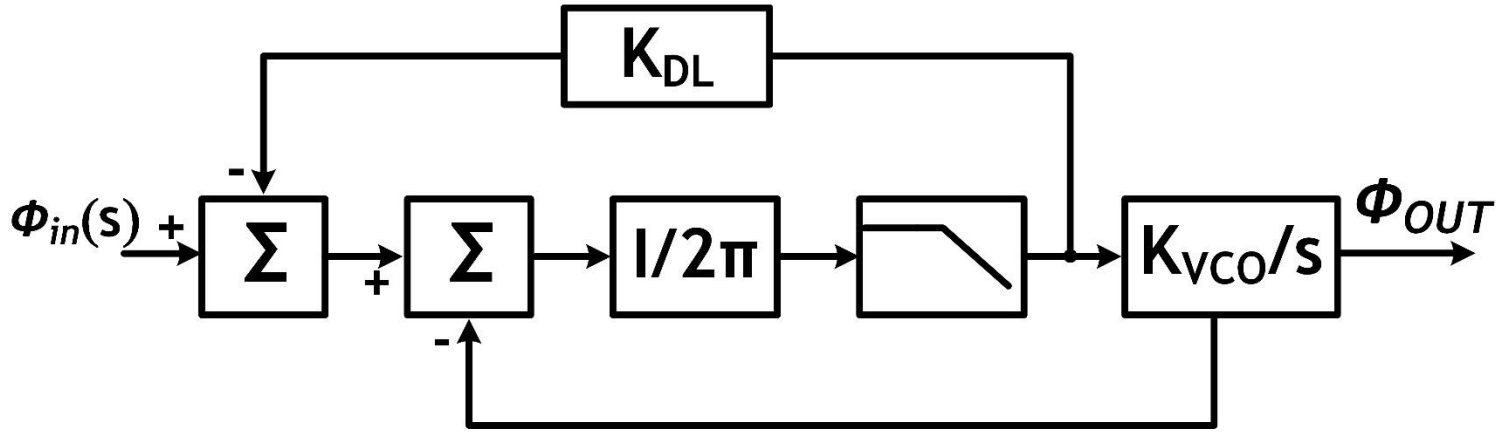




- Large jitter transfer leads to:
  - **Jitter accumulation** over multiple stages
  - **Uncorrelated jitter** across multiple parallel transceivers

Conventional Dual-Loop/Path Architecture

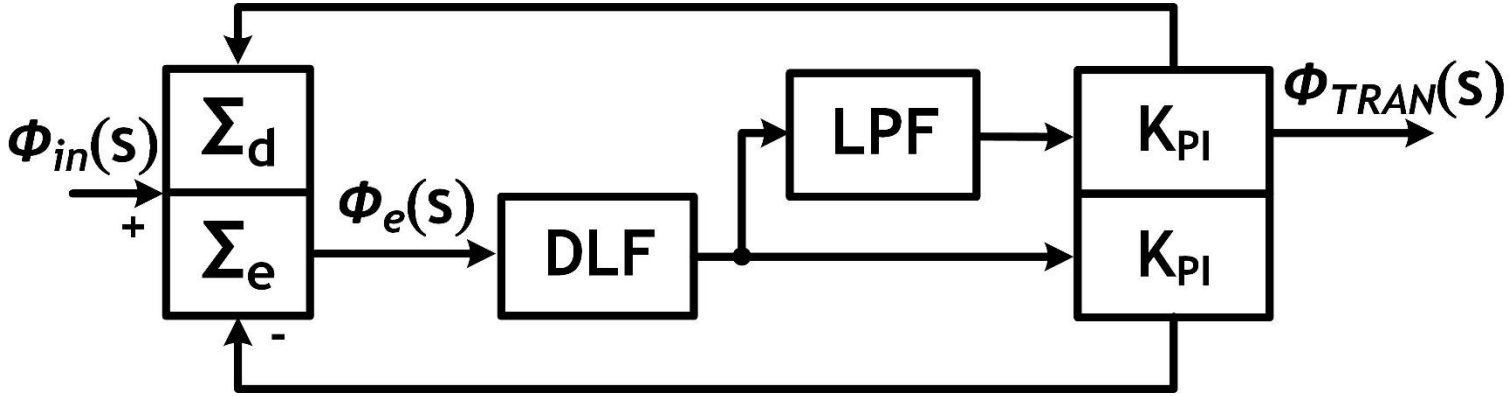
- Delay/Phase-locked loop (D/PLL) based dual-loop CDR



- **Fast proportional path**
- **Slow integral path**

[G. SHU, JSSC2015]

- Separated loop filters for data sampling and edge sampling



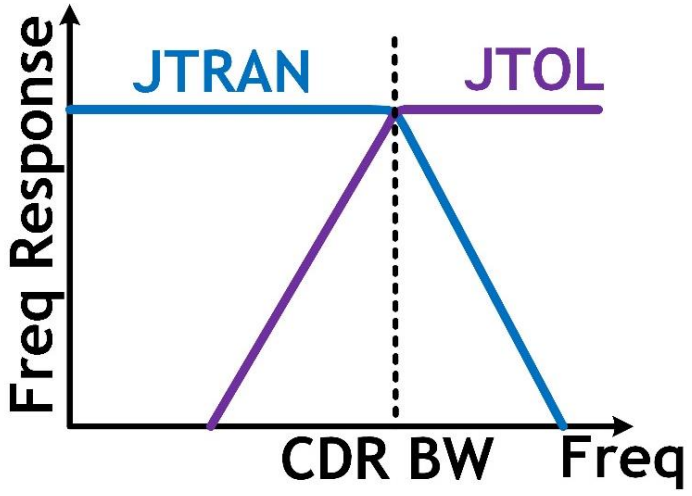
- **Fast edge path**
- **Slow data path**

[X. ZHENG, JSSC2017]

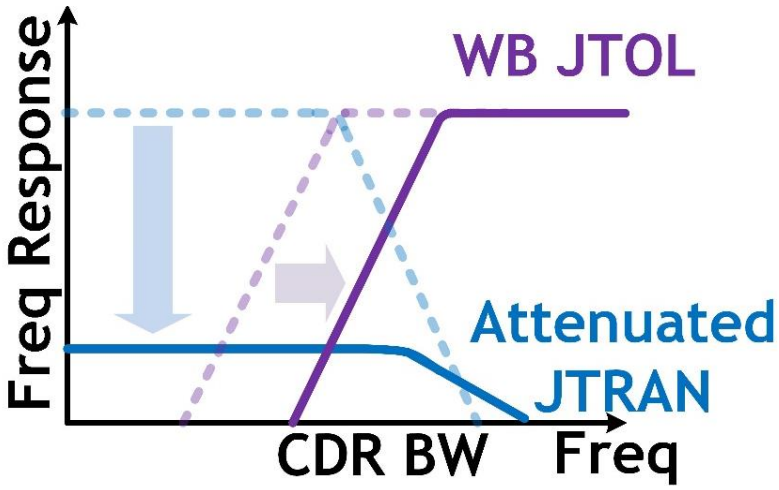
[M Hossain, VLSI2014]

Motivation

Conventional



Proposed

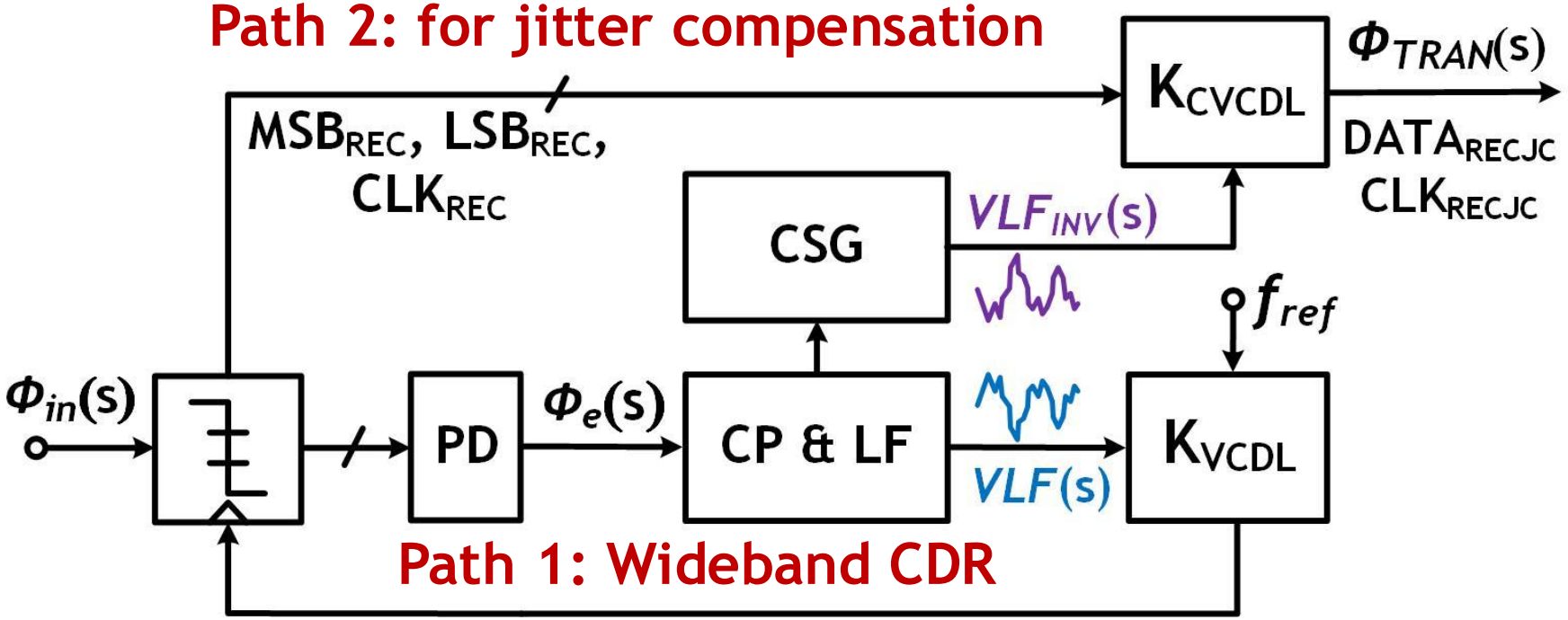


- Challenges:
  - Conventional dual-loop CDR not applicable to PAM4 ¼-rate RX
  - Low frequency jitter cannot be attenuated.
- Design targets:
  - High data rate, 60-Gbps, quarter-rate architecture
  - Narrow jitter transfer, wideband jitter tolerance

Outline

- Motivation
- **System Architecture**
- Circuit Description
- Measurement Results
- Conclusion

Conceptual Dual-Path RX Architecture



PD: phase detector

CP: charge pump

LF: loop filter

VLF: loop filter voltage

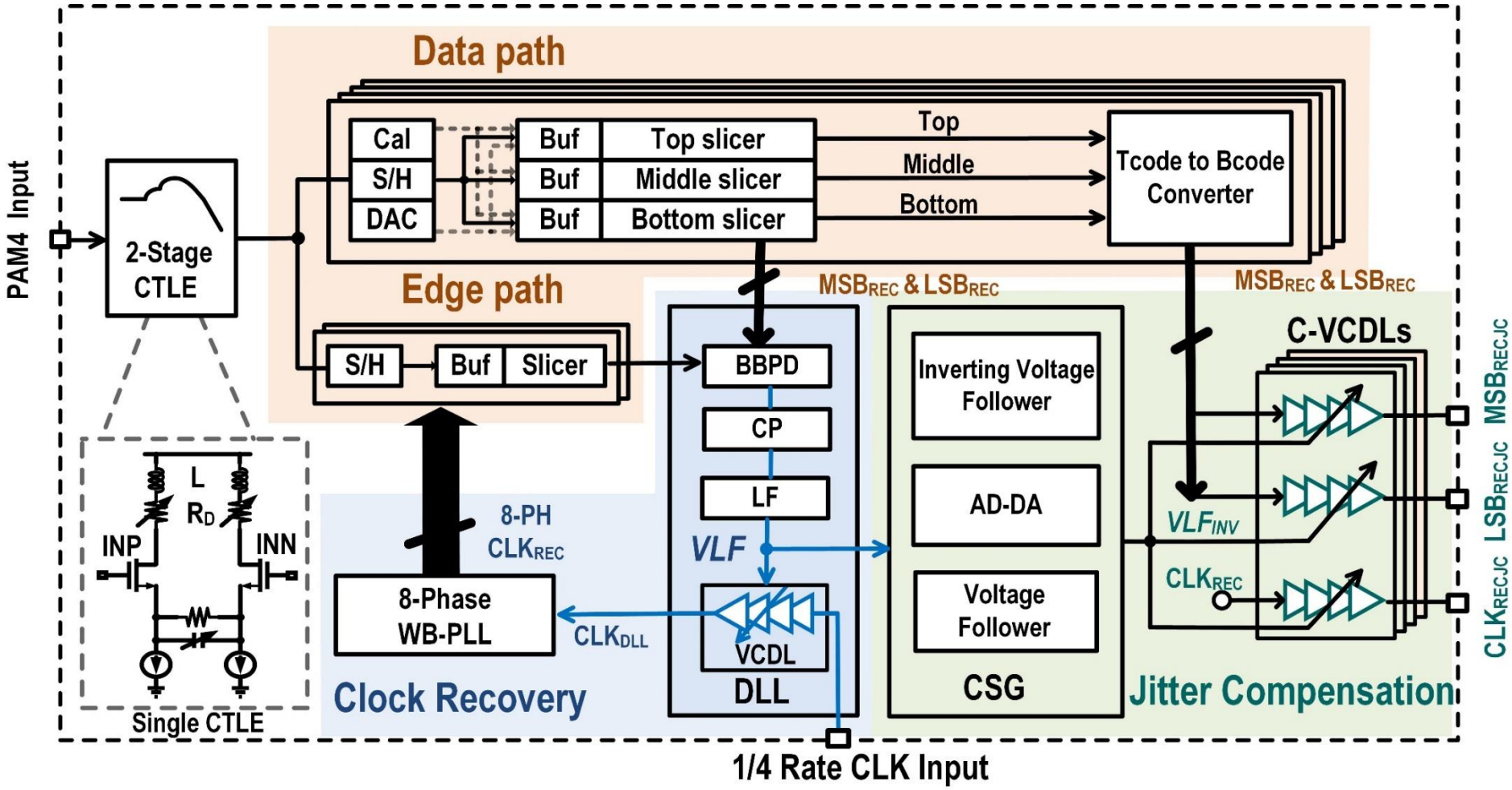
VLF_{INV}: inverted VLF

VCDL: voltage-controlled delay line

CSG: complementary signal generator

- Path 1: 40-MHz wideband CDR for large jitter tolerance
- Path 2: jitter compensation path

Detailed Block Diagram



Tcode: thermometer code

Bcode: Binary Code

LF: loop filter

VLF: loop filter voltage

VLF_{INV}: inverted VLF

VCDL: voltage-controlled delay line

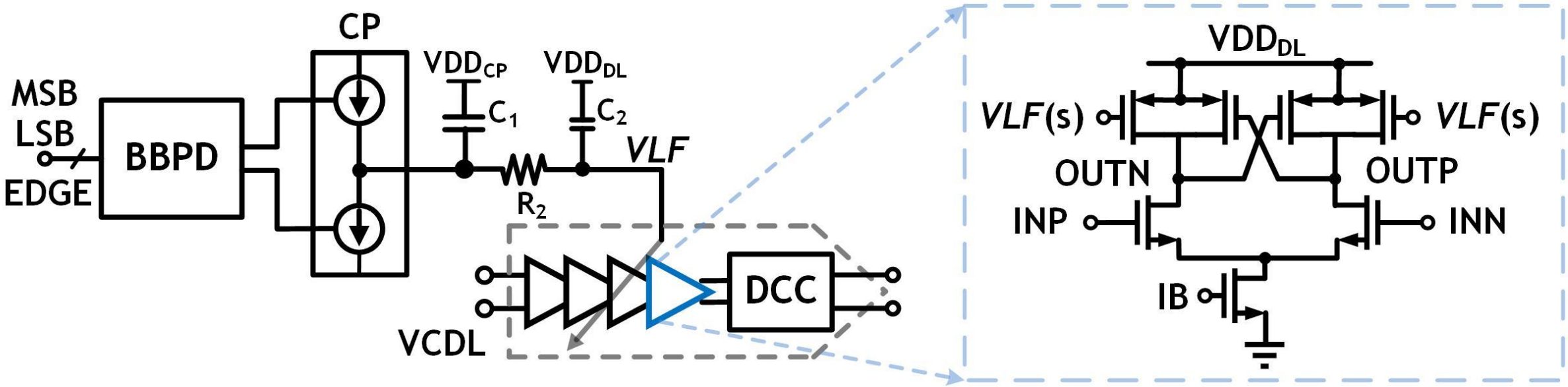
CVCDL: Complementary voltage controlled delay line

CSG: complementary signal generator

CLK_{REC}: recovered clock

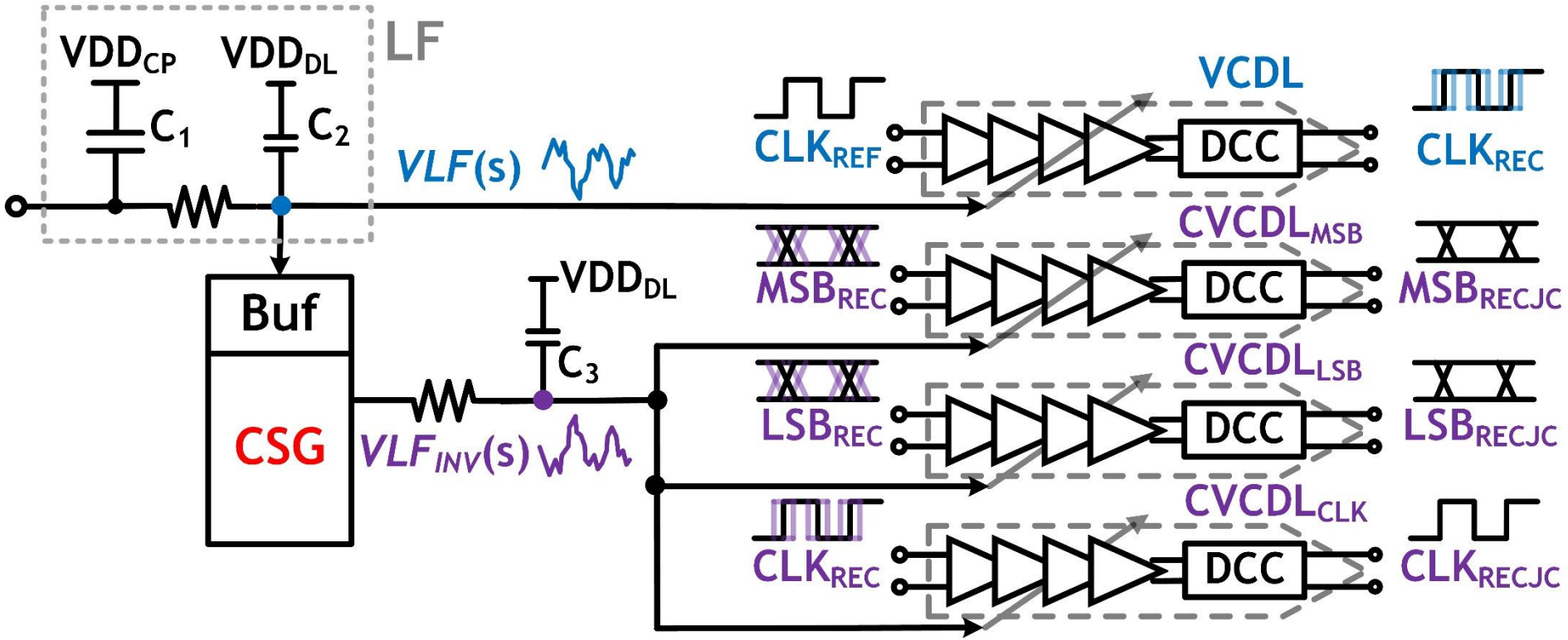
CLK_{RECJC}: recovered clock after jitter compensation

Delay-Locked Loop



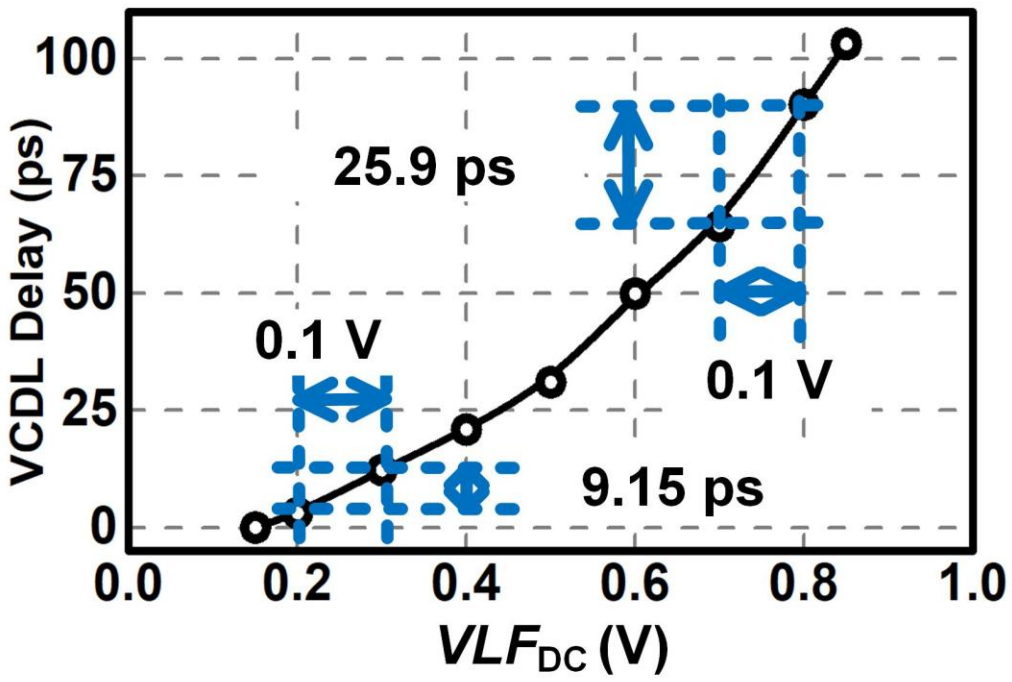
- C_1>>C_2 alleviates the effects of CP current steering on VDD_{DL}.
- R_2, C_2 filter out the spur due to charging and discharging.
- *VLF*(s) controls the time constant of output rising edge.
- Duty cycle correction (DCC) and cross-coupled PMOS ensures 50% duty cycle.

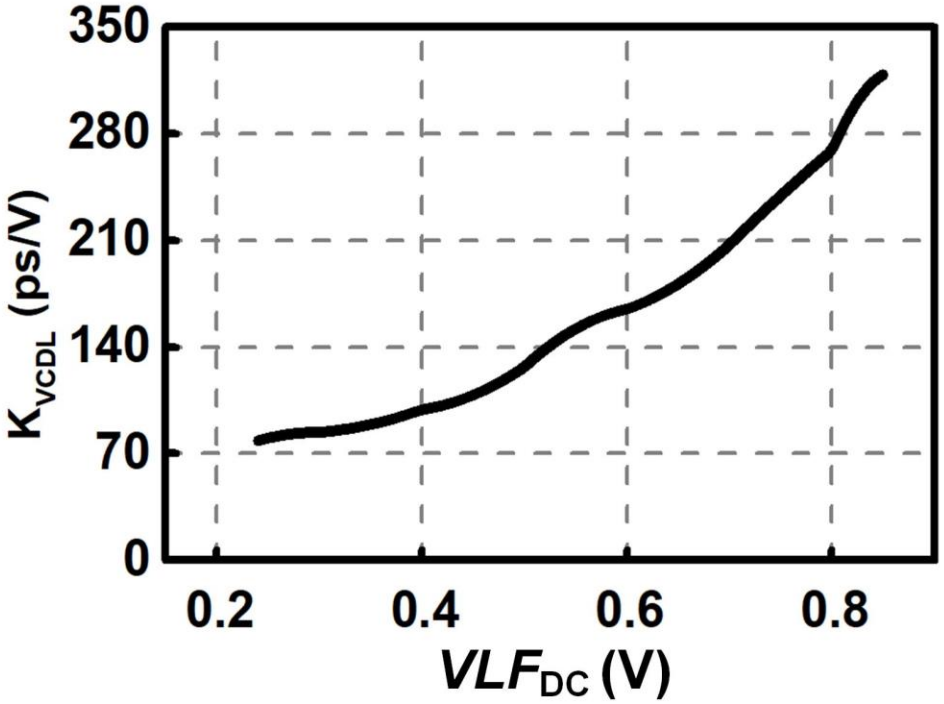
Jitter Compensation Block Following the DLL



- Complementary signal generator (CSG) generates VLF_{INV}, controlling CVCDL to compensate the jitter from DLL.
- VCDL and CVCDL adopt identical layouts, with dummy in middle and two sides to improve matching.

Characteristics of VCDL



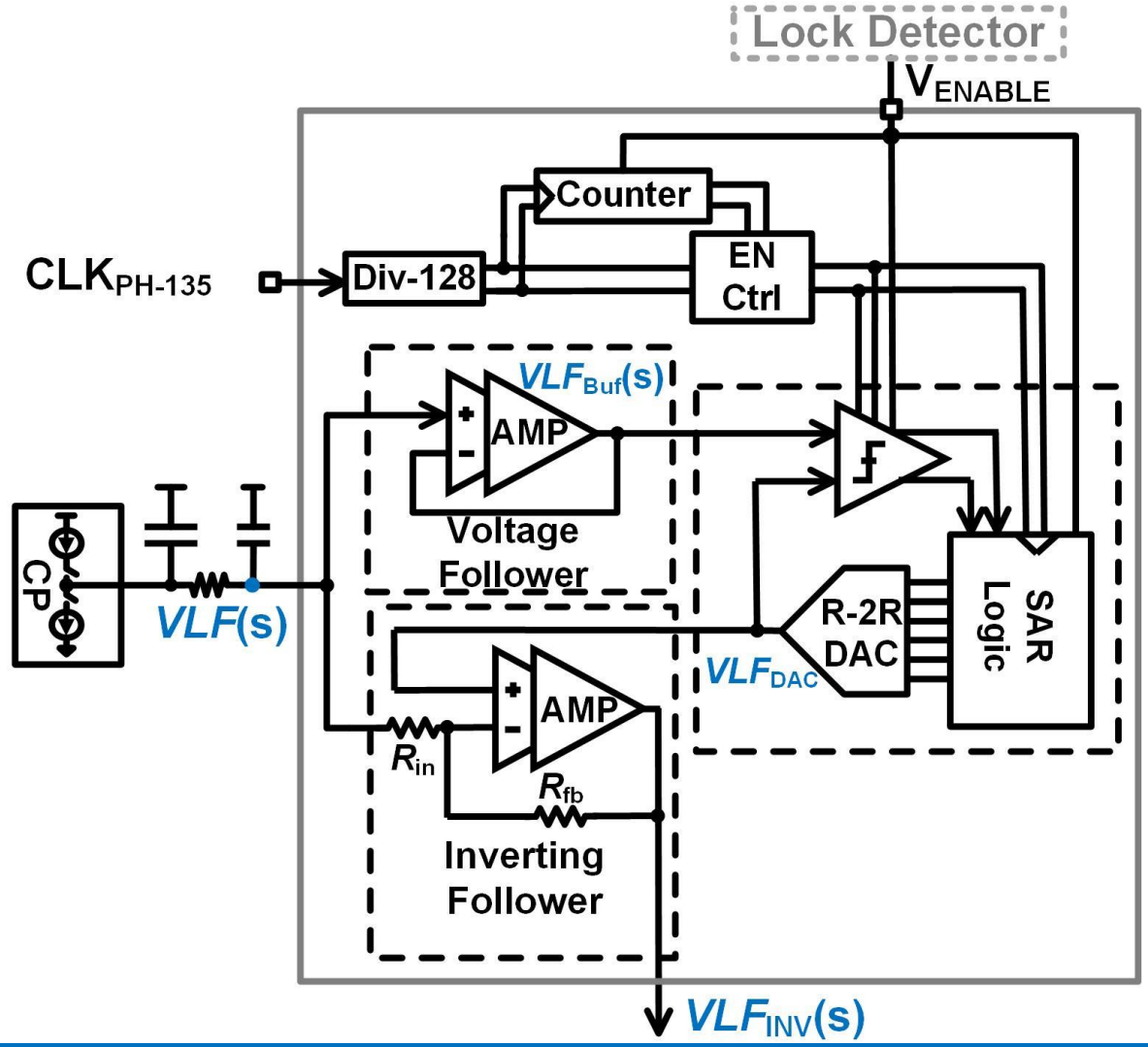


- VCDL covers a delay range from 0~105 ps, with VLF_{DC} from 0.15 ~ 0.85 V.
- K_{VCDL} varies from around 70 ps/V to 300 ps/V, from 0.15 ~ 0.85 V.

- **CVCDL should be operated at the same DC level as VCDL to match their gain.**

Complementary Signal Generator

- Voltage follower isolates *VLF*(s) from comparator kick-back noise.
- 8-bit SAR-ADC detects the DC level of $VLF_{Buf}(s)$.
- Inverting follower receives *VLF*(s) and VLF_{DAC} and generate $VLF_{INV}(s)$.

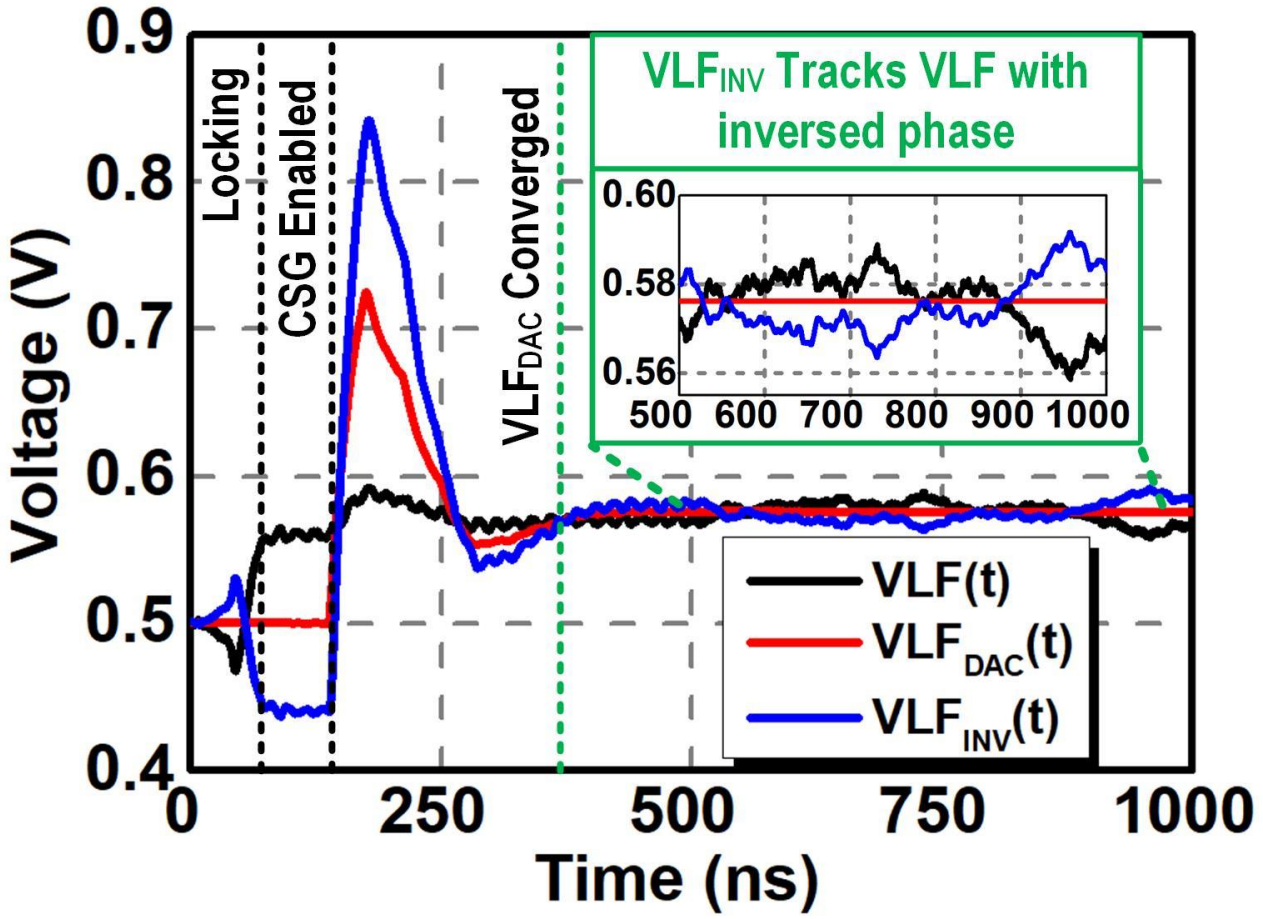


Transient Simulation of CSG

- Stage-1: DLL locked within around 20ns
- Stage-2: CSG enabled to yield VLF_{DAC} within 200ns
- Stage-3: CSG converged, jitter compensation started

➢ Enough tracking accuracy

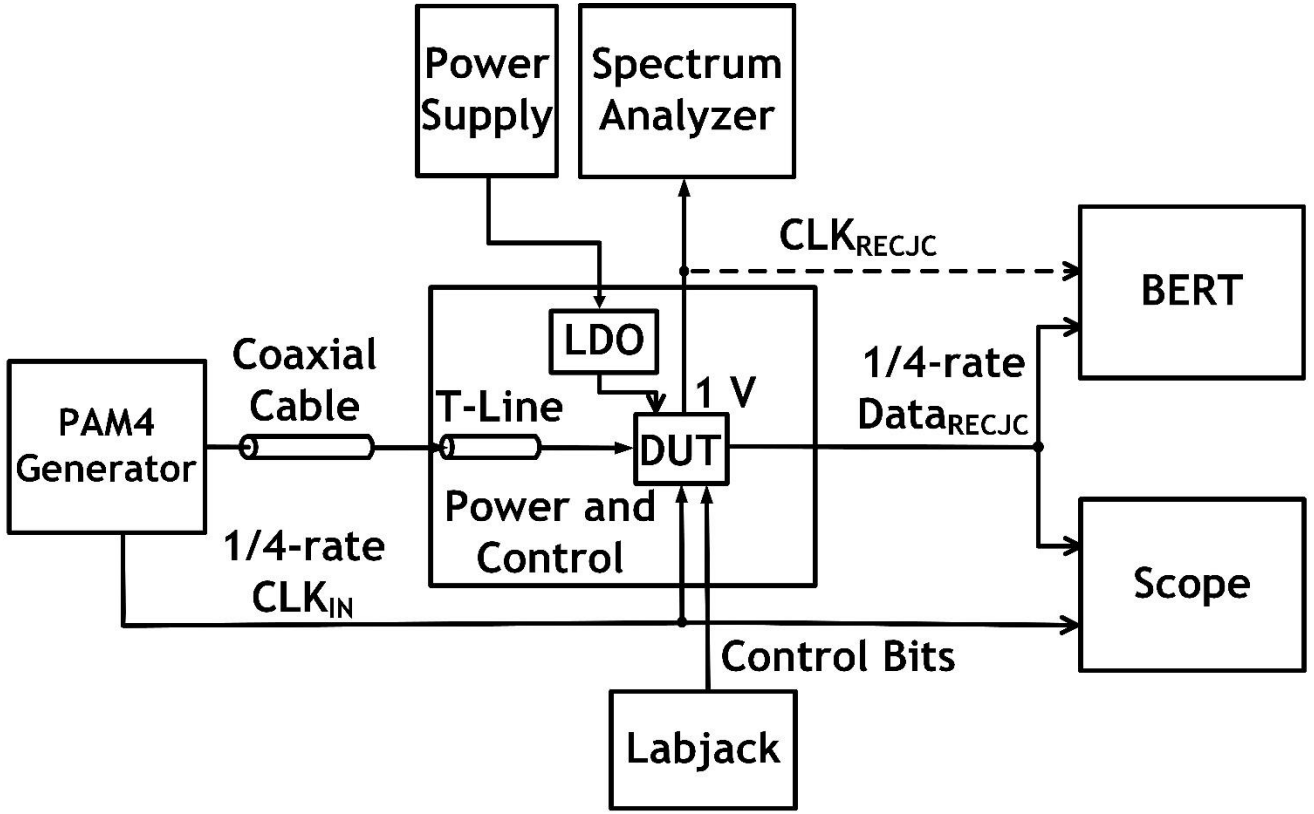
➢ Faster convergence speed compared to low pass filter method

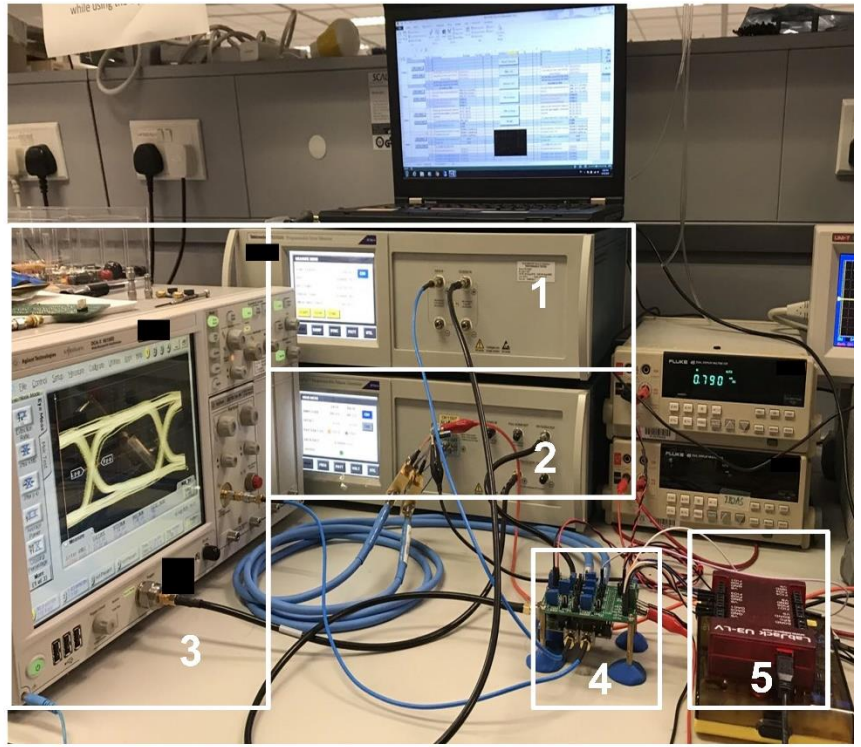


Outline

- Motivation
- Conceptual System Architecture
- Circuit Description
- **Measurement Results**
- Conclusion

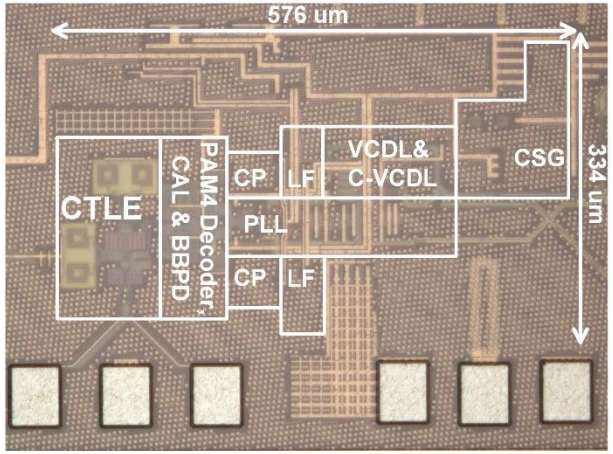
Measurement Setup

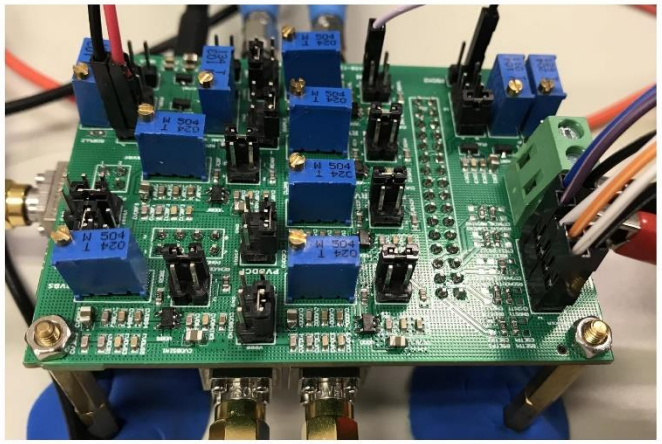




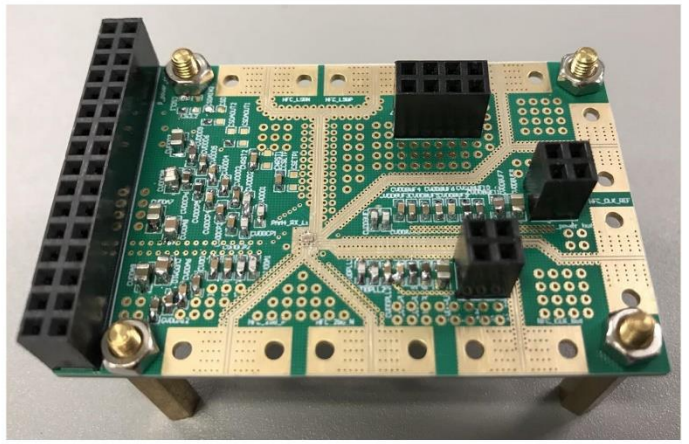
1. Bit error rate tester (BERT); 2. Pattern generator; 3. Scope;
4. Chip on power and control PCB module; 5. Labjack

Chip Diagram and Testing Modules





Power and control board



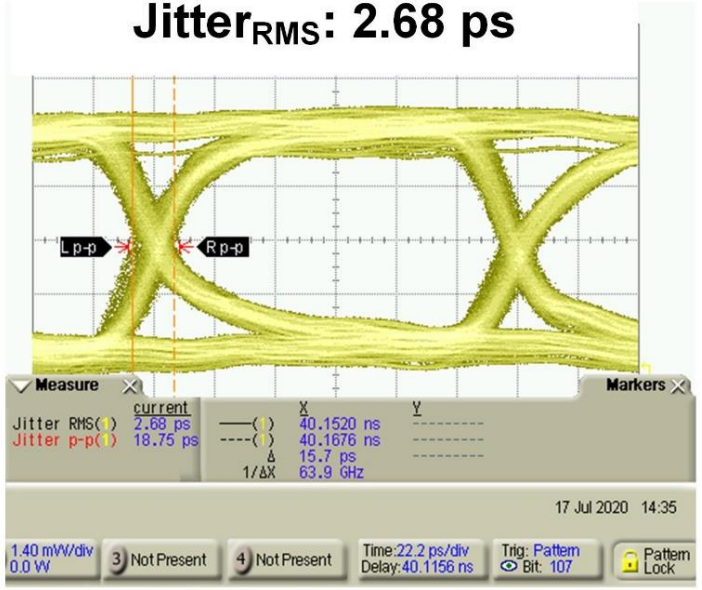
High frequency board

- Chip:
  - Fabricated in TSMC's 40-nm CMOS process
  - Active area: 334 μm x 576 μm
- Testing Module
  - Power and control board & High frequency board

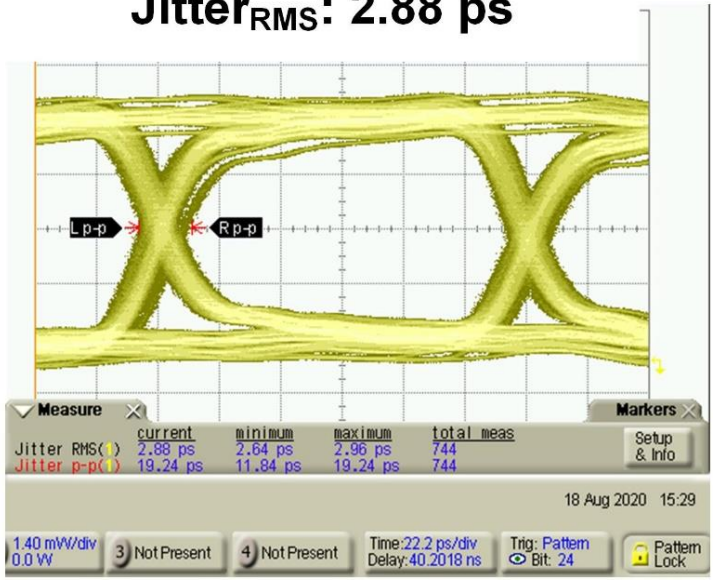
Recovered ¼-Rate Data and Clock

7.5 GHz CLK_{RECJC}
$Jitter_{RMS}$: 0.97 ps

7.5 Gb/s MSB_{RECJC}
$Jitter_{RMS}$: 2.68 ps

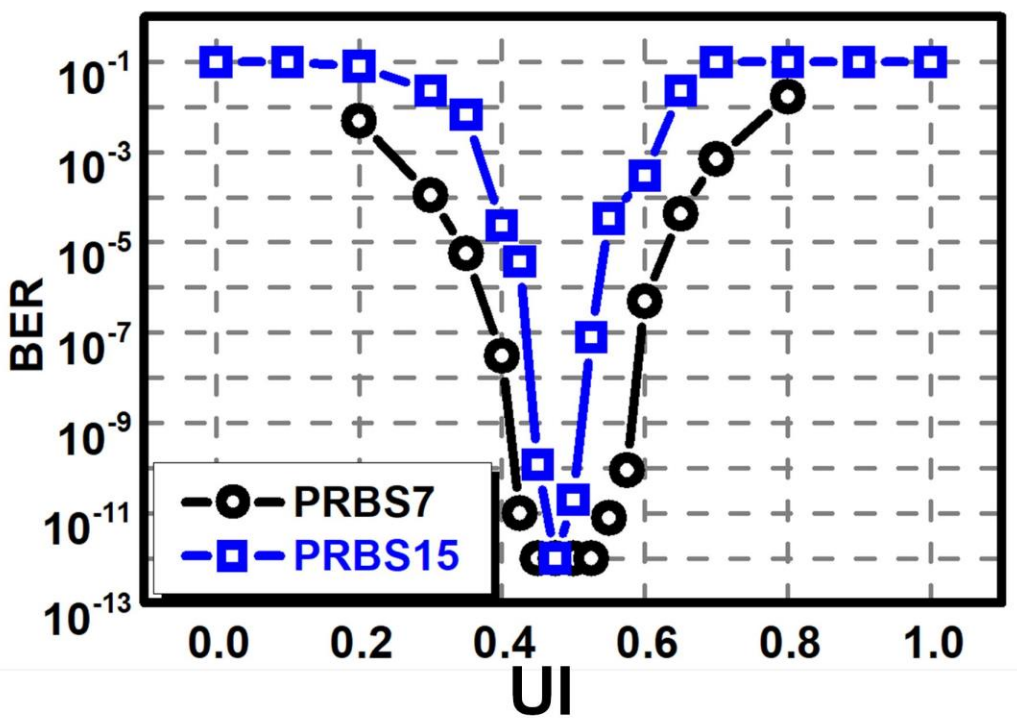


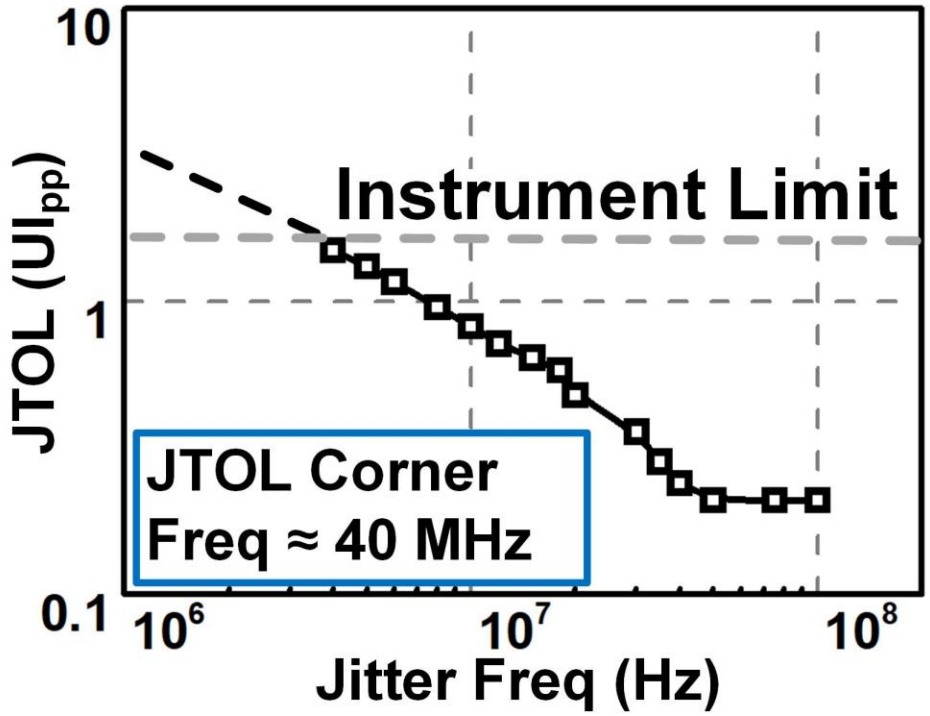
7.5 Gb/s LSB_{RECJC}
$Jitter_{RMS}$: 2.88 ps



- 60-Gb/s PAM-4 input, recovered 7.5-GHz CLK, 7.5-Gb/s MSB and LSB

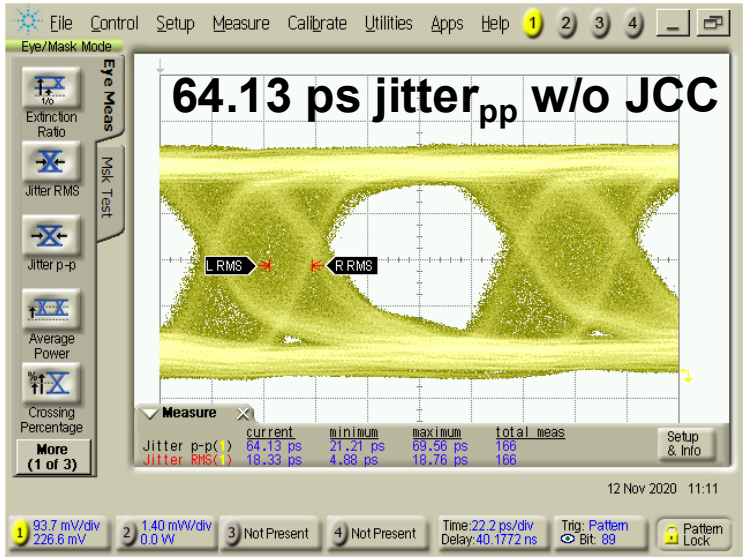
Measured Bathtub Curve and JTOL

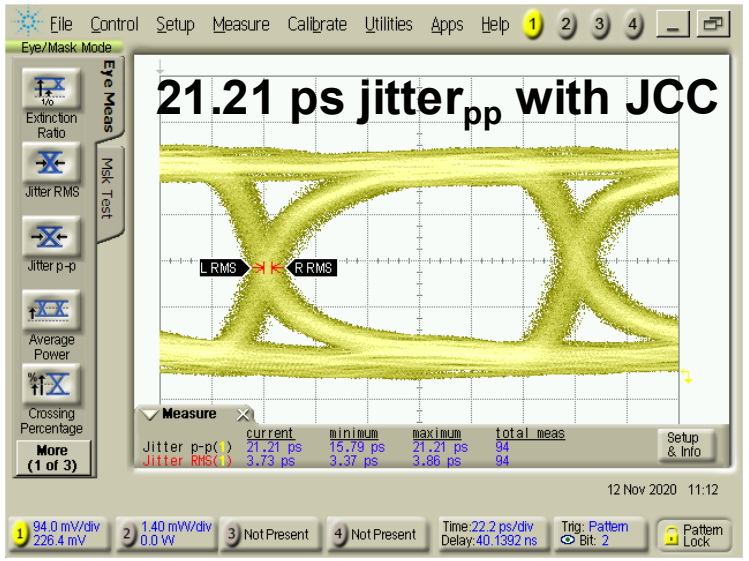


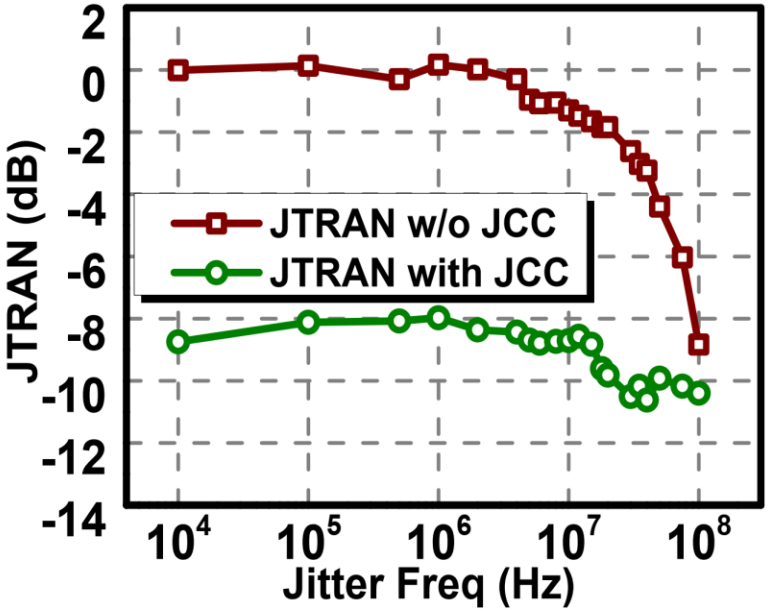


- The eye opening is 0.25 UI for PRBS-7 and 0.12 UI for PRBS-15 (FEC=1E-6)
- JTOL: 0.2 UI_{PP} at a corner frequency of 40 MHz

JTRAN Measurement





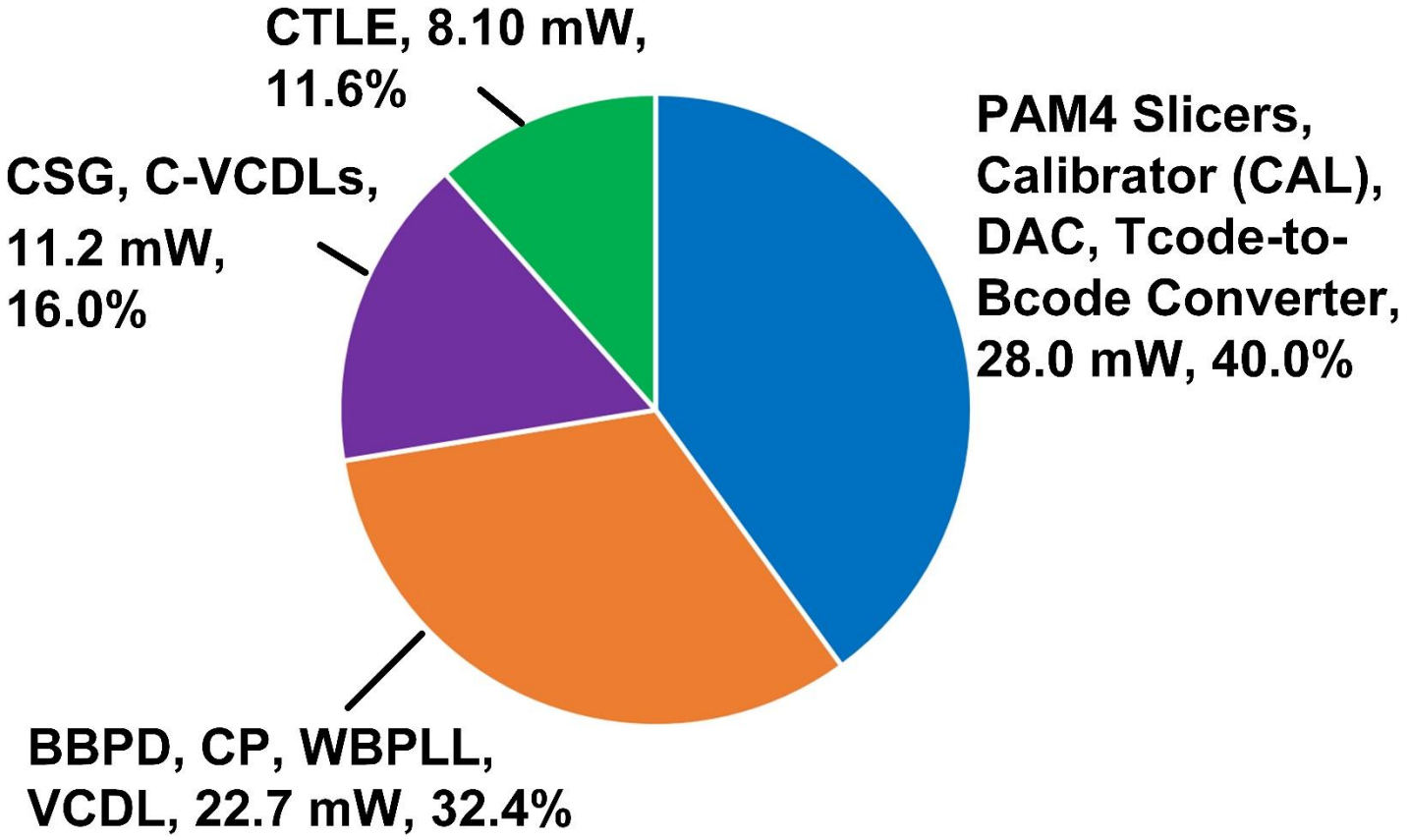


- By enabling the jitter compensation function, the jitter$_{PP}$ in the eye diagram can be reduced from 64 ps to 21 ps, 66% reduction
- The JTRAN is attenuated to below -8 dB with the jitter compensation circuit

Comparison Table

	[2] JSSC'16	[3] VLSI'14	[4] JSSC'17	[5] JSSC'19	**This work**
Technology	28 nm	65 nm	65 nm	28 nm	**40 nm**
Architecture Signaling Scheme	1/4-rate NRZ	1/4-rate NRZ	1/4-rate NRZ	1/4-rate PAM4	**1/4-rate PAM4**
Rate [Gb/s]	16-32	14	40	64	**30-60**
Power [mW]	4.87	7.8	225	180	**70.8**
Eff. [pJ/bit]	0.153	0.56	5.625	2.8	**1.18**
JTOL [UI_{PP}] @ Corner Freq.	None	0.1 UI_{PP} @1 MHz	0.41 UI_{PP}* @20 MHz	0.1 UI_{PP} @10 MHz	**0.2 UI_{PP} @40 MHz**
JTRAN @ 0.1 MHz	None	0 dB	0 dB	None	**-8 dB**
JTRAN @ @ Corner Freq.	None	-3 dB @ 1 MHz	-3 dB @ 4 MHz	None	**-10 dB @ 40 MHz**
Supply (V)	1.0	0.8	1.2	1.0	**1.0**

Power Breakdown



Total Power: 70.8 mW

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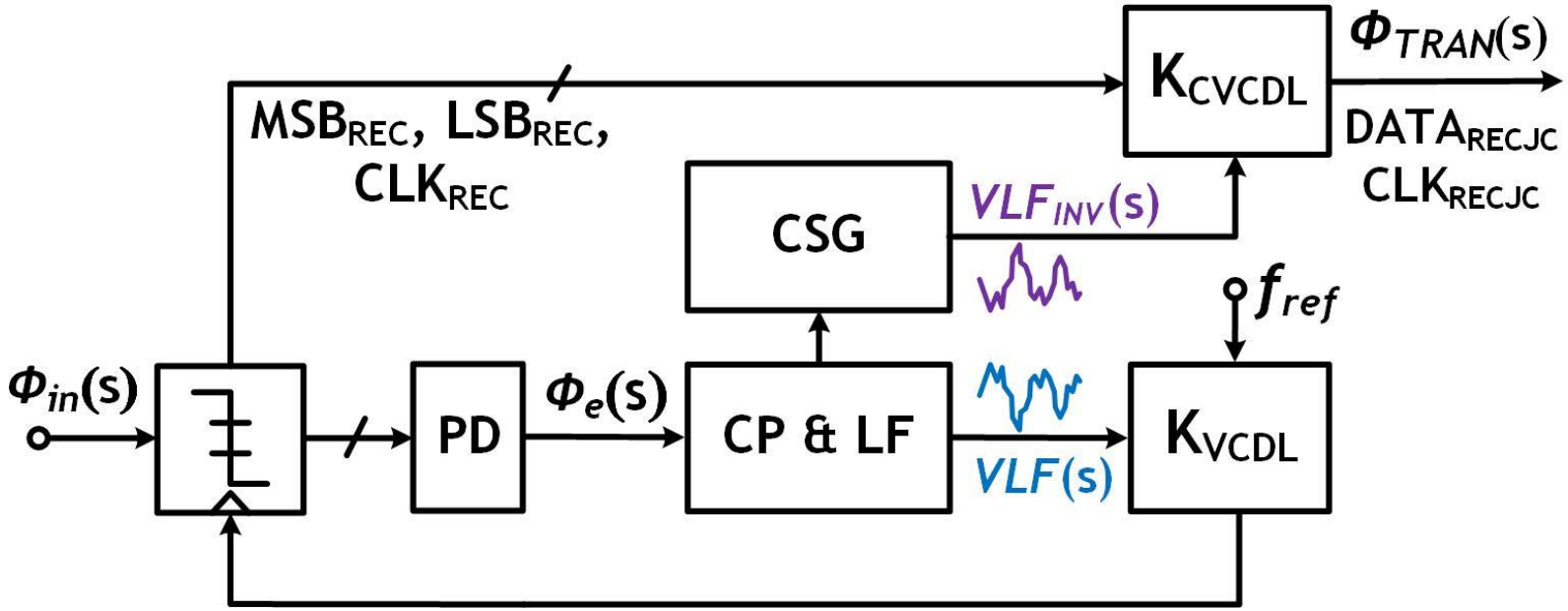
Conclusions



- Jitter compensation CDR overcomes the trade-off between JTRAN and JTOL BW
- The architecture is compatible with quarter-rate architecture up to 60-Gb/s
- JTOL BW of 40 MHz, JTRAN < -8-dB are achieved with the jitter compensation function

Reference

- H. Li, S. Chen, L. Yang, R. Bai, W. Hu, F.Y. Zhong, S. Palermo and P.Y. Chiang, "A 0.8 V, 560fJ/bit, 14Gb/s injection-locked receiver with input duty-cycle distortion tolerable edge-rotating 5/4X sub-rate CDR in 65nm CMOS," in *2014 Symposium on VLSI Circuits Digest of Technical Papers*, 2014, pp. 1-2.
- X. Zheng, C. Zhang, F. Lv, F. Zhao, S. Yuan, S. Yue, Z. Wang, F. Li, Z. Wang and H. Jiang, "A 40-gb/s quarter-rate SerDes transmitter and receiver chipset in 65-nm CMOS," *IEEE J. Solid State Circuits*, vol. 52, no. 11, pp. 2963-2978 2017.
- Y. Lee, W. Ho and W. Chen, "A 25-gb/s, 2.1-pJ/bit, fully integrated optical receiver with a baud-rate clock and data recovery," *IEEE J. Solid State Circuits*, vol. 54, no. 8, pp. 2243-2254 2019.
- Y. Fan, A. Kumar, T. Iwai, A. Roshan-Zamir, S. Cai, B. Sun and S. Palermo, "A 32-gb/s simultaneous bidirectional source-synchronous transceiver with adaptive echo cancellation techniques," *IEEE J. Solid State Circuits*, vol. 55, no. 2, pp. 439-451 2019.

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HKUST OWL

Key Circuits: A Bang-Bang Phase Detector for PAM-N Signaling

Outline

- Motivation
- Design Challenges and Requirements
- Proposed Architecture
- Simulation Results
- Comparing the Proposed and Conventional Solutions
- Conclusion

Outline

- **Motivation**
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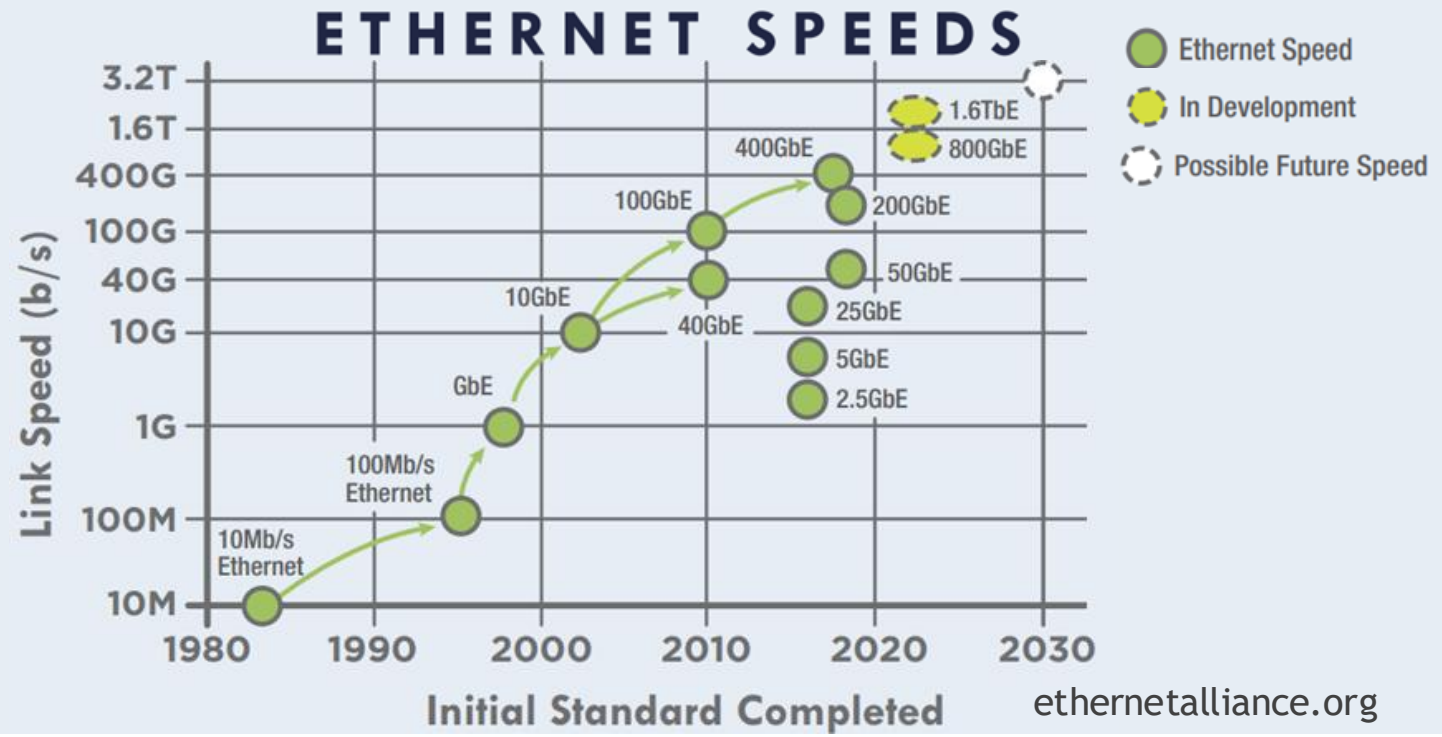
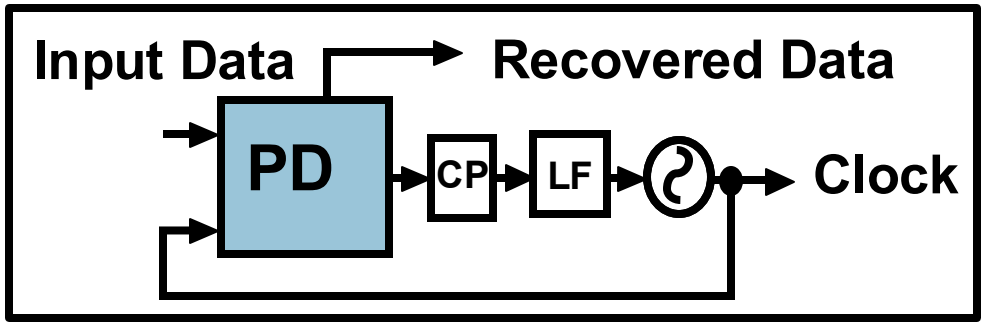
Motivation



Clock and data recovery (CDR)



Phase Detector (PD)

- Phase error
- Control signals
- Recover data
- CDR's impact on the link energy efficiency

- Growing internet traffic **necessitates** high-speed data links
- NRZ is replaced by **PAM-4** and **PAM-8** for bandwidth efficiency
- CDR ensures **error-free** data recovery

Phase detector (PD) design becomes challenging for higher orders of PAM

Outline

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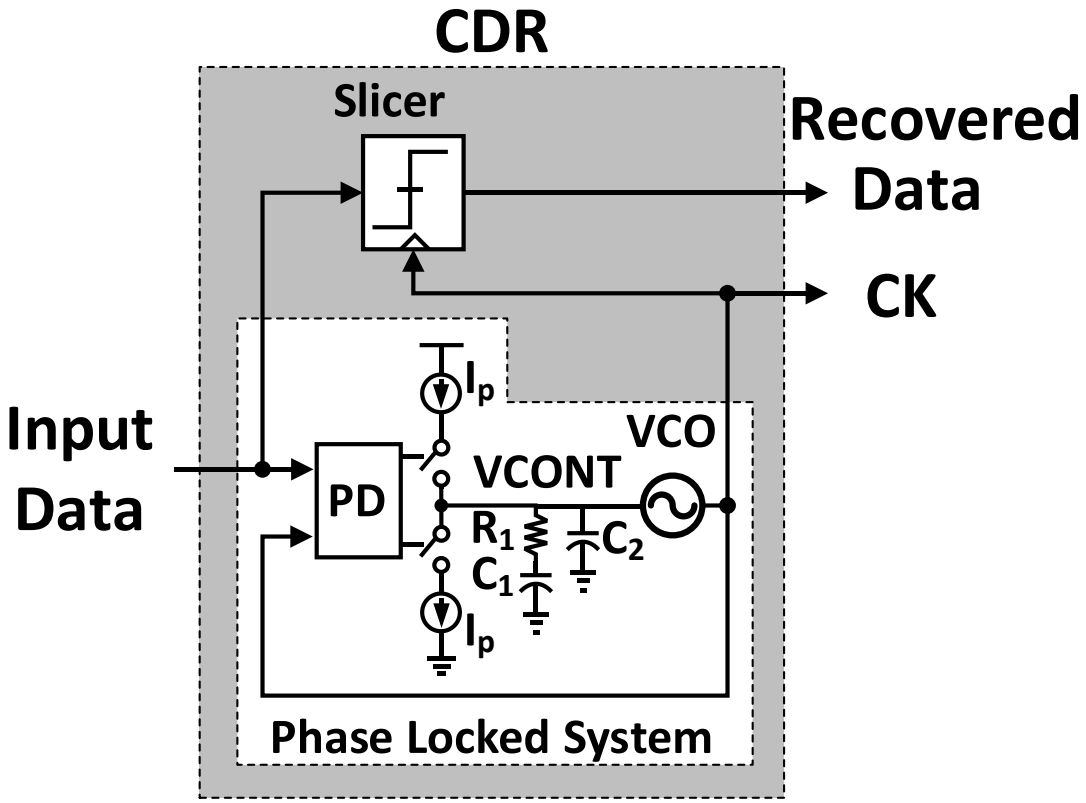
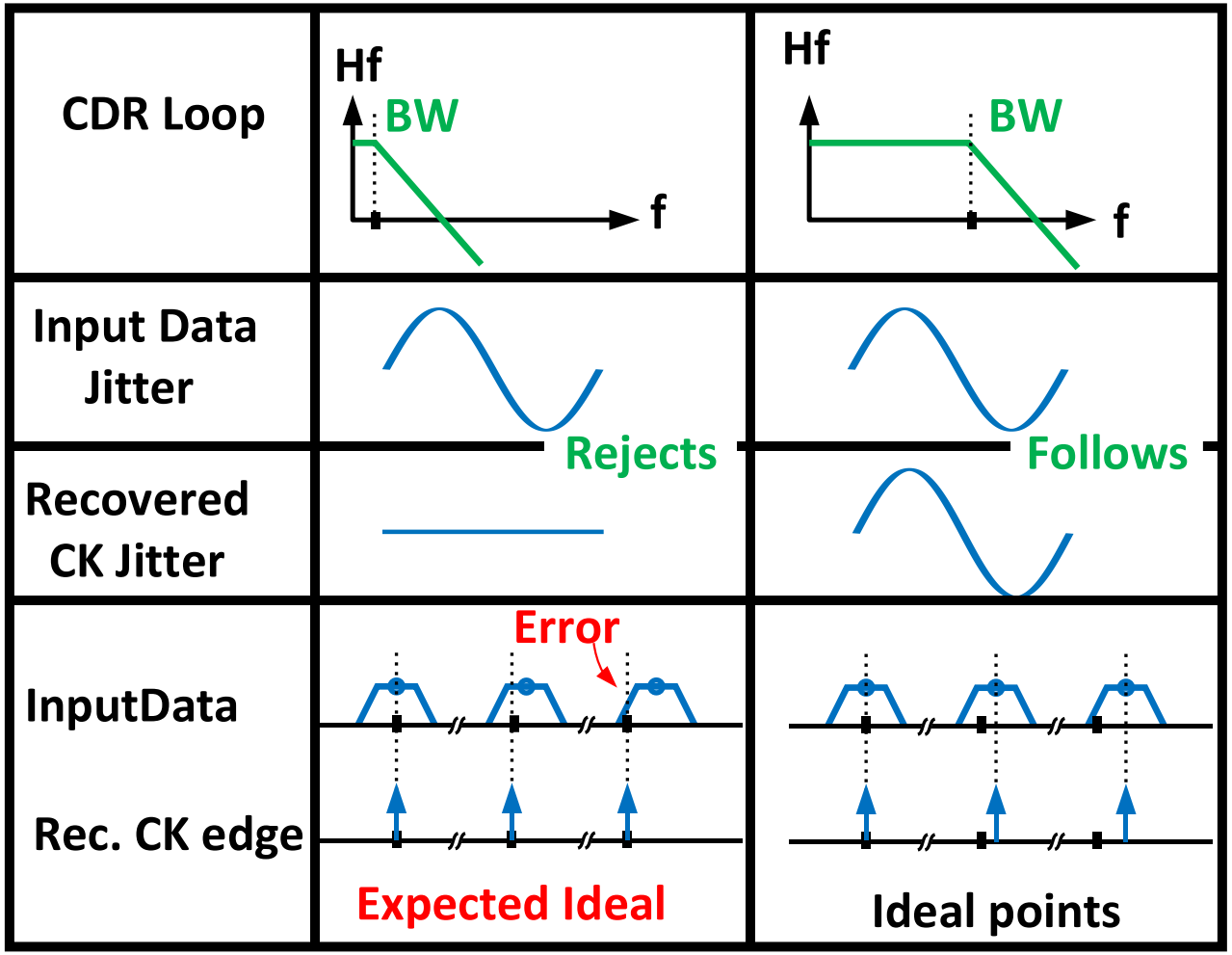
CDR Performance in the Presence of Jittery Data

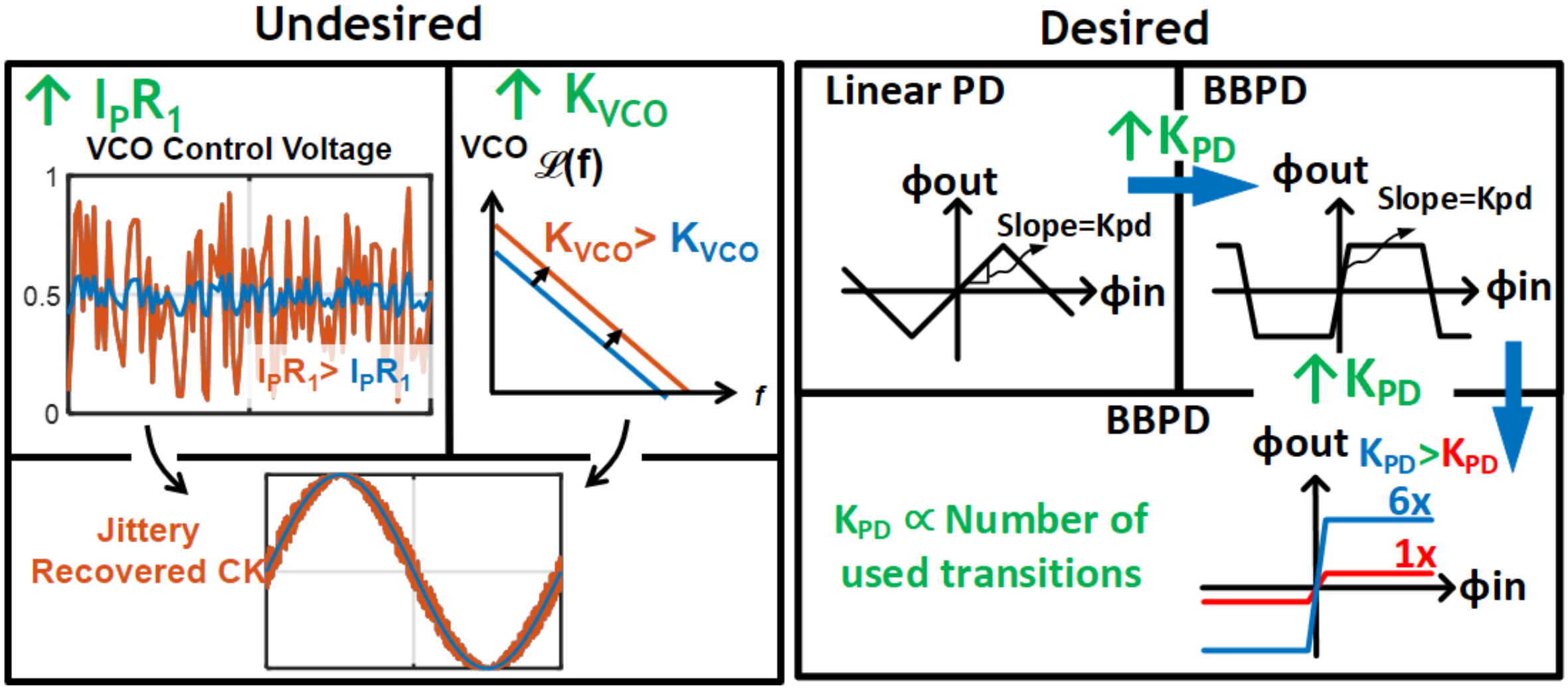


$$BW \approx K_{pd} I_p R_1 K_{VCO}$$



- To ensure accurate recovery of jittery data, the CDR's loop bandwidth (BW) must be increased.

Options to Increase CDR's Loop Bandwidth

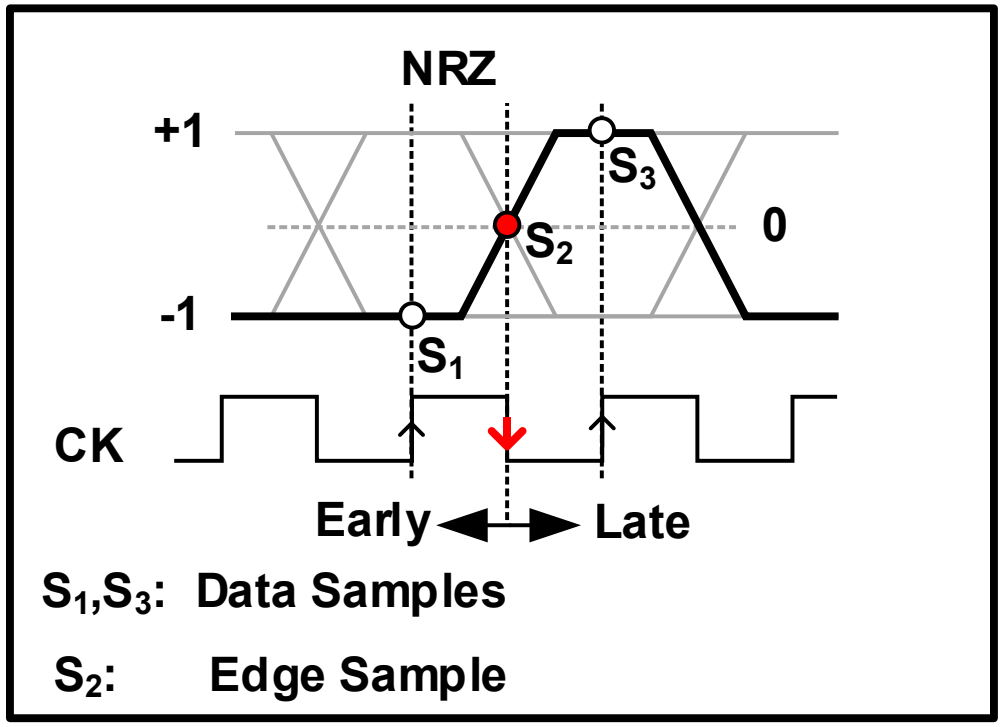


- $BW \approx K_{PD} I_P R_1 K_{VCO}$

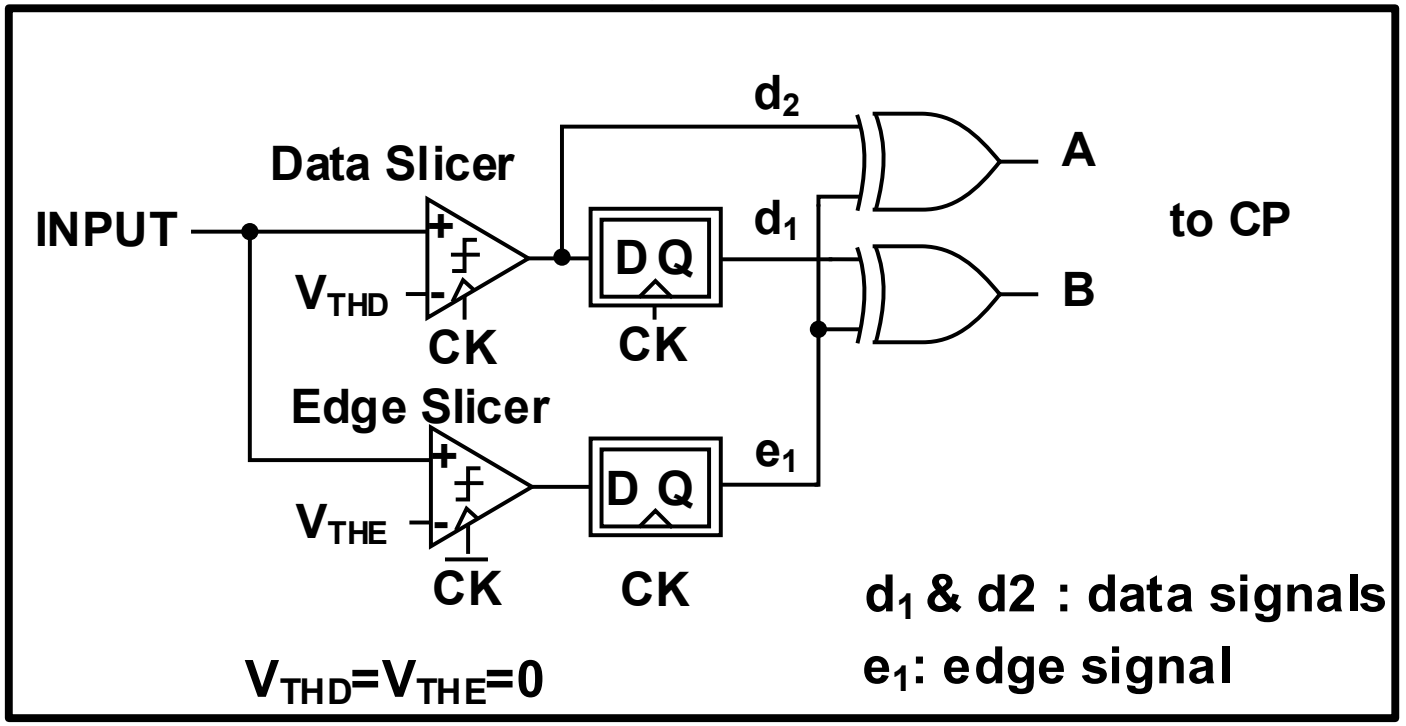
Use all PAM transitions and a BBPD

Bang-Bang Phase Detector (NRZ BBPD)

waveform



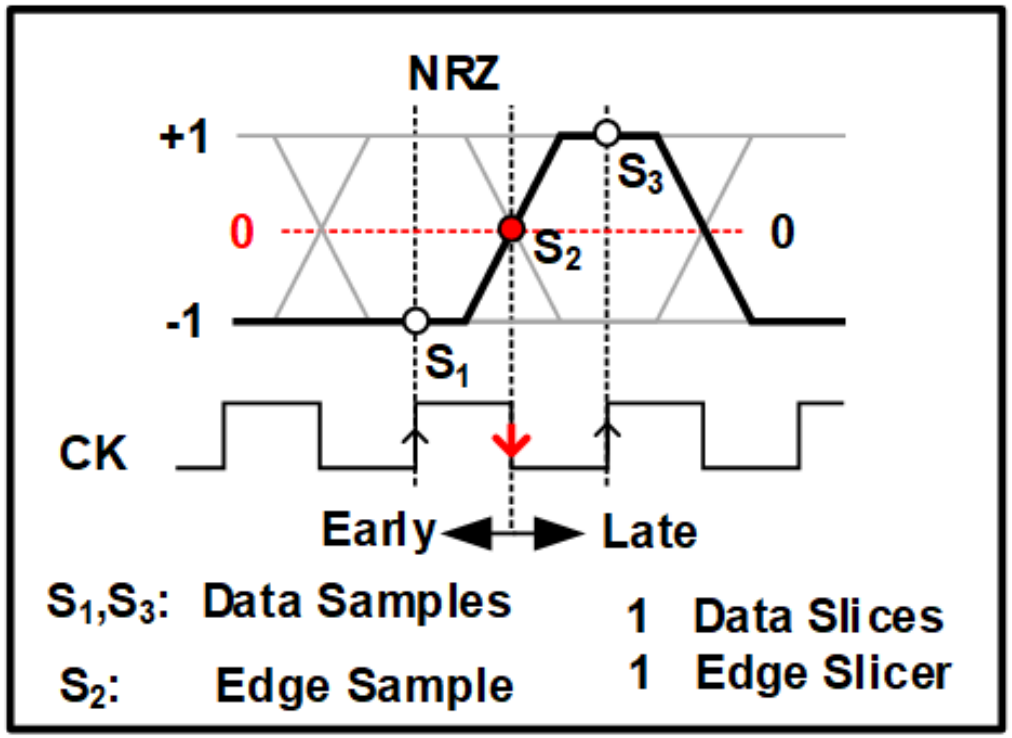
Diagram

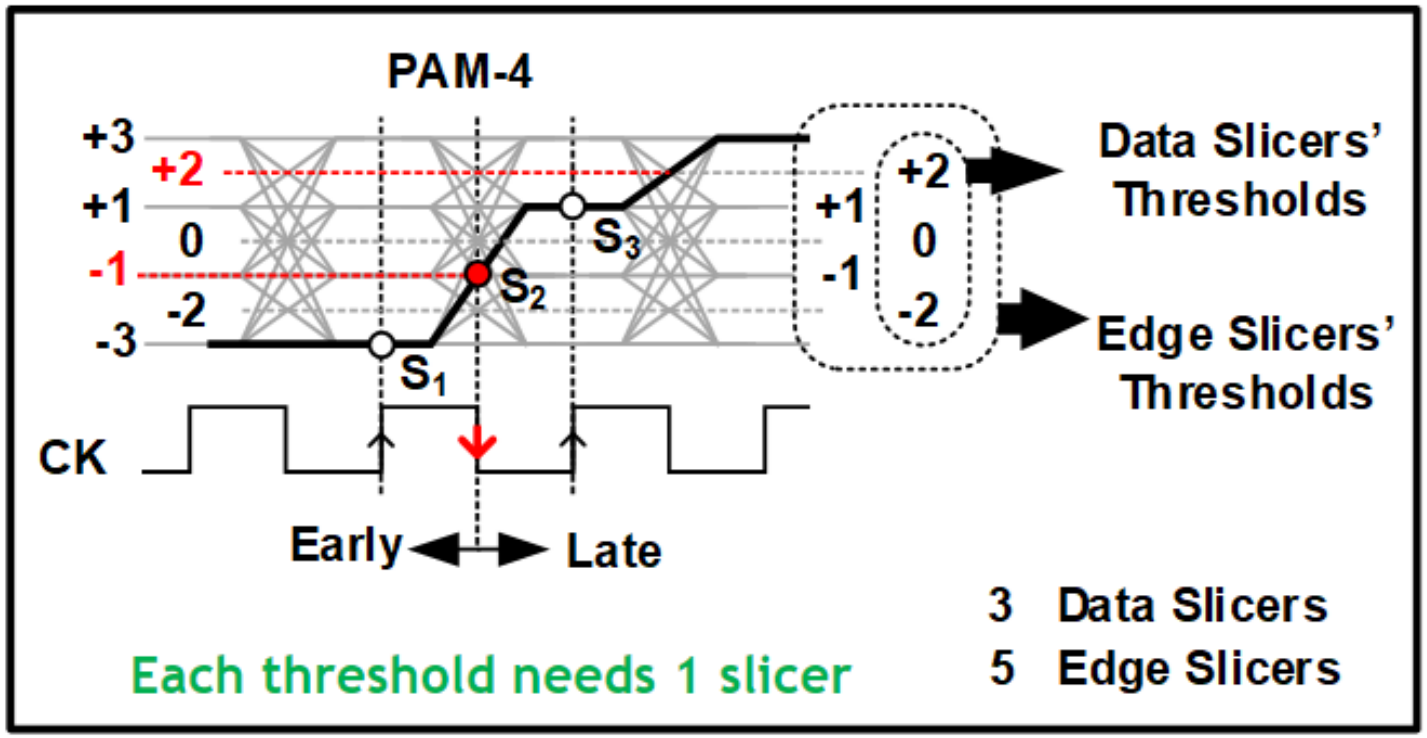


- Quantize & compare 3 samples (Needs 1 Data Slicer & 1 Edge Slicer)
- Alignment= CK↓ edge is in the middle of data transition

Bang-Bang Phase Detector (PAM-N)

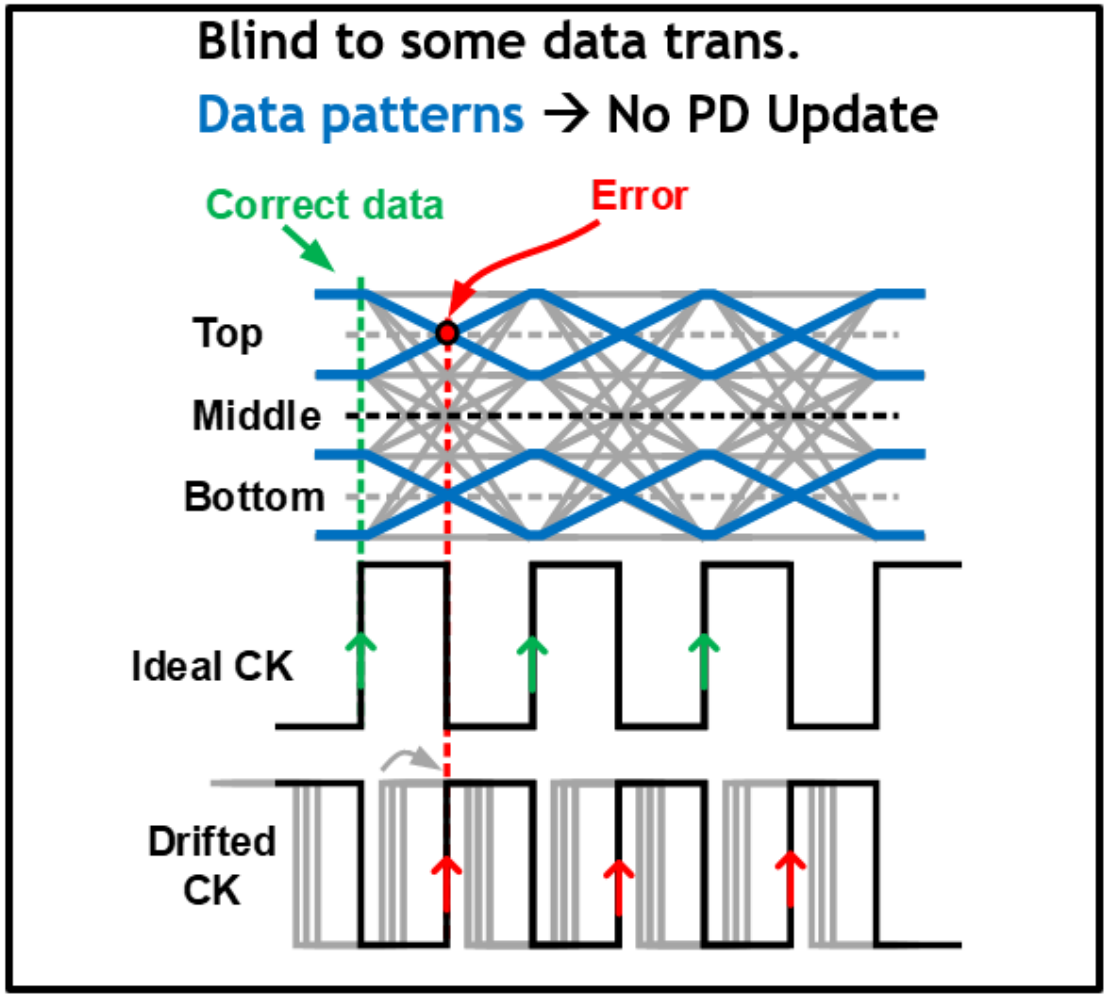
- Quantize & compare 3 samples
- Alignment= CK↓ edge is in the middle of data transition

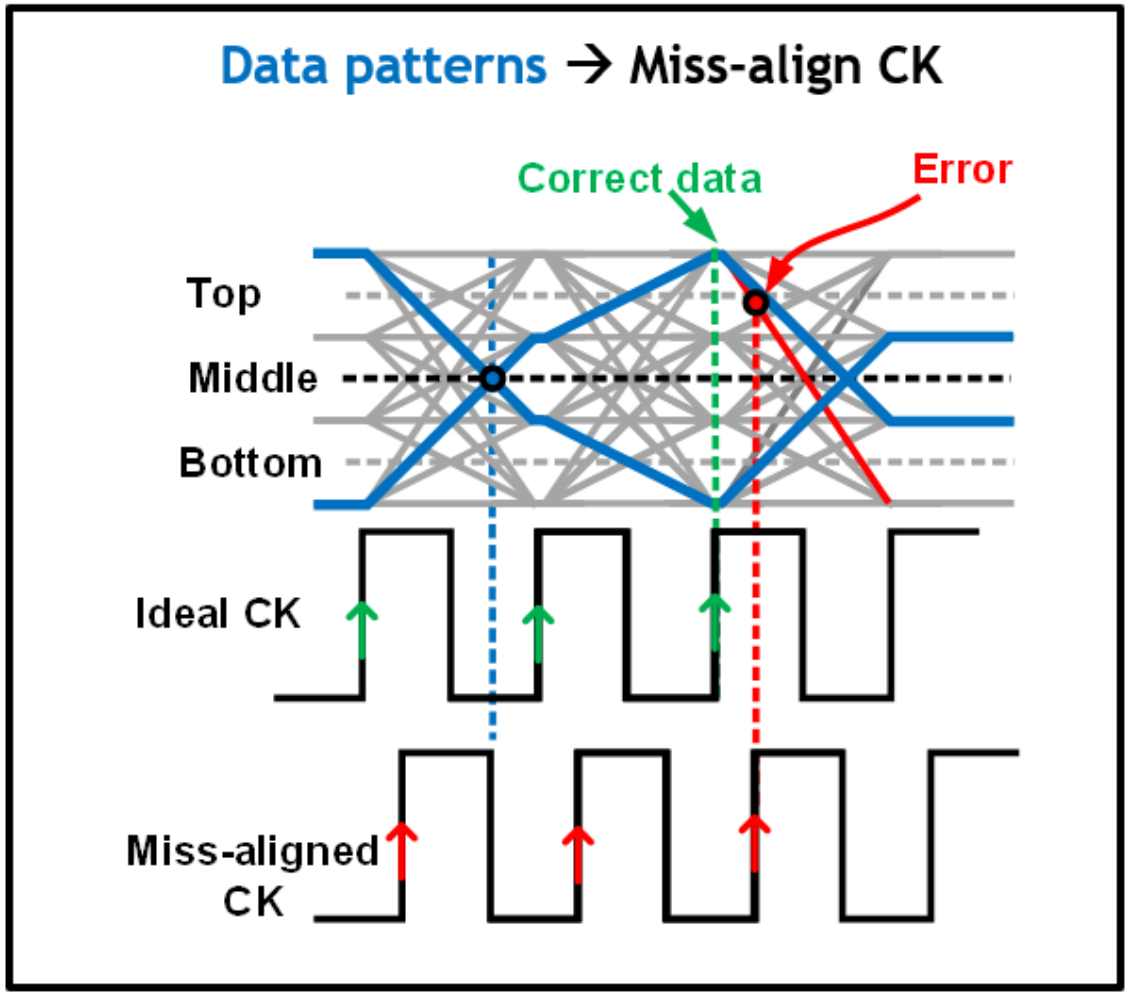




- PAM-N BBPD requires 2N-3 Slicers to extract the whole Edge Information

Why not to use NRZ PD for PAM-4?





- Solution= Choose the threshold level according to the transition

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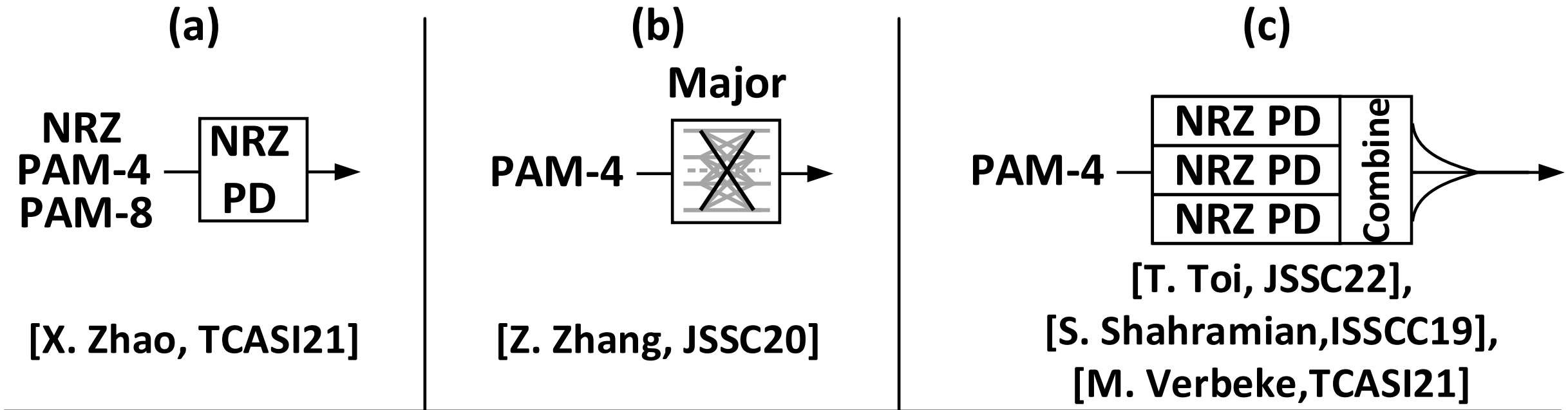
- Conclusion

Prior Work on PD

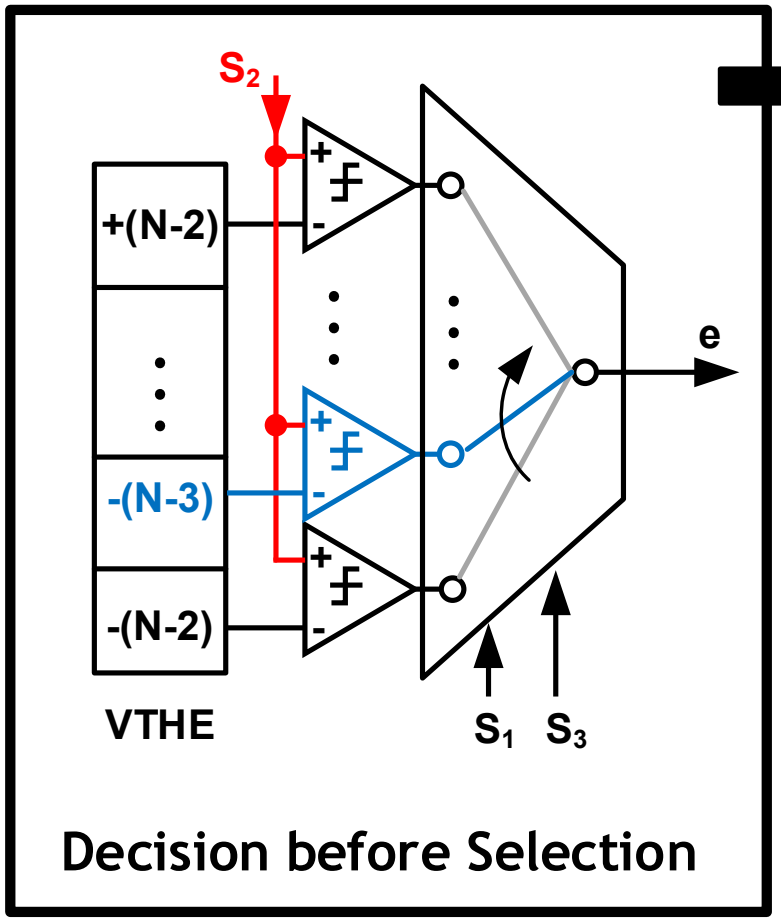


- Although (a) is a simple solution that supports multimode operation, it has a poor bit error rate for high orders of PRBS PAM-4/8 data.

Proposed Phase Detection Approach

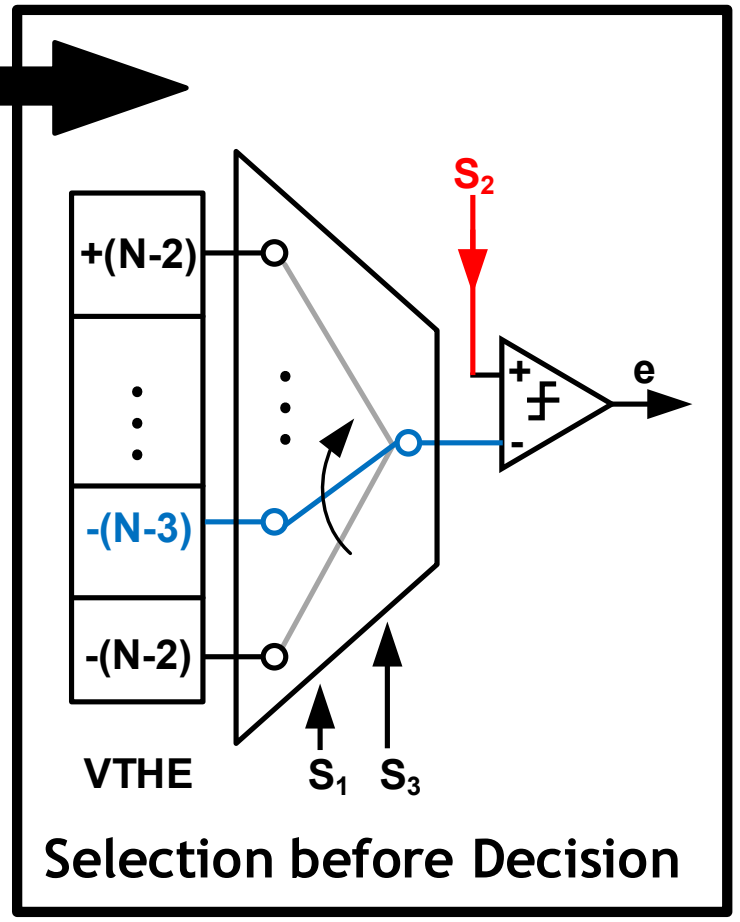
Edge Information Extraction

Using 2N-3 Slicers (13 for PAM-8)



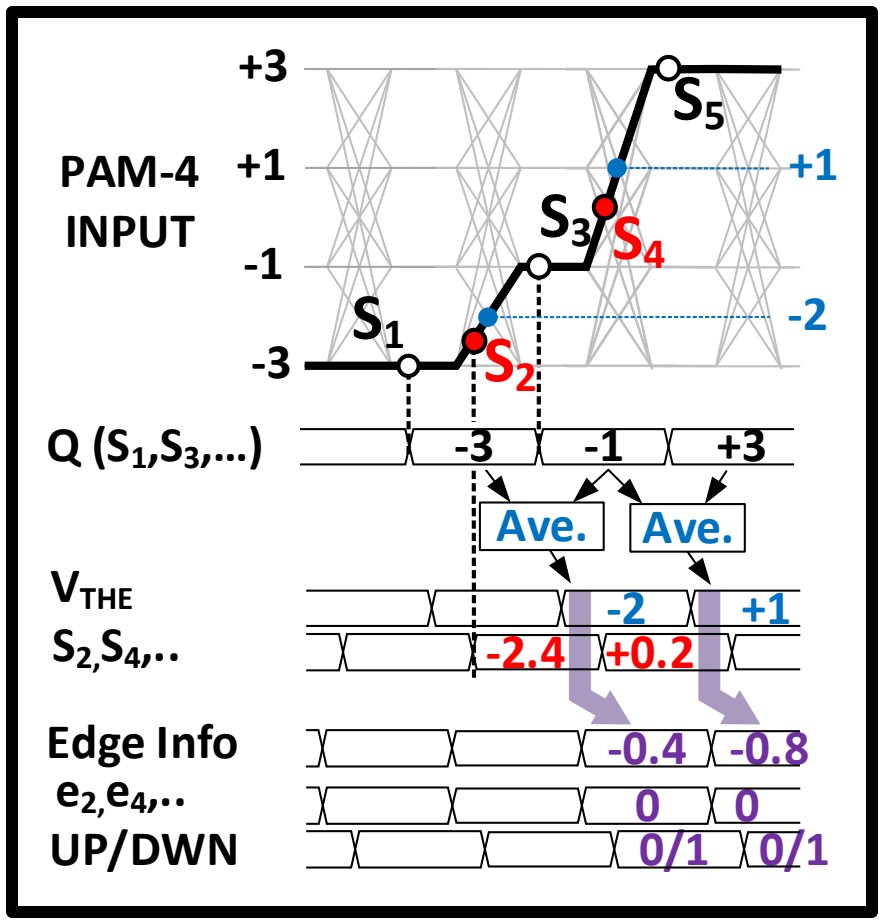
Decision before Selection

Proposed Solution (1 Slicer)

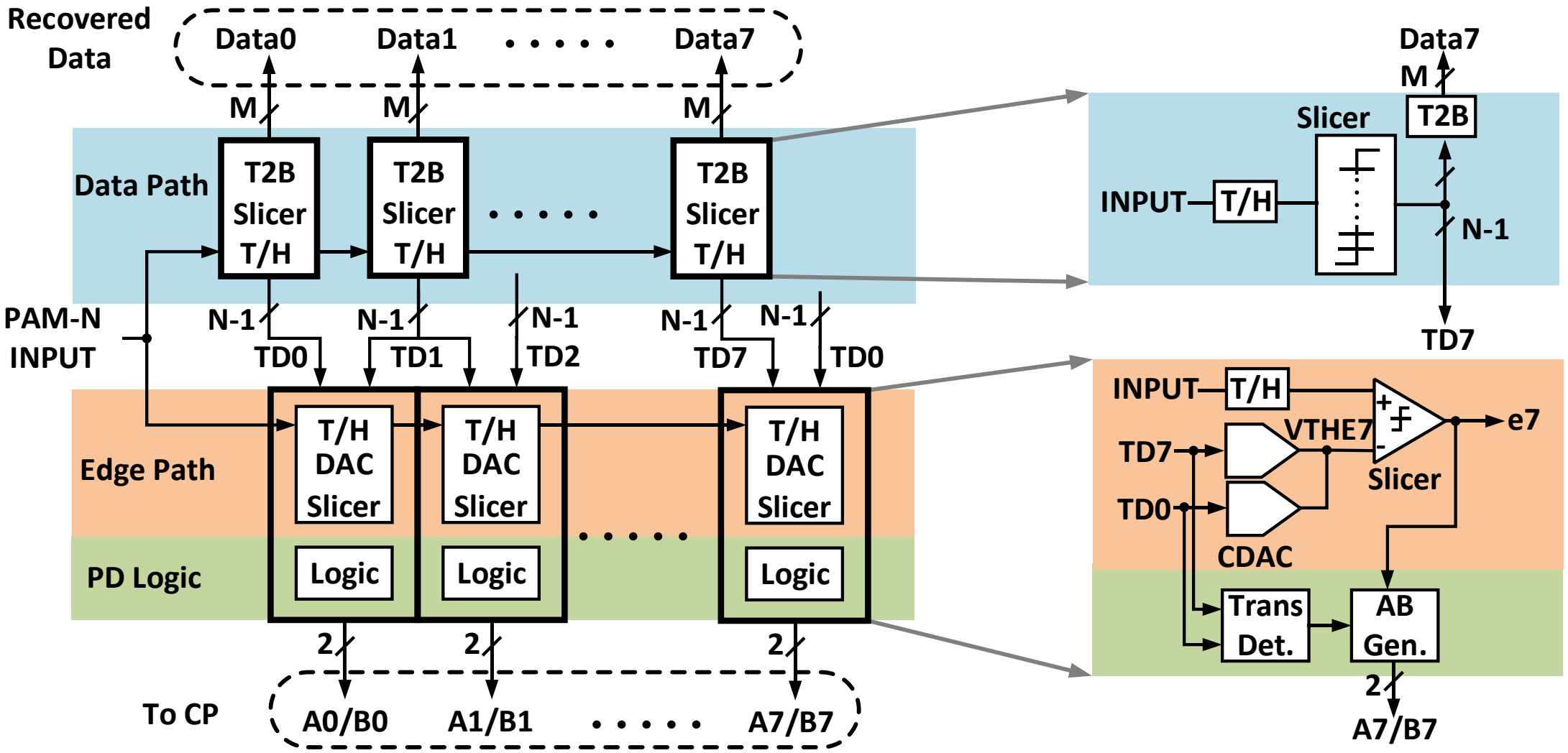


Selection before Decision

Conceptual Example (Early CK)

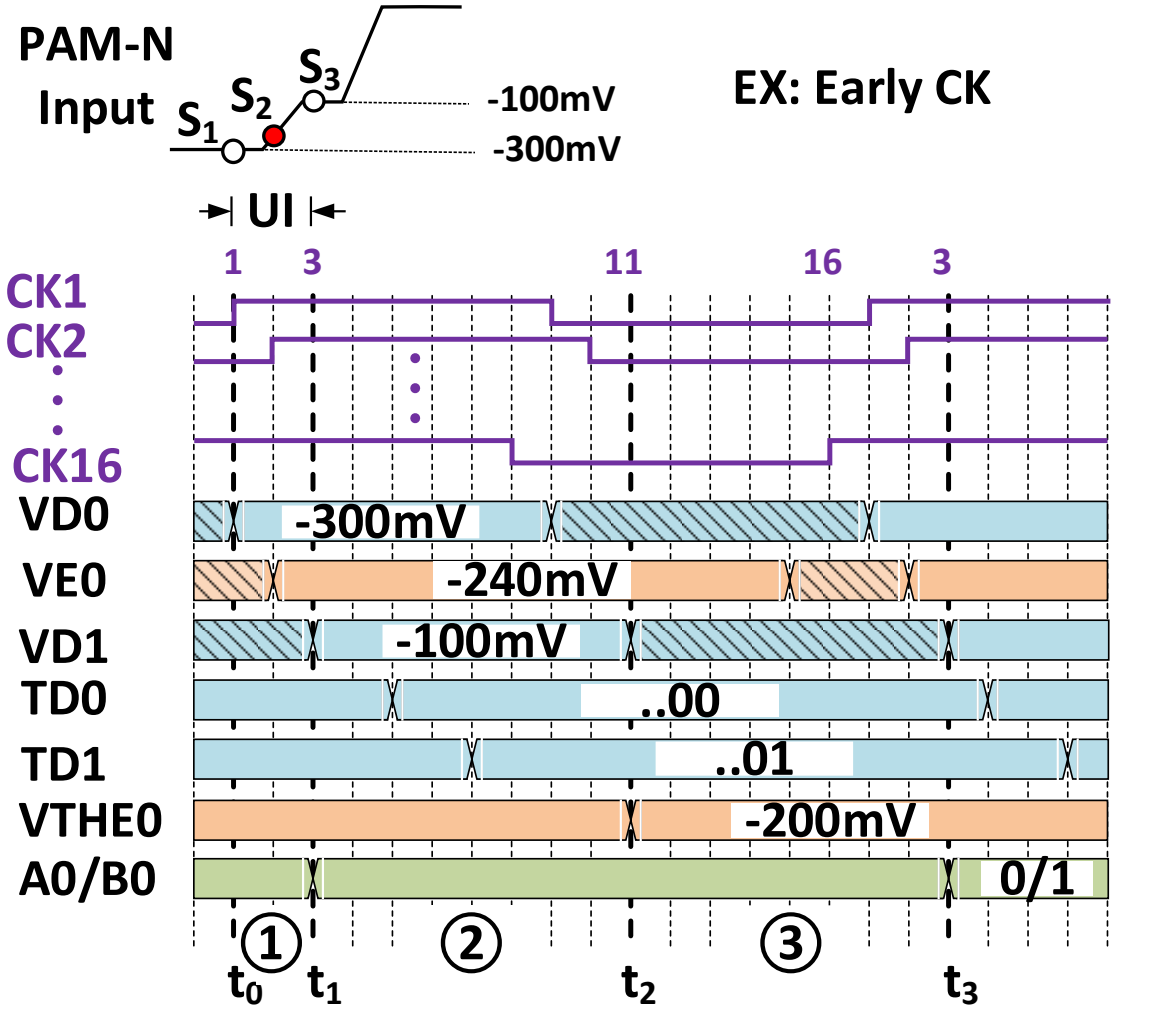


Proposed PAM-N BBPD Architecture

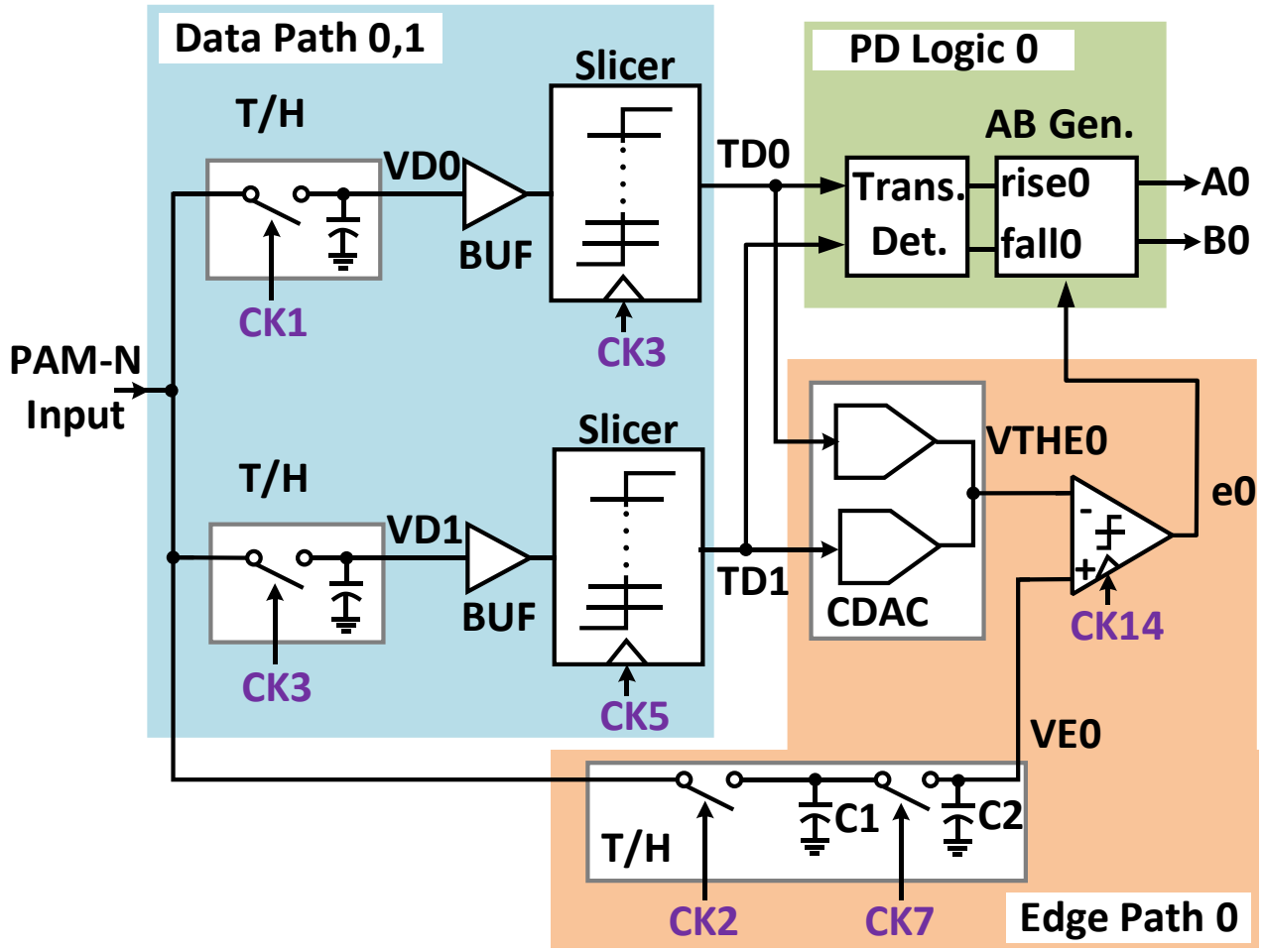


- high-speed → 1/8 rate

Timing Diagram of Operation



EX: Early CK



①: Sample V_{D0},V_{D1},&V_{E0} ②: Update TD0,TD1,&VTHE0

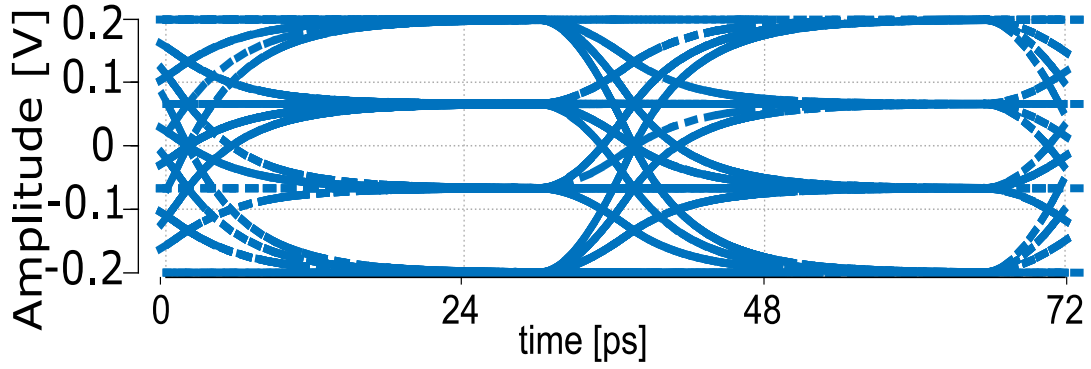
③: Update A0 & B0

Outline

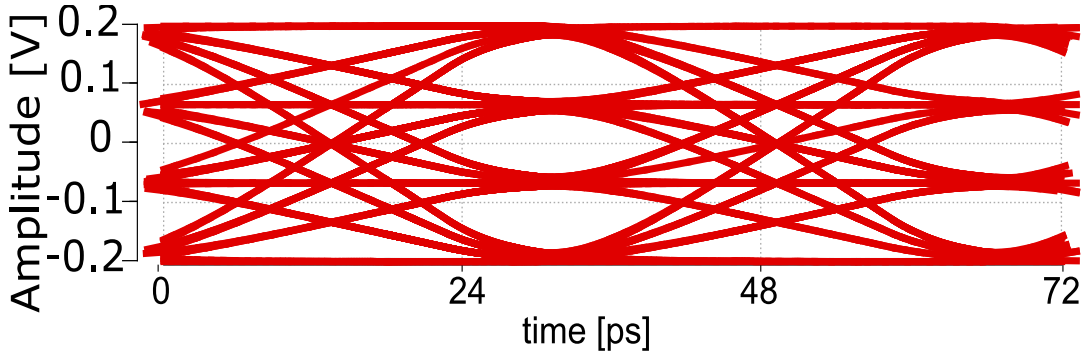
- Motivation
- Design Challenges and Requirements
- Proposed Architecture
- **Simulation Results**
- Comparing the Proposed and Conventional Solutions
- Conclusion

Simulation Results

56Gb/s PAM-4 eye diagrams

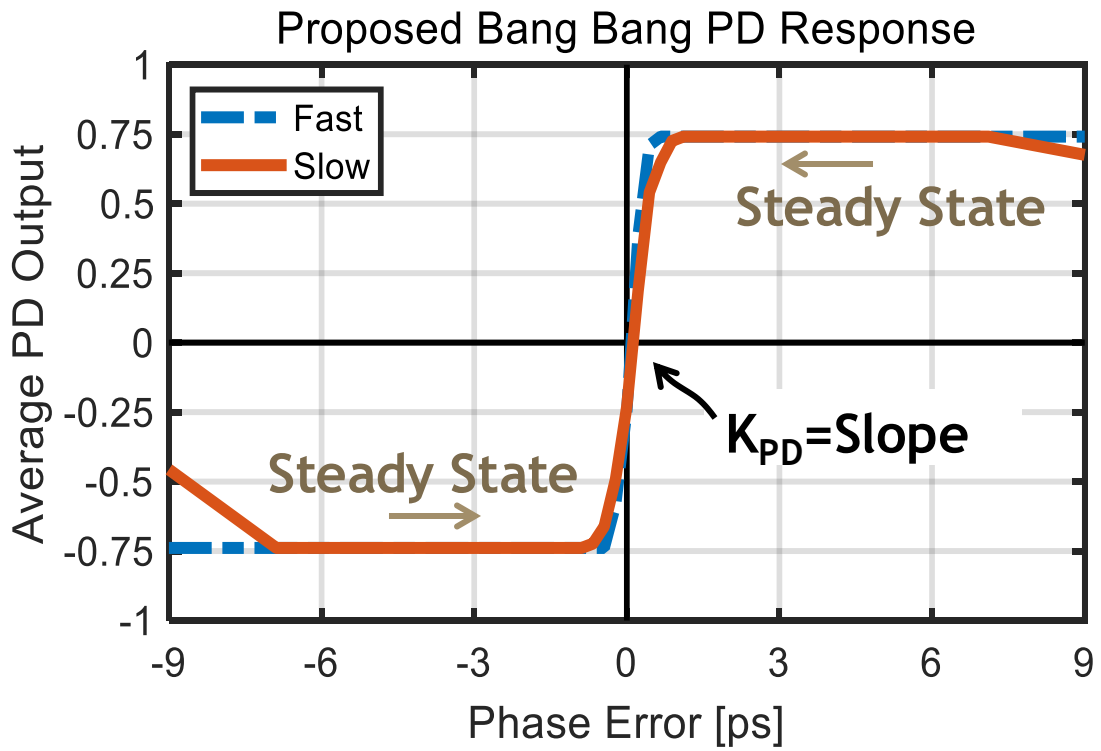


(a) fast rise/fall time (0.2UI)



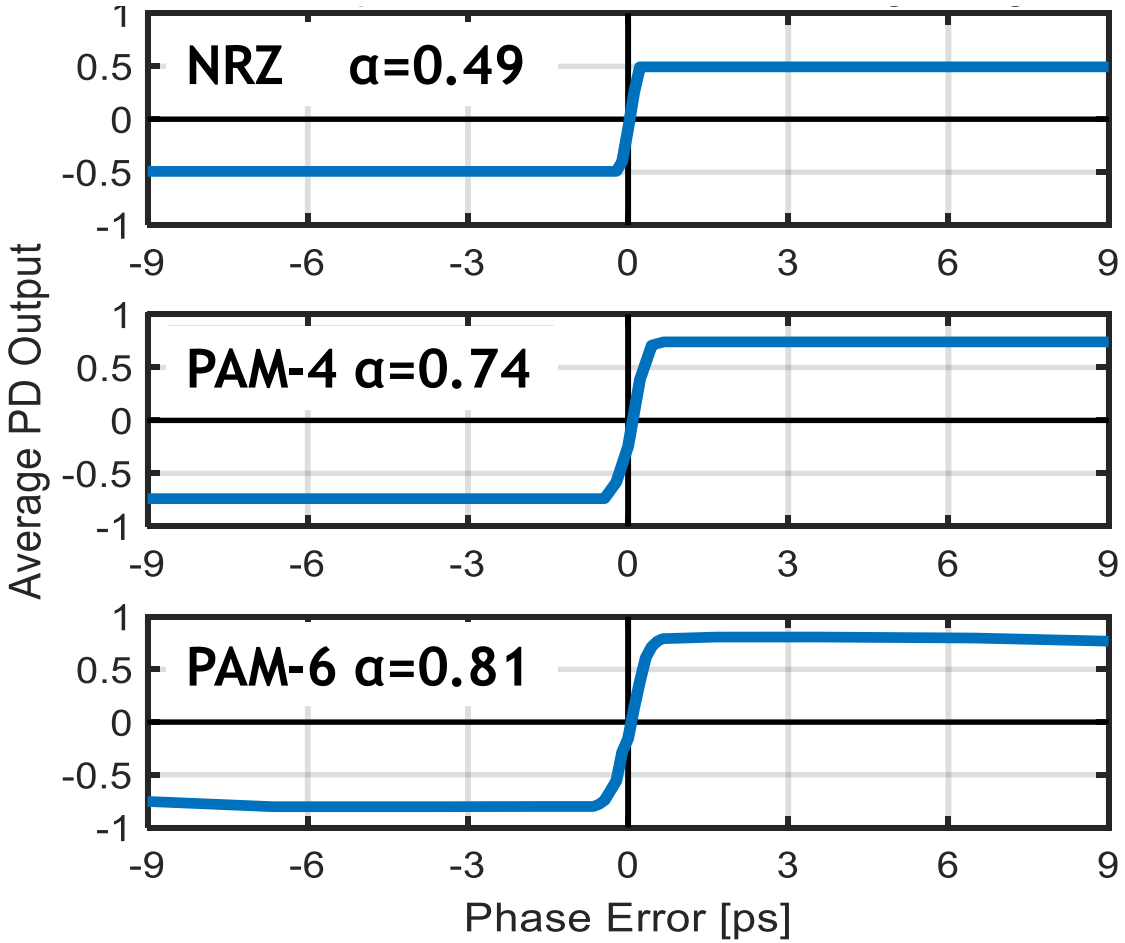
(b) slow rise/fall time (0.4UI)

Simulation results in 28nm CMOS

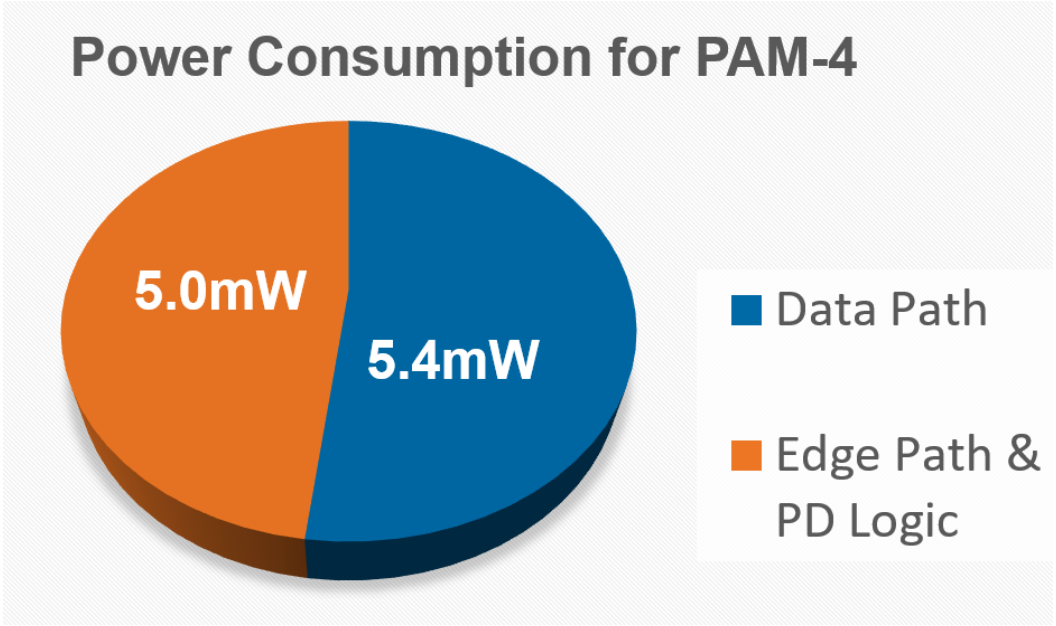


Simulation Results (Con.)

PD response for different PAM Signaling



α= transition density
Simulations are for 28nm CMOS



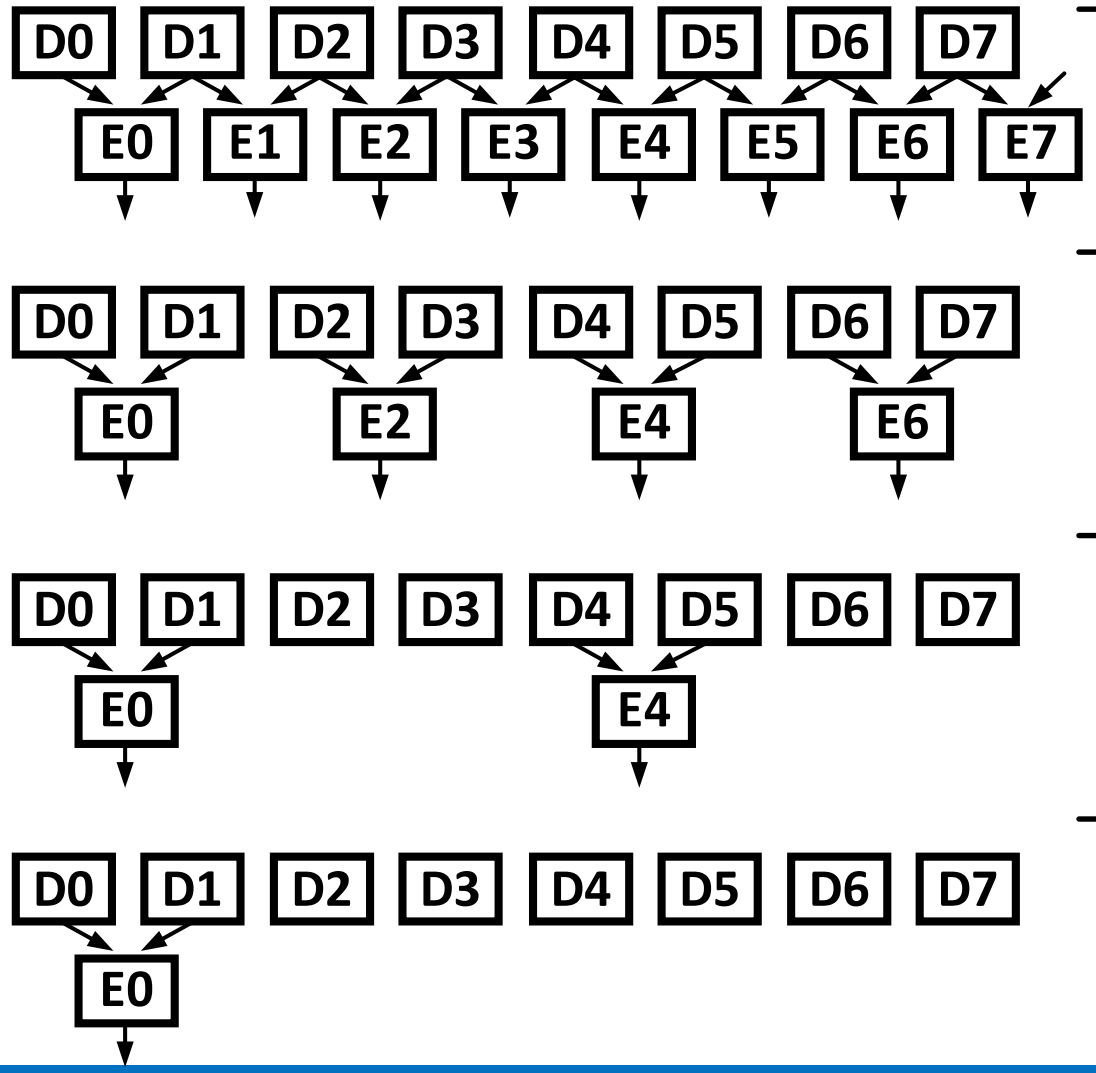
Data rate = 56Gb/s
Power consumption=10.4mW
52% data path, 48% edge path& PD logic
Energy efficiency= 0.18pJ/bit

We can further reduce the power consumption (next)

Outline

- Motivation
- Design Challenges and Requirements
- Proposed Architecture
- Simulation Results
- **Comparing the Proposed and Conventional Solutions**
- Conclusion

Reducing Power Consumption



	Edge Power	Trans. Density (α)
(a): Every Edge	1X	$\frac{(N-1)}{N}$
(b): Every 2 Edges	$\frac{1}{2}$X	$\frac{(N-1)}{2N}$
(c): Every 4 Edges	$\frac{1}{4}$X	$\frac{(N-1)}{4N}$
(d): Every 8 Edges	$\frac{1}{8}$X	$\frac{(N-1)}{8N}$

Proposed V.S. using Major Transitions

Modulation ↓	Proposed PD (Every K edges)								Major
	K=1	K=2	K=4	K=8	K=16	K=32	K=64	K=128	
PAM-4	$\frac{12}{16}$	$\frac{6}{16}$	$\frac{3}{16}$	$\frac{1.5}{16}$	$\frac{0.75}{16}$	$\frac{0.38}{16}$	$\frac{0.19}{16}$	$\frac{0.09}{16}$	$\frac{2}{16}$
PAM-6	$\frac{30}{36}$	$\frac{15}{36}$	$\frac{7.5}{36}$	$\frac{3.75}{36}$	$\frac{1.88}{36}$	$\frac{0.94}{36}$	$\frac{0.47}{36}$	$\frac{0.23}{36}$	$\frac{2}{36}$
PAM-8	$\frac{56}{64}$	$\frac{28}{64}$	$\frac{14}{64}$	$\frac{7}{64}$	$\frac{3.5}{64}$	$\frac{1.75}{64}$	$\frac{0.88}{64}$	$\frac{0.44}{64}$	$\frac{2}{64}$
PAM-16	$\frac{240}{256}$	$\frac{120}{256}$	$\frac{60}{256}$	$\frac{30}{256}$	$\frac{15}{256}$	$\frac{7.5}{256}$	$\frac{3.75}{256}$	$\frac{1.88}{256}$	$\frac{2}{256}$

- For PAM-N and K=8, $\alpha \cong 0.1$, close to using major trans. for PAM-4 (Edge path power is reduced by 8)

$\alpha = \frac{N-1}{KN}$ for proposed PD

Outline

- Motivation
- Design Challenges and Requirements
- Proposed Architecture
- Simulation Results
- Comparing the Proposed and Conventional Solutions
- **Conclusion**

Conclusion

- The proposed architecture for PAM-N PD aims at high jitter tolerant CDRs.
- It utilizes all PAM-N transitions and requires only one slicer to extract edge information.
- The design is not sensitive to clock misalignment by data and does not require complicated transition selection logic.
- The architecture is energy efficient and scalable with technology.
- We anticipate higher speed and improved energy efficiency in more advanced nodes.
- A fast sampler leads to higher speed.
- A low latency slicer enables quarter rate or faster eighth rate.

Reference

- Z. Zhang, G. Zhu, C. Wang, L. Wang and C. P. Yue, "A 32-Gb/s 0.46-pJ/bit PAM4 CDR Using a Quarter-Rate Linear Phase Detector and a Self-Biased PLL-Based Multiphase Clock Generator," *IEEE J. Solid-State Circuits*, vol. 55, no. 10, pp. 2734-2746, Oct. 2020.
- X. Zhao, Y. Chen, P. -I. Mak and R. P. Martins, "A 0.14-to-0.29-pJ/bit 14-GBaud/s Trimodal (NRZ/PAM-4/PAM-8) Half-Rate Bang-Bang Clock and Data Recovery (BBCDR) Circuit in 28-nm CMOS," *IEEE Trans. Circuits Syst. I*, vol. 68, no. 1, pp. 89-102, Jan. 2021
- M. Verbeke, G. Torfs and P. Rombouts, "The Truth About 2-Level Transition Elimination in Bang-Bang PAM-4 CDRs," *IEEE Trans. Circuits Syst. I*, vol. 68, no. 1, pp. 469-482, Jan. 2021.
- T. Toi et al., "A 25.6-Gb/s Interface Employing PAM-4-Based Four-Channel Multiplexing and Cascaded Clock and Data Recovery Circuits in Ring Topology for High-Bandwidth and Large-Capacity Storage Systems," *IEEE J. Solid-State Circuits*, vol. 57, no. 5, pp. 1517-1526, May 2022.
- S. Shahramian et al., "30.5 A 1.41pJ/b 56Gb/s PAM-4 Wireline Receiver Employing Enhanced Pattern Utilization CDR and Genetic Adaptation Algorithms in 7nm CMOS," *ISSCC*, San Francisco, CA, USA, 2019, pp. 482-484.

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HKUST OWL

Key Circuits:
L-C Voltage-Controlled Oscillator

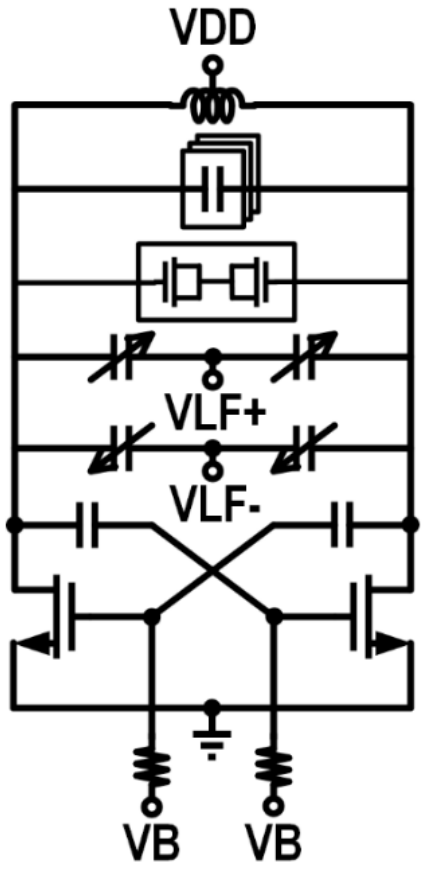
LC VCO Implementation Example

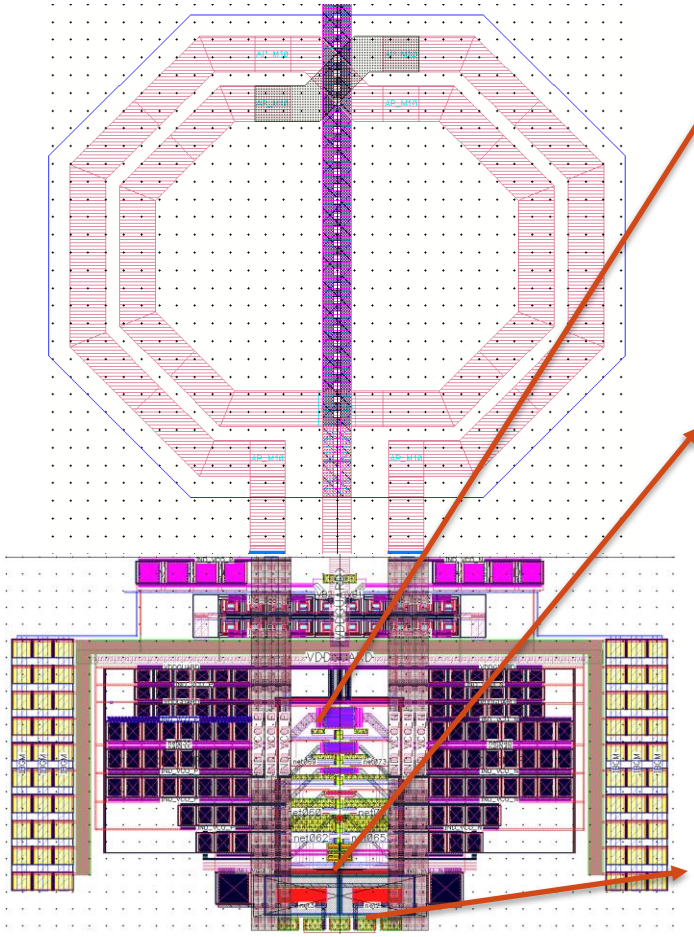
$$L(\Delta\omega)=10\log\left\{\frac{2FkT}{P_{sig}}\left[1+\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right]\left(1+\frac{\omega_1}{|\Delta\omega|}\right)\right\}$$

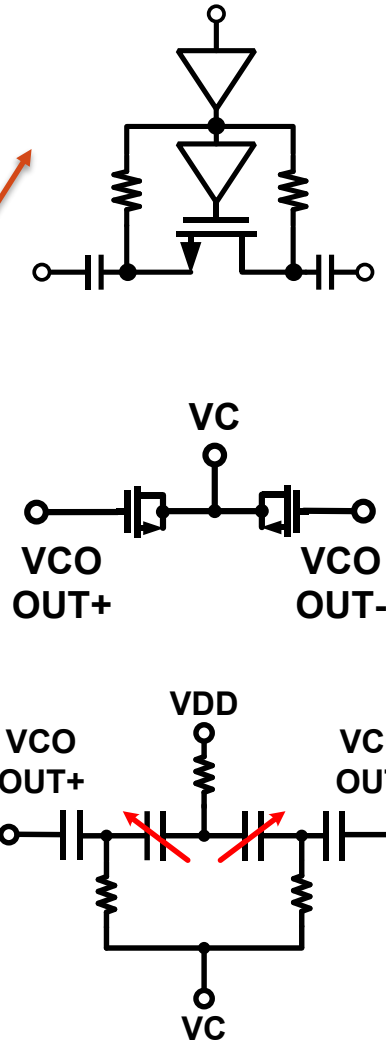
- Leeson's equation for phase noise
  - P_{sig}: oscillating signal power in the LC tank
  - ω_0: oscillating frequency
  - Q: LC tank quality factor
  - ω_1: flicker noise corner frequency (corner frequency between 30dB/dec and 20dB/dec slope region)
- Indications:
  - Higher LC-tank quality (Q_l)
  - Smaller inductance for higher signal power in LC-tank (for higher P_{sig})

LC VCO Typical Layout

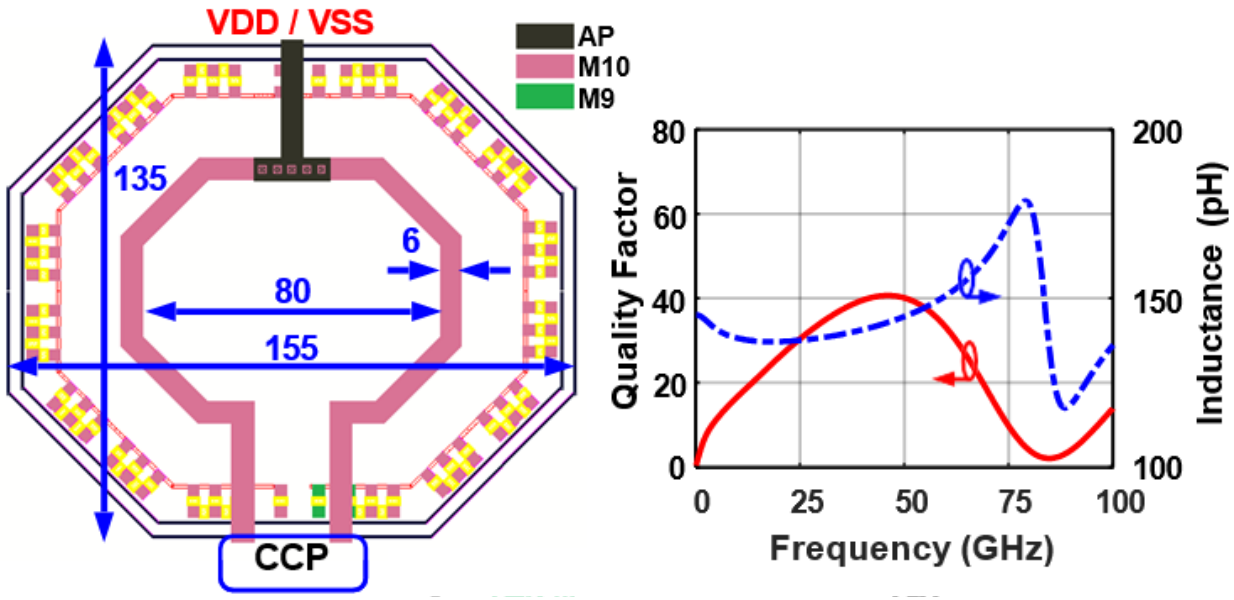
- Design Targets:
  - High-Q inductor
    - With proper power routing
  - High-Q capacitor bank
  - Properly-bias varactor for:
    - Integral path
    - Proportional path

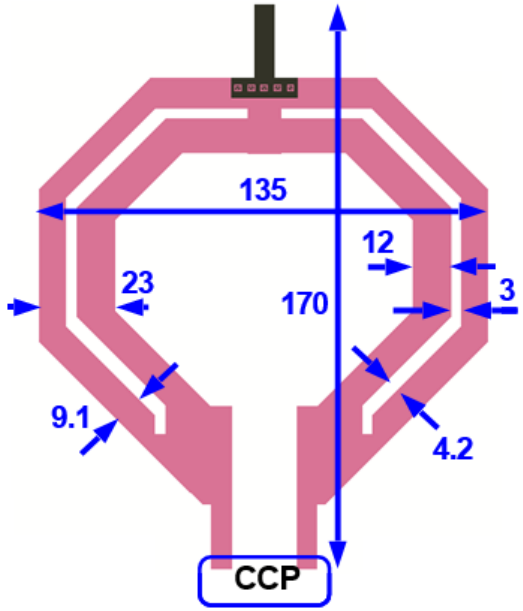




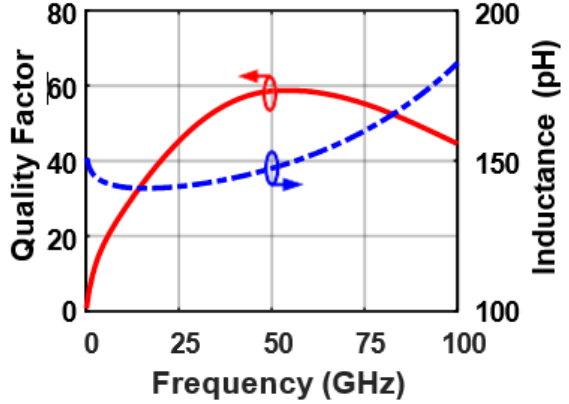


Inductor Design and Simulation





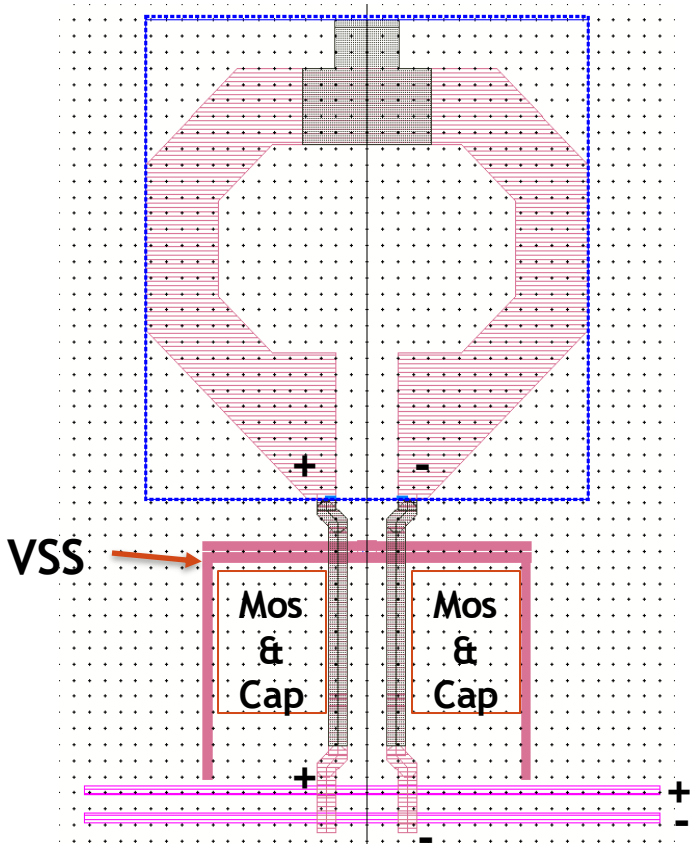
Technique 1: guard-ring removal & slotted wide-track layout

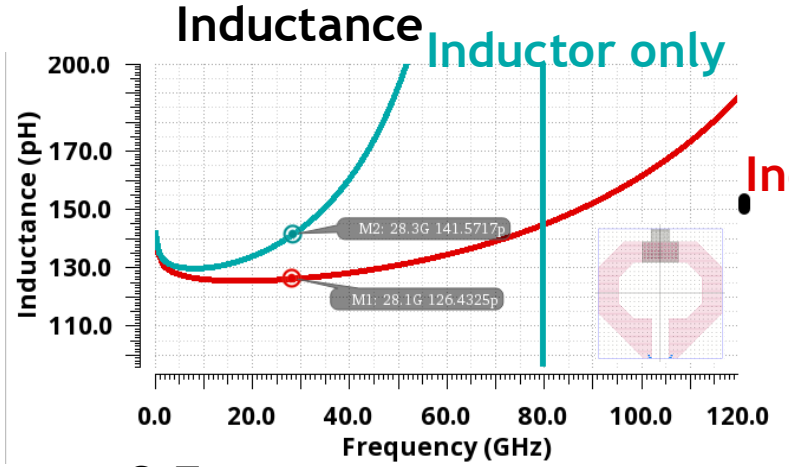


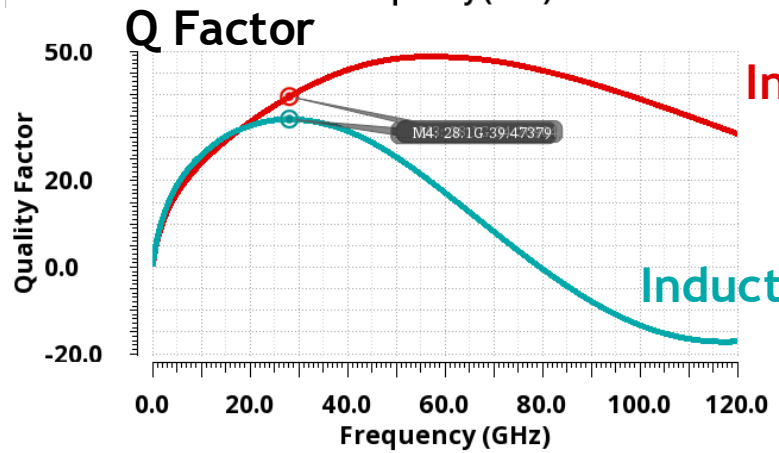
- Directly using PDK inductor
  - L = 138 pH, Q = 32.7
- Simplified inductor
  - L = 153 pH, Q = 46.8

Inductor and Interconnections

- The interconnection path between the inductor and the active device/capacitor bank leads to reduced phase noise

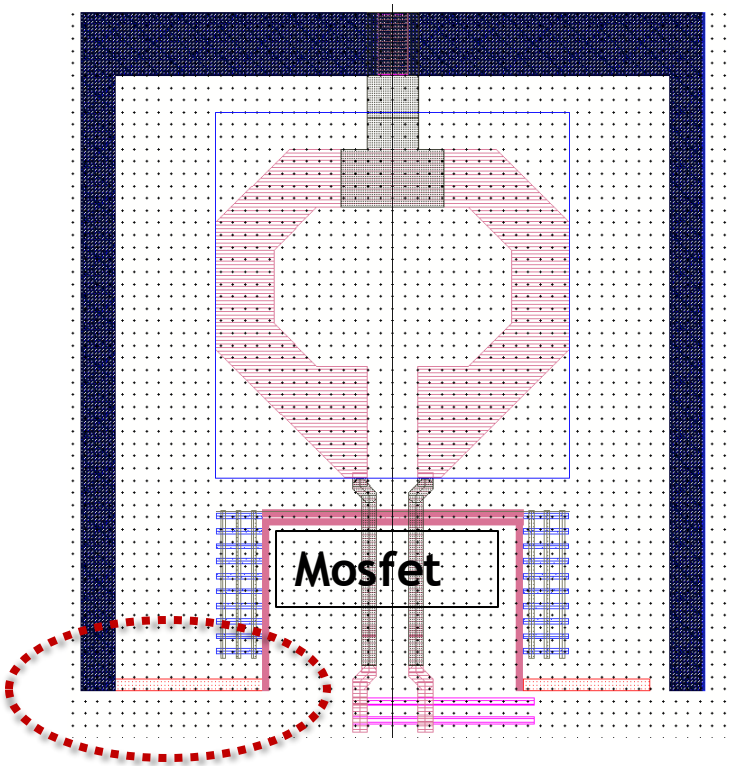




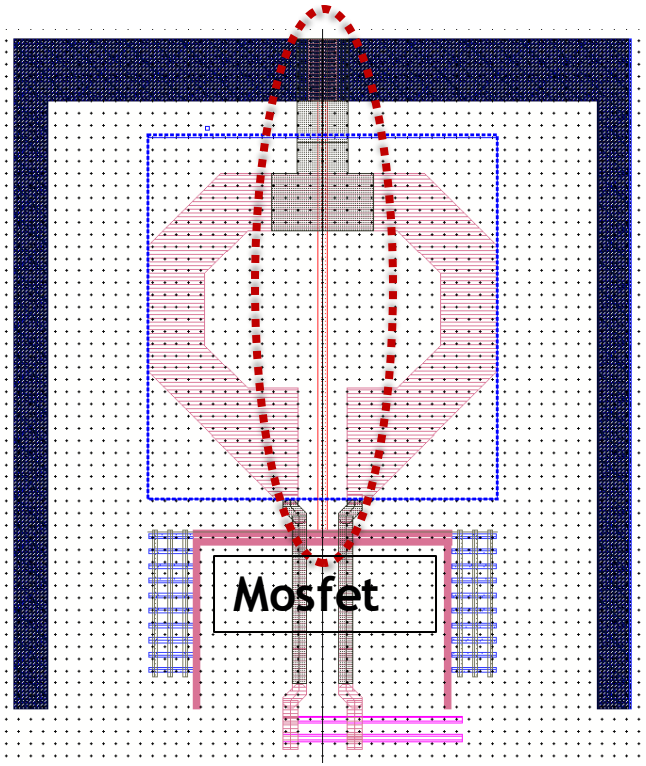


Inductor with Power Routing

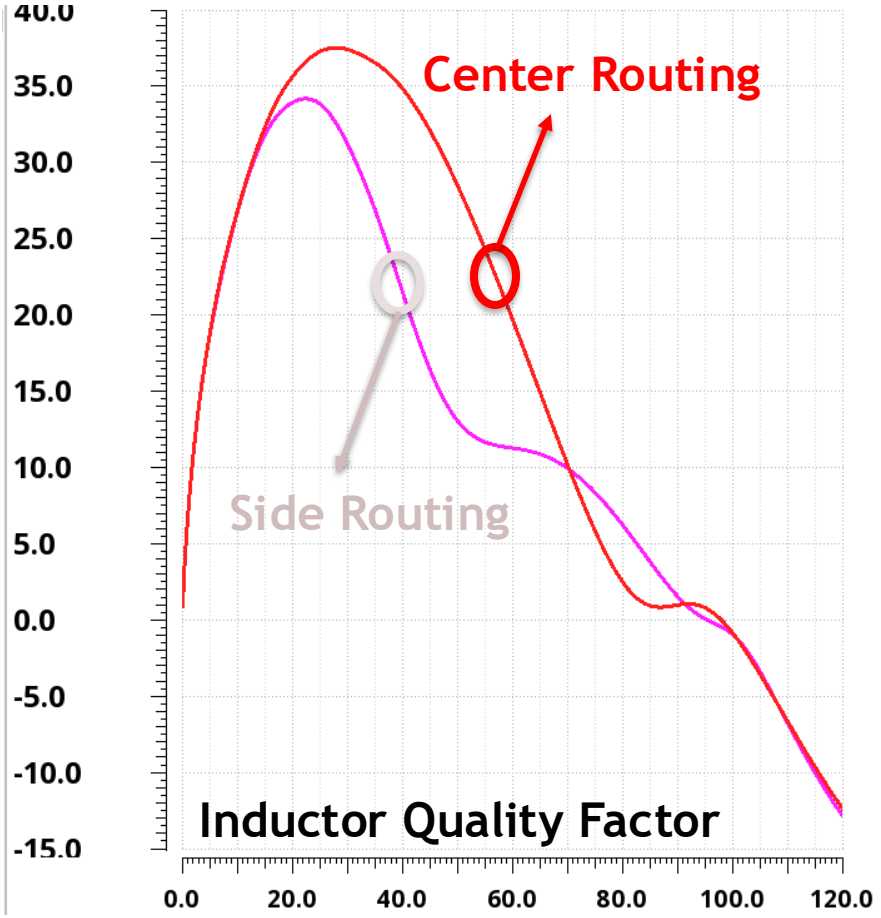
- Comparison of two power routing techniques
  - Side routing or center routing?



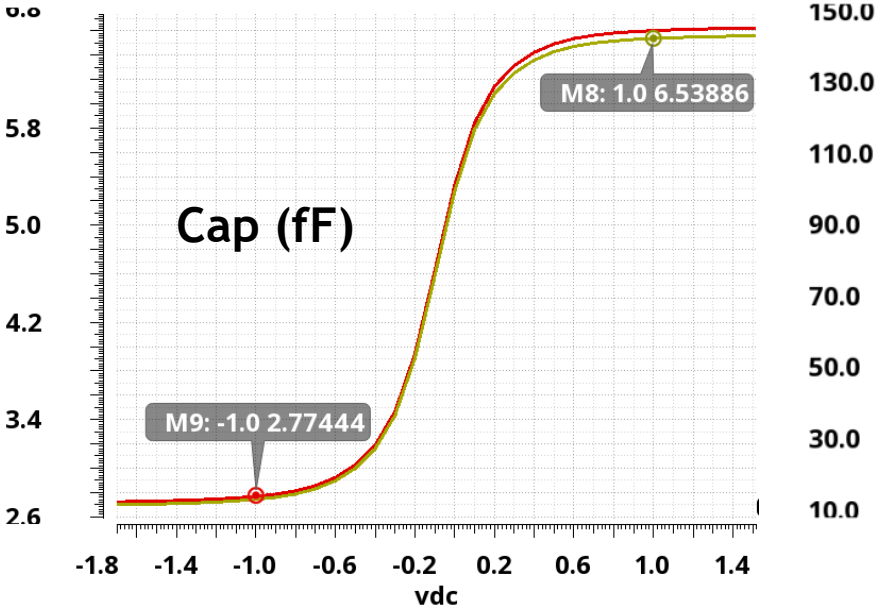
Power Routing from One Side



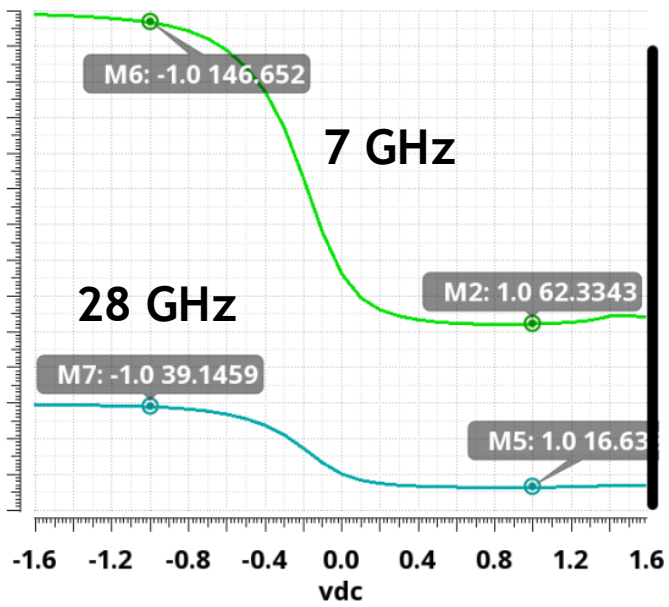
Power Routing from Center



Varactor Design



Capacitance versus Vdc



Q versus Vdc

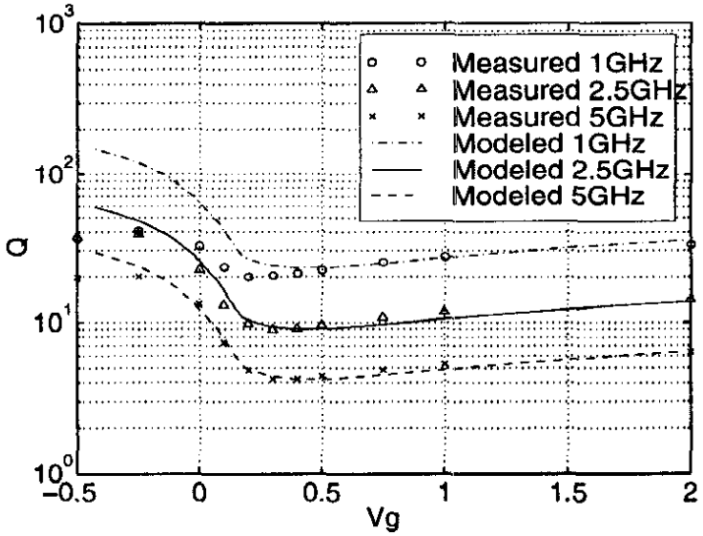


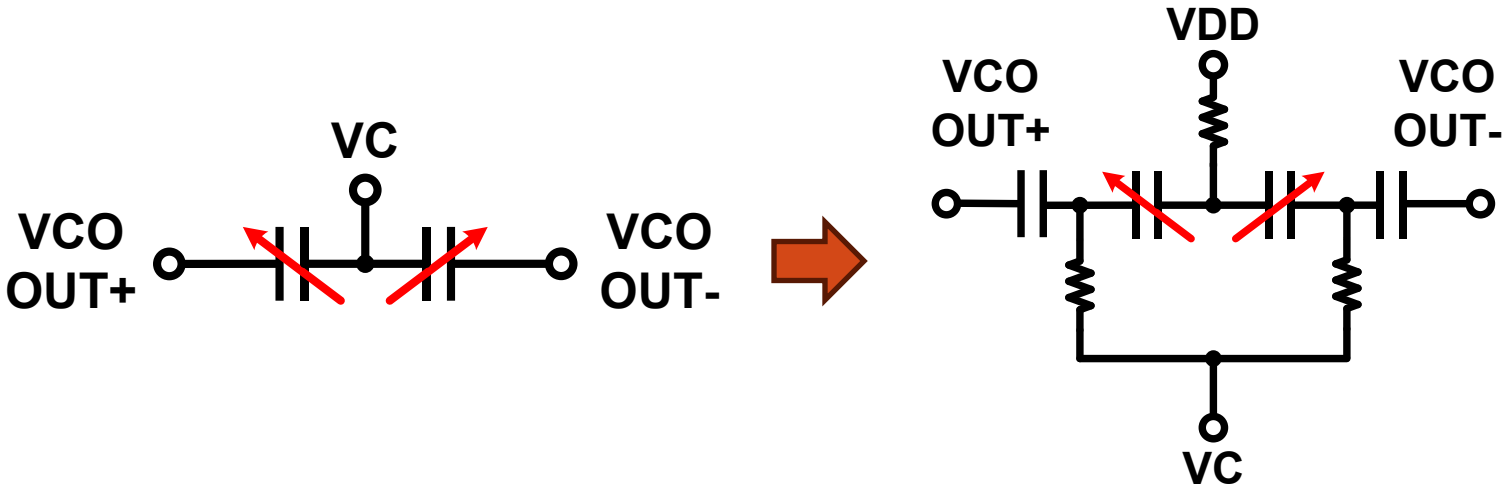
Fig. 6. Measured and Modeled Q

[S. S. WONG 1998 VLSI]

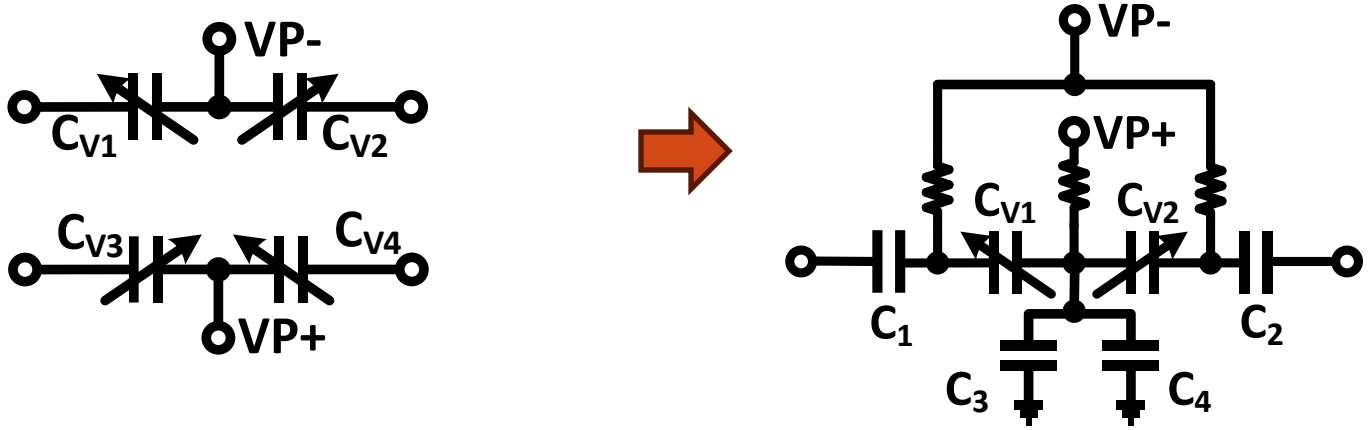
- The varactor should be designed and biased to achieve
  - Higher ΔC / ΔVcont
  - Higher quality factor

Varactor Design

- Varactor for integral path

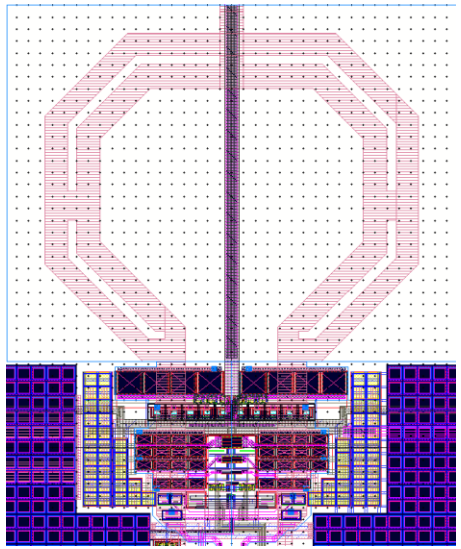


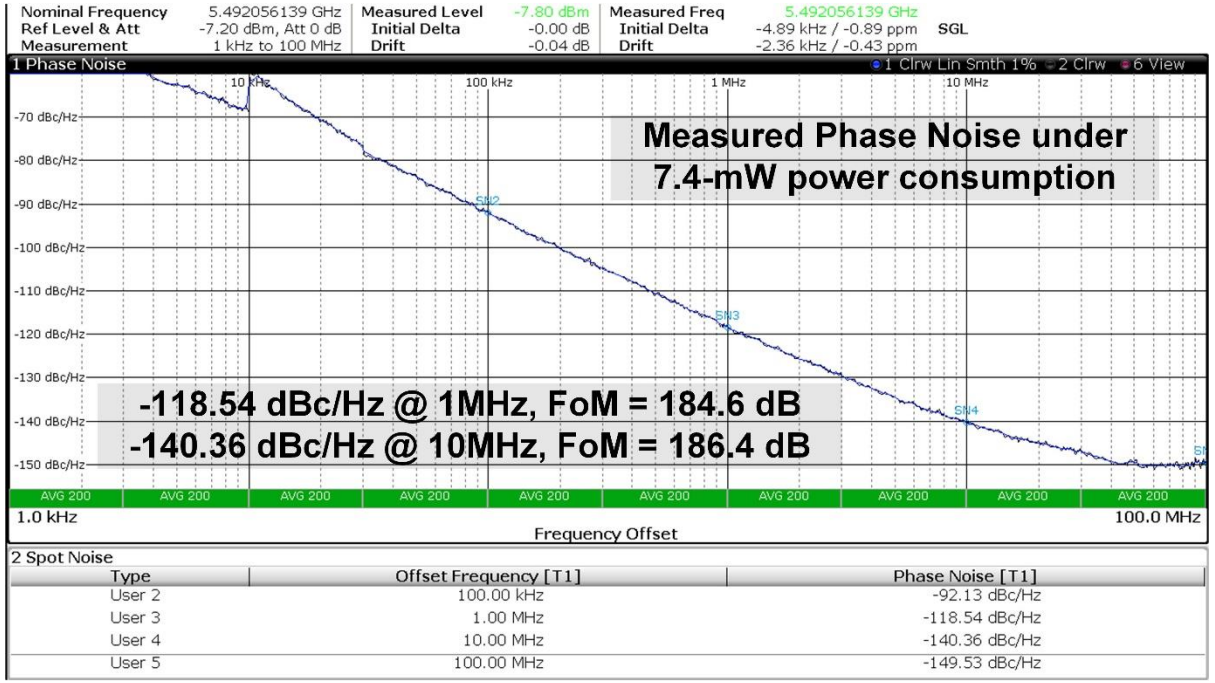
- Varactor for proportional path (differential operation)



A Design Example on Github

- A 20-24-GHz Class-C VCO with -186-dB FoM





Layout

Measurement Results

Website QR Code

[A-20-24-GHz-Class-C-VCO-with-186-dB-FoM/Measurement Results.jpg at main · HKUST-OWL-WANG-Li/A-20-24-GHz-Class-C-VCO-with-186-dB-FoM (github.com)]

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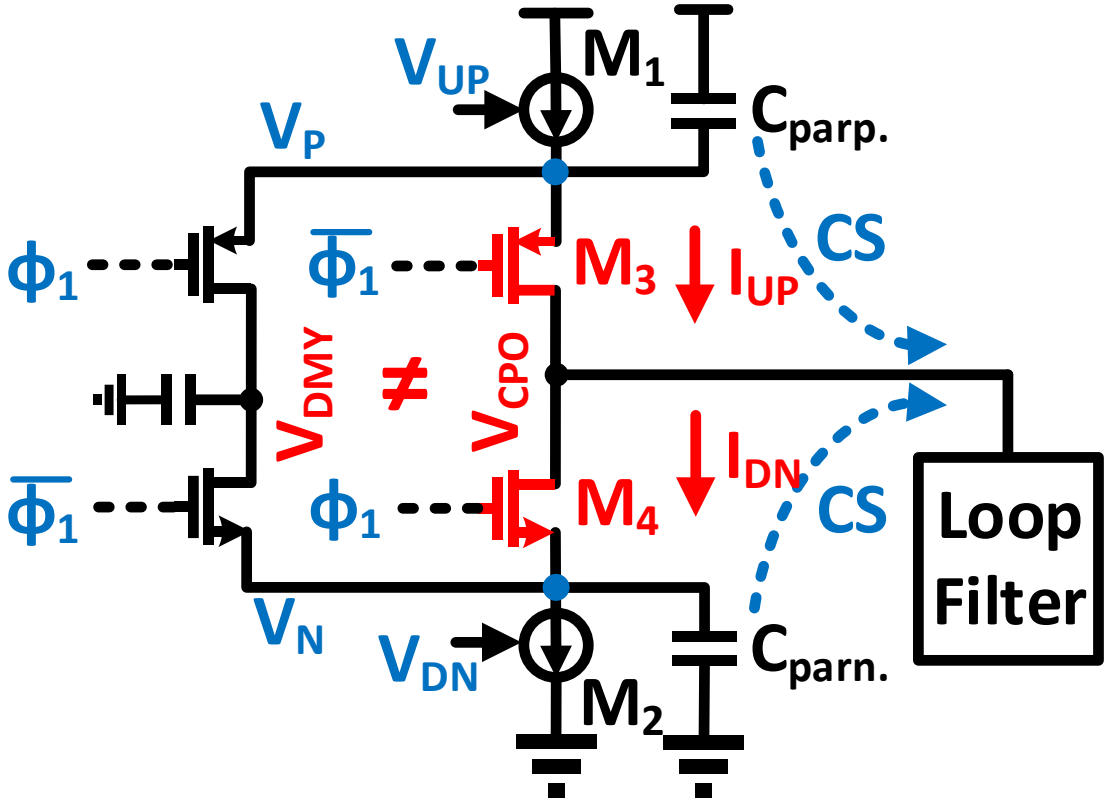
Key Circuits:
AC-Coupled Sub-Sampling Charge Pump

Offset Current in Conventional SSCP

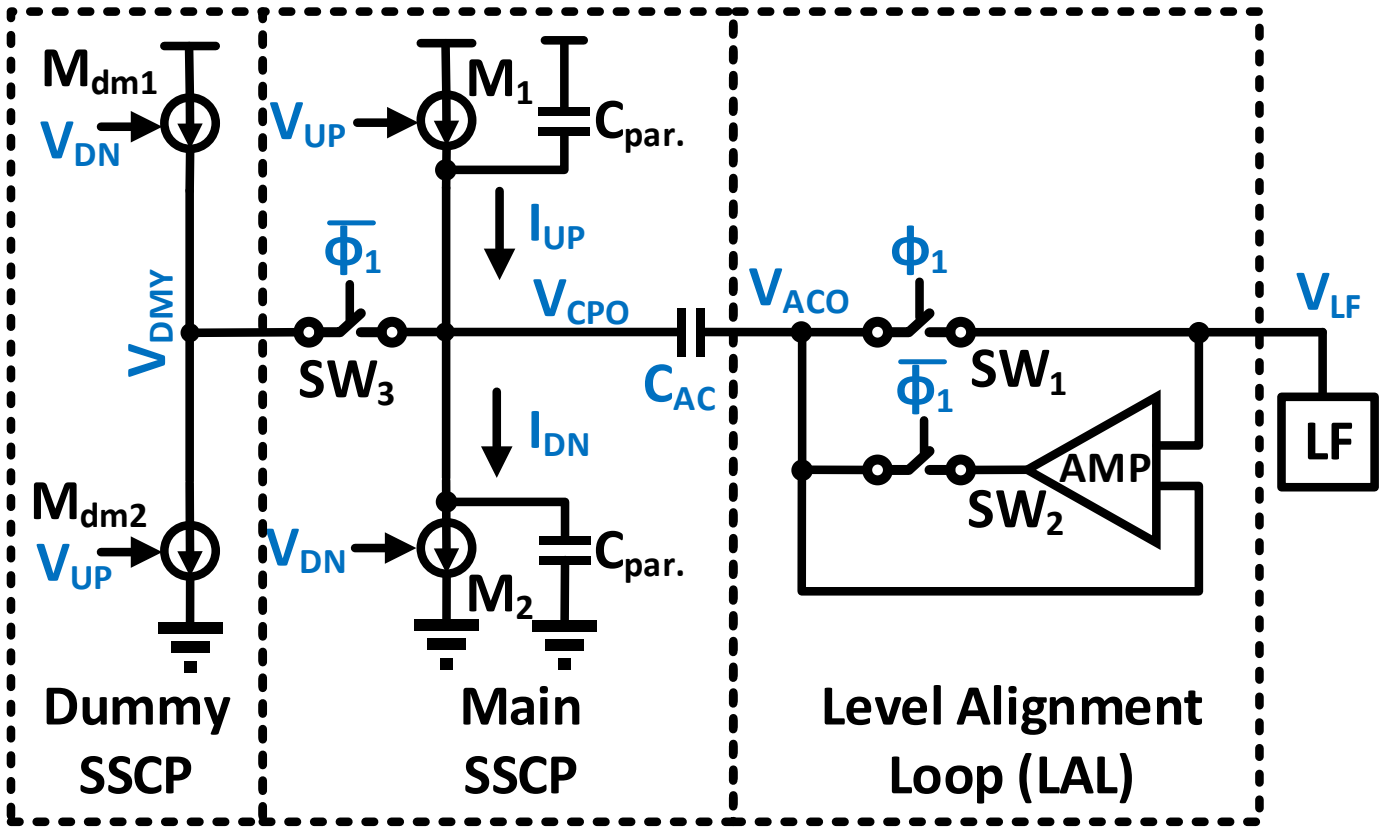
- $V_{DMY} \neq V_{CPO}$, charge sharing (CS).
- $I_{UP} \neq I_{DN}$ channel length modulation
- Mismatch between switch-on/off time of M_3 and M_4



- Offset charging current
- Extra current noise
- Reduced SSPD gain
- Degraded PN and spur

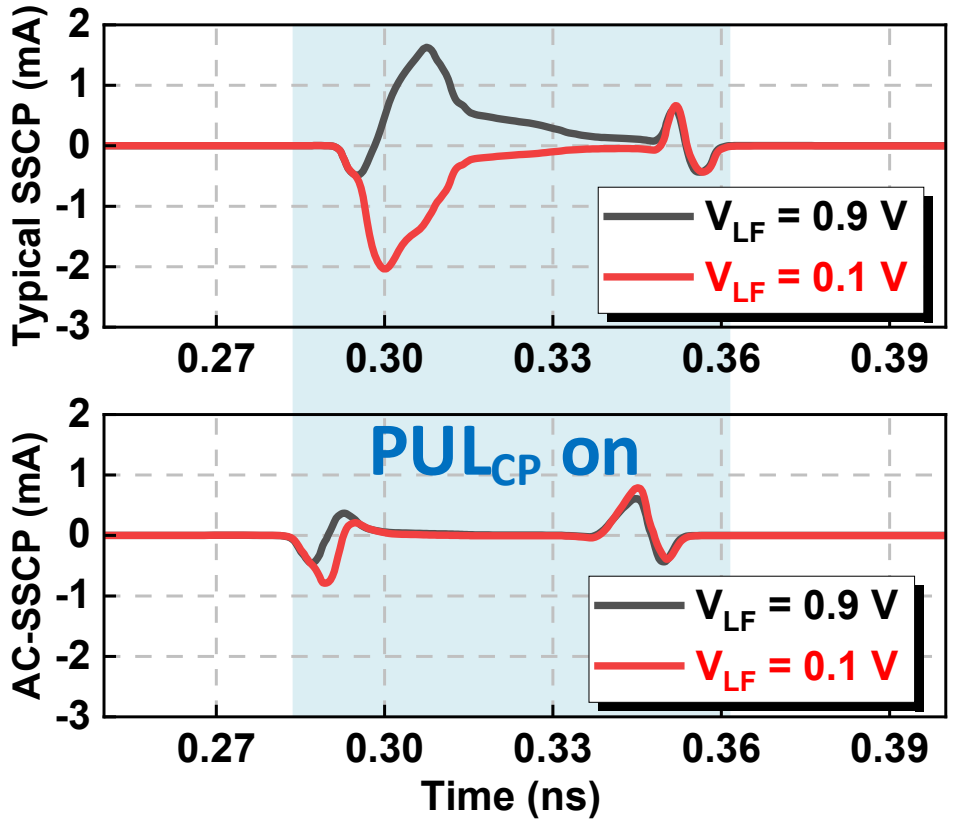
Proposed AC-SSCP

- **SSCP, LF isolated by C_{AC}**
  - V_{CPO} and V_{ACO}, regulated by Dmy SSCP and LAL
  - ☑ Resolves charge sharing issue
- **V_{CPO} aligned with V_{DMY}**
  - I_{UP} matches with I_{DN}
  - ☑ Resolves channel-length-modulation-induced current offset

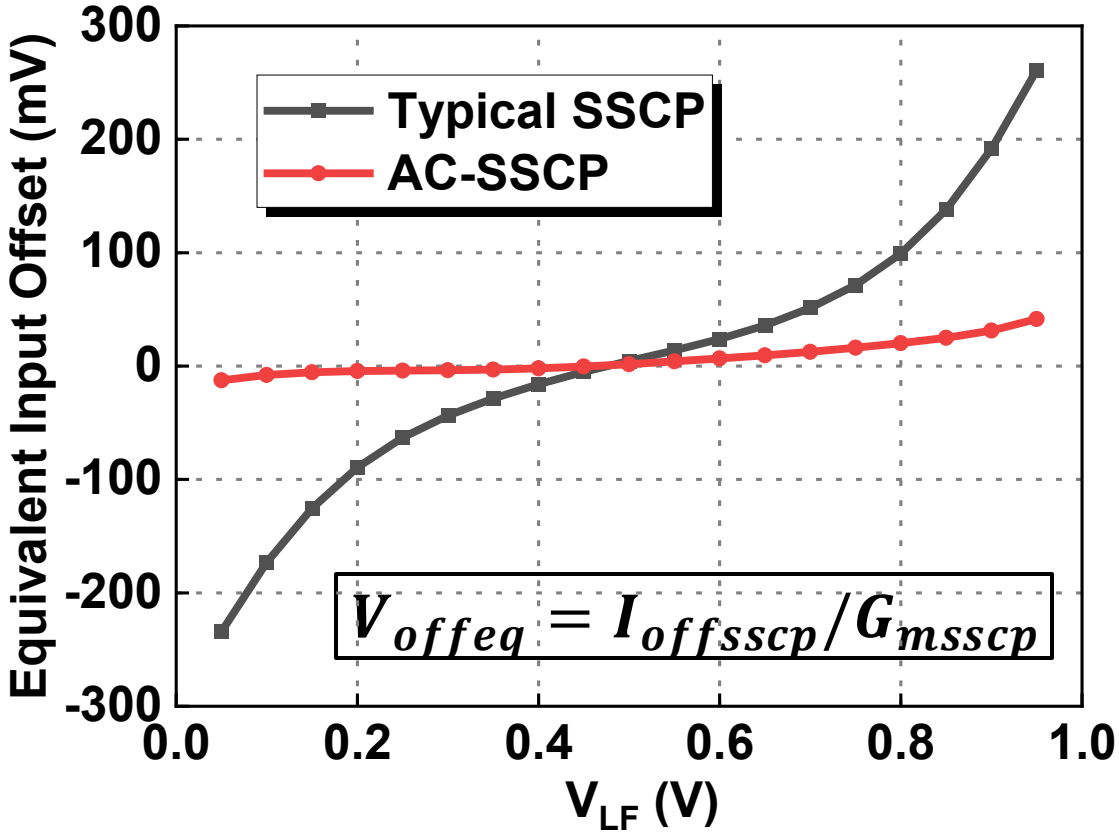


Simulation Validation

- Simulation setup: SSCP P/N input set to be equal, extract the offset output current ($I_{offsscp}$) versus VLF



$I_{offsscp}$ versus V_{LF}



Equivalent Input offset voltage (V_{offeq}) vs V_{LF}

Key Circuits:
Rail-to-Rail Double-Tail Comparator

Outline

- Motivation
- Input Common Mode Effect on Dynamic Comparators
- Proposed Comparator
- Performance Comparison
- Conclusion

Outline

- **Motivation**
- Input Common Mode Effect on Dynamic Comparators
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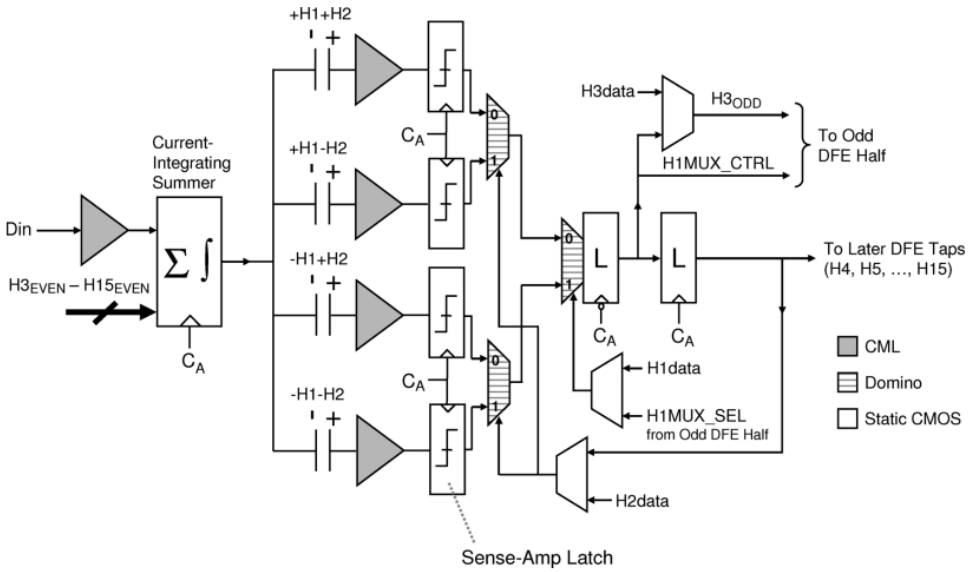
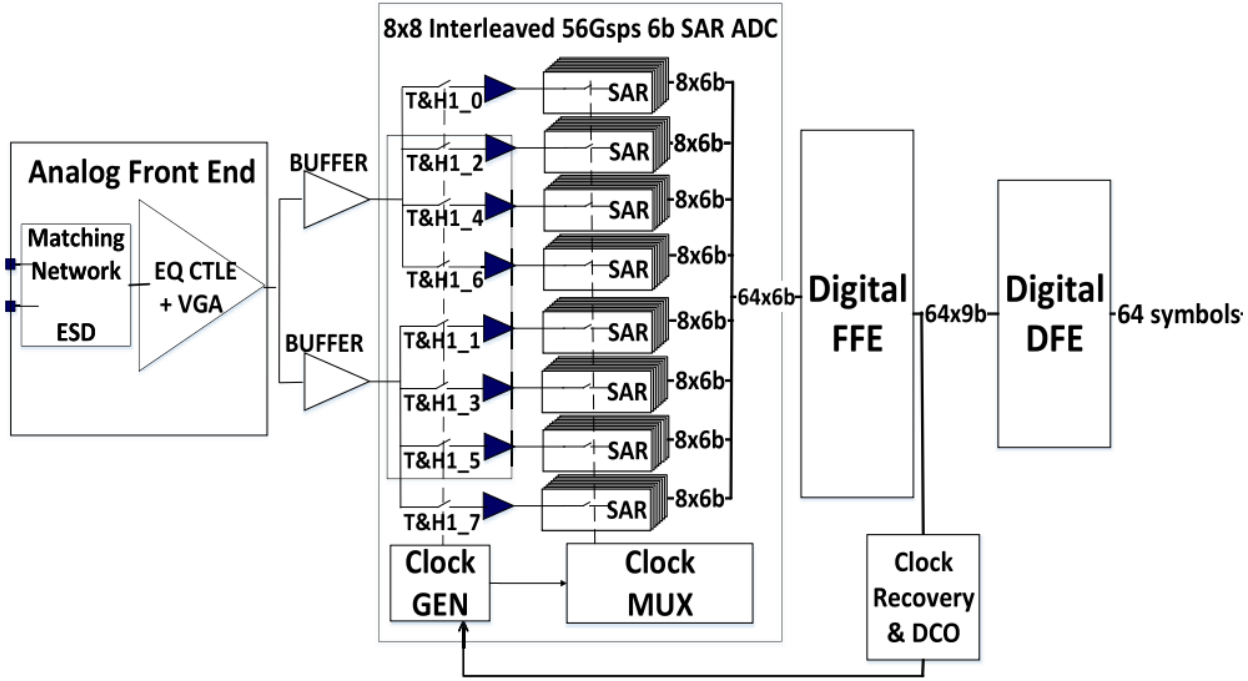
Motivation

- Comparators are widely used in analog and ADC-based receivers

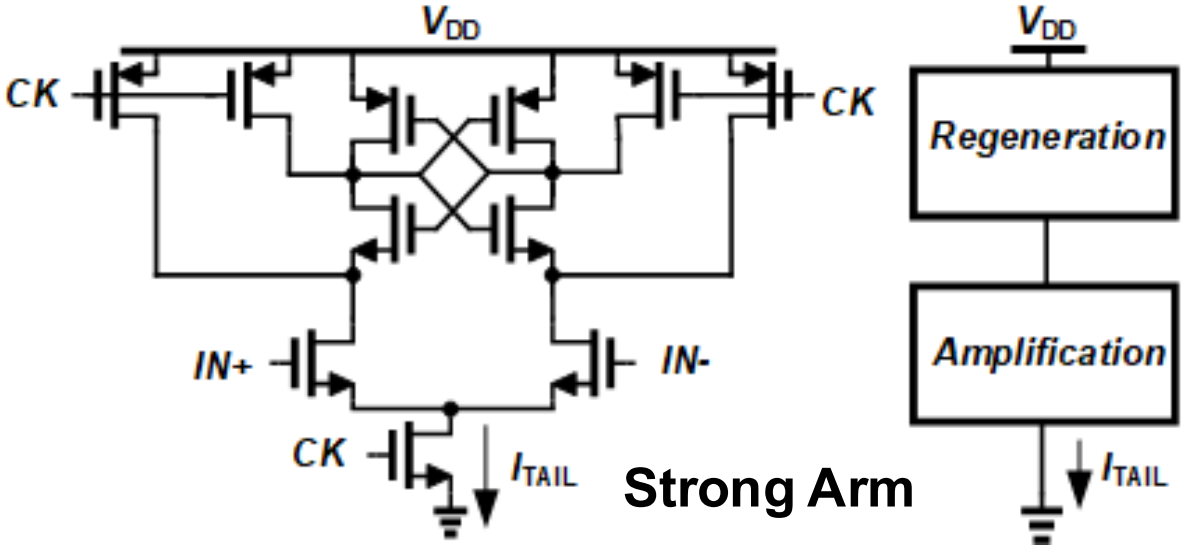




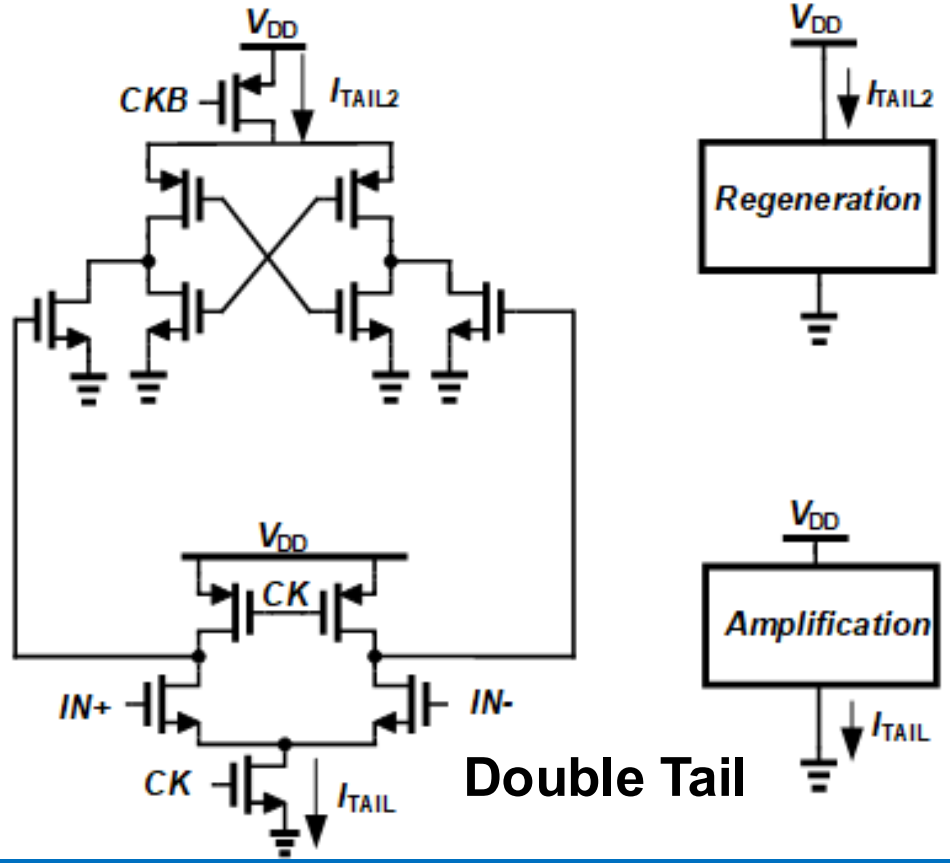
- The latency and power consumption of comparators are critical in these applications

Commonly used dynamic comparators

- Strong Arm
  - Tail current is shared between amplification and regeneration
- Double Tail
  - Separates the tail currents
  - Less sensitive to input common mode



- For a small input common mode, the input differential pairs are turned off
  - Speed for both is highly degraded



Outline

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- **Input Common Mode Effect on Dynamic Comparators**
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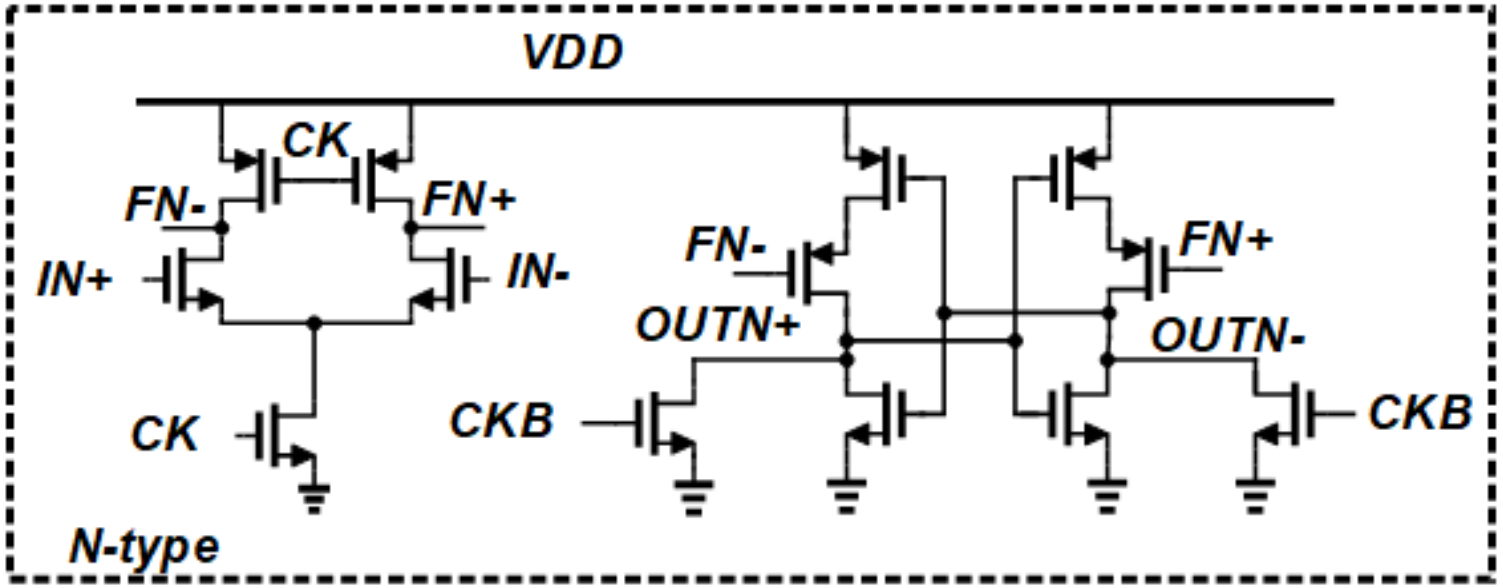
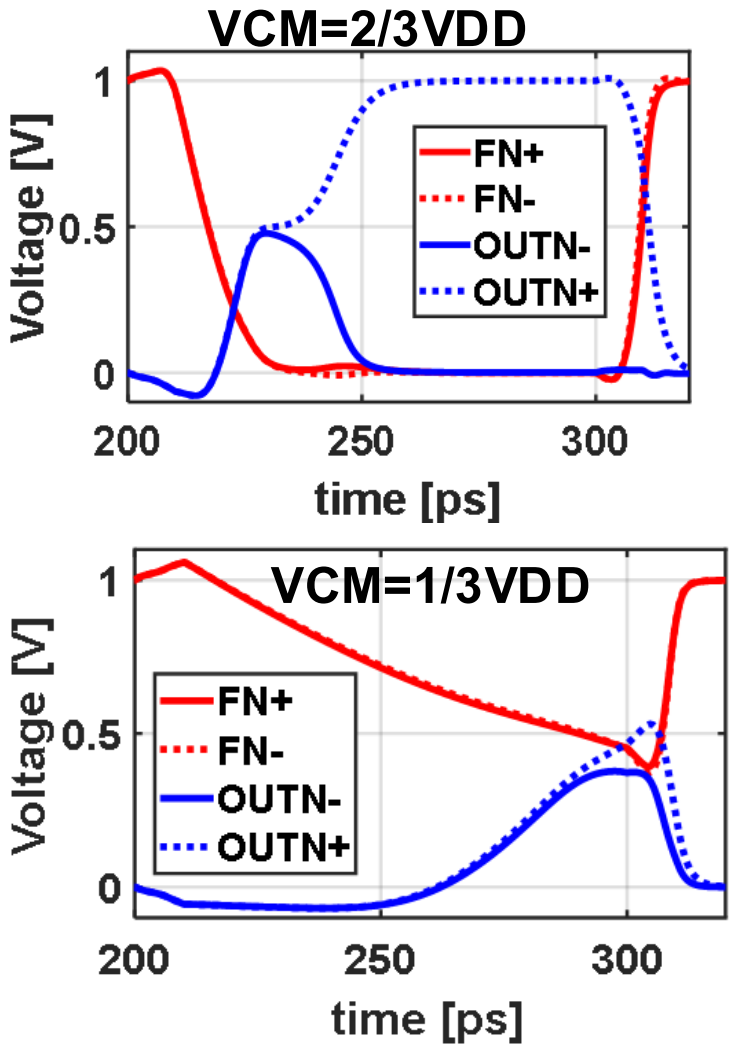
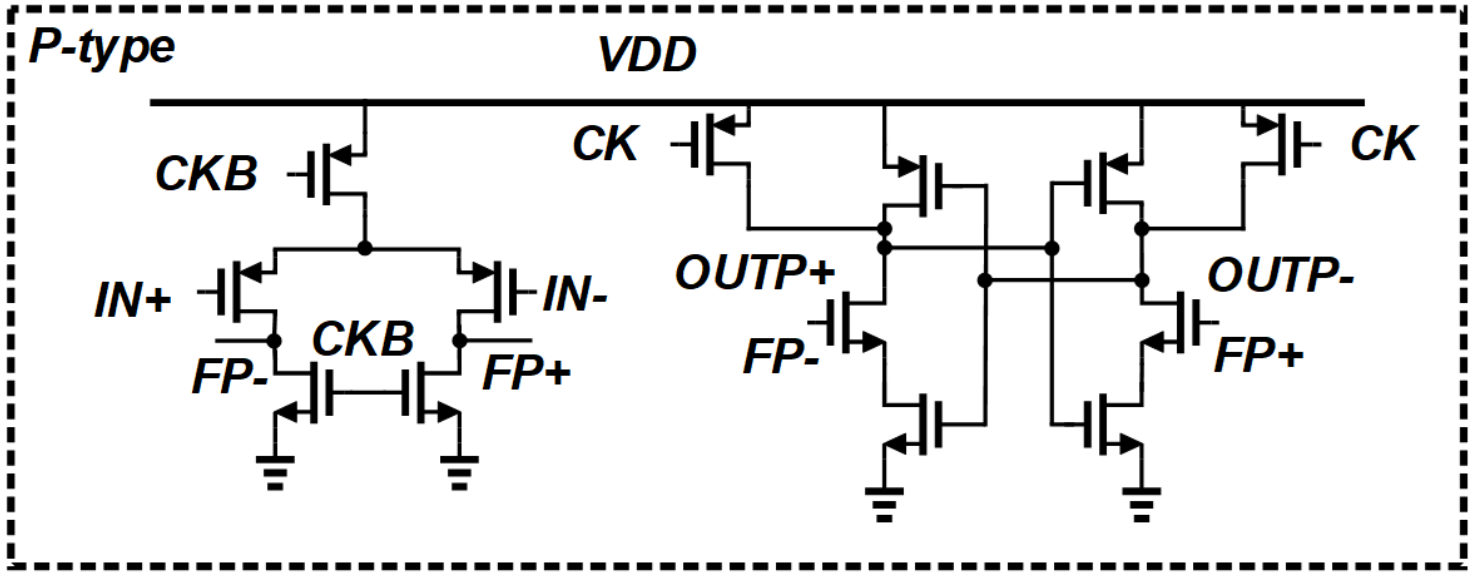
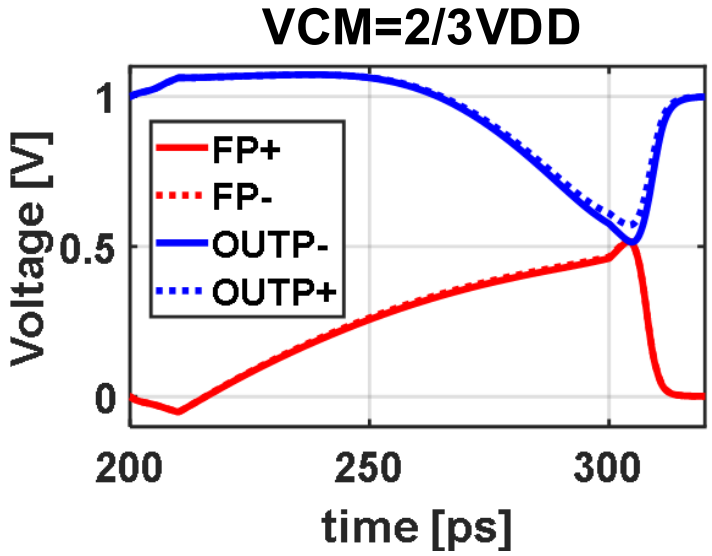
N-type Dynamic Comparator

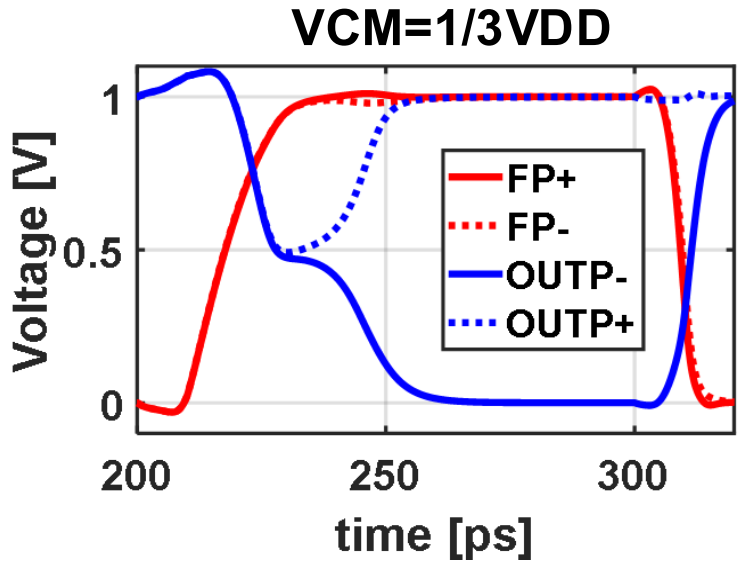




P-type Dynamic Comparator







Outline

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- **Proposed Comparator**
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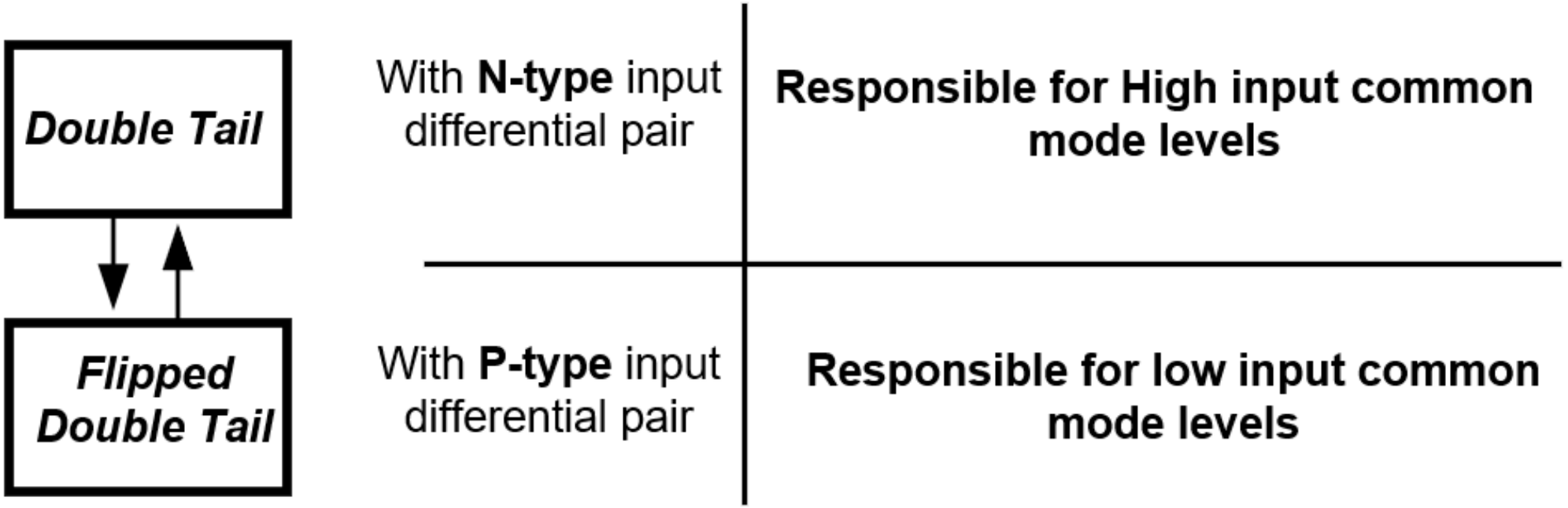
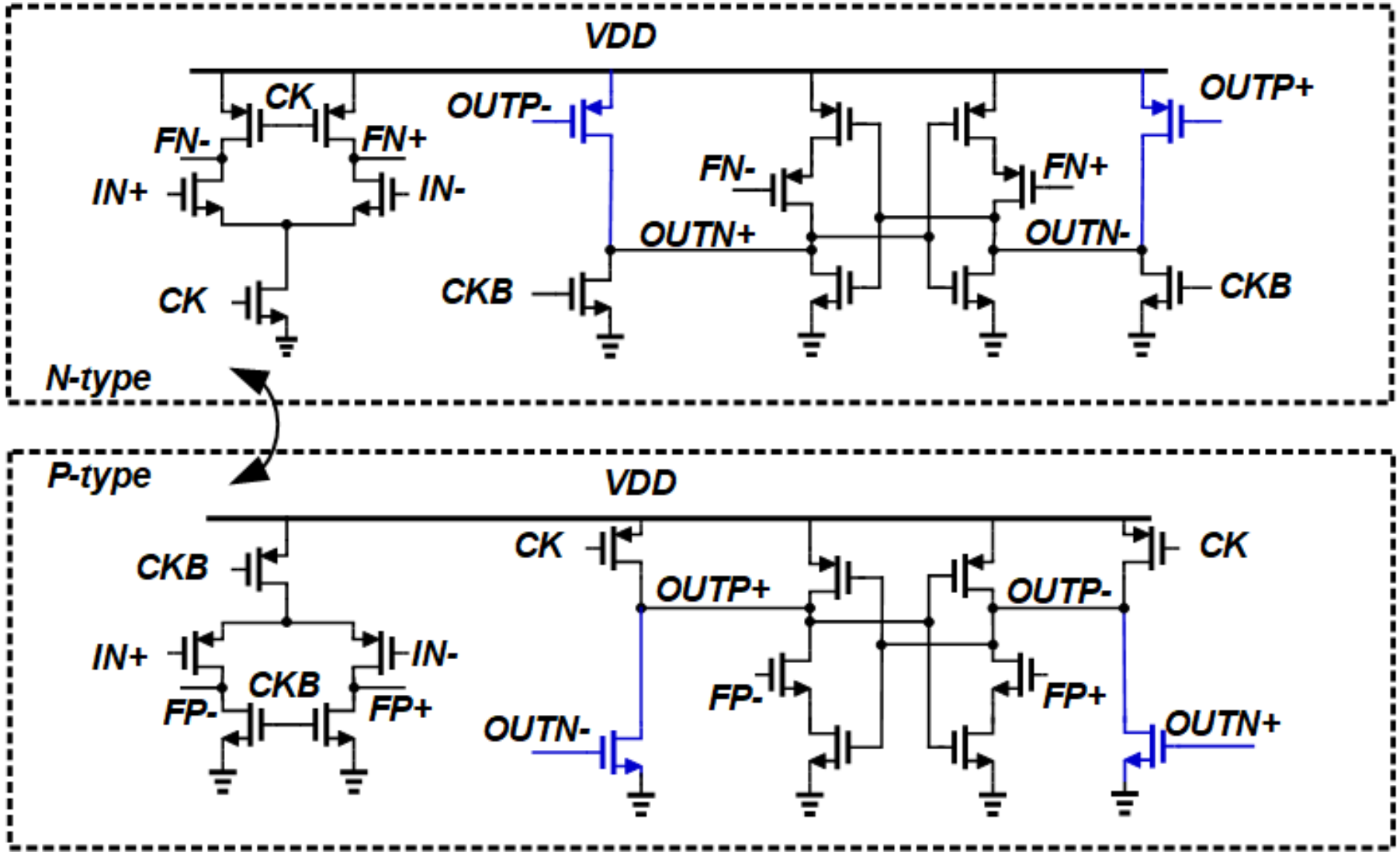
Proposed Dynamic Comparator

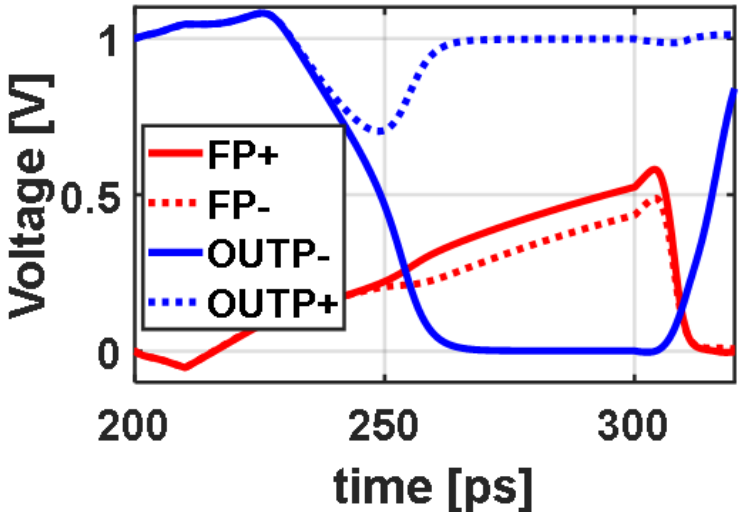


- A desired mutual connection of N-type and P-type avoids
  - Speed degradation
  - Static power consumption

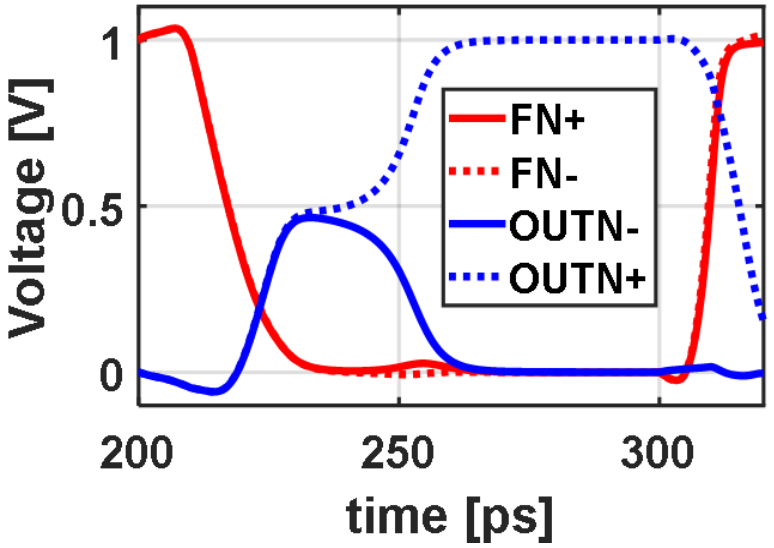
Proposed Dynamic Comparator

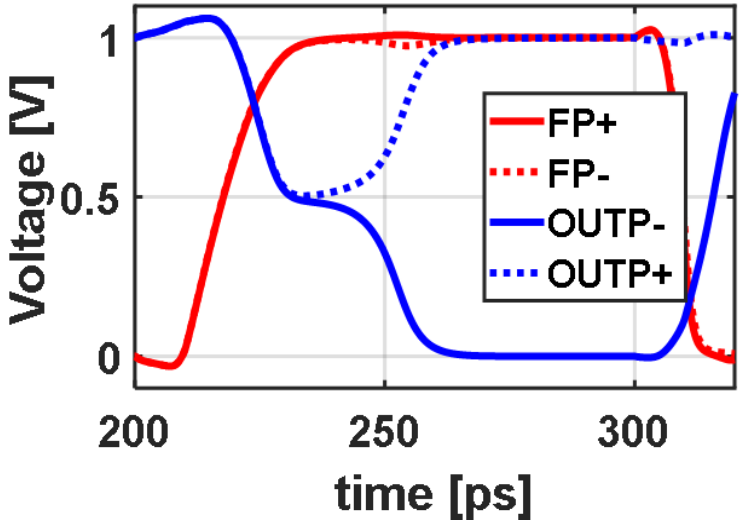


Proposed Dynamic Comparator (cont.)

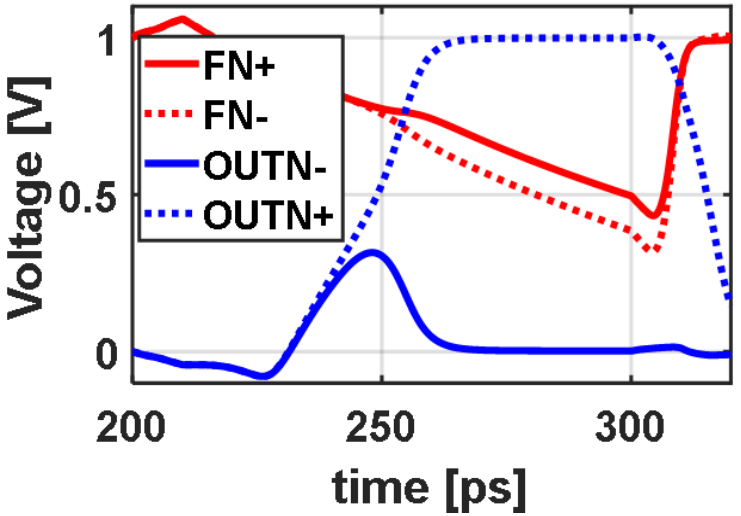


VCM=2/3VDD

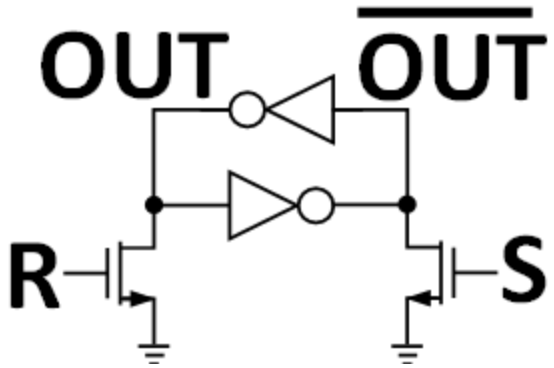


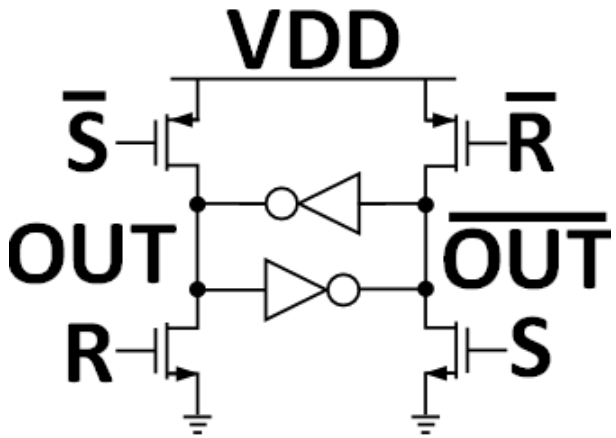


VCM=1/3VDD



SR-latch





- Conventional
  - Pull-down is stronger than pull-up
  - Asymmetric output

- Proposed
  - Equally strong pull-down and pull-up
  - Symmetric outputs

Outline

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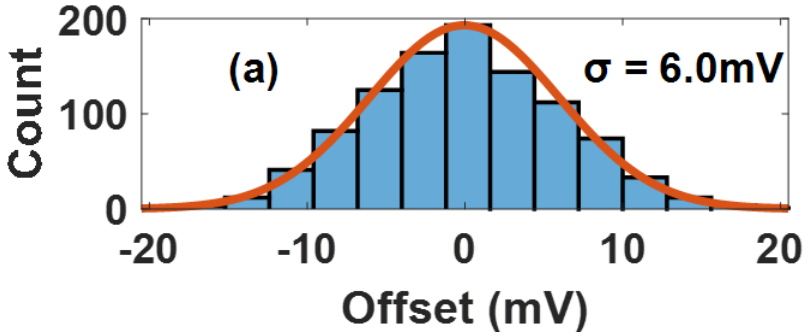
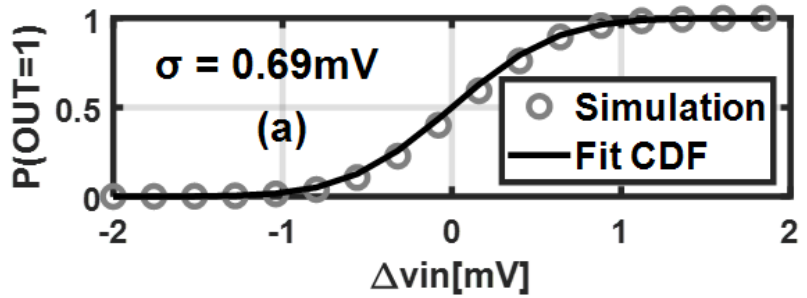
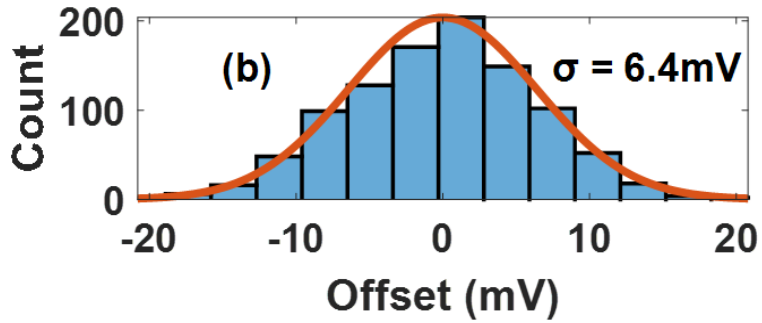
Input referred offset and noise comparison

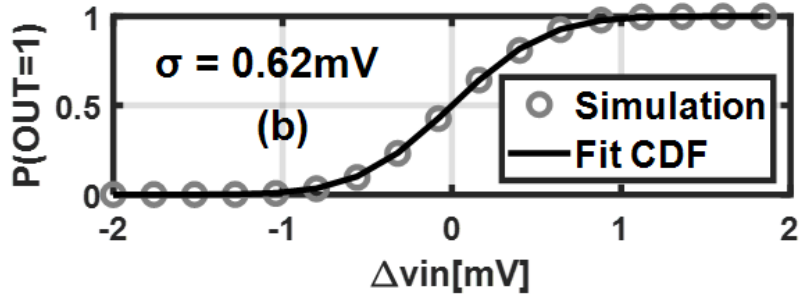


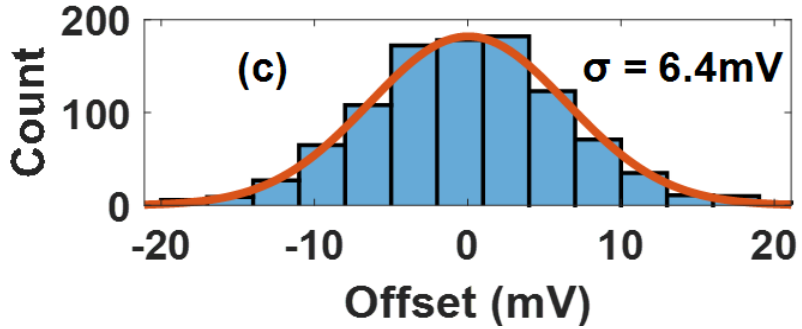
N-type



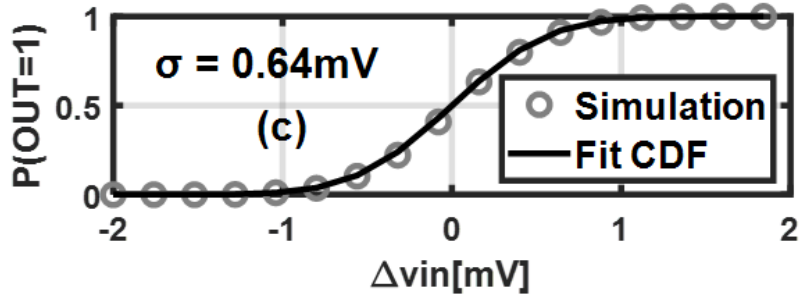


P-type

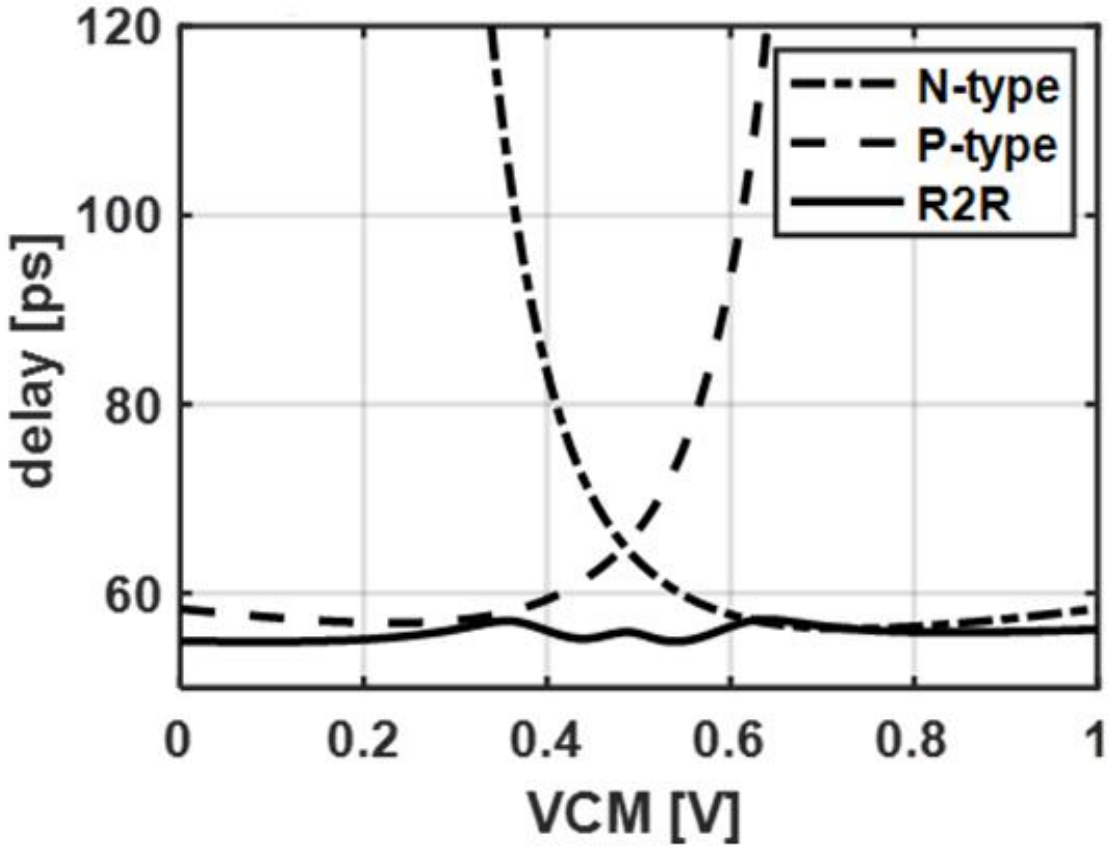




Proposed



Latency Comparison



- The latency of the proposed comparator is almost constant in the common mode range from 0 to VDD

Comparator Latency

Specifications	N-type*	P-type*	Proposed
Noise (σ)	0.69mV	0.62mV	0.64mV
Offset (σ)	6.0mV	6.4mV	6.4mV
Delay variation	>700%	>700%	<4%
Energy efficiency (pJ)	0.13	0.13	0.17

*The coupling transistors and their loading effect are not included

Outline

- Motivation
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Conclusion

- Proposed a rail-to-rail dynamic comparator that maintains constant latency with input common mode variations.
- Non-rail-to-rail counterparts of the proposed dynamic comparator slow down or fail to operate for almost half of the input common mode range.
- The power efficiency penalty of the proposed comparator is 33%.

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- L. Wang, Y. Chen, C. Yang, X. Zhao, Pui-In Mak, Franco Maloberti, and Rui P. Martins et al., "A 10.8-to-37.4 Gb/s Reference-Less FD-Less Single-Loop Quarter-Rate Bang-Bang Clock and Data Recovery Employing Deliberate-Current-Mismatch Wide-Frequency-Acquisition Technique," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 70, no. 7, pp. 2637-2650, July 2023.
- L. Wang, Y. Chen, X. Zhao, Pui-In Mak ,Franco Maloberti and Rui P. Martins. “A 6-to-38Gb/s capture-range bang-bang clock and data recovery circuit with deliberate-current-mismatch frequency detection and interpolation-based multiphase clock generation.” *Int J Circ Theor Appl.* 2023; 51(5): 1988-2015.
- L. Wang , Y. Chen, C.Yang, X. Zhao, Pui-In Mak, Franco Maloberti, and Rui P. Martins "A 10.8-to-37.4Gb/s Single-Loop Quarter-Rate BBCDR Without External Reference and Separate FD Featuring a Wide-Frequency-Acquisition Scheme," *29th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, Glasgow, United Kingdom, 2022, pp. 1-4.

Reference from Our Work

- L. Wang, Z. Liu and C. P. Yue, "A 24-30 GHz Cascaded QPLL Achieving 56.8-fs RMS Jitter and −248.6-dB FoMjitter," *2023 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, Kyoto, Japan, 2023, pp. 1-2
- L. Wang, Z. Zhang, C. Wang, R. Azmat, W. Shi and C. P. Yue, "A 60-Gb/s 1.2-pJ/bit 1/4-Rate PAM-4 Receiver With a Jitter Compensation CDR," *IEEE Journal of Solid-State Circuits*, vol. 59, no. 2, pp. 449-463, Feb. 2024
- L. Wang, Z. Zhang and C. P. Yue, "A 60-Gb/s 1.2-pJ/bit 1/4-Rate PAM4 Receiver with a -8-dB JTRAN 40-MHz 0.2-UIPP JTOL Clock and Data Recovery," *2021 Symposium on VLSI Circuits*, Kyoto, Japan, 2021, pp. 1-2
- J. Abdekhoda, L. Wang, R. Sarvari and C. P. Yue, "A Bang-Bang Phase Detector for PAM-N Signaling," 2023 IEEE 15th International Conference on ASIC (ASICON), Nanjing, China, 2023, pp. 1-4

香港科技大學
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HKUST OWL

Practical Implementation Techniques
芯片设计技巧

Prof. C. Patrick Yue 俞捷教授

芯动力人才计划®第 125 期国际名家讲堂

Outline

- Motivation
  - Practical Implementation Techniques
- Example 1
  - A Performance Study of Layout and Vt Options for Low Noise Amplifier Design in 65-nm CMOS [RFIC'12]
- Example 2
  - Differential Stacked Spiral Inductor and Transistor Layout Designs for Broadband High-Speed Circuits [RFIT'14]
- Example 3
  - Package Design for a 10 Gigabit Ethernet Transceiver [DesignCon'2004]
- Conclusion

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Motivation

- Physical layout implementations and technology options are becoming more and more crucial for circuits design
- The actual design performance is strongly affected by the layout practice and style
- Parasitic capacitance brought by routings and the choice of threshold voltage should be taken care
- On-chip inductor occupies a huge amount of chip area: high cost and long interconnections
- A more compact inductor layout with higher inductance density is more desirable

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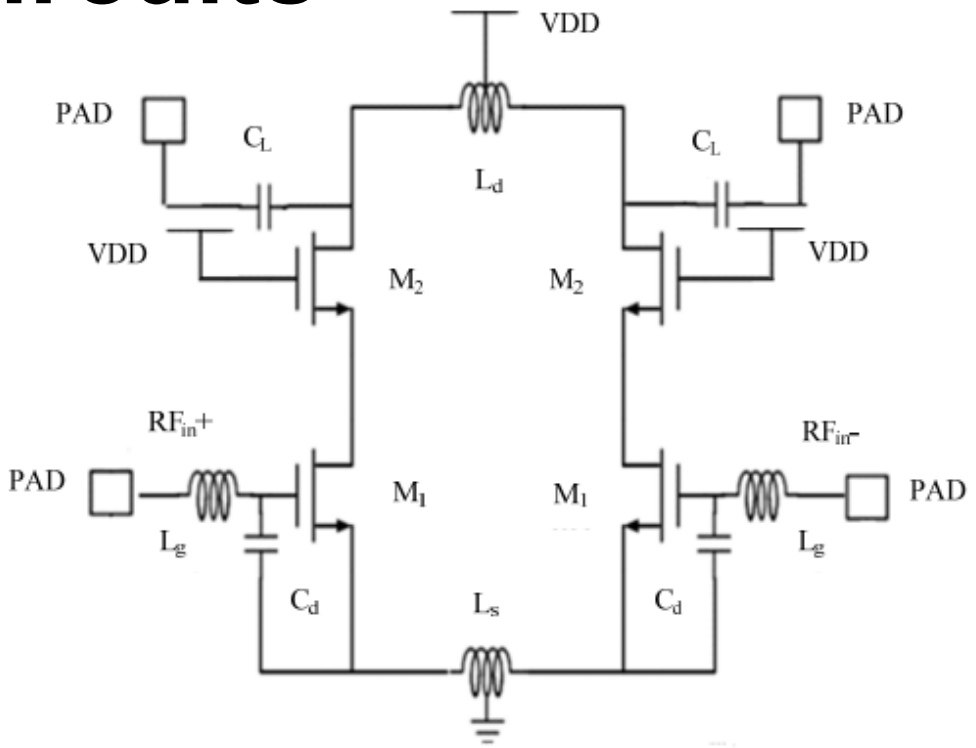
A Performance Study of Layout and Vt Options for Low Noise Amplifier Design in 65-nm CMOS

LNA Test Circuits

- Differential cascode LNA topology
- Noise figure performance has higher priority with an S_{11} < 10dB
- Input noise and impedance matching are realized by the series inductor L_g and the source degeneration inductor L_s
- MIM capacitors Cd are inserted to reduce the gate-induced current noise



M_1		M_2	
W : L	I_{bias} (μA/um)	W : L	I_{bias} (μA/um)
80 μm : 60nm	94	80 μm : 60nm	94

L_g	L_s	L_d	C_d	C_L
4.3 nH, Q=11	0.5 nH, Q=14	7.7 nH, Q=11	160 fF	190 fF

- Schematic of the 5-GHz LNA

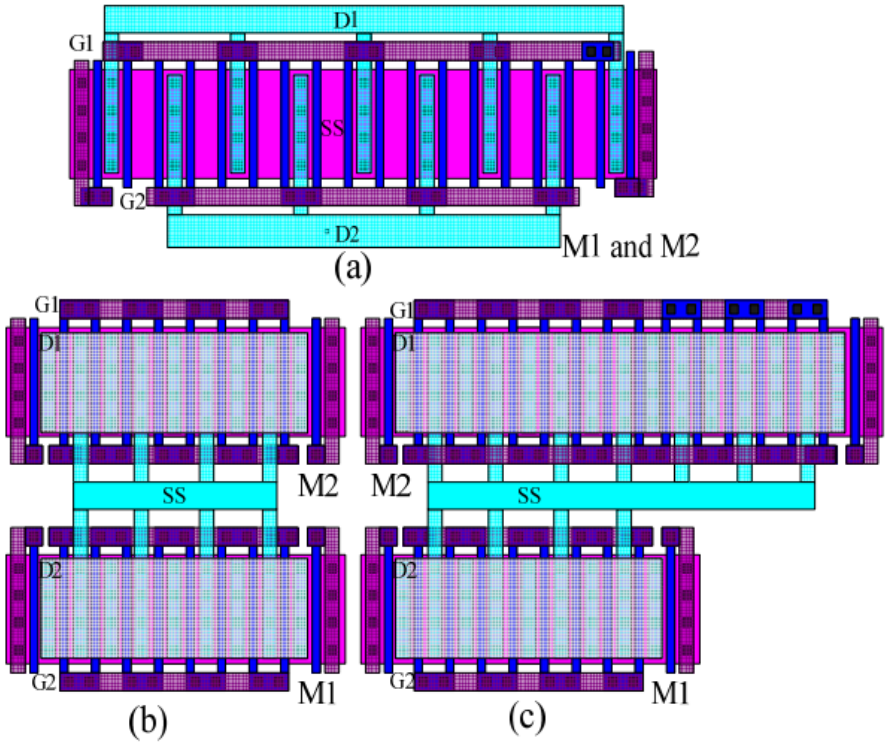
Layout and Vt Options

- 5 different versions of LNA test circuits are designed
- Design choice: merged diffusion layout / individual device from PDK
- Design choice: normal Vt / low Vt

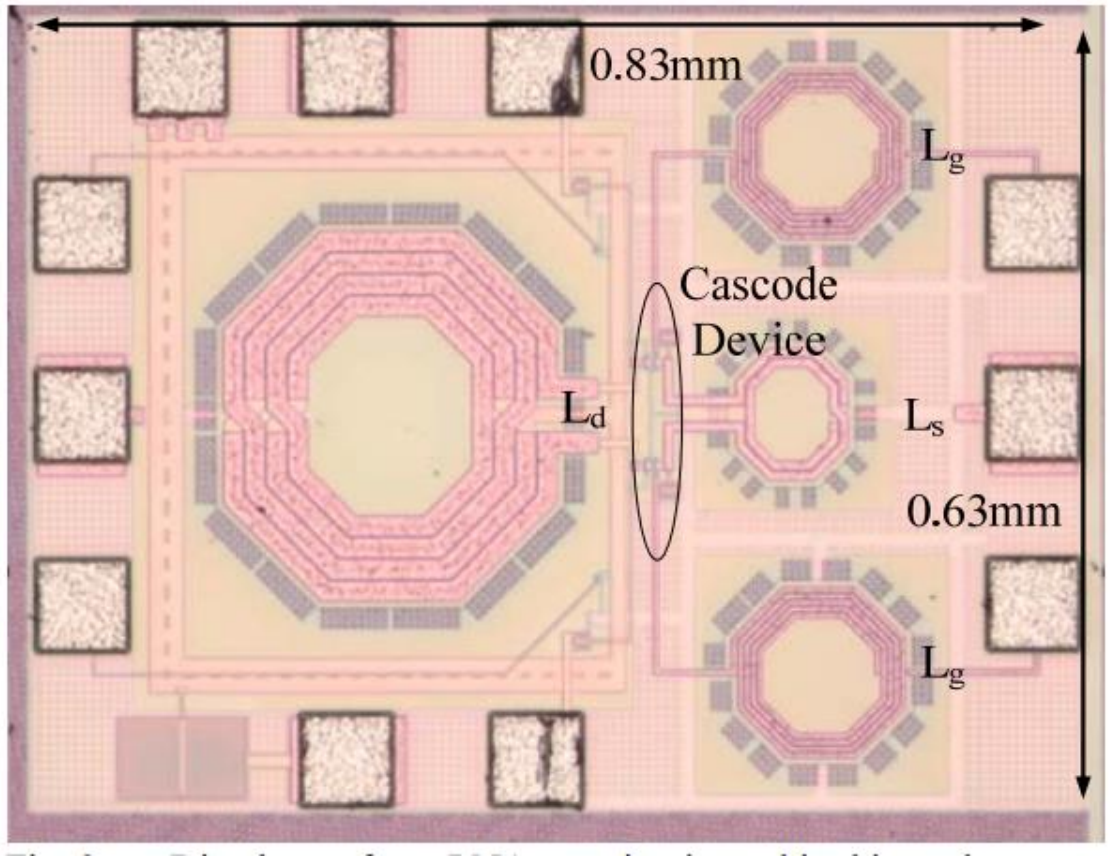
#	Design Splits Label	Cascode to Main Device Ratio	Vt Option	Layout Features	
1	Merged_Nor *V_t (RBC)*	1 : 1	Normal	Merged cascode and main device	Single-sided gate contact
2	Merged_L*V_t (RBC)*	1 : 1	Low		
3	PDK_NorVt	1 : 1	Normal	Individual cascode and main device using PDK RF transistors	Double-sided gate contact
4	PDK_LVt	1 : 1	Low		
5	PDK_LVt_ 1.7:1	1.7 : 1	Low		

- Design splits and key attributes

Layout View

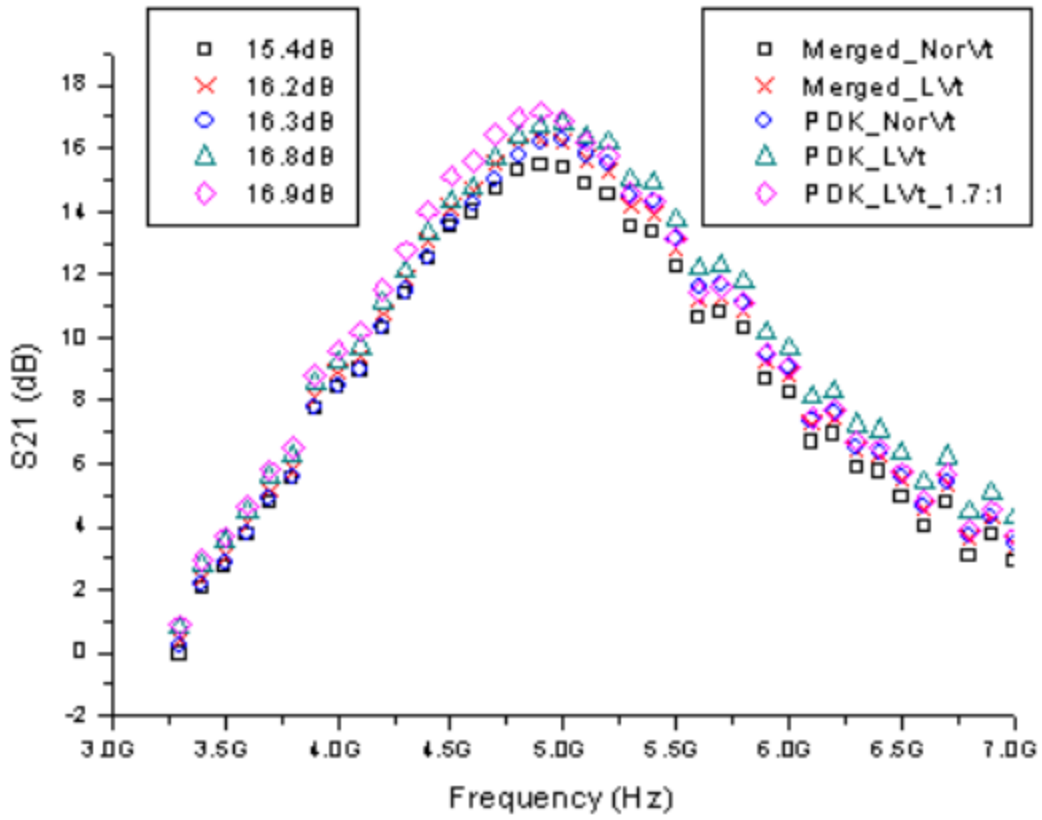


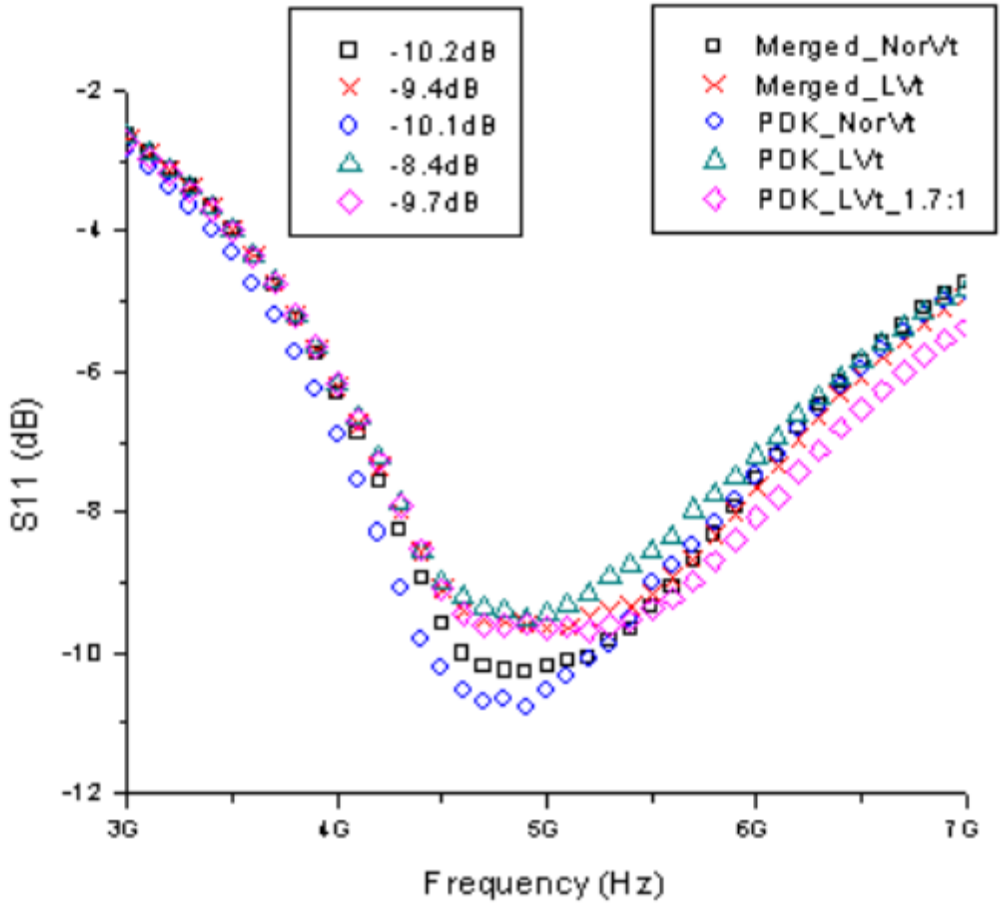
- (a) Merged diffusion layout
- (b) Standard single transistor RF cell
- (c) Standard RF cell, but the main device width ratio is changed



- Die photo of one LNA test circuit

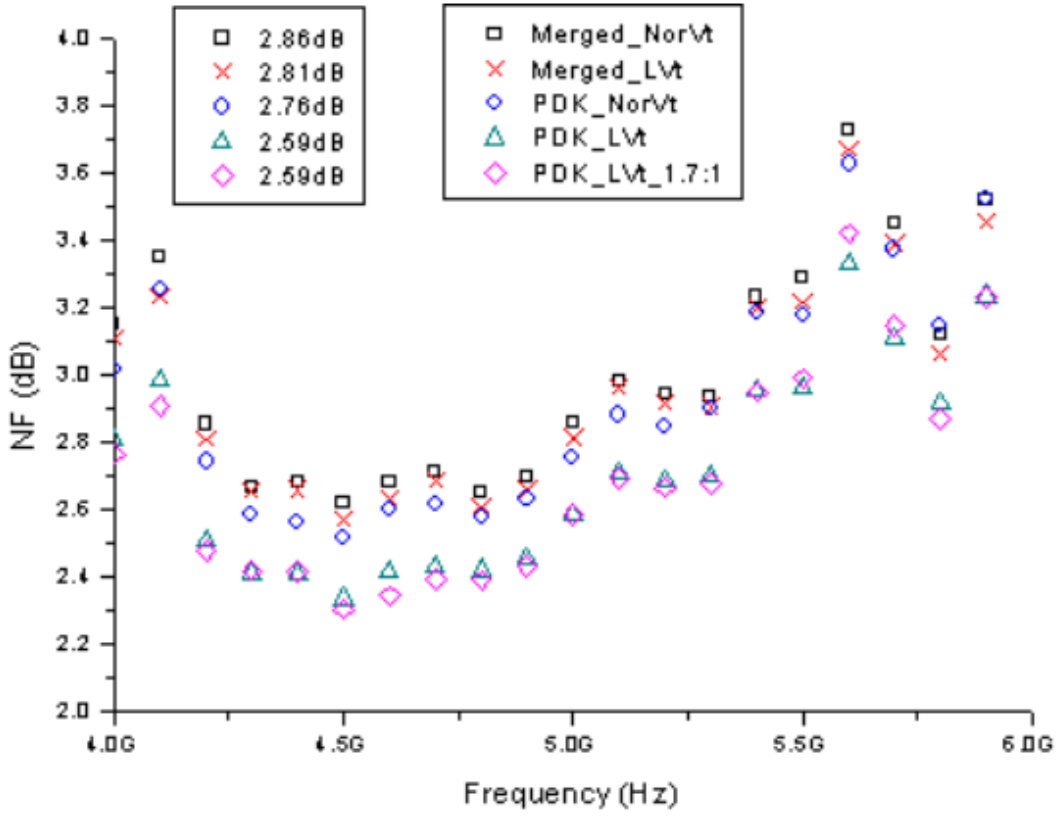
Measurement Results

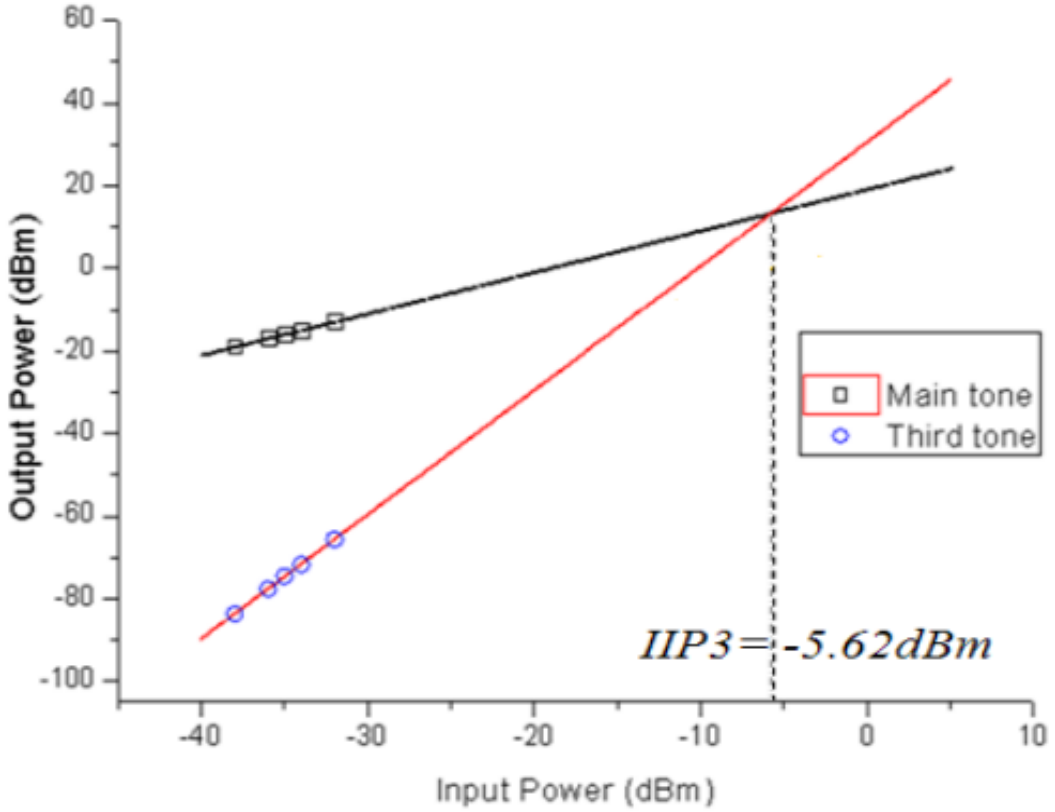




- Measured results of S_{21} for all 5 LNAs
- Measured results of S_{11} for all 5 LNAs

Measurement Results





- Measured noise figure for all 5 LNAs
- Measured IIP3 for the LNA using merged diffusion and normal Vt

Conclusions

- A set of 5-GHz LNAs are designed, and the performance impact of different layout and Vt options are evaluated
- For gain and NF considerations, individual transistor and low Vt are preferred
- When linearity and matching are more important, normal Vt devices with merged diffusion area can yield better performance

Outline

- Motivation
  - Practical Implementation Techniques
- Example 1
  - A Performance Study of Layout and Vt Options for Low Noise Amplifier Design in 65-nm CMOS [RFIC'12]
- Example 2
  - Differential Stacked Spiral Inductor and Transistor Layout Designs for Broadband High-Speed Circuits [RFIT'14]
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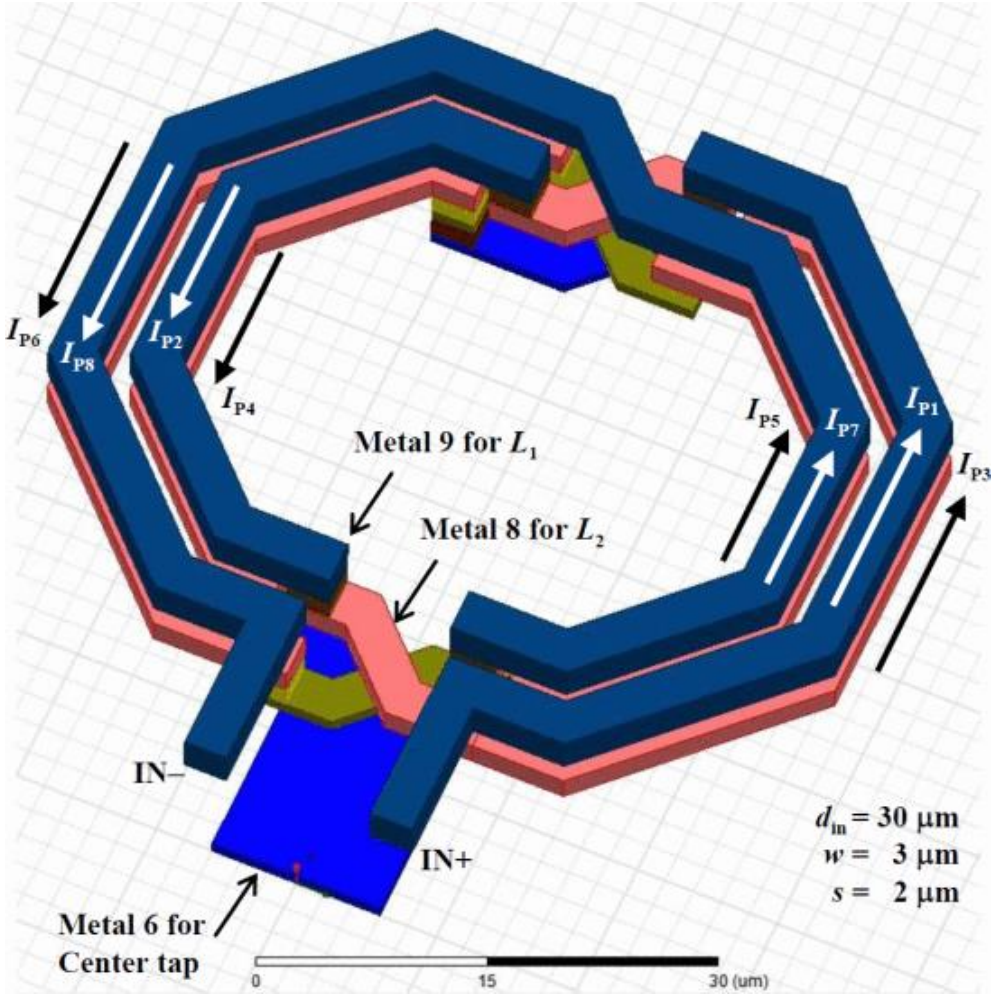
Differential Stacked Spiral Inductor and Transistor Layout Designs for Broadband High-Speed Circuits

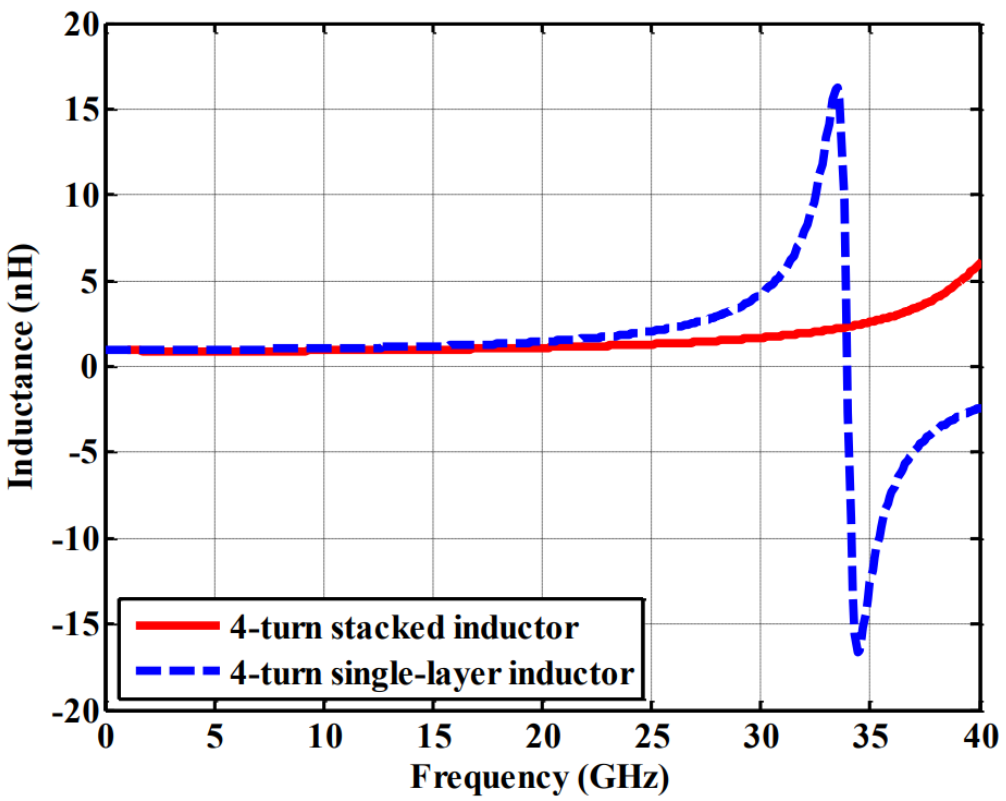
Differential Stacked Spiral Inductor

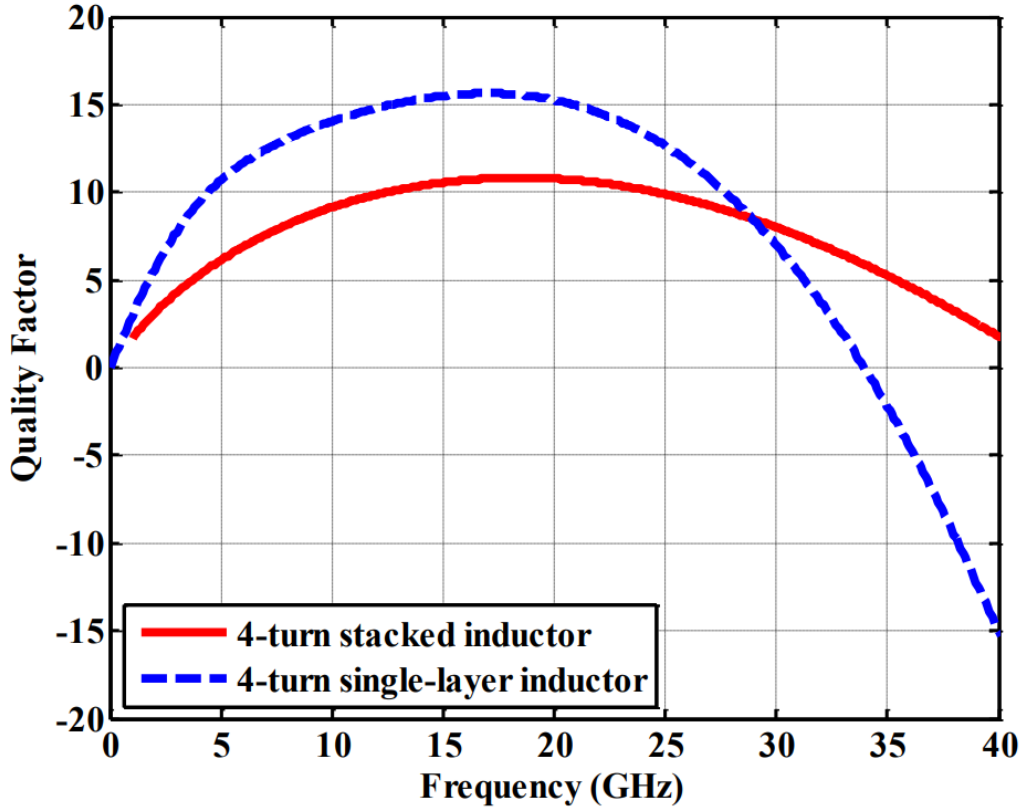
- Inductor provided by the PDK usually adopts the top thick metal to achieve a high Q with inevitably large area
- For broadband high-speed applications with shunt peaking, high Q is not an important design parameter anymore



- The presented DSSI which sacrifices Q but obtains much higher inductance density

Simulated Results



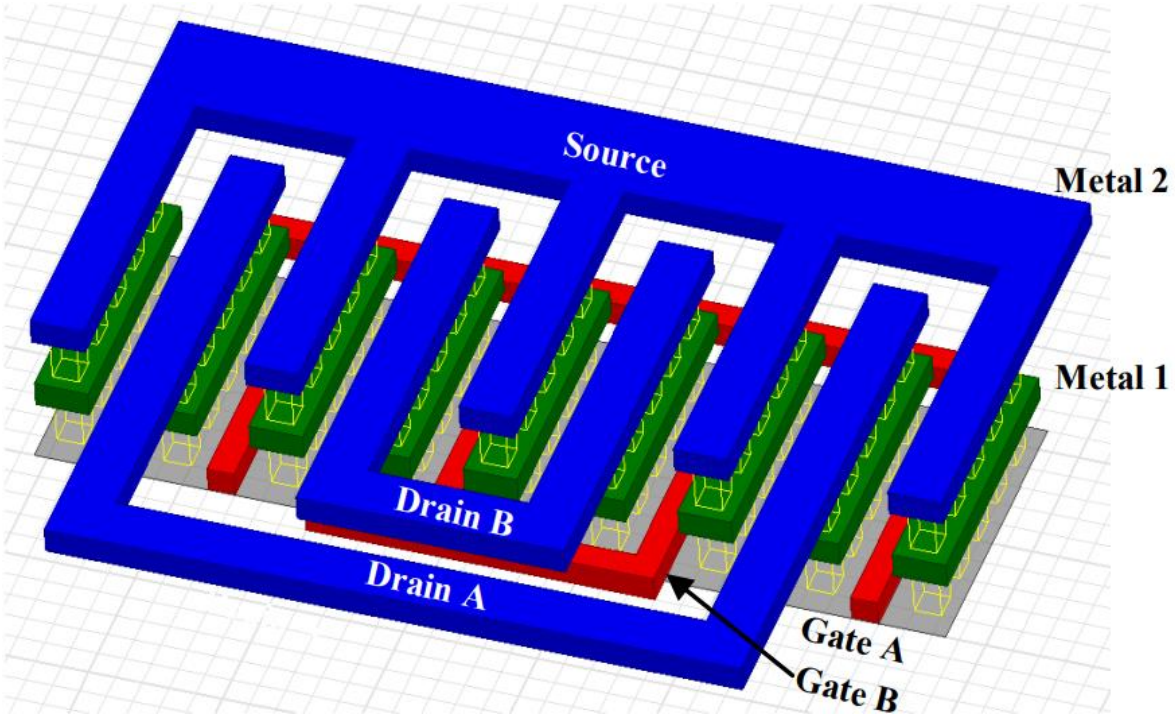


- Simulated results of 4-turn single-layer PDK inductor and 4-turn customized DSSI: inductance (left), and quality factor (right)

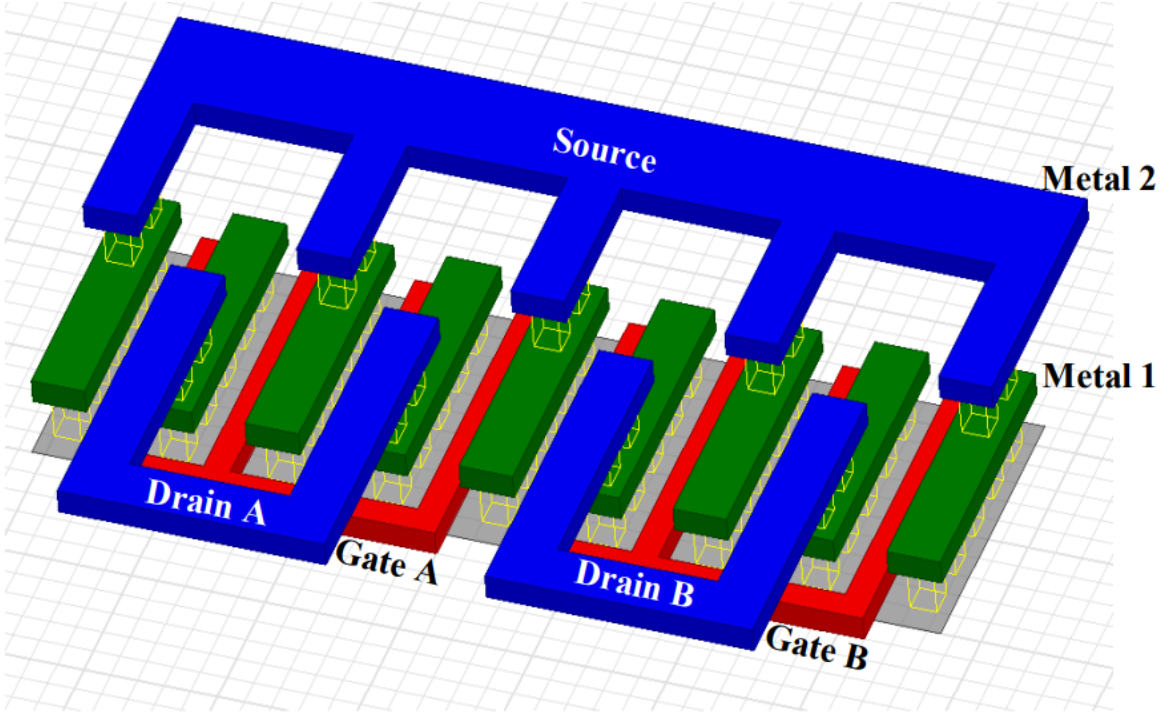
HFSS Comparison

	Single-layer inductor	Stacked inductor
Low-frequency inductance (nH)	1.0	1.0
Area (μm^2)	110 x 116	60 x 66
Self-resonance frequency (GHz)	34.7	41.5
Peaking quality factor	16	11
Number of turns	4	4
Inductance density ($pH/\mu m^2$)	0.078	0.25

Transistor Layout



(a)



(b)

- 3-D views of differential pairs: (a) Conventional ‘ABBA’ inter-digitated layout, and (b) the proposed ‘AABB’ half-inter-digitated layout

Comparison of Two Layout Style

Layout style (24 μm/60 nm)	'ABBA' inter-digitated	'AABB' half-inter-digitated	Improvement Factor
Coupled parasitic caps between inputs	5.0 fF	65.1 aF	X 77
Coupled parasitic caps between outputs	3.2 fF	133.8 aF	X 24
Total parasitic caps at one output node	10.7 fF	5.5 fF	X 2
Total parasitic caps at one input node	15.3 fF	7.7 fF	X 2

Conclusions

- The performance impact of the compact differential stacked spiral inductor (DSSI) and different transistor layouts are evaluated based on the simulation and measurement results
- For high-speed broadband circuits design, the compact DSSI has much larger inductance density and much smaller parasitic capacitance from the interconnections than the inductor provided in PDK

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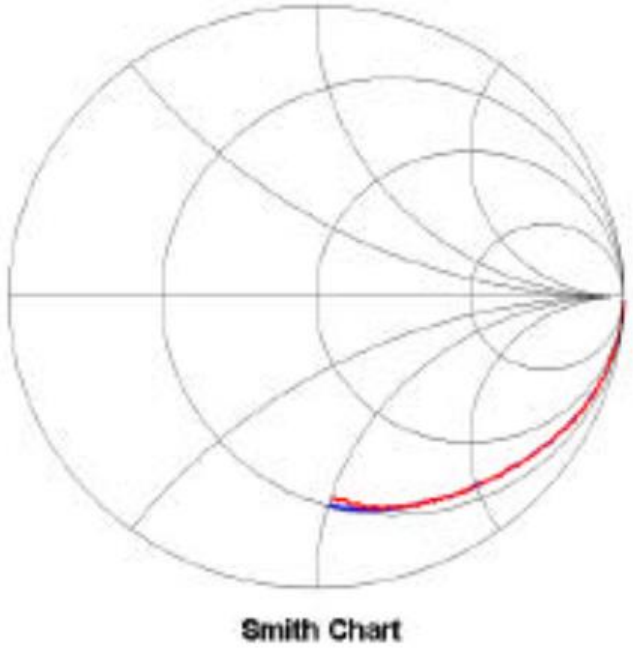
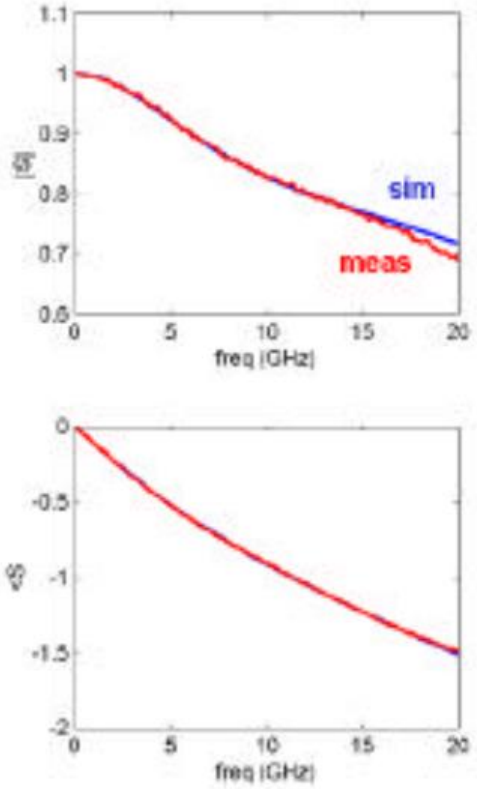
Package Design for a 10 Gigabit Ethernet Transceiver

Step 1: Behavior of A Bond Pad

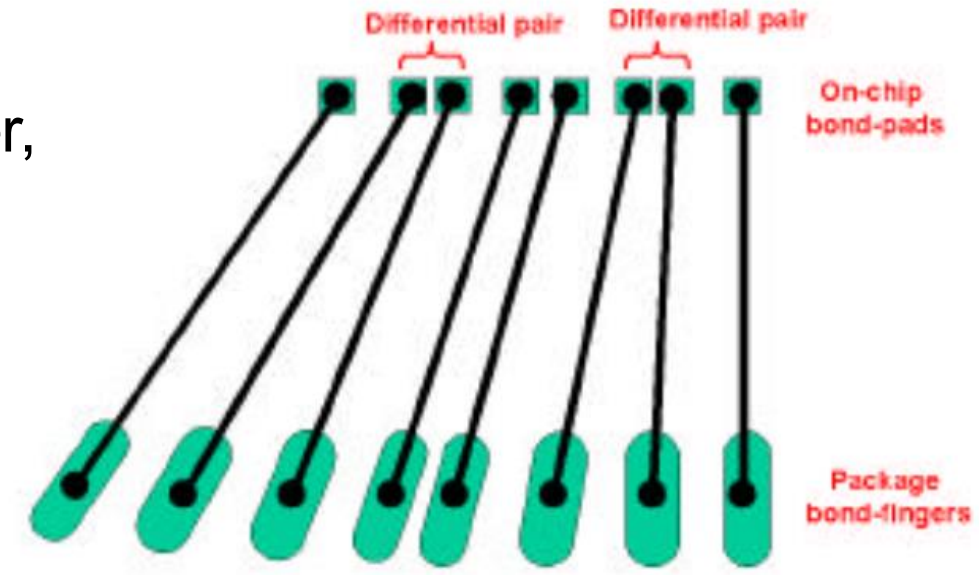
- Comparison between measurement and simulation indicates that:
  - A **simple R-C network** is sufficient to describe the bond-pad parasitic from DC up to 20 GHz





Step 2: Package Design

- What's the package design?
  - A cavity up, wire-bond plastic BGA is desired, for **low cost, high volume technology, and easy probe** access
- Major limitation:
  - Bond-wire inductance in combination with the on-chip capacitance
- Design Choice:
  - Diff-pair are angled towards each other, to **increase differential coupling**



Step 3: Package Stack-up and Diff Pair Design

- The figure shows the stack up
- What needs to be optimized?
  - Trace thickness
  - Solder mask
  - Plastic modelling compound
  - Trapezoidal cross section
- Techniques:
  - Use wide trace width to avoid width variation
  - Commonly used width and space: **W-150um-S-130um**, or **W-100um-S-75um** for **100-Ohm** matching

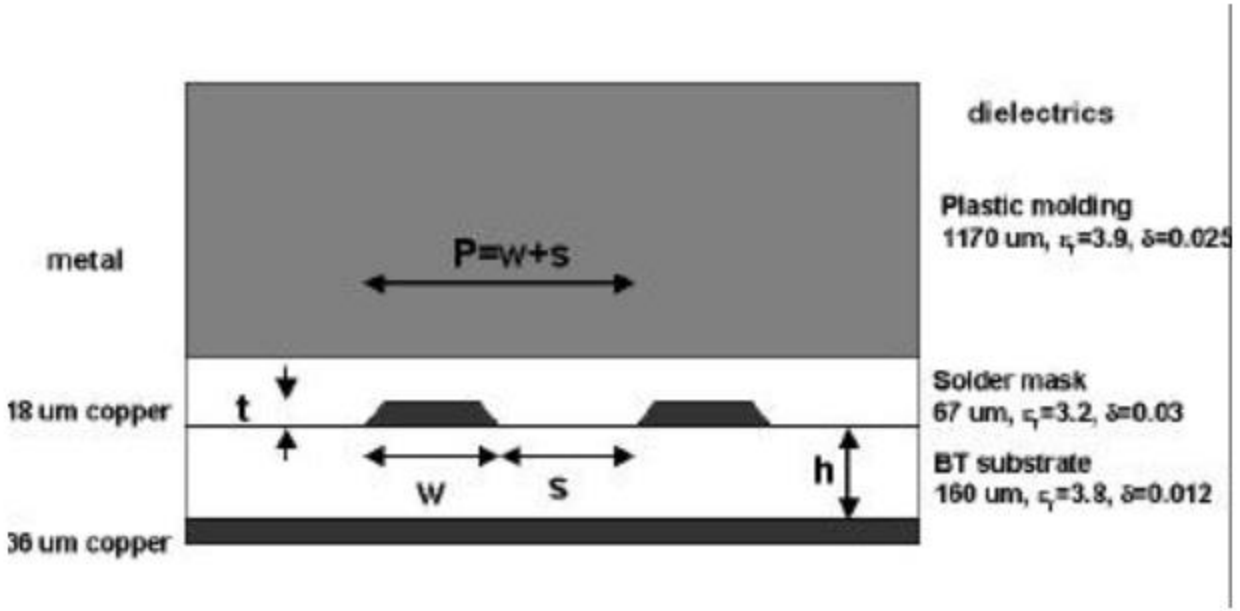
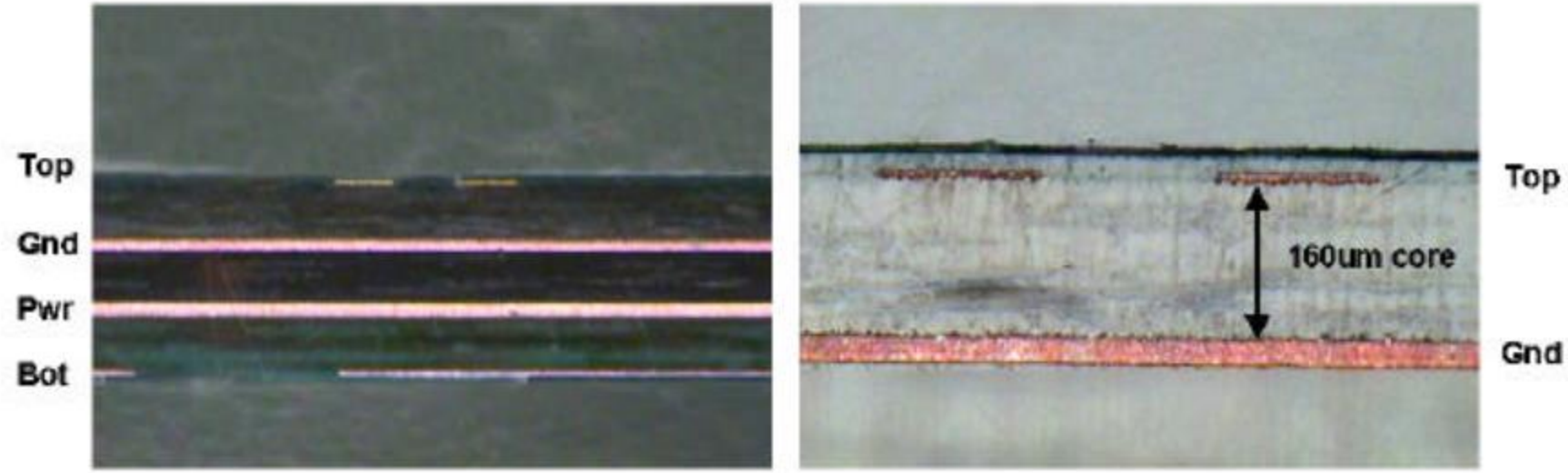


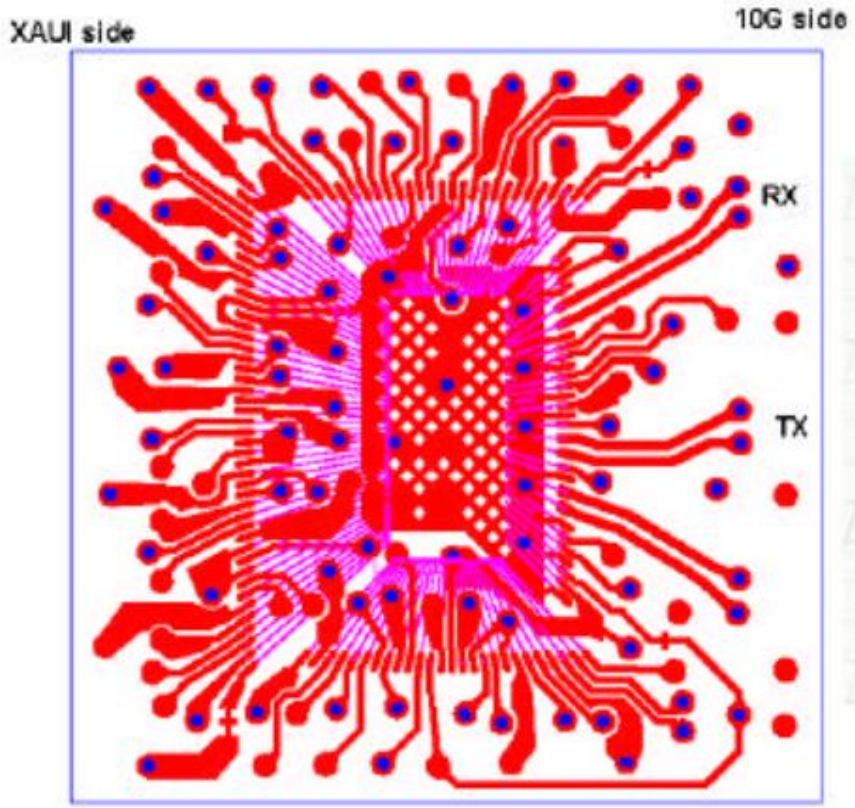
Figure 3. Partial package stack-up and differential pair cross section

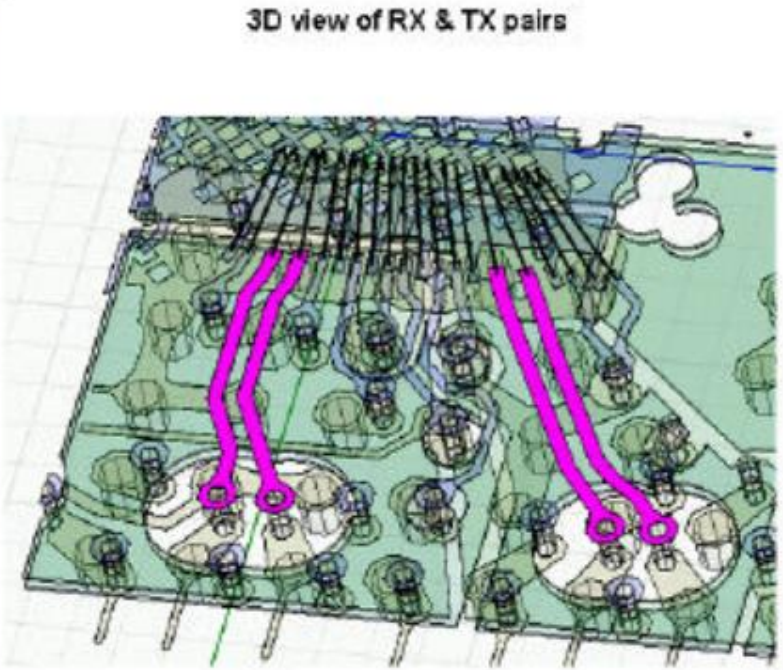
Package Cross Section



- Inner layers for Gnd and Pwr are thick, for better heat sink
- The pre-laminated side of the metal (facing the dielectric core) can be rougher, and increase the signal loss.
  - Not a big issues for 10 Gb/s level

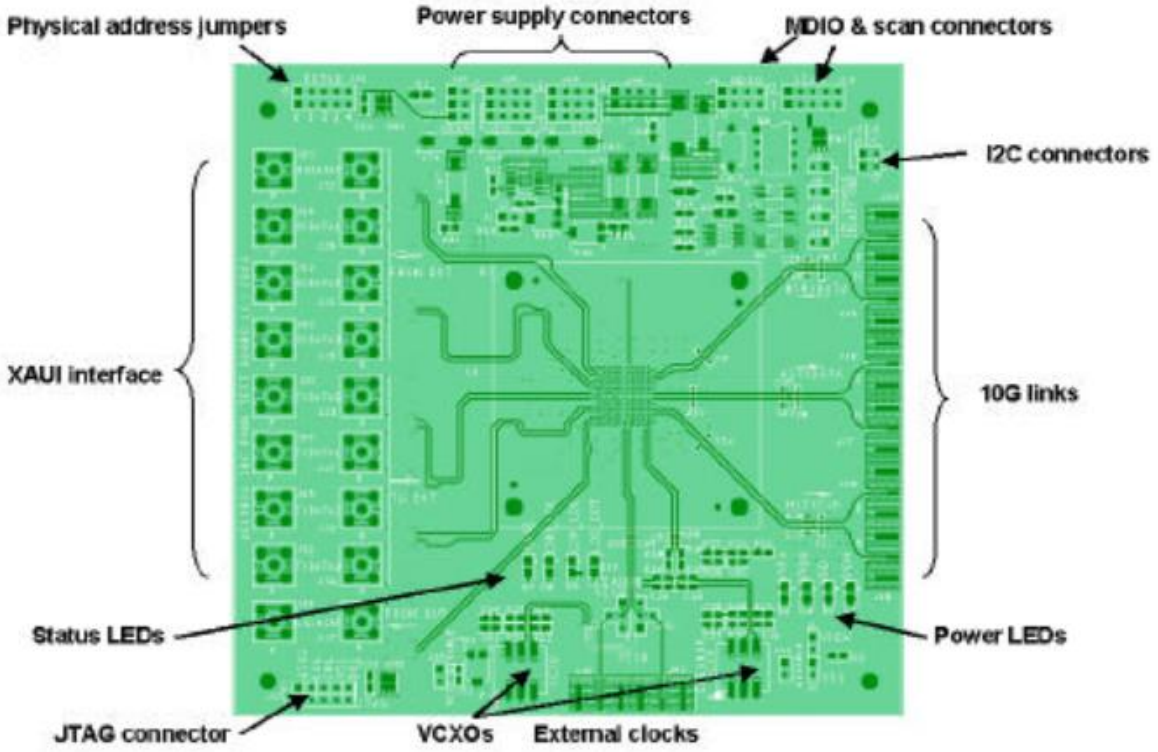
3D View of the Overall Package



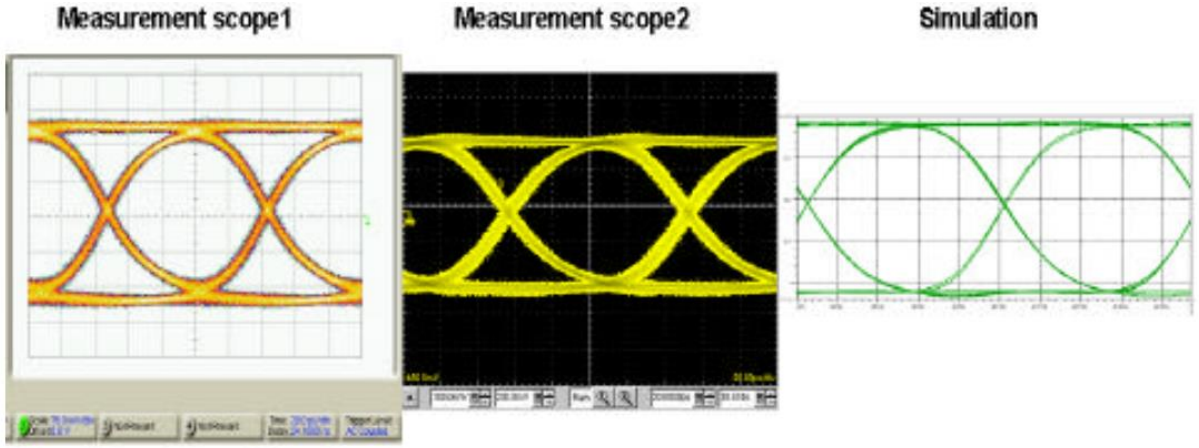


- The via design is critical, needs to be verified together with the soldering balls connected to it, using 2.4-D planar EM wave solver, and 3-D EM wave solver

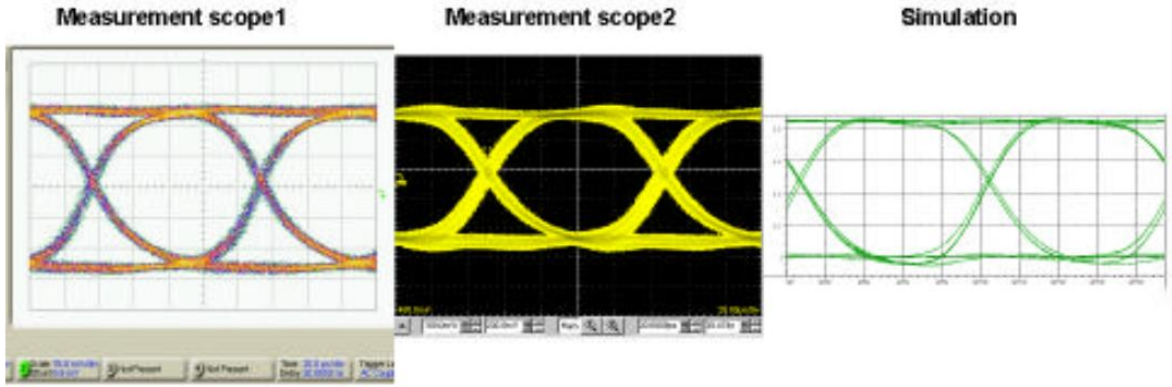
Test board and Verification



Top view of the test board



10 Gbps eyes in slow edge mode



10 Gbps eyes in fast edge mode

Conclusion

- The design of the package and test environment for a 10 Gigabit Ethernet to XAUI transceiver was discussed with an emphasis on the 10G links
- Several comparisons between simulated and measured performance were shown with good agreement.
- These off-chip interconnects are as crucial as on-chip circuits for achieving a high performance, low-cost device at 10Gb/s.

PIT Reference (OWL)

- Q. Pan, T. -J. Yeh, C. Jou, F. -L. Hsueh, H. Luong and C. P. Yue, "A performance study of layout and Vt options for low noise amplifier design in 65-nm CMOS," 2012 IEEE Radio Frequency Integrated Circuits Symposium, Montreal, QC, Canada, 2012, pp. 535-538.
- Q. Pan, L. Sun and C. P. Yue, "Differential stacked spiral inductor and transistor layout designs for broadband high-speed circuits," 2014 IEEE International Symposium on Radio-Frequency Integration Technology, Hefei, China, 2014, pp. 1-4.
- Dr. PAN Quan's Thesis: Optoelectronic Receivers in Standard CMOS for Short-Range Optical Communications.
- H. J. Liaw, C. Patrick Yue et al. "Package and Test Environment Design for a 10 Gigabit Ethernet Transceiver." DesignCon. 2004.