香港科技大學
THE HONG KONG UNIVERSITY OF SCIENCE AND TECHNOLOGY

Hi5Semi

High5 Semiconductor (HK) Limited
高武半導體(香港)有限公司

HQ OWL

光、毫米波通信集成电路与初创企业

Prof. C. Patrick Yue 俞捷, 香港科技大学

首届“湘智兴湘”大会 — 湖南 长沙

2025-09-19

Integrated Circuit Design Center, Optical Wireless Lab
Department of Electronic and Computer Engineering
The Hong Kong University of Science and Technology (HKUST)

Hi5 Semiconductor
High5 Semiconductor (Hong Kong) Limited
高武半導體(香港)有限公司

內容綱要

- **團隊成員與技術協同**
- **市場機遇**
- **技術路綫與目標市場**
- **產品描述與原型**
- **商務拓展**

CMOS芯粒+GaN芯粒領域的綜合技術專長

Optical Wireless Lab

Prof. C. Patrick Yue

- Co-founder of Atheros, IPO in 2004
- Developed First-gen Wifi products
- Fellow, IEEE & Optica
- HKUST IC Design Center Director
- Expert in CMOS optical and wireless communication IC

- Deep partnership GaN foundry Dynax
- Process development and device optimization
- Our CGTA Prof. Man Hoi Wong is an expert in wide-bandgap semiconductors

dynax 能讯

CMOS + GaN = High-End Eco-Semiconductor Chiplets

High-Energy Efficiency

Faraconix 升新科技

Dr. Chi Law

Heterogenous integrated system-in-package (HISiP)

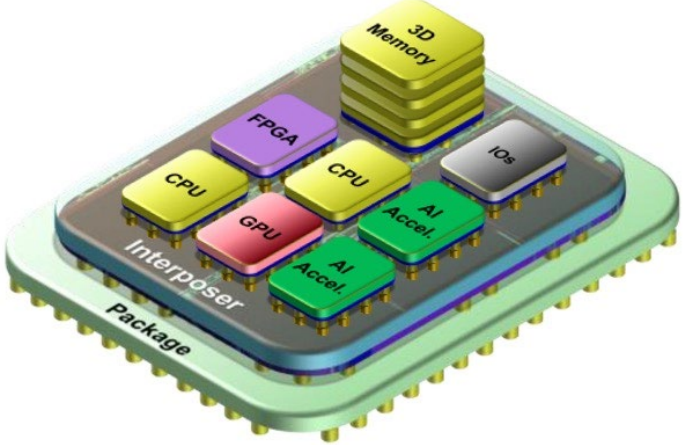
- Partnering with Faraconix on RF module integration
- Jointly tackling heat and high-freq loss issues

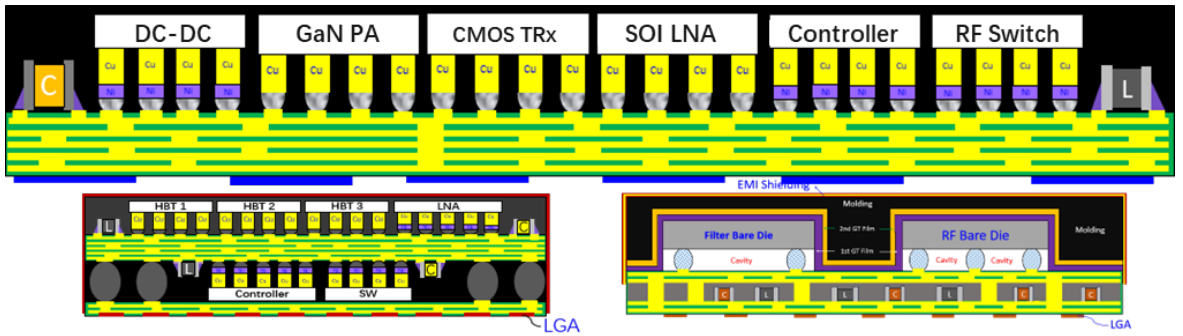
"High-SPLIQ"

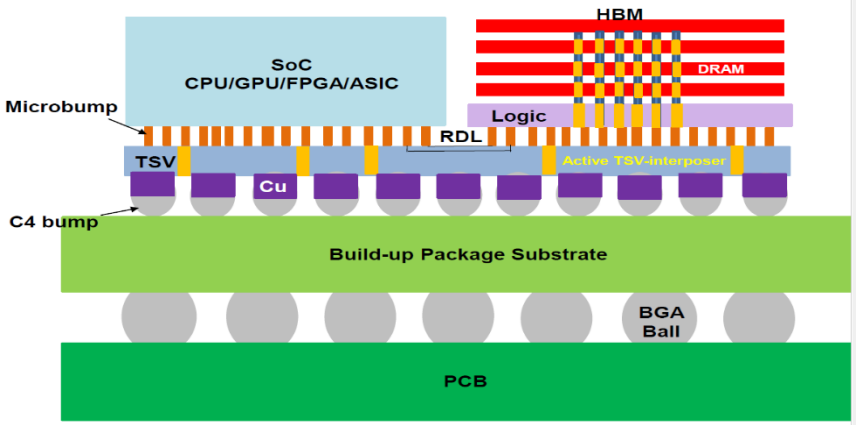
High-Speed
High-Power Efficiency
High-Linearity
High-Integration
High-Q-Factor Passives

High5 Semi 的解決方案 / 深度技術 / IP

透過異質集成芯粒封裝技術 Heterogeneous Integration of Chiplets
同時解決無線與光通信技術瓶頸，並滿足降低成本的產業需求







- **By integrating CMOS + GaN we aim to deliver best-in-class energy-efficient solutions for the two highest growth enterprise communication market in the next decade:**
  - **High-speed optical communication for Data Center Interconnection (DCI)**
  - **Satellite communication for 6G networks**

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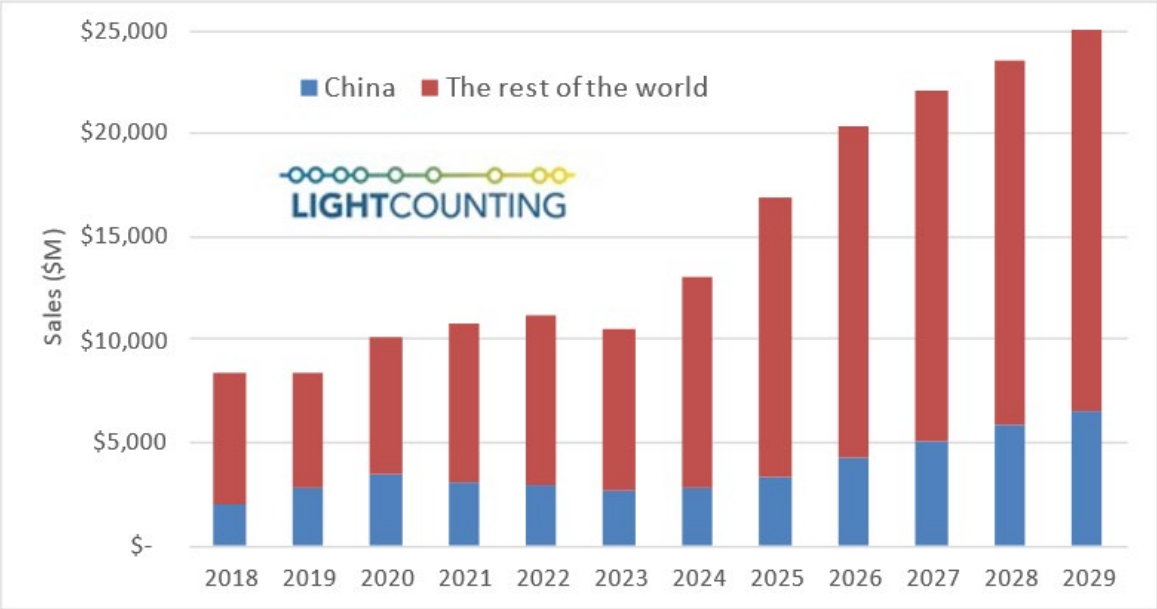
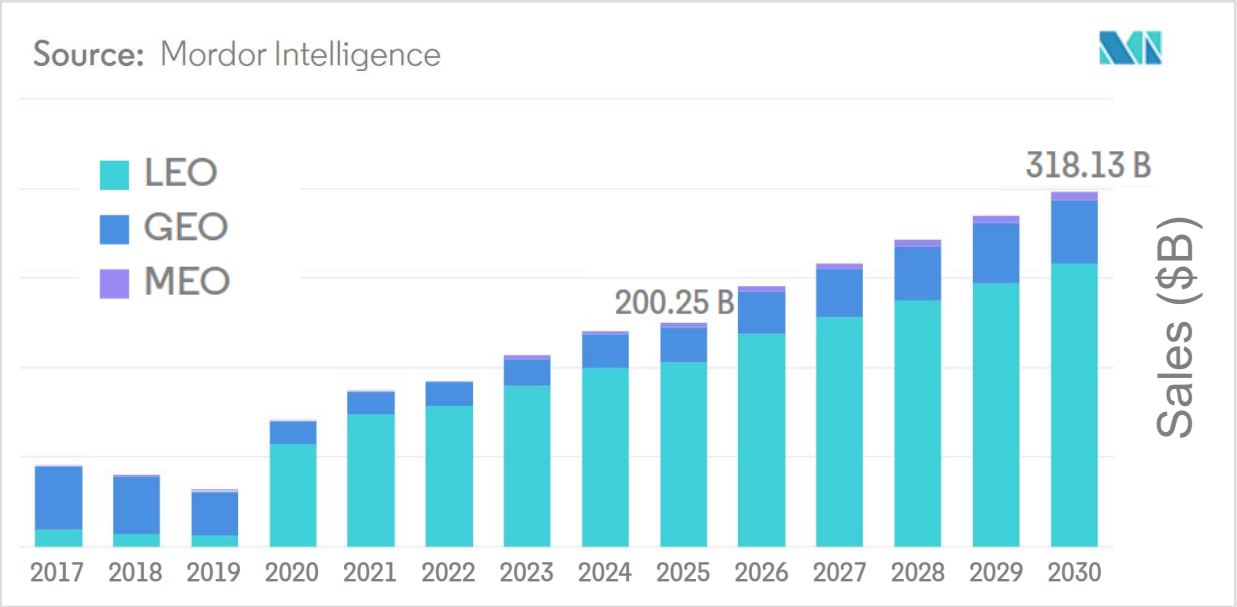
市場機遇 & 總潛在市場 (TAM) 預測

光通信市場規模：
中國與全球其他地區 (單位：USD Million)



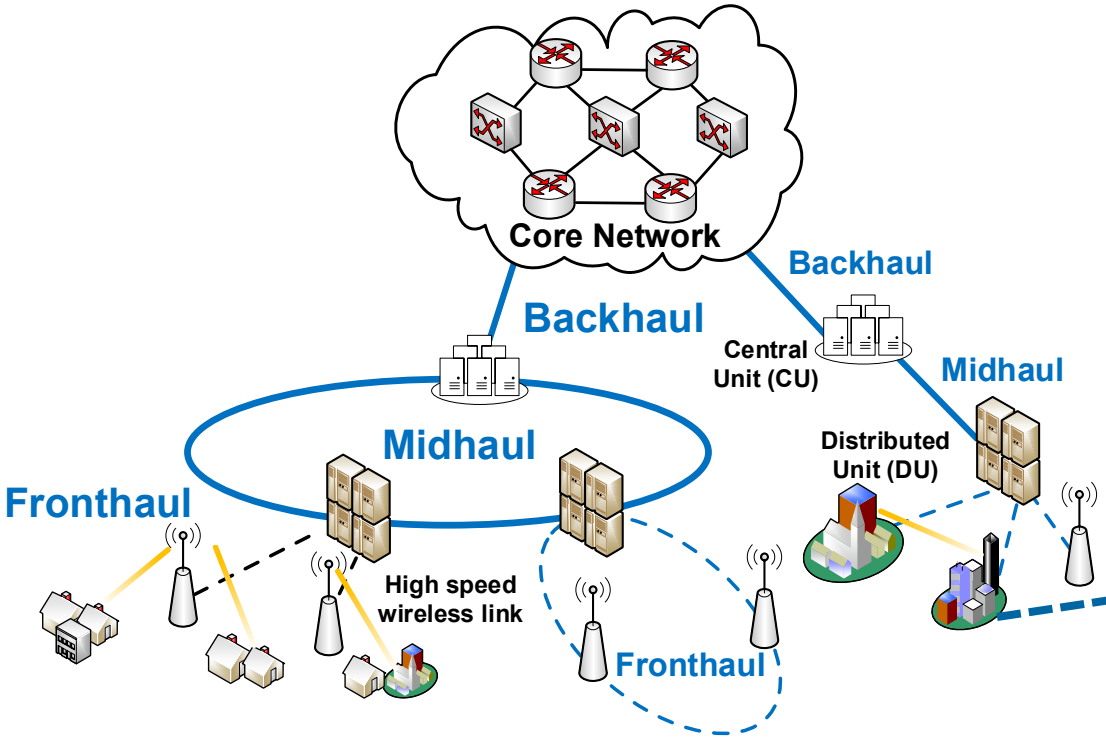
全球衛星通信市場規模：
按軌道類型劃分 (單位：USD Billion)

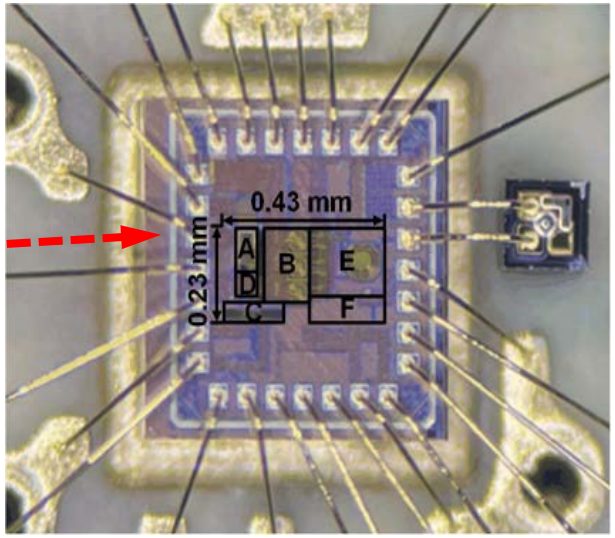


- **For the first stage, optical communication products for DCI, the total addressable market in next 5 years is 40 billion USD**
- **For the second stage, wireless communication products for LEO satellite communication, the total addressable market in next 5 years is 26 billion USD**

數據中心光通信模塊市場機遇

■ 數據中心互連光模塊



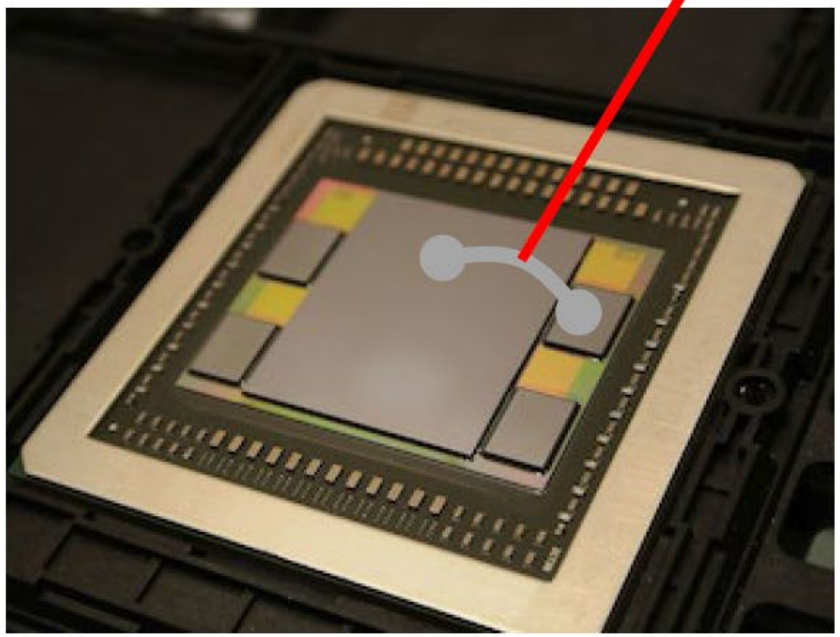


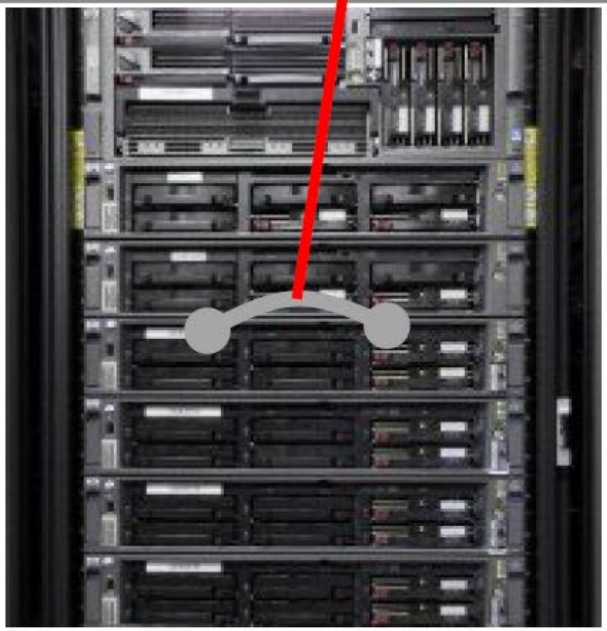
新一代數據中心互連需要高效率、高速的光收發模塊

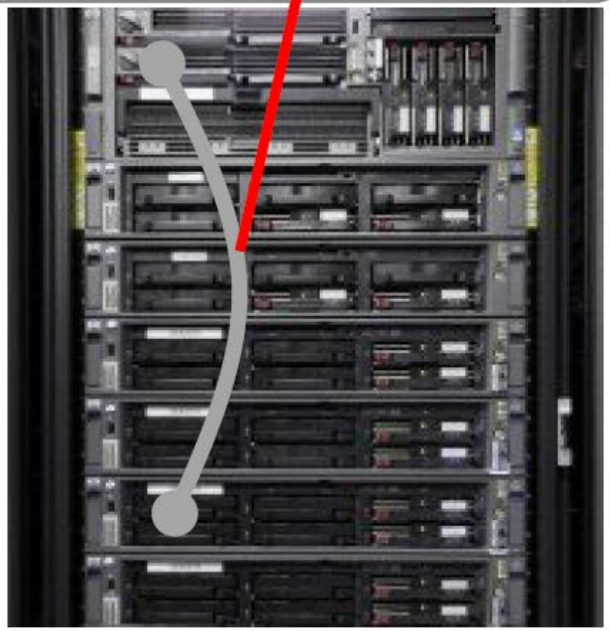
數據中心光通信模塊市場機遇

- **Interconnect Power and Density Bottleneck**

Best-in-class interconnects	Intra-package: > 0.5pJ/bit	Intra-machine: > 2pJ/bit	Intra-rack: > 5pJ/bit



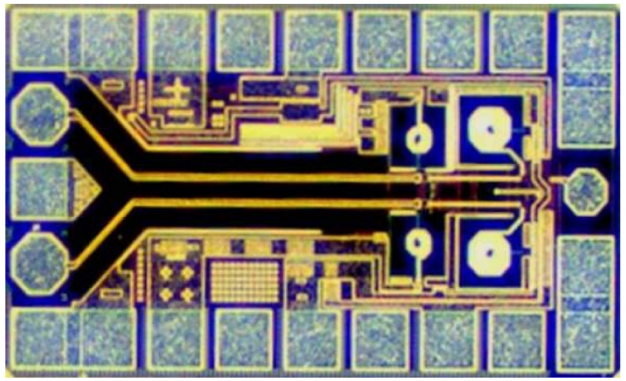




- **Internal chips are slow, but >50Tb interface to ICs overwhelm packaging density**
- **200Gb/s SERDES take area, yield, and power, all with limited reach**

數據中心光通信模塊產品挑戰

■ AIGC數據中心互連遇到的帶寬瓶頸



Due to the data exchange and transmission requirements brought by AIGC, the market for high-speed optical modules have seen exponential growth

- Current optical communication products (InP, SiGe, GaAs) **cannot** meet high-energy efficient bandwidth and cost requirements
- Low-frequency solutions fail for modern data center interconnects

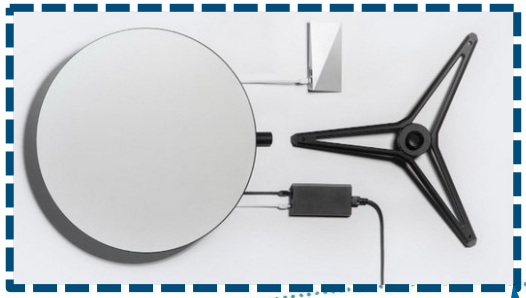
- Designing heterogeneous optical chiplets to boost bandwidth and data rates
- Targeting 4x bandwidth growth from 200/400G to 1.6T optical modules

Refused to be choked! **拒绝被卡脖子!**

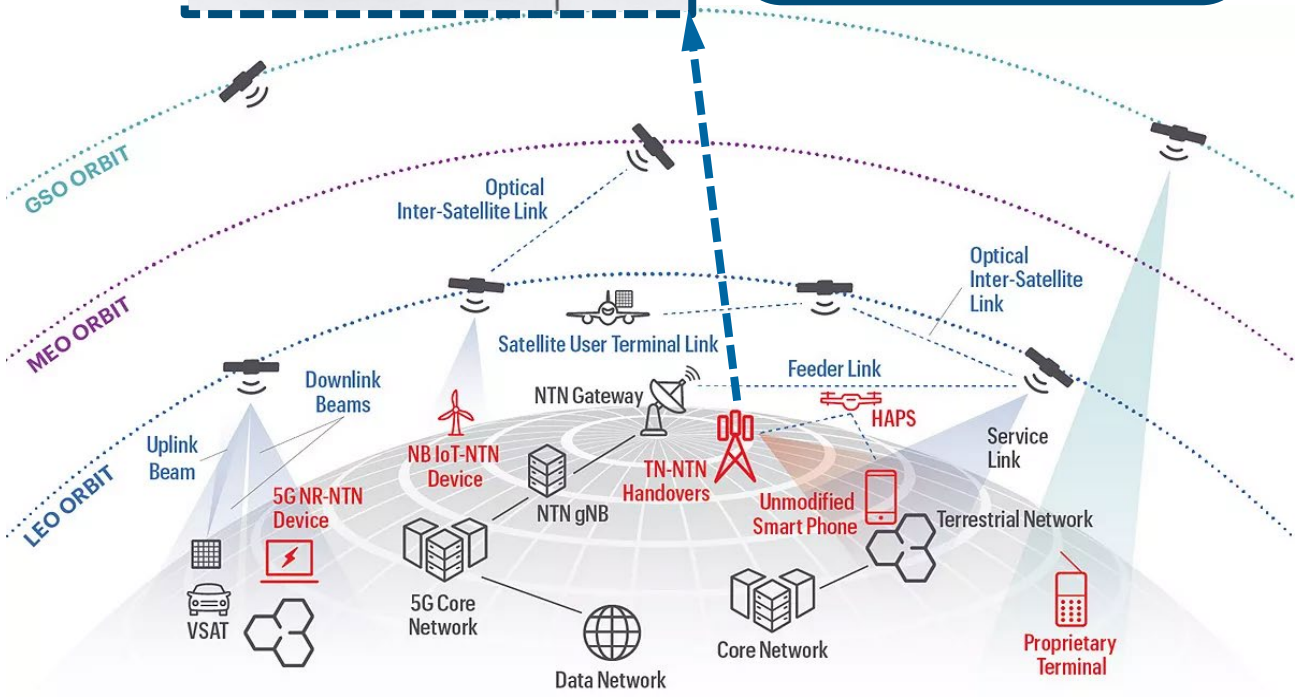
6G衛星通信市場機遇

6G及未來衛星通信的全球競賽：
有限的頻譜資源與傳輸容量

- **LEO capacity limit: < 100K satellites**
- **China's opportunity**: Must develop a **Starlink-level solution** to ensure global competitiveness in satellite internet
- **ITU rules**: **"First come, first served"**, escalating the race

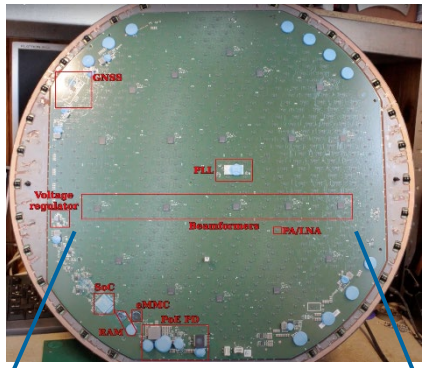


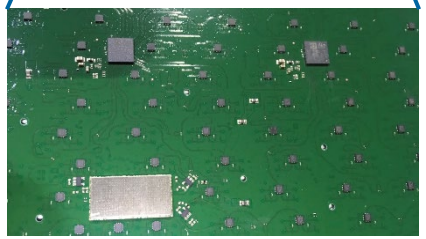
5 million customers in 2025 for revenue US$3B

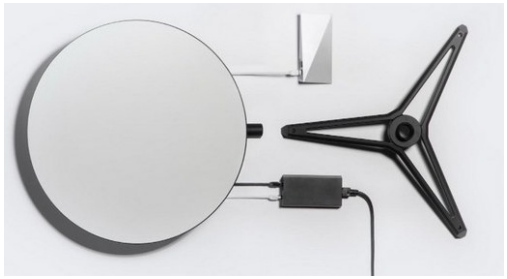


6G衛星通信產品挑戰

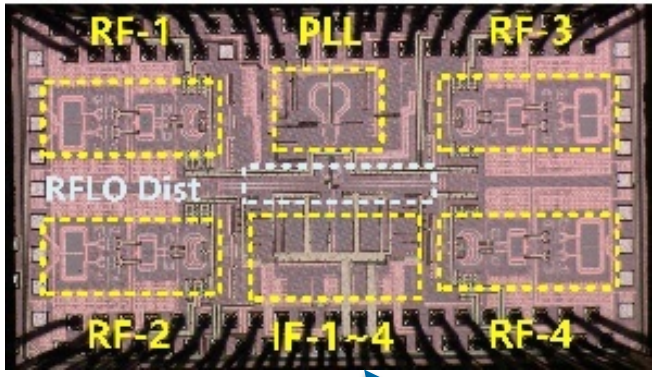
當前市場領導者：StarLink Satcom



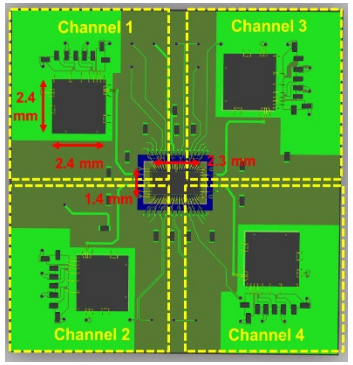


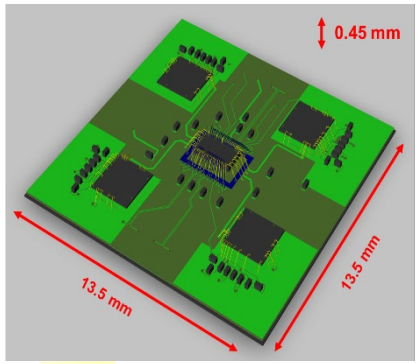


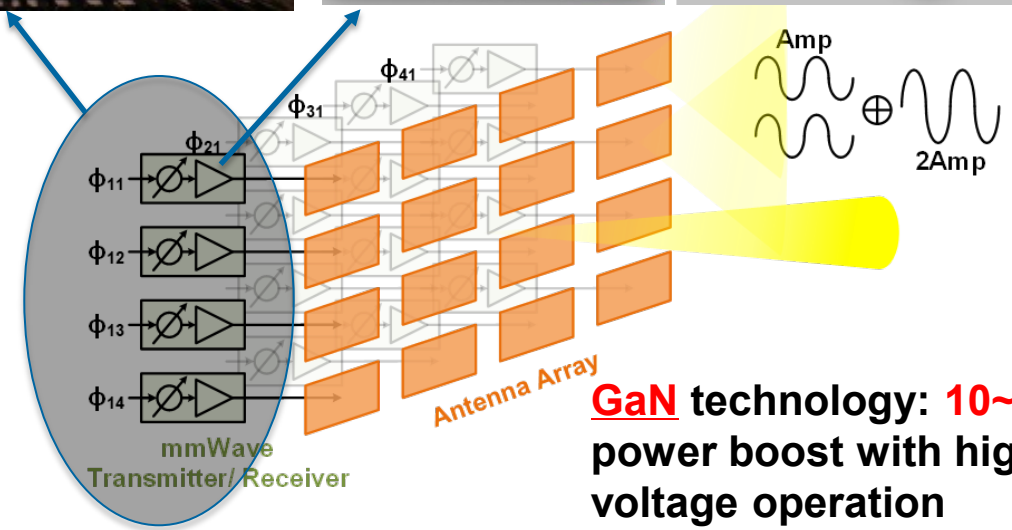
- Mechanical satellite tracking
- Electrical and digital beamforming
- Combining individual PAs and LNAs for gain enhancement



CMOS phased array circuits: 10~20x power enhancement







GaN technology: 10~50x power boost with high-voltage operation

- **Long-distance inter-satellite communication requires high-end eco-semiconductors**
  - **High-integration CMOS circuit array**
  - **High-energy-efficiency GaN power amplifiers**
  - **Heterogeneous chiplet packaging technology**

Overall 1,000x Power Increase!
Unprecedent Performance in Integration/Power/Efficiency/Cost!

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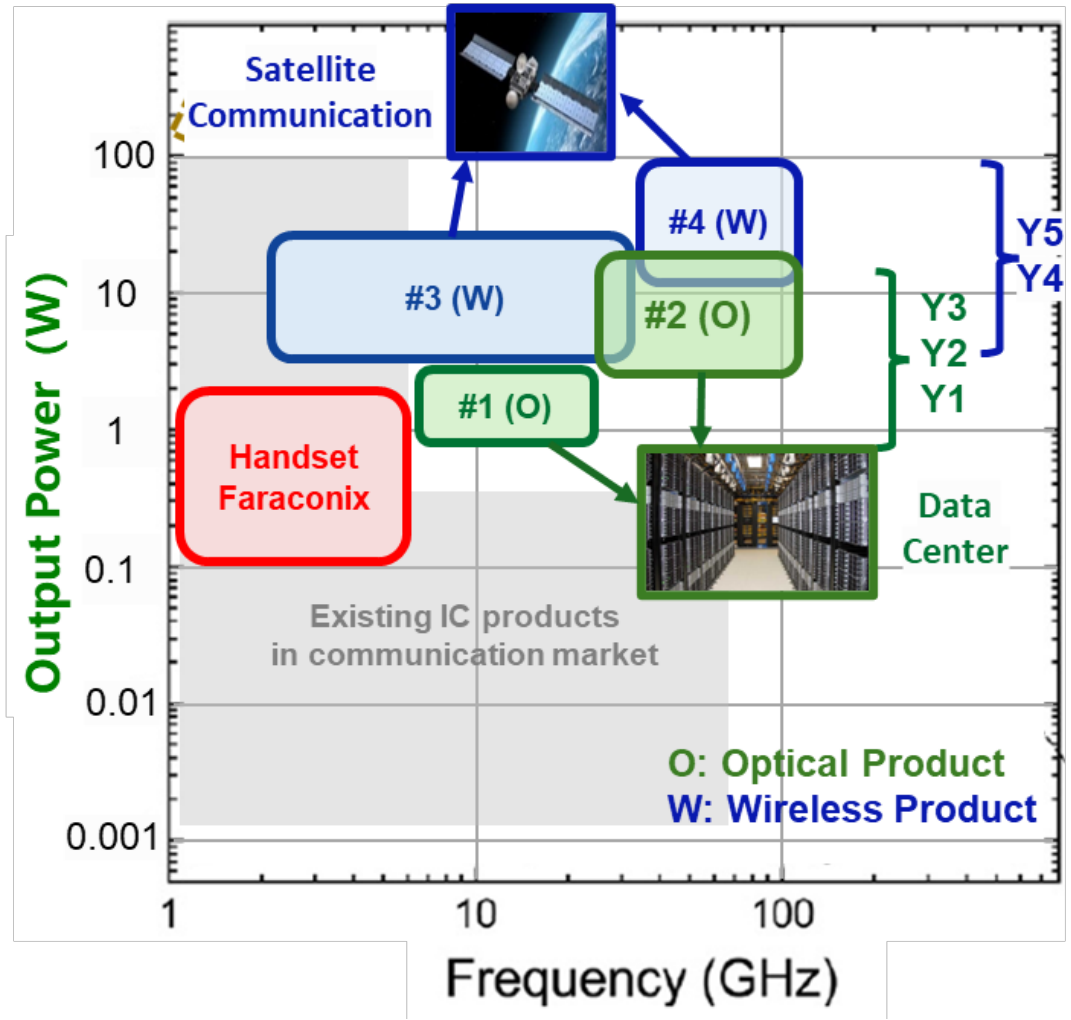
High5 CMOS+GaN 無線與光通信技術路線圖概覽



Stage	Key Deliverables
RAISe+ Stage 1 R&D focusing on optical chiplet module (Year 1~3, 2026~28)	Performance analysis of (CMOS+GaN) materials
	Initial design and prototype of (CMOS+GaN) HiSiP for data center interconnection
	Prototype for short-reach 1-2 Tb/s links
RAISe+ Stage 2 Commercialization (Year 4~5, 2029~30)	Mass production of optical communication products
	Design (CMOS+GaN) chiplets for 6G satellite communication
	Compliance with 3GPP Release 18 and Chinese satellite standards

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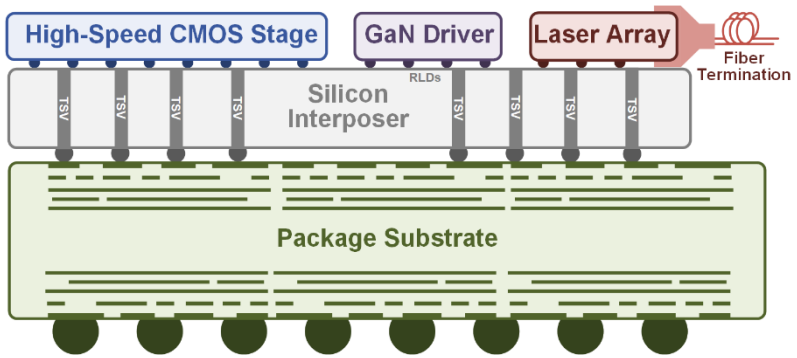
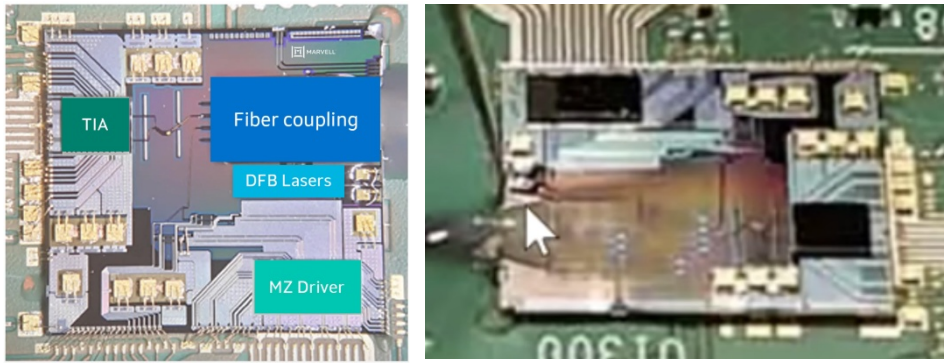
產品描述: CMOS + GaN Chiplet HiSiP

■ 數據中心互聯的光通信異質集成芯粒

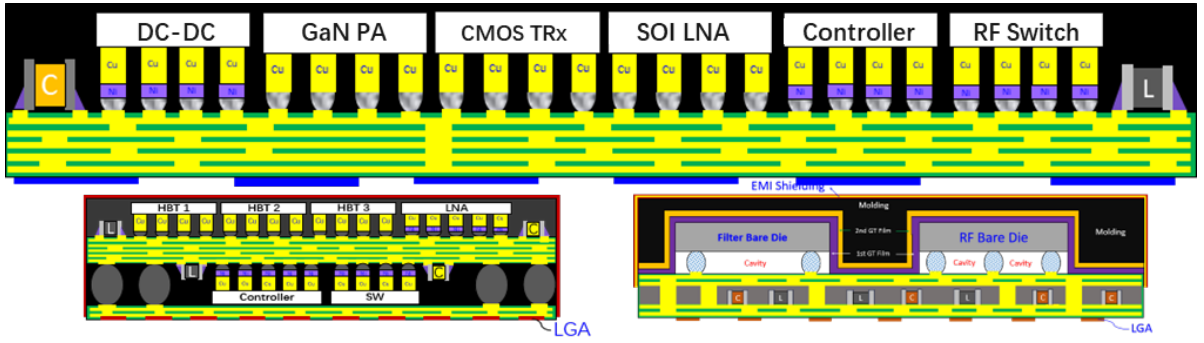


Cross section of the optical chiplet in package

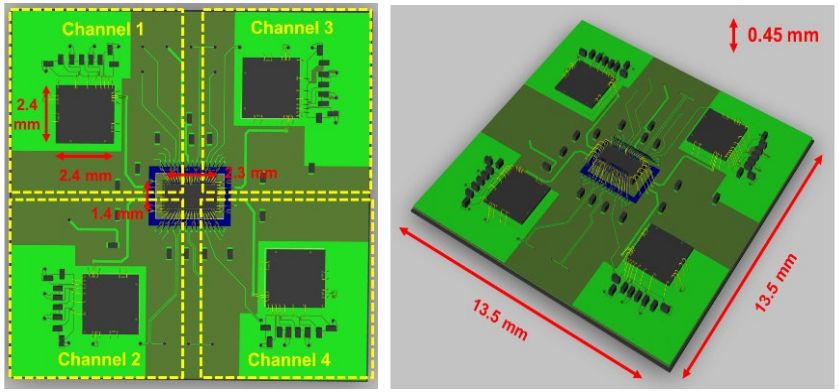


Integrated optical module (source: Marvell)

■ 衛星通信的無線異質集成芯粒

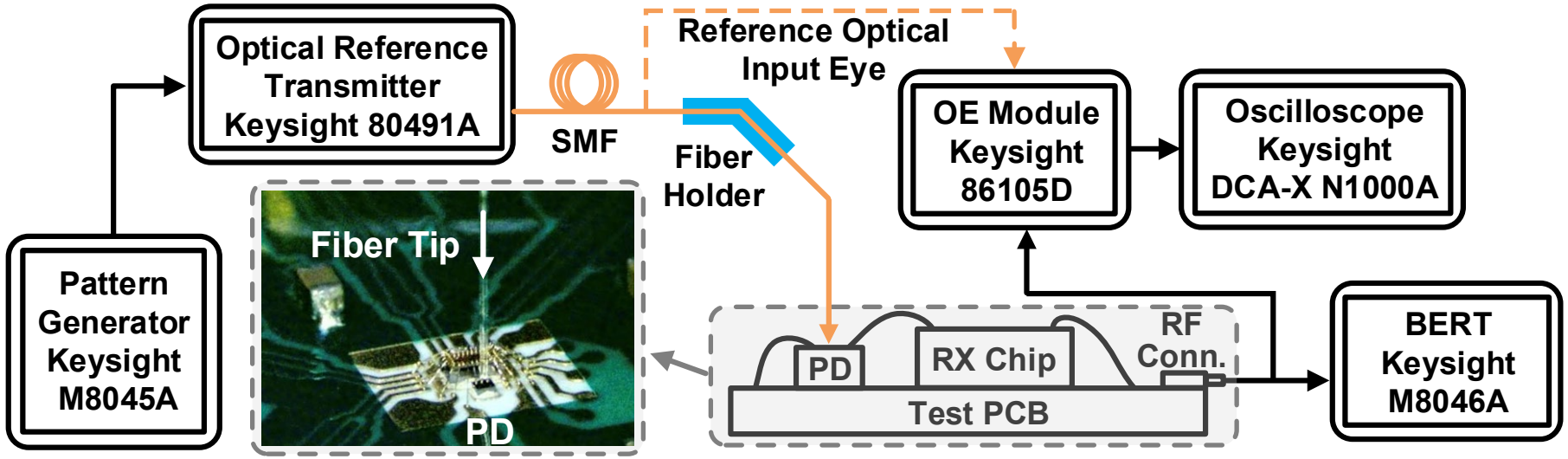


Cross section of the wireless chiplet in a package

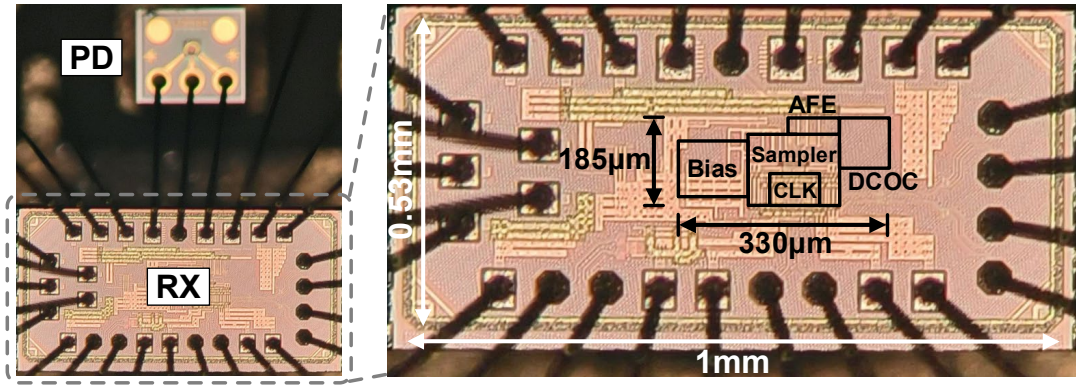


3D Layout of the wireless chiplet in a package

CMOS 產品原型：48-Gb/s PAM-4 Optical Receiver

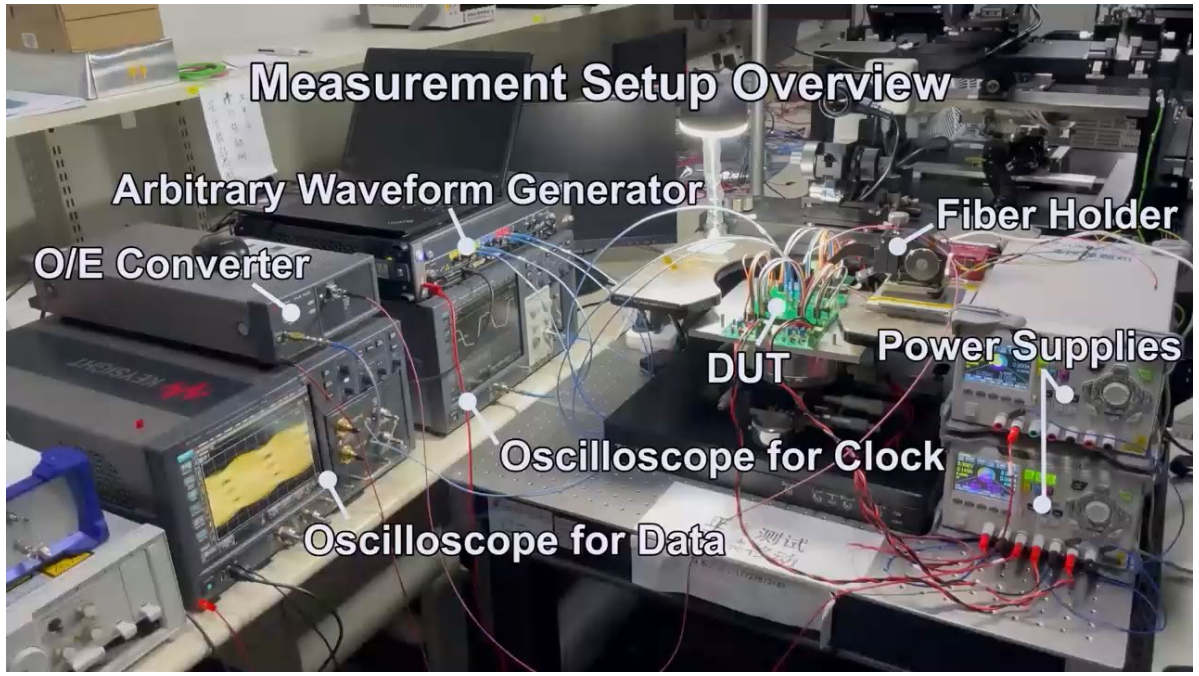


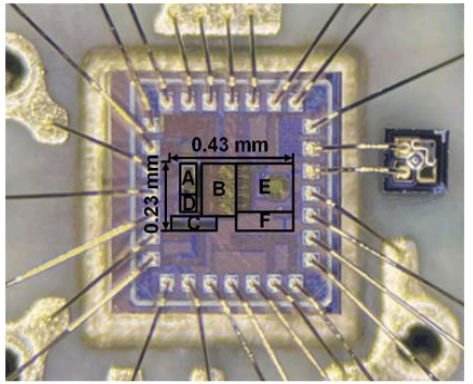
- Fabricated in 28-nm bulk CMOS
- 1308-nm light source is coupled to PD through a single-mode fiber
- Optical power level is adjusted by an internal optical attenuator
- Deserialized MSB and LSB are sent to off-chip BER testing

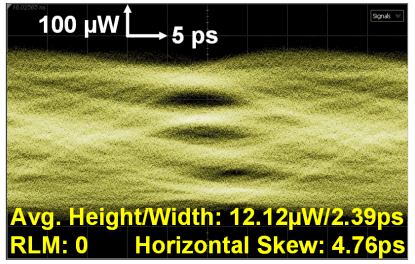


C. Zhang, C.P. Yue et al., VLSI 2024, Honolulu, HI, USA.

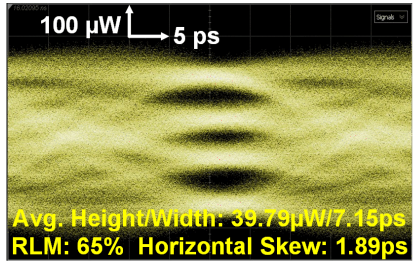
CMOS 產品原型：56-Gb/s PAM-4 Optical Transmitter



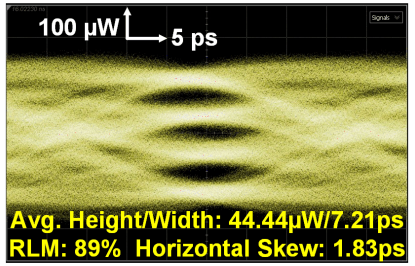




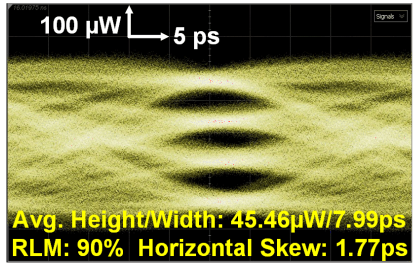
(a) EQ OFF, Equal Slice Gain



(b) Equal Slice EQ and Slice Gain



(c) Equal Slice EQ, Piecewise Tuned Slice Gain



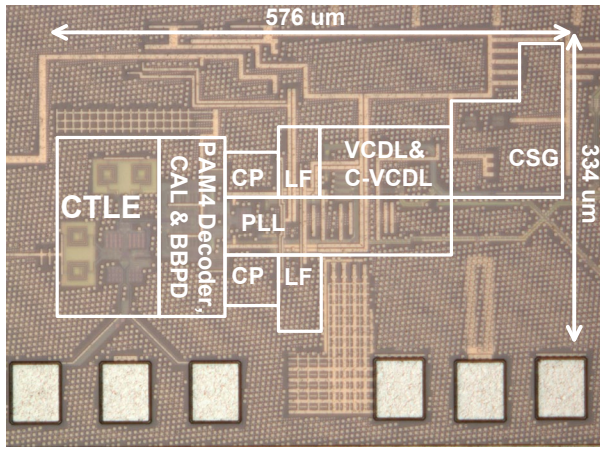
(d) Piecewise Tunned Slice EQ and Slice Gain

- **Data path: thermometer-coded architecture**
- **Clock path: Wideband PLL and cascading VCDL**
- **Optical part: Wire-bonded anode-driven VCSEL**

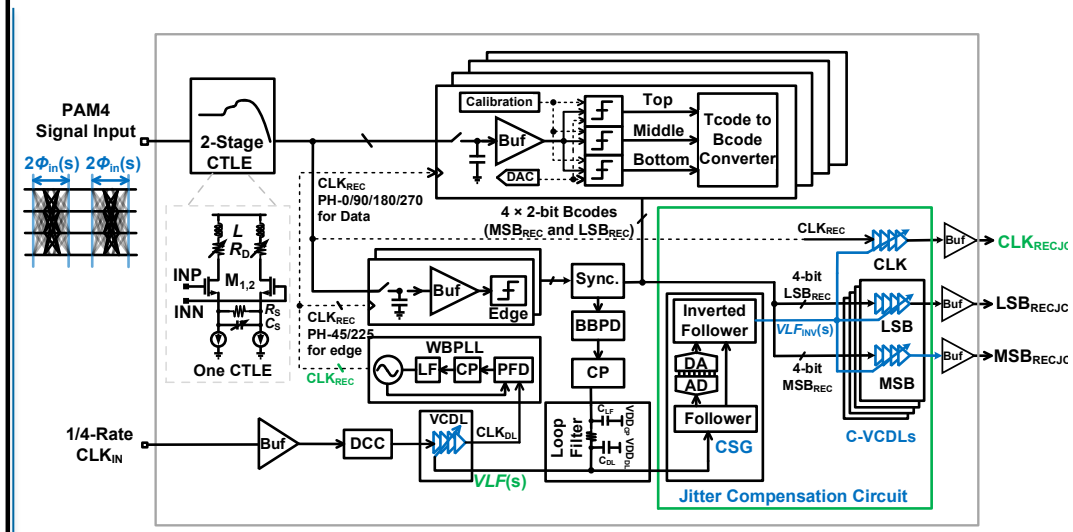
F. Chen and **C. P. Yue**, ESSCIRC 2023, Lisbon, Portugal.

CMOS 產品原型：60-Gb/s CDR with Jitter Compensation

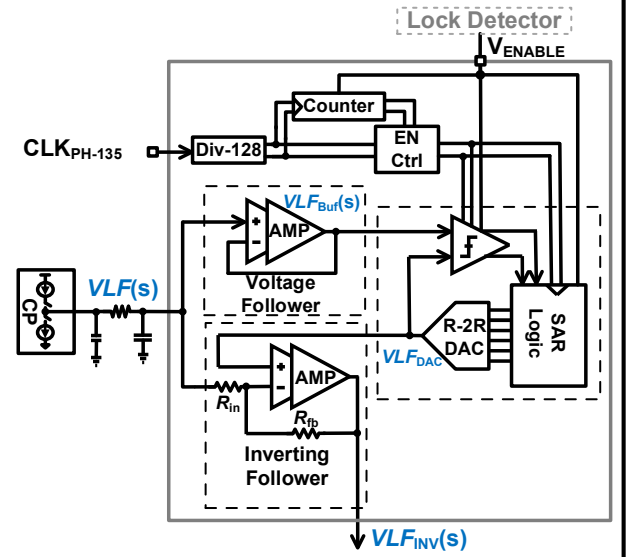
- 60-Gbps PAM-4 Receiver with Jitter Compensation CDR



Prototyped in 40nm CMOS
Core area: 0.2 mm^2



30-60-Gb/s PAM-4 Receiver with Jitter Compensation CDR System Diagram



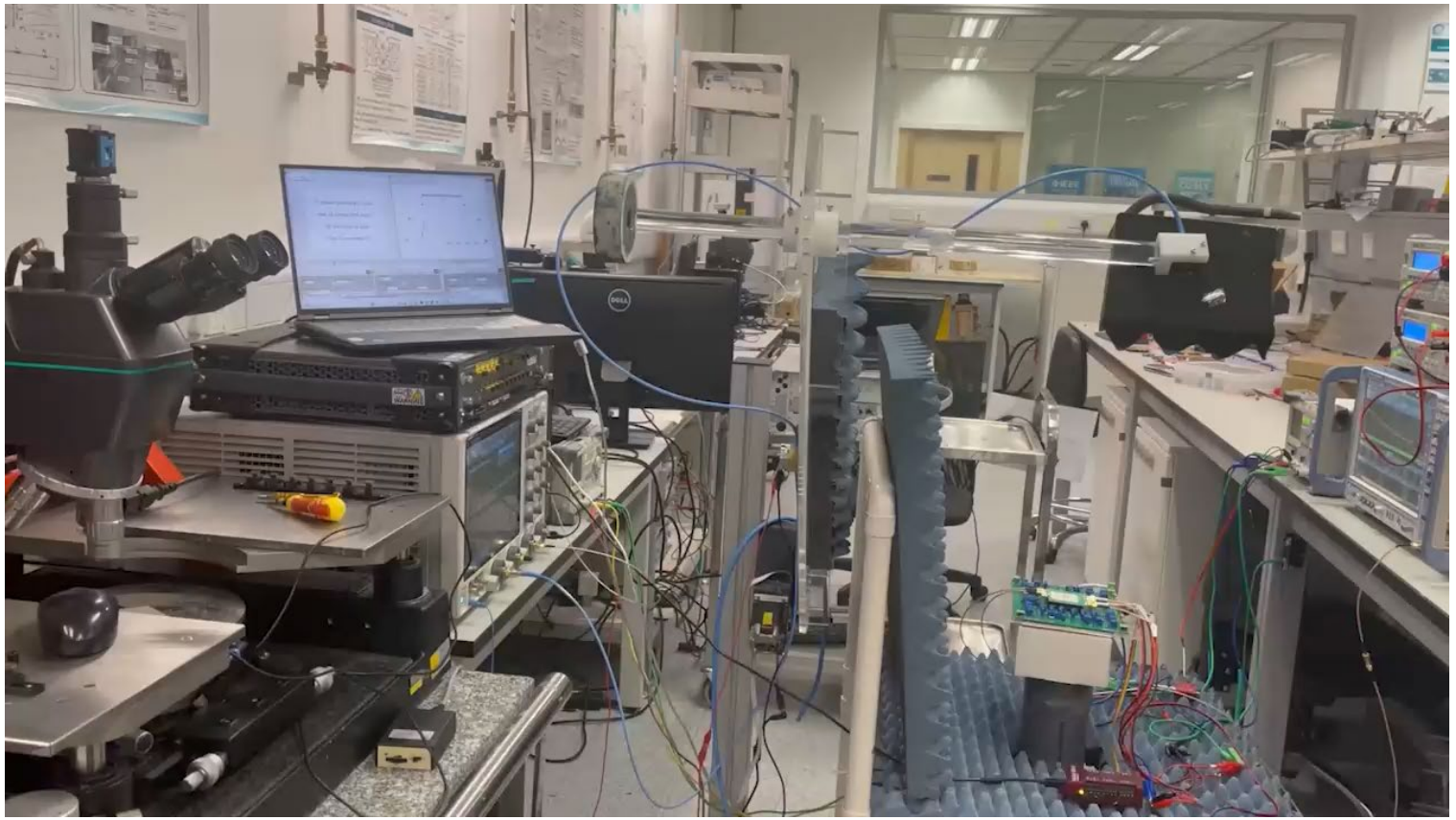
Complementary Signal Generator

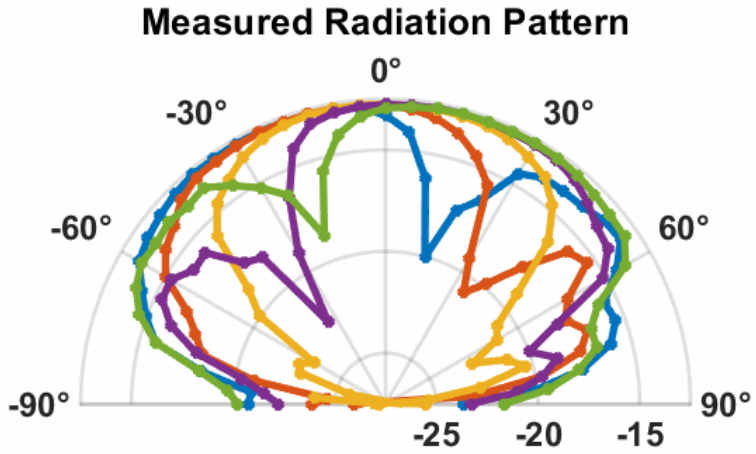
- The receiver integrates a Clock and Data Recovery (CDR), capable of detecting the phase and amplitude of the input jitter and generating a complementary jitter to negate the jitter transfer.

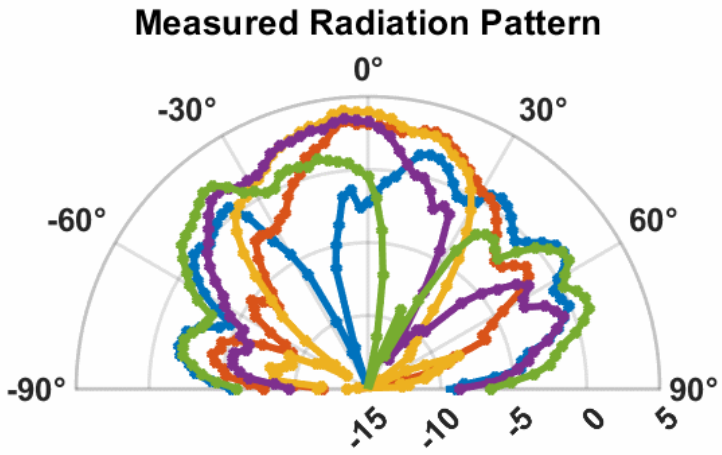
L. Wang, Z. Zhang, C. Wang, R. Azmat, W. Shi and C. P. Yue, "A 60-Gb/s 1.2-pJ/bit 1/4-Rate PAM-4 Receiver With a Jitter Compensation CDR," in *IEEE Journal of Solid-State Circuits*, vol. 59, no. 2, pp. 449-463, Feb. 2024

CMOS 產品原型：28GHz Phased-array Beamformer

- **Beamsteering Demo**

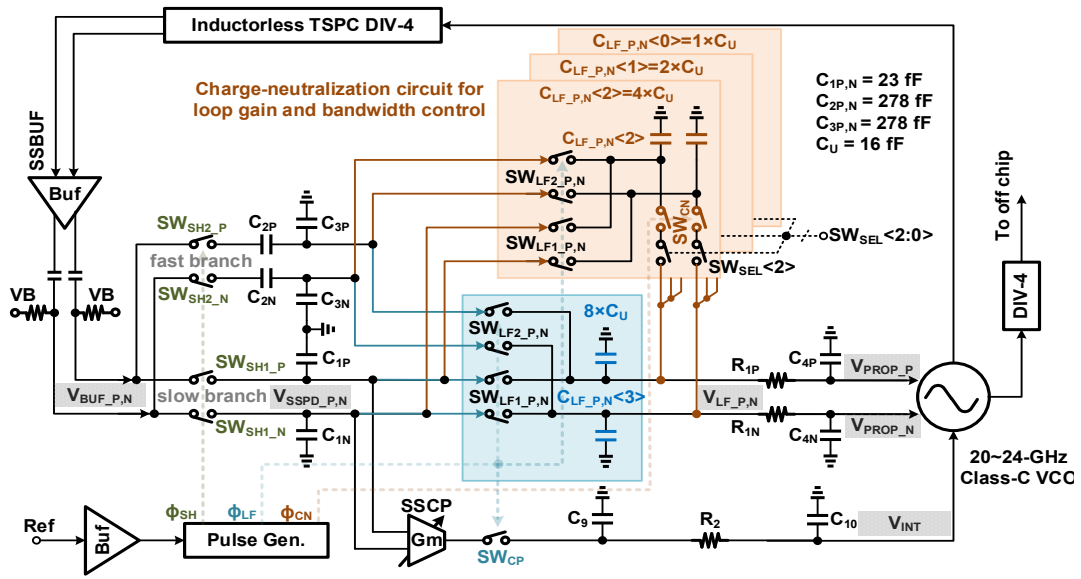




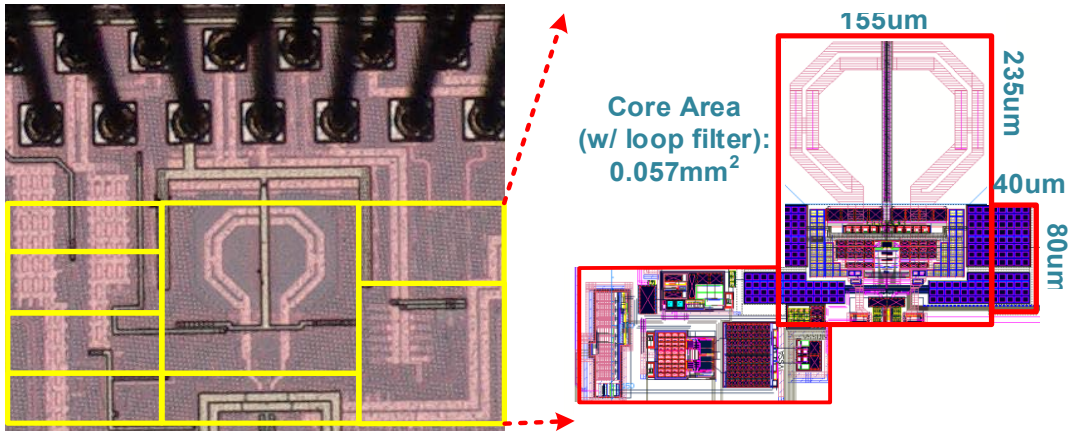


CMOS 產品原型：20–24-GHz Sub-Sampling PLL

- 22-GHz Compact, Low-Jitter Dual-path Sub-Sampling Phase-Locked Loop



System architecture of the proposed DPSSPLL



Total Chip Area: 0.126 mm²

Core Area: 0.057 mm²

- A low-noise charge-domain gain control technique provides a bandwidth tuning range greater than 30 dB, with noise contribution less than 3 fs
- The design achieves a compact area (0.057 mm²) and ultra-low jitter (61.23 fs), making it highly suitable for integration into phased array systems

L. Wang, Z. Liu, R. Ma and C. P. Yue, "A Compact 20–24-GHz Sub-Sampling PLL With Charge-Domain Bandwidth Control Scheme," in *IEEE Journal of Solid-State Circuits*, vol. 60, no. 3, pp. 768-784, March 2025

GaN 產品原型: PA, LNA, Laser Diode Driver

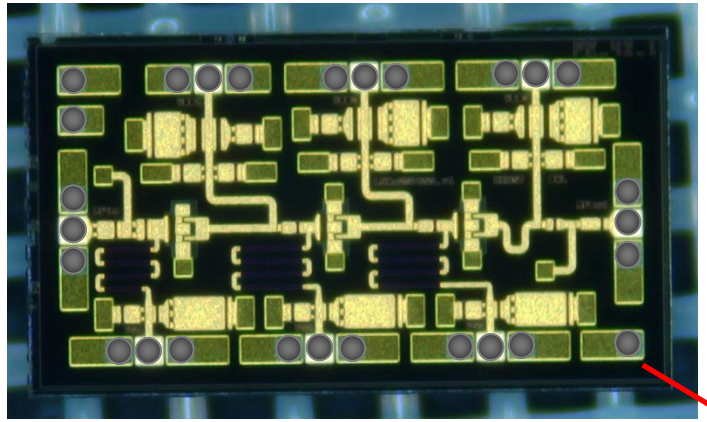


Fig. a

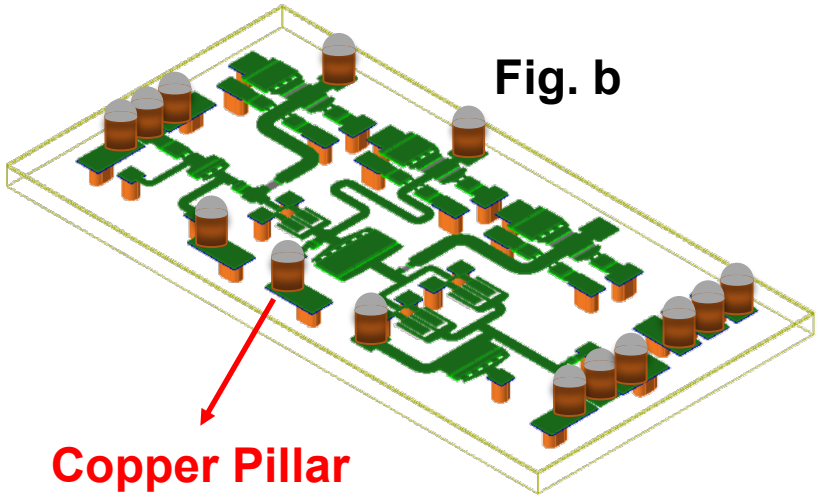


Fig. b

Copper Pillar Bumps for Flip-chip Bonding

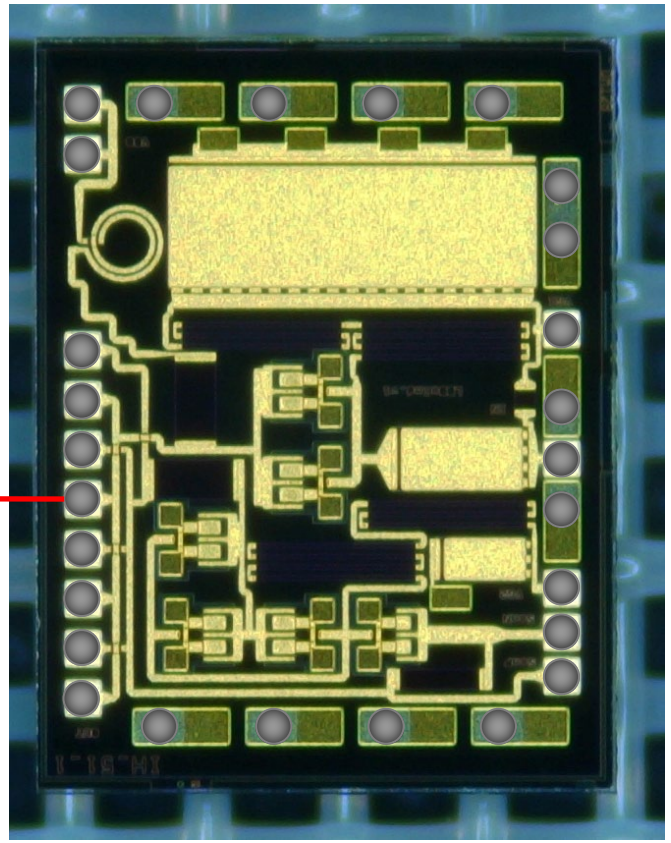
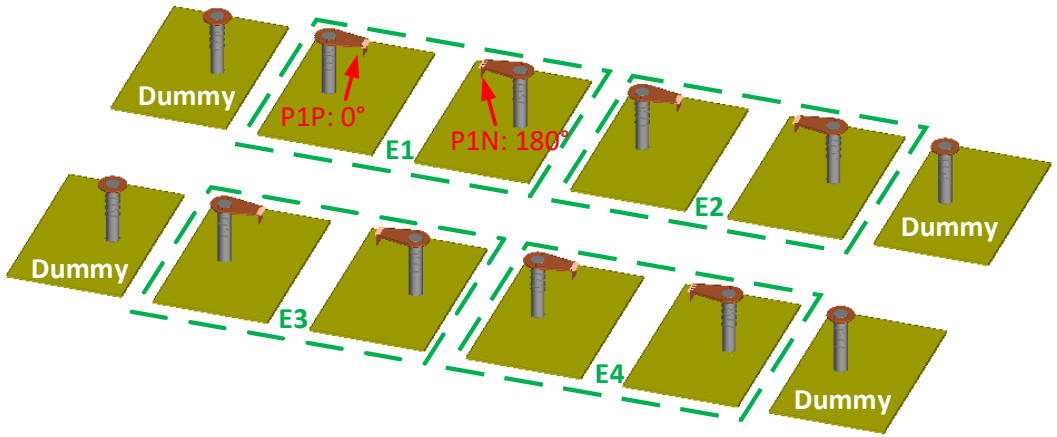


Fig. c

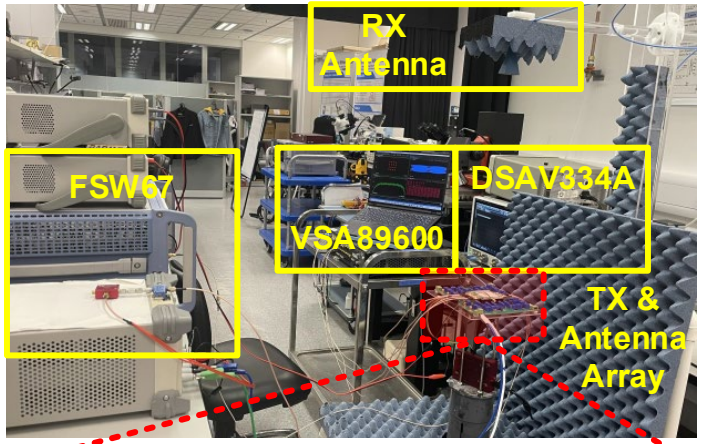
a. Top-view of a GaN low-noise Amplifier (LNA) chip with bumps
b. Top-left view of a GaN power amplifier (PA) chip with bumps
c. Top-view of a GaN laser diode driver (LDD) chip with bumps

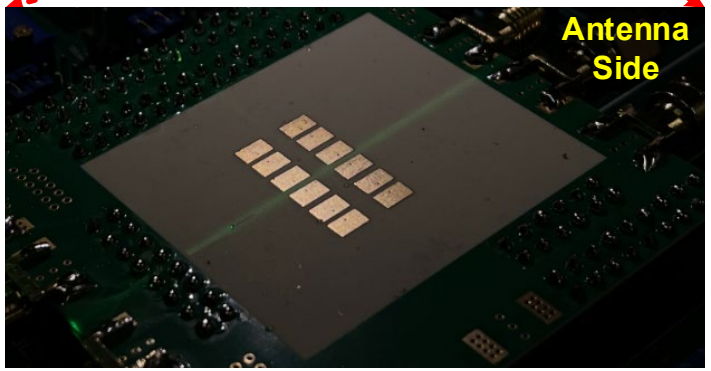
先進封裝產品原型：Chip-to-antenna-on-PCB Design

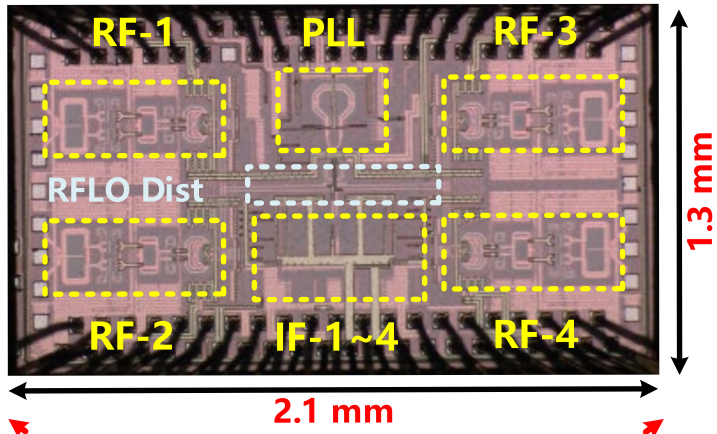
- **Antenna array**
  - **4 flipped patches, 4 dummy patches**
  - **Flipped patch driven by differential signals**
  - **Dummy patches are ground**



EM model of patch antenna on PCB







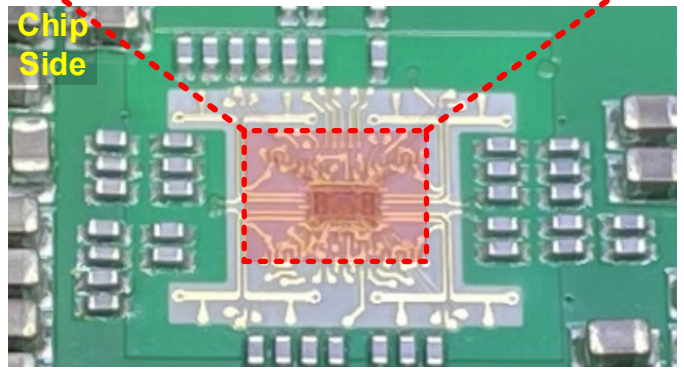
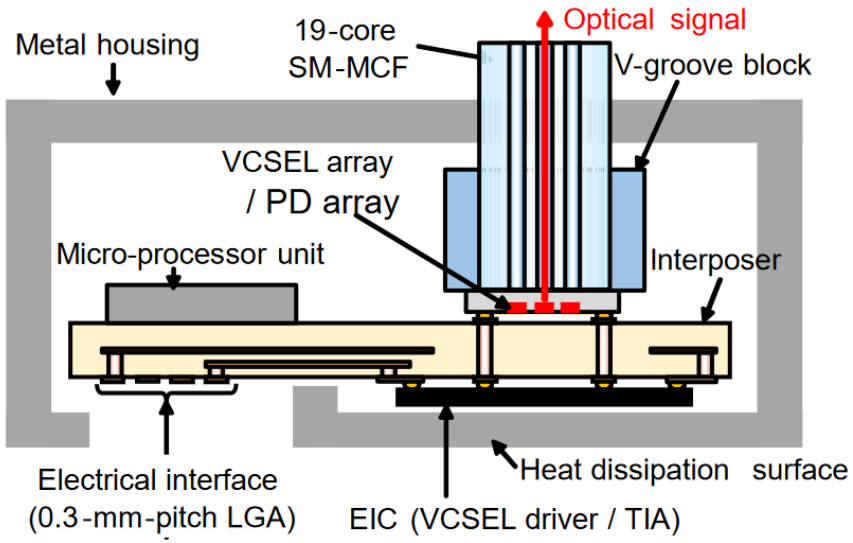


Photo of the top side (chip) and back side (antenna)

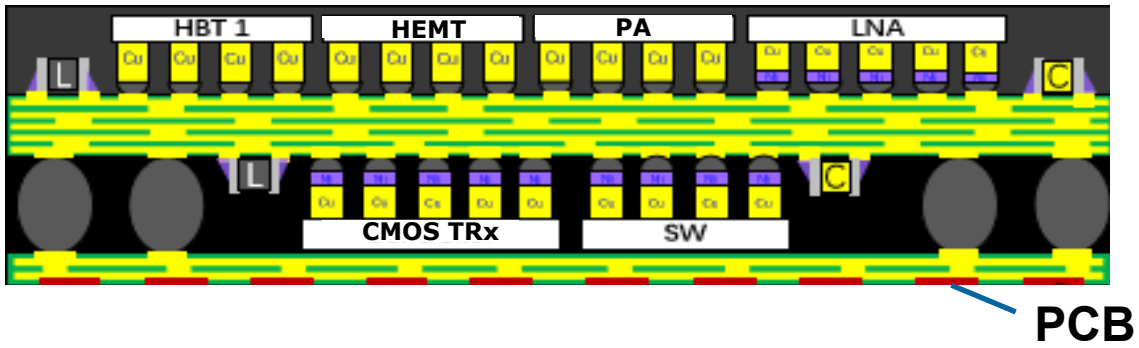
Z. Liu, L. Wang, R. Ma, Z. Chen and C. Patrick Yue, "A Compact 28-GHz Transmitter Front End With Co-Optimized Wideband Chip–Antenna Interface," in *IEEE Transactions on Microwave Theory and Techniques*

先進封裝產品原型: Interposer Substrate Design



Dual-side Co-Packaged Optics (CPO)

- Double-sided flip-chip-bonding
- Direct Multi-Core Fiber (MCF) buttom-coupling
- Core-less organic build-up interposer (thinner)



Dual-side Interposer for Wireless Satcom

- Double-sided flip-chip-bonding
- Passive components in the middle layer of the interposer for matching, filtering, etc.
- Front-end modules on the top side
- CMOS chiplets on the back side
- Solder balls to connect the interposer to the PCB
- Patch antennas will be designed on PCB

內容綱要

- 團隊成員與技術協同
- 市場機遇
- 技術路綫與目標市場
- 產品描述與原型
- 商務拓展

產品競爭力 / 市場格局

Competitive Analysis	Area	Company	Product Descriptions
Optical Communication Products for DCI	Domestic	WISEWAVE, InSiGa XXXX Bridging Technologies, 中晟微电子 LEADINGSPEED TECHNOLOGY	100G/400G/800G optical modules, optoelectronic chips, lasers, etc.
	Global	MARVELL, MACOM, BROADCOM, ANALOG DEVICES	High-speed optical modules (400G/800G), optoelectronic chips (CPO), PAM4 chips, high-speed DSP chips
Wireless Products for Satellite Communication	Domestic	天锐星通, 国博电子 Guobo Electronics, 铖昌科技 CHENGCHANGTECH	Satellite ground equipment, inter-satellite communication modules, RF front-end chips, low-earth orbit satellite terminals
	Global	STARLINK, OneWeb, MACOM, ANALOG DEVICES	Satellite communication terminals, low-earth orbit satellite networking systems, RF front-end modules, high-speed ADC/DAC chips

與 RAISe+ 相關的合作夥伴及背書支持

Packaging Partner

Faraconix 升新科技

GaN Partner

dynax 能讯

思坦科技 SITAN TECHNOLOGY

Other Partners

ASTRI

WISEWAVE

berxel 博升光电

ICLEGEND MICRO

Investors and Customers

Faraconix 升新科技

思坦科技 SITAN TECHNOLOGY

NLMILE

HUAWEI

6 technology R&D partners

4 engaged customers

與 GaN 行業建立戰略合作夥伴關係

- **與 GaN 代工夥伴 Dynax (蘇州能訊高能半導體)**

- **與 GaN & micro-LED 代工夥伴 Sitan (思坦科技)**

總部設立於香港科學園（HKSTP）

- 在香港註冊並設立辦公室
- 由香港投資推廣署（InvestHK）支持

編號 No. 77009722

CR

公司註冊處
COMPANIES REGISTRY

公司註冊證明書
CERTIFICATE OF INCORPORATION

* * *

本人謹此證明
I hereby certify that

High5 Semiconductor (Hong Kong) Limited
高武半導體（香港）有限公司

李強發表開幕式主旨演講 周霽龔正李家超

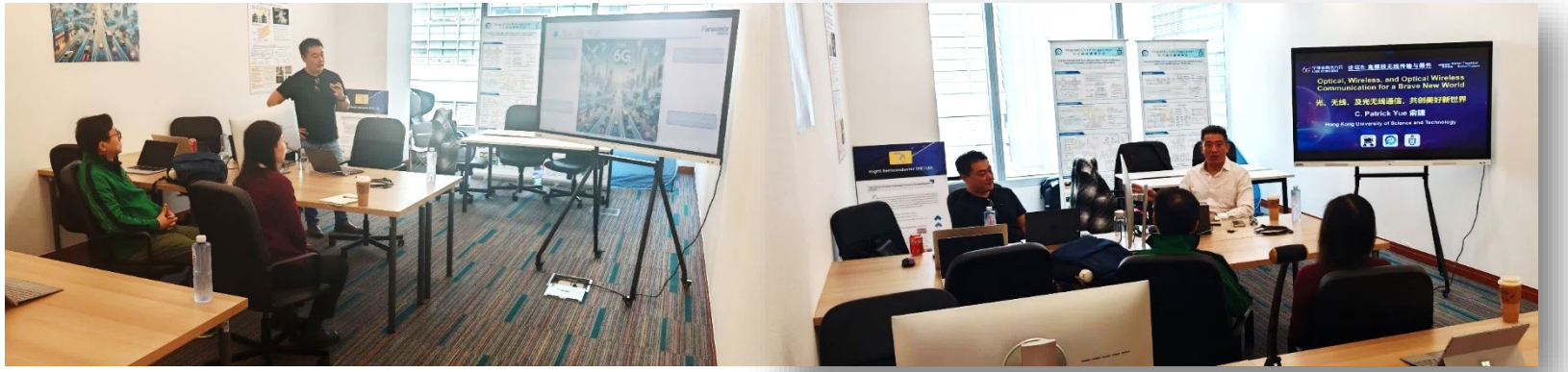
進博會首日 五大滬企與

李家超昨日早上與財政司司長陳茂波等一同出席進博會暨虹橋國際經濟論壇開幕式。隨後，李家超陪同國務院總理李強巡視中國館香港展區。下午到貿發局在企業商業展設立的展區參觀和支持香港企業。投資推廣署及旅發局亦在其間設展位重點宣傳香港優勢，介紹最新旅遊特色。其後，李家超和陳茂波出席了「2024投資香港推介大會——上海專場」，並分別在會上致辭。

歡迎企業善用港優勢謀發展

李家超在致辭中回顧了滬港交流的悠久歷史和取得的重要成就。他表示，滬港兩地多年來的合作不斷走深走實，根深葉茂。目前，在港上市的上海企業就有接近200家，市值超過兩萬億港元，充分顯示香港可以成為服務上海和內地企業發展的投融資平台。歡迎更多上海和內地的企業，利用香港走向世界，共謀發展。

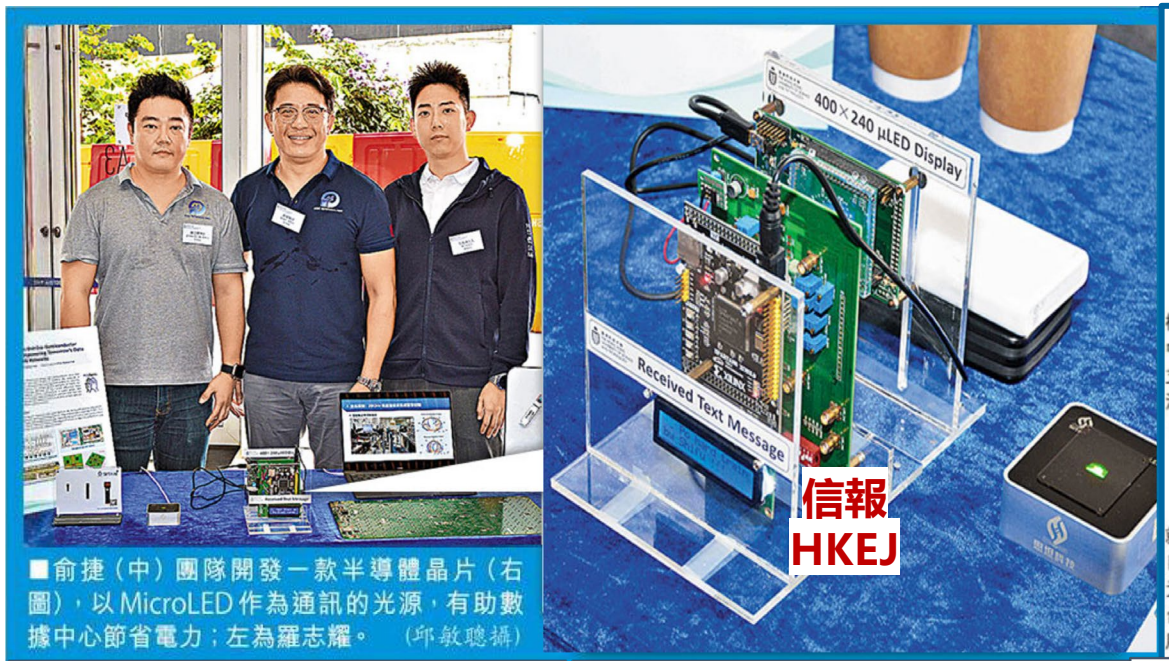
▶李家超在進博會見證了多個合作項目簽約，並與參與簽約的企業負責人交流。圖為與升新科技（上海）有限公司總經理蘇志耀（左）和上海哈曜智惠科技有限公司高級副總裁褚軼群（右）合影。



InvestHK
The Government of the Hong Kong Special Administrative Region

傳媒廣汎關注與報道

- 獲批港府創新科技署(ITC)產學研1+(RAISe+)資助，受到傳媒廣汎關注



■俞捷（中）團隊開發一款半導體晶片（右圖），以MicroLED作為通訊的光源，有助數據中心節省電力；左為羅志耀。（邱敏聰攝）

信報
HKEJ

李強發表開幕式主旨演講 周霽龔正李家超

進博會首日 五大滬企與

李家超昨日早上與財政司司長陳茂波等一同出席進博會暨虹橋國際經濟論壇開幕式。隨後，李家超陪同國務院總理李強巡視中國館香港展區。下午到[illegible]設立的展區參觀和支持香港企業。投資推廣[illegible]設展位重點宣傳香港優勢，介紹最新旅遊特[illegible]家超和陳茂波出席了「2024投資香港推介大會」[illegible]並分別在會上致辭。

香港電臺
RTHK

歡迎企業善用港優勢謀發展

李家超在致辭中回顧了滬港交流的悠久歷史和取得的重要成就。他表示，滬港兩地多年來的合作不斷走深走實，根深葉茂。目前，在港上市的上海企業就有接近200家，市值超過兩萬億港元，充分顯示香港可以成為服務上海和內地企業發展的投融資平台。歡迎更多上海和內地的企業，利用香港走向世界，共謀發展。

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A9 港聞

教育線上

科大 從癌症治療到半導體研發

7項目獲產學研1+資助

香港科技大學（科大）在創新科技署推出的「產學[illegible]計劃」（RAISe+）第二輪撥款中表現超[illegible]，在本港高[illegible]這七[illegible]展，其中[illegible]龍和發[illegible]新、治療及基因療法等，另外三個專注於人工智能（AI）晶片、半導體及其材料的開發，第七個項目則有關開發顯示器及先進光電設備。

大公報記者 華英明

▲科大在第二輪「產學研1+計劃」撥款中，共有七個項目獲批資助。

大公報

科大第二批獲「產學研 1+ 計劃」部分資助項目

首創高效治療宮頸癌前病變及宮頸癌的原研DRIPs抑制劑開發

主要研究員及項目負責人：科大生命科學部副教授梁純

團隊利用DNA複製起始蛋白（DRIPs）作標靶，首創一款能誘導異常癌細胞凋亡的「除道凝膠」，指動物實驗結果顯示，凝膠在動物體內的抑瘤率達96%，稱近乎完全消除子宮頸癌及癌前細胞。凝膠亦可治療皮膚癌，正展開第二期臨牀測試。產品可放於室溫、容易使用，團隊料於2031年推出市面

高效能大模型推理晶片與系統

主要研究員：智能晶片與系統研發中心副主任崔志英

項目負責人：港芯智能副總經理王懷斌

團隊研發一款高效能邊緣晶片及系統，結合軟硬件協同設計平台、AI大模型壓縮技術及數字存內計算技術，透過即時處理與可持續效能，提升端側人工智能的計算性能

多中心臨牀開發用於檢測前驅症狀、輕度認知障礙和早期阿茲海默症的血液生物標誌物

主要研究員：科大[illegible]後研究員江源冰

項目負責人：康至[illegible]恩經理歐陽麗

全球首個針對阿[illegible]血液測試技術，並開發兩款血液[illegible]款可精準檢測病理及分析疾病生[illegible]96%。另一款高效、低成本的血液測試則可用於大規模篩檢，特別適用於低收入地區。比對傳統大腦「PET掃描」，該技術能降低80%檢測成本

賦能未來數據中心和6G網絡的下一代高端節能半導體芯粒

主要研究員及負責人：科大電子及計算機工程學系教授俞捷

結合了硅基CMOS和GaN芯粒的半導體晶片，適用於先進的通訊系統，能提高數據處理和傳輸速率、能效及信號質量，有望支援6G網絡，為低軌衛星系統等應用提供高頻、長距離通訊

資料來源：香港科技大學

明報

科大7研究項目獲「產學研1+計劃」資助

創新科技署早前公布第二批「產學研1+計劃」的資助名單，共有25個研究項目獲資助，其中香港科技大學有7個研究項目入選，成為本地大學中獲批項目最多的院校。其中，獲資助的「多中心臨床開發用於檢測前驅症狀、輕度認知障礙和早期阿茲海默症（AD）的血液生物標誌物」研究項目，是香港首個針對阿茲海默症的多蛋白血液檢測技術，主要研究員江源冰及其團隊期望，未來開展全球臨床試驗，以加速血液檢測產品通過監管審批。

研阿茲海默症檢測新技術

科大昨日[illegible]資助團隊的代[illegible]包括江源冰及[illegible]計劃推出兩款[illegible]PlasmarkAD® Pro系列及PlasmarkA® Lite。PlasmarkAD® Pro系列是已正式推出的全面血液測試，但成本比PlasmarkAD® Lite高，並於10天內生成檢測報告。至於PlasmarkAD® Lite，則是一款更高效、更低成本的檢測技術，目前處於原型設計階段，尚未推出，需要通過審批。未來，該產品將以試劑盒形式推出，方便醫生直接在醫院現場為患者進行檢測，預計成本約為1000元。

被問及科大正計劃申請建立香港第三間醫學院，其研究項目未來將如[illegible]院的發展，江源冰及團隊[illegible]目前無法直接預測相關資[illegible]學院的具體貢獻，但血液[illegible]核心在於與臨床的緊密合作，這對培養醫科生及醫學技術的落地應用具有重要意義。

另一獲資助研究項目「首創高效治療宮頸癌前病變及宮頸癌的原研DRIPs抑制劑開發」項目負責人梁純回應指「醫藥不分家」，指出其研究不僅能促進醫學知識的發展，也能幫助提升學生在生物技術領域的專業能力，助力培育未來醫療人才。 記者 陳美英

■科大共有7個研究項目入選第二批「產學研1+計劃」資助名單。左四為江源冰。 汪旭峰攝

星島日報

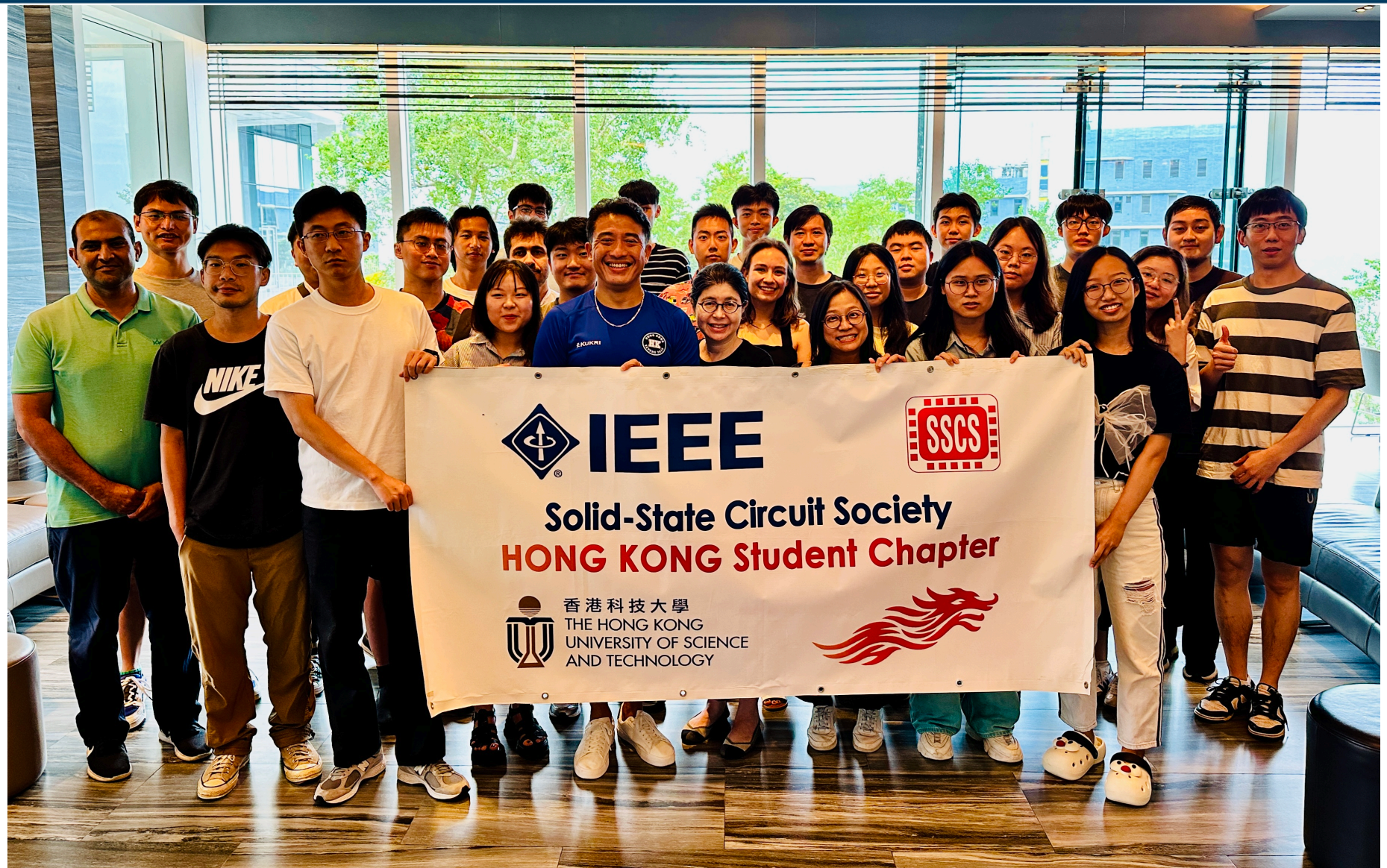
從癌症治療到半導體開發

港科大七項目獲特區資助

華僑報

Acknowledgements (HKUST OWL Alumni)

Acknowledgements (HKUST OWL Current Members)



香港科技大學
THE HONG KONG UNIVERSITY OF SCIENCE AND TECHNOLOGY

Hi5Semi

High5 Semiconductor (HK) Limited

高武半導體(香港)有限公司

HQ OWL

Thanks!

謝謝!

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https://high5semi.github.io/

Optical Wireless Lab

Department of Electronic and Computer Engineering

The Hong Kong University of Science and Technology (HKUST)

Hi5 Semi

High5 Semiconductor (Hong Kong) Limited

高武半導體(香港)有限公司