香港科技大學
THE HONG KONG UNIVERSITY OF SCIENCE AND TECHNOLOGY

HKUST OWL

Silicon-based Transmitter Design for Optical Fiber Communications

Fuzhan Chen
Supervisor(s): Prof. C. Patrick Yue, Prof. Quan Pan (SUSTech)

2024-11-15

Optical Wireless Lab
Department of Electronic and Computer Engineering
The Hong Kong University of Science and Technology (HKUST)

Outline

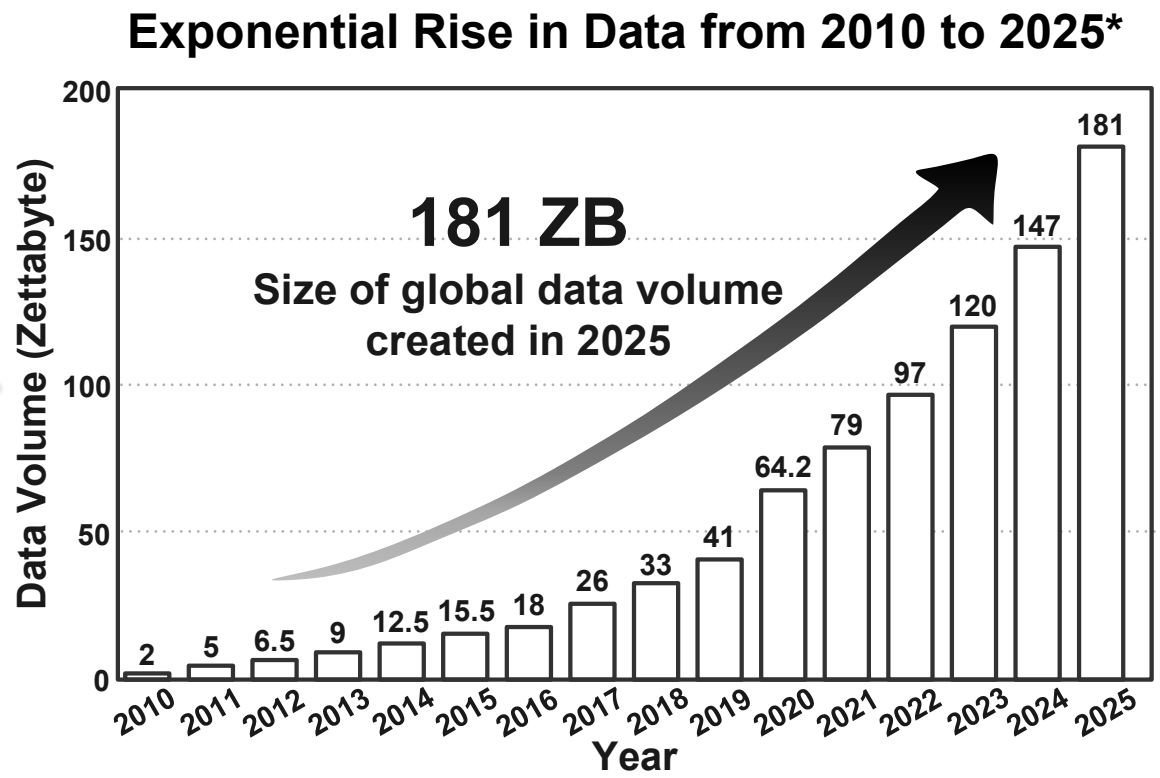
- Background
- Transmitter Design for VCSEL-based Optical Links
  - Imperfections of VCSEL
  - Implementation and Measurement of A 56-Gb/s PAM-4 VCSEL Transmitter
- Transmitter Design for Optical Modulator-based Optical Links
  - Design Challenges
  - Implementation and Measurement of A 56-Gbaud Linear Modulator Transmitter
  - Implementation and Measurement of A 100-Gbaud Linear Modulator Driver
- Conclusions

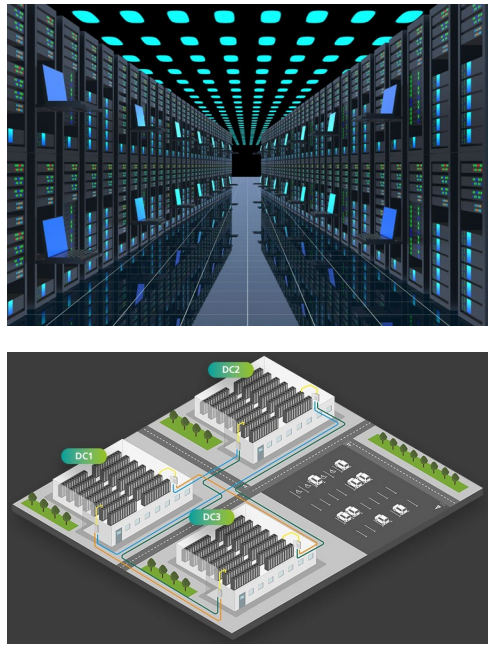
Outline

- **Background**
- Transmitter Design for VCSEL-based Optical Links
  - Imperfections of VCSEL
  - Implementation and Measurement of A 56-Gb/s PAM-4 VCSEL Transmitter
- Transmitter Design for Optical Modulator-based Optical Links
  - Design Challenges
  - Implementation and Measurement of A 56-Gbaud Linear Modulator Transmitter
  - Implementation and Measurement of A 100-Gbaud Linear Modulator Driver
- Conclusions

Research Background

- Cutting-edge information technologies create **massive data volume**
- **Data center interconnects** to be upgraded towards **higher data rate** and **better energy efficiency**

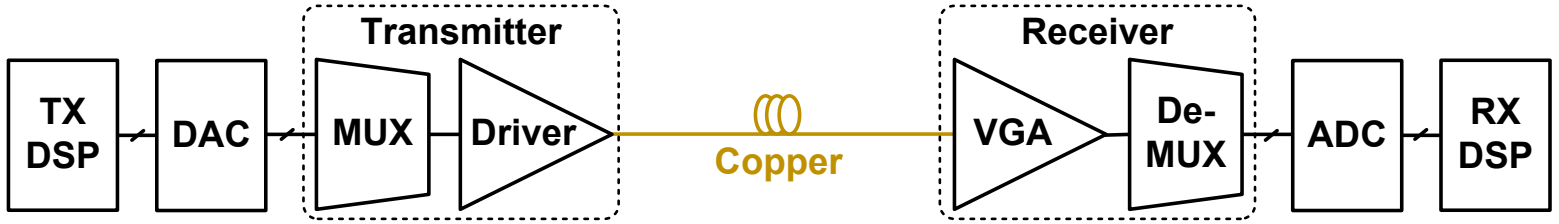




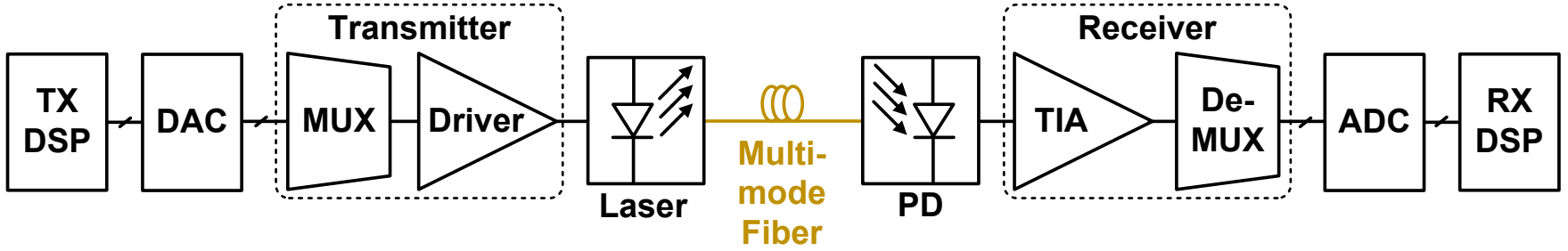
(*IDC and Statista, "Volume of data/information created, captured, copied, and consumed worldwide from 2010 to 2020, with forecasts from 2021 to 2025," in *https://www.statista.com/statistics/871513/worldwide-data-created/*, June 2021.)

Electrical vs MM Optical vs SM Optical Links

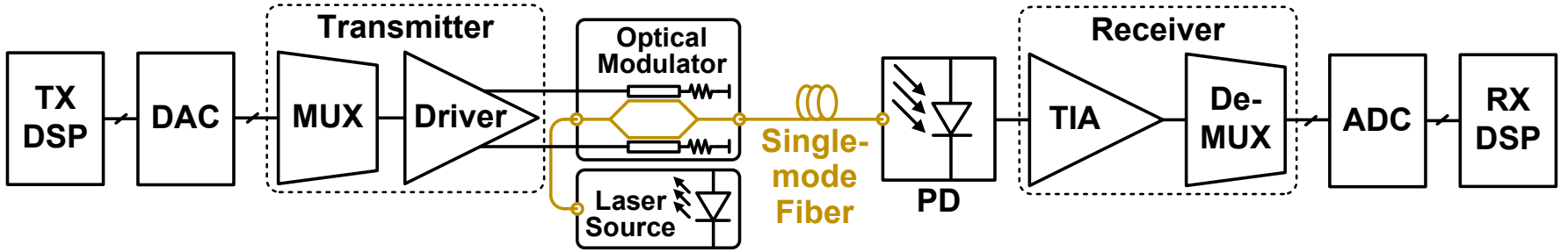
Electrical Link



Multi-mode (MM) Optical Link

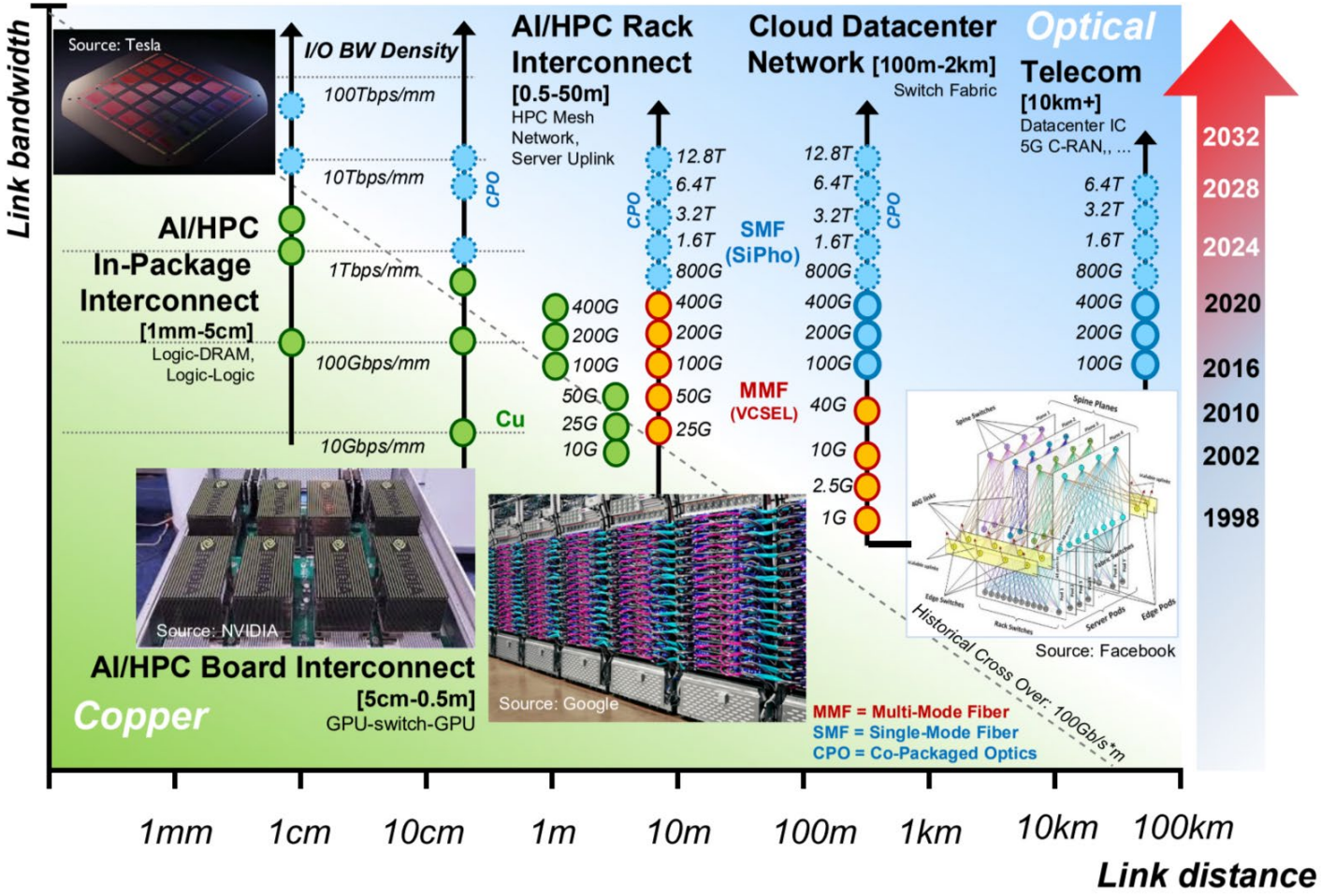


Single-mode (SM) Optical Link



Electrical vs MM Optical vs SM Optical Links

Wireline Interconnect Roadmap*



Electrical Link

- High loss, low bandwidth
- Low cost
- Distance-data rate product (DDP) < 100 Gb/s*m

MM Optical Link

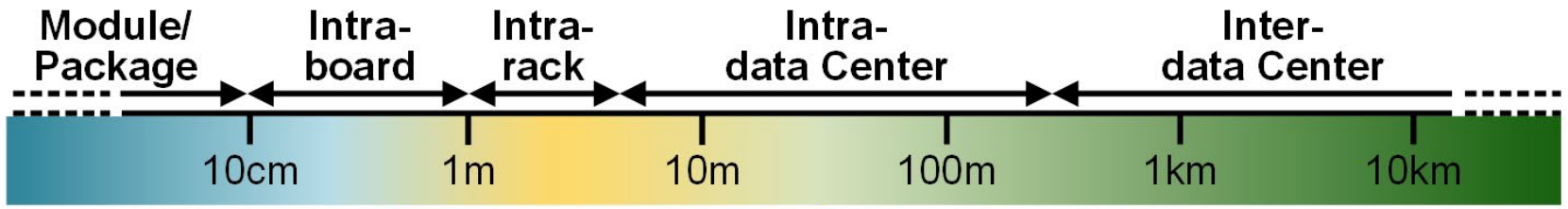
- Low loss, high bandwidth
- Moderate cost, dispersion issue
- 100 Gb/s*m < DDP < 4000 Gb/s*m

SM Optical Link

- Low loss, high bandwidth, low dispersion
- High cost
- 4000 Gb/s*m < DDP

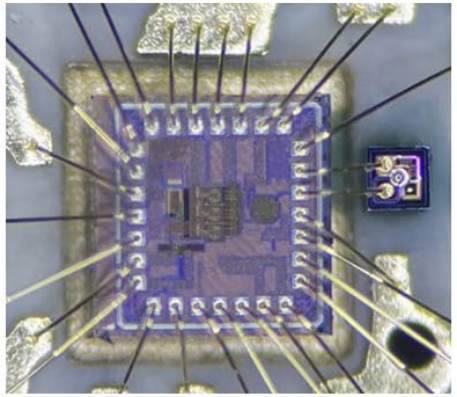
(*Joris Van Campenhout, "Silicon Photonics Technology for Next-Generation Transceivers," in *ISSCC 2022 Forum 4*, Feb. 2022.)

Thesis Scope

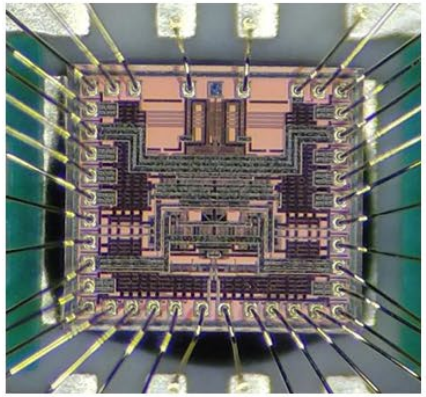


Multi-mode Optics

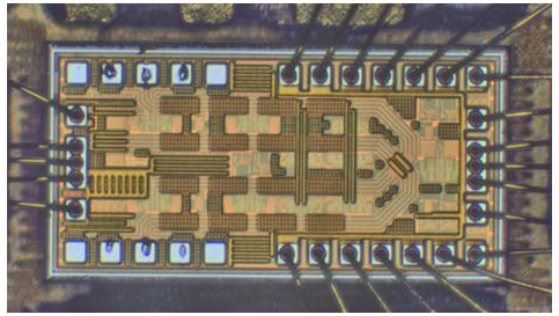
Single-mode Optics



Work-1: A 56-Gb/s PAM-4 VCSEL TX with Piecewise Compensation



Work-2: A 56-Gbaud Linear Modulator TX with AMUX-FFE and Large-swing Driver

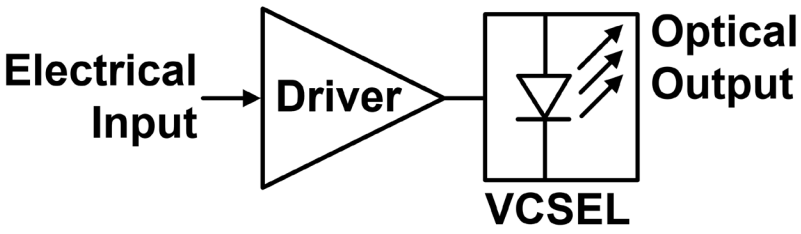


Work-3: A 100-Gbaud Distributed Linear Driver with Built-in FFE

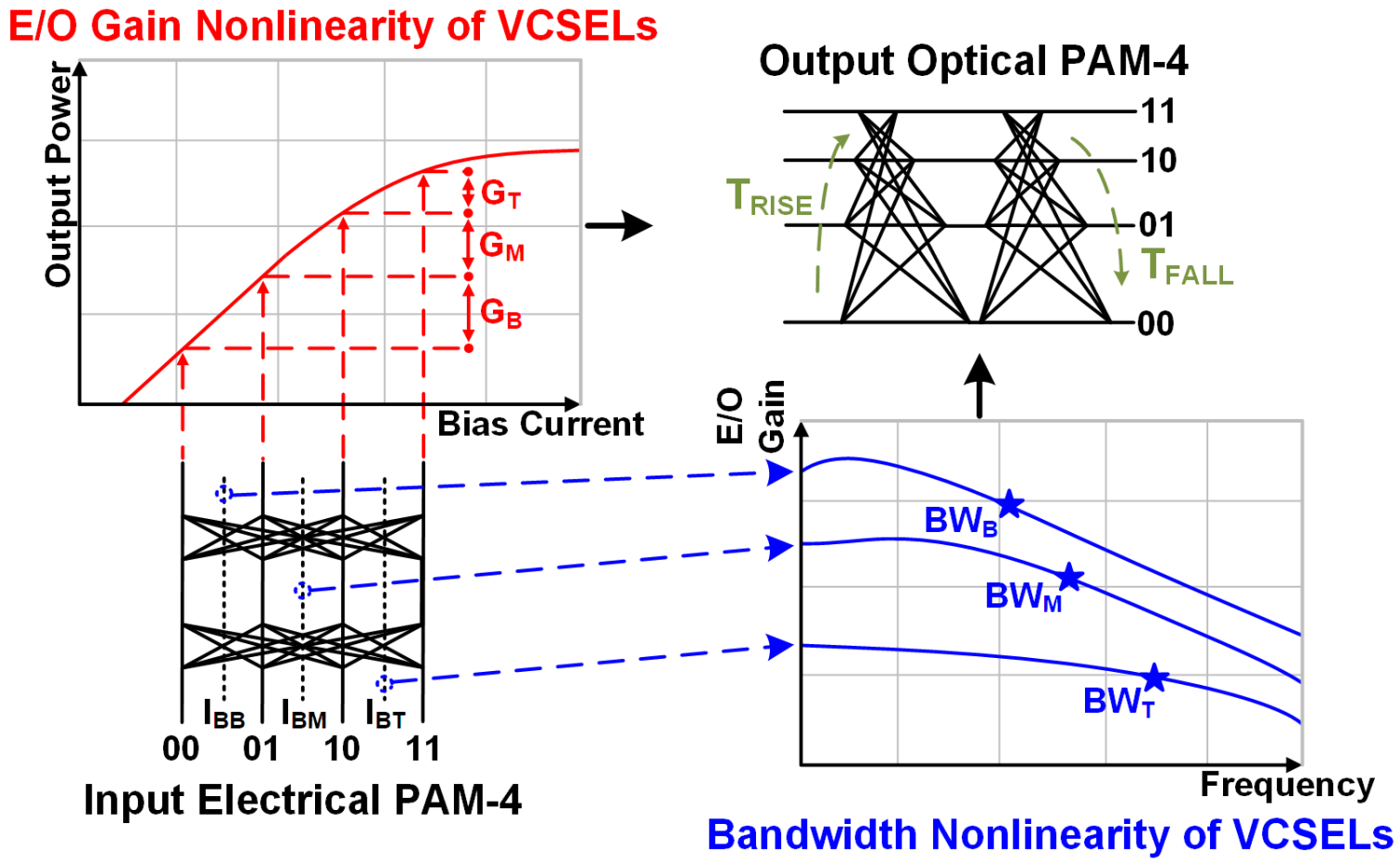
Outline

- Background
- **Transmitter Design for VCSEL-based Optical Links**
  - **Imperfections of VCSEL**
  - Implementation and Measurement of A 56-Gb/s PAM-4 VCSEL Transmitter
- Transmitter Design for Optical Modulator-based Optical Links
  - Design Challenges
  - Implementation and Measurement of A 56-Gbaud Linear Modulator Transmitter
  - Implementation and Measurement of A 100-Gbaud Linear Modulator Driver
- Conclusions

Imperfections of VCSEL



- Bias current ↑, E/O gain ↓ ($G_B > G_M > G_T$)
- Bias current ↑, bandwidth ↑ ($BW_B < BW_M < BW_T$)
- $T_{RISE} < T_{FALL}$

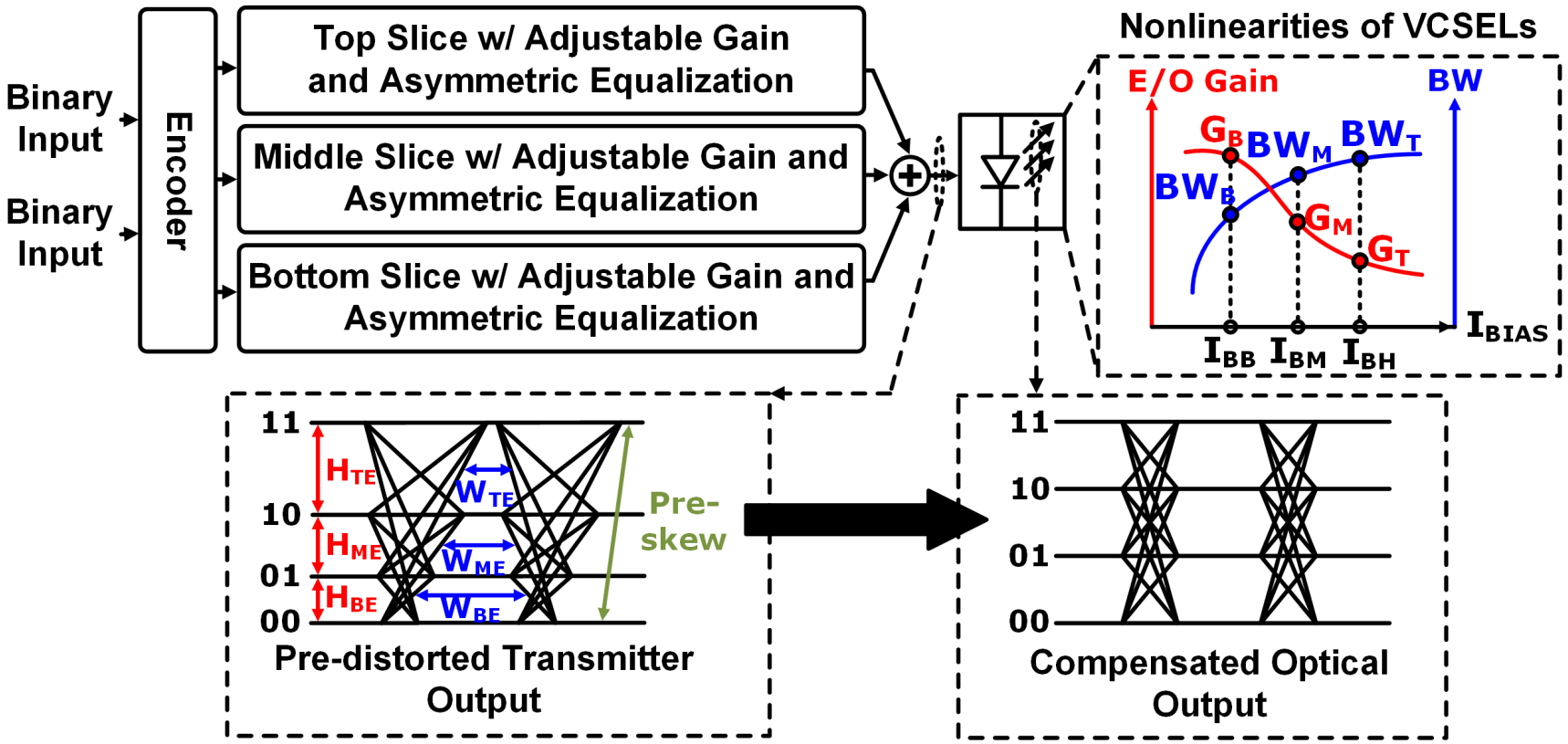


Outline

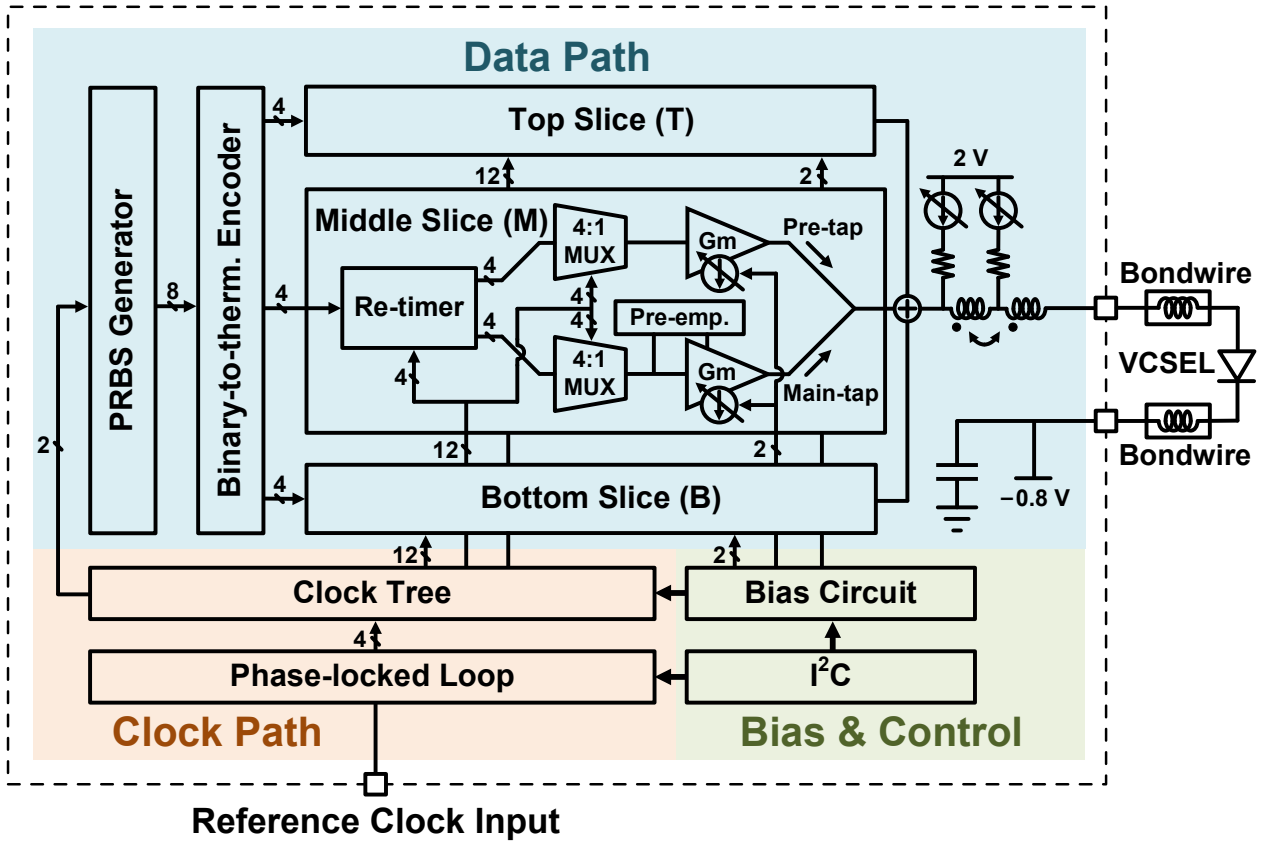
- Background
- **Transmitter Design for VCSEL-based Optical Links**
  - Imperfections of VCSEL
  - **Implementation and Measurement of A 56-Gb/s PAM-4 VCSEL Transmitter**
- Transmitter Design for Optical Modulator-based Optical Links
  - Design Challenges
  - Implementation and Measurement of A 56-Gbaud Half-rate Linear Transmitter
  - Implementation and Measurement of A 100-Gbaud Distributed Linear Driver
- Conclusions

Conceptual Architecture

Thermometer code-based architecture to **piecewise compensate** for **nonlinearity in E/O gain**, **nonlinearity in bandwidth**, and **asymmetric responses to rising/falling transitions**



Detailed Architecture

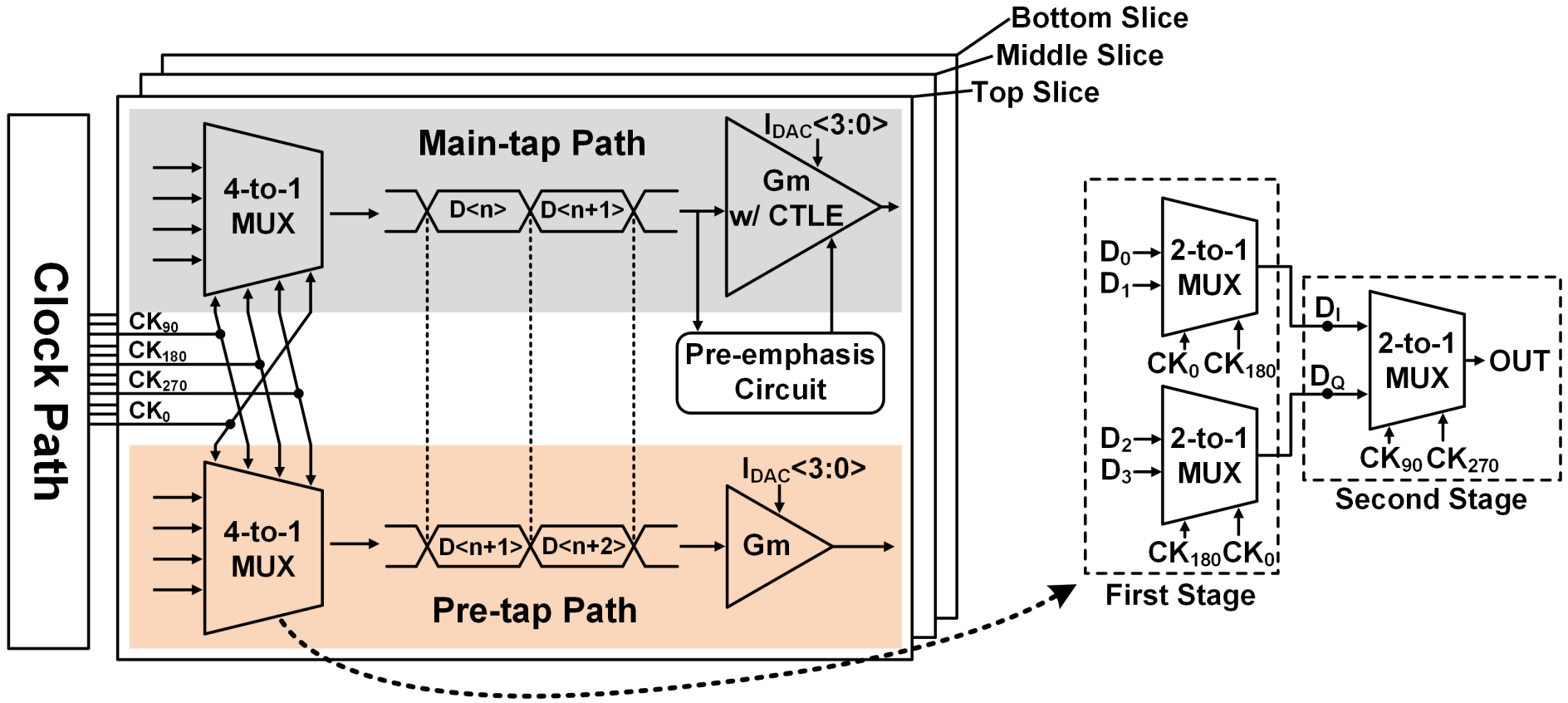


- Data path
  - 2-tap feed-forward equalizer
  - Gm cell-merged CTLE
  - Pre-emphasis circuit
- Clock path
  - Wideband phase-locked loop
  - Clock tree with cascading VCDLs
- Bias & control part
- Optical part
  - Wire-bonded anode-driven VCSEL
  - Negative bias for power saving

4-to-1 Multiplexer (MUX)

Functions of 4-to-1 MUX

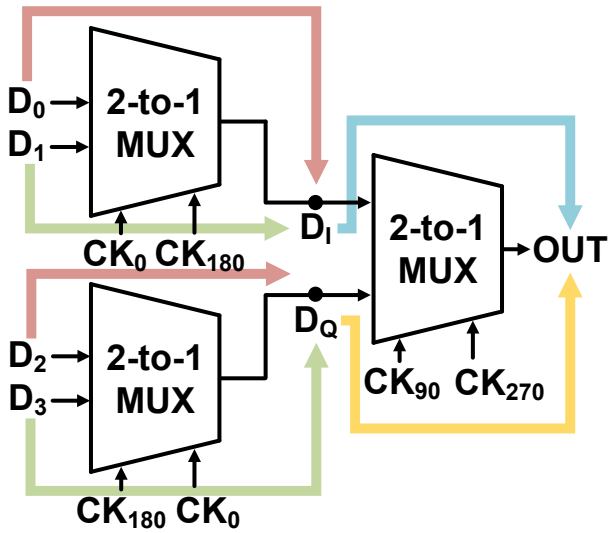
- 4 quarter-rate data streams → 1 full-rate data stream
- Controls tap interval of the 2-tap FFE



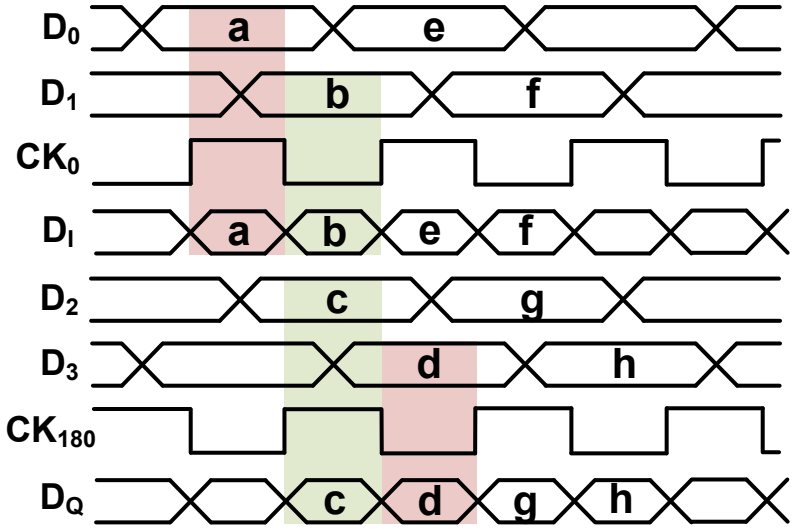
4-to-1 Multiplexer (MUX)

Principle of 4-to-1 MUX

- Implemented by cascading two-stages of 2-to-1 MUXs
- 1st-stage 2-to-1 MUX serializes D_0~D_1 to D_I and D_Q
- 2nd-stage 2-to-1 MUX further serializes D_I and D_Q to OUT



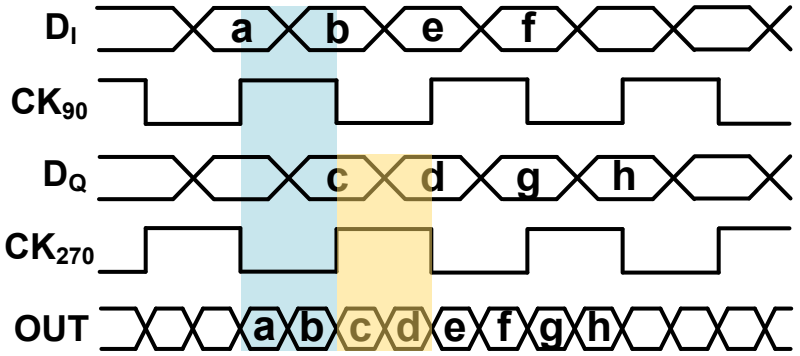
First-stage Serialization



Time window when CK_0 is high

Time window when CK_{180} is high

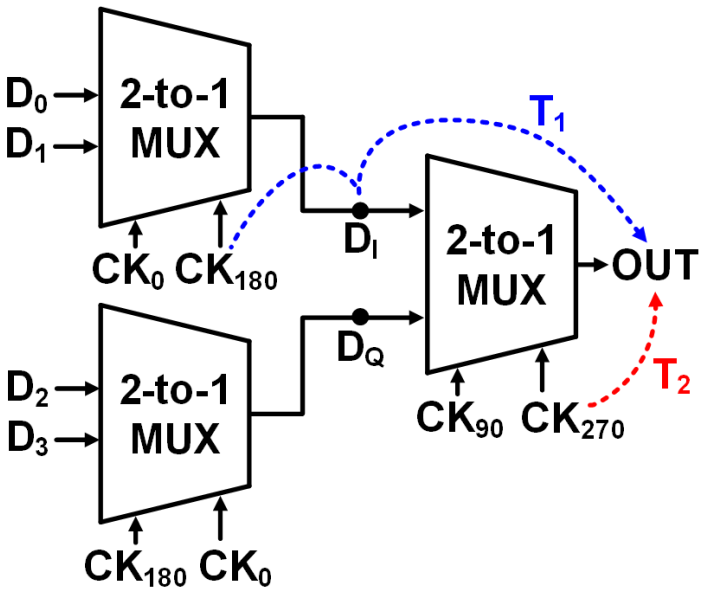
Second-stage Serialization

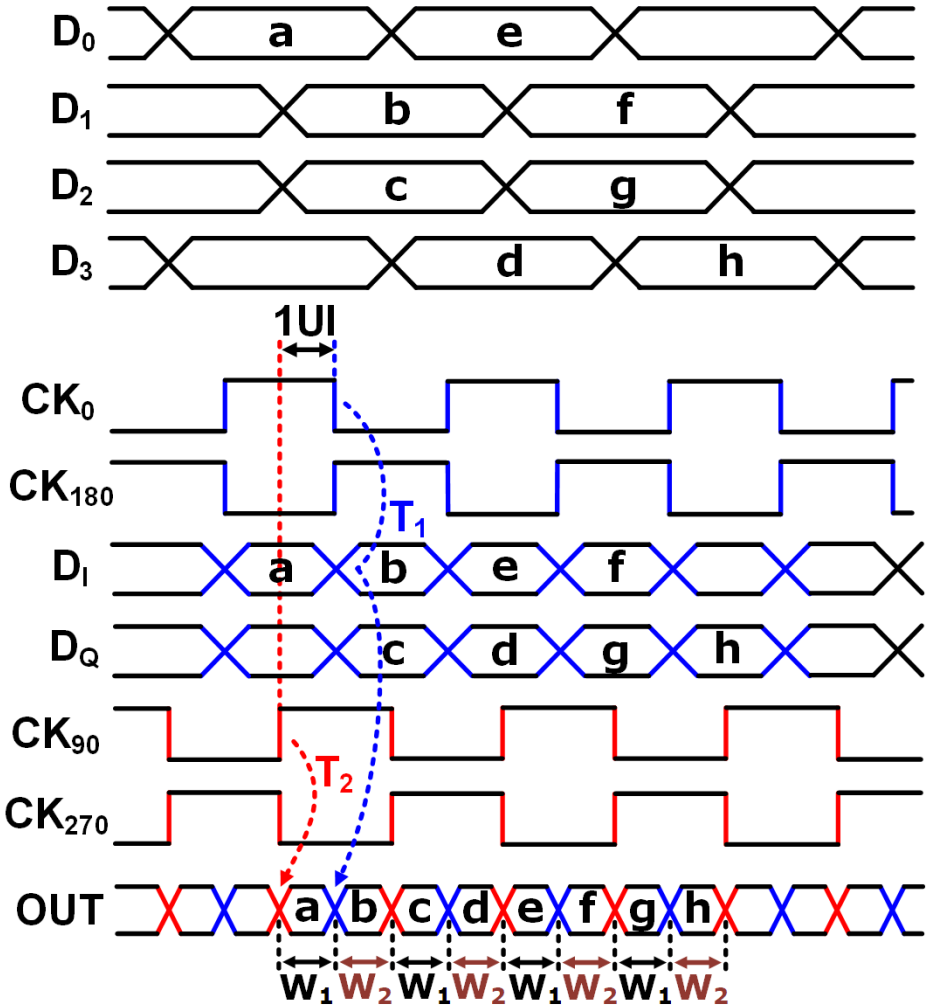


Time window when CK_{90} is high

Time window when CK_{270} is high

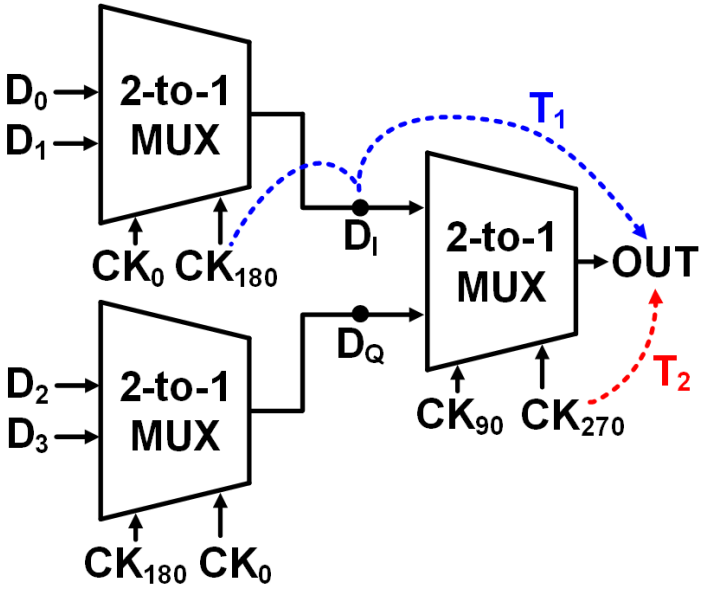
4-to-1 Multiplexer (MUX)

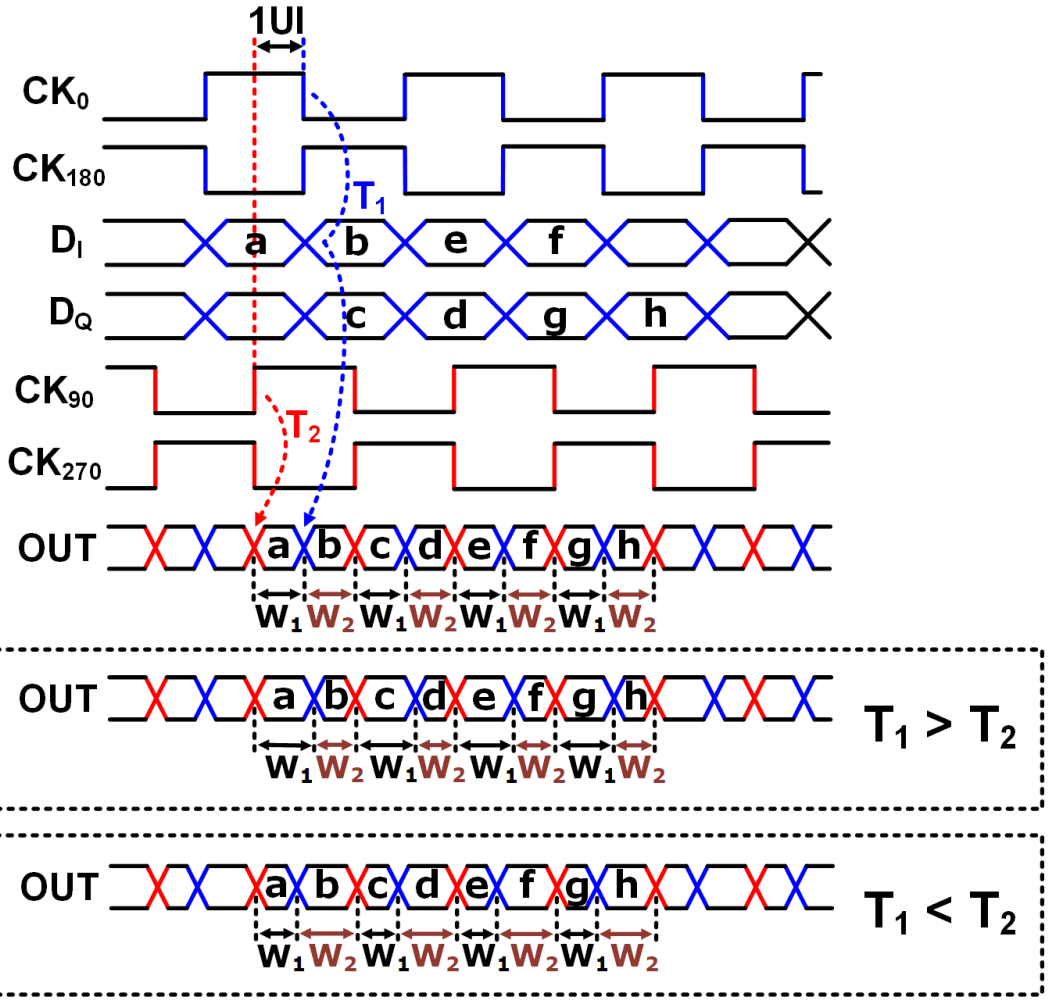




- T_1: Delay from CK_0 (CK_{180}) to OUT
- T_2: Delay from CK_{90} (CK_{270}) to OUT
- $T_1 \neq T_2 \rightarrow$ Duty Cycle Distortion of the Output

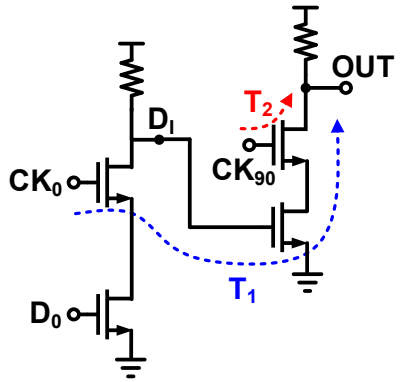
4-to-1 Multiplexer (MUX)



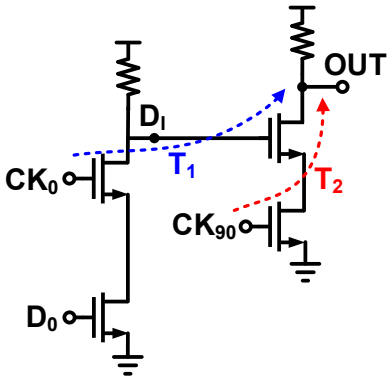


- T_1: Delay from CK_0 (CK_{180}) to OUT
- T_2: Delay from CK_{90} (CK_{270}) to OUT
- $T_1 \neq T_2 \rightarrow$ Duty Cycle Distortion of the Output

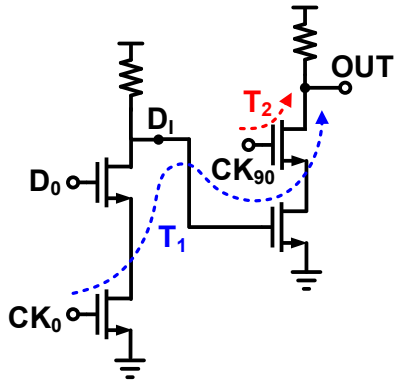
4-to-1 Multiplexer (MUX)



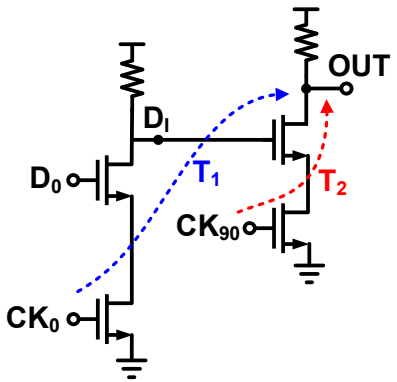
☹ Clock Up-Clock Up
($T_1 > T_2$)



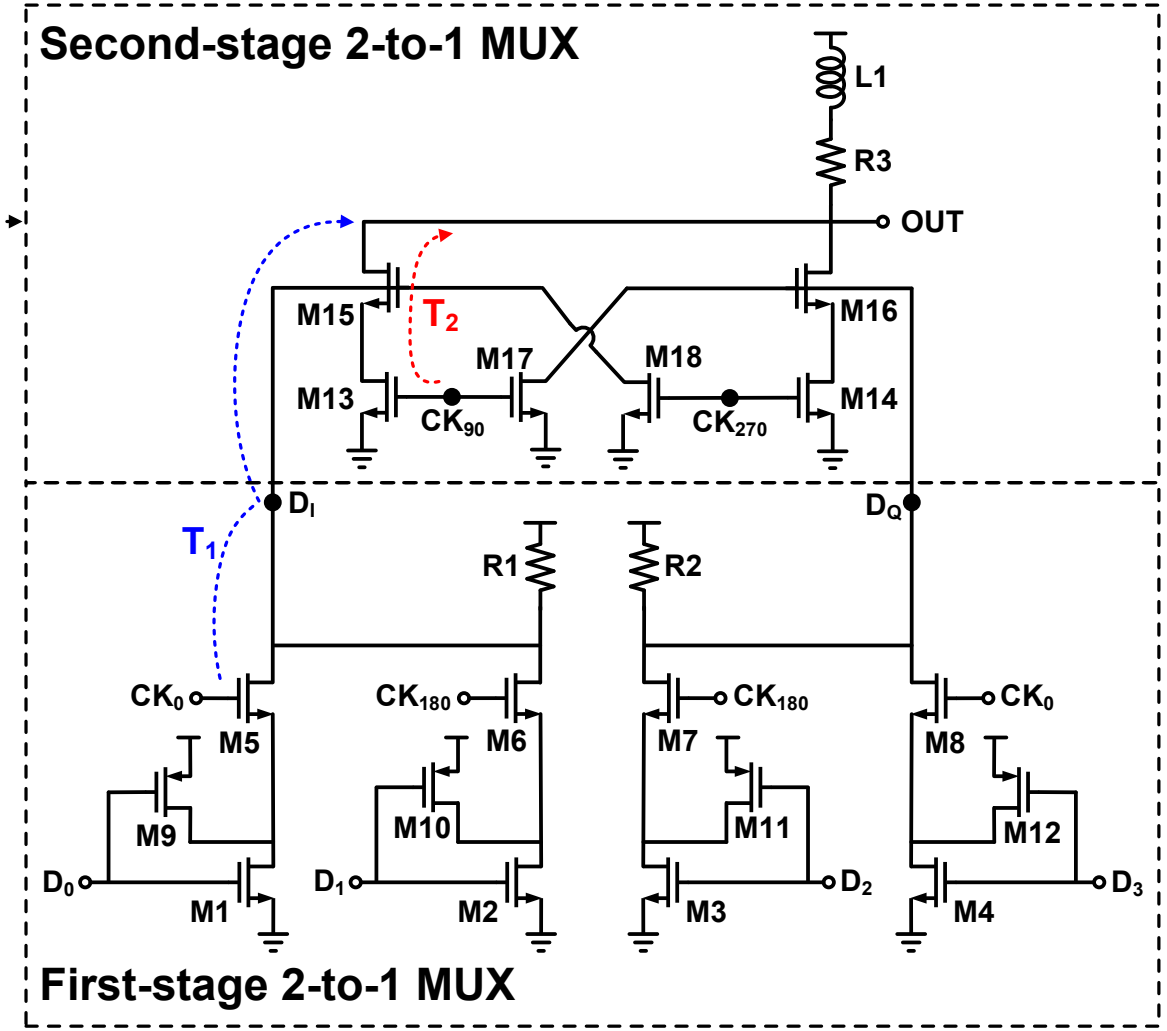
☺ Clock Up-Clock Down
($T_1 \approx T_2$)



☹ Clock Down-Clock Up
($T_1 >> T_2$)



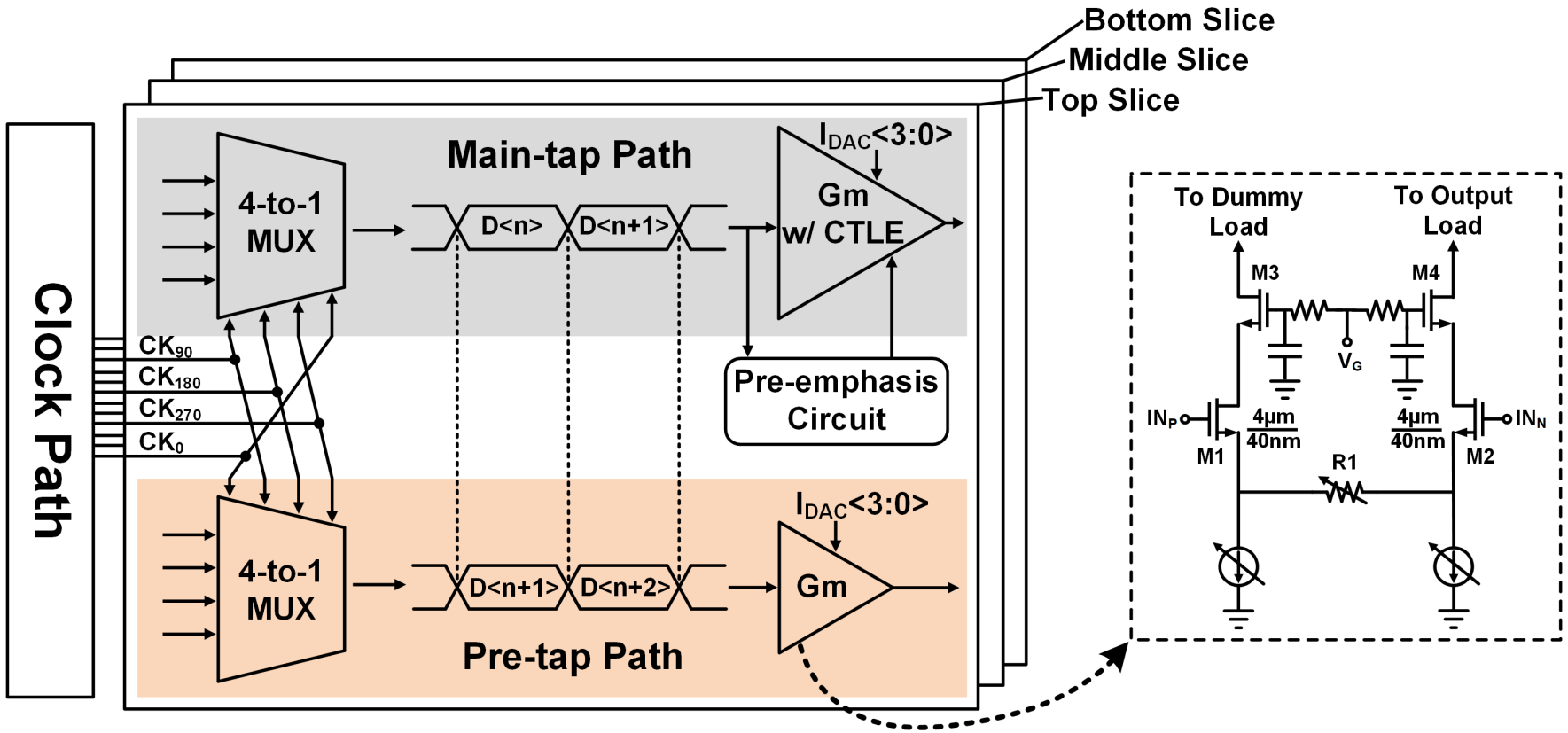
☹ Clock Down-Clock Down
($T_1 > T_2$)



Output Driver

Design of Pre-tap Gm Cell

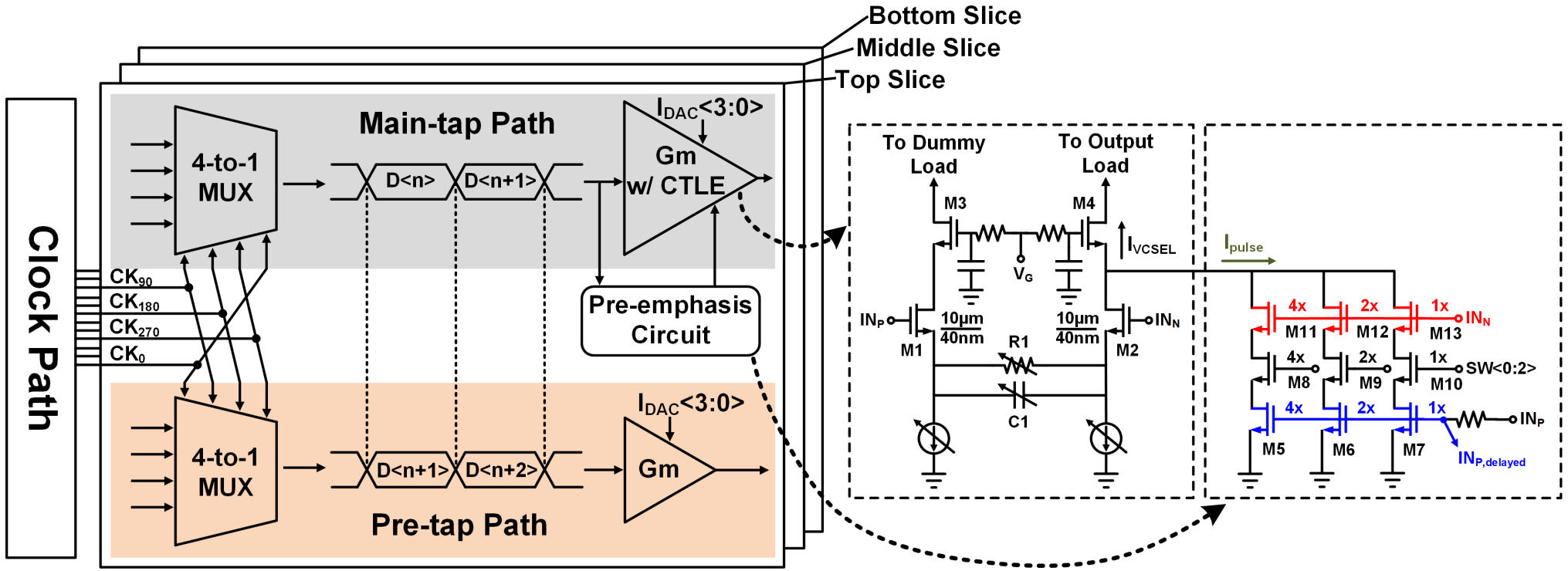
- Cascode structure for preventing breakdown issue
- Tunable tail current source for gain adjustment



Output Driver

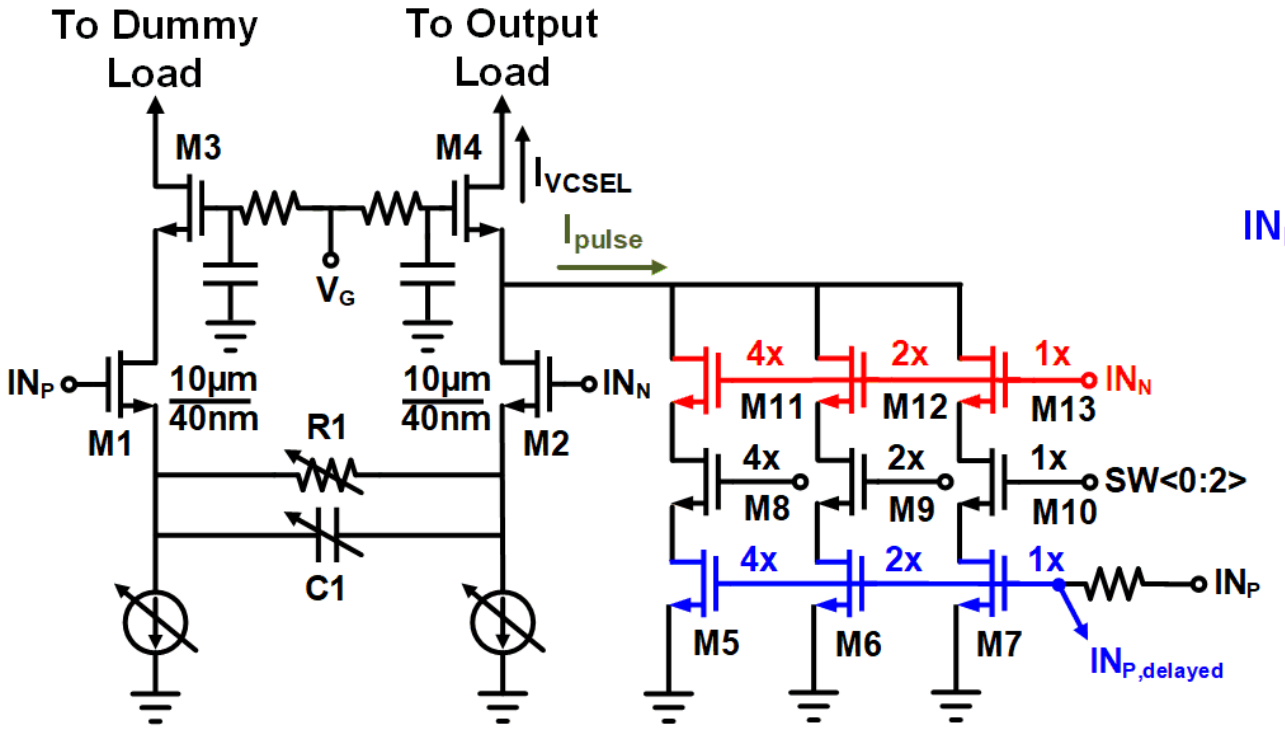
Design of Main-tap Gm Cell

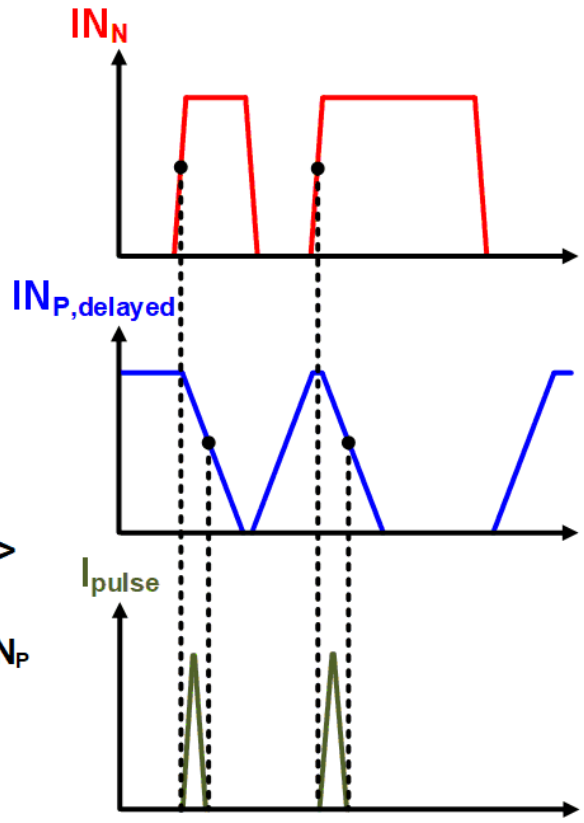
- Transistors size 2.5 times larger than pre-tap Gm cell
- Source-degenerated capacitor for BW extension
- Pre-emphasis circuit for mitigating optical eye skew



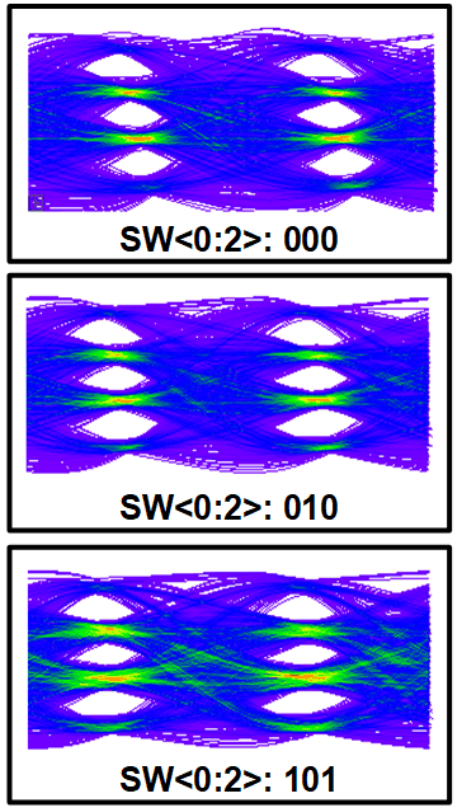
Output Driver

- $IN_N \uparrow \rightarrow I_{VCSEL} \downarrow \rightarrow IN_N$ & $IN_{P,delayed}$ both high → A sharp current pulse I_{pulse} generated

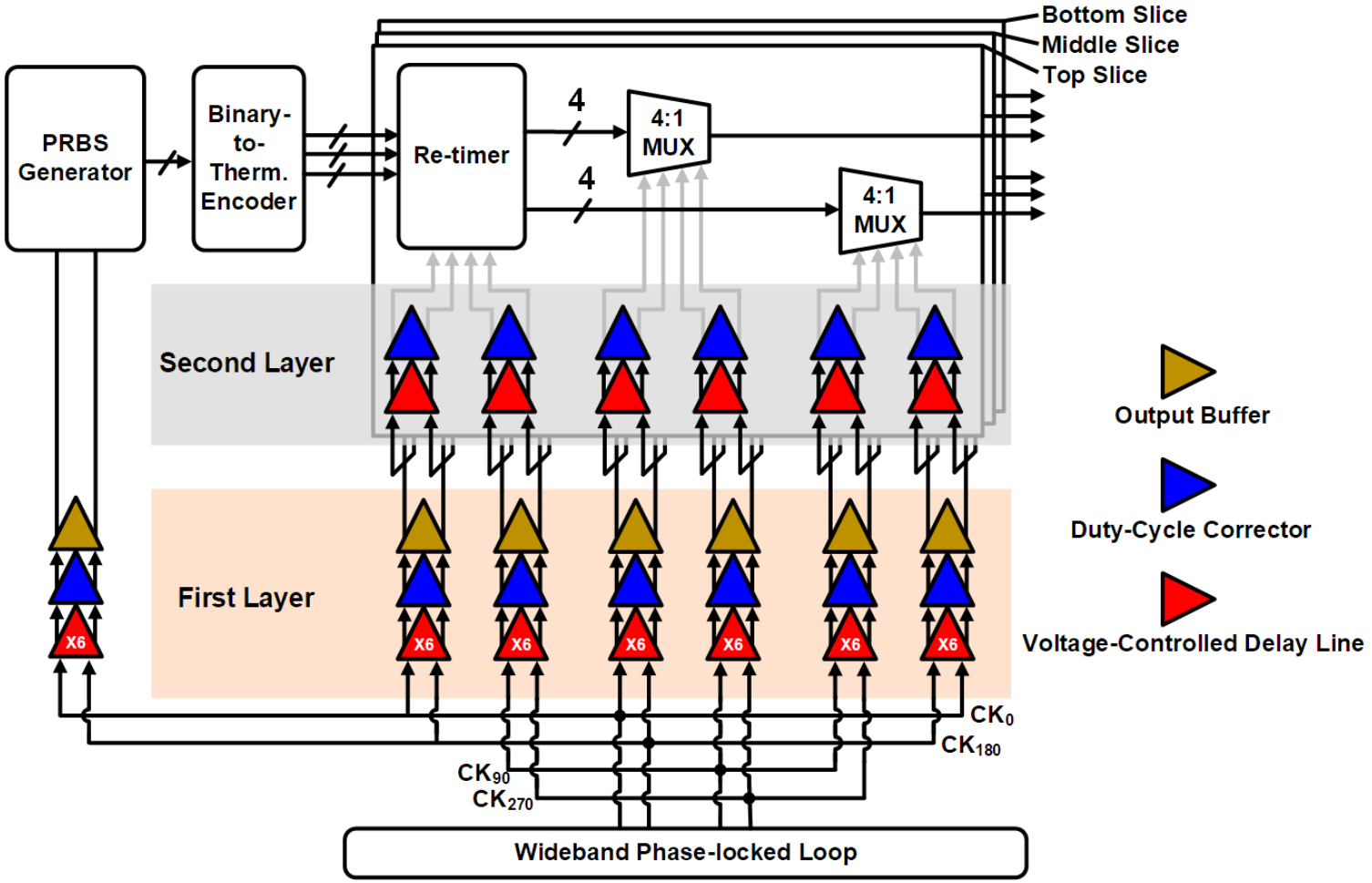




Simulated Optical Eye Diagrams



Clock Tree



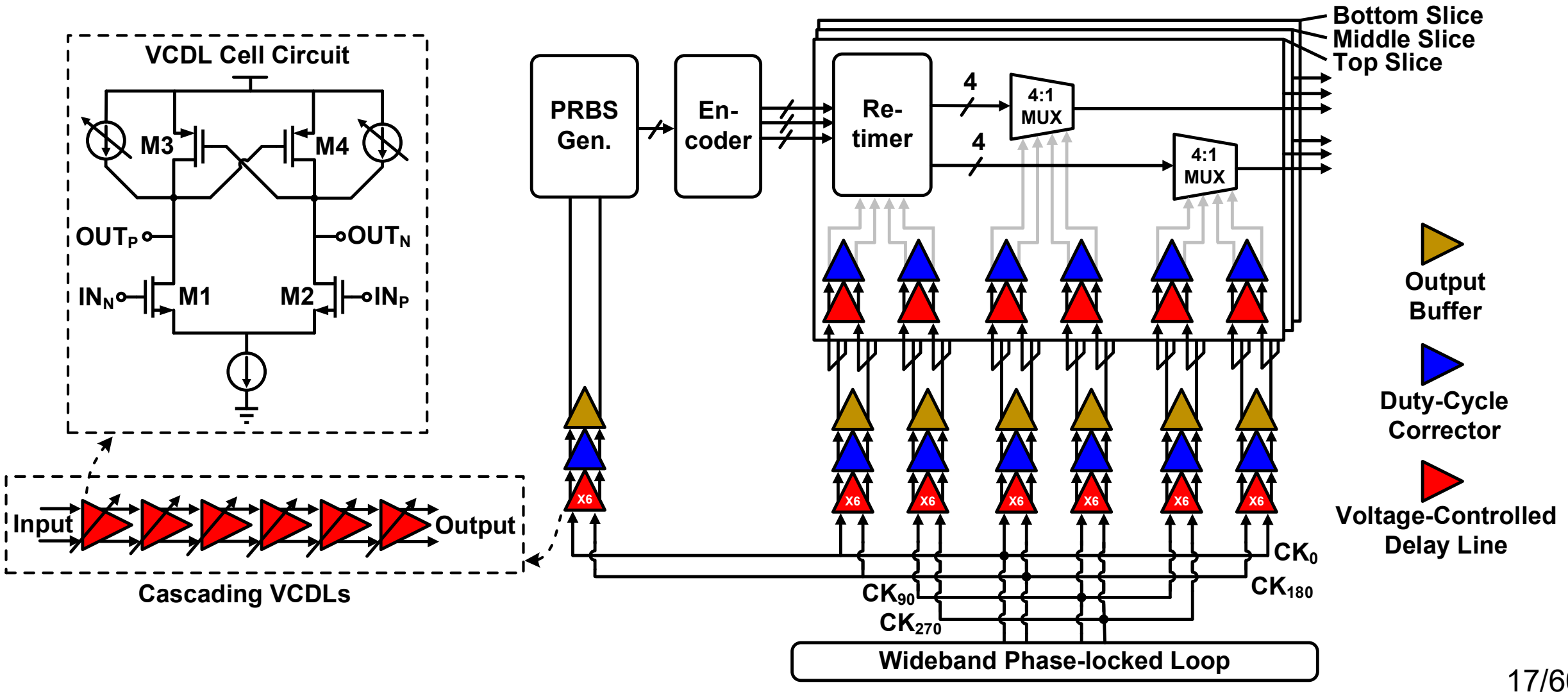
1st-Layer Clock Tree

- Aligns the timing between the PRBS generator, re-timer and 4-to-1 MUXs

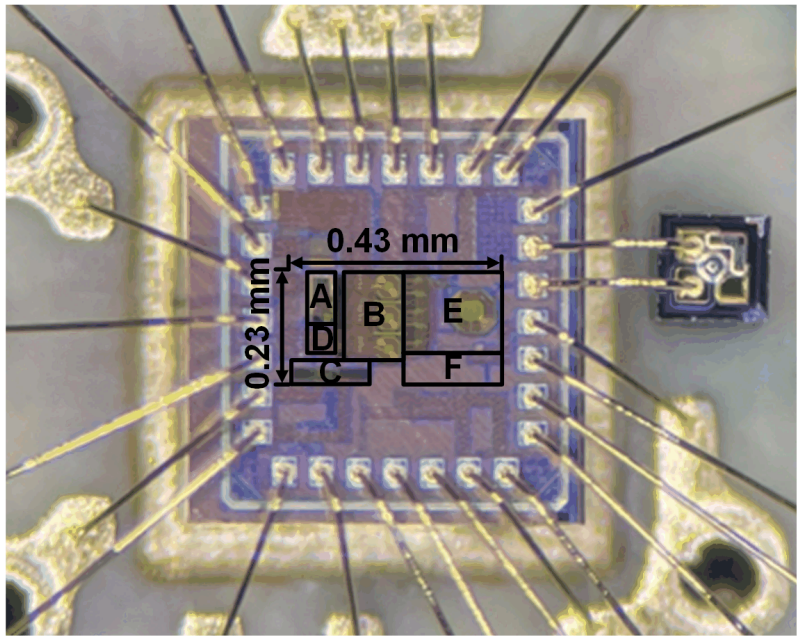
2nd-Layer Clock Tree

- Mitigates the timing skew between the three slices

Clock Tree

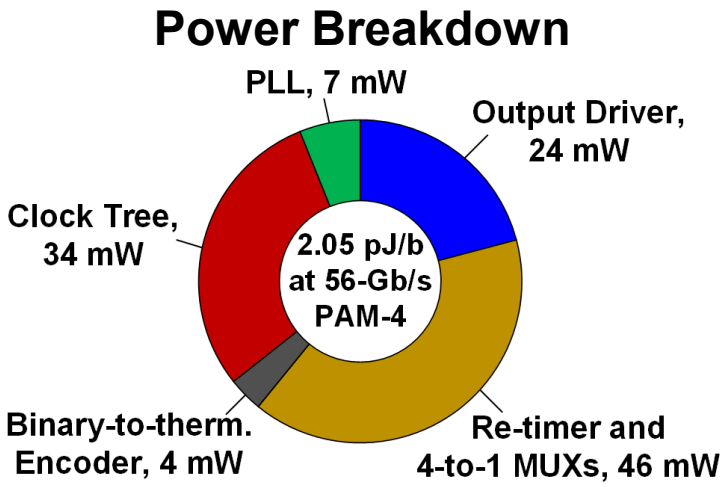

VCDL Cell Circuit
M3
M4
OUT_P
OUT_N
IN_N
M1
M2
IN_P
Input
Output
Cascading VCDLs
PRBS Gen.
En-coder
Re-timer
4
4
4:1 MUX
4:1 MUX
Bottom Slice
Middle Slice
Top Slice
X6
CK_0
CK_{180}
CK_{90}
CK_{270}
Wideband Phase-locked Loop
Output Buffer
Duty-Cycle Corrector
Voltage-Controlled Delay Line

Design Under Test



A — PRBS Generator + Binary-to-therm. Encoder
B — Re-timer + 4-to-1 Multiplexers
C — Phase-locked Loop
D — Clock Tree
E — Output Driver
F — Bias Circuit + I²C

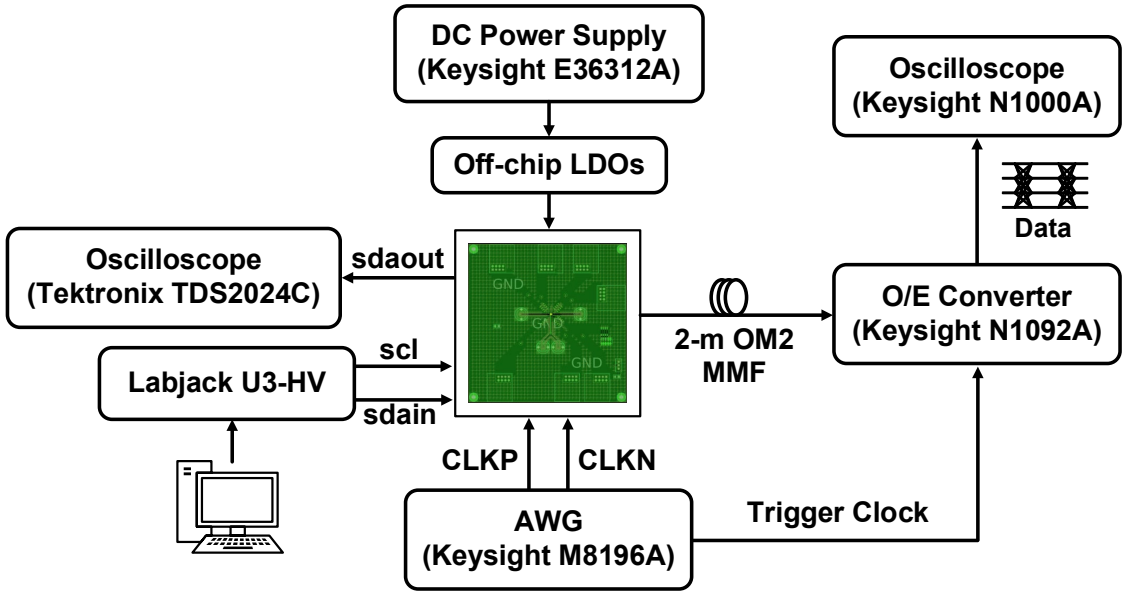
- Fabricated in 40-nm bulk CMOS
- Transmitter core occupies 0.1 mm^2
- Consumes 115 mW at 56-Gb/s PAM-4



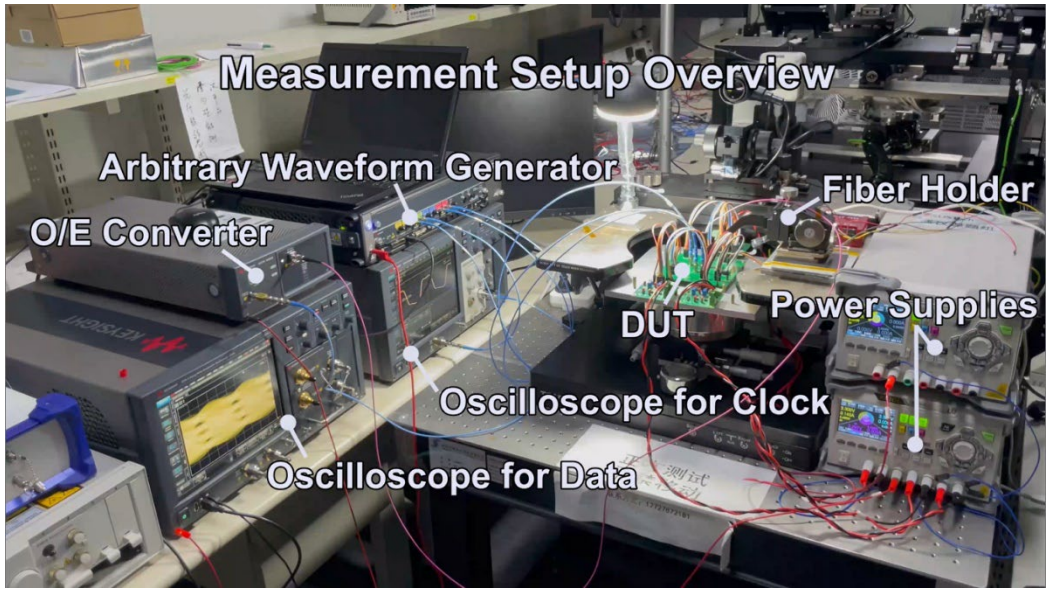
Measurement Setup

- A commercial VCSEL is wire-bonded with the transmitter for optical measurements
- The optical signal is butt-coupled to the multi-mode fiber

Scan to Visit Measurement Video

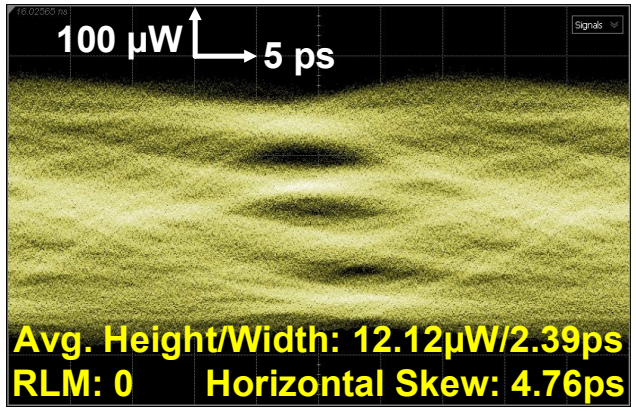


Measurement Setup

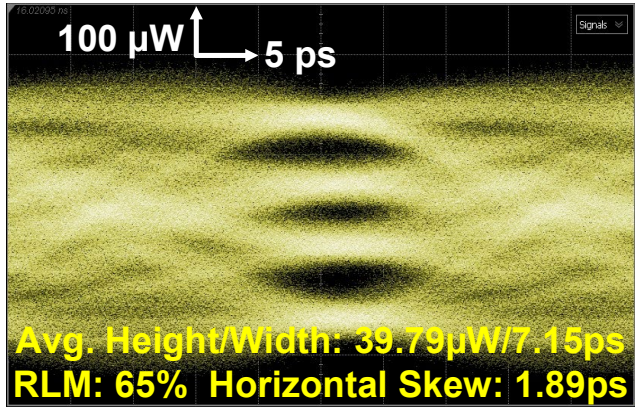


Measurement Environment

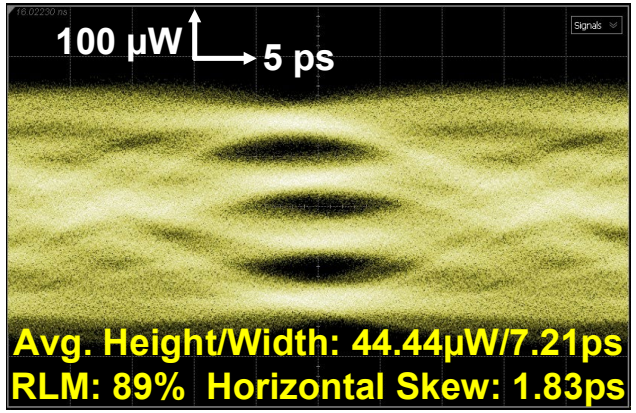
Measurement Results



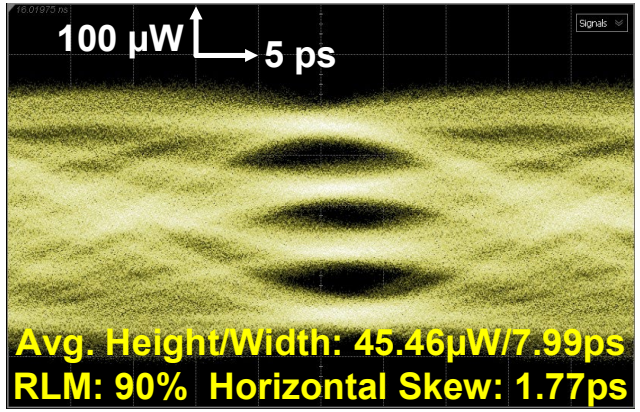
(a) EQ OFF, Equal Slice Gain



(b) EQ ON, Equal Slice EQ, Equal Slice Gain

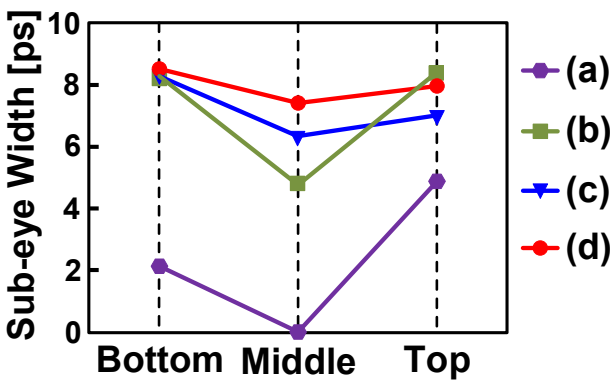


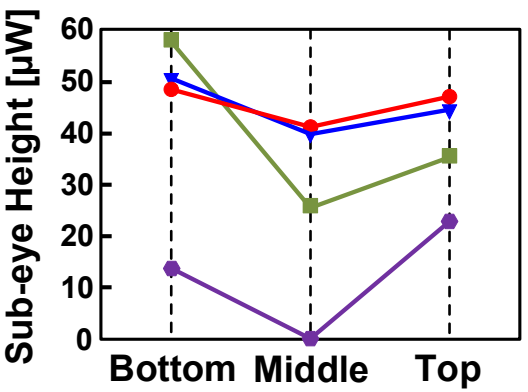
(c) EQ ON, Equal Slice EQ, Piecewise Tuned Slice Gain



(d) EQ ON, Piecewise Tunned Slice EQ and Slice Gain

	(a)	(b)	(c)	(d)
Average Sub-Eye Height [μW]	12.12	39.79	44.44	45.46
Average Sub-Eye Width [ps]	2.39	7.15	7.21	7.99
Ratio-of-Level Mismatch	0	65%	89%	90%
Horizontal Skew [ps]	4.76	1.89	1.83	1.77





Comparison with Prior Works

	[2] PTL'18	[3] JSSC'22	[4] VLSI'19	[5] ASSCC'21	[1] This work
CMOS Node [nm]	65	40	65	40	40
Architecture Signaling Scheme	1/2-rate PAM-4	1/4-rate PAM-4	1/4-rate PAM-4	1/4-rate PAM-4	1/4-rate PAM-4
Data Rate [Gbps]	50	56	64	64	56
OMA [mW]	2.00	0.81*	2.50*	1.08*	1.18*
Power effi. [pJ/b]	5.12	1.73	2.69#	2.09	**2.05#**
Core Area [mm^2]	0.31	0.47	0.28	0.16	**0.10**
Asymmetric Equalization	2.5-tap DAC-based FFE	2-tap DAC-based FFE	3-tap LSB/MSB-based Asymmetric FFE	3-tap LSB/MSB-based Asymmetric FFE	2-tap FFE + CTLE + Pre-emphasis
Imperfection Compensation	Full	Full	Partial	Partial	**Full**
Method Type	Digital	Digital	Analog	Analog	**Mixed-signal**

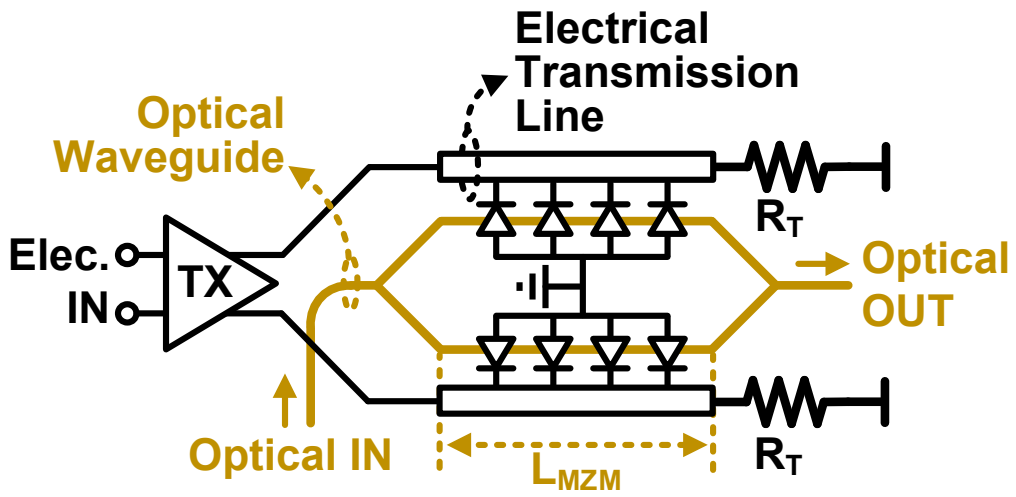
*3-dB butt coupling loss de-embedded [6]
#Includes on-chip PLL

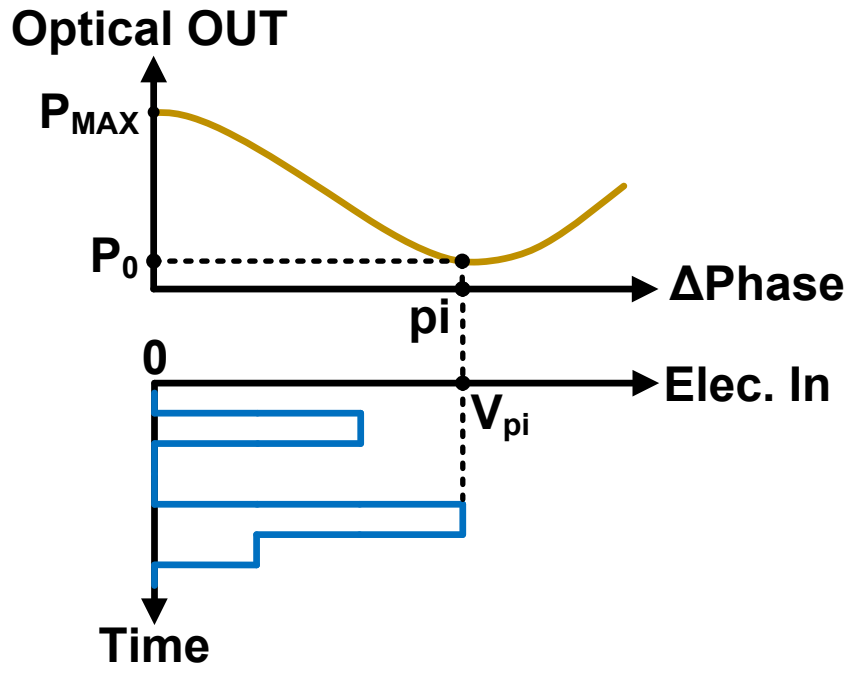
Outline

- Background
- Transmitter Design for VCSEL-based Optical Links
  - Imperfections of VCSEL
  - Implementation and Measurement of A 56-Gb/s PAM-4 VCSEL Transmitter
- **Transmitter Design for Optical Modulator-based Optical Links**
  - **Design Challenges**
  - Implementation and Measurement of A 56-Gbaud Linear Modulator Transmitterr
  - Implementation and Measurement of A 100-Gbaud Linear Modulator Driver
- Conclusions

Design Challenges for Modulator TX

- **Large output swing** for high optical extinction ratio
- **High linearity** to support advanced modulation schemes for high data rate
- **High bandwidth** to increase the link speed
- **Equalization** to compensate for high-frequency loss from E/E and E/O interfaces

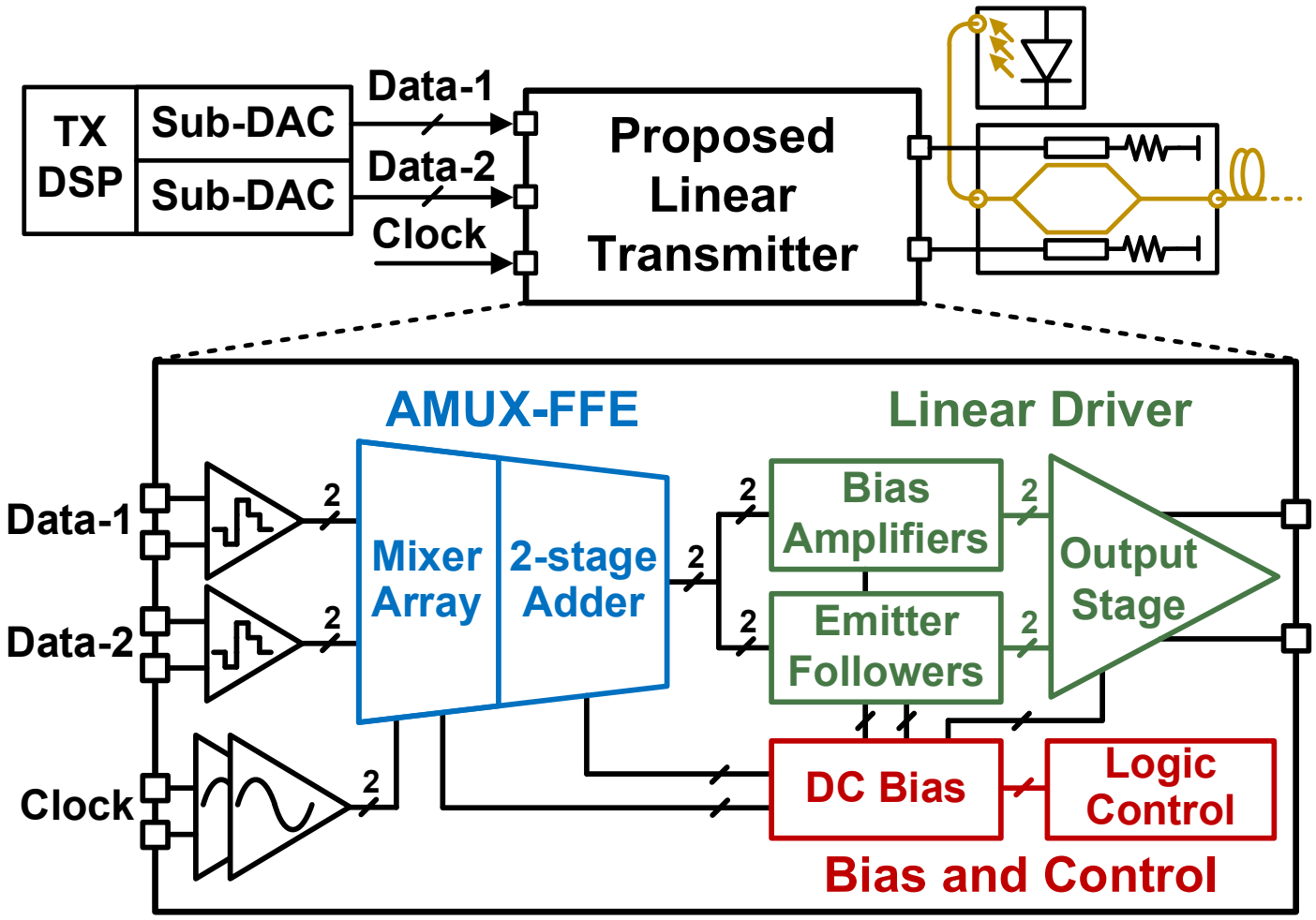




Outline

- Background
- Transmitter Design for VCSEL-based Optical Links
  - Imperfections of VCSEL
  - Implementation and Measurement of A 56-Gb/s PAM-4 VCSEL Transmitter
- **Transmitter Design for Optical Modulator-based Optical Links**
  - Design Challenges
  - **Implementation and Measurement of A 56-Gbaud Linear Modulator Transmitter**
  - Implementation and Measurement of A 100-Gbaud Linear Modulator Driver
- Conclusions

Architecture Design



AMUX-FFE

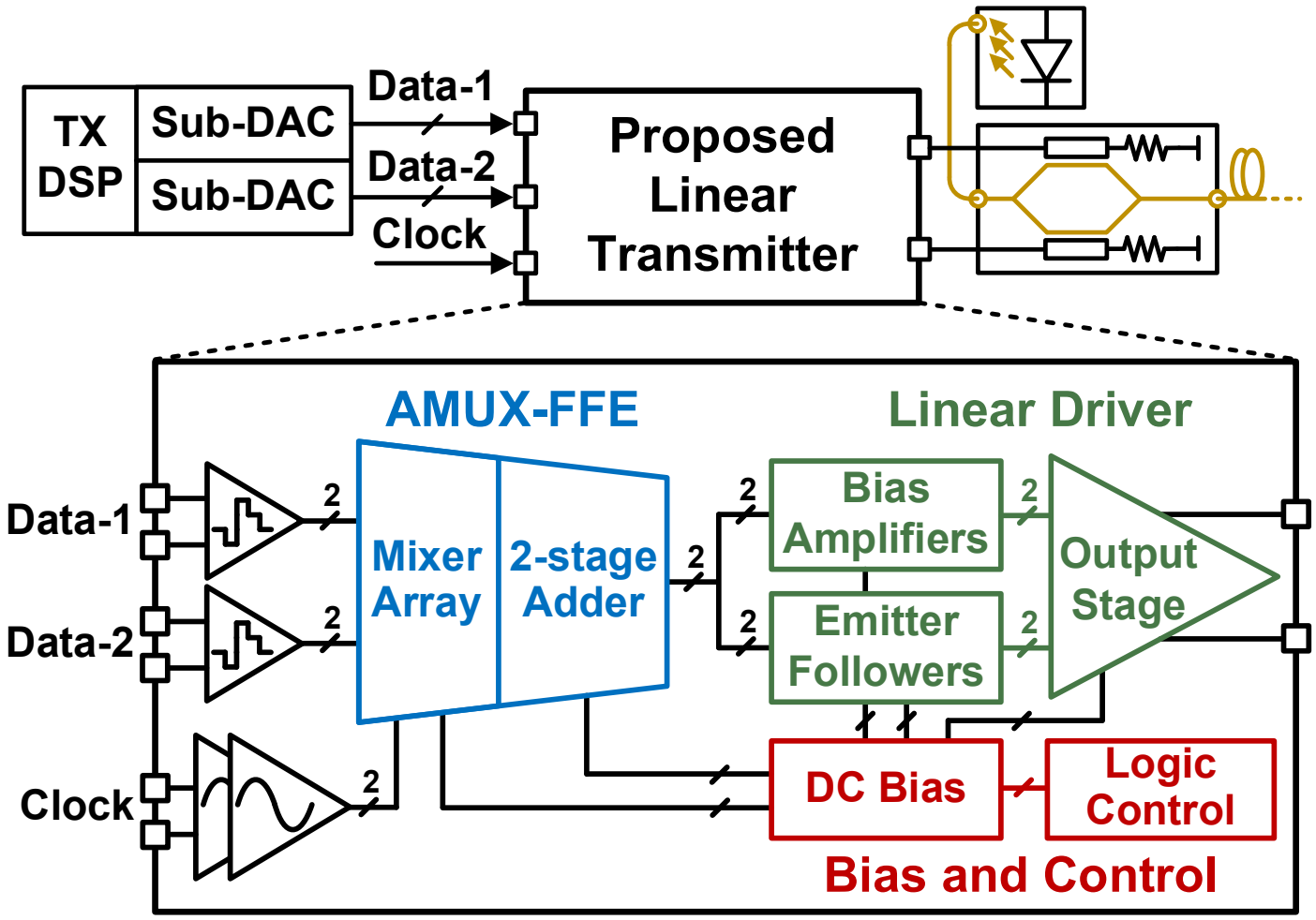
Analog serialization

- Serializes analog data streams from half rate to full rate

Equalization

- Generates equalized signal with a re-configurable FFE
- No tap generator required to save power

Architecture Design



Linear Driver

Large output swing

- Adopts a **dynamic triple-stacked (DTS) topology** to achieve large output swing without breakdown

High linearity

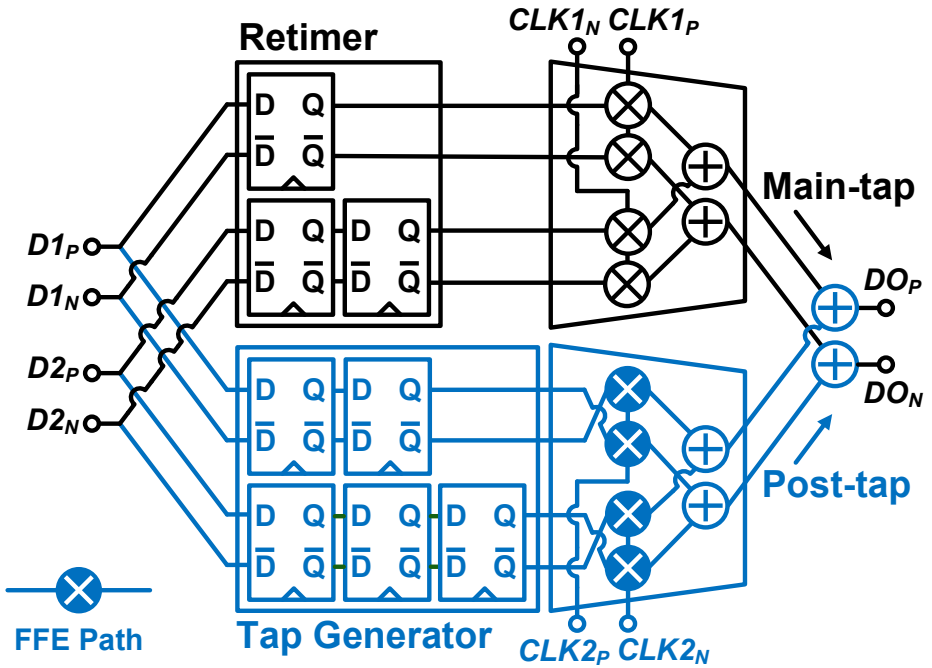
- The DTS topology also provides high linearity by decreasing V_{CE} variations of HBTs

Comparison btw Conv. and Prop. AMUX-FFEs

Conventional AMUX-FFE

Uses latches to generate FFE tap

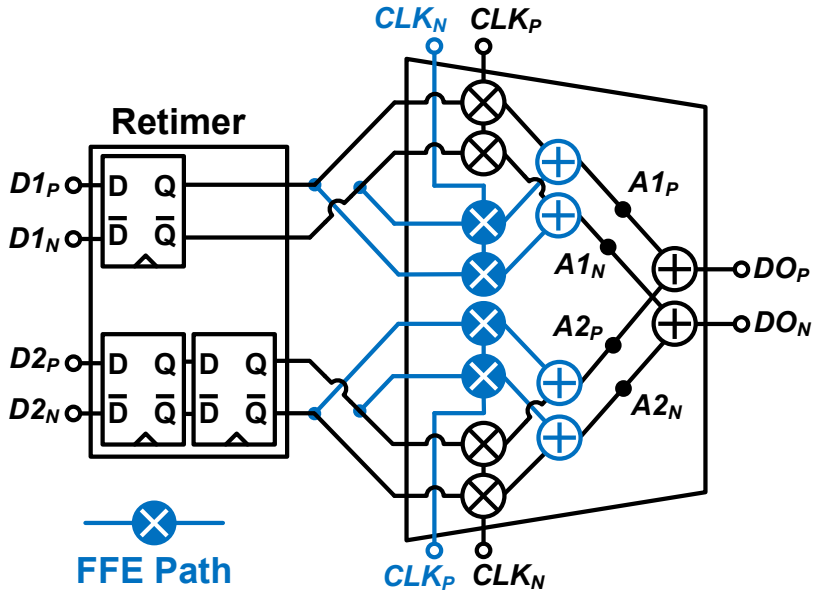
- High hardware & power overhead ☹
- Bad re-configurability ☹



Proposed AMUX-FFE

Uses re-timed differential data streams to generate FFE tap

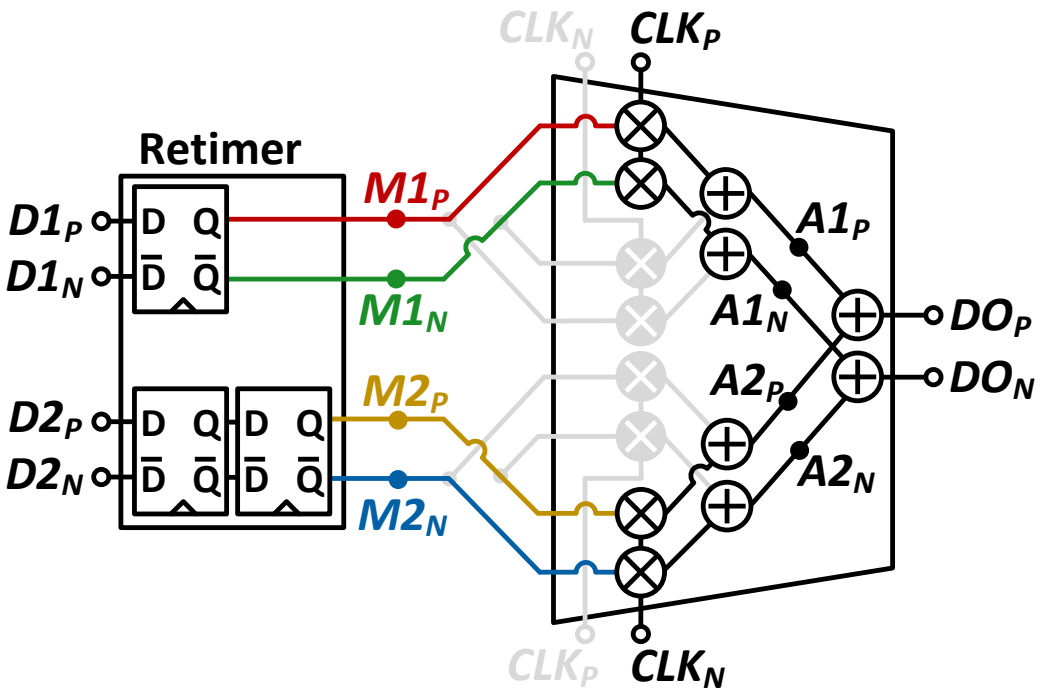
- Low hardware & power overhead ☺
- Good re-configurability ☺

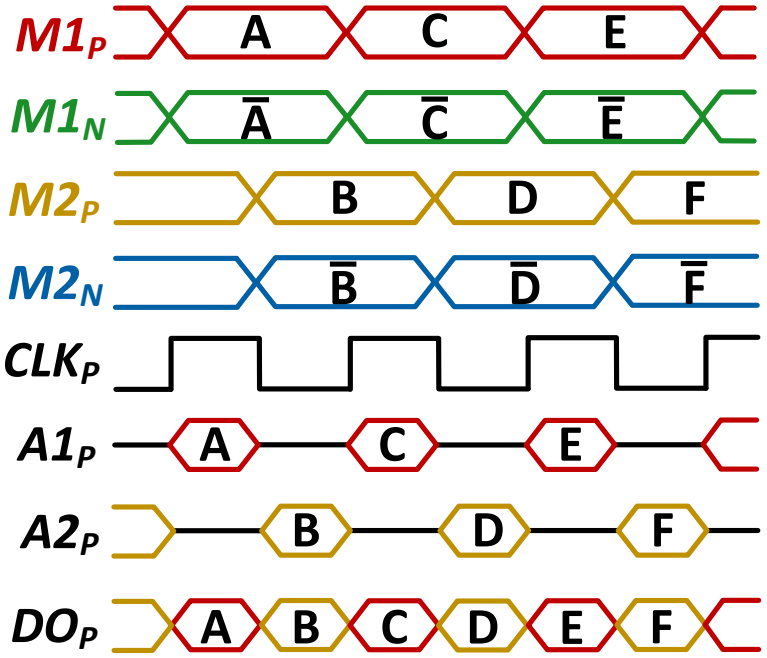


Principle of the AMUX-FFE

CONFIG-1: FFE Turned OFF

When mixers of four FFE paths are turned off, the AMUX functions as a normal 2-to-1 serializer

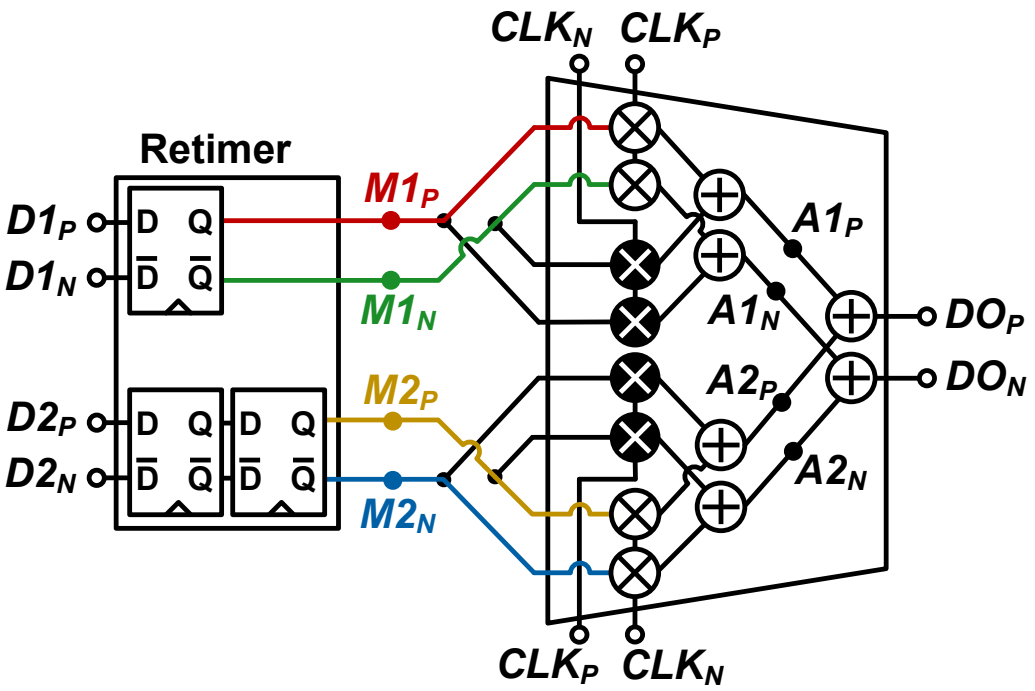


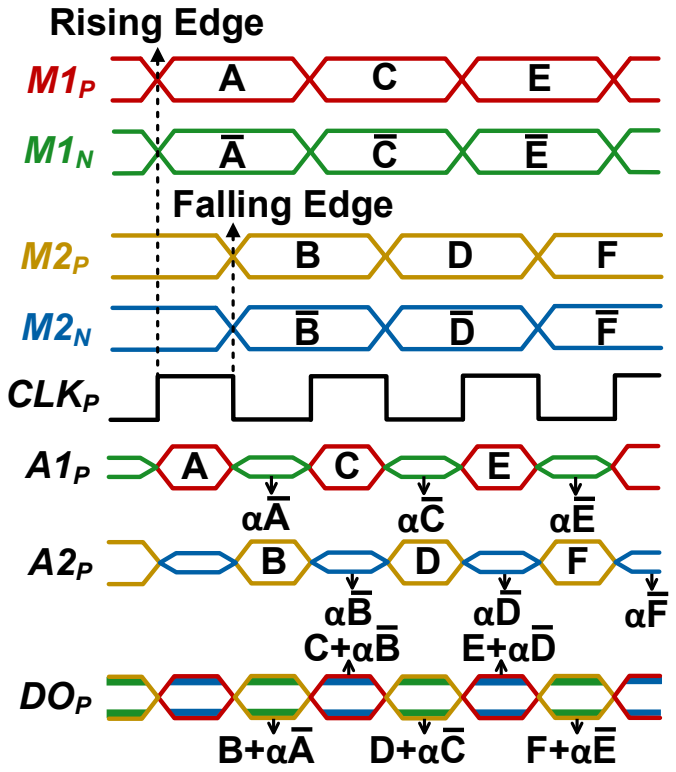


Principle of the AMUX-FFE

CONFIG-2:
1 Main + 1 Post

DO_P is the same with the output of a FFE with 1 main tap and 1 post-tap, tap spacing = 1 UI

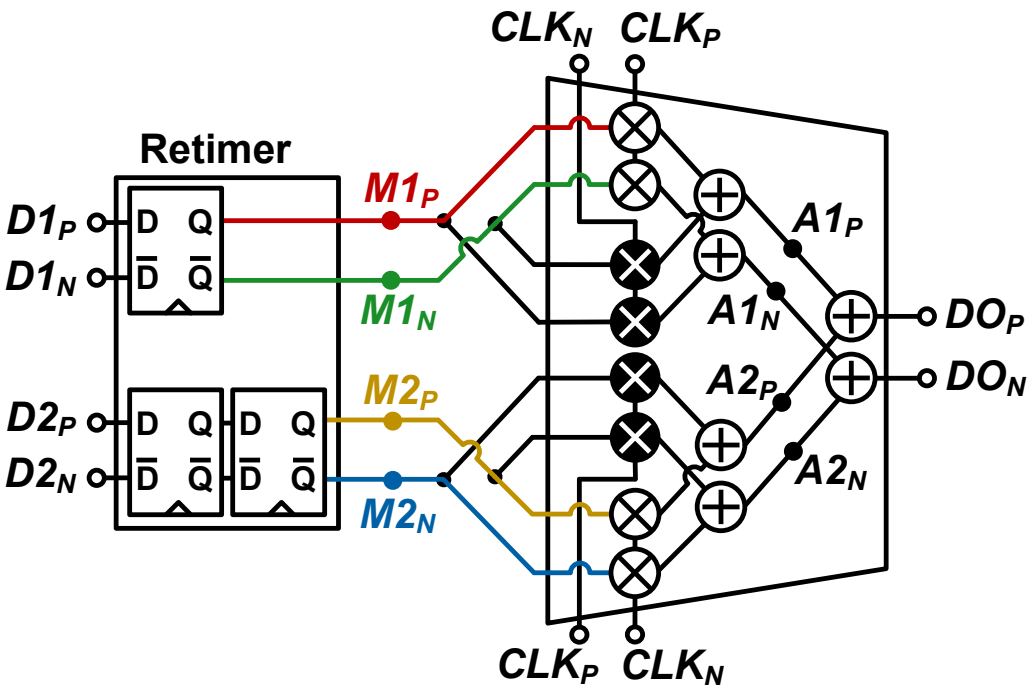


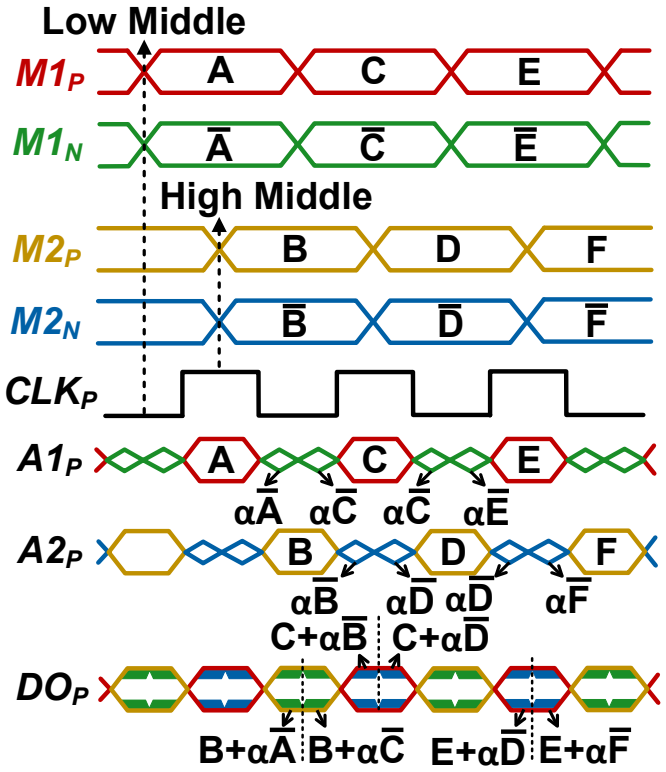


Principle of the AMUX-FFE

CONFIG-3:
1 Main + 1 Pre + 1 Post

DO_P is the same with the output of a FFE with 1 pre-tap, 1 main tap and 1 post-tap, tap spacing = 0.5 UI

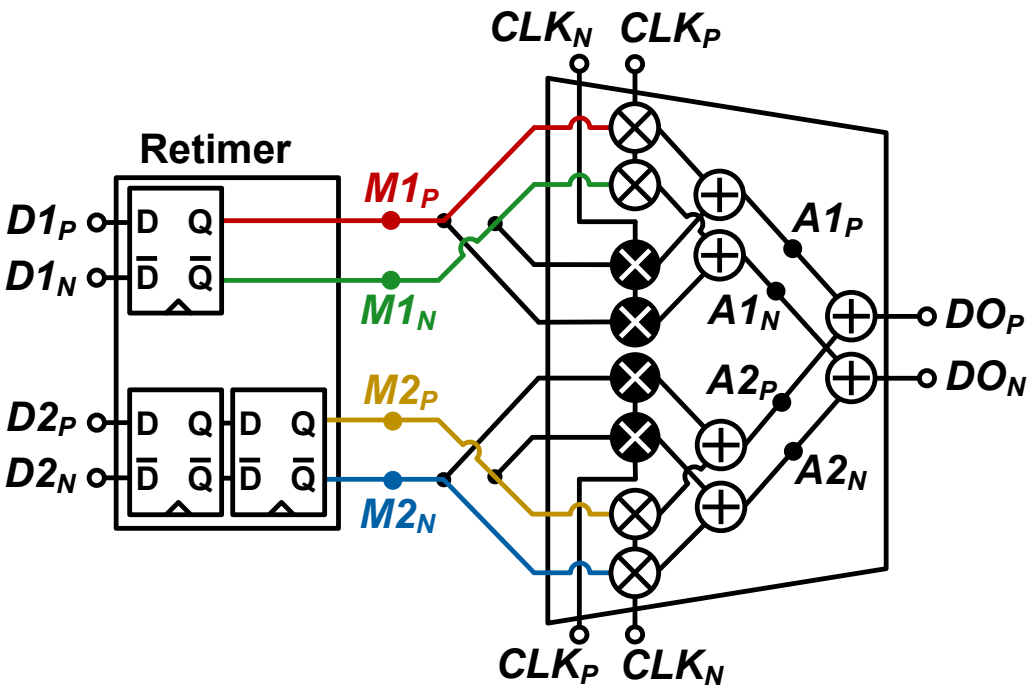


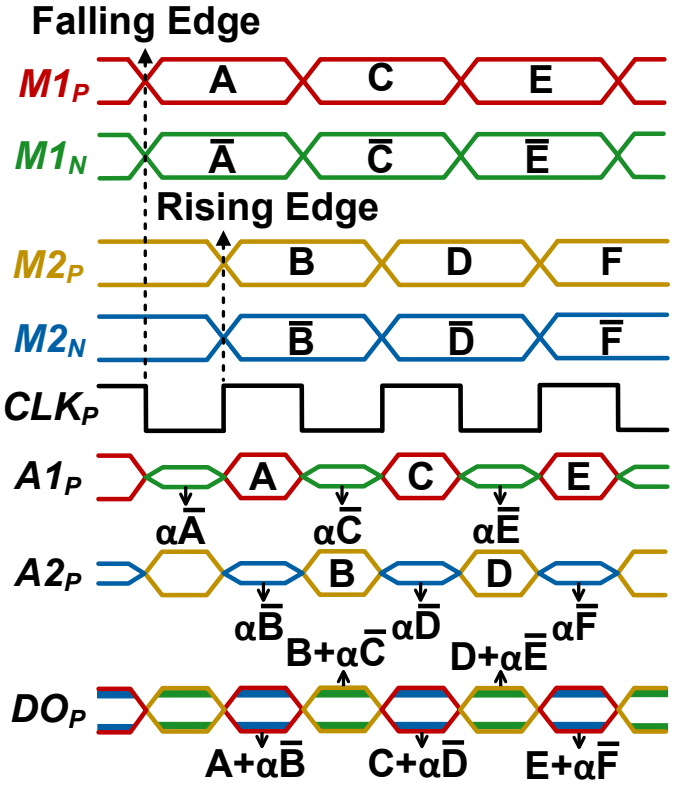


Principle of the AMUX-FFE

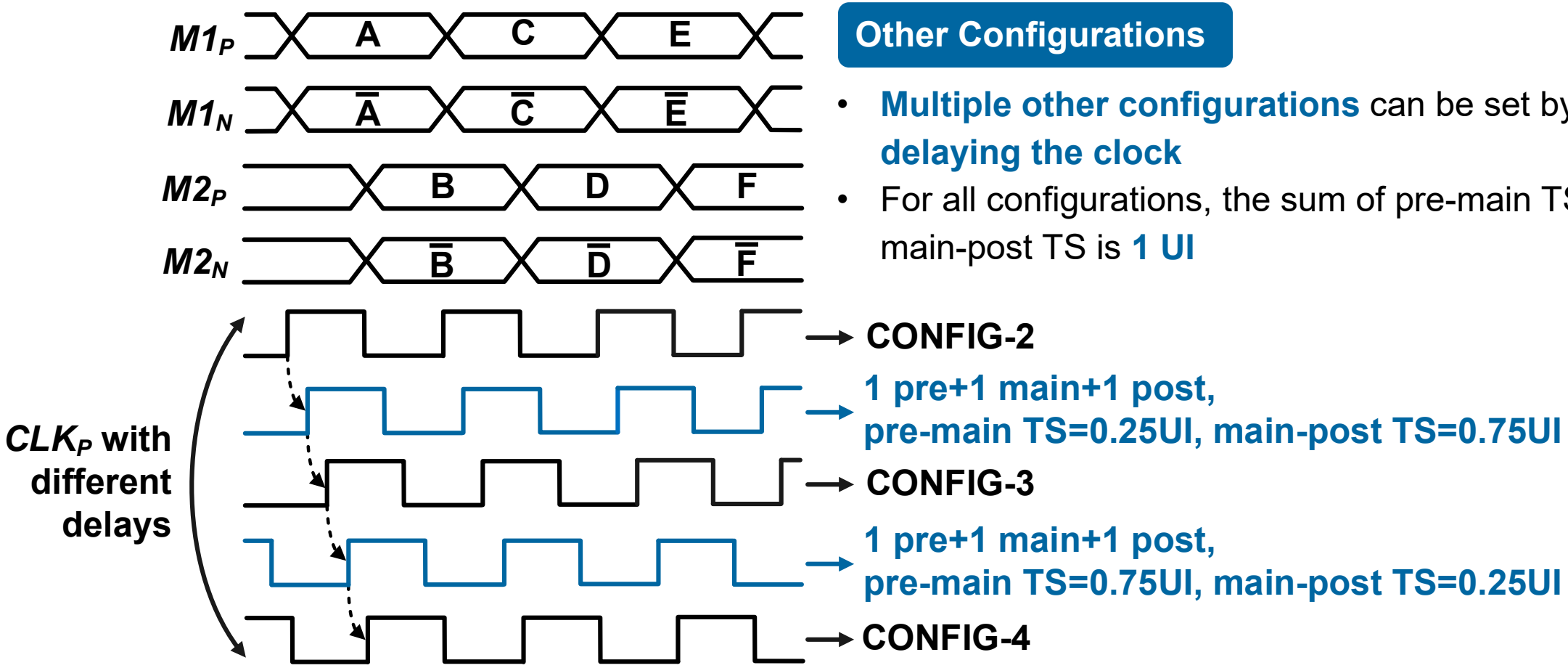
CONFIG-4:
1 Main + 1 Pre

DO_P is the same with the output of a FFE with 1 pre-tap and 1 main tap, tap spacing = 1 UI





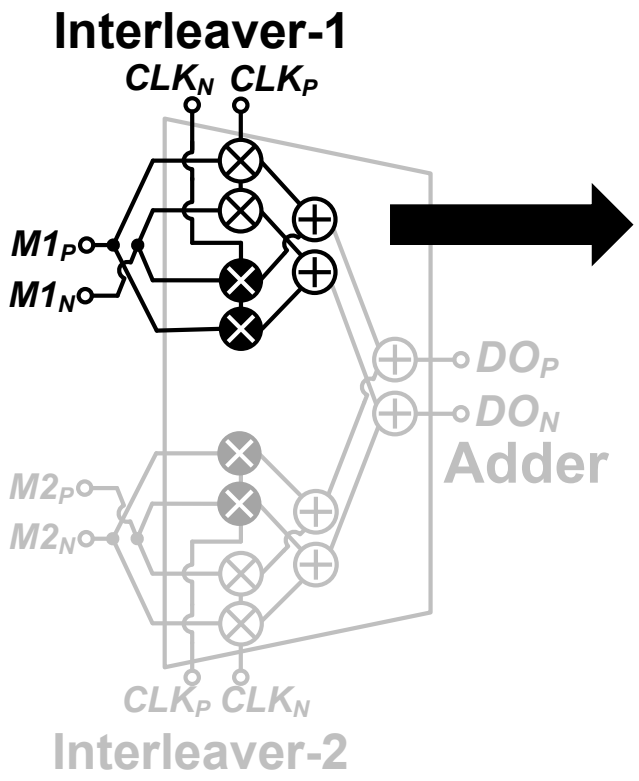
Principle of the AMUX-FFE

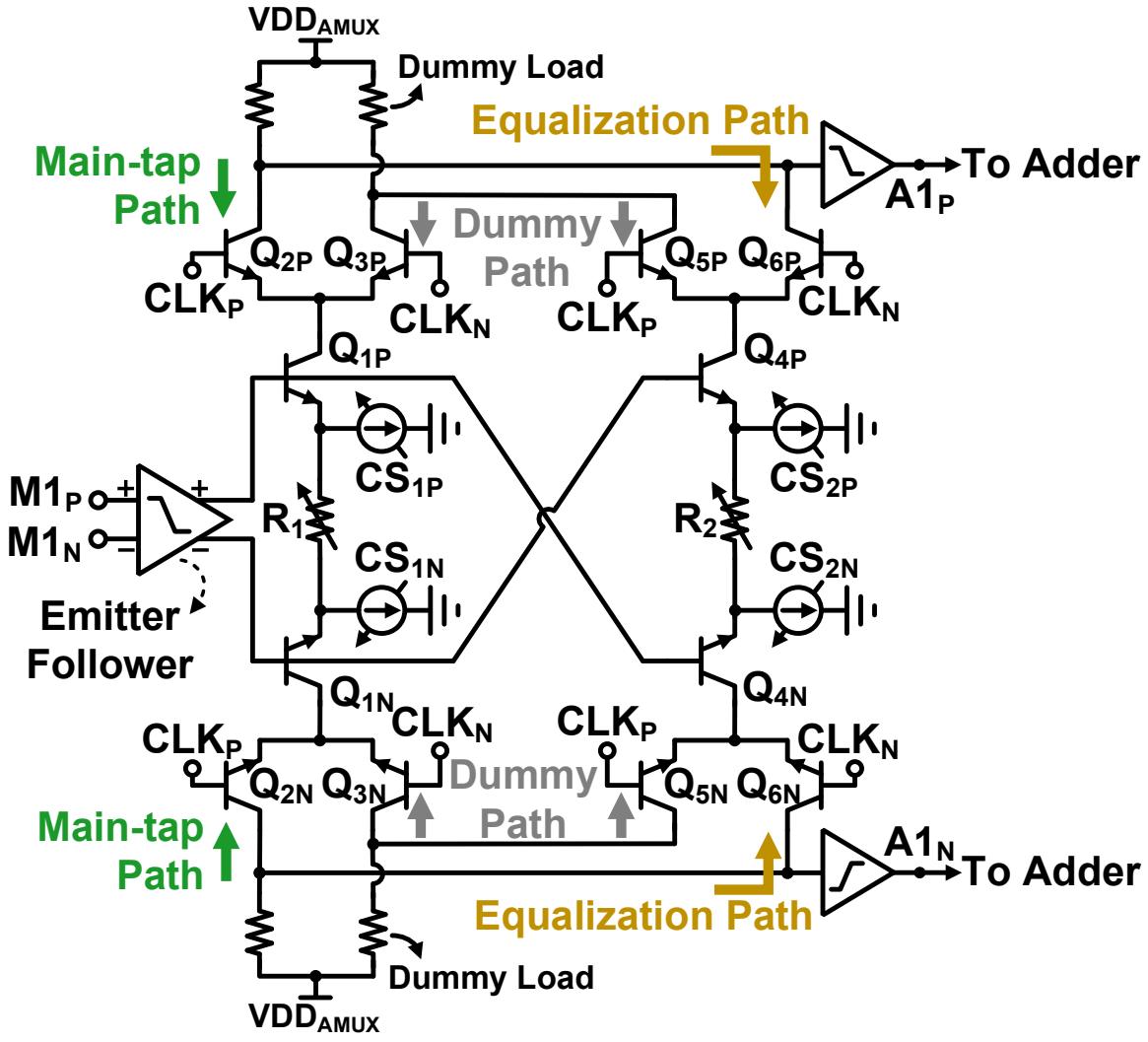


Other Configurations

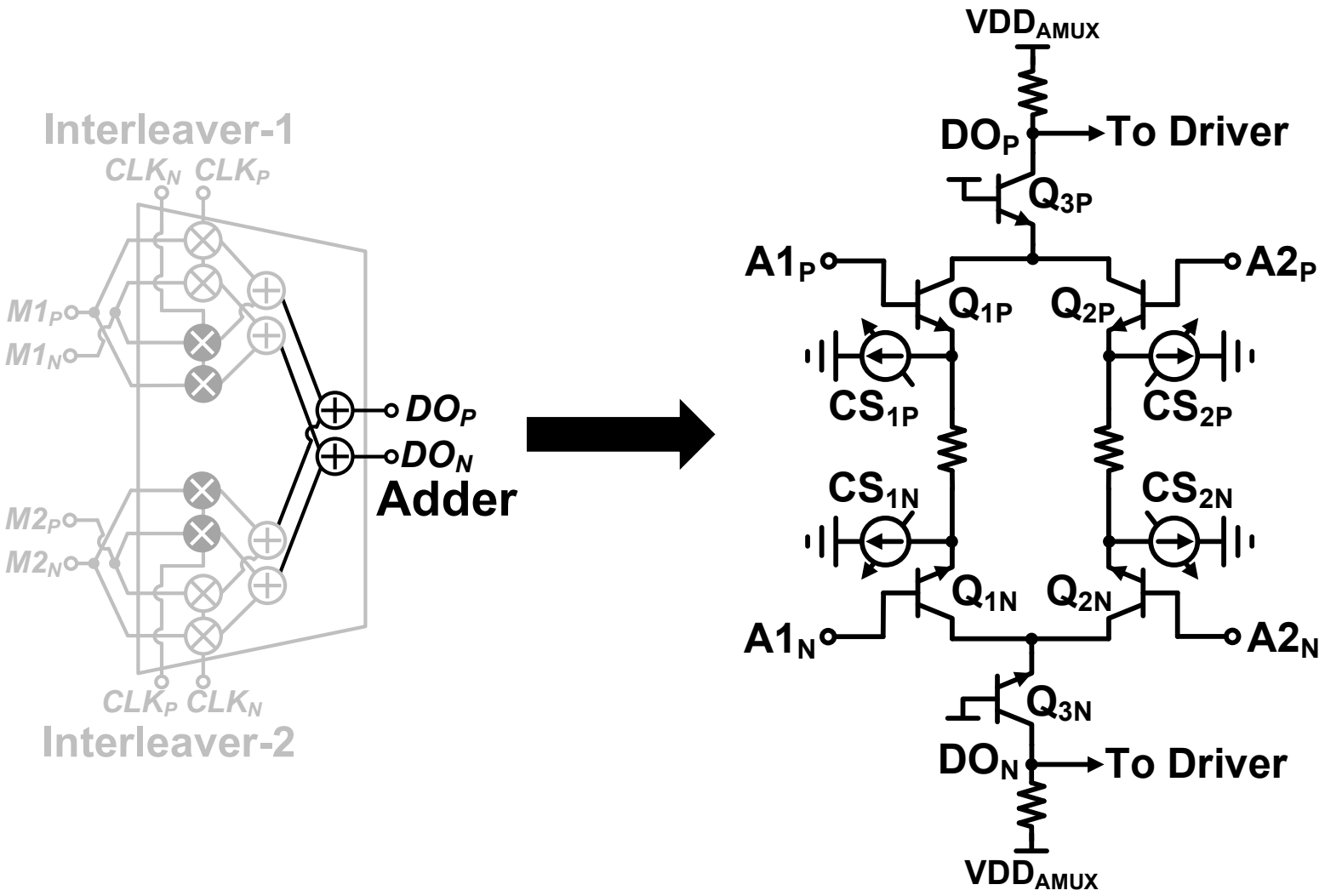
- **Multiple other configurations** can be set by simply **delaying the clock**
- For all configurations, the sum of pre-main TS and main-post TS is **1 UI**

Schematic of the AMUX-FFE





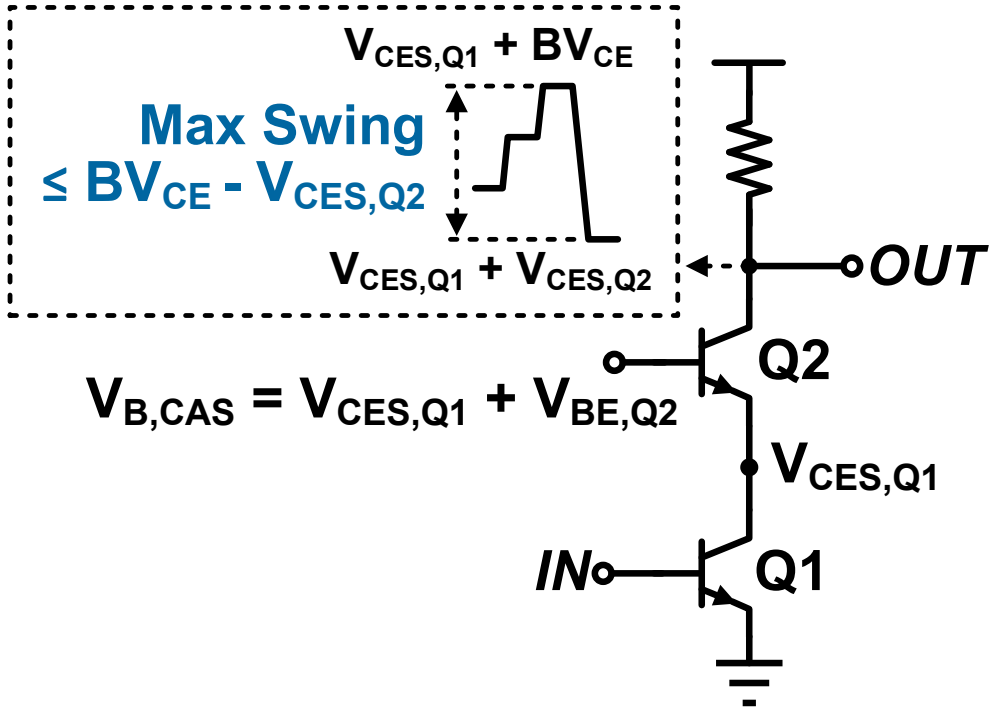
Schematic of the AMUX-FFE



Comparison Between Driver Topologies

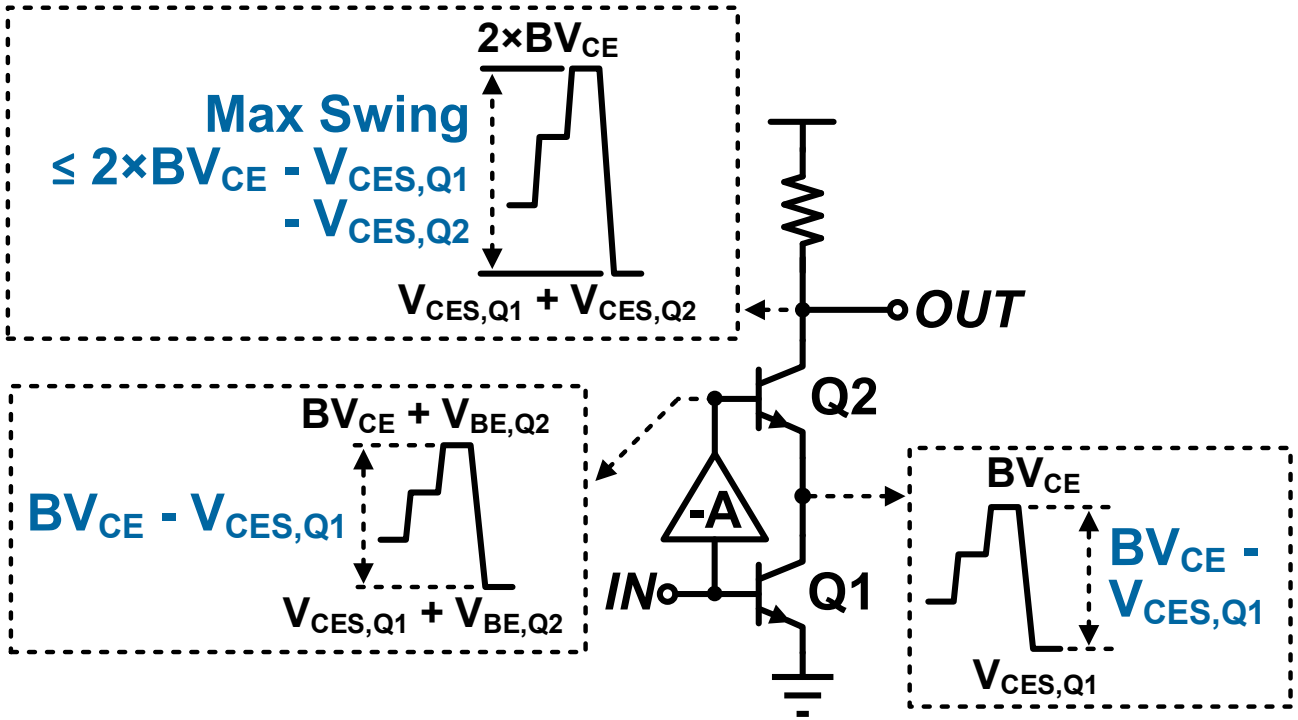
Conventional Cascode

Limited output voltage swing



Breakdown Voltage (BV) Doubler

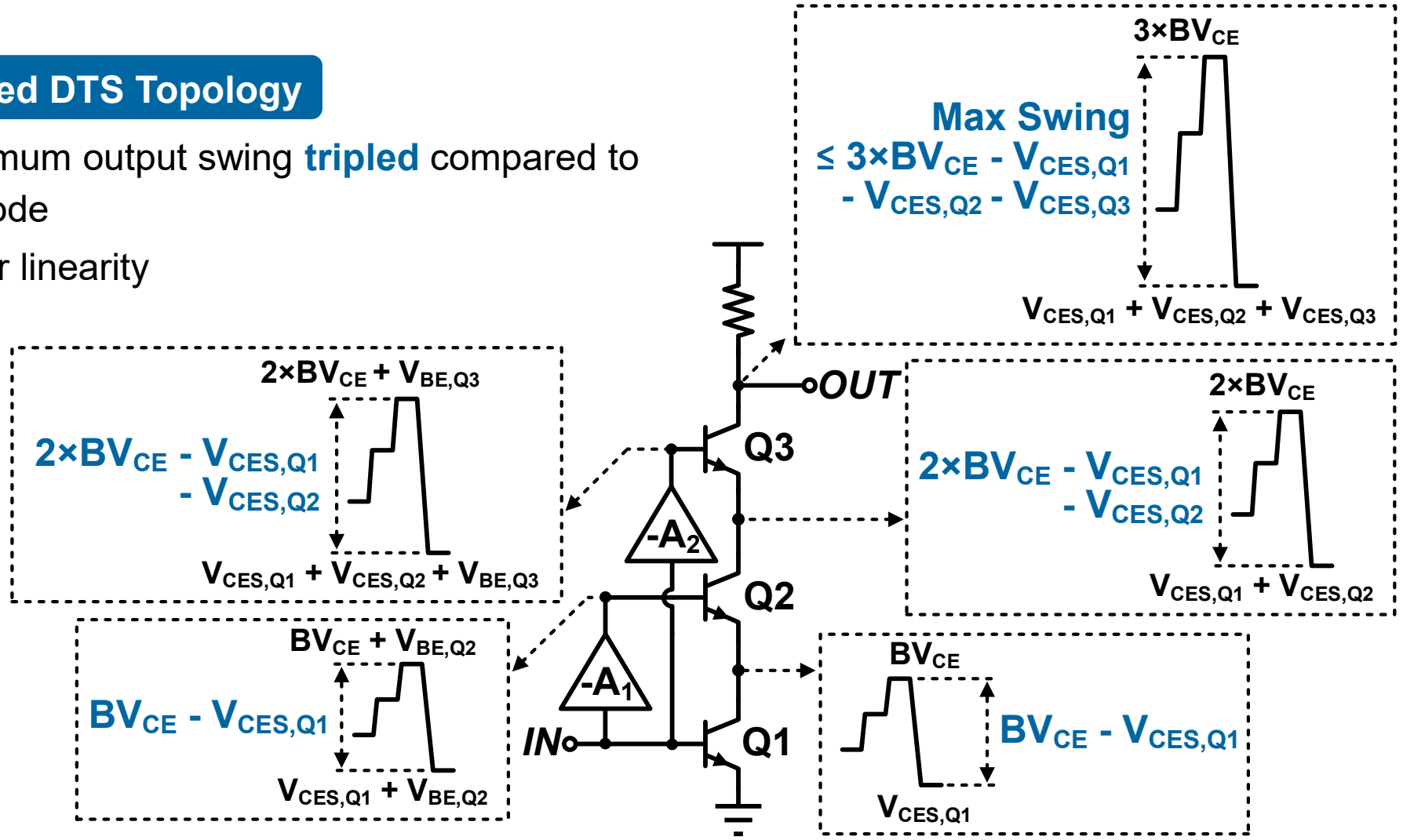
Maximum output swing doubled



Comparison Between Driver Topologies

Proposed DTS Topology

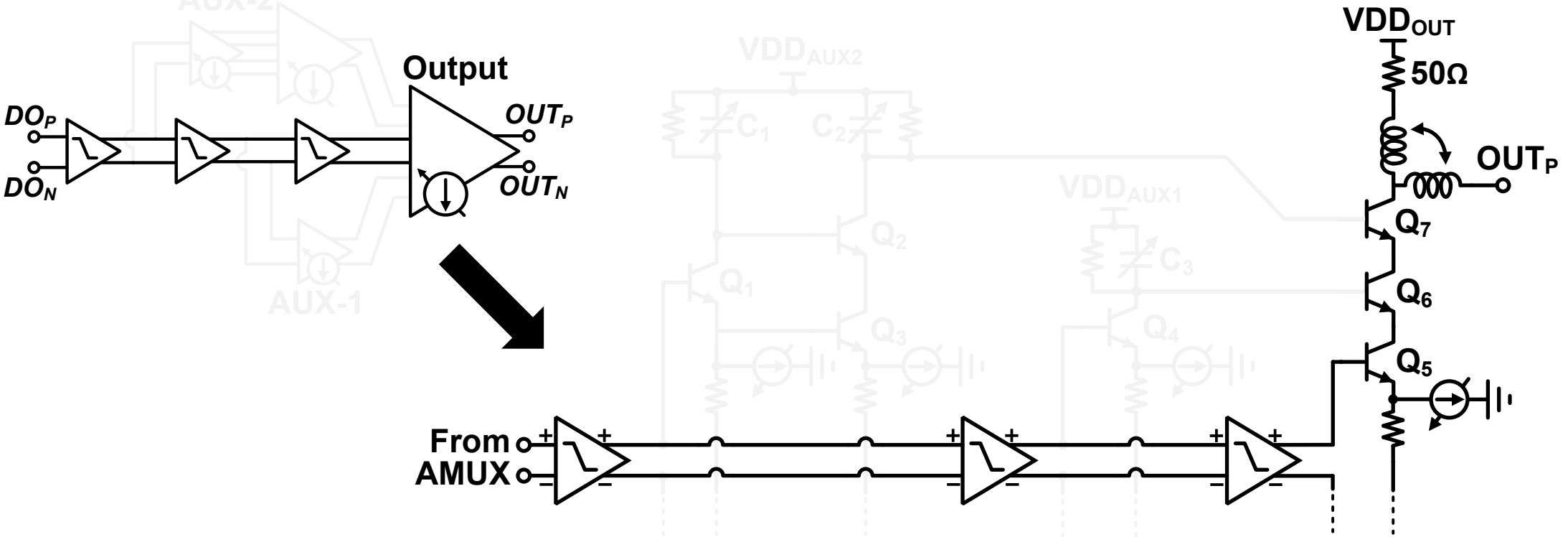
- Maximum output swing **tripled** compared to cascode
- Better linearity



Schematic of the Output Driver

Main Path

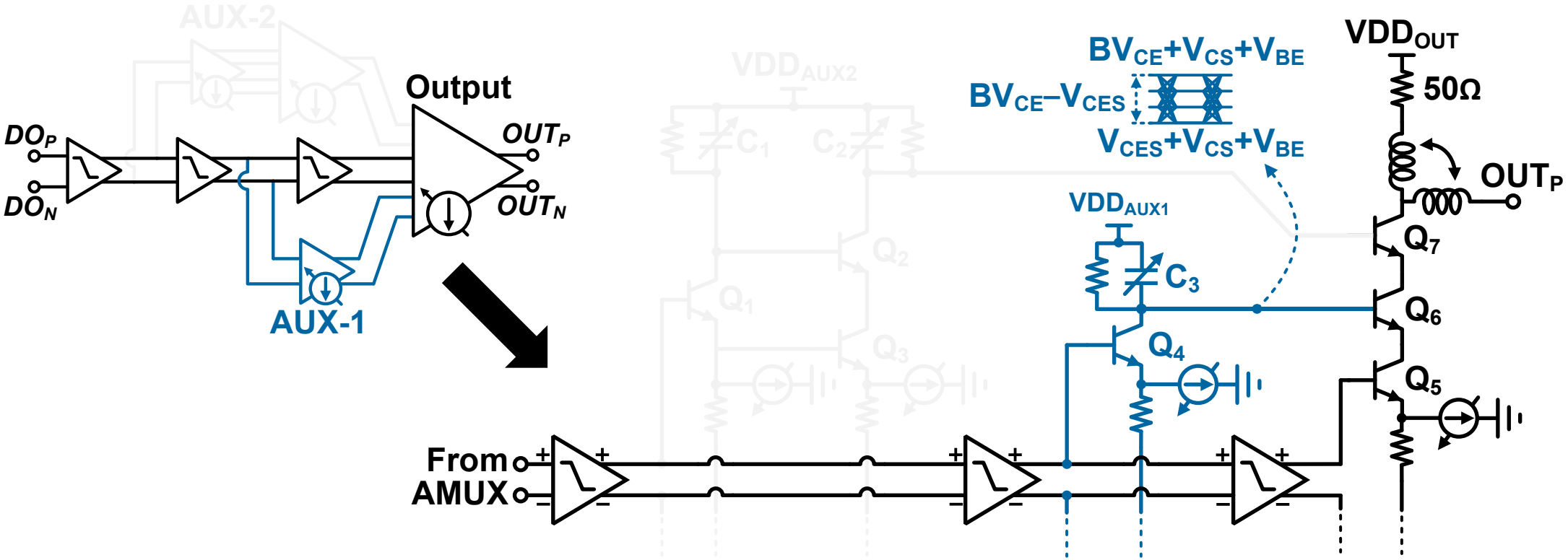
- Three emitter followers for **ensuring appropriate DC conditions** for main path, AUX-1 path, and AUX-2 path and **buffering signals**
- VDD_{OUT} = 6.5 V



Schematic of the Output Driver

AUX-1 Path

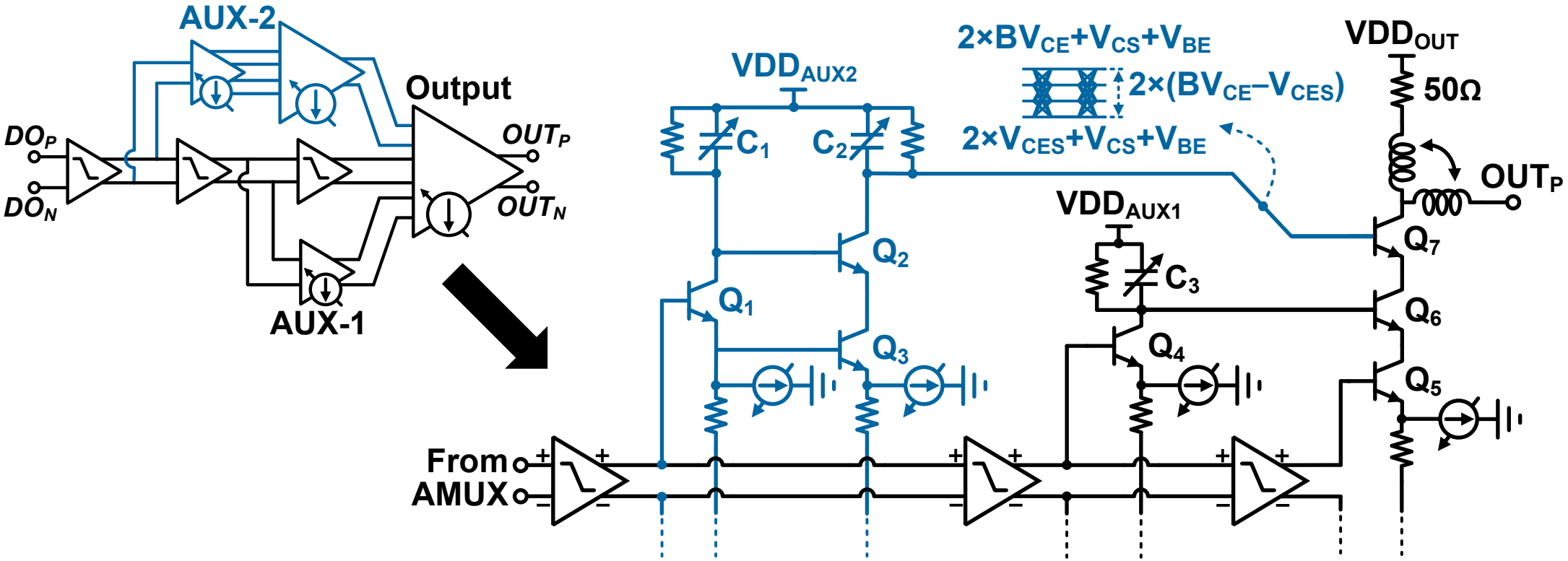
- AUX-1 path for **dynamically biasing** the base of Q_6
- VDD_{AUX-1} = 3.5 V



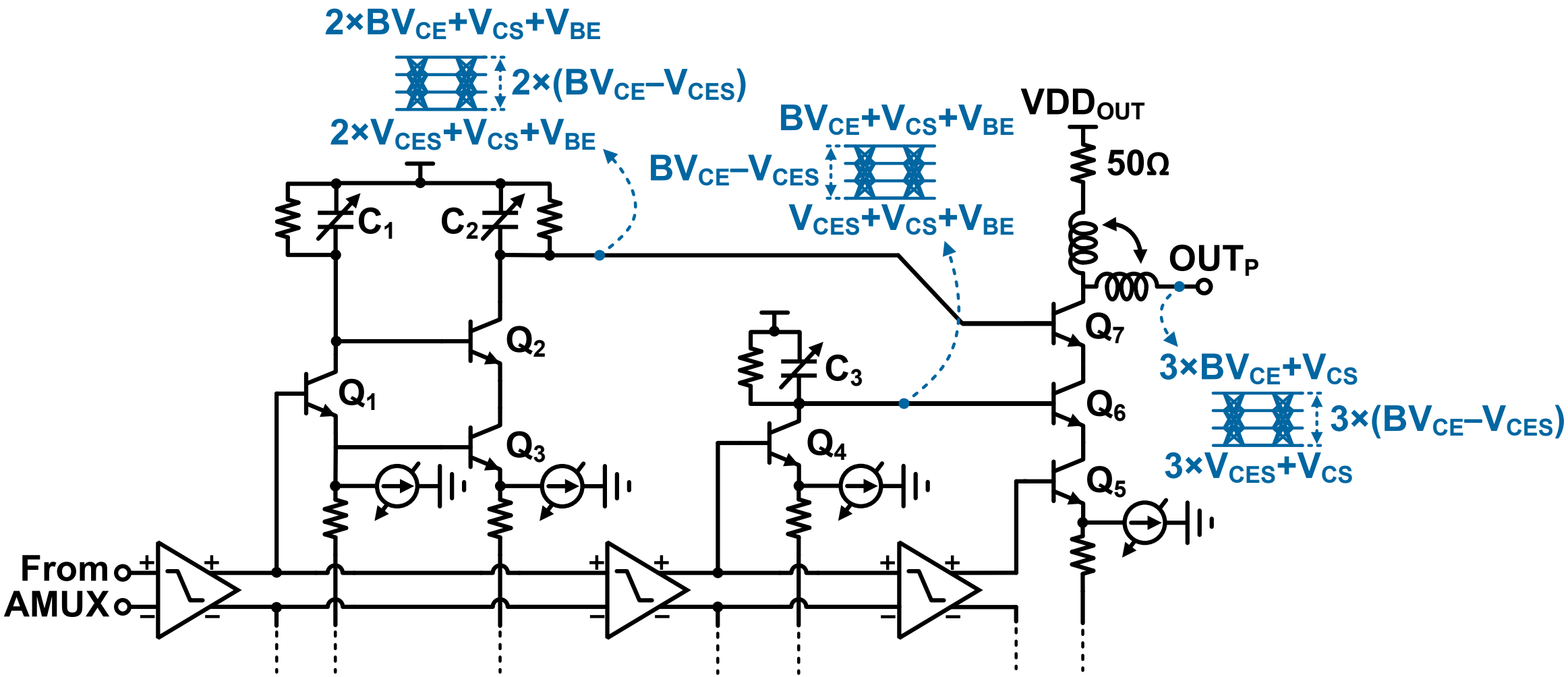
Schematic of the Output Driver

AUX-2 Path

- AUX-2 path for **dynamically biasing** the base of Q7
- AUX-2 itself is a BV doubler
- VDD_{AUX-2} = 4.5 V

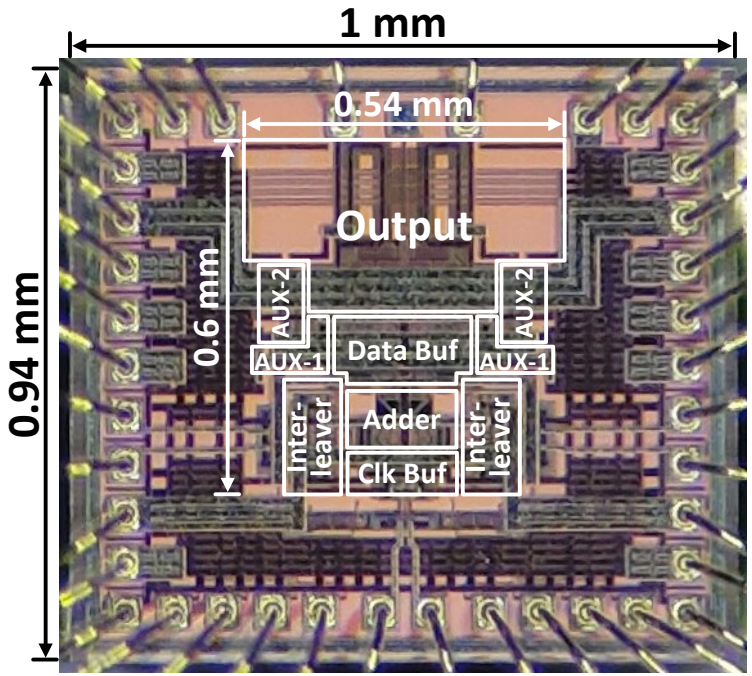


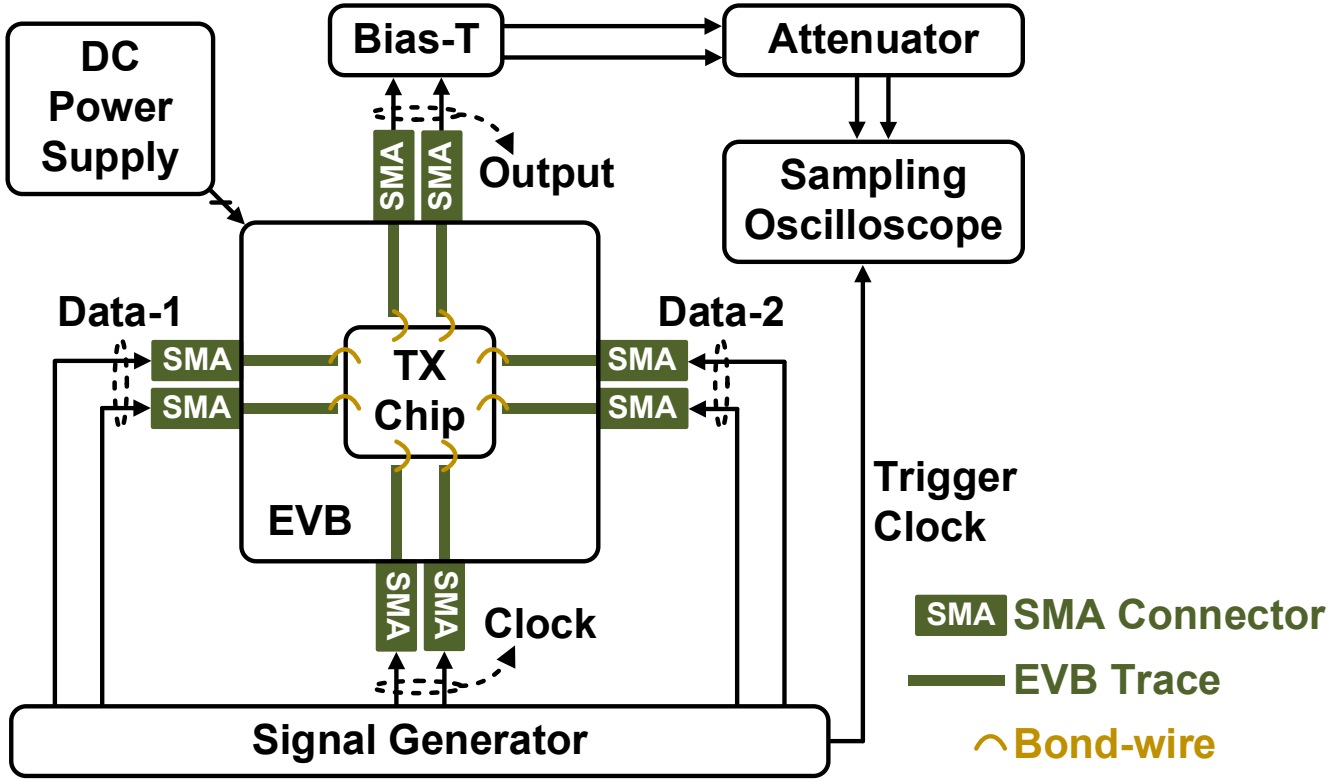
Schematic of the Output Driver



Design Under Test

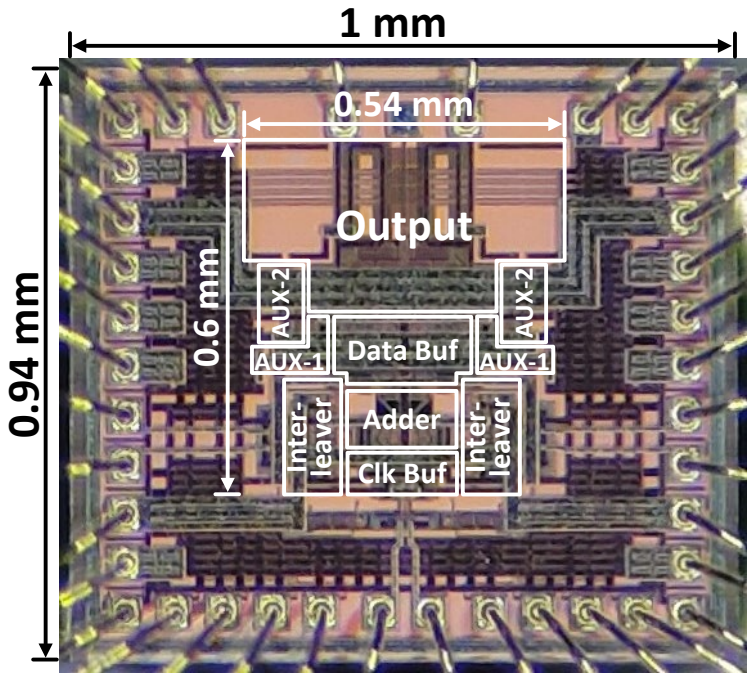
- The transmitter is fabricated in **130-nm SiGe BiCMOS** with f_T/f_{max} of 250/340 GHz
- All signals are wire-bonded to the EVB for measurement

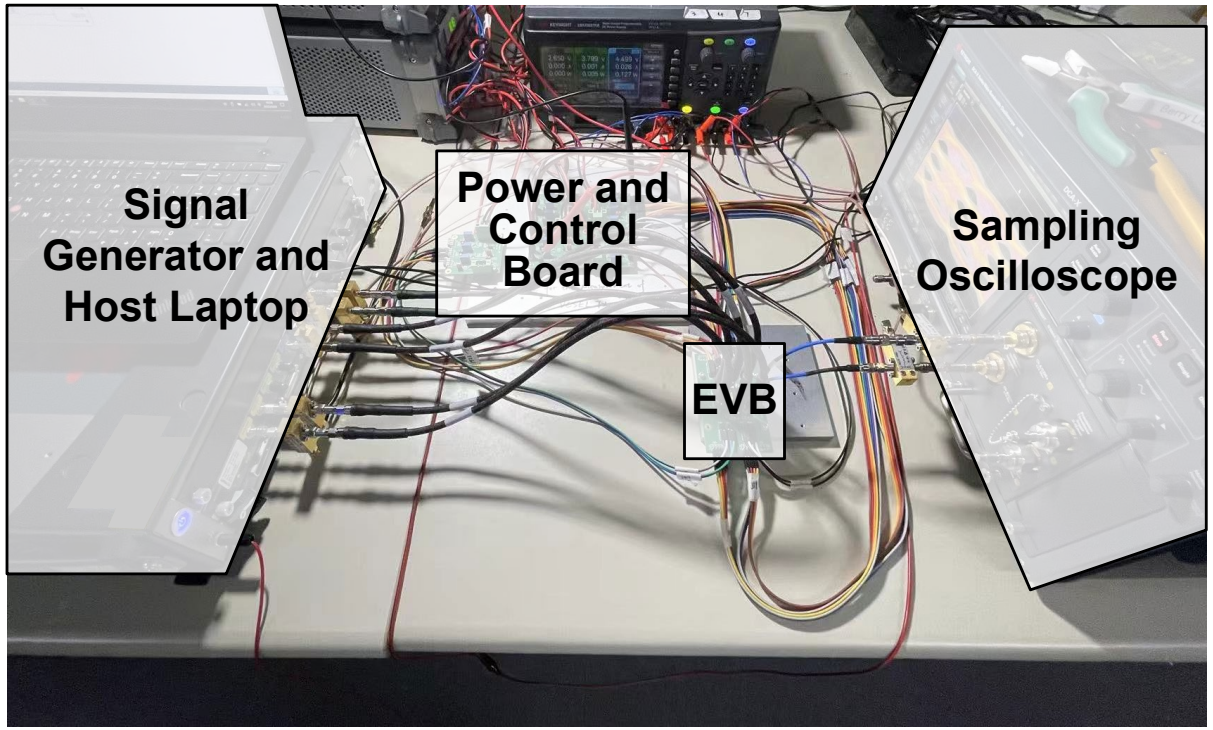




Design Under Test

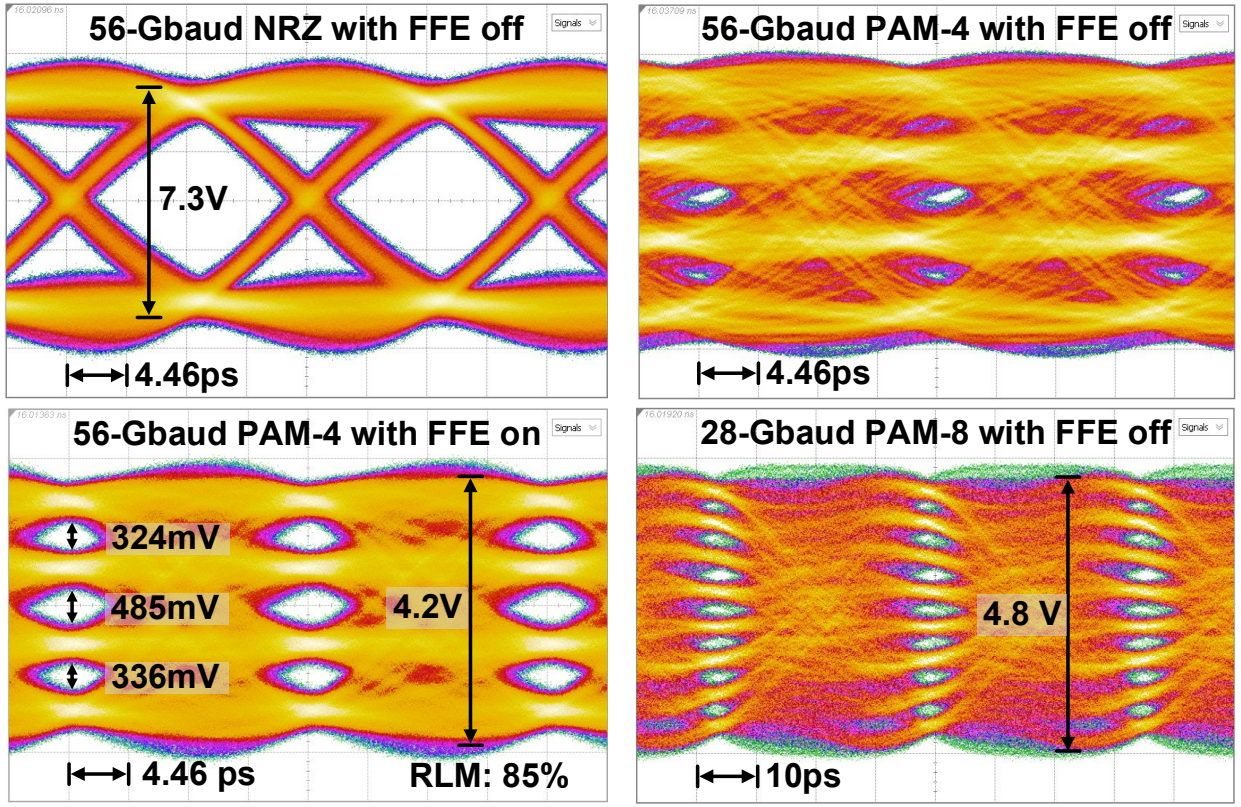
- The transmitter is fabricated in **130-nm SiGe BiCMOS** with f_T/f_{max} of 250/340 GHz
- All signals are wire-bonded to the EVB for measurement

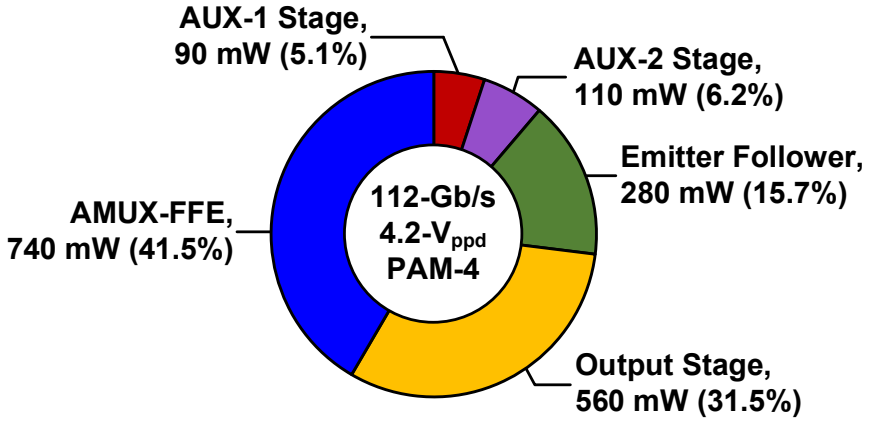




Measurement Results

- The whole transmitter supports **a maximum output swing of 7.3 V_{ppd} @ 56-Gbaud NRZ**
- With FFE, **56-Gbaud 4.2-V_{ppd} PAM-4** is achieved, with 1.78-W power consumption
- The speed of the PAM-8 case is limited by the equipment





Comparison with Prior Works

		[8] TMTT'17	[9] JSSC'20	[10] BCICTS'21	[11] BCICTS'22	[7] This Work
Technology		130-nm SiGe BiCMOS	130-nm SiGe BiCMOS	130-nm SiGe BiCMOS	130-nm SiGe BiCMOS	130-nm SiGe BiCMOS
f_T / f_{MAX} [GHz]		300/500	250/NA	300/500	380/520	250/340
Type		Distributed, Linear	Lumped, Linear	Distributed, Linear	Lumped, Linear	Lumped, Linear
Output Impedance Matching [Ω]		100	100	100	100	100
Equalization		NA	NA	1-tap FFE	NA	**Reconfig. FFE**
Serialization		NA	NA	NA	NA	**2:1 Analog**
Maximum Ouput Swing [V_{ppd}]		4 @90-Gb/s PAM-4	6 @64-Gb/s NRZ	4 @64-Gb/s Duobinary	2 (estimated by P1dB)	**7.3 @56-Gb/s NRZ**
Maximum Data Rate [Gb/s]		120 @3-V_{ppd} NRZ	138 @2.4-V_{ppd} PAM-4	64 @4-V_{ppd} Duobinary	128 @1.2-V_{ppd} PAM-4	**112 @4.2-V_{ppd} PAM-4**
Data Rate-Output Swing Product [V·Gb/s]		360	384	256	256	**470**
Driver THD		3.8% @1GHz, 3V_{ppd}	3.6% @1GHz, 6V_{ppd}	5.5% @1GHz, 4V_{ppd}	6% @5GHz, 2V_{ppd}	**1.6% @1GHz, 6V_{ppd}**
Driver Gain [dB]		12.5	30 (with VGA)	24	18	17
Area [mm^2]		1.2	1.6	1.5	0.55	0.9
Power Consumption [mW]	Driver	550	1000	1030	280	1040
	AMUX	NA	NA	NA	NA	740
FoM# [bit/s/Hz]		0.00818	0.00397	0.00414	0.00217	**0.00867**

$$^{\#}\text{FoM} = \frac{\text{Maximum Data Rate}}{f_T} \cdot \frac{(\text{Output Swing @ Maximum Data Rate})^2}{8 \cdot \text{Output Impedance Matching} \cdot \text{Power Consumption}}$$

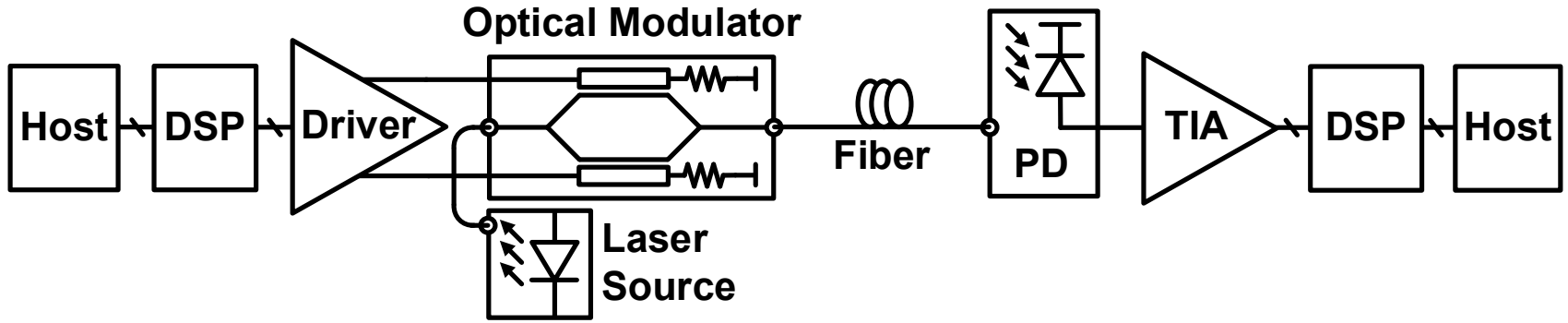
Outline

- Background
- Transmitter Design for VCSEL-based Optical Links
  - Imperfections of VCSEL
  - Implementation and Measurement of A 56-Gb/s PAM-4 VCSEL Transmitter
- **Transmitter Design for Optical Modulator-based Optical Links**
  - Design Challenges
  - Implementation and Measurement of A 56-Gbaud Half-rate Linear Transmitter
  - **Implementation and Measurement of A 100-Gbaud Linear Modulator Driver**
- Conclusions

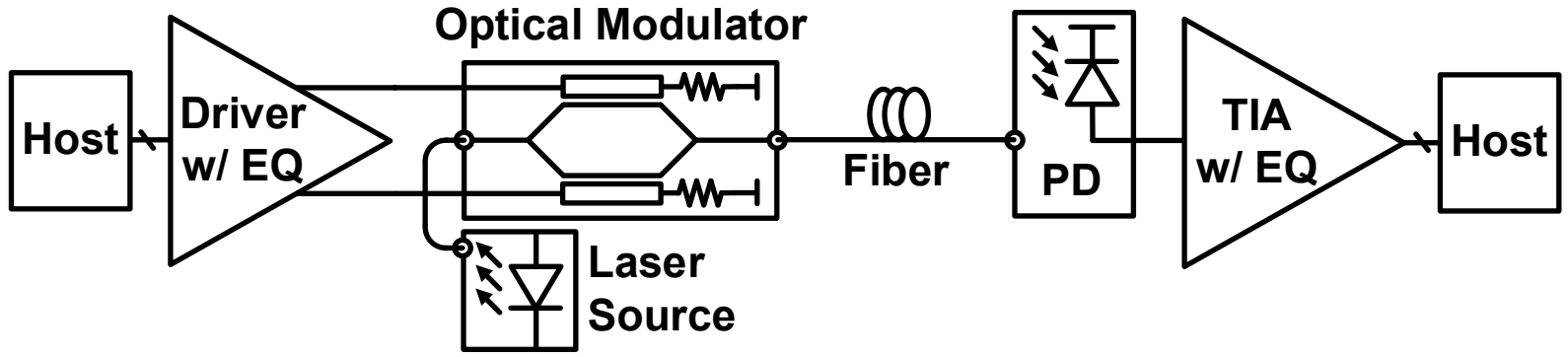
Motivation

- For medium-reach optical communications, **linear pluggable optics (LPO)** outperforms DSP-based solutions in terms of **energy efficiency**, **cost** and **latency**
- However, **how to implement EQ in driver? How to increase the link speed?**

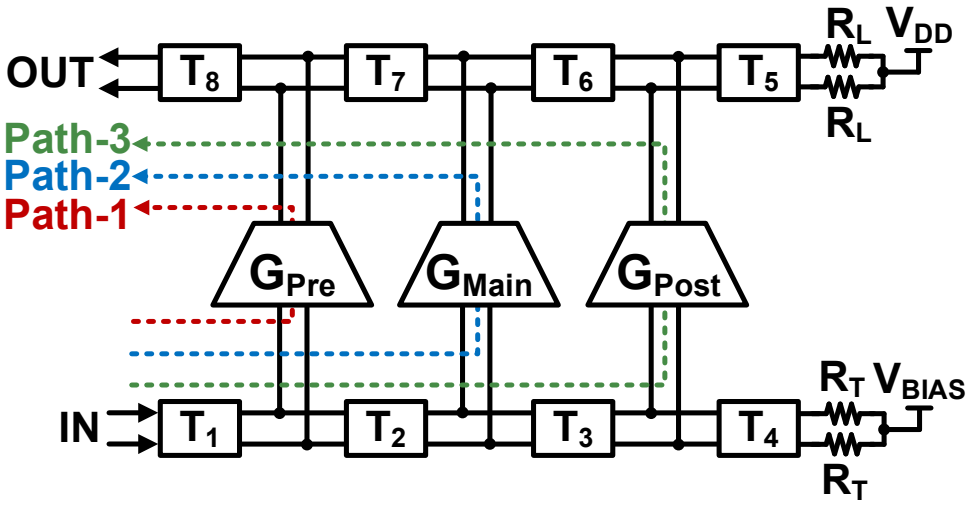
DSP-based Solution



LPO Solution



Motivation



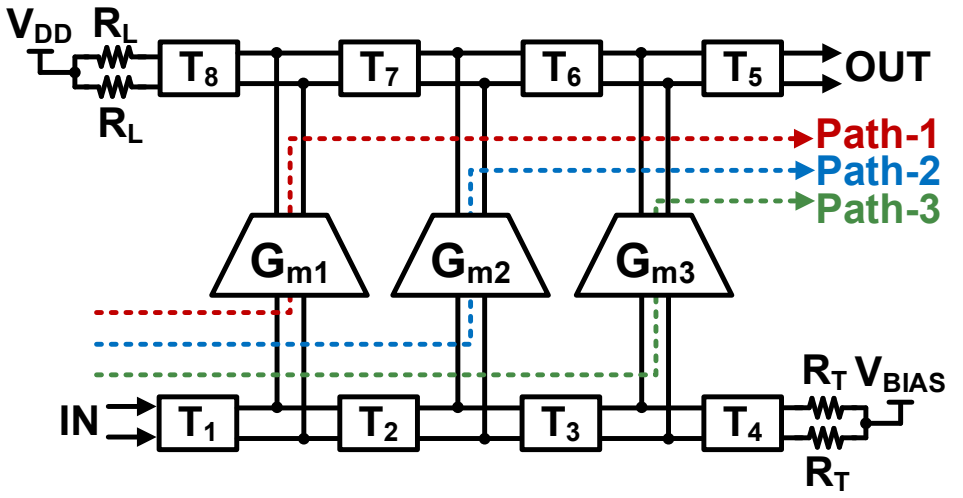
TL-based Equalizer

Pre-to-main Spacing = $Delay_{Path-2} - Delay_{Path-1}$

Main-to-post Spacing = $Delay_{Path-3} - Delay_{Path-2}$

☺ Good EQ capability

☹ Small swing and low gain



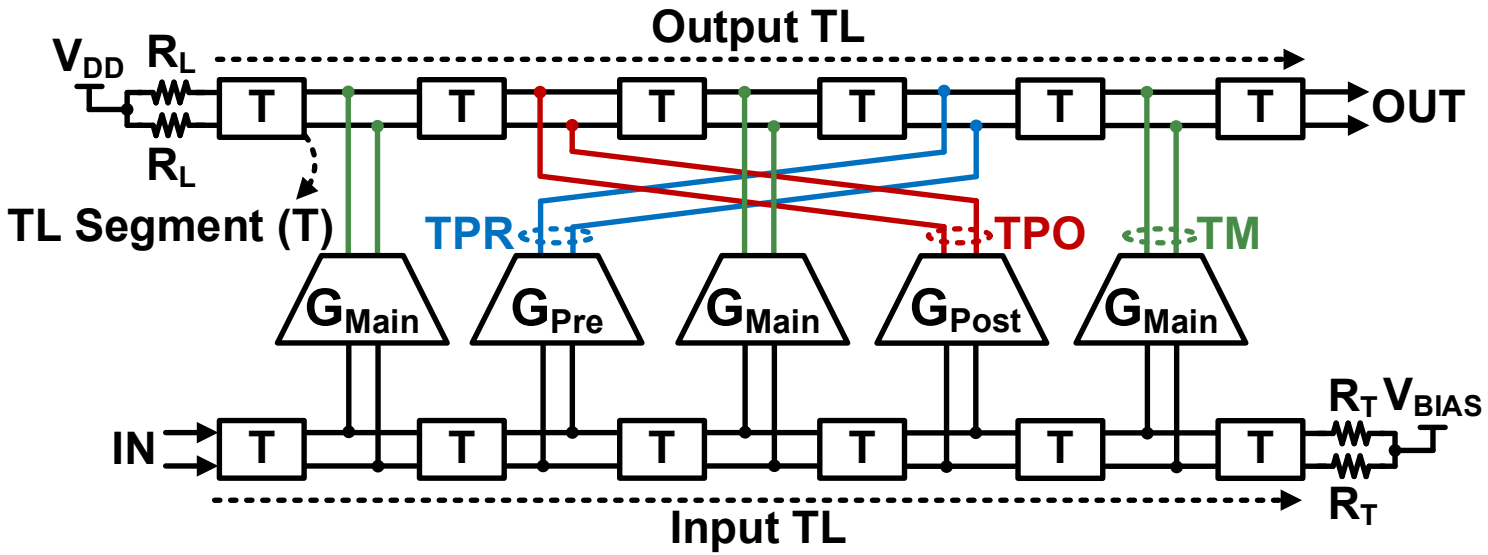
Distributed Amplifier

$Delay_{Path-1} = Delay_{Path-2} = Delay_{Path-3}$

☺ Large swing and high gain

☹ No EQ

Architecture Design Evolution (1st Vesion)



1st Version

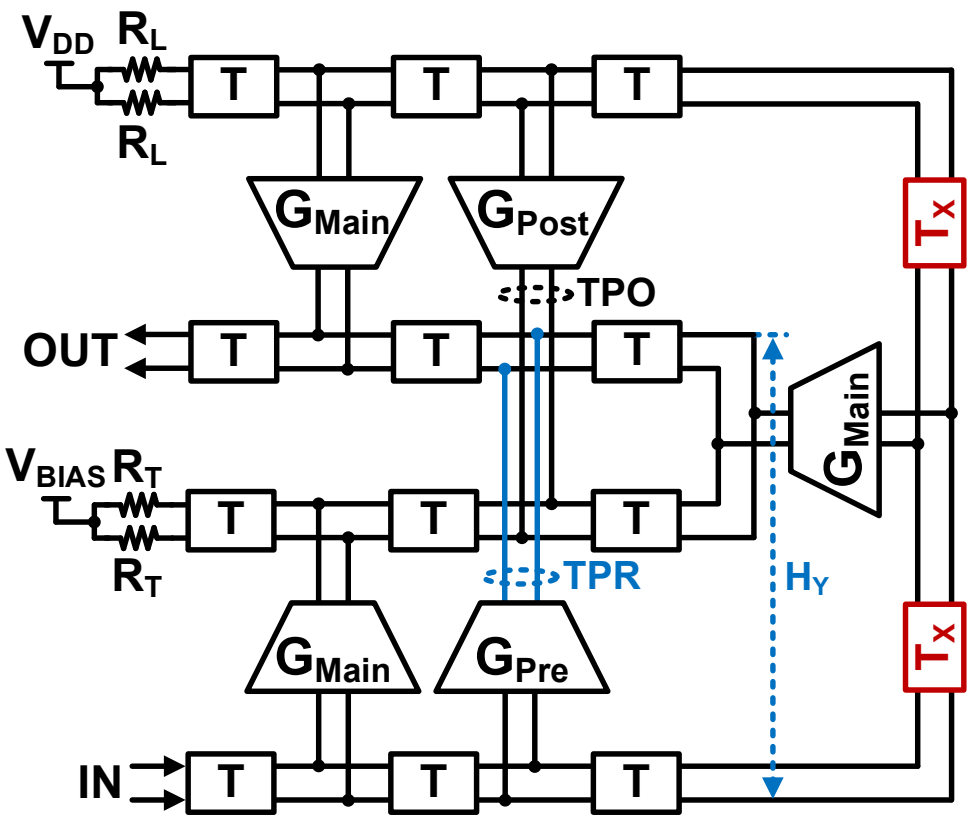
- Good EQ capability
- Large swing and high gain
- High bandwidth

However, …

- Main-to-post Spacing = 2 × $Delay_T$ + $Delay_{TPO}$ − $Delay_{TM}$
- Pre-to-main Spacing = 2 × $Delay_T$ + $Delay_{TM}$ − $Delay_{TPR}$

☹ Useless because 2 × $Delay_T$ + $Delay_{TM}$ is so close to $Delay_{TPR}$

Architecture Design Evolution (2nd Version)



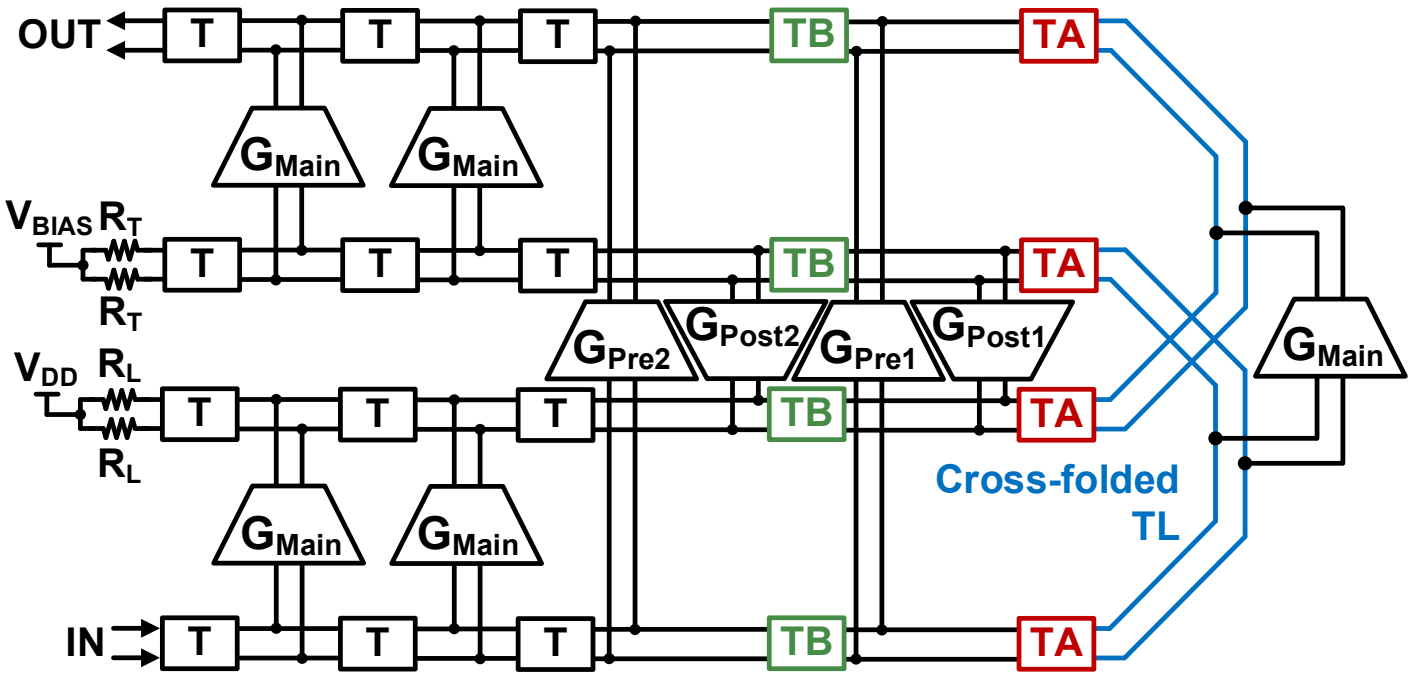
2nd Version

- Good EQ capability
- Large swing and high gain
- $Delay_{TPR}$ can be smaller by minimizing H_Y to increase pre-to-main spacing

However, …

- A length discrepancy of $2 \times T_X$ between input and output TL is introduced

Architecture Design Evolution (Final Scheme)

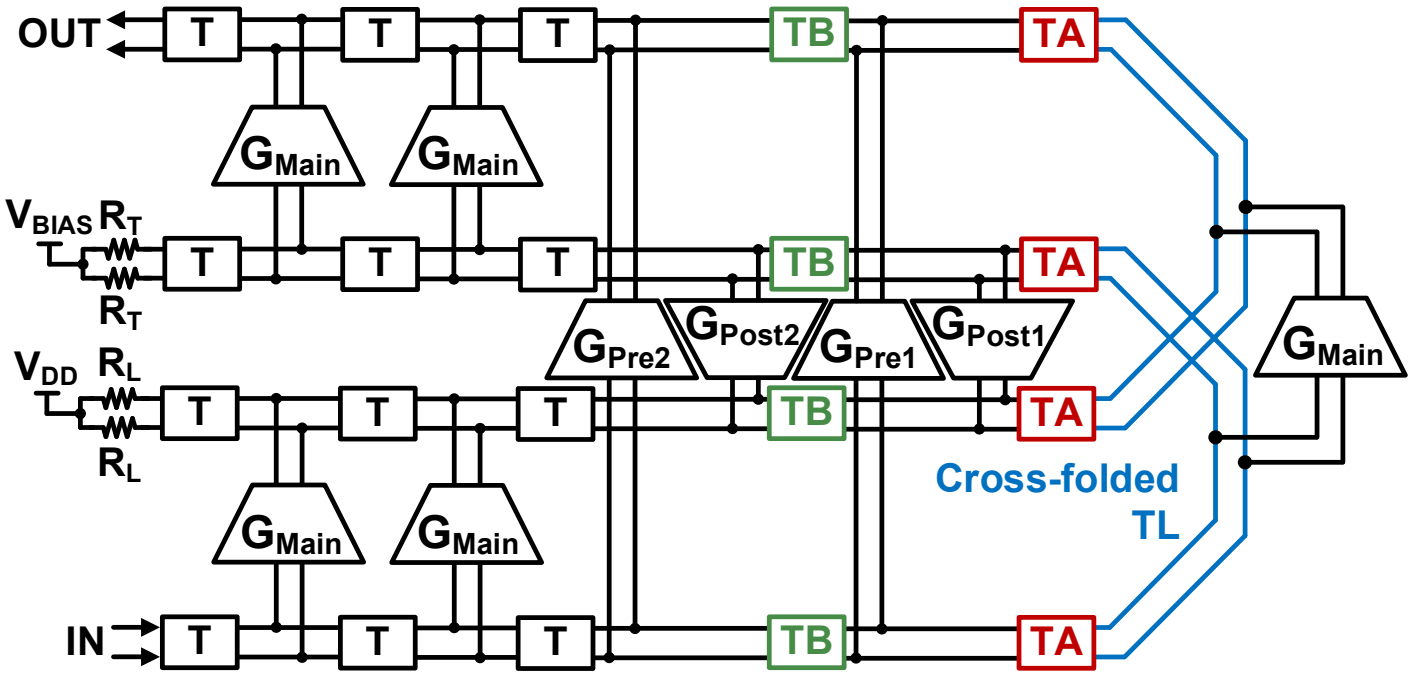


Final Scheme

- Good EQ capability
- Large swing and high gain
- Pre-to-main and Main-to-post spacings can be properly set
- No discrepancy between the lengths of input and output TLs

Architecture Design Evolution (Final Scheme)

- The **tap spacings** can be designed by adjusting the length of related TL segment
- In the future, the FFE Gm cells can be designed to be **controllable delay cell**

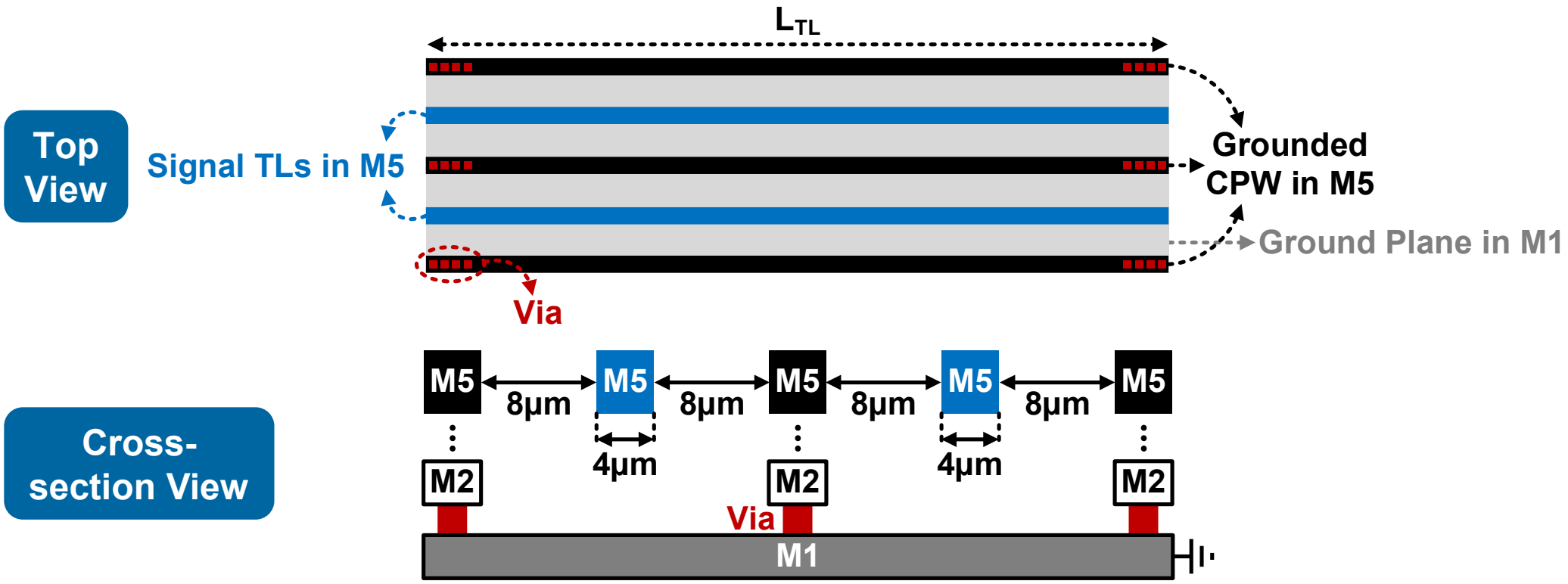


Tap Spacings

2nd Pre	
	2 × $Delay_{TB}$ + $Delay_{Pre1}$ − $Delay_{Pre2}$
1st Pre	
	2 × $Delay_{TA}$ + $Delay_{Main}$ − $Delay_{Pre1}$
Main	
	2 × $Delay_{TA}$ + $Delay_{Post1}$ − $Delay_{Main}$
1st Post	
	2 × $Delay_{TB}$ + $Delay_{Post2}$ − $Delay_{Post1}$
2nd Post	

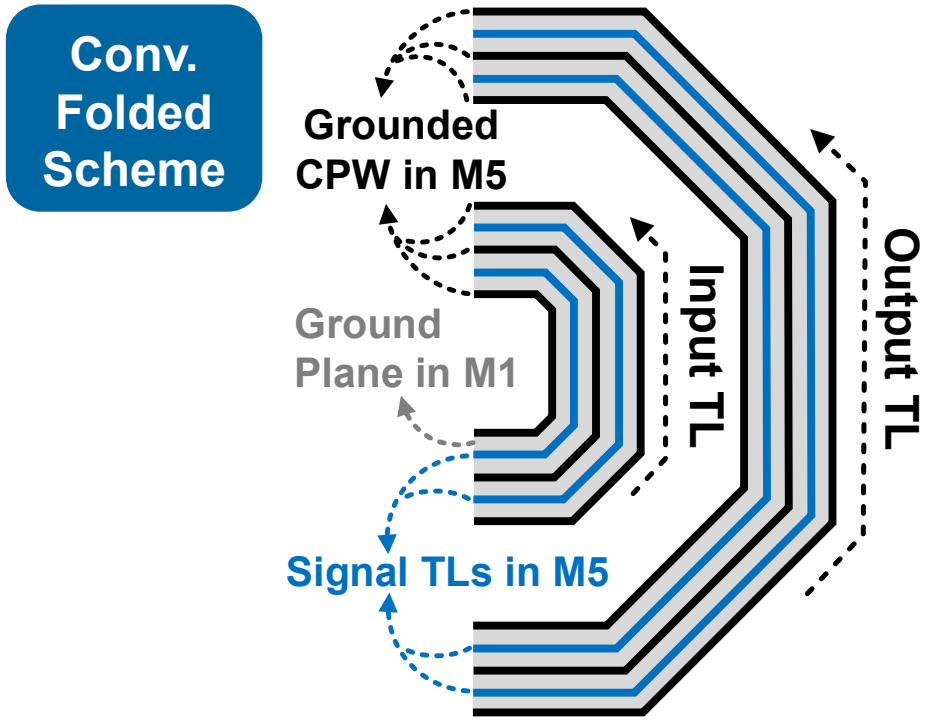
Implementation of TL Segments

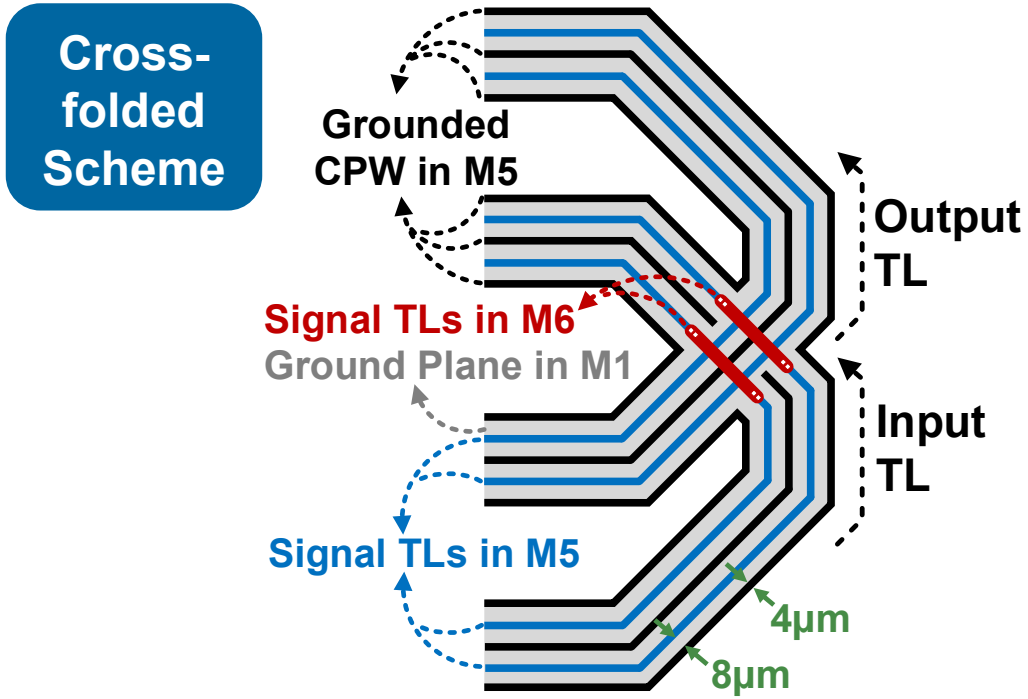
- Differential signals delivered in metal-5 (M5) and shielded by three grounded CPW also in M5
- Ground plane in metal-1 (M1) implemented for substrate shielding



Implementation of Cross-folded TL

- A **cross-folded scheme** to balance the lengths of input and output TLs
- Input TL jumps from M5 to M6 and then back to M5, which may bring **some degradations**

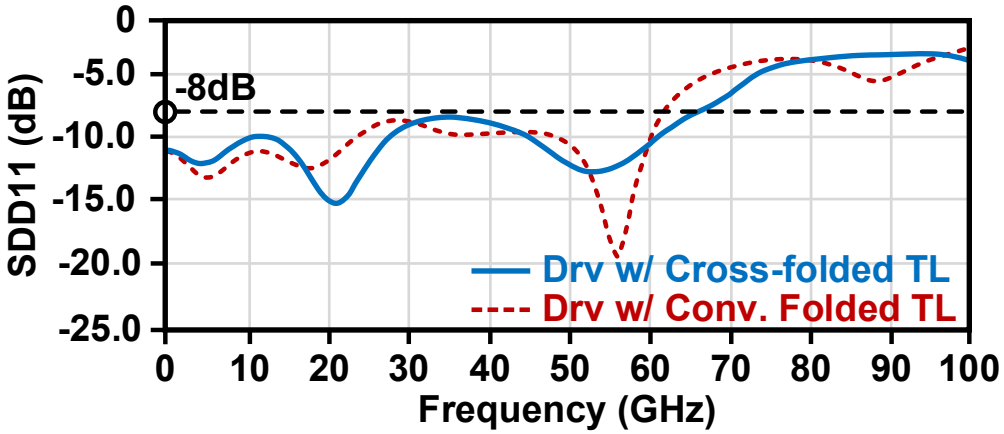




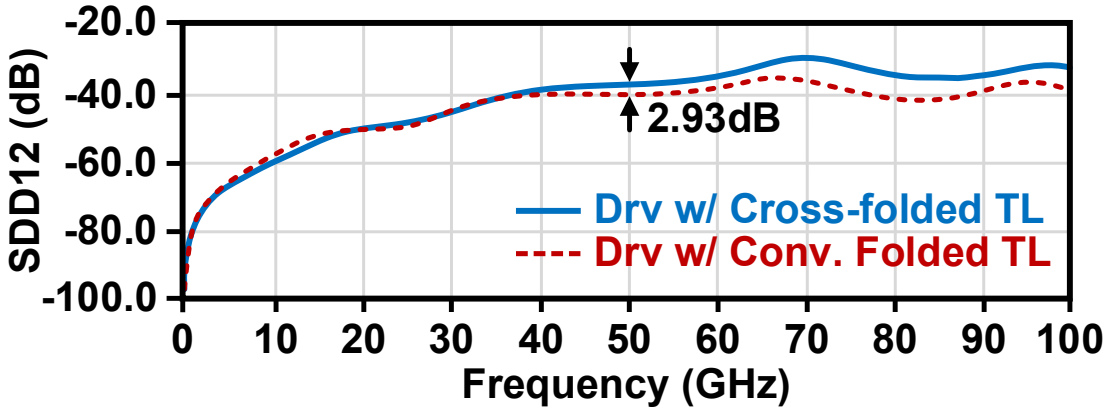
Implementation of Cross-folded TL

- The intersection results in the **discontinuity of the input impedance** which may degrade the **input reflections**
- The intersection aggravates the **parasitic effect between input and output TLs** which may degrade the **inverse isolation**

Simulated Input Reflection

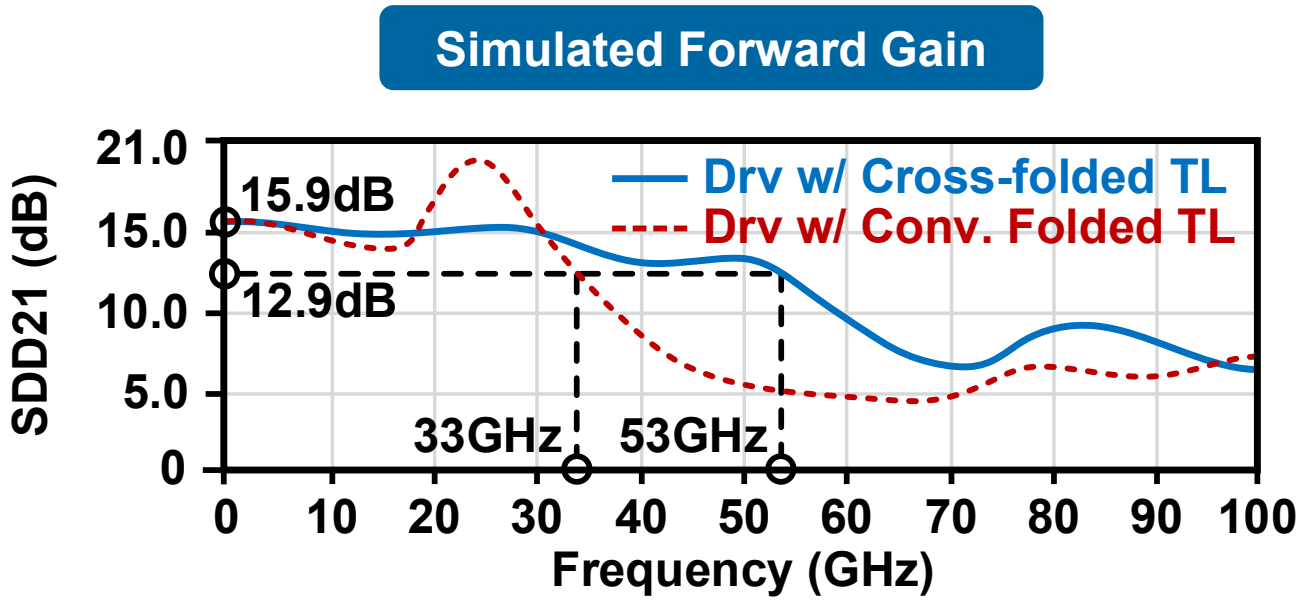


Simulated Reverse Isolation

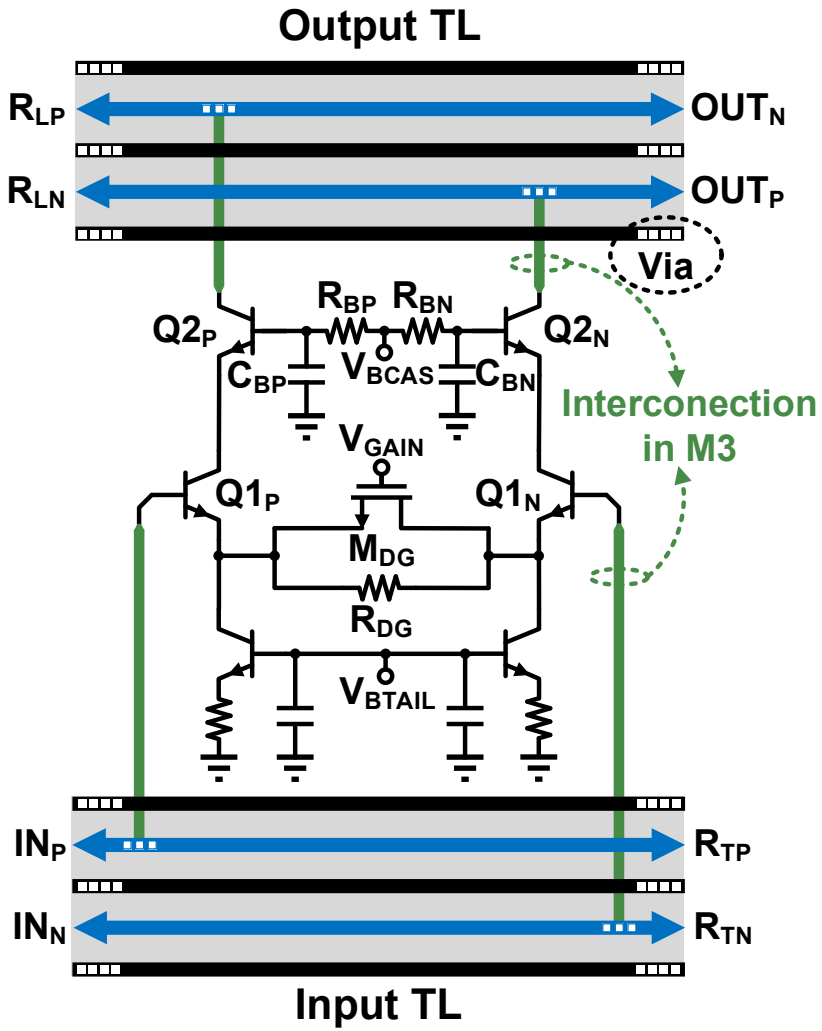


Implementation of Cross-folded TL

- With much smaller discrepancies between the lengths of input and output TLs, the cross-folded scheme achieves much **better in-band gain response** and **higher 3-dB bandwidth**



Schematic of the Gm Cell

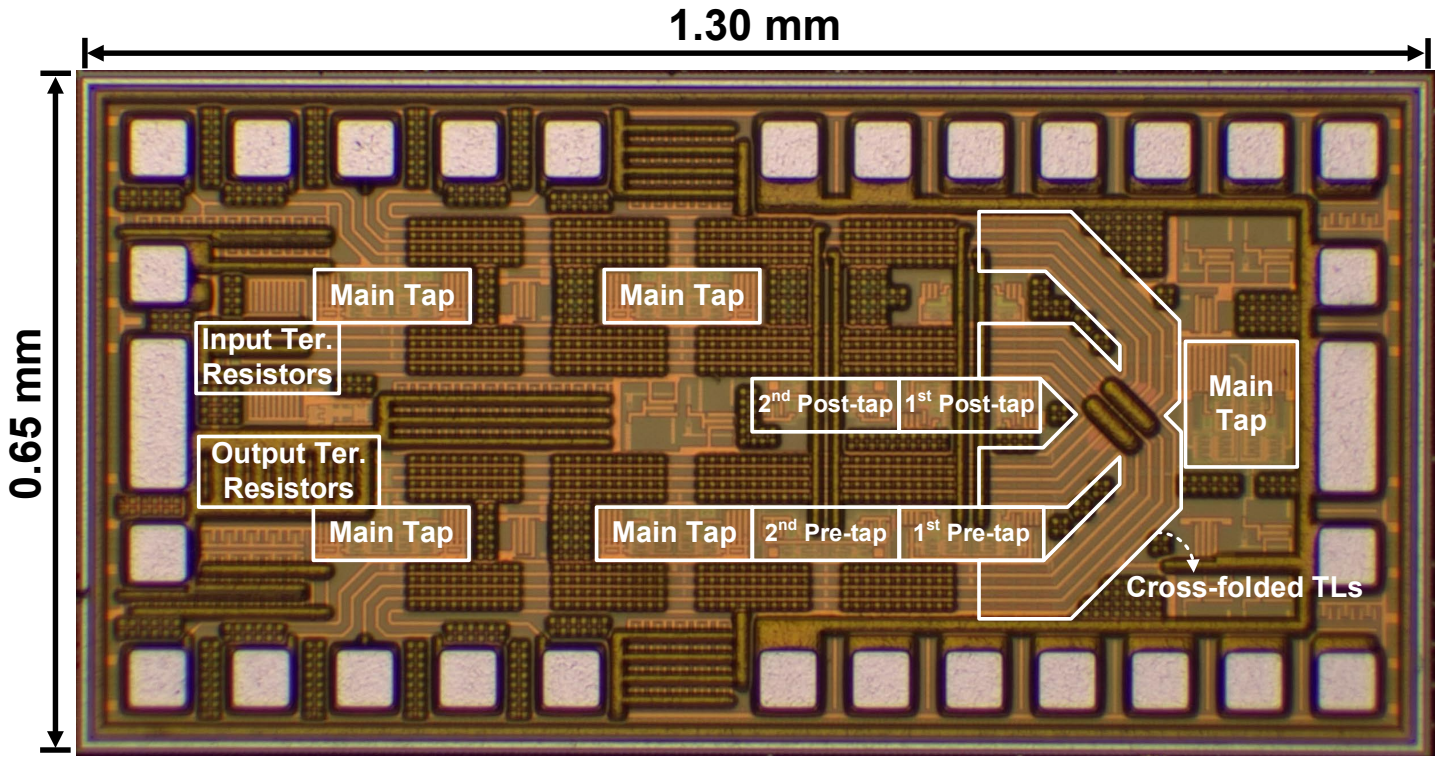


Design of Gm Cell

- All the main-tap and FFE-tap Gm cells adopt the **same design**
- A **cascode topology** is selected to improve the breakdown voltage
- R_{DG} for **linearity enhancement**
- M_{DG} for **gain tunning**
- The Gm cells are connected to the input and output TLs using **metal-3 (M3) layer**

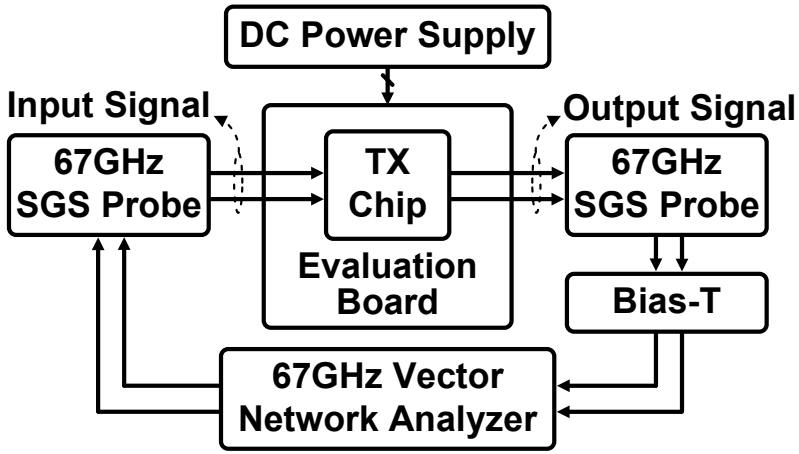
Design Under Test

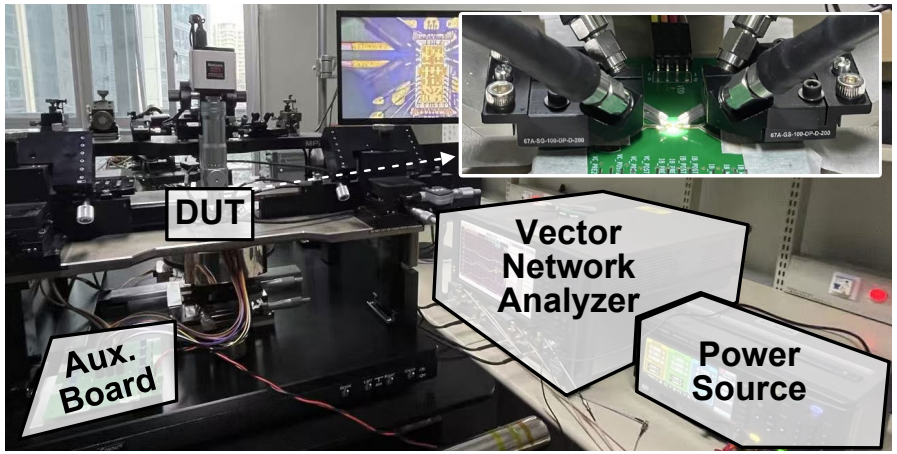
- The distributed driver is fabricated in **130-nm SiGe BiCMOS** with f_T/f_{max} of 250/340 GHz
- The RF signals are probed using 67-GHz SGS probe during measurement
- All other signals are wire-bonded to the evaluation board



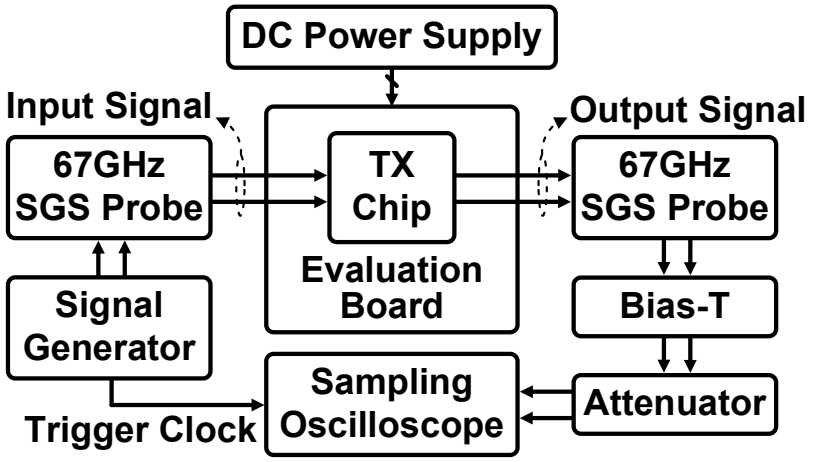
Measurement Setups

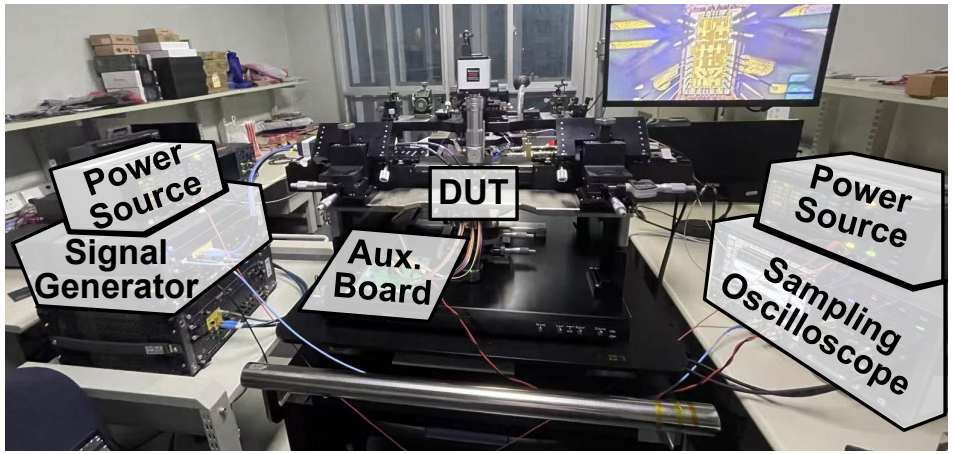
Frequency-domain Measurement





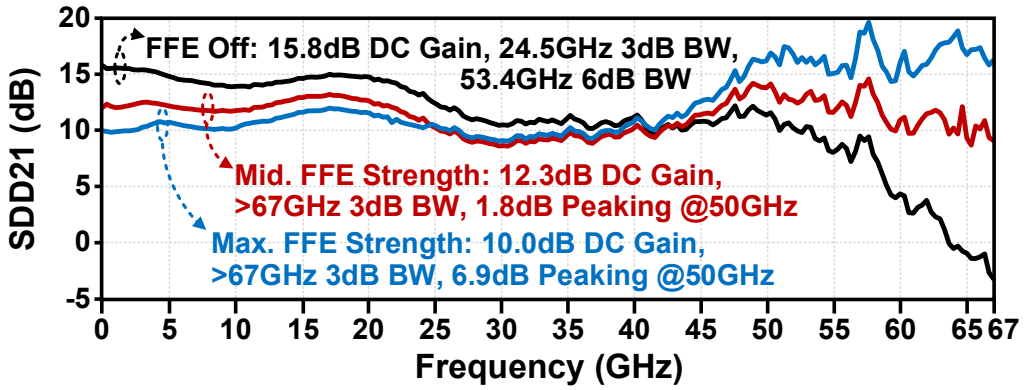
Time-domain Measurement

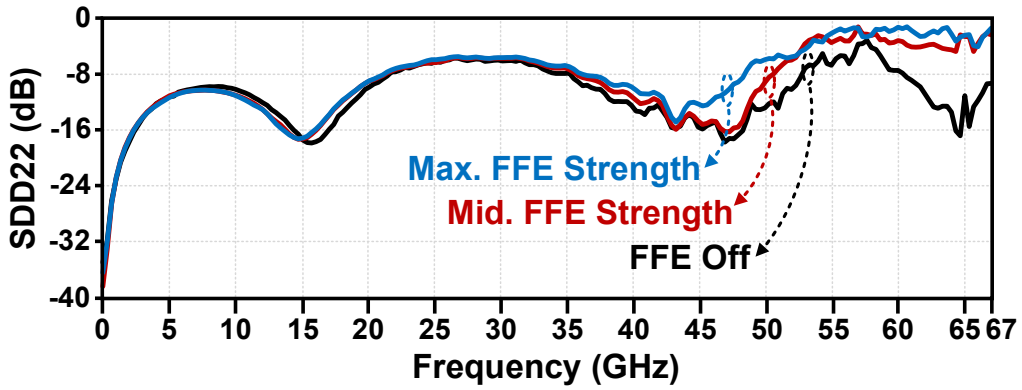


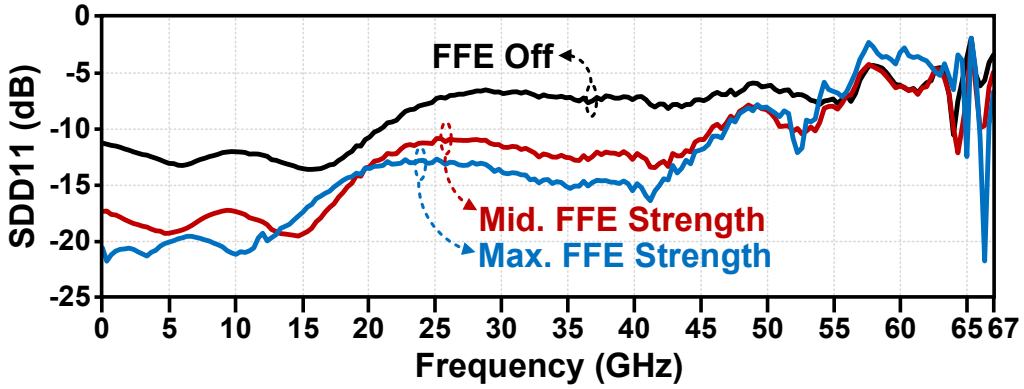


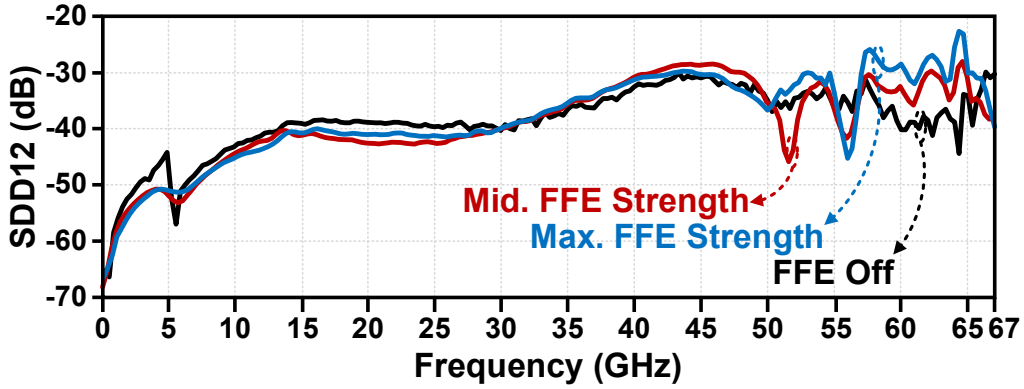
Measurement Results

- With FFE off, a **DC gain of 15.8dB**, a **3-dB BW of 24.5GHz**, and a **6-dB BW of 53.4GHz** are achieved
- With FFE on, a **DC gain of 10dB**, a **3-dB BW of >67GHz**, and a **peaking gain of 6.9dB@50GHz** are achieved



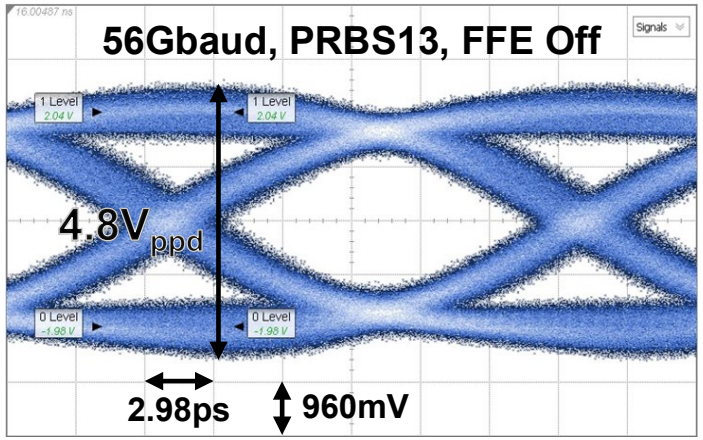


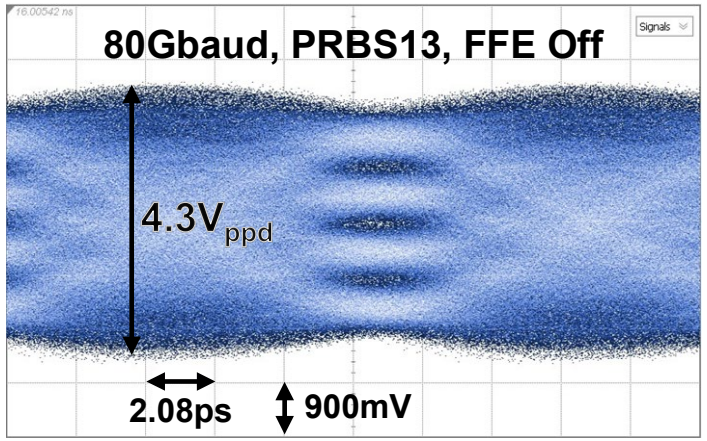


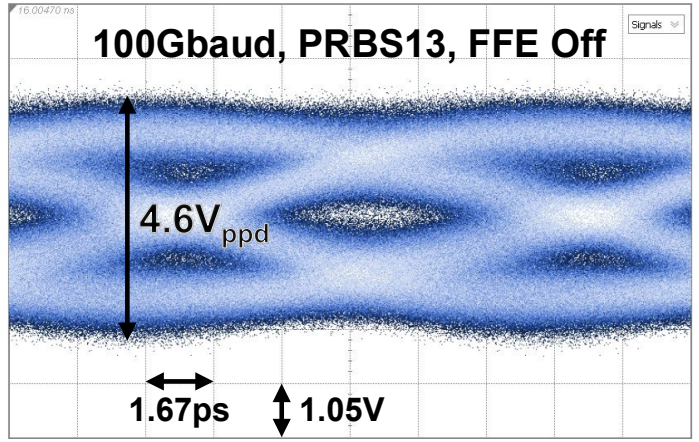


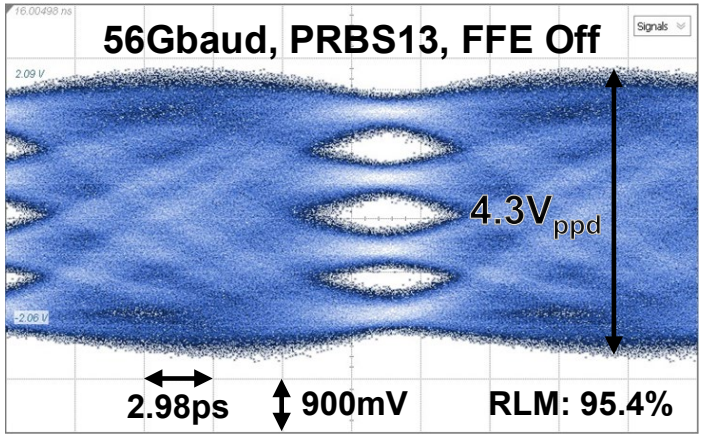
Measurement Results

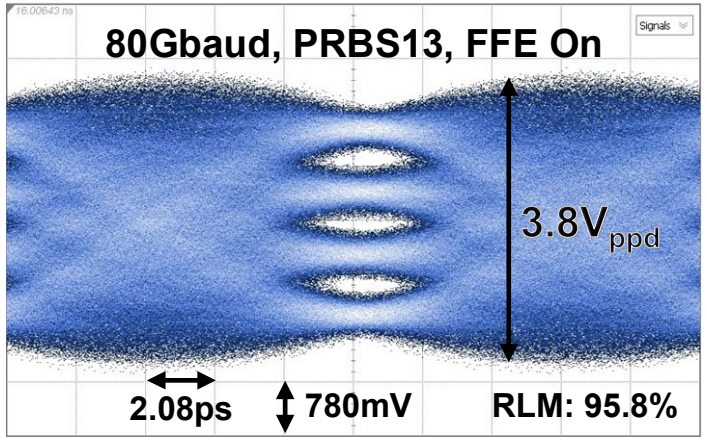
- The driver is capable of outputting **3.8-V_{ppd} 160-Gb/s PAM-4** and **4.0-V_{ppd} 100-Gb/s NRZ** signals

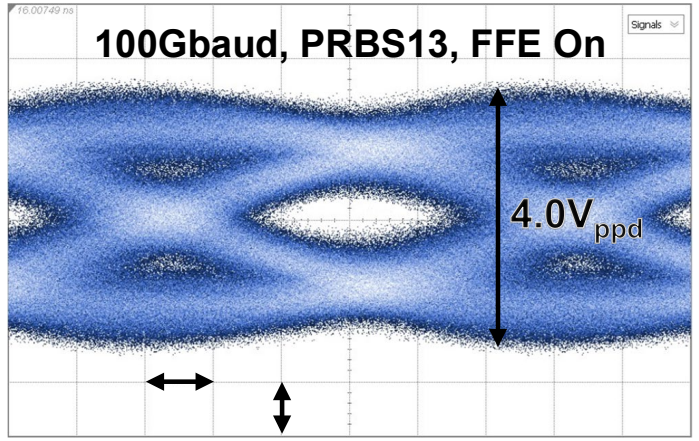












Comparison with Prior Works

	[8]TMTT'17	[9] JSSC'20	[7] CICC'24	[13] TMTT'24	[12] This Work
SiGe Node (nm)	130	130	130	55	130
f_T / f_{MAX} (GHz)	300/500	250/NA	250/340	330/370	250/340
Topology Type	Distributed	Lumped	Lumped	Hybrid	Distributed
Equalization in Driver	No	No	No	No	**5-tap FFE**
3-dB Bandwidth (GHz)	90	>40	38	>70	>67
Maximum Data Rate (Gb/s)	120 @3V_{ppd} NRZ	138 @2.4V_{ppd} PAM-4	112 @4.2V_{ppd} PAM-4	256 @3.4V_{ppd} PAM-4	**160 @3.8V_{ppd} PAM-4**
THD	<5.00% @1GHz, 3V_{ppd}	3.60% @1GHz, 6V_{ppd}	1.60% @1GHz, 6V_{ppd}	<2.00% @1GHz, 3.6V_{ppd}	2.21% @5GHz, 4V_{ppd}
DC Gain (dB)	12.5	30.0	17.0	11.2~21.8	10.0~15.8
Supply (V)	5.5	5.5	NA	3.0/4.0	4.8
Power (mW)	550	1000	1040	725	**612**
Area (mm^2)	1.19	1.60	0.66	1.07	0.85
Z_o (ohm)	100	100	100	100	100
*FoM (bit/s/Hz)	0.008	0.004	0.009	0.016	**0.019**

$$*\text{FoM} = \frac{\text{Maximum Data Rate}}{f_T} \cdot \frac{(\text{Output Swing @ Maximum Data Rate})^2}{8 \cdot Z_o \cdot \text{Power Consumption}}$$

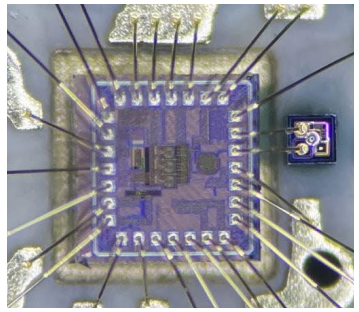
Outline

- Background
- Transmitter Design for VCSEL-based Optical Links
  - Imperfections of VCSEL
  - Implementation and Measurement of A 56-Gb/s PAM-4 VCSEL Transmitter
- Transmitter Design for Optical Modulator-based Optical Links
  - Design Challenges
  - Implementation and Measurement of A 56-Gbaud Half-rate Linear Transmitter
  - Implementation and Measurement of A 100-Gbaud Linear Modulator Driver
- **Conclusions**

Conclusions

For multi-mode optical links

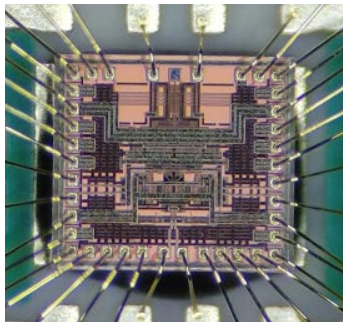
- Proposes a **VCSEL transmitter with piecewise compensation scheme**, effectively enhances the optical eye opening, achieves **56-Gb/s PAM-4** with **2.05-pJ/bit** energy efficiency



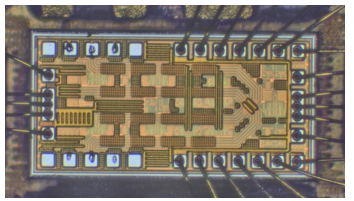
ESSCIRC'23

For single-mode optical links

- Proposes a **linear modulator transmitter** with AMUX-FFE and large-swing driver, achieves **2-to-1 analog serialization**, **reconfigurable 3-tap FFE**, **7.3-V_{ppd} maximum swing**, and **4.2-V_{ppd} 112-Gb/s PAM-4 outputs**
- Proposes a **linear distributed modulator driver** with cross-folded transmission lines and cross-coupled Gm cells, achieves **5-tap built-in FFE** and **3.8-V_{ppd} 160-Gb/s PAM-4 output**

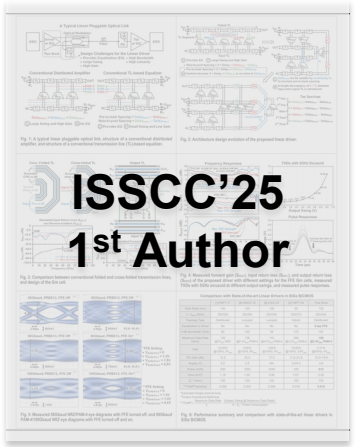


CICC'24

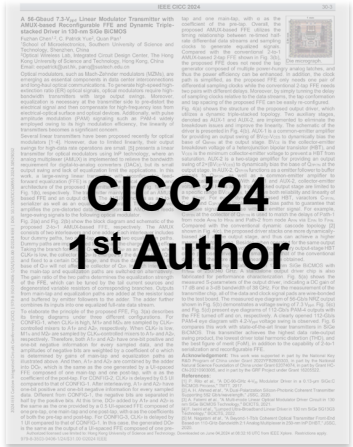


ISSCC'25

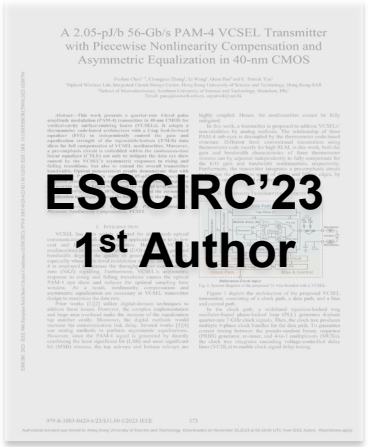
Research Outcomes



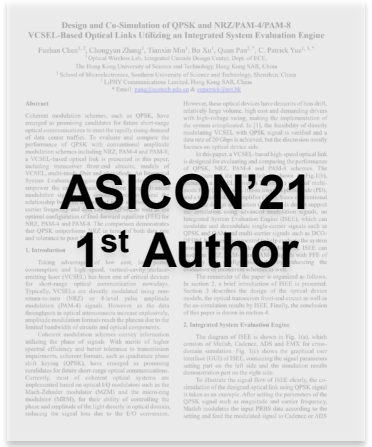
ISSCC'25
1st Author



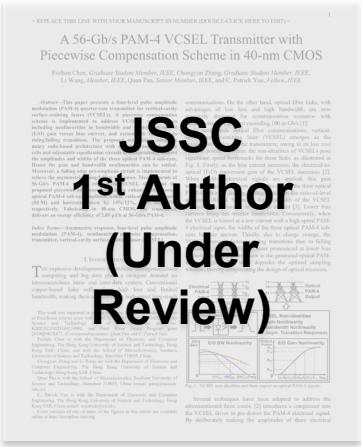
CICC'24
1st Author



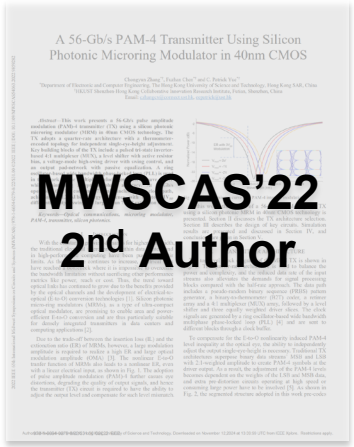
ESSCIRC'23
1st Author



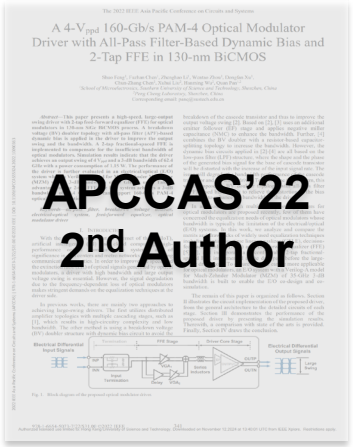
ASICON'21
1st Author



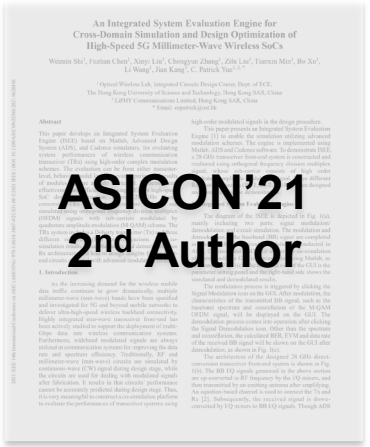
JSSC
1st Author
(Under Review)



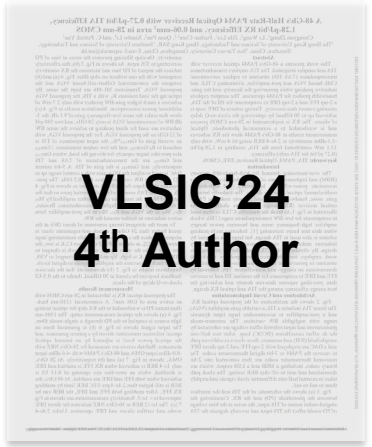
MWSCAS'22
2nd Author



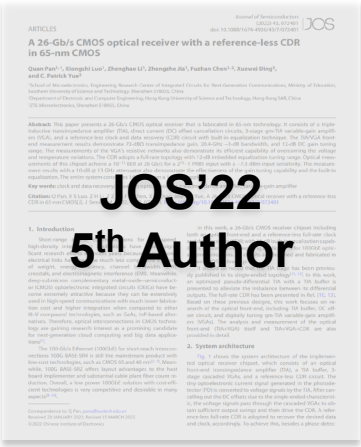
APCCAS'22
2nd Author



ASICON'21
2nd Author



VLSIC'24
4th Author



JOS'22
5th Author

Acknowledgement

- Prof. C. Patrick Yue
- Prof. Quan Pan
- Prof. Kam Sing Wong
- Prof. Wei-Zen Chen, Prof. Kam Tuen Law, Prof. Man Hoi Wong, Prof. Fengbin Tu
- All Groupmates
- My parents

香港科技大學
THE HONG KONG UNIVERSITY OF SCIENCE AND TECHNOLOGY

HKUST OWL

Q & A

Thank you!

Optical Wireless Lab
Department of Electronic and Computer Engineering
The Hong Kong University of Science and Technology (HKUST)

References

[1] F. Chen, C. Zhang, L. Wang, Q. Pan and C. P. Yue, “A 2.05-pJ/b 56-Gb/s PAM-4 VCSEL Transmitter with Piecewise Nonlinearity Compensation and Asymmetric Equalization in 40-nm CMOS,” in *2023 IEEE 49th European Solid State Circuits Conference (ESSCIRC)*, Lisbon, Portugal, 2023, pp. 373-376.

[2] A. Tyagi *et al.*, "A 50 Gb/s PAM-4 VCSEL Transmitter With 2.5-Tap Nonlinear Equalization in 65-nm CMOS," *IEEE Photonics Technology Letters*, vol. 30, no. 13, pp. 1246-1249, July 2018.

[3] P. -J. Peng *et al.*, "A 56-Gb/s PAM-4 Transmitter/Receiver Chipset With Nonlinear FFE for VCSEL-Based Optical Links in 40-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 57, no. 10, pp. 3025-3035, Oct. 2022.

[4] J. Hwang *et al.*, "A 64Gb/s 2.29pJ/b PAM-4 VCSEL Transmitter With 3-Tap Asymmetric FFE in 65nm CMOS," in *2019 Symposium on VLSI Circuits*, Kyoto, Japan, 2019, pp. C268-C269.

[5] H. Do *et al.*, "A 64 Gb/s 2.09 pJ/b PAM-4 VCSEL Transmitter with Bandwidth Extension Techniques in 40 nm CMOS," in *2021 IEEE Asian Solid-State Circuits Conference*, Busan, Korea, 2021, pp. 1-3.

[6] M. Raj et al., "A Modelling and Nonlinear Equalization Technique for a 20 Gb/s 0.77 pJ/b VCSEL Transmitter in 32 nm SOI CMOS," IEEE Journal of Solid-State Circuits, vol. 51, no. 8, pp. 1734-1743, Aug. 2016.

References

[7] F. Chen, C. P. Yue and Q. Pan, "A 56-Gbaud 7.3-Vppd Linear Modulator Transmitter with AMUX-Based Reconfigurable FFE and Dynamic Triple-Stacked Driver in 130-nm SiGe BiCMOS," in *2024 IEEE Custom Integrated Circuits Conference (CICC)*, Denver, CO, USA, 2024.

[8] P. Rito *et al.*, "A DC-90-GHz 4-V_{pp} Modulator Driver in a 0.13-µm SiGe:C BiCMOS Process," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 12, pp. 5192-5202, Dec. 2017.

[9] A. H. Ahmed *et al.*, "A Dual-Polarization Silicon-Photonic Coherent Transmitter Supporting 552 Gb/s/wavelength," in *IEEE Journal of Solid-State Circuits*, vol. 55, no. 9, pp. 2597-2608, Sept. 2020.

[10] A. Fatemi *et al.*, "A Multi-mode Linear Optical Modulator Driver Circuit in 130 nm SiGe BiCMOS Technology," in *2021 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, Monterey, CA, USA, 2021, pp. 1-4.

[11] F. Iseini *et al.*, "Lumped Ultra-Broadband Linear Driver in 130 nm SiGe SG13G3 Technology," in *2022 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, Phoenix, AZ, USA, 2022, pp. 136-139.

References

[12] F. Chen , C. P. Yue and Q. Pan , "A 100Gbaud 4V_{ppd} Distributed Linear Driver with Cross-folded Transmission Lines and Cross-coupled Gm Cells for Built-in 5-tap FFE in 130nm SiGe BiCMOS," in *2025 IEEE International Solid-State Circuit Conference (ISSCC)*, San Francisco, CA, USA, 2025.

[13] S. Niu *et al.*, "A Linear Modulator Driver With Over 70-GHz Bandwidth 21.8-dB Gain and 3.4-Vppd Output Swing for Beyond 120-GBd Optical Links," *IEEE Transactions on Microwave Theory and Techniques*, vol. 72, no. 7, pp. 4080-4091, July 2024.