香港科技大學
THE HONG KONG UNIVERSITY OF SCIENCE AND TECHNOLOGY

HKUST OWL

Energy-Efficient CMOS Optical Receiver for Short-Reach Data Center Application

Chongyun Zhang

Thesis supervisor: Prof. C. Patrick Yue

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Optical Wireless Lab
Department of Electronic and Computer Engineering
The Hong Kong University of Science and Technology (HKUST)

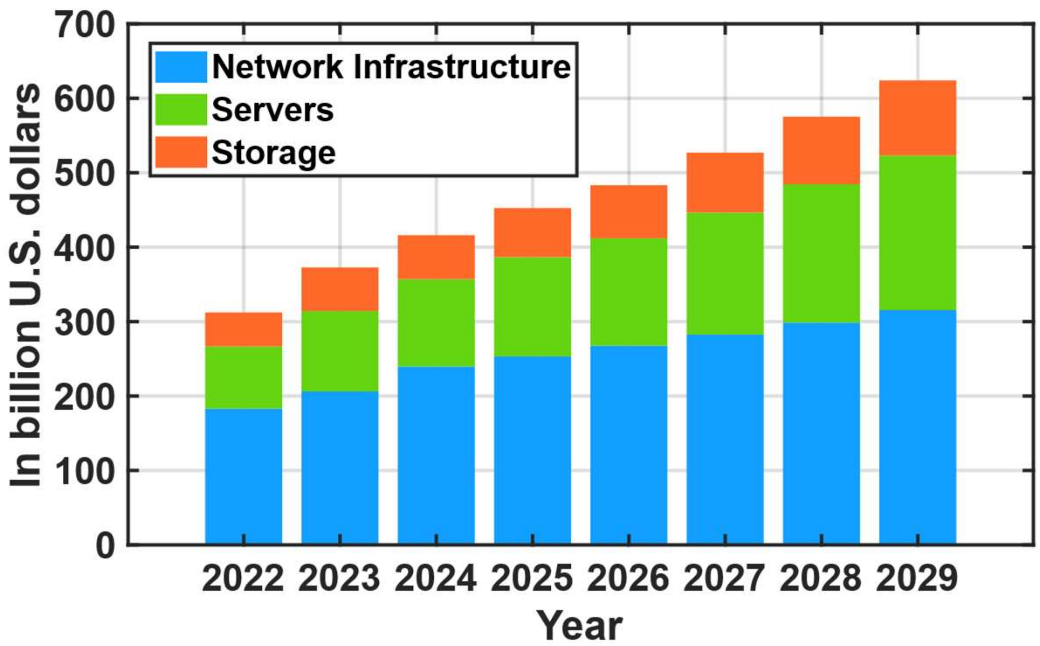
Outline

- Background
- PAM-4 Optical Receiver Data Path
- PAM-4 Optical Receiver Front End
- Conclusion

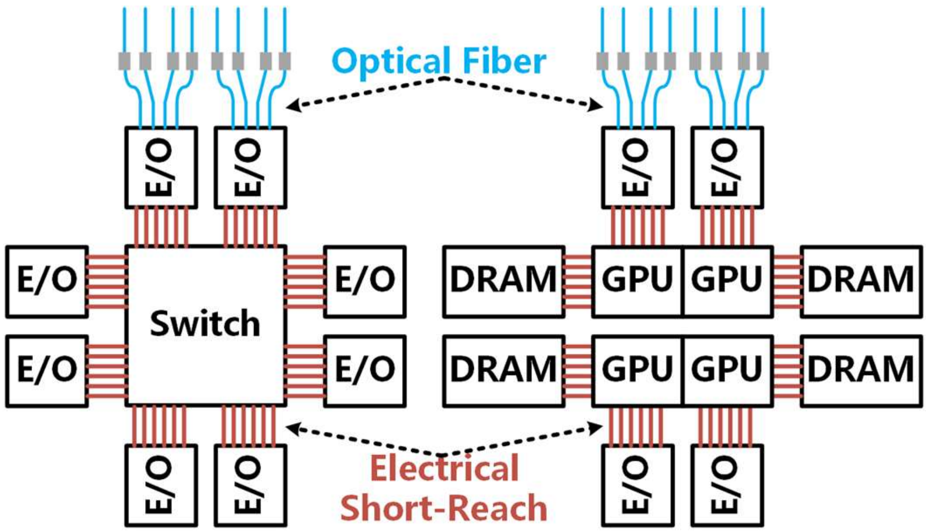
Research Background

- Data center networks keep scaling in BW and physical size
- Optical interconnects offer enhanced traffic capacity and reduced power consumption
- Further scaling of efficiency and density remains challenging due to limited integration in optical modules

Revenue in the data center market*



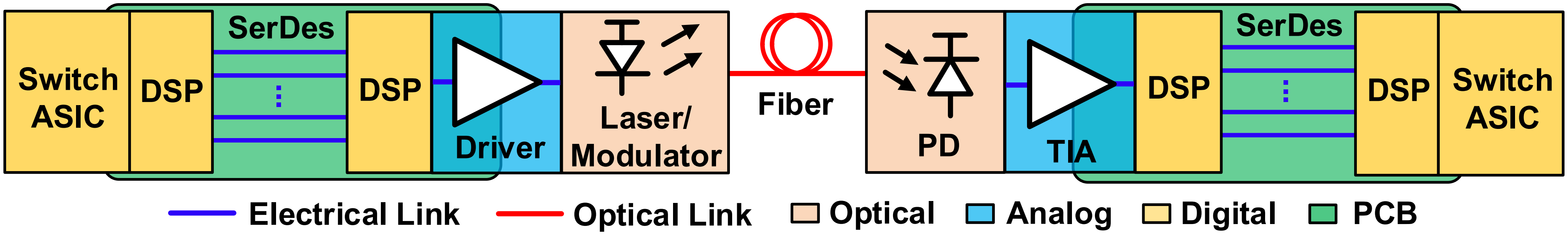
Network switch arrays with E/O interfaces



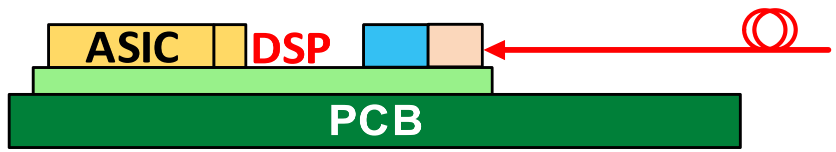
(*Revenue in the Data Center market for different segments Worldwide from 2018 to 2029 [Graph], Statista Market Insights, July 22, 2024. [Online]. Available: https://www.statista.com/forecasts/1441973/revenue-data-center-market-for-different-segments-worldwide.)

Development Trend in Optical Interconnect

Intensity-Modulation Direct-Detection (IMDD) Optical Link



Retimed Pluggable Optics (RPO)



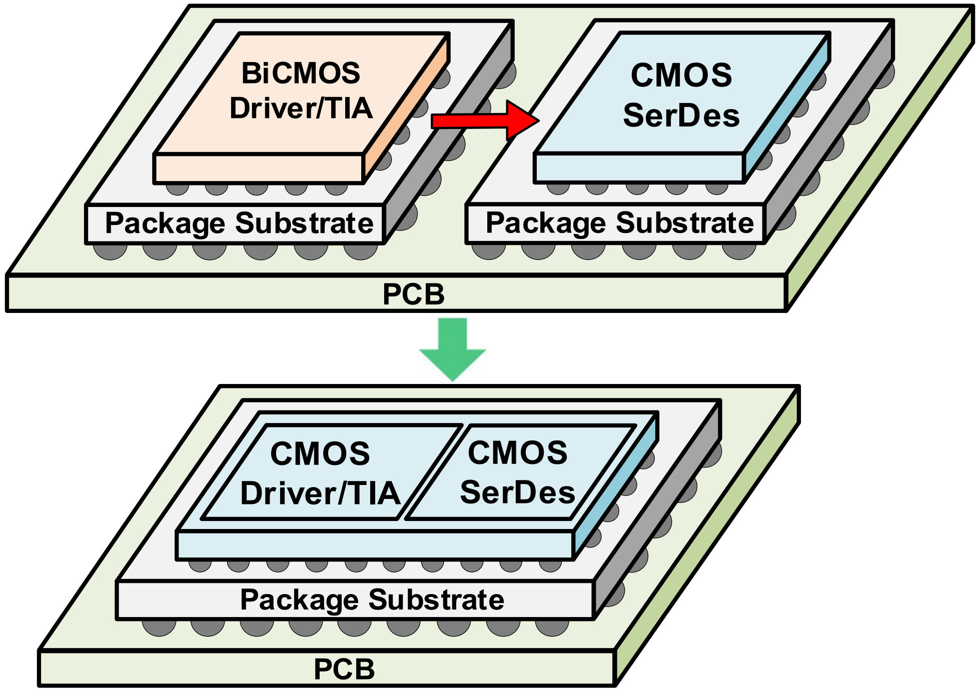
Co-Packaged Optics (CPO)

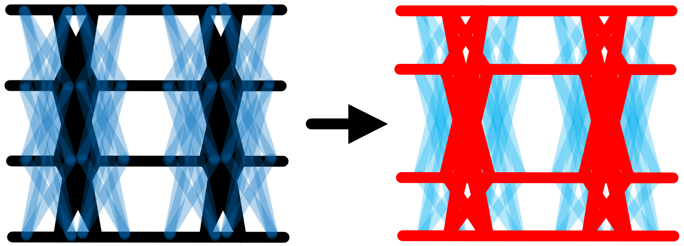
- High power consumption from DSP chips
- Increase of frequency-dependent losses in PCB
- Heavy cost and power from SiGe BiCMOS front end

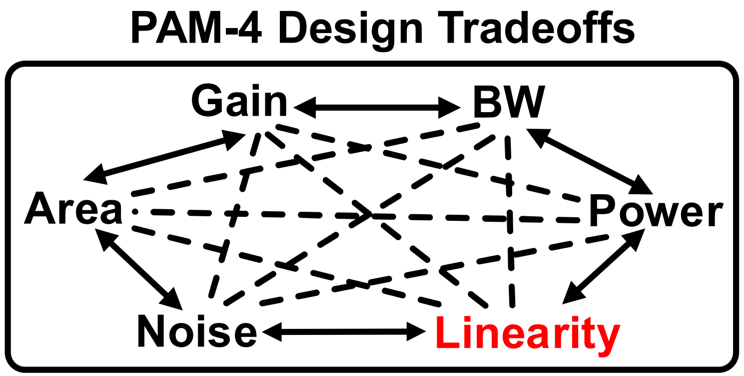
Linear Pluggable Optics (LPO)

SerDes: Serializer/Deserializer; DSP: digital signal processor; ASIC: application-specific integrated circuit

Design Challenges







Integration of front-end transceivers in CMOS

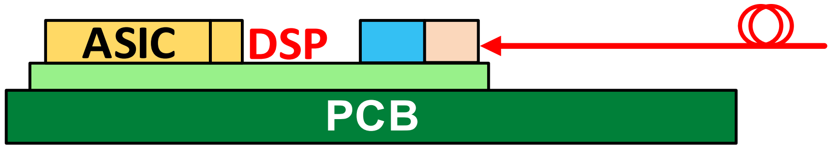
- Lower f_T and intrinsic gain
- Worse noise performance
- Limited supply voltage

Adoption of four-level pulse amplitude modulation (PAM-4)

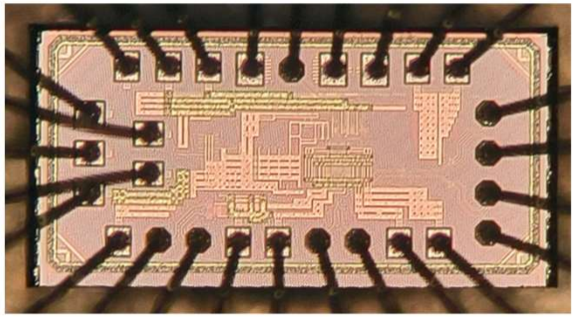
- ~9.5 dB worse signal-to-noise ratio (SNR)
- Higher linearity to preserve four symbols

Research Scope

Retimed Pluggable Optics (RPO)

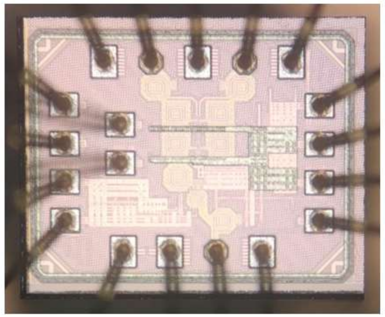


Co-Packaged Optics (CPO)



Work-1: A 1.28-pJ/bit 48-Gb/s PAM-4 Optical Receiver

Linear Pluggable Optics (LPO)



Work-2: A 0.32-pJ/bit 100-Gb/s PAM-4 TIA

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- Background
- **PAM-4 Optical Receiver Data Path**
  - **System Architecture**
  - Implementation
  - Measurement Result
- PAM-4 Optical Receiver Front End
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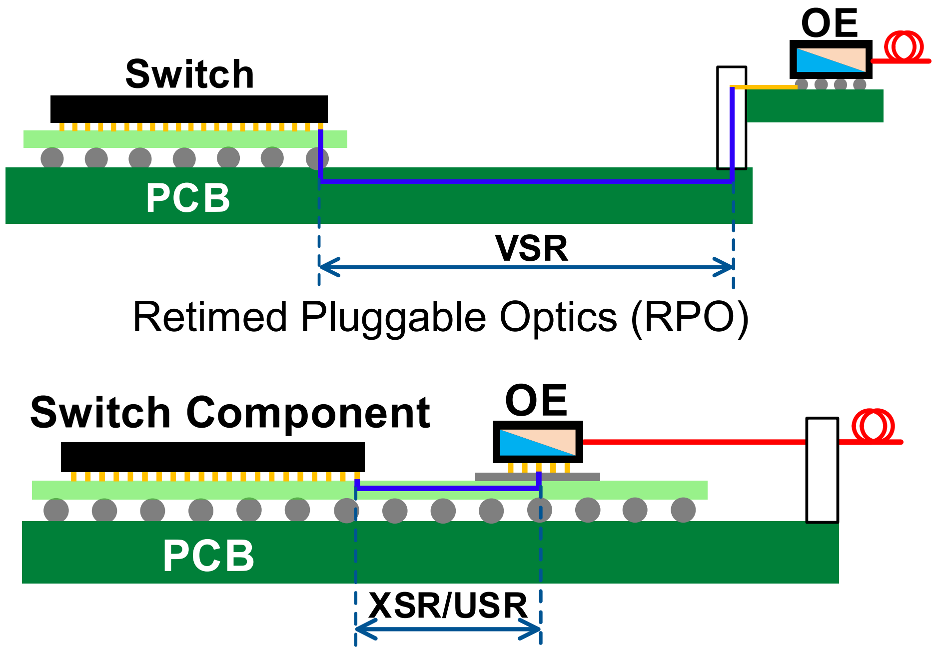
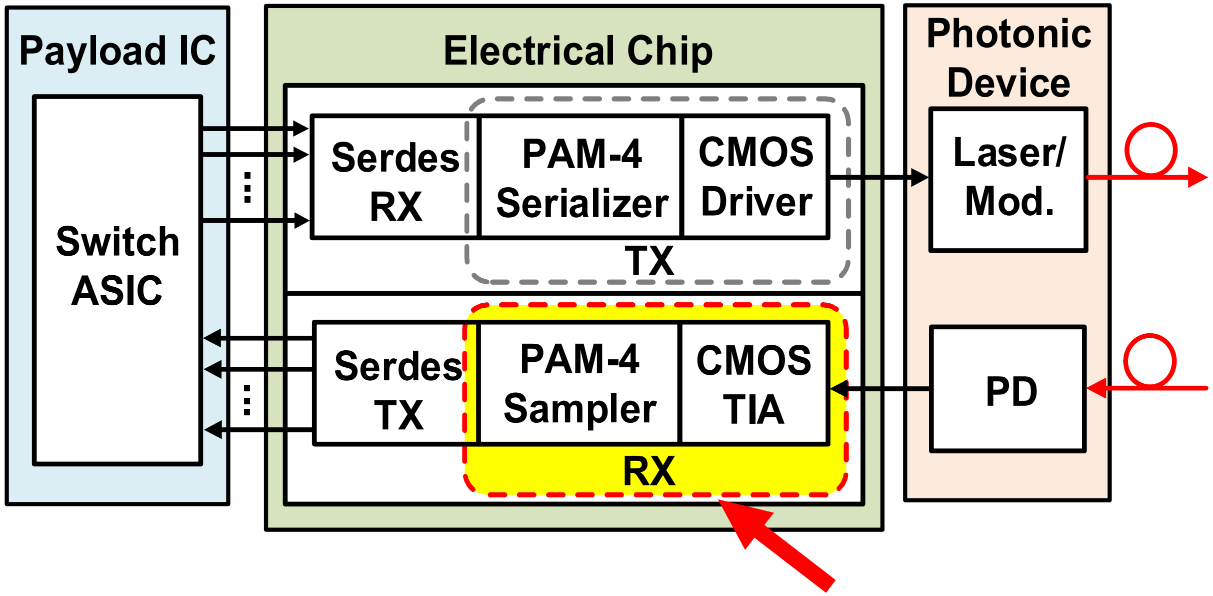
Data Center Optical Interconnect



Retimed Pluggable Optics (RPO)

Co-Packaged Optics (CPO)

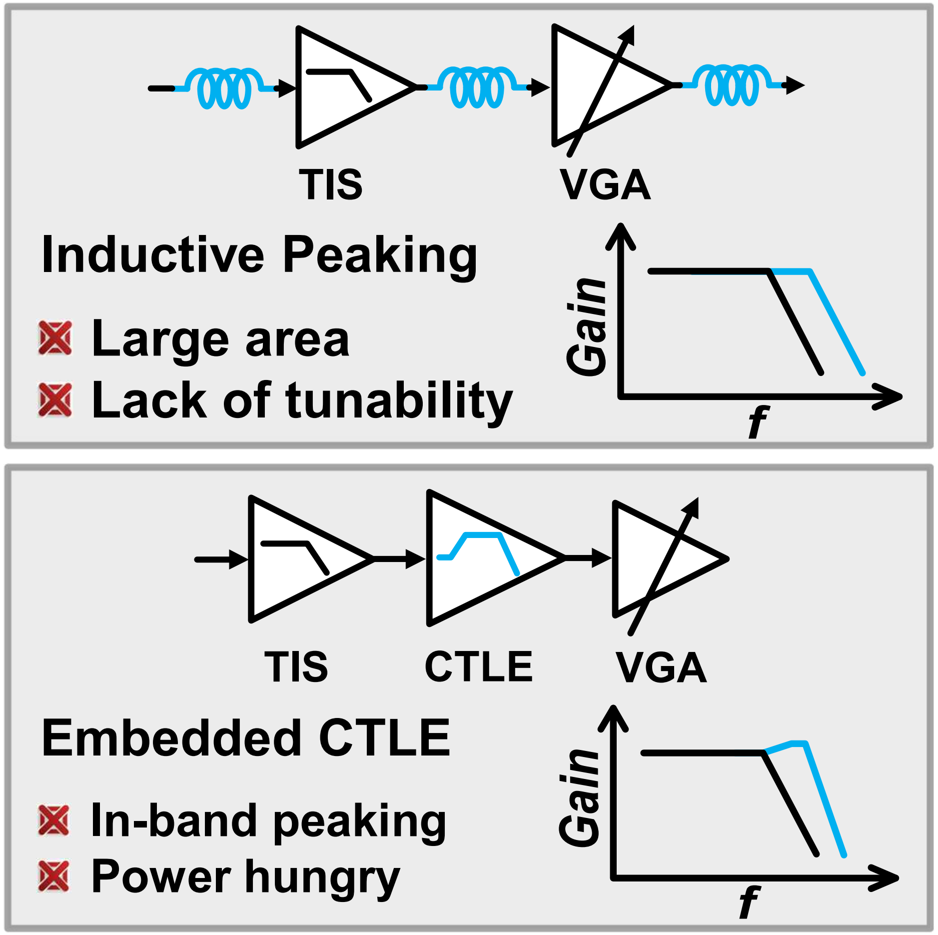


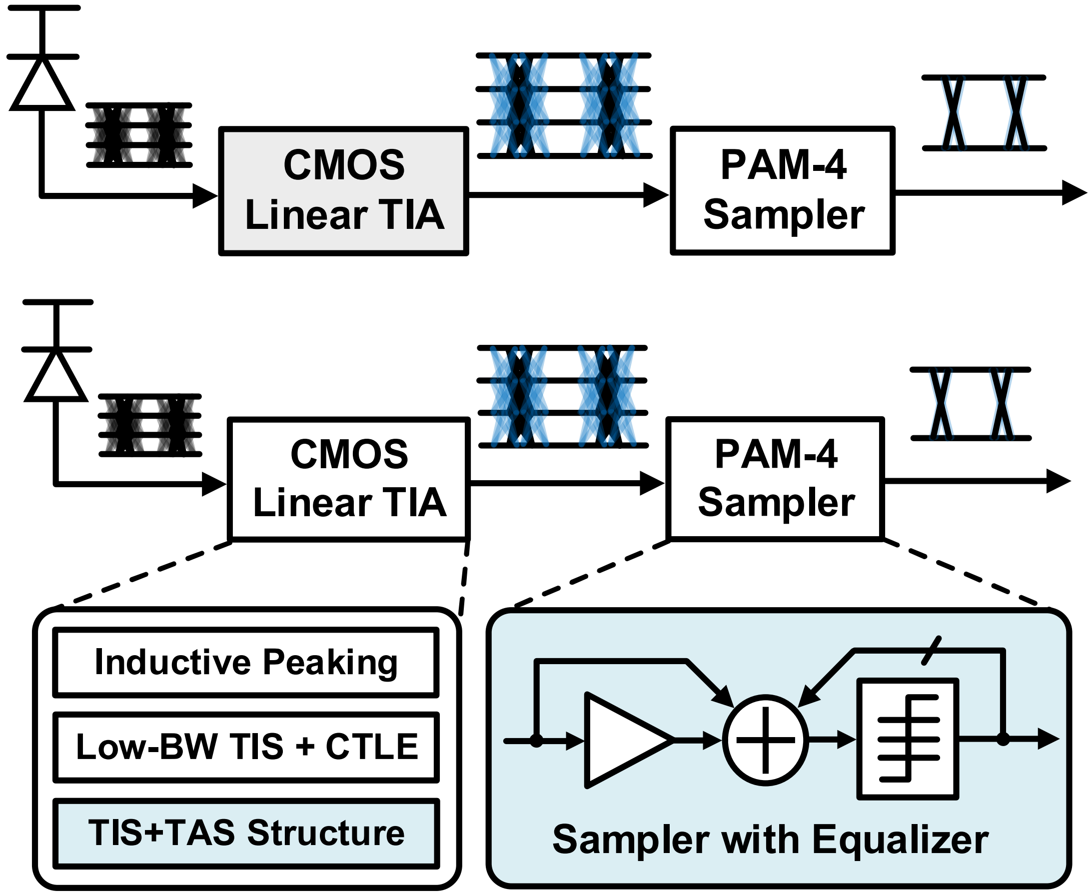
Focus of this work

- Integrating TIA and sampler (deserializer) reduces the overhead and electrical connections
- Low power consumption and low cost for 50-Gb/s link

VSR: very short-reach; XSR: extra short-reach; USR: ultra short-reach

Design Challenges

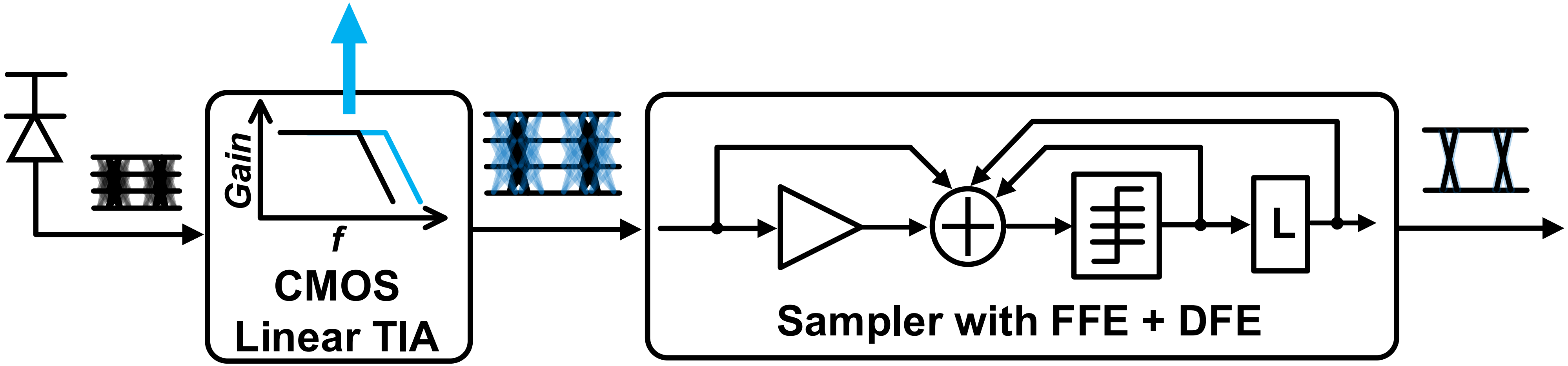




TIS: transimpedance amplifier; VGA: variable gain amplifier; CTLE: continuous-time linear equalizer

RX Architectural Consideration

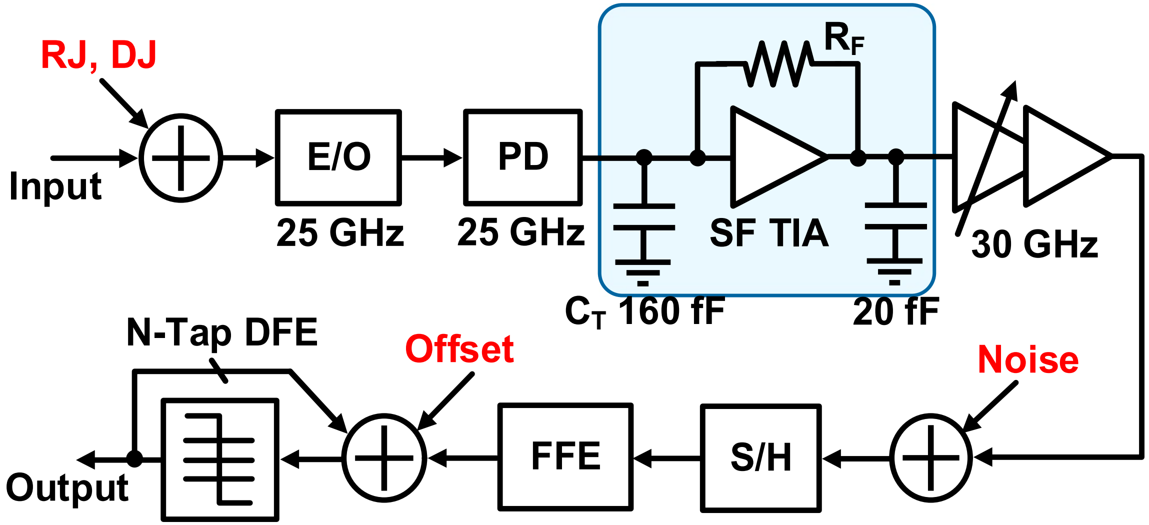
- CTLE is avoided to save power
- Passive inductors are avoided to save area
- Transadmittance-stage transimpedance-stage (TAS-TIS) topology is employed



- Equalizers are integrated at sampler to mitigate the residual ISI of TIA

ISI: intersymbol interference; FFE: feedforward equalizer; DFE: decision feedback equalizer

RX Architectural Consideration



$$BW_{3dB} = \frac{\sqrt{2A_0(A_0+1)}}{2\pi R_F C_T} \approx \frac{\sqrt{2}A_0}{2\pi R_F C_T}$$

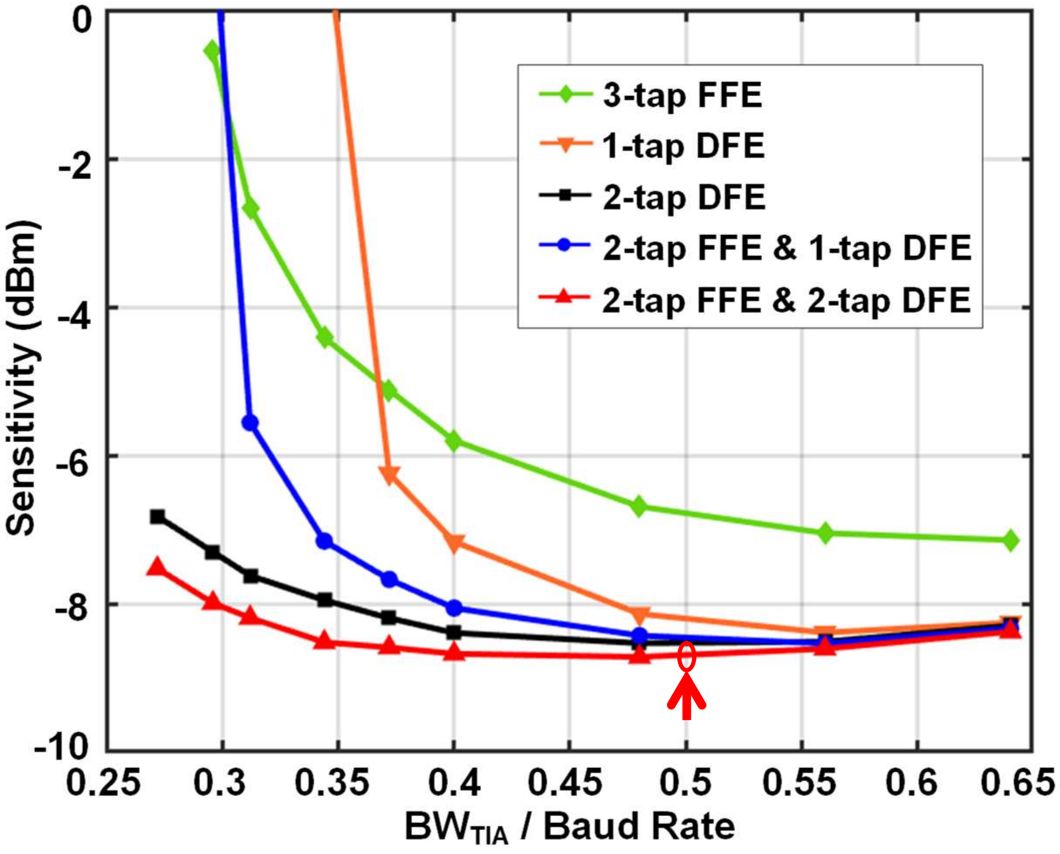
$$\boldsymbol{R_F} = \frac{(A_0+1)\omega_A}{C_T \boldsymbol{BW_{3dB}^2}} \approx \frac{GBW_A}{2\pi C_T BW_{3d}^2}$$

$$\overline{\boldsymbol{i_n^2}} = 4kT\frac{2\pi C_T}{f_T}\boldsymbol{BW_{3dB}^3} \times \left(I_1 \times \frac{f_T}{GBW_A} + \frac{I_2^3}{3} \times 2\gamma\right)$$

- ORX link model to evaluate post-TIA equalization
- TIA model with a second-order flat response

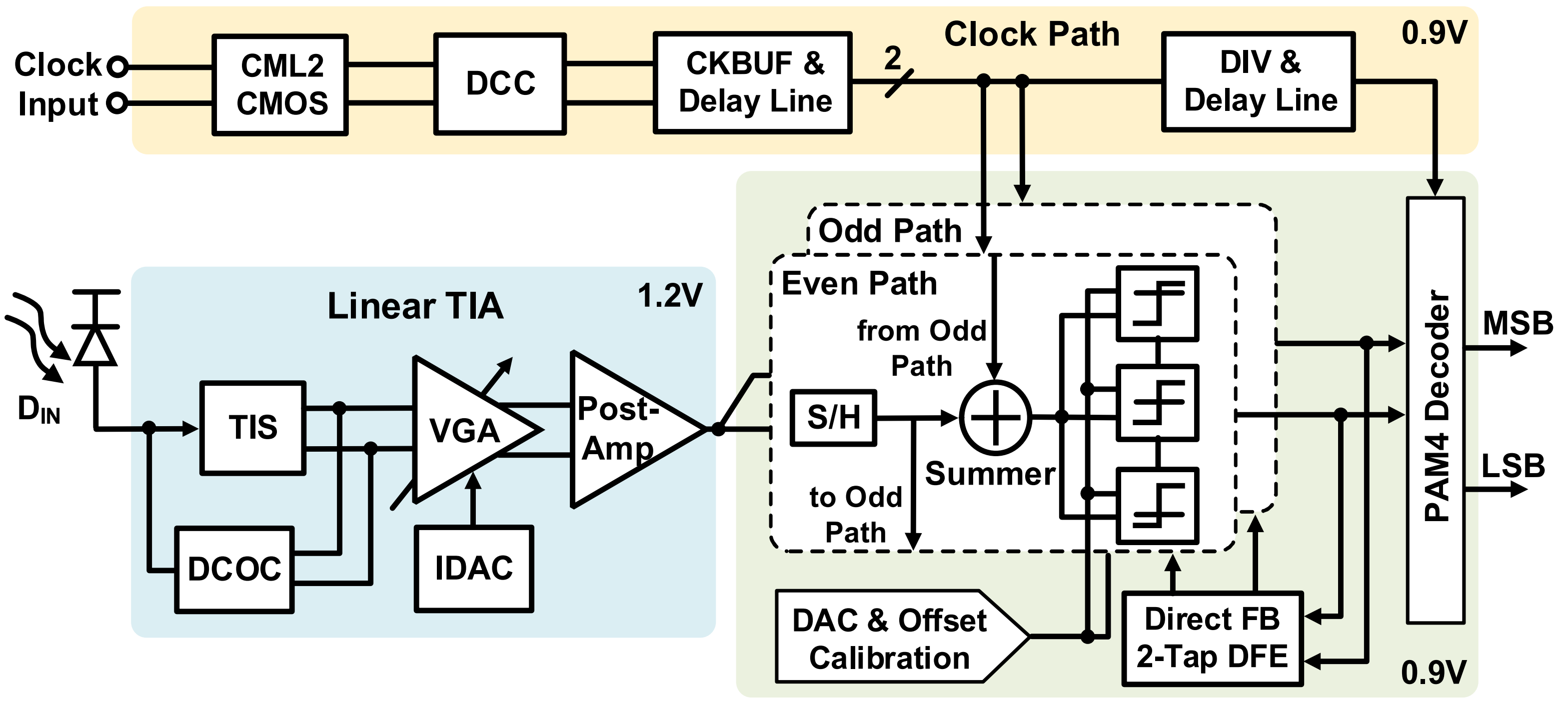
RJ: random jitter; DJ: duty cycle error

RX Architectural Consideration



- BW_{TIA} < 0.45x baud rate, sensitivity is limited by ISI
- BW_{TIA} > 0.45x baud rate, sensitivity is limited by noise
- A combination of a 2-tap FFE and a 2-tap DFE delivers the best overall sensitivity
- Optical receiver (ORX) is designed with a BW_{TIA} of ~0.5x baud rate, followed by a 2-tap FFE and a 2-tap DFE

Proposed Architecture



- **Linear TIA**
  - >73 dBΩ maximum gain
  - >20 dB dynamic range
  - Compact and energy-efficient
- **PAM-4 sampler**
  - Half-rate structure
  - 2-tap FFE + 2-tap DFE
- **Clock path**
  - External differential clock
  - Voltage-controlled delay line
  - Divider (DIV)

DCOC: dc offset cancellation; DCC: duty cycle correction; MSB: most significant bit; LSB: least significant bit

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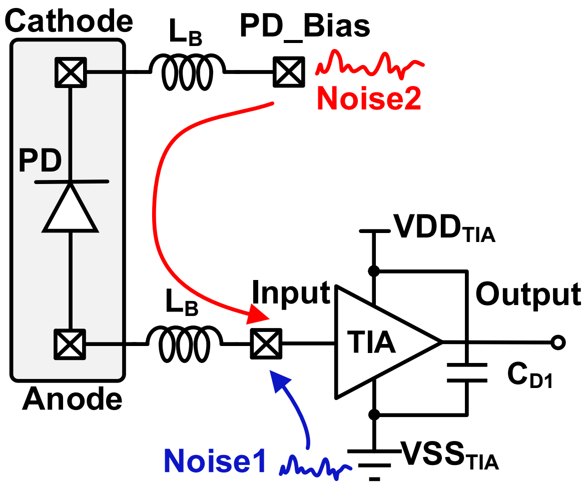
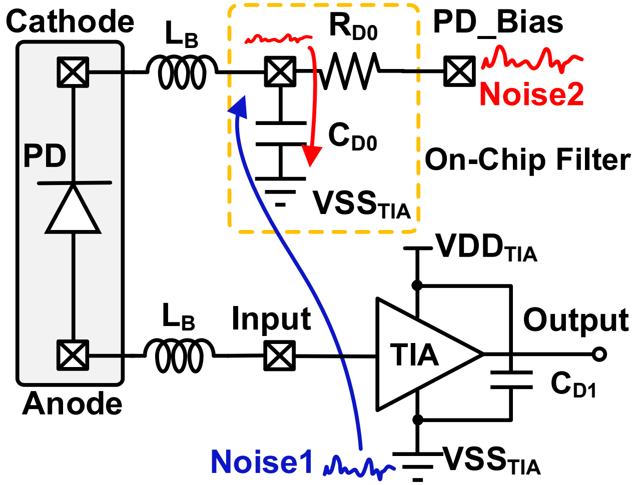
PD Interface and TIS



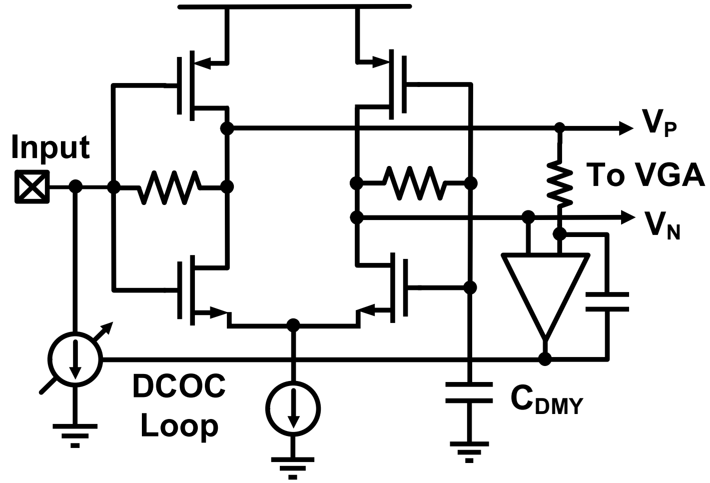
Direct connection scheme

- ✓ Simple and save pads
- ☒ Noise at VSS_{TIA} and PD bias affects the single-ended input signal



On-chip connection scheme

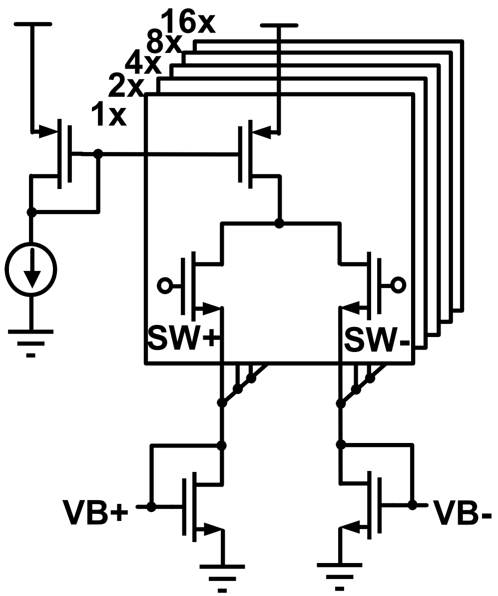
- ✓ Enhanced ground noise rejection by ac-coupled VSS_{TIA} and PD cathode
- ✓ R_{D0} and C_{D0} provide on-chip filtering for noise2

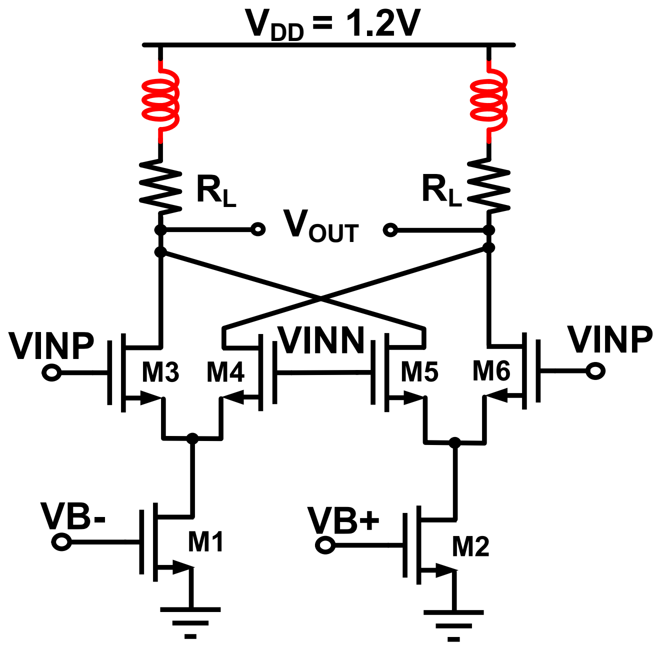


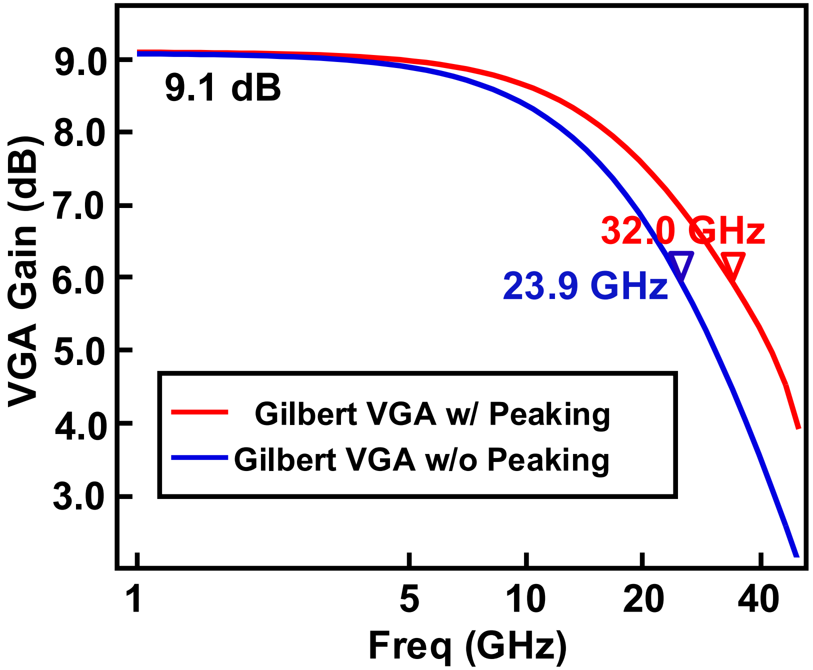
Schematic of TIS with DCOC

- Pseudo-differential push-pull TIS provides single-to-differential conversion
- Current tail for better supply noise rejection

Gilbert-Cell-Based VGA







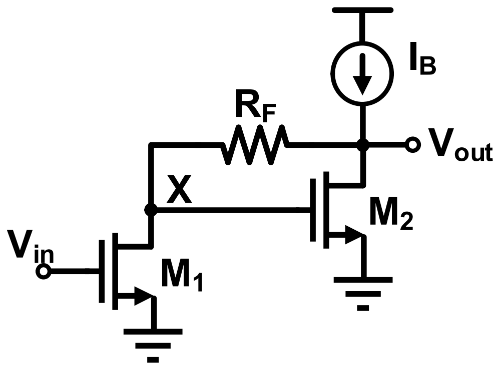
- 5-bit current DAC for Gm control
- Gain = Gm*$R_{L,}$ fixed load impedance: R_L
- Shunt peaking required to expand BW

- Two 580-pH inductors required to expand the BW to 32 GHz

VGA Employing TAS-TIS Topology

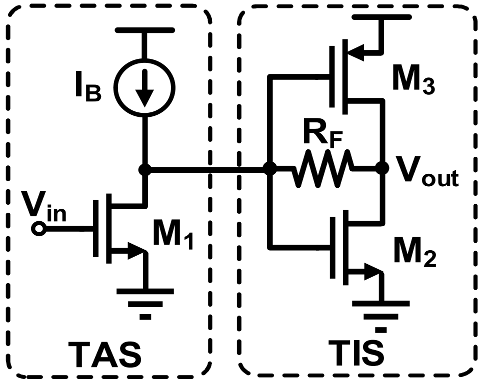
Cherry-Hooper Amp

- $z_X \approx \frac{1}{g_{m2}}$
- $z_{out} \approx \frac{1}{g_{m2}}$

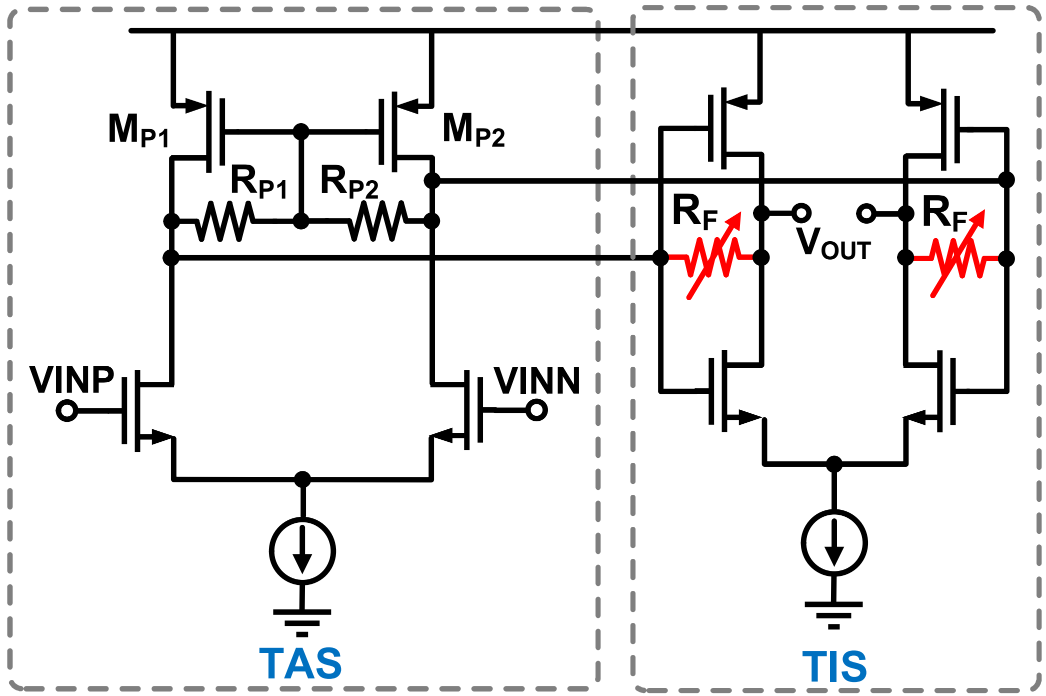


TAS-TIS topology

- Modified Cherry-Hooper Amplifier
- Split into two stages: TAS and TIS

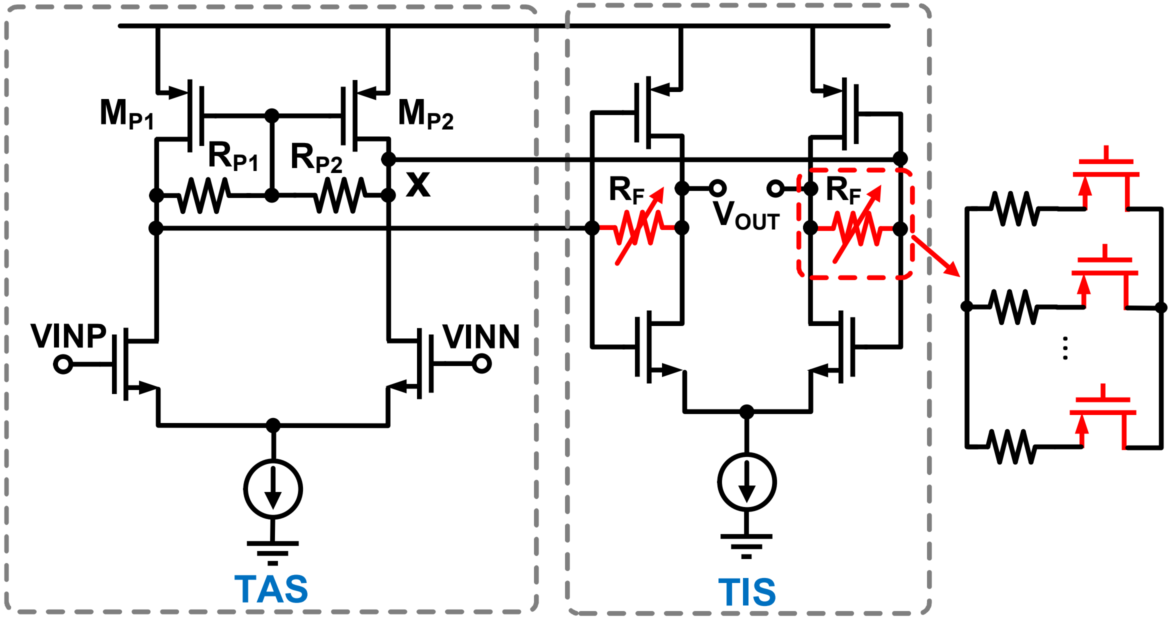


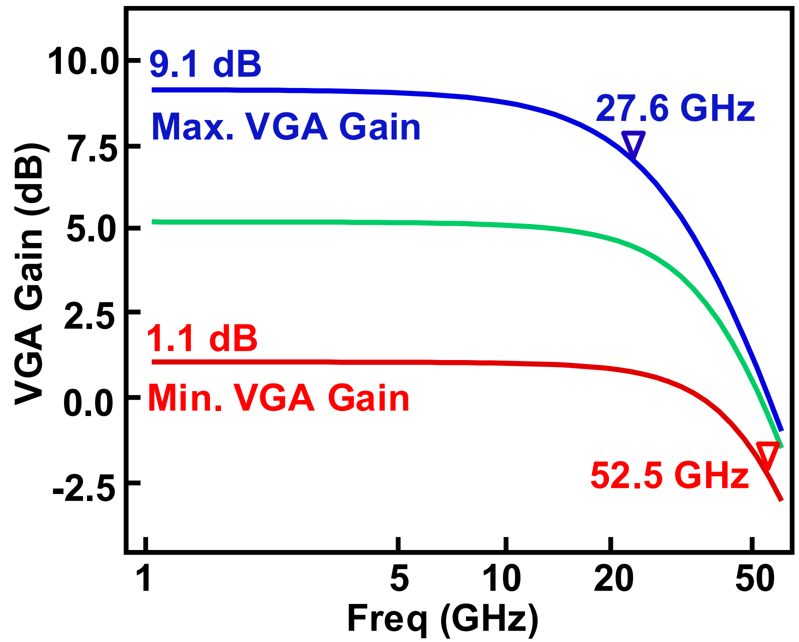
VGA employing a TAS-TIS topology



TAS: transadmittance stage TIS: transimpedance stage

VGA Employing TAS-TIS Topology

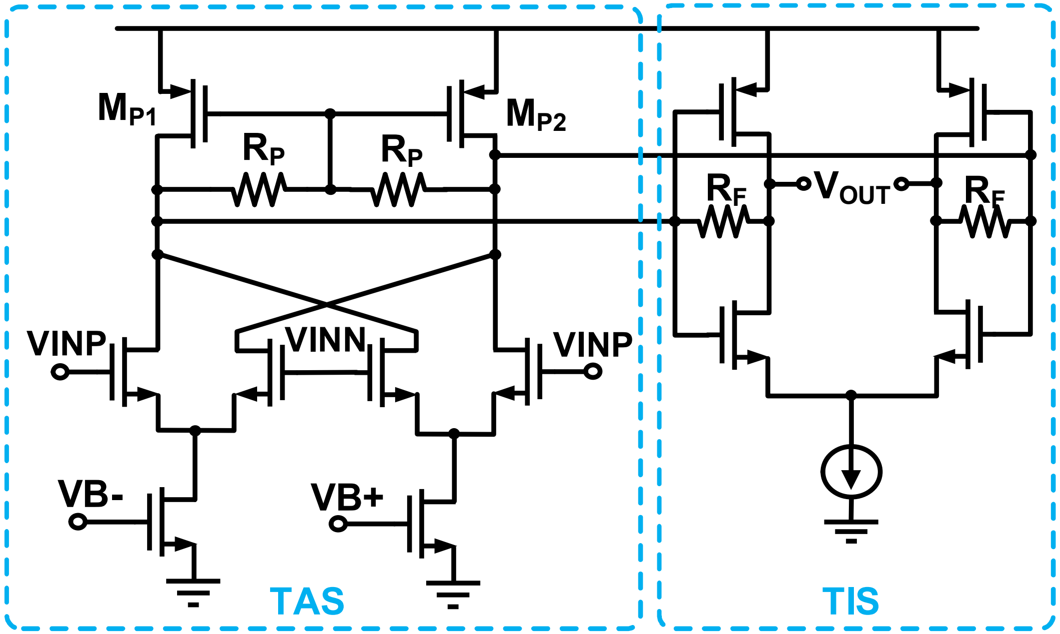


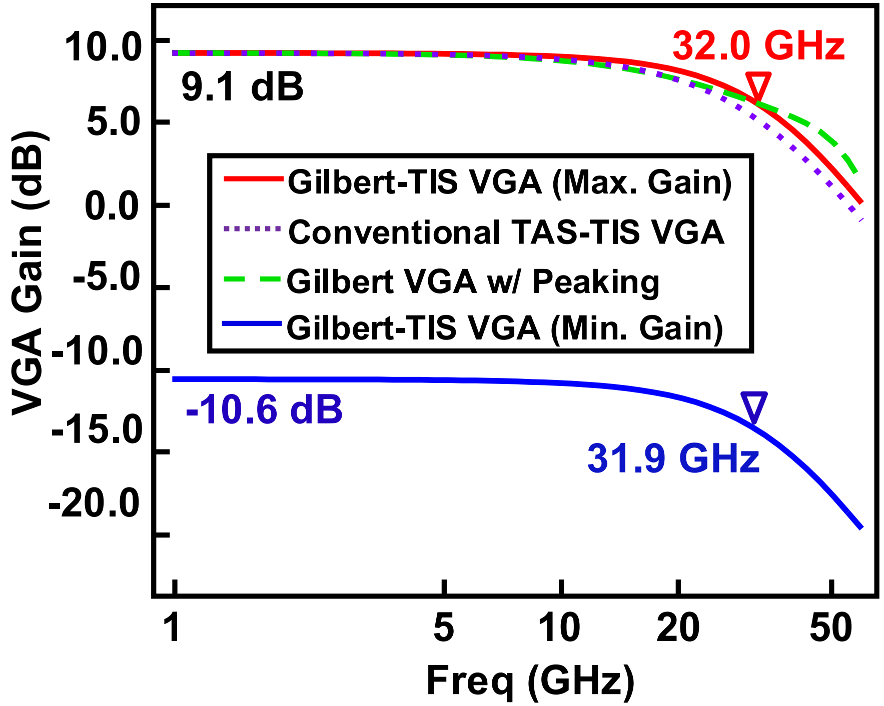


- Gain $= Gm_{TAS} \times R_F$
- Load impedance of TAS: R_F/A_{TIS}, higher BW
- Output impedance: $1/Gm_{TIS}$, larger driving capacity
- Variable R_F causes BW variations over gain variations
- Switches for R_F control bring extra parasitics

- 3-bit TAS-TIS VGA
- 8-dB gain tuning range
- ~25-GHz BW variation

Proposed Gilbert-TIS VGA

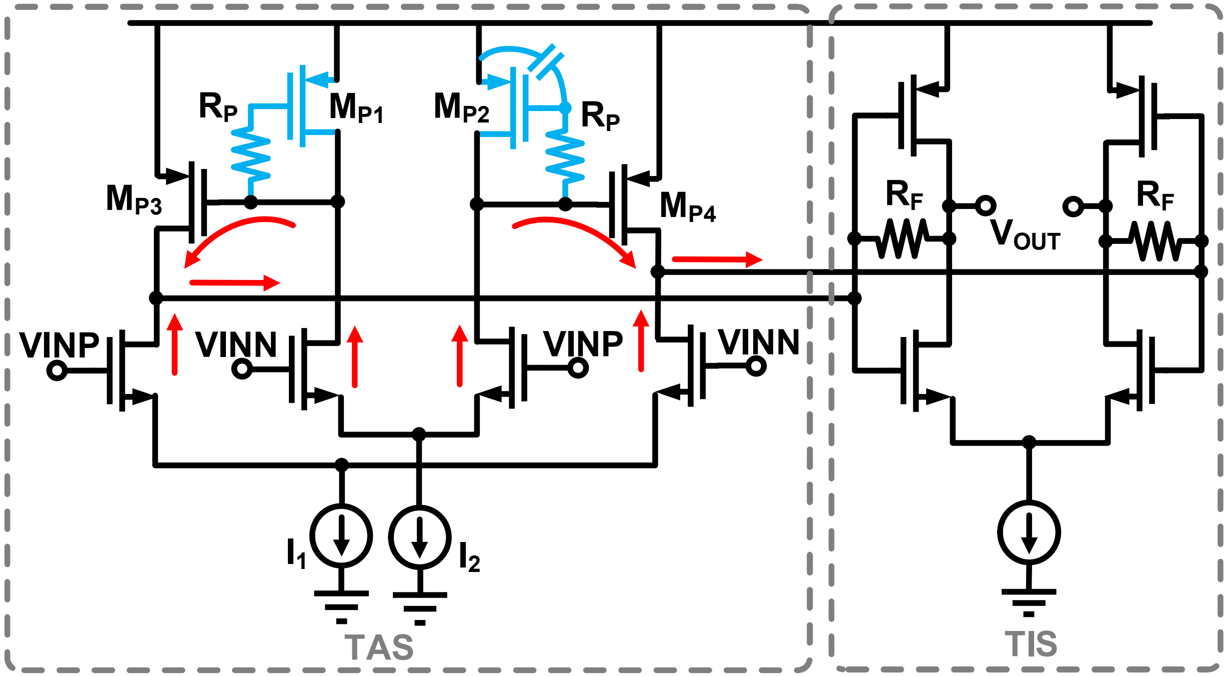


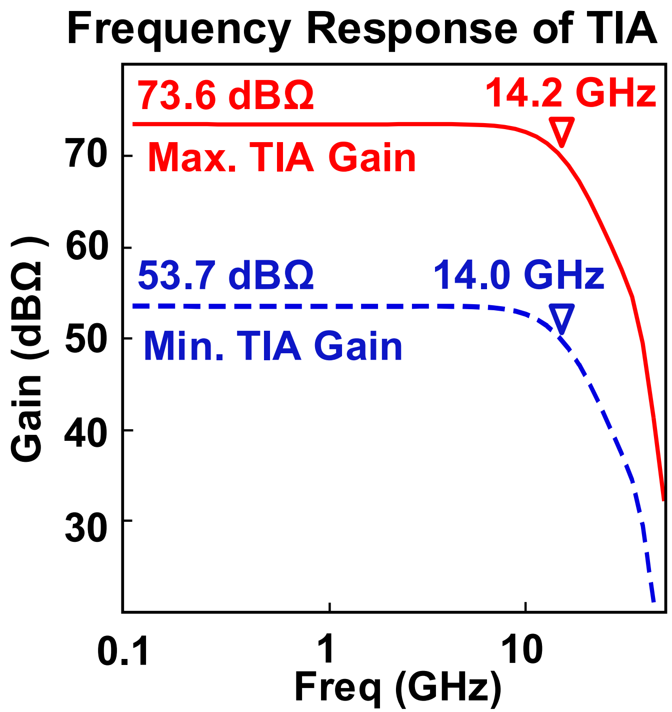


- Load impedance of TAS: R_F/A_{TIS}, higher BW
- Output impedance: $1/Gm_{TIS}$, larger driving capacity
- Fixed R_F mains a constant BW over gain variations
- CML-based TAS to get fully differential signal

- High gain-BW product
- <0.2-GHz BW variation

Post-Amp Design and TIA Frequency Response

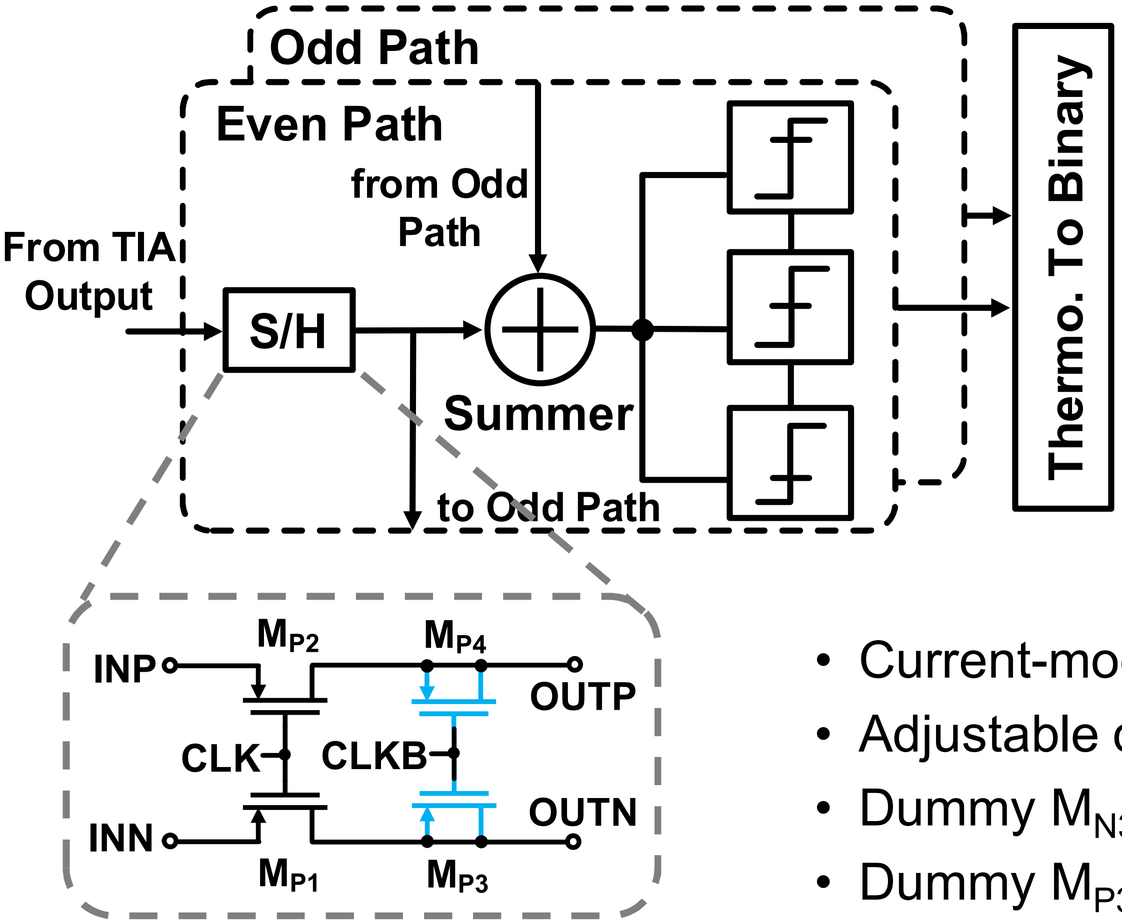


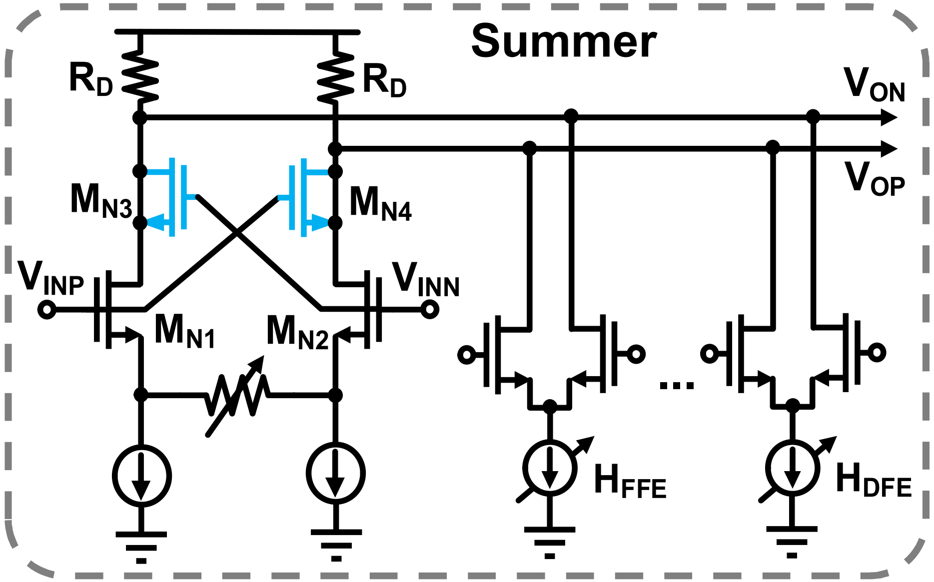


- TAS-TIS topology
- Two differential pairs to achieve high Gm_{TAS}
- R_P, M_{P1}, M_{P2} form active inductors to expand BW

- TIA achieves 73.6-dBΩ max. gain with 14.2-GHz BW
- < 0.3 GHz BW variation

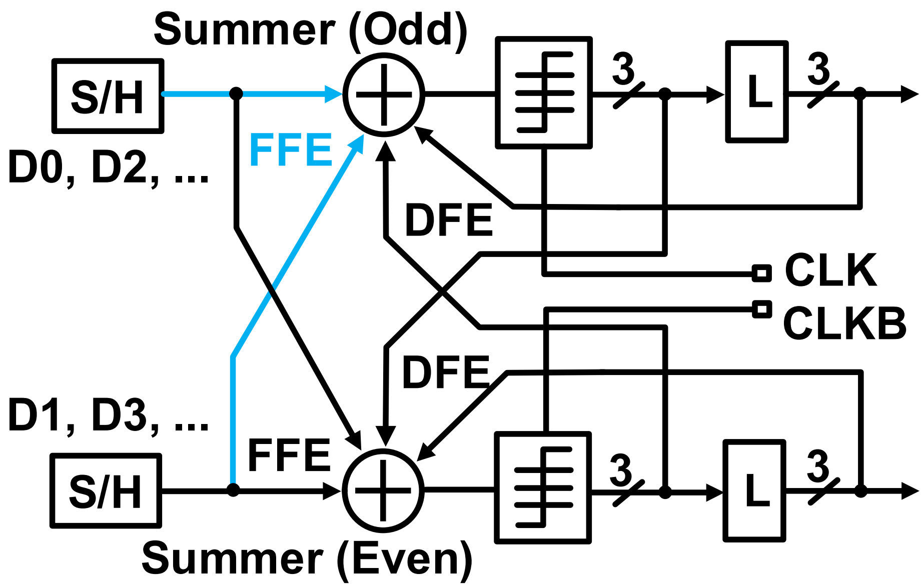
Sampler with Integrated Equalizer

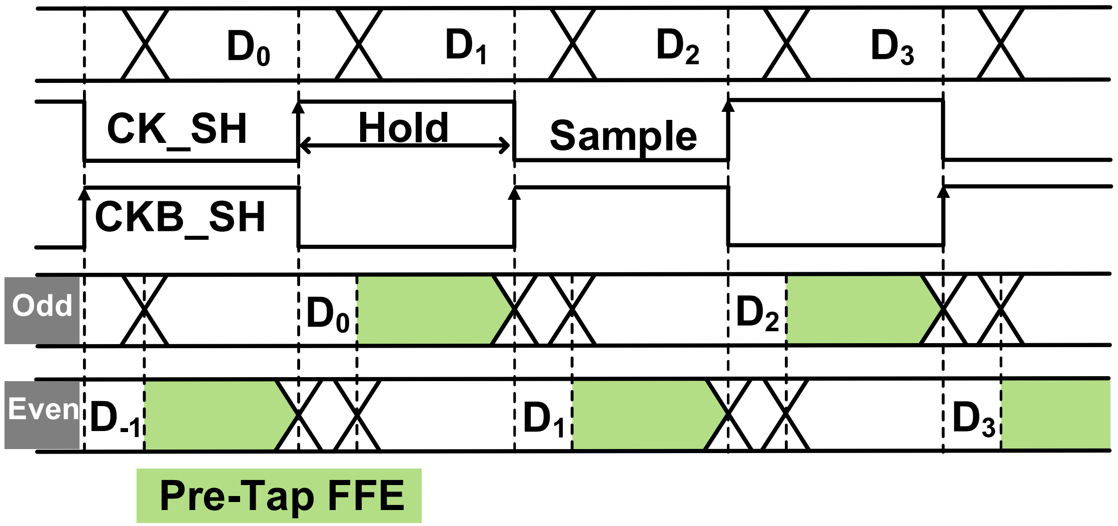




- Current-mode summer with resistive load
- Adjustable degeneration resistor to improve linearity
- Dummy M_{N3}/M_{N4} to reduce feedback from V_{OP}/V_{ON}
- Dummy M_{P3}/M_{P4} to mitigate clock through from M_{P1}/M_{P2}

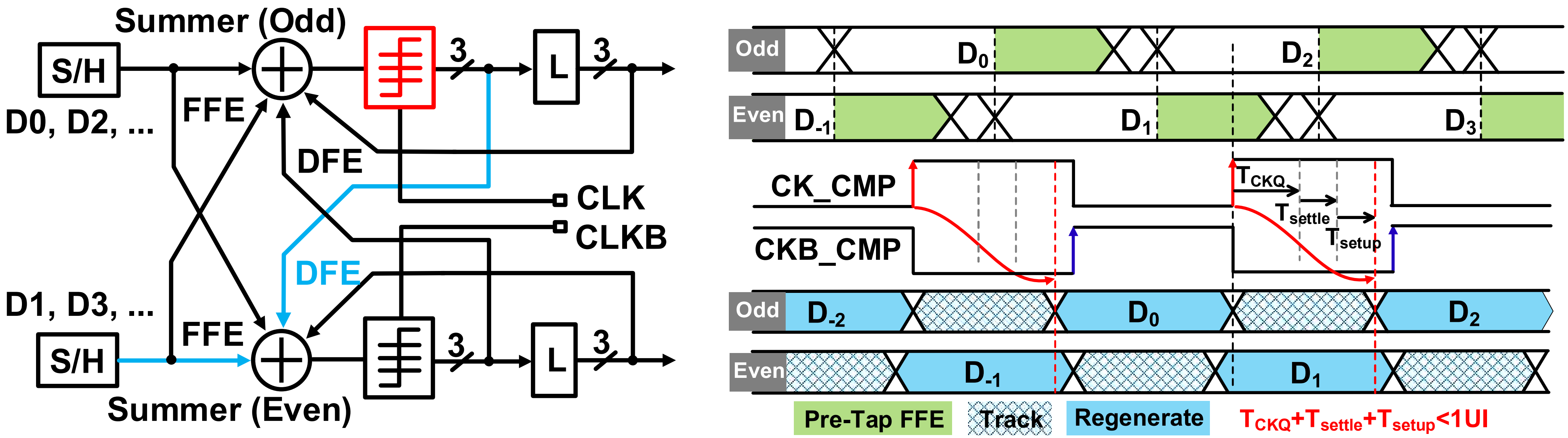
FFE and Summer Timing Diagram





- Data is sampled and held for 1 UI by S/H circuits using CK_SH and CKB_SH alternatively
- Data in the even path experiences an 1-UI delay relative to the odd path
- 0.5-UI precursor of D_1 is cancelled by subtracting D_2 from D_1

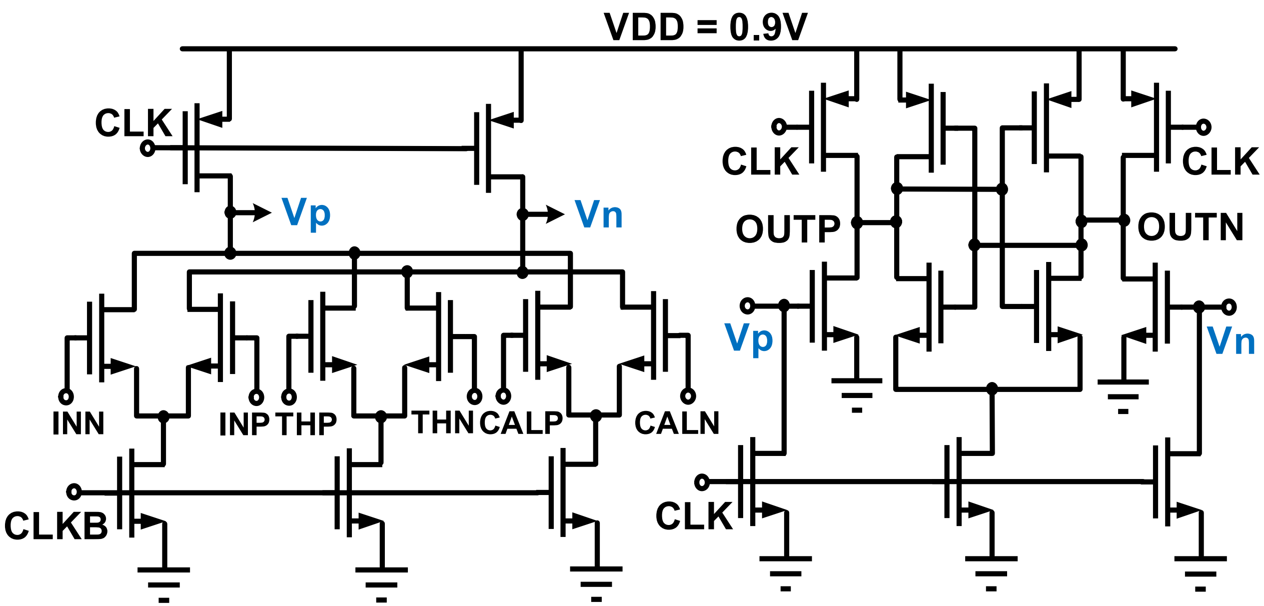
DFE and Summer Timing Diagram

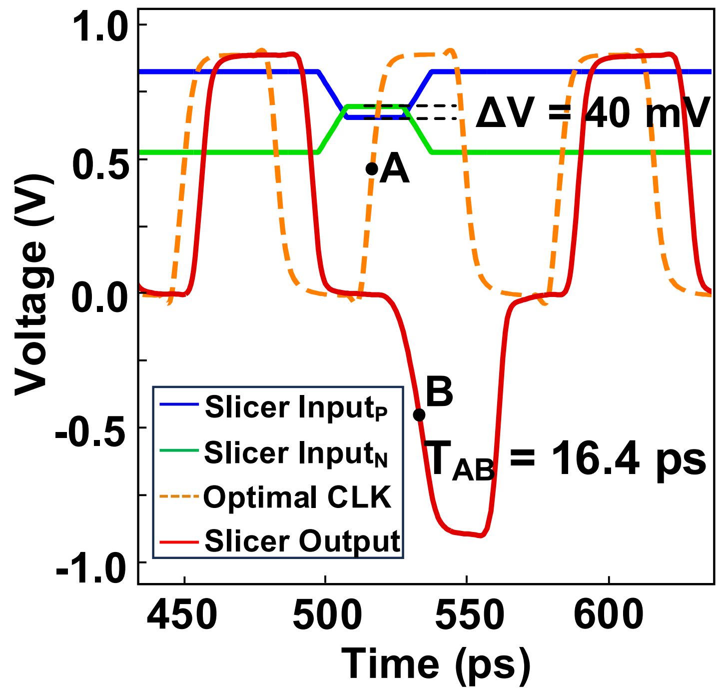


- Before D_1 is sliced by the rising edge of CK_CMP, D_0 must be regenerated and subtracted from D_1
- Stringent timing constrain to close decision feedback loop for the first tap
- 1-UI < 42ps for 48-Gb/s PAM-4 operation
- The delay performance of slicers is critical: **reduce T_{CKQ}**

UI: unit interval

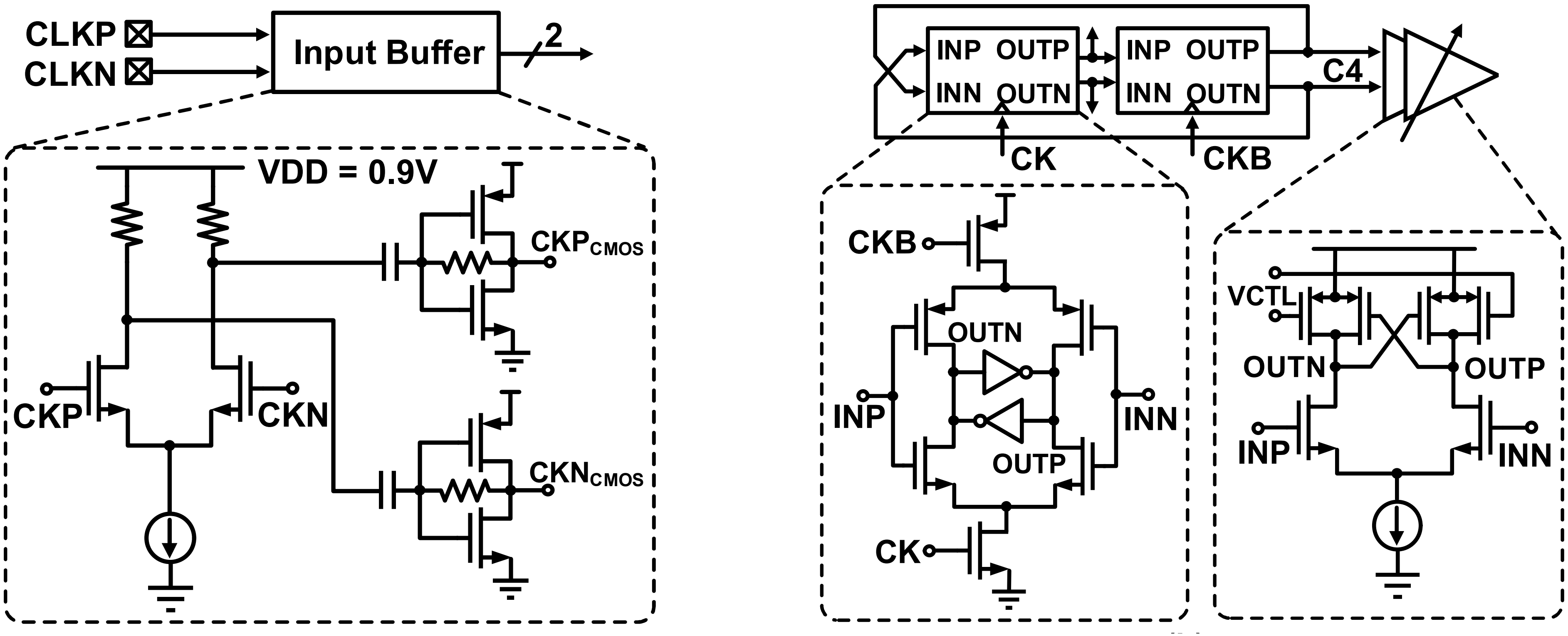
Track-and-Regenerate Slicer





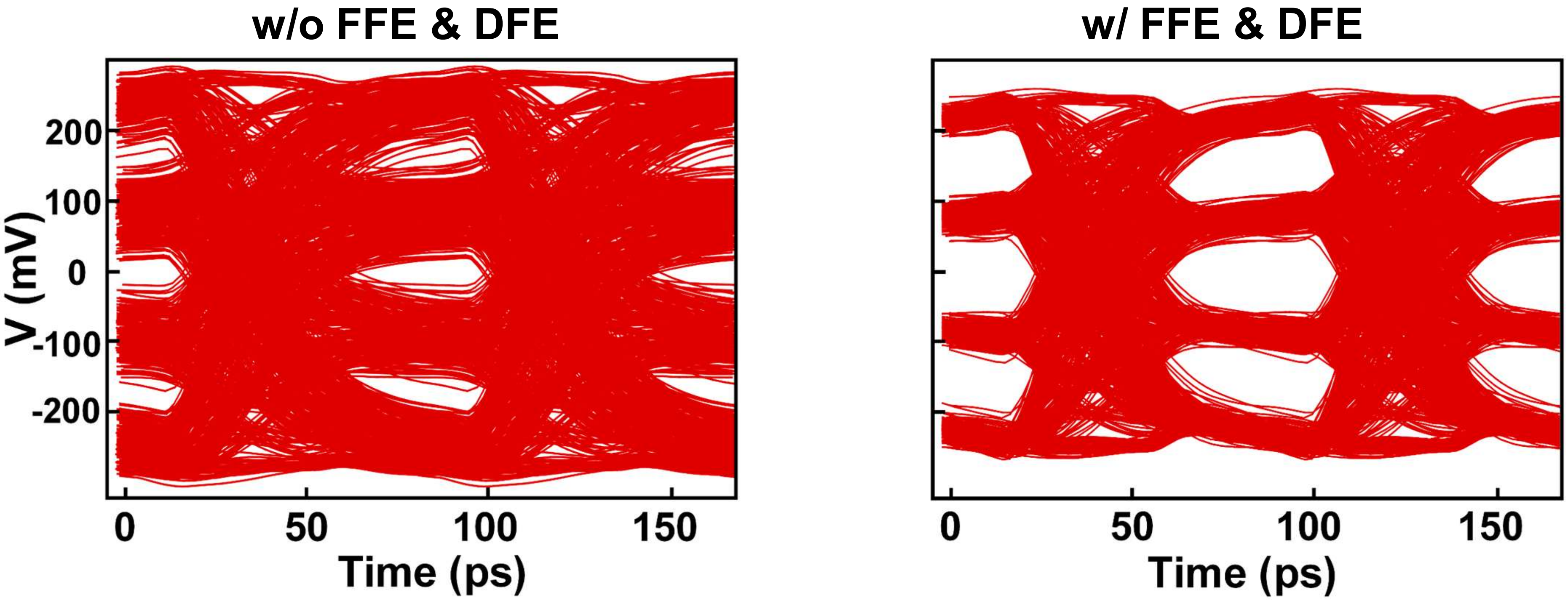
- Track-and-regenerate slicer
- CLK=0, CLKB=1, input tracked by Vp and Vn, latch is charged to V_{DD}
- CLK=1, CLKB=0, Vp and Vn discharged to V_{SS}, latch regenerates signal
- Optimized clock-to-Q delay, < 17ps

Clock Path



- CML to CMOS clock buffer amplifies sinusoidal clock signals to rail-to-rail
- C^2MOS frequency divider is used to provide clock signals for PAM-4 decoder
- Delay line controlled by a 6-bit R2R ladder is used to accommodate delay variations

Simulated Eye Diagram at Summer Output



- 48-Gb/s PAM-4 input with 220-uA amplitude, 70-fF PD, 1.5-ps RJ
- Eye diagrams of half-rate 24-Gb/s PAM-4 at summer output before decoding
- Coefficients of FFE, first-tap DFE, second-tap DFE: 0.07, 0.08, 0.01

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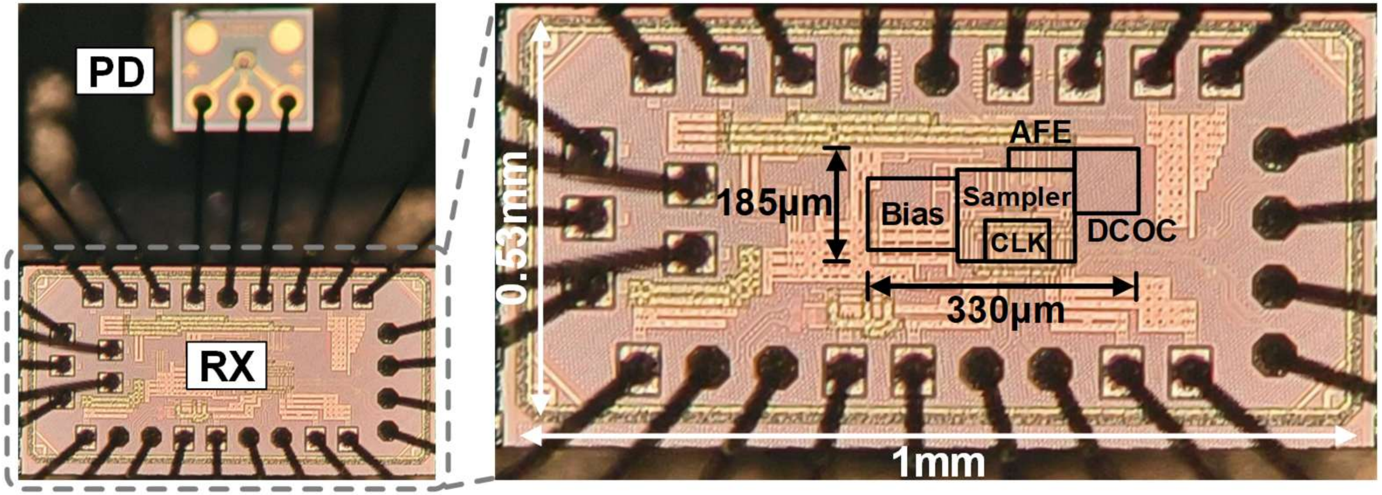
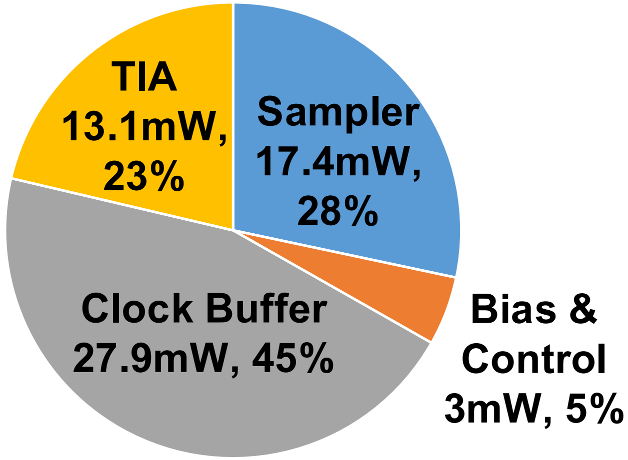
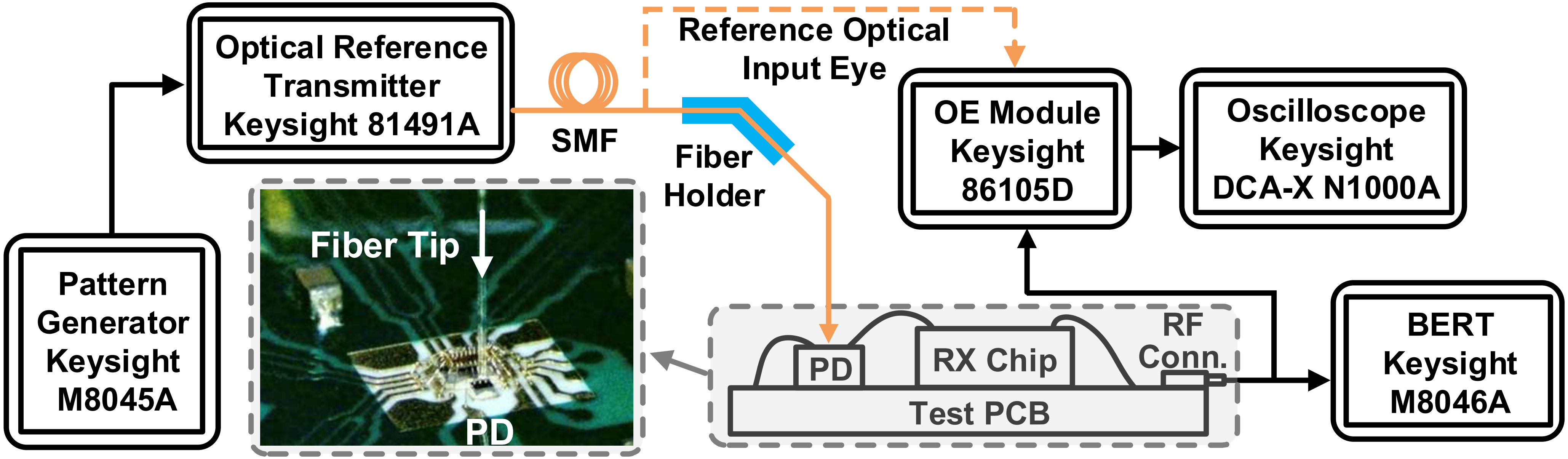
Die Photo and Power Breakdown





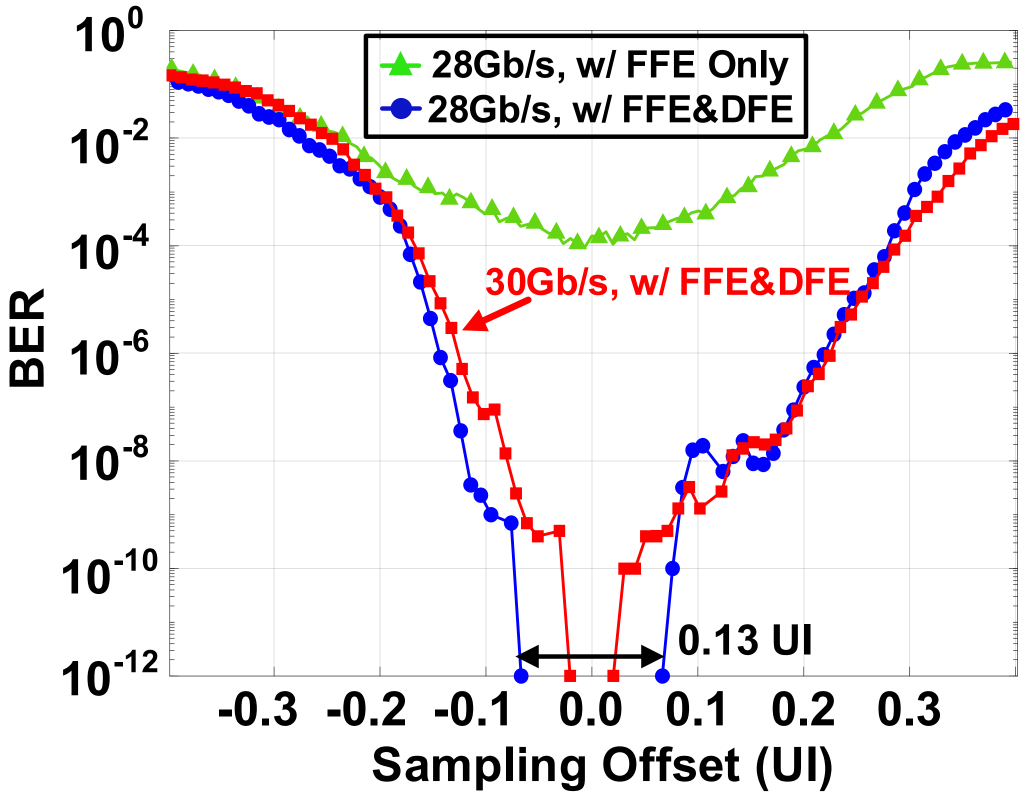
- Fabricated in a 28-nm bulk CMOS
- ~0.06 mm^2 core area for ORX
- Wire-bonded to a 27-GHz PD with 0.75-A/W responsivity
- 61.4 mW at 48-Gb/s in total, TIA contributing 13.1 mW

Measurement Setup



- 1308-nm light source is coupled to PD through a single-mode fiber
- Optical power level is adjusted by an internal optical attenuator
- Deserialized MSB and LSB are sent to off-chip BER testing

NRZ BER Bathtub Curves

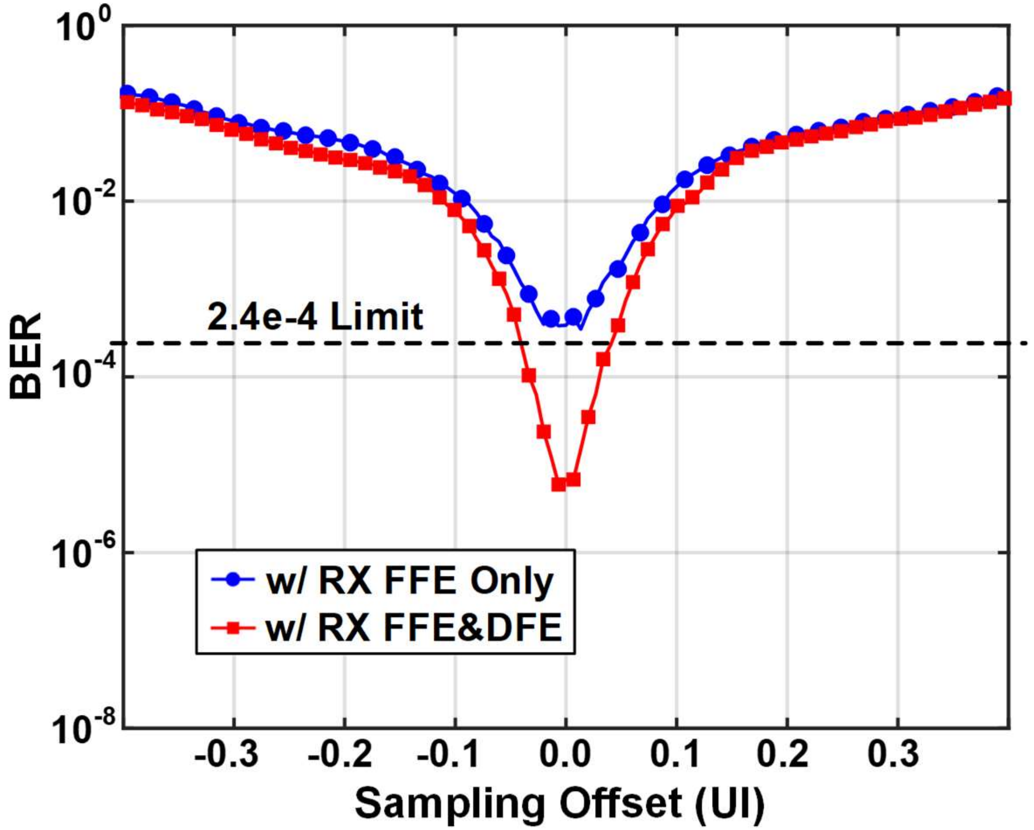


NRZ input signal

- All data slicers are enabled without PAM-4 threshold voltages
- 28-Gb/s NRZ input with -8.0-dBm input OMA
- 30-Gb/s NRZ input with -7.7-dBm input OMA
- 1e-12 BER at 30-Gb/s validate slicer design and DFE operation

BER: bit error rate; OMA: optical modulation amplitude

PAM-4 BER Bathtub Curves

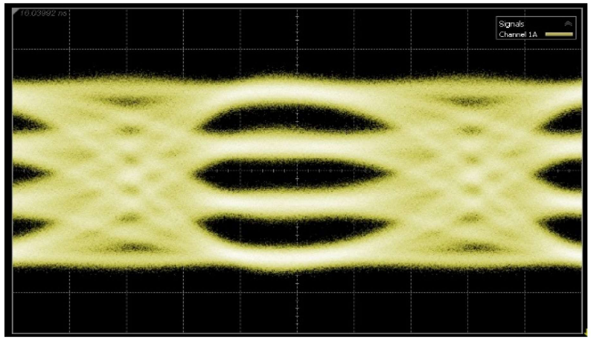


PAM-4 input signal

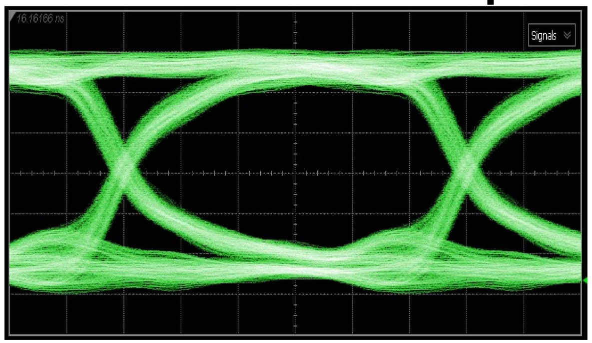
- 48-Gb/s PAM4 with -4.6-dBm input OMA
- Only enabling FFE, BER is higher than pre-FEC limit
- After enabling both FFE and DFE, BER is improved to < 1e-5

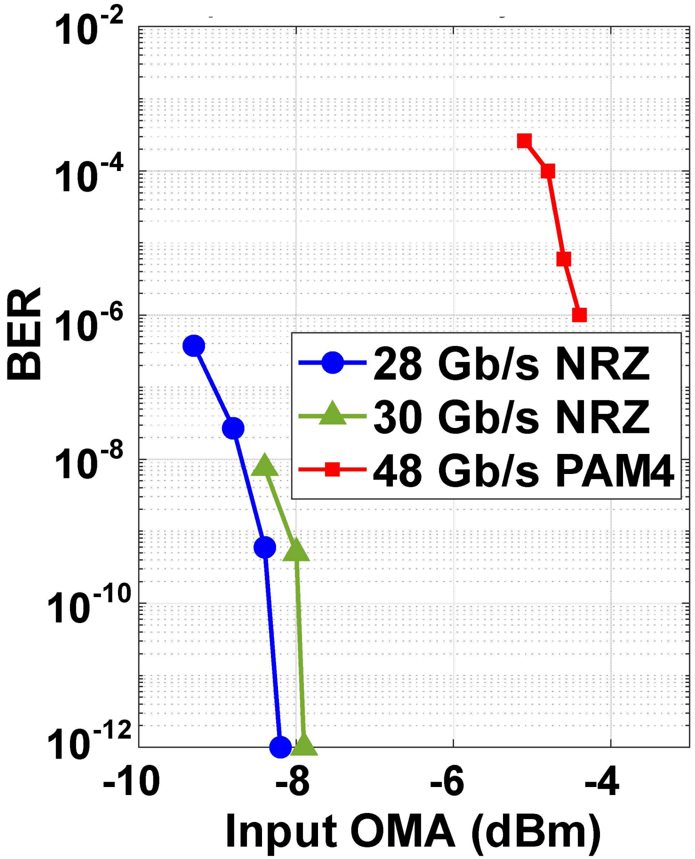
ORX Sensitivity

48-Gb/s PAM4 Optical Input



Decoded 6-Gb/s Output





- PAM-4 optical input with 4.8-dB extinction ratio
- Under 1e-12 BER target, -8.2-dBm sensitivity at 28-Gb/s NRZ is achieved
- Under 2.4e-4 BER target, -5.1-dBm sensitivity at 48-Gb/s PAM-4 is achieved

Comparison Table

	JSSC'21 [1]		OJCAS'21[2]	JSSC'22 [3]		RFIC'23 [4]	VLSI'24 [5]		**This Work**	
Technology	65nm CMOS		40nm CMOS	28nm CMOS		28nm CMOS	22nm FinFET		**28nm CMOS**	
Data Rate (Gb/s)	16 (Duobinary)		36 (PAM-4)	100 (PAM-4)		42.7 (NRZ)	50 (NRZ)		**48 (PAM-4)**	
PD Capacitance (fF)	180		100	70		N/A	100		**60**	
PD Responsivity (A/W)	0.8		0.8	1		0.8	0.48		**0.75**	
NRZ OMA Sens. at BER 1e-12 (dBm)	-11.6		N/A	-11.1 @56Gb/s		-3.6	-6		**-8.2 @28Gb/s**	
PAM-4 OMA Sens. at BER 2.4e-4 (dBm)	N/A		-4.8*	-8.9		N/A	N/A		**-5.1**	
RX EQ Capabilities	N/A		2-tap DFE	2-tap FFE + 2-tap DFE		CTLE	CTLE + 2-tap FFE		**2-tap FFE + 2-tap DFE**	
Area (mm²)	0.09		0.23	0.45		0.11**	0.32 (TIA + RX)		**0.06**	
Power (mW)	4.0 (TIA)	11.2 (ORX)	128.8 (RX)	117 (TIA)	381 (RX)	145.2** (RX)	15.8 (TIA)	75.9 (ORX)	**13.1 (TIA)**	**61.4 (RX)**
Efficiency (pJ/bit)	0.25	0.7	4.0	1.17	3.9	3.4	0.38	1.5	**0.27**	**1.28**
FoM (Gbps/mm²/mW)	2570		473	1725		889	622		**2589**	

*Estimated from reported sensitivity curve **CDR included FoM = Data Rate / Area / Input OMA Sensitivity

Outline

- Background
- PAM-4 Optical Receiver Data Path
- **PAM-4 Optical Receiver Front End**
  - **System Architecture**
  - Implementation
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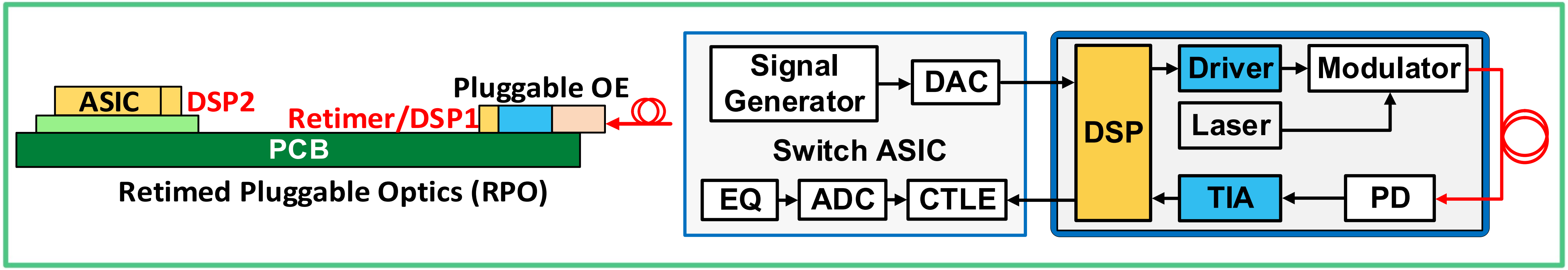
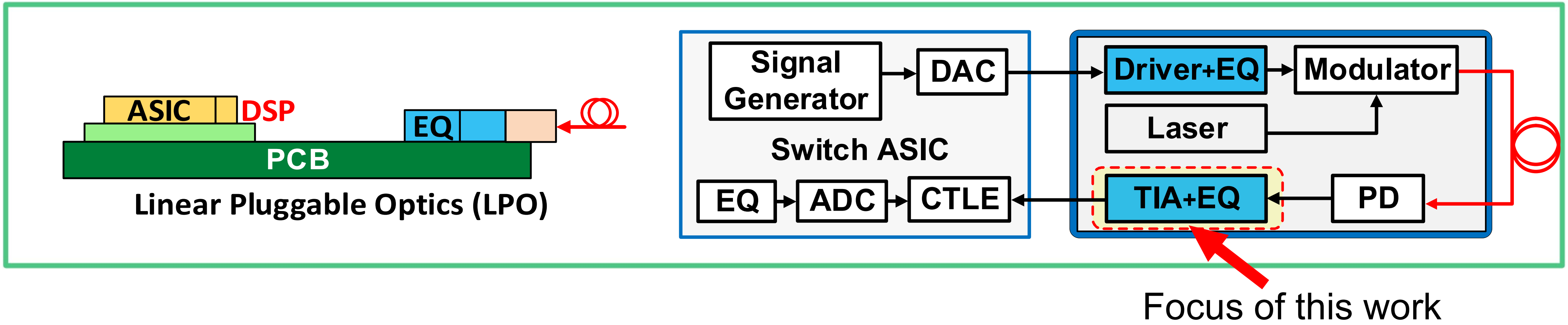
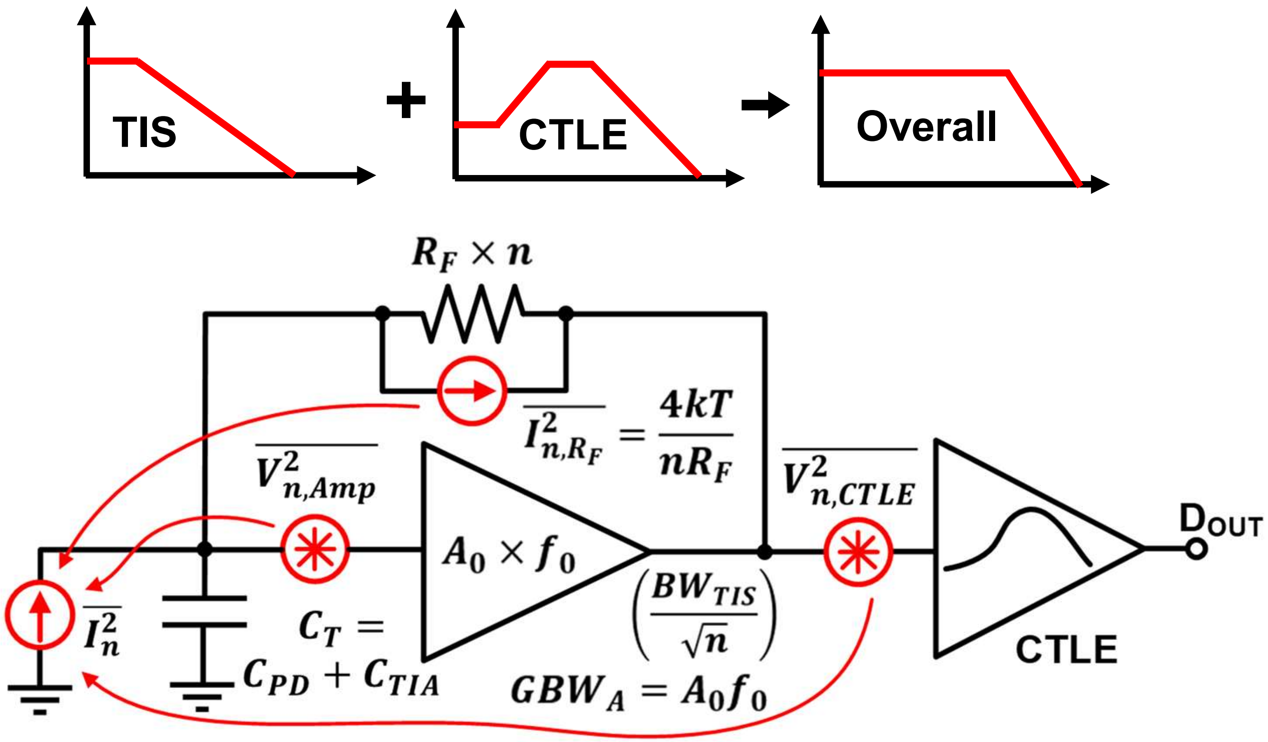
Motivation


ASIC
DSP2
Pluggable OE
Retimer/DSP1
PCB
Retimed Pluggable Optics (RPO)
Signal Generator
DAC
Switch ASIC
EQ
ADC
CTLE
DSP
Driver
Modulator
Laser
TIA
PD


ASIC
DSP
EQ
PCB
Linear Pluggable Optics (LPO)
Signal Generator
DAC
Switch ASIC
EQ
ADC
CTLE
Driver+EQ
Modulator
Laser
TIA+EQ
PD
Focus of this work

Architectural Consideration



$$R_F = \frac{(A_0+1)\omega_A}{C_T BW^2_{\mathrm{TIS}}} \approx \frac{GBW_A}{2\pi C_T BW^2_{\mathrm{TIS}}}$$

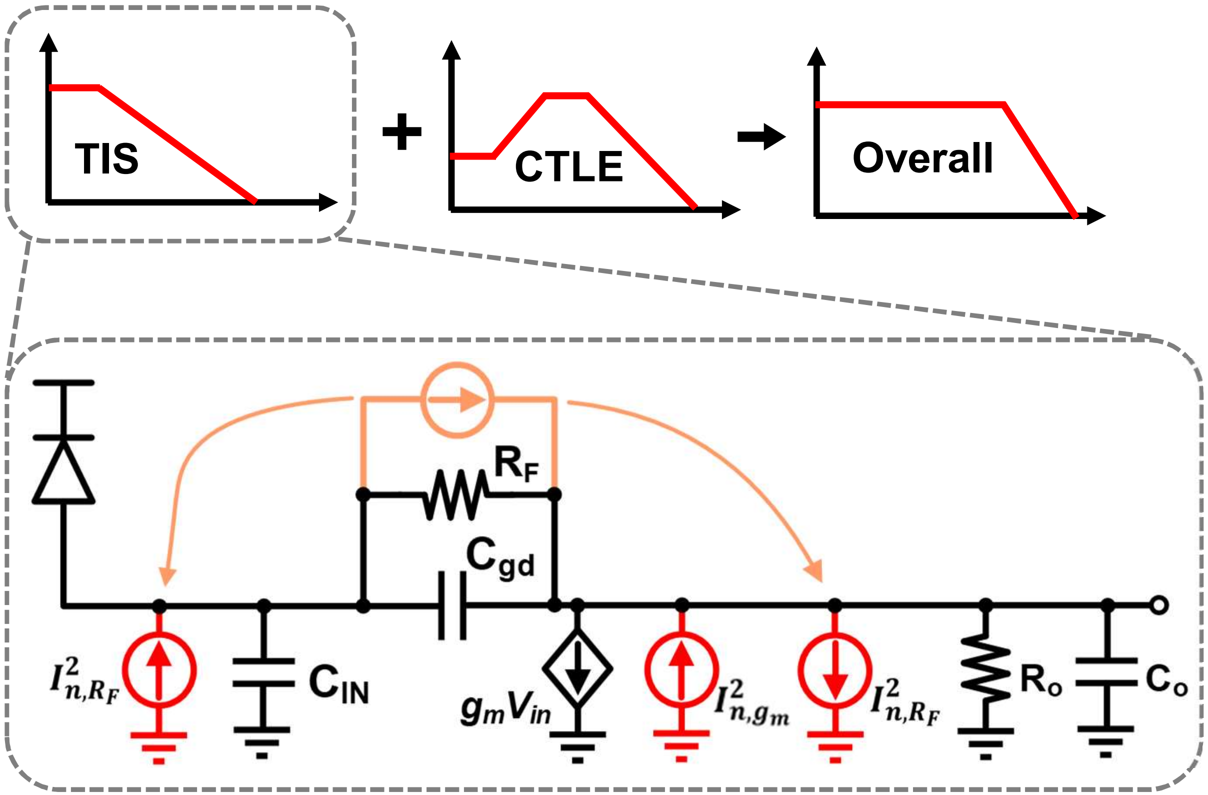
$$\overline{i^2_{n,TIS|CTLE}}(f) =$$

$$\underbrace{\frac{4kT}{R_F n} + \frac{4kT\gamma}{g_m R_F^2 n^2} + 4kT\gamma \times \frac{(2\pi C_T)^2}{g_m} f^2}_{\overline{i^2_{n,TIS}}(f)}$$

$$+ \underbrace{\frac{4kT\gamma}{g_{m,eq} R_F^2 n^2} + \frac{4kT\gamma}{g_{m,eq} R_F^2}\left(\frac{f}{BW_{TIS}}\right)^4}_{\overline{i^2_{n,CTLE}}(f)}$$

- Low-BW TIS + CTLE is used to beak the BW-noise trade-off
- Increasing n reduces white noise terms, while $f^2$and f^4 color noise terms remain unchanged
- Large scaling factor n resulting in reduced BW_{TIS}, necessitating higher peaking from CTLE

Architectural Consideration



- I^2_{n,R_F} is split at TIS input and output

- TIS transfer function

$$\boldsymbol{Z_{TIS}(s)} = \frac{-R_o(g_m \boldsymbol{n} R_F - 1 - sC_{gd}\boldsymbol{n}R_F)}{1 + g_m nR_F + sK_1 + s^2K_2}$$

- TIS output impedance

$$\boldsymbol{Z_o(s)} = \frac{R_o[1 + s\boldsymbol{n}R_F(C_{gd} + C_{IN})]}{1 + g_m\boldsymbol{n}R_F + sK_1 + s^2K_2}$$

$$K_1 = C_{IN}(R_o + nR_F) + C_oR_o + C_{gd}nR_F(1 + g_mR_o)$$

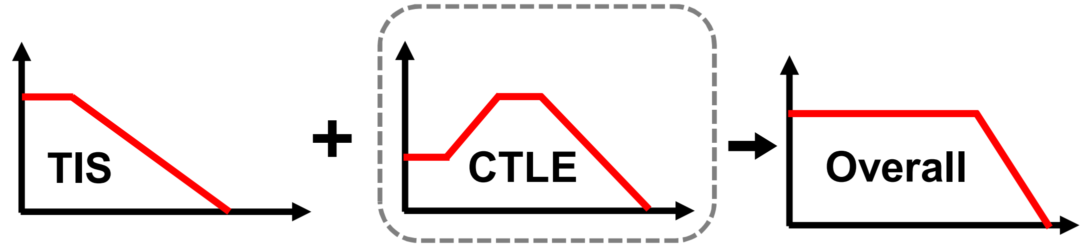
$$K_2 = nR_FR_o(C_{IN}C_o + C_{IN}C_{gd} + C_{gd}C_o)$$

- Noise PSD at TIS output

$$\boldsymbol{S_{TIS,out}(s)} = I^2_{n,R_F}|Z_{TIS} - Z_o|^2 + I^2_{n,g_m}|Z_o|^2$$

PSD: power spectral density

Architectural Consideration



- Transfer function of an ideal unity-gain CTLE stage that recovers the full BW

$$\boldsymbol{H_{CTLE}(s)} = \frac{1 + g_m R_F + sK_1 + s^2 K_2}{(1 + g_m R_a)\left(1 + \frac{s}{\boldsymbol{n}Q2\pi f_{TIS}} + \frac{s^2}{(\boldsymbol{n}2\pi f_{TIS})^2}\right)}$$

- Zeros of CTLE cancel the poles of TIS

$$\boldsymbol{Z_{TIS}(s)} \times \boldsymbol{H_{CTLE}(s)} = \frac{-R_o\left(g_m \boldsymbol{n} R_F - 1 - sC_{gd}\boldsymbol{n}R_F\right)}{(1 + g_m R_a)\left(1 + \frac{s}{\boldsymbol{n}Q2\pi f_{TIS}} + \frac{s^2}{(\boldsymbol{n}2\pi f_{TIS})^2}\right)}$$

- Noise PSD at CTLE output

$$\boldsymbol{S_{CTLE,out}(s)} = I_{n,R_F}^2 |(Z_{TIS} - Z_o) \times \boldsymbol{H_{CTLE}}|^2 + I_{n,g_m}^2 |Z_o \times \boldsymbol{H_{CTLE}}|^2$$

- Thermal noise of feedback resistor R_F

$$I_{n,R_F}^2 = 4kT/\boldsymbol{n}R_F$$

- Channel thermal noise

$$I_{n,g_m}^2 = 4kT\gamma g_m$$

- RMS noise at CTLE output

$$\boldsymbol{V_{noise,out}} = \sqrt{\int_0^{\infty} S_{CTLE,out}(s)\,df}$$

Architectural Consideration

- SNR at CTLE-equalized TIA output

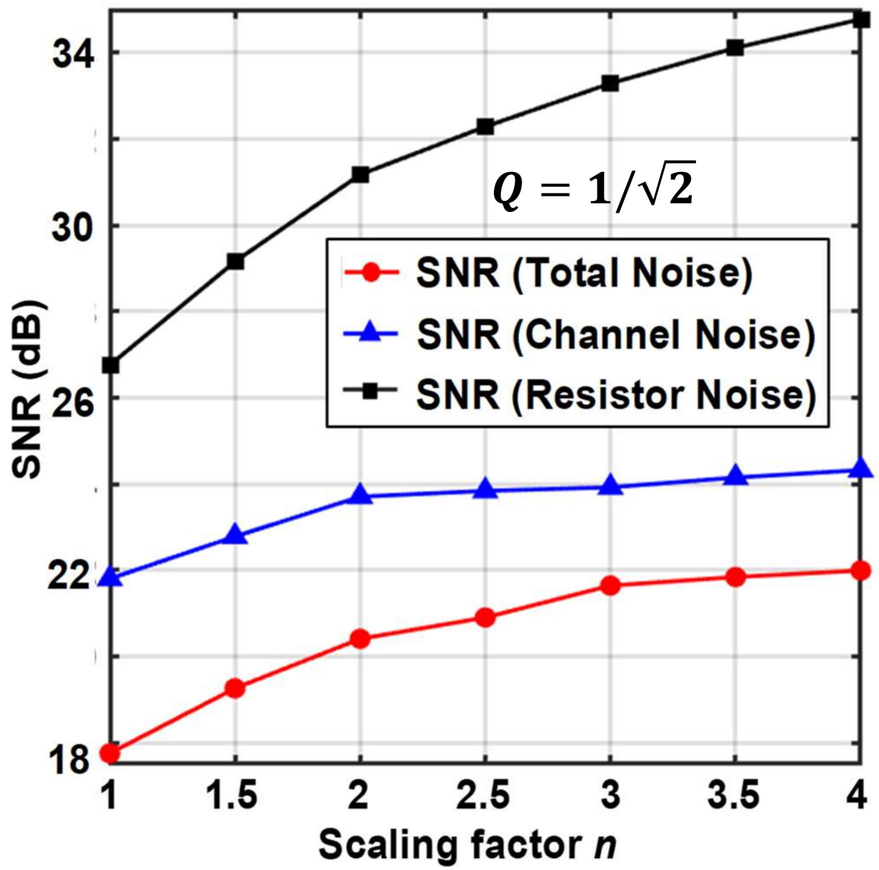
$$\boldsymbol{SNR} = 20log_{10}\left(\frac{V_{ISI}}{V_{n,out}}\right)$$

- Worst eye opening $\boldsymbol{V_{ISI}}$ is calculated from the main cursor V_0 and the i_{th} cursors V_i

$$\boldsymbol{V_{ISI}} = |V_0| - 3\sum_{i\neq 0}|V_i|$$

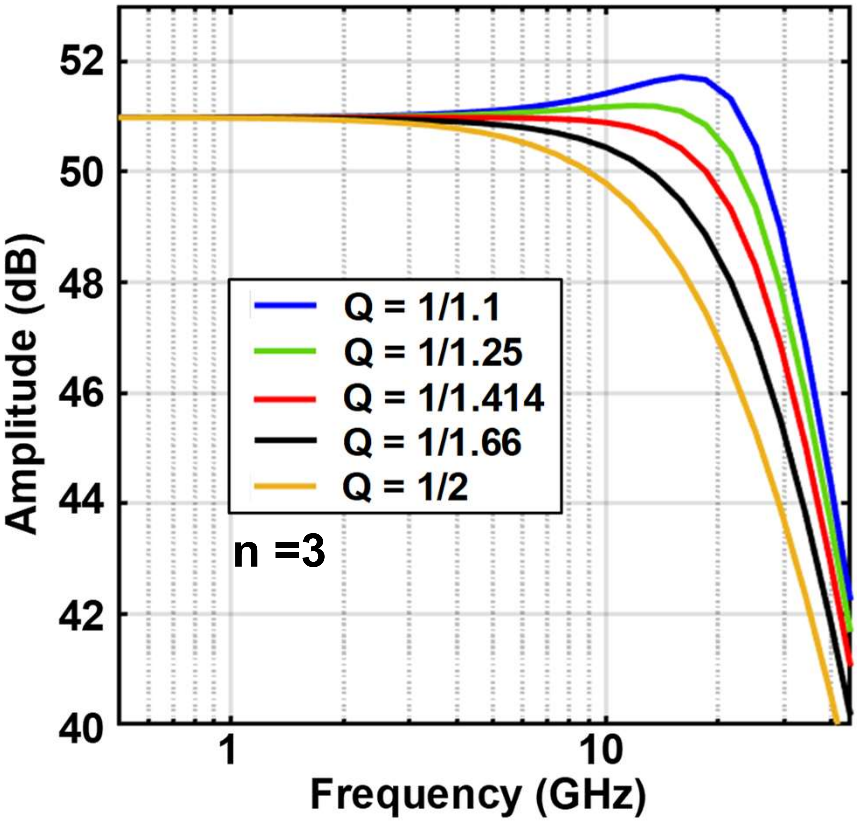
- SNR improves as $\boldsymbol{n}$ increases
- $\boldsymbol{n > 3}$, color noise component dominated
- White noise is suppressed, while the color noise is not affected

SNR as a function of $\boldsymbol{R_F}$ scaling factor $\boldsymbol{n}$

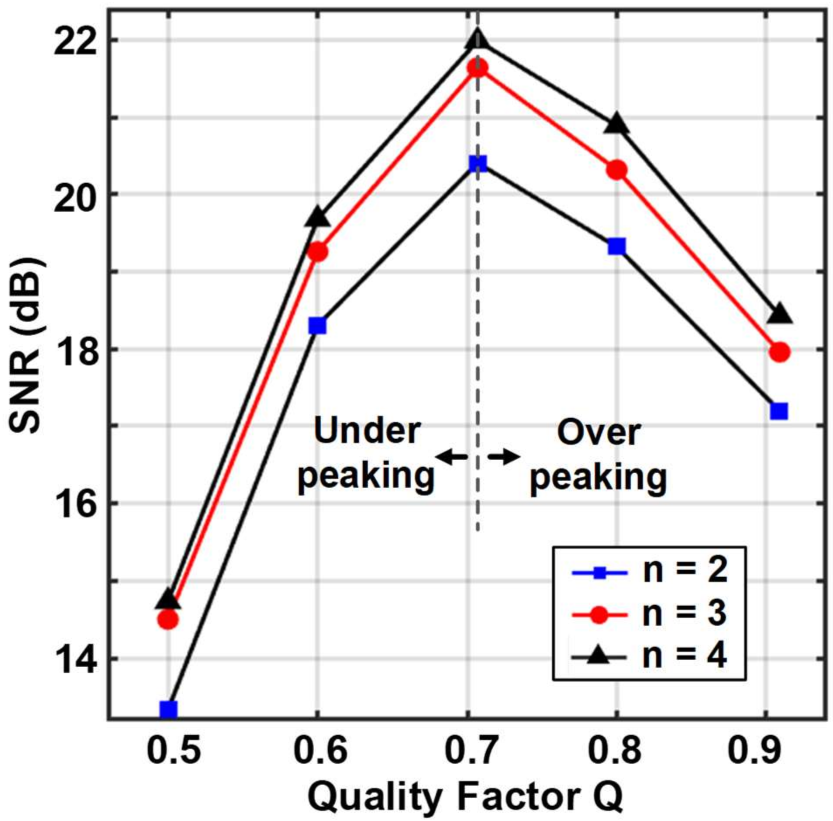


Architectural Consideration

CTLE-equalized TIA response

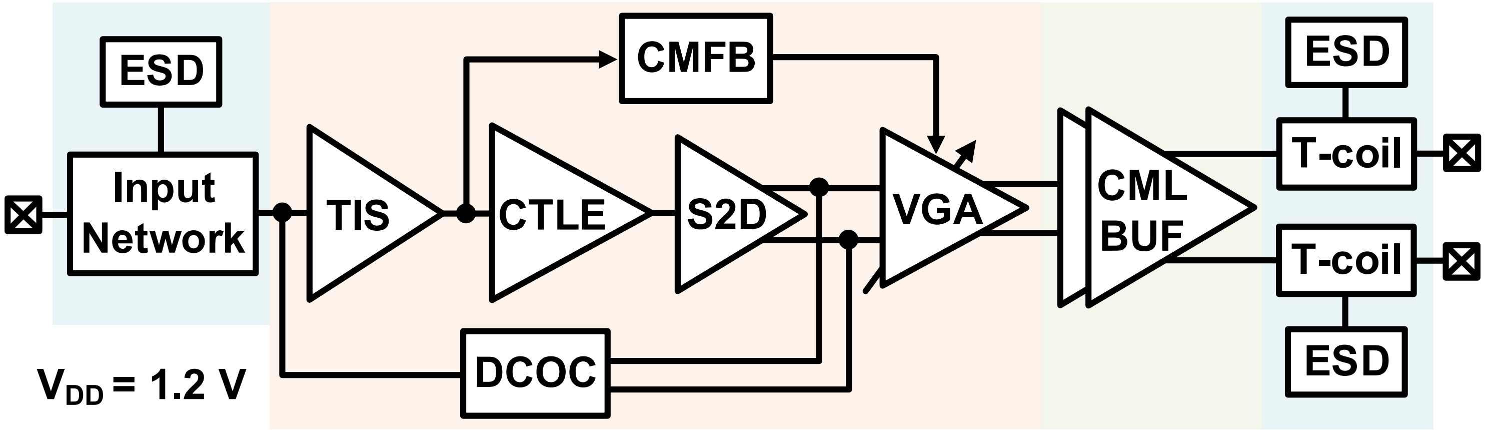


SNR as a function of quality factor Q



- CTLE over/under-peaking affects TIA noise
- Q variation < 15%, degradation < 2.5 dB

Proposed Architecture



- $n = \sim 3.5$ to obtain a large TIS gain and eliminate the post-amplifier
- Gain and middle/high-frequency peaking of the CTLE are tunable
- S2D conversion is put after the single-ended CTLE instead of the TIS
- T-coils are integrated to optimize return loss and relieve BW degradation from ESD

CMFB: common-mode feedback; S2D: single-to-differential

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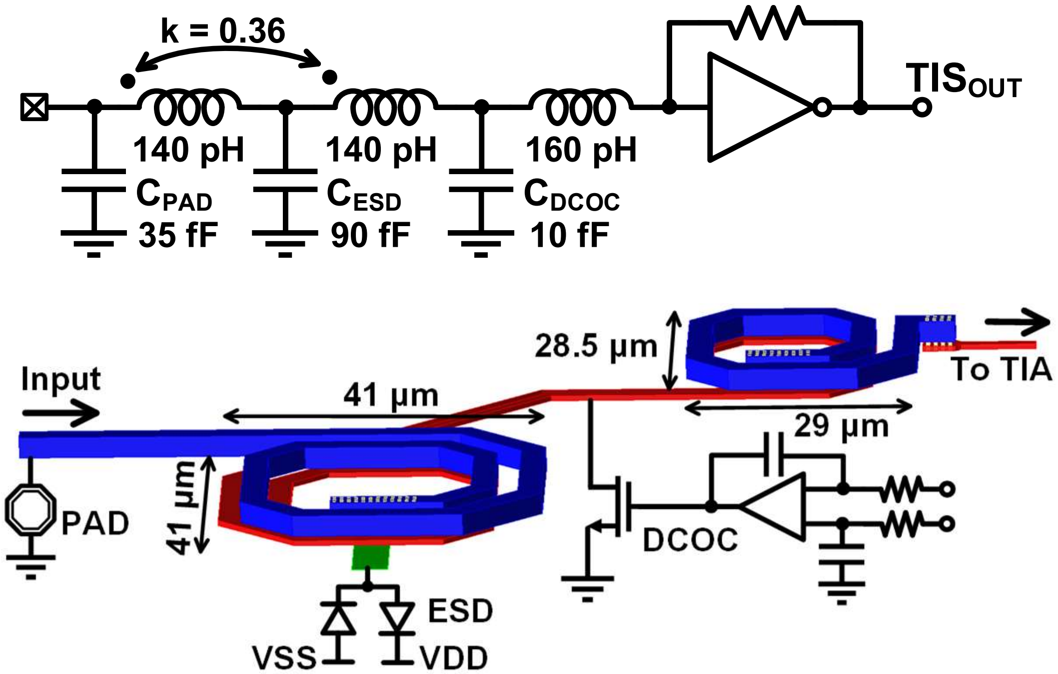
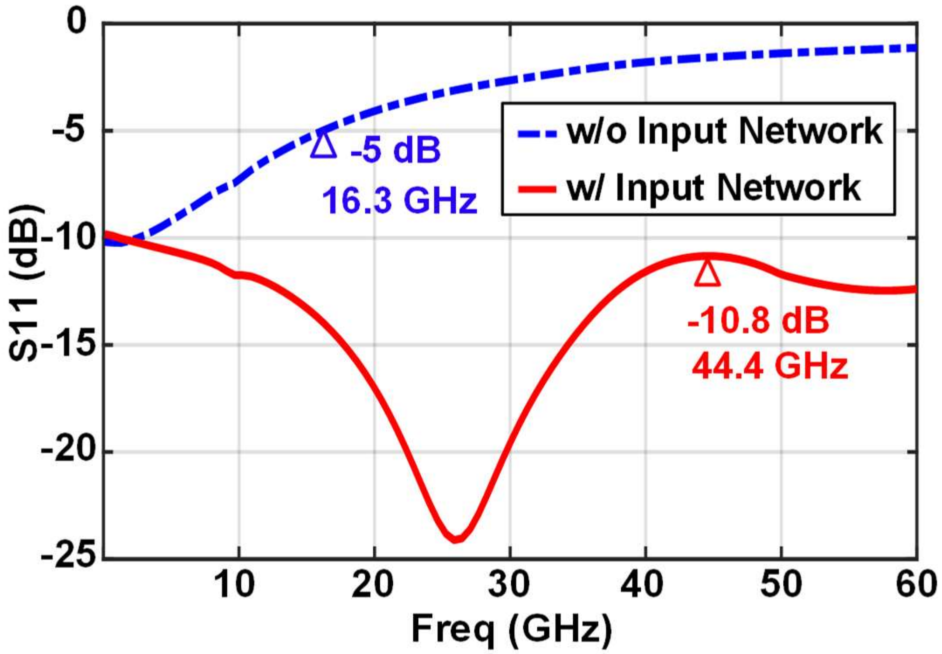
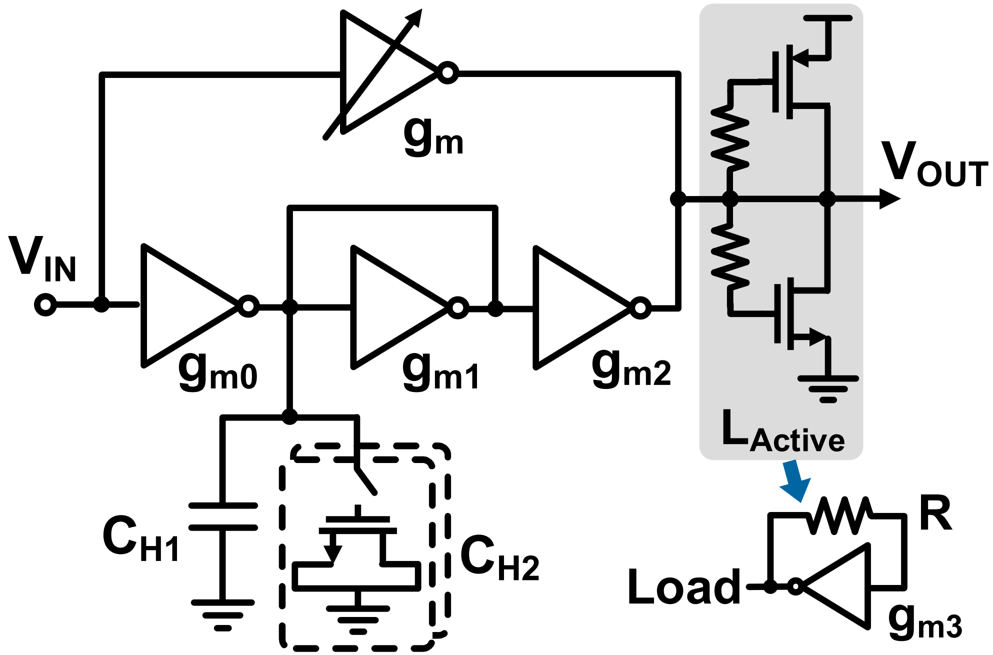
TIS with Multi-Peaking Input Network





- Multi-peaking input network to distribute parasitic capacitance
- Multi-layer stacked T-coil and inductor are custom designed
- Good broadband impedance matching under heavy capacitive loading achieved

Single-Ended Inverter-Based CTLE



- Gm-C filter create one pole at

  $g_{m1}/(C_{H1}+C_{H2})$

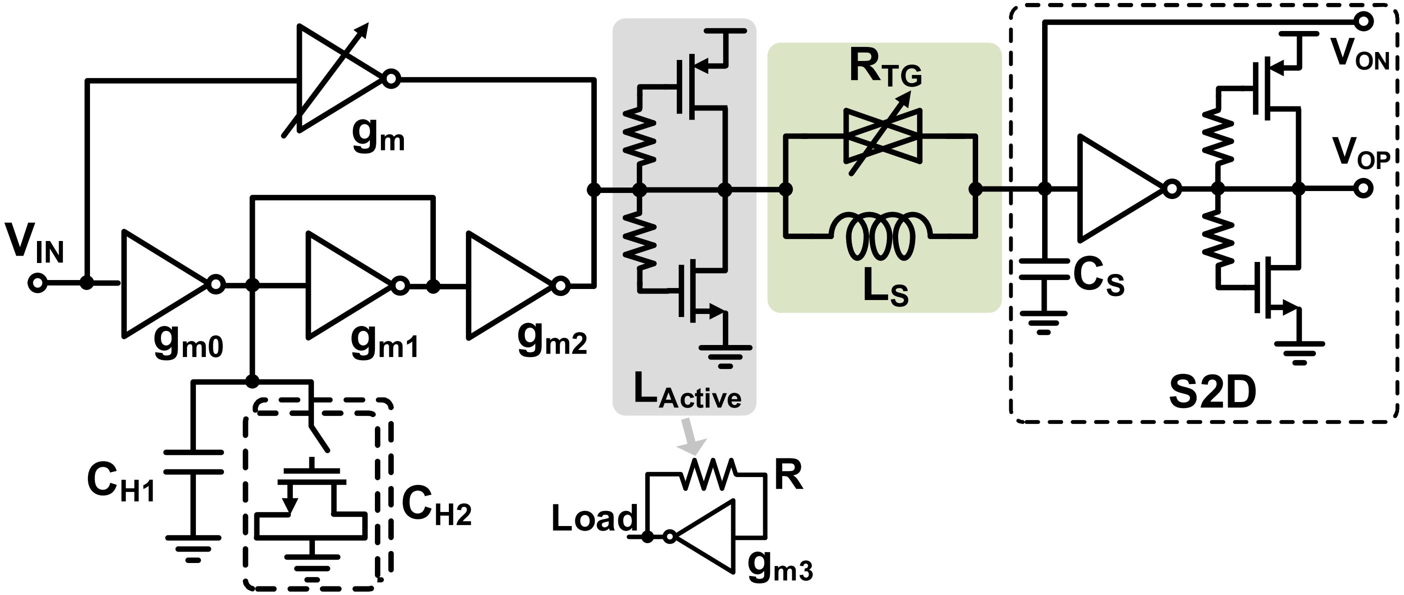
- CTLE response

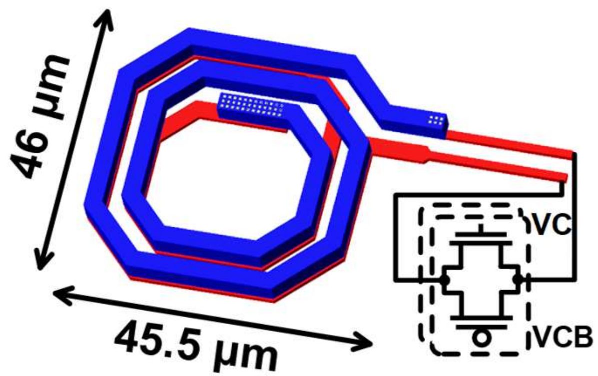
  $H(s) = [H_M(s) - H_L(s)] \cdot L_{Active}$

  $$= \left[g_m - \frac{g_{m0}g_{m2}}{g_{m1}} \cdot \frac{1}{1+s\,(C_{H1}+C_{H2})/g_{m1}}\right] \cdot \frac{sRC_{gs}}{2g_{m3}}$$

- High f_T of PMOS in deep sub-micron CMOS technologies
- CTLE engages two parallel paths: main and low-pass paths
- Peaking is created by subtracting the low-pass path from the main path
- 3-bit dc gain control and 2-bit middle-frequency (MF) tuning implemented

CTLE with Q-Shaping Inductor



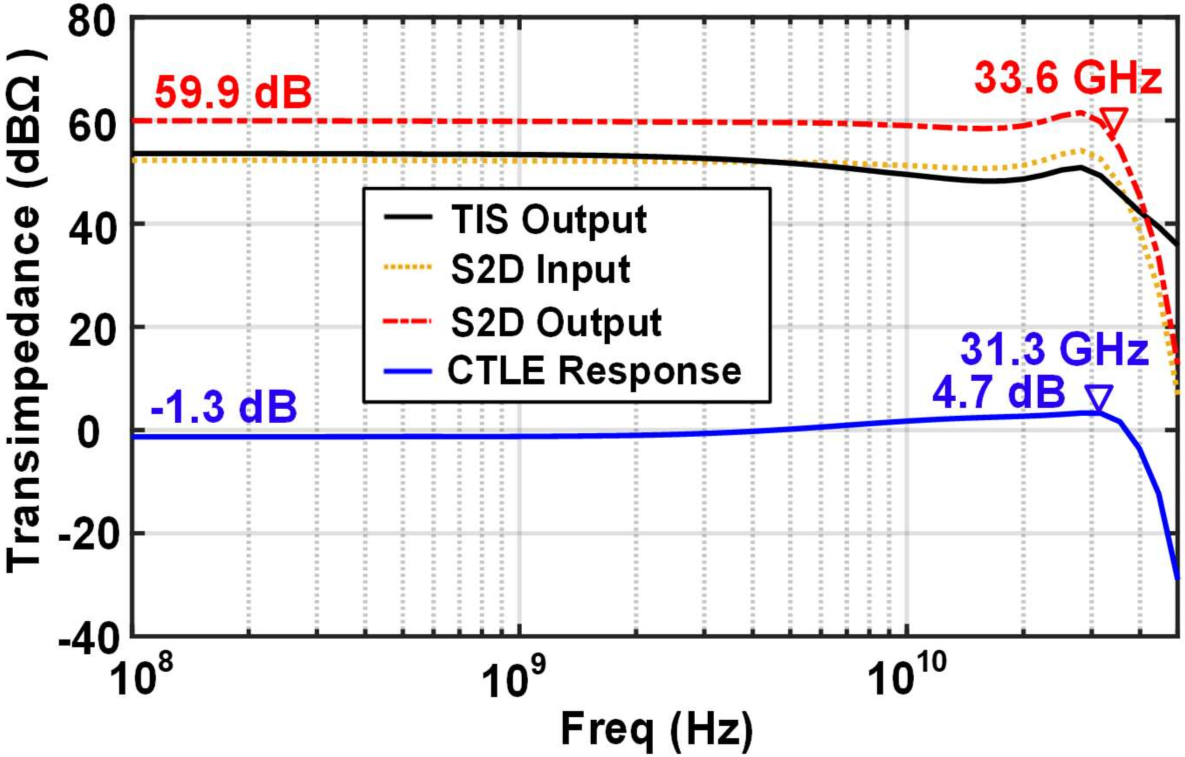


$$\frac{1}{Q_{tank}} = \frac{1}{Q_{ind}} + \frac{\omega_{PK} L_S}{R_{TG}} + \frac{1}{Q_C} = \frac{BW_{3d}}{\omega_{PK}}$$

- Accommodate BW variation of TIA caused by bond wires and input capacitance
- Tunable Q: programmable transmission gate $\mathbf{R_{TG}}$ in parallel with a 670-pH inductor $\mathbf{L_S}$
- S2D circuit is implemented by a unity gain buffer with active inductor load

Simulated Frequency Response

Post-layout simulation result



At TIS output:

- 53.6 dBΩ with BW_{3dB} of 7.1-GHz
- BW_{6dB} of 15.1 GHz, 23.8 GHz and 33.7 GHz

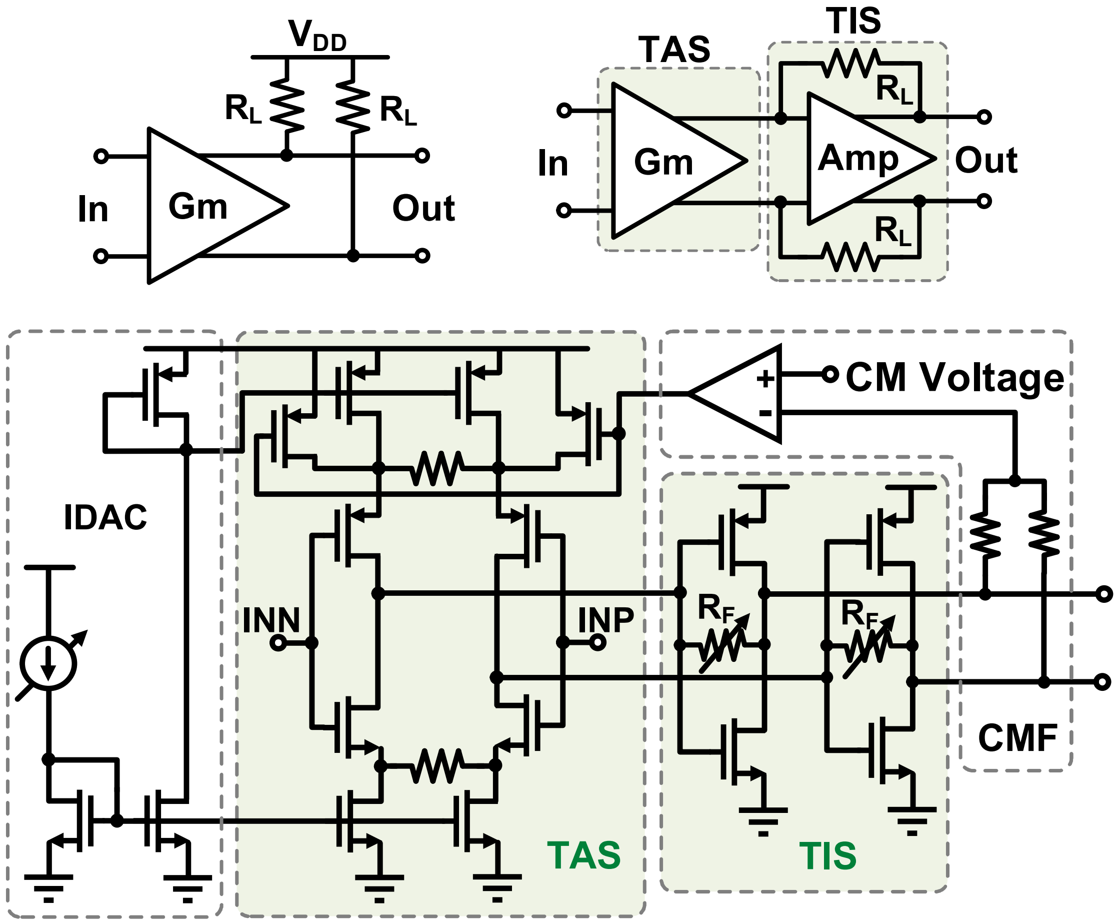
CTLE response:

- 6-dB peaking at 31.3 GHz

At S2D output:

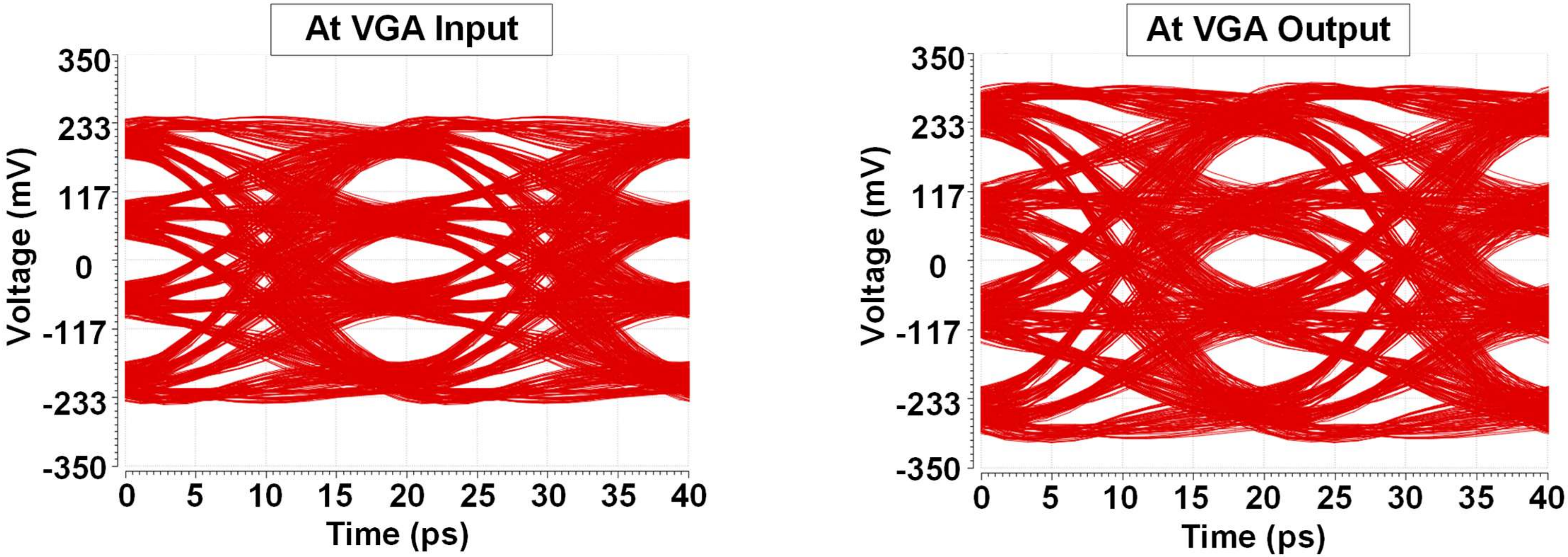
- 59.9 dBΩ with BW_{3dB} of 33.6 GHz

VGA Design



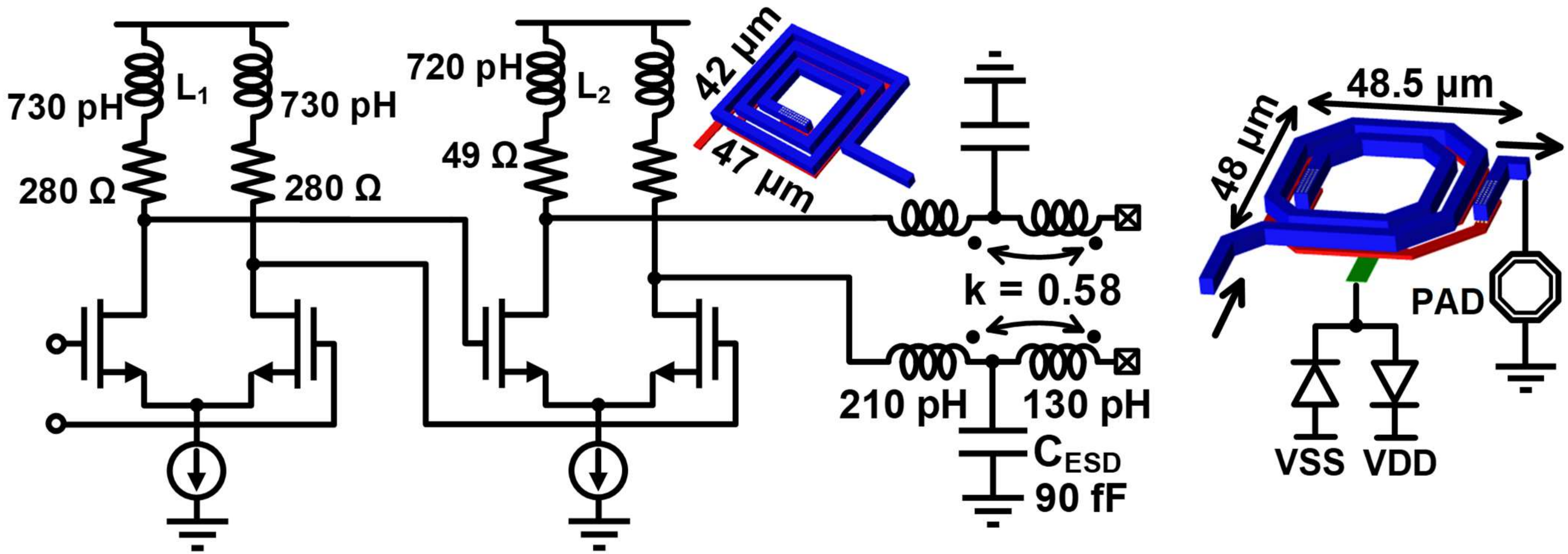
- NMOS- or PMOS-only input pairs exhibit compromised linearity
- CMOS input pairs of both TAS and TIS improve linearity
- Combine the tunability of both Gm and R_F 3-bit Gm control and 2-bit R_F control
- Tail current sources to improve immunity to supply variations and CM rejection
- Source degeneration resistor to further enhance linearity
- Gain: -2.4 dB to 7.3 dB

Simulated Eye Diagrams



- TIA input amplitude of 600 μA_{pp}
- Simulated 100-Gb/s PAM-4 eye diagrams at VGA input and output
- VGA output: ratio level mismatch (RLM) > 96%

Output BUF Design



- Two cascaded differential pairs with shunt-inductive peaking to drive 50-Ω off-chip load
- Multi-layer stacked T-coils to accommodate ESD capacitance
- Buffer with T-coil and ESD diodes provides 0-dB gain with 42-GHz BW

Outline

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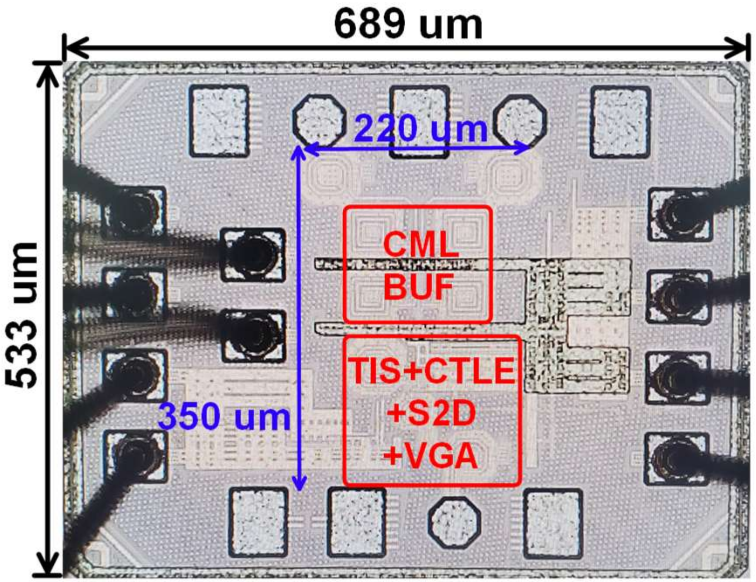
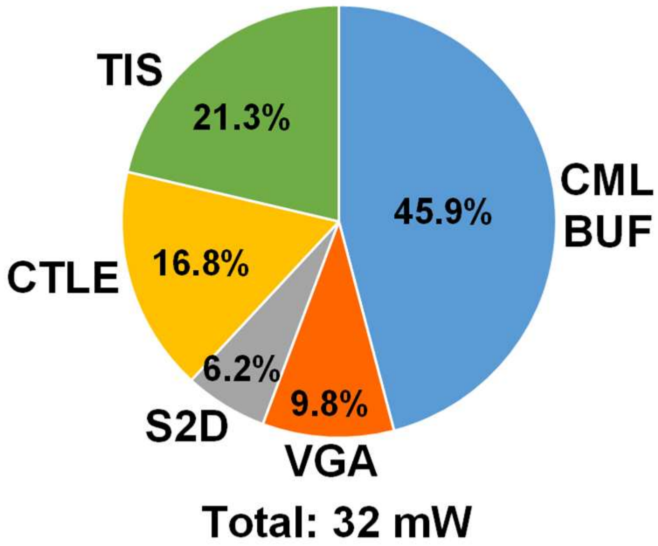
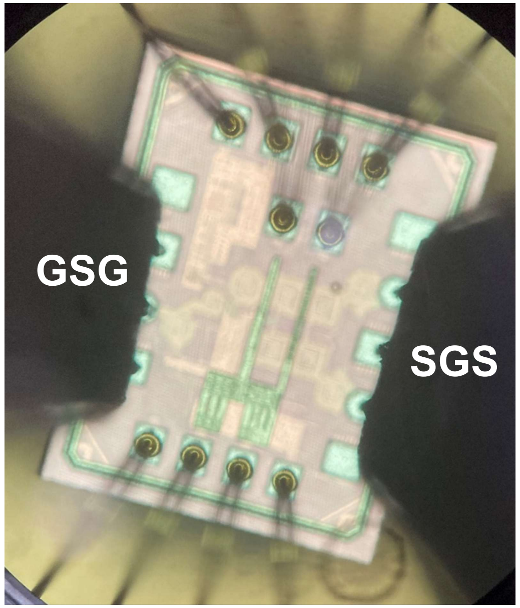
Die Photo and Power Breakdown

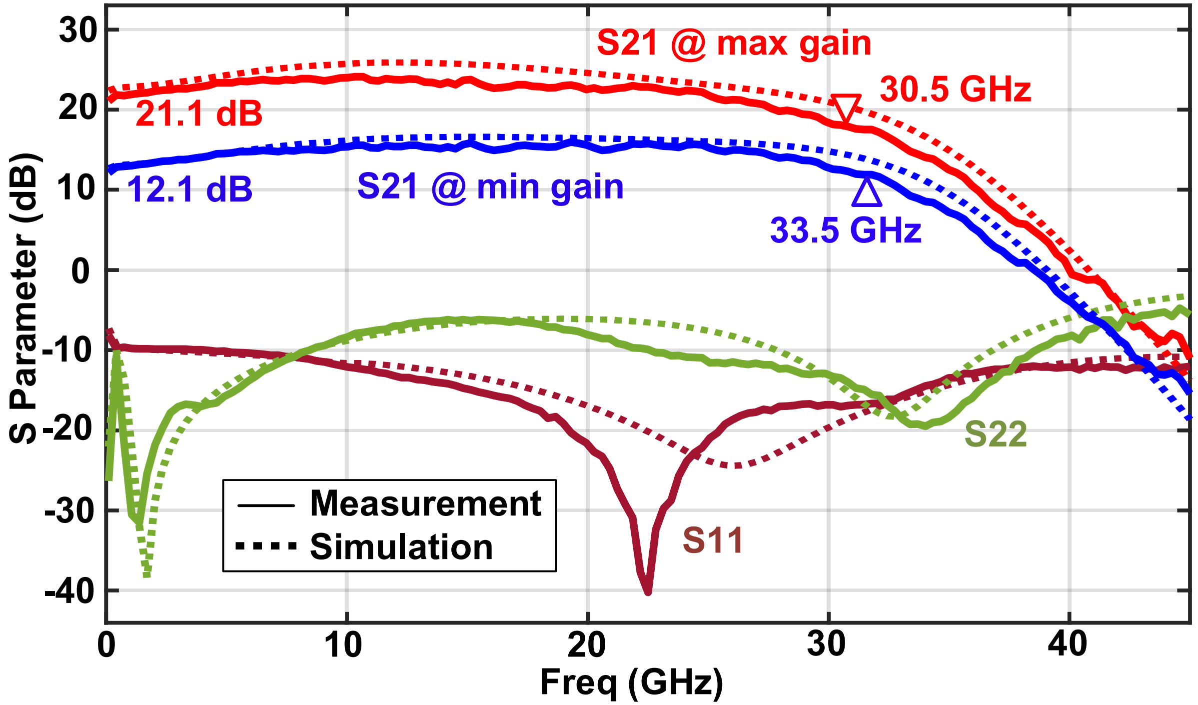




- Fabricated in a 28-nm bulk CMOS technology
- 0.69 × 0.53 mm^2 area defined by the pad frame
- 32 mW power consumption including output buffer from a 1.2-V supply

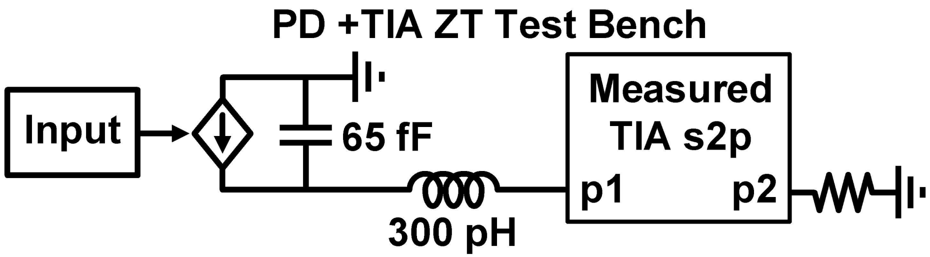
Small Signal Measurement: S-Parameter



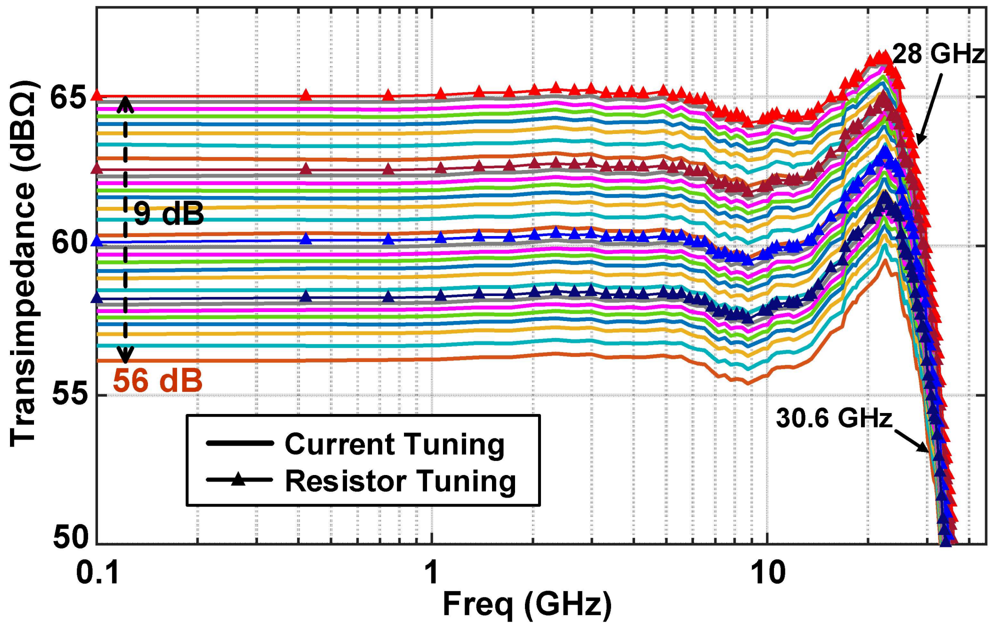


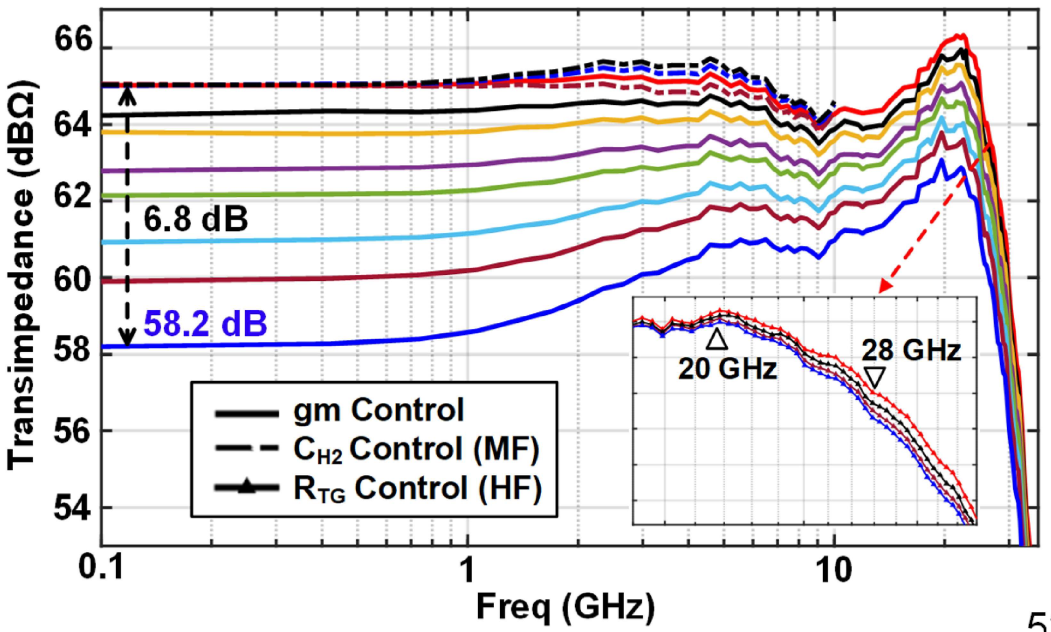
- Four-port S-parameter measurement up to 50 GHz
- S21: maximum gain of 21.1 dB with a BW of 30.5 GHz
- S11 and S22 lower than -6 dB up to 40 GHz

Small Signal Measurement: Transimpedance

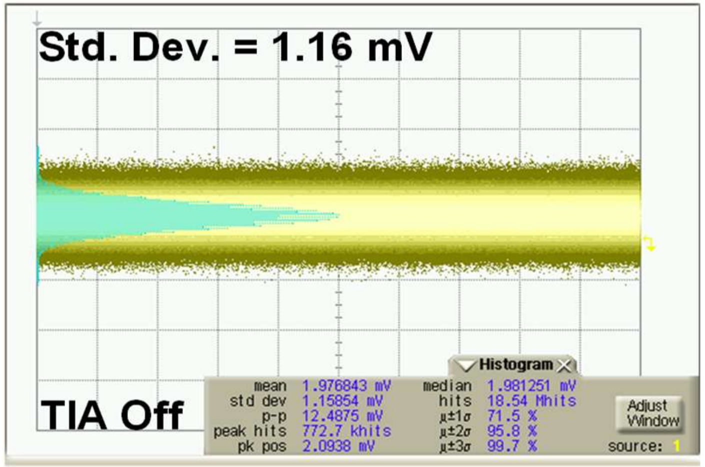


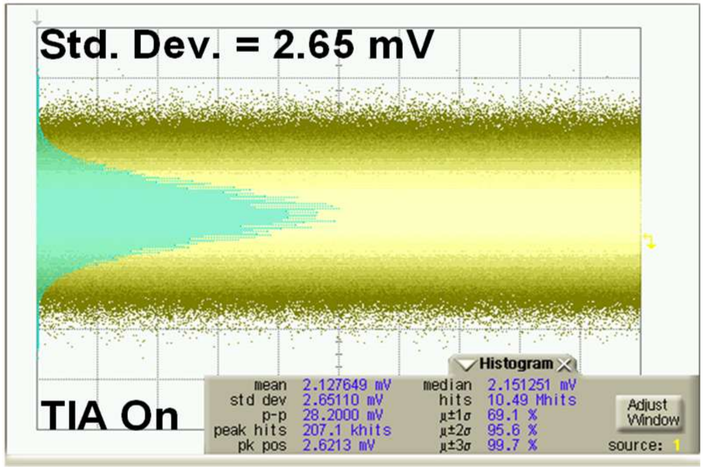
- ZT: max. gain of 65 dBΩ with a 28 GHz BW
- 9-dB gain control range with an average step of 0.3 dB, overall BW variation < 3 GHz
- CTLE: dc gain control range of 6.8 dB





Noise Measurement





Single-ended output noise distribution

- 80-GHz sampling oscilloscope
- Noise from oscilloscope de-embedded

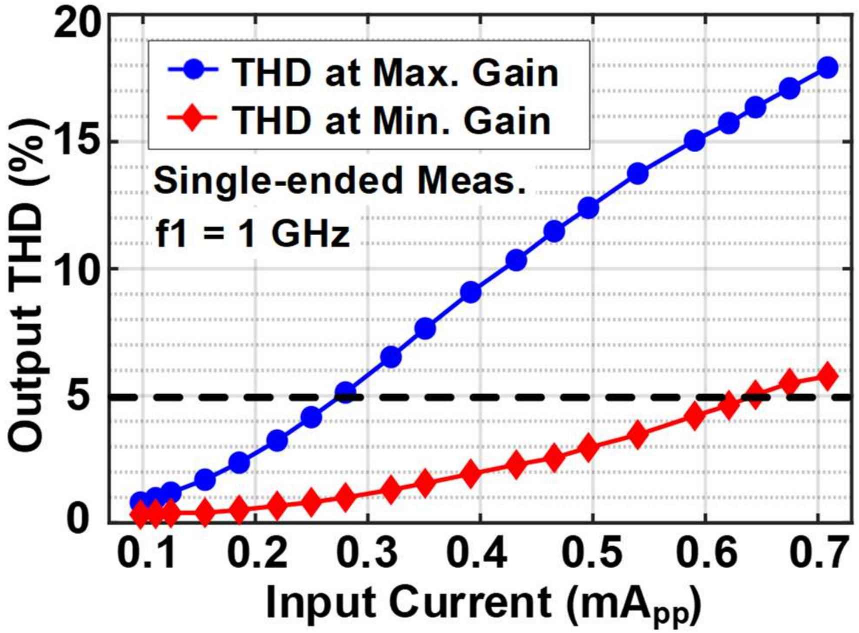
Input-referred current noise

$$i_{n,in}(rms) = \frac{2\times\sqrt{(2.65mV)^2-(1.16mV)^2}}{10^{\left(\frac{65}{20}\right)}} = 2.68\ \mu A_{rms}$$

Average input-referred current noise density

$$2.68\ \mu A_{rms}/\sqrt{28\ GHz} = 16\ pA/\sqrt{Hz}$$

THD Measurement



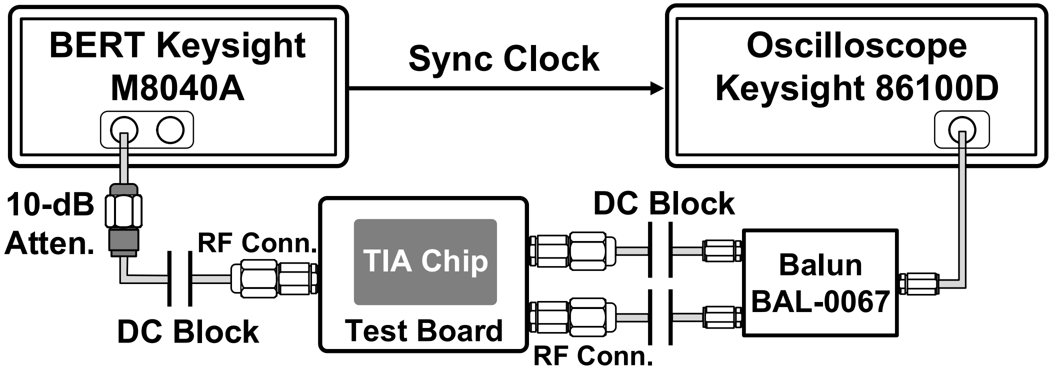
Single-ended total harmonic distortion (THD)

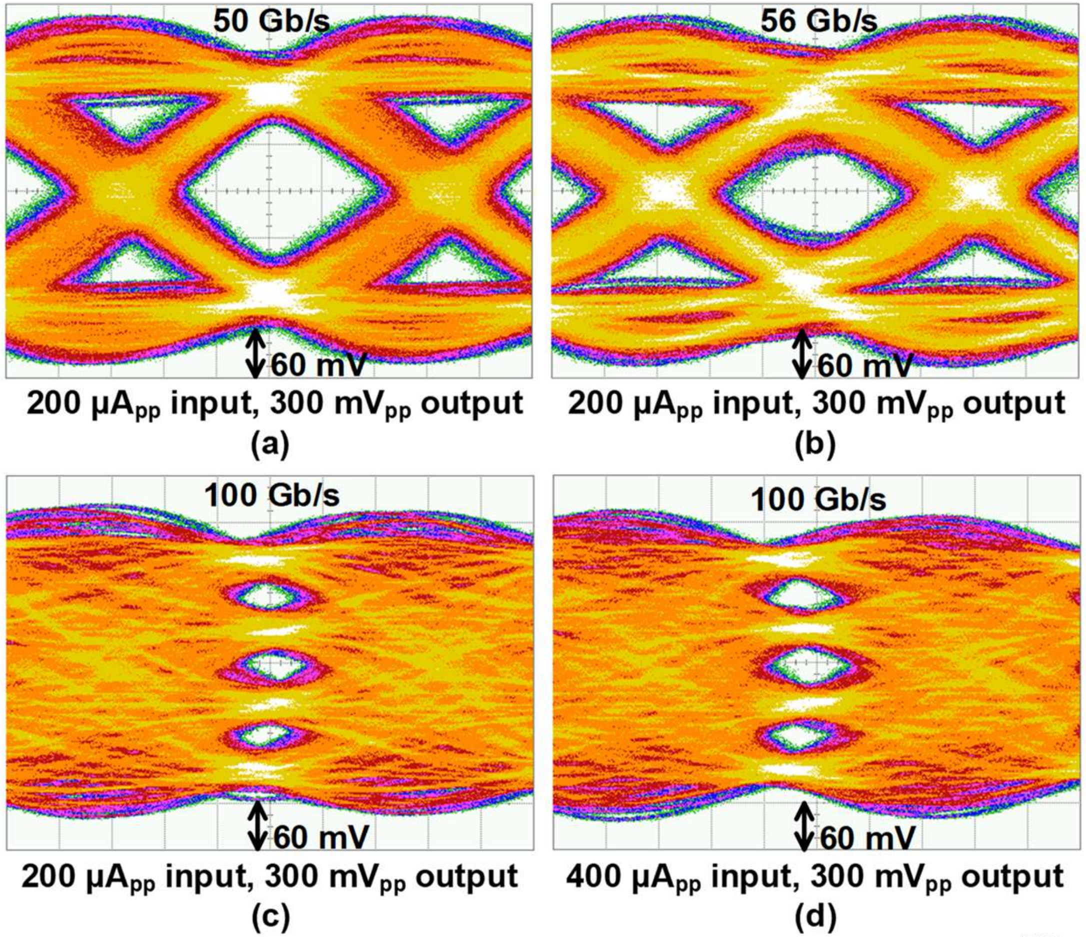
- 67-GHz spectrum analyzer
- 1-GHz fundamental frequency
- 10 harmonics counted

Within a THD of 5%

- At max. gain: 280 μA_{pp} input, ~500 mV_{pp} output
- At min. gain: 640 μA_{pp} input, ~400 mV_{pp} output

Time Domain Measurement

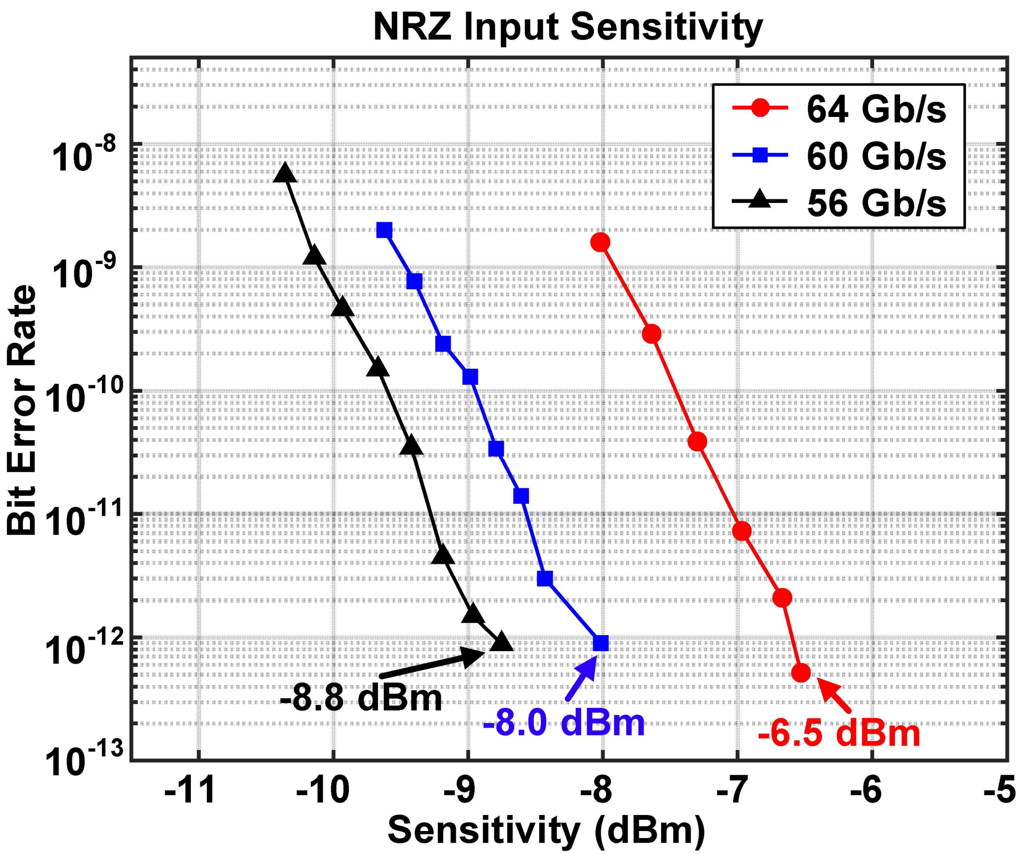




Time domain measurement setup

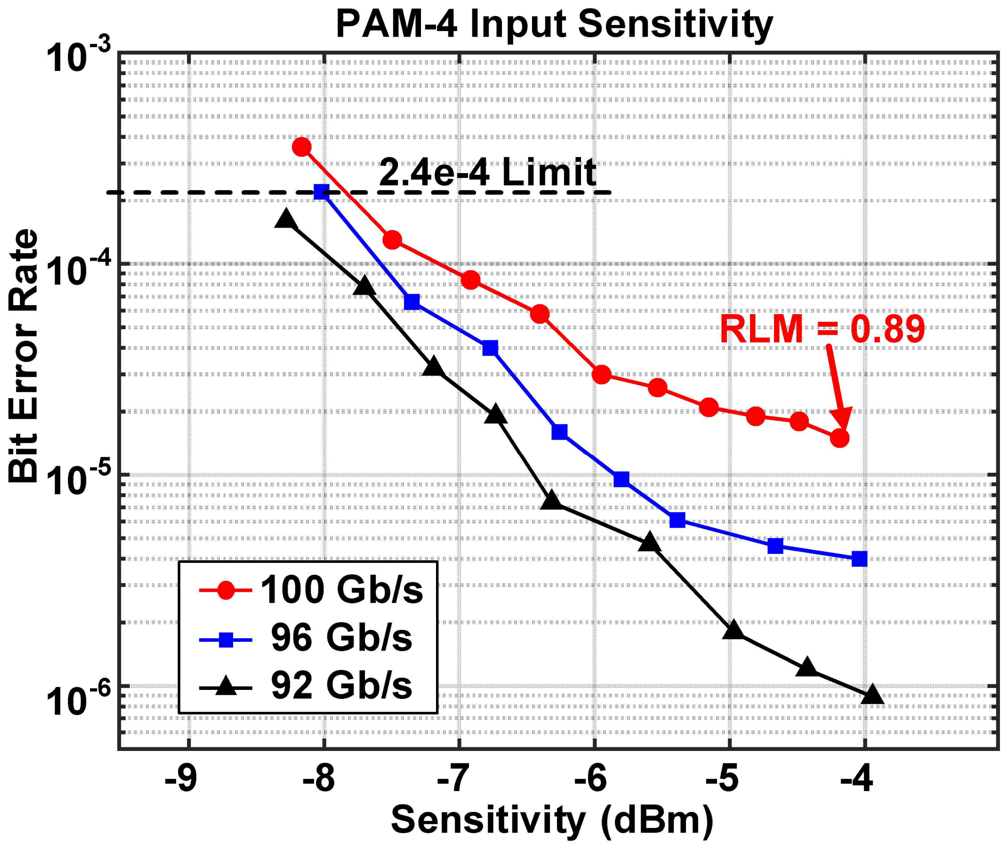
- 64-Gbaud bit error rate tester (BERT)
- 10-dB attenuator at data input
- TIA differential output combined by a balun
- More than 10k UI of PRBS-9 pattern

BER Measurement: NRZ



- **BER at different amplitudes of electrical input signals is measured**
  - Assume a PD responsivity of 0.75 A/W
  - Estimated BER versus input OMA sensitivity
- **Under 1e-12 BER**
  - -6.5-dBm sensitivity at 64 Gb/s
  - -8.8-dBm sensitivity at 56 Gb/s

BER Measurement: PAM-4



- **BER at different amplitudes of electrical input signals is measured**
  - Assume a PD responsivity of 0.75 A/W
  - Estimated BER versus input OMA sensitivity
- **Under 2.4e-4 pre-FEC limit**
  - -7.8-dBm sensitivity at 100 Gb/s
  - With -4-dBm input at 100 Gb/s, 1.5e-5 BER achieved with a RLM of 0.89

Comparison Table

Reference	ESSCIRC'18 [6]	JSSC'22 [7]	JSSC'22 [3]	JSSC'23 [8]	VLSI'23 [9]	SSCL'23 [10]	SSCL'24 [11]	This Work
Technology	28nm CMOS	22nm FinFET	28nm CMOS	16nm FinFET	12nm FinFET	22nm FD-SOI	28nm CMOS	**28nm CMOS**
Data Rate (Gb/s)	112*	128*	100	112	90	106.25	85*	**100***
Gain (dBΩ)	65	59.3	68.6	63	65	74	65	**65**
BW (GHz)	60	45.5	20.8	32	25	28	24	**28**
THD@ Input Current, Output Amplitude)	<5%@ 1mA$_{pp}$, N/A	<5%@ 330μA$_{pp}$, 304mV$_{pp}$	NA	<8%@ 670μA$_{pp}$, 336mV$_{pp}$	<9%@ 600μA$_{pp}$, N/A	<4%@2.46 mA$_{pp}$, 550mV$_{pp}$	<1.77%@ 330μA$_{pp}$, 660mV$_{pp}$	**<5%@ 640μA$_{pp}$, 400mV$_{pp}$**
Noise ($pA/\sqrt{Hz}$)	19.3	12.6	17	16.9	13.4	11	10.4	**16**
Input/Output ESD	No	No	No	Yes (80f)	Yes	Yes	No	**Yes (90f)**
Power (mW)	107	11.2	117	77	29.2	155	56	**32**
Efficiency (pJ/bit)	0.96	0.09	1.17	0.69	0.32	1.46	0.66	**0.32**
FoM**	997	3748	478	739	1522	905	762	**1556**

*Electrical Measurement

$$**\text{FoM} = \frac{Gain(\Omega)\times BW_{3dB}(GHz)}{P_{dc}(mW)}$$

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Conclusion

- **PAM-4 ORX Data Path**
  - A 48-Gb/s PAM-4 ORX is proposed with a linear TIA and a PAM-4 sampler integrated
  - The TIA avoids CTLE and passive inductors, and the sampler incorporates a 2-tap FFE and a 2-tap DFE to mitigate ISI from TIA
  - Under 2.4e-4 BER, -5.1-dBm sensitivity is achieved with 1.28-pJ/bit (0.27-pJ/bit for TIA alone) efficiency
- **PAM-4 ORX Front End**
  - A 100-Gb/s PAM-4 linear TIA is proposed with high inductance density
  - A single-ended inverter-based CTLE is implemented, and a current reuse VGA based on a TAS-TIS topology provides a large gain-BW product and high linearity
  - 28-GHz BW with a 65-dBΩ gain is achieved, consuming only 32 mW

Publication

[1] **Chongyun Zhang**, Fuzhan Chen, Li Wang, Lin Wang, and C. Patrick Yue, "Recent advances of high-speed short-reach optical interconnects for data centers," *IEEE Open J. Solid-State Circuits Soc.*, vol. 5, pp. 86-100, 2025.

[2] **Chongyun Zhang**, Li Wang, Zilu Liu, Fuzhan Chen, Quan Pan, Xianbo Li, and C. Patrick Yue, "A 48-Gb/s half-rate PAM4 optical receiver with 0.27-pJ/bit TIA efficiency, 1.28-pJ/bit RX efficiency, and 0.06-mm^2 area in 28-nm CMOS," in *Proc. IEEE Symp. VLSI Technol. Circuits (VLSI Technol. Circuits)*, Jun. 2024, pp. 1–2.

[3] **Chongyun Zhang**, Fuzhan Chen, and C. P. Yue, "A 56-Gb/s PAM-4 transmitter using silicon photonic microring modulator in 40nm CMOS," in *Proc. IEEE Int. Midwest Symp. Circuits Syst. (MWSCAS)*, Aug. 2022, pp. 1-4.

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[4] Fuzhan Chen, **Chongyun Zhang**, Li Wang, Quan Pan, and C. Patrick Yue, "A 56-Gb/s PAM-4 VCSEL transmitter with piecewise compensation scheme in 40-nm CMOS," *IEEE J. Solid-State Circuits*, early access.

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  - Chairperson: Prof. Wenjing Ye
  - External: Prof. Chao Wang
  - ECE: Prof. Howard Cam Luong
    Prof. Man Hoi Wong
  - CSE: Prof. Song Guo
- All Optical Wireless Lab Members
  - Dr. Li Wang
  - Dr. Fuzhan Chen

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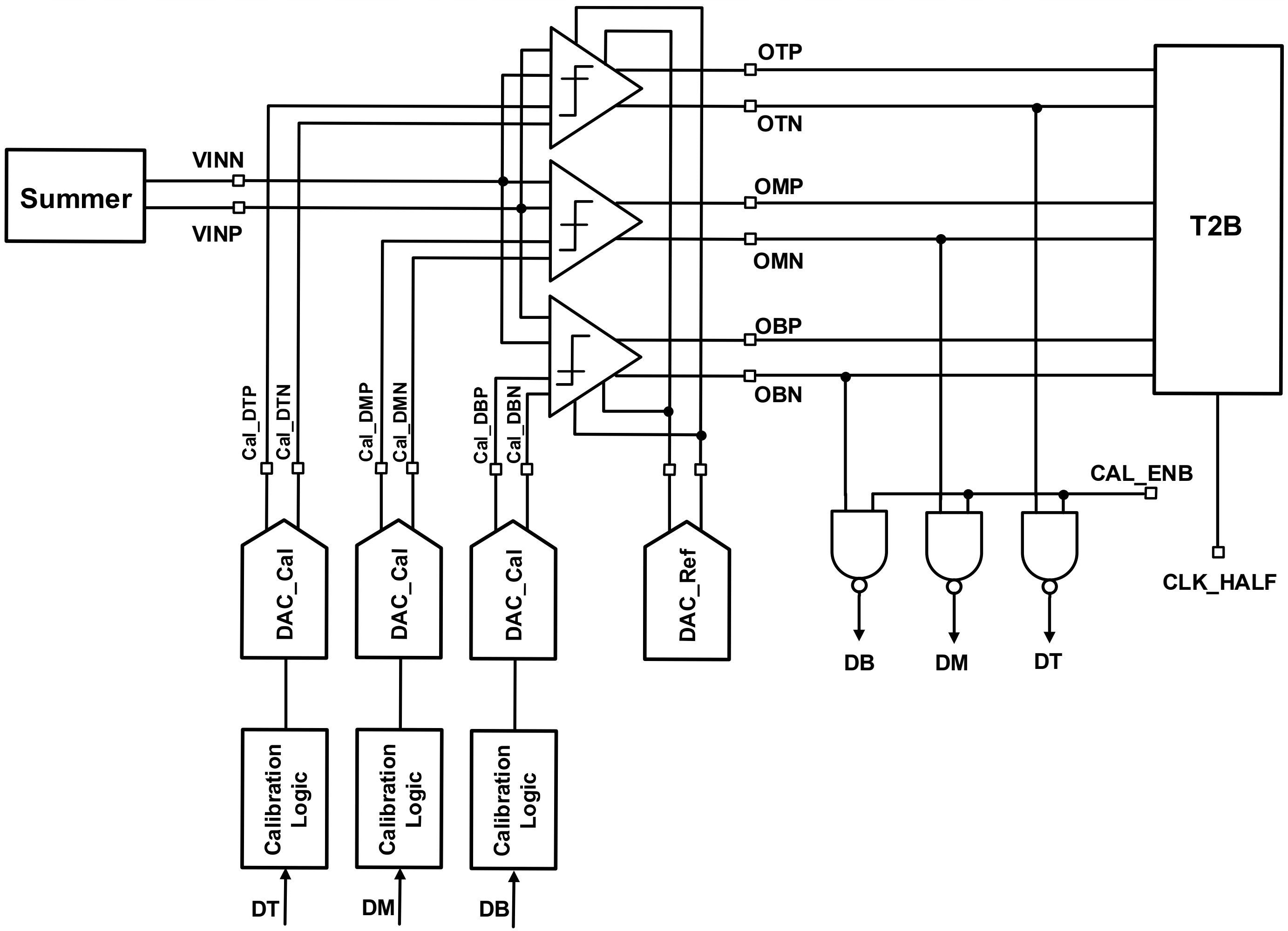
Thank you

Optical Wireless Lab
Department of Electronic and Computer Engineering
the Hong Kong University of Science and Technology (HKUST)

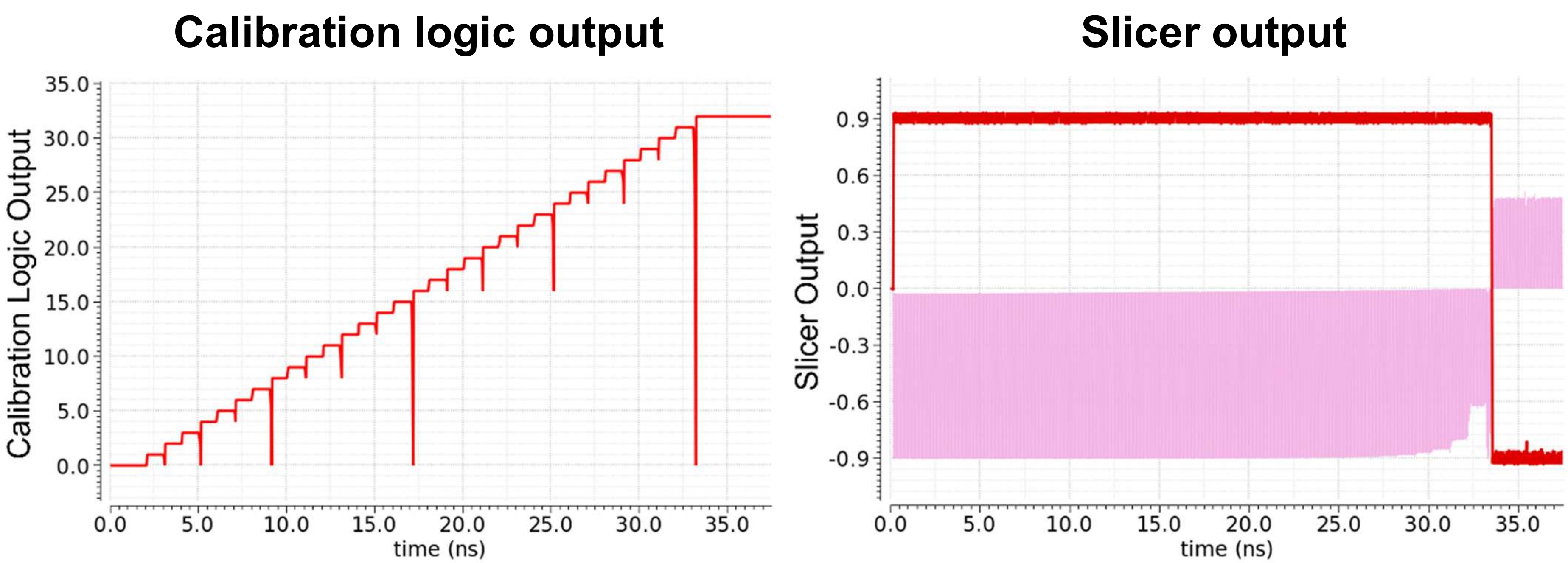
Back-up: Calibration Logic



Slicers with calibration circuits

- Calibration logic
- 6-bit calibration DACs, DAC_Cal

Back-up: Calibration Logic



(a) (b)

- If the comparator does not generate ‘0’ within 8 clock cycles, calibration logic output increases by 1 and DAC_cal increases by 1 MSB
- The process continues until a transition from ‘1’ to ‘0’ happens at slicer output and the calibration ends

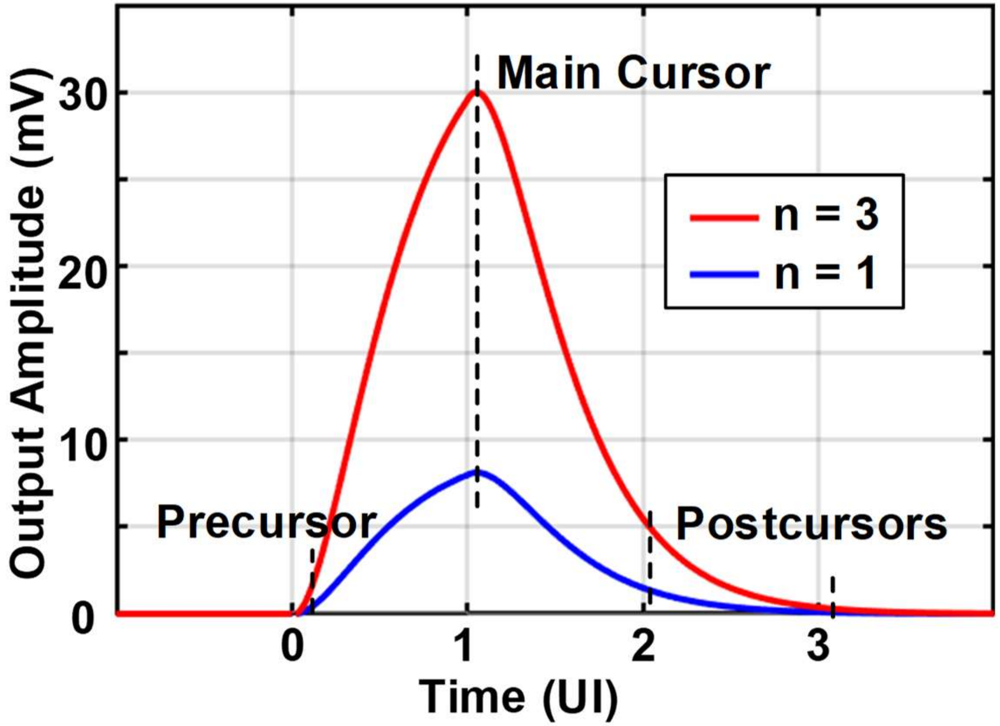
Back-up: V_{ISI} Calculation

- Worst eye opening $\boldsymbol{V_{ISI}}$ for PAM-4 is calculated from

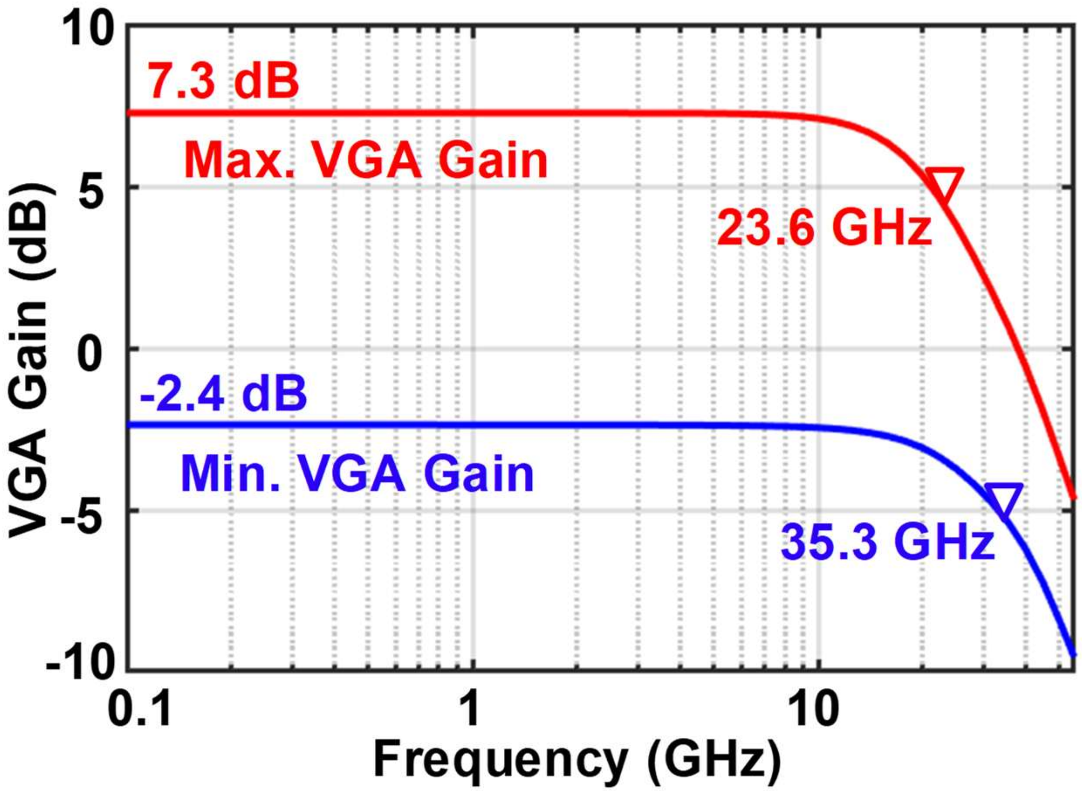
$$\boldsymbol{V_{ISI}} = |V_0| - 3\sum_{i\neq 0}|V_i|$$

- V_0 is the main cursor
- V_i is the i_{th} pre/post cursors

Pulse responses at TIS output

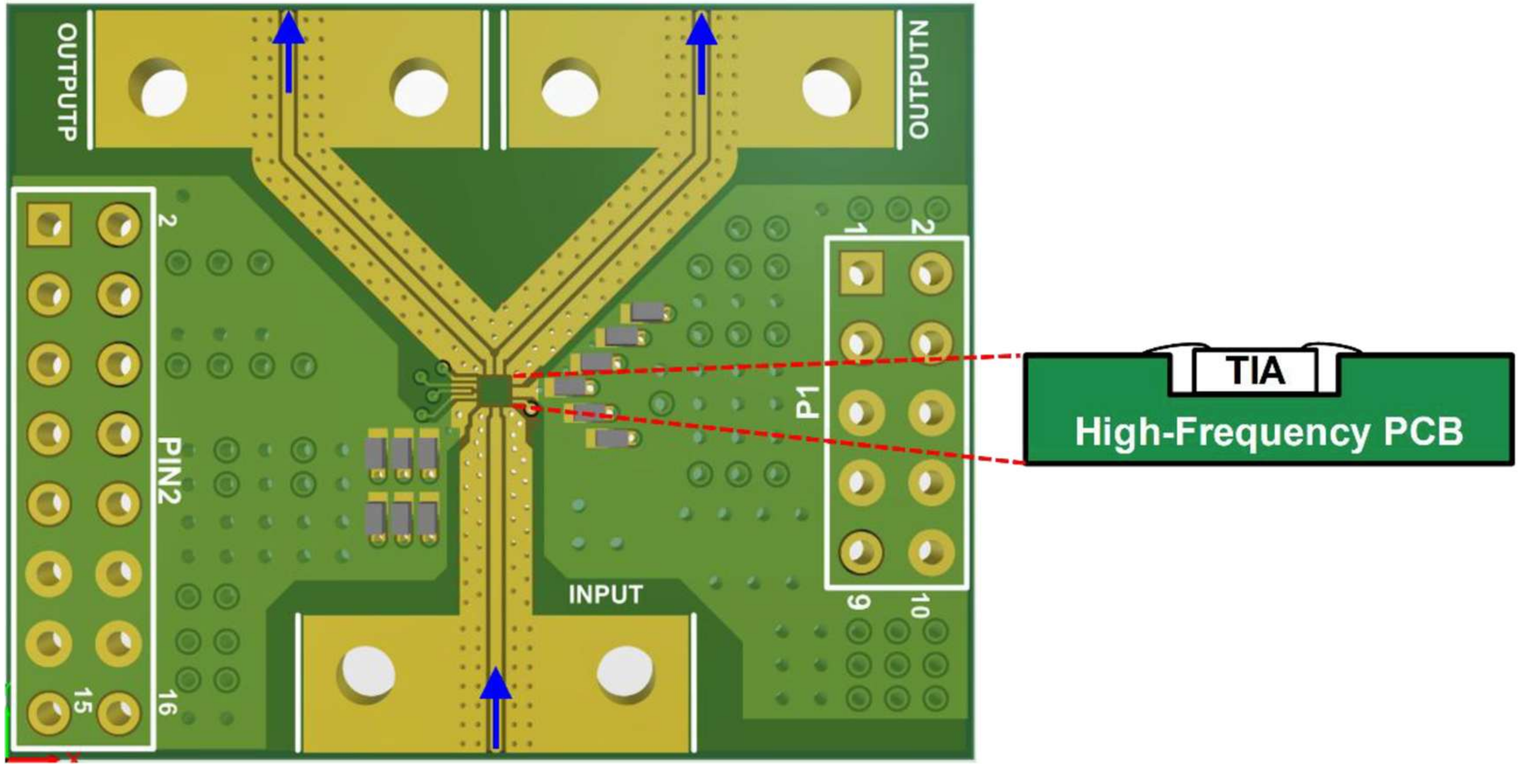


Back-up: Response of Proposed VGA in 100-Gb/s TIA



- 7.3 dB with 23.6 GHz BW
- -2.4 dB with 35.3 dB
- 9.7 dB dynamic range, 11.7 GHz BW variation

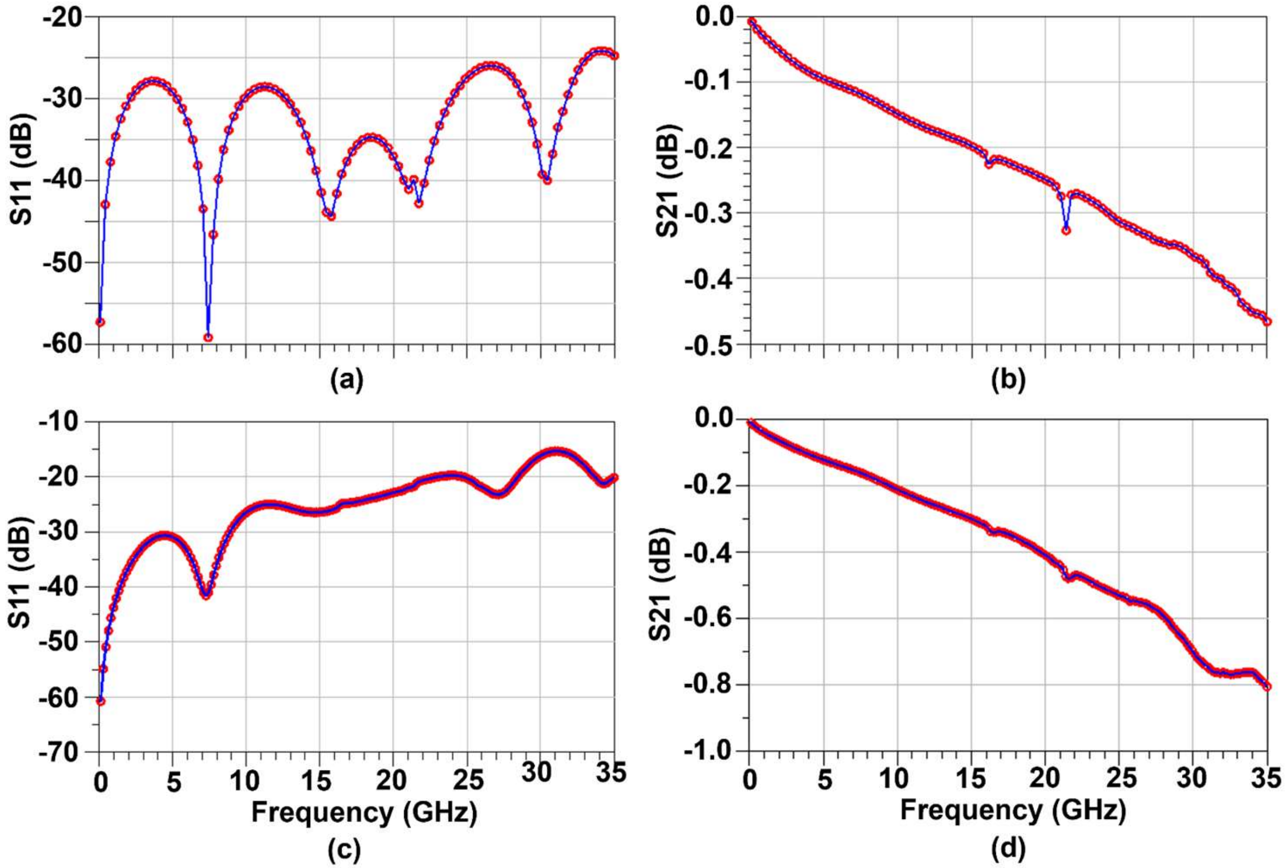
Back-up: High-Frequency PCB Design



- 10-mil RO4350B material for laminates
- PCB is trenched to accommodate the TIA die, reducing the length of bond wires

Back-up: High-Frequency PCB Design

Simulated S parameters of PCB traces



Input trace:

- S11 < -20 dB up to 35 GHz
- S21 > -0.4 dB at 25 GHz

Output trace:

- S11 < -10 dB up to 35 GHz
- S21 > -0.6 dB at 25 GHz