CMOS Photodetector and Limiting Amplifier for High Speed Optical Communication

by

Zhengxiong HOU

A Thesis Submitted to

The Hong Kong University of Science and Technology

in Partial Fulfillment of the Requirements for

the Degree of Master of Philosophy

in the Department of Electronic and Computer Engineering

July 2014, Hong Kong

Authorization

I hereby declare that I am the sole author of the thesis.

I authorize the Hong Kong University of Science and Technology to lend this thesis to other institutions or individuals for the purpose of scholarly research.

I further authorize the Hong Kong University of Science and Technology to reproduce the thesis by photocopying or by other means, in total or in part, at the request of other institutions or individuals for the purpose of scholarly research.

Hou Zhengxiong

Zhengxiong HOU

July 2014

CMOS Photodetector and Limiting Amplifier for High Speed Optical Communication

by

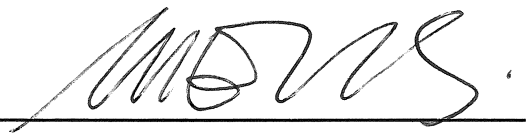
Zhengxiong HOU

This is to certify that I have examined the above Mphil thesis

and have found that it is complete and satisfactory in all respects,

and that any and all revisions required by

the thesis examination committee have been made.



Professor C. Patrick Yue (Thesis Supervisor)

Professor Ross. D. Murch (Department Head)

Department of Electronic and Computer Engineering

July 2014

Acknowledgements

First and most importantly, I would like to express my sincere gratitude to my supervisor, Prof. C. Patrick Yue, for his guidance and support throughout my study. It is a valuable experience to be Professor Yue's student. I have learned how to conduct research, how to treat people and how to pursue a successful life from him. All of these bring me a brand new world that has never been experienced before.

I would like to thank Dr. Li Sun for sharing his experience and knowledge with me during his one and a half year in the HKUST.

I would like to thank Prof. Kei May Lau and Prof. Philip K.T. Mok from the Department of Electronic and Computer Engineering for serving in the thesis proposal committee and for their insightful comments and suggestions during my Mphil thesis proposal.

I would like to thank the technician of the wireless lab, K. W. Chan for the help in the optical measurement. I would like to thank Miss Yu Li and Mr Yu Zhang in the optical lab for her support to my experimental work.

. I would like to thank my friends at the university, Dr. Rongxiang Wu, Dr. Xiaodong Huang, Dr. Lulu Peng, Dr. Quan Pan, Mr. Xiangming Fang, Mr. Zhou Fang, Miss Jie Ren, Mr. Yipeng Wang, Mr. Fengyu Che, Miss Liwen Jing, Mr Duona Luo for having fun together and for making my life colorful.

I would like to thank my girlfriend Grace for bringing me so many happiness and inspiration.

Finally, I would like to express my sincere gratitude to my parents for their unconditional love and support.

Table of Contents

List of Figures

List of Tables

List of Publications

[1] **Z. Hou**, Q. Pan, Y. Wang, L. Wu and C. P. Yue, "A 23-mW 30-Gb/s Digitally Programmable Limiting Amplifier for 100GbE Optical Receivers" in *IEEE RFIC Symp. Tech. Dig.*, Jun. 2014 (accepted).

[2] **Z. Hou**, Y. Wang, Q. Pan and C. P. Yue, "A 25-Gb/s 32.1-dB CMOS Limiting Amplifier for Integrated Optical Receivers" in *Proceedings of IEEE International Conference on ASIC,* 2013.

[3] **Z. Hou**, Q. Pan, Y. Li, S. Feng, A. W. Poon and C. P. Yue, "Integrated CMOS Photodetectors for Short-Range Optical Communication" in *Proceedings of IEEE EDSSC* 2013.

[4] Quan Pan, **Zhengxiong Hou**, and C. Patrick Yue, "A 65-nm CMOS P-well/Deep N-well photodetector for fully integrated 850-nm optical receivers," revised and resubmitted to *IEEE Photonics Technology Letters*.

[4] Quan Pan, **Zhengxiong Hou**, Yipeng Wang, Yan Lu, Wing-Hung Ki, Keh Chung Wang, and C. Patrick Yue, "A 48-mW 18-Gb/s Fully Integrated CMOS Optical Receiver with Photodetector and Adaptive Equalizer," in *2014 IEEE Symposium on VLSI Circuits.*

[5] Q. Pan, **Z. Hou**, Y. Wang and C. P. Yue, "A 65-nm CMOS P-well/Deep N-well Avalanche Photodetector for Integrated 850-nm Optical Receivers", in *Proceedings of IEEE International Conference on ASIC,* 2013.

[6] Quan Pan, Yipeng Wang, **Zhengxiong Hou**, Yan Lu, Li Sun, Liang Wu, Wing-Hung Ki, Patrick Chiang, and C. Patrick Yue , "A 41-mW 30-Gb/s CMOS Optical Receiver with Digitally-Tunable Cascaded Equalization ," in *2014 IEEE ESSCIRC* (accepted).

[7] Li Sun, Yipeng Wang, Quan Pan, **Zhengxiong Hou**, Yan Lu and C. Patrick Yue, "A 26-Gb/s Optical Receiver Front-end in 65-nm CMOS," *2013 IEEE International Solid-State Circuits Conference Student Research Preview* (ISSCC SRP).

[8] Y. Wang, Y. Lu, Q. Pan, **Z. Hou**, L. Wu, W. Ki, and C. P. Yue, "A 3-mW 25-Gb/s CMOS Transimpedance Amplifier with Fully Integrated Low-Dropout Regulator for 100GbE Systems" in *IEEE RFIC Symp. Tech. Dig.*, Jun. 2014 (accepted).

ABSTRACT

Optical communication is essential in industrial applications and the consumer market. Active optical fiber has great potential to replace copper in short-distance wire line communication. Current products and some research focus on 100-Gb/s Ethernet. This is achieved by 10 channels, with each operating at 10-Gb/s. In our group, we have started building each block of a 25-Gb/s optical receiver for next generation Ethernet.

In this thesis, two major areas are covered. Firstly, CMOS photodetectors, including the n+/p-substrate, n-well/p-substrate, and n-well/Deep n-well/p-substrate photodiode and PNP phototransistors and the Darlington pair, are presented. Currently, the common photodetector is made of Ge, InGaAs or GaAs. Although Ge p-i-n photodiodes are proved CMOS process compatible, the standard CMOS process still cannot build these photodetectors integrated with the circuits. The measured responsivity of the CMOS photodetectors is extracted and built into a model for our circuit simulation. Secondly, a limiting amplifier with high gain and large bandwidth is presented. Bipolar transistors in III-V compound technology used to be employed in high speed front ends due to their high mobility and low noise, but they cost much power and area. Currently, advanced CMOS technology is more attractive in terms of integration and power consumption. In this thesis, a CMOS limiting amplifier based on the structure of the modified Cherry-Hooper amplifier design is presented in detail.

The CMOS photodetector and the limiting amplifier are fabricated in TSMC 65 nm CMOS technology with f_T=185 GHz. The n-well/p-substrate has the largest bandwidth, 120 MHz, and the Darlington pair has the highest responsivity, 1176 mA/W. Simulation results show

that the CMOS photodiode is capable of achieving a 14Gb/s optical receiver. The measured results of the 25-Gb/s optical receiver with off-chip photodiode indicate that the limiting amplifier achieves a high gain and large bandwidth with low power consumption 23 mW.

CHAPTER 1

Introduction

In this chapter, background research, contribution and organization of the thesis are given. First, applications and challenges of short-range optical communication are discussed in Section 1.1. The photodetector and limiting amplifier in the optical receiver, as major contents of the thesis, are introduced in Section 1.2. Finally, the organization of the thesis is given in Section 1.3.

1.1 Applications of short-range optical communications

The rapid growth of global data communications, such as cloud computing and high-definition video watching, brings challenges in the proliferation of the scale of metro inter-data centers, corresponding to inter links over 100 meters to tens of thousands of meters. Major network providers have predicted that global data center traffic will reach 7.7 zeta bytes (trillion gigabytes) by the year 2017, a three-fold increase from 2012 to 2017, as shown in Fig. 1.1.

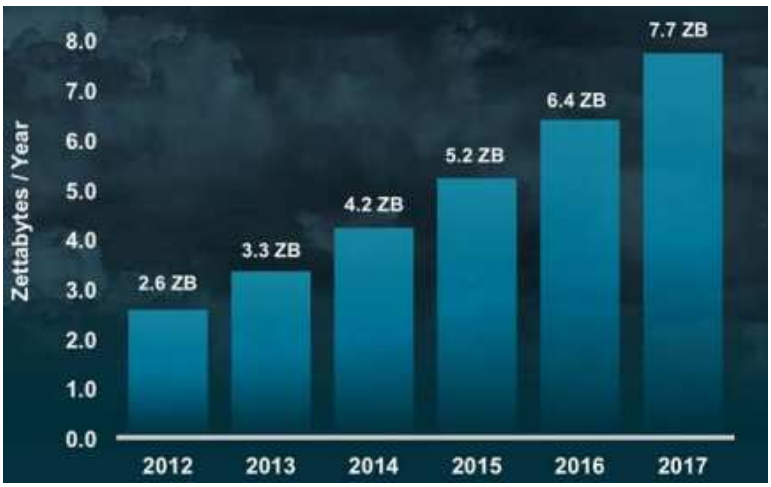


Fig. 1. 1. Global data center IP traffic growth estimation by Cisco, 2012–2017 [1.1].

As the scale of data centers, as shown in Fig. 1.2, increases dramatically, a high-speed, low-cost and power-efficient interconnects' solution becomes much more vital than ever before for processing the huge amount of data. The data rate requirement has reached the bandwidth limit of conventional copper cables. Optical links are preferred for telecommunication applications because fiber has advantages over a copper wire in terms of lower loss, crosstalk, electromagnetic interference (EMI), better cooling and less weight [1.2]. Single-mode fibers and a 1550-nm wavelength laser source are widely deployed for long-haul application, over 10 kilometers. In data centers, active optical cable (AOC), which is typically used for connectivity up to tens of meters, using multi-mode fiber (MMF) as the transmission path and a 850-nm vertical-cavity surface-emitting laser (VCSEL) as the light source, are being pursued by researchers and industry.

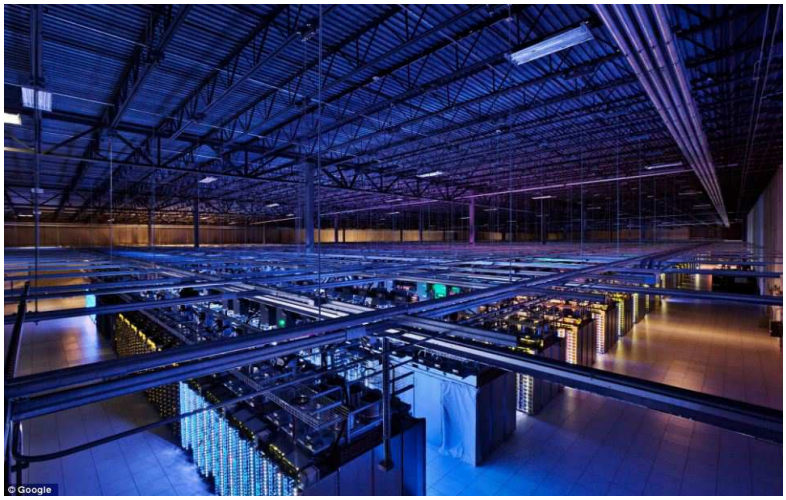


Fig. 1. 2. Google's server farm over 115,000 square feet of space in Council Bluffs, Iowa.

In high speed communications, the IEEE P802.3ba Ethernet Standard has been proposed as the standard for 100-Gb/s Ethernet (100 GbE). The first generation of 100-GbE opto-electronics (OE) is based on 10 x 10 Gb/s electrical lane and optical lane architectures, such as the SFP module in Fig. 1.3. For the next generation 100 GbE, OE communication will be achieved by 4 x 25 Gb/s lanes. In a high density data center, the cost-effective MMF

technology and VCSEL are chosen at the interface to take advantage of the development of advanced technology nodes. An example is shown in Fig. 1.4. In this thesis, the research focused on the optical receiver is conducted.

Fig. 1. 3. 10-Gb/s Optical Transceiver MMF SFP from Avago.

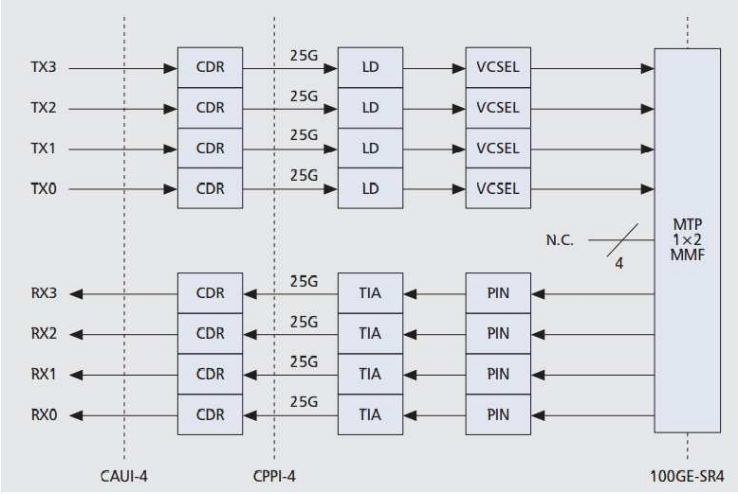


Fig. 1. 4. Next generation 100-Gb/s high density data center parallel MMF optics [1.3].

1.2 Review of the CMOS photodetector and limiting amplifier

A typical optical receiver is shown in Fig. 1.5. The transimpedance amplifier (TIA) converts the small input photocurrent from the photo detector (PD) into voltage. Next, a DC offset cancellation (DOC) circuit is required to reduce the DC offset and to convert the single-

end signal to differential. Before the equalizer (EQ) compensates for the loss in high frequency from the PD, the main amplifier (MA) increases the amplitude of the signal to protect the TIA from the noise of the EQ, while a limiting amplifier (LA) is employed to amplify the signal further to meet the input sensitivity requirement of the clock and data recovery (CDR). Lastly, the CDR recovers the signal and clock for the de-serializing.

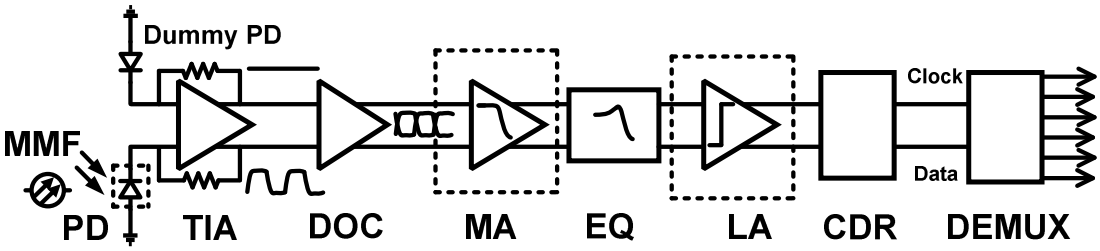


Fig. 1. 5. Block diagram of an optical receiver front-end for a 100GbE system.

In this work, the CMOS photodetector and limiting amplifier in the optical receiver are a major part of the discussion.

1.2.1 Review of the CMOS photodetector

Many publications in recent years have demonstrated that CMOS photodetectors are capable of multi-gigabyte optical communications. One reason for choosing the CMOS photodetector in short-range optical communications is that silicon is able to absorb at a wavelength of 850-nm, but not at 1550 nm. The other reason is that a fully integrated solution can avoid bond-wired parasitics, IR drop and capacitance from ESD protection.

Sandage and Connelly [1.4] discussed six photo-detectors' configurations produced in standard digital CMOS technology. The measured response comparison of the photo-detectors revealed that a vertical photo-detector absorbed less photonic power than a lateral structure. Radovanovic et al. [1.5] firstly proposed a 3-Gb/s monolithic optical receiver with an n-well/p-substrate CMOS photodiode, which showed that a CMOS photodiode could be

used in giga-byte optical communication. To further increase the operating speed of a CMOS photodiode, many techniques are applied. Lee and Park [1.6] used a slop-detection adaptive equalizer and differential photodiode structure [1.7] to achieve an 8.5-Gb/s optical receiver. Huang et al. [1.8] compared a strip and meshed spatially modulated photodetector and biased the PD in avalanche mode to gain a 6.9-GHz bandwidth for a 10 Gb/s data rate. Lee and Choi [1.9] proposed the smallest size CMOS avalanche photodetector (APD), enhancing the bandwidth to 7.6 GHz.

1.2.2 Review of the limiting amplifier

A limiting amplifier is widely used in high speed applications. It was made up of bipolar transistors [1.10] due to the high mobility. As the f_T of the CMOS technology has increased, the CMOS limiting amplifier has interested many researchers.

Gala and Razavi [1.11] presented a 10-Gb/s limiting amplifier based on an active feedback CMOS Cherry-Hooper amplifier under 1.8-V supply. In [1.7], a limiting amplifier with a negative capacitance and resistance was achieved. Weiss et al. [1.12] proposed a limiting amplifier with the feature of a digitally programmable loading resistor to compensate for the PVT variations in a data rate of 40 Gb/s.

1.3 Organization of the thesis

This thesis is organized as follows. In Chapter 2, a total of seven CMOS photodetectors are described and characterized. The performances of the photodetector and limiting amplifier are experimentally demonstrated. The measured responsivity of the n-well/Deep n-well/p-substrate photodiode is extracted and made into a model. In the spectra simulation, it is shown that the optical system with a CMOS photodetector can reach 14 Gb/s. In Chapter 3, firstly, the high speed performances of the inverter amplifier, NMOS amplifier and current mode logic (CML) are compared. Then a modified CMOS Cherry-Hooper

amplifier is designed, demonstrated and characterized. In Chapter 4, a limiting amplifier design for the 25-Gb/s optical receiver is characterized and discussed. The limiting amplifier integrated with the other circuit blocks and off-chip photodiode is measured at a data rate of 25 Gb/s. Finally, conclusions and suggestions for future work are given in Chapter 5.

References:

[1.1] Cisco Global Cloud Index: Forecast and Methodology, 2012–2017, 2013.

[1.2] A. C. Carusone, H. Yasotharan and T. Kao, "CMOS Technology Scaling Considerations for Multi-Gbps Optical Receivers With Integrated Photodetectors," *IEEE J. Solid-State Circuits*, vol. 46, no. 8, pp. 1832–1841, Aug. 2011.

[1.3] Beyond 100G Client Optics, Finisar Corp.

[1.4] R. Sandage and J. Connelly, "Producing phototransistors in a standard digital cmos technology," in *Proc. Circuits and Systems*, 1996, pp. 369-372 vol.1.

[1.5] S. Radovanovic, A. Annema and B. Nauta, "A 3-Gb/s Optical Detector in Standard CMOS for 850-nm Optical Communication," *IEEE J. Solid-State Circuits*, vol. 40, no. 8, pp. 1706–1776, Aug. 2005.

[1.6] D. Lee, J. Han, and S. M. Park, "An 8.5-Gb/s fully integrated CMOS optoelectronic receiver using slope-detection adaptive equalizer," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2861–2873, Dec. 2010.

[1.7] M. Kujik, D. Coppée, and R. Vounckx, "Spatially modulated light detector in CMOS with sense-amplifier receiver operating at 180 Mb/s for optical data link applications and parallel optical interconnects between chips," *IEEE J. Select. Topics Quantum Electron.*, vol. 4, pp. 1040?045,Nov.-Dec. 1998.

[1.8] S. Huang, W. Chen, Y. Chang, and Y. Huang, "A 10-Gb/s OEIC with meshed spatially-modulated photo detector in 0.18-μm CMOS technology," IEEE J. Solid-State Circuits, vol. 46, no. 5, pp. 1158–1169, May 2011.

[1.9] M. J. Lee, W. Y. Choi, "Area-Dependent Photodetection Frequency Response Characterization of Silicon Avalanche Photodetectors Fabricated With Standard CMOS Technology", *Electron Devices, IEEE Transactions on*, On page(s): 998 - 1004 Volume: 60, Issue: 3, March 2013

[1.10] Y. Baeyens, G. Georgiou, J. S. Weiner, A. Leven, V. Houtsma, P. Paschke, Q. Lee, R. F. Knopf, Y. Yang, L. Chua, C. Chen, C. T. Liu, and Y.-K. Chen, "InP D-HBT IC's for 40 Gb/s and higher bitrate lightwave transceivers," IEEE J. Solid-State Circuits, vol. 37, no. 9, pp. 1152–1159, Sept. 2002

[1.11] S. Galal and B. Razavi, "10 Gb/s Limiting Amplifier and Laser/Modulator Driver in 0.18-μm CMOS Technology". *IEEE J. Solid-State Circuits*, vol.38, pp. 2138-2146, Dec. 2003

[1.12] J. R. M. Weiss, M. L. Schmatz, and H. Jaeckel, "A 40 Gb/s, digitally programmable peaking limiting amplifier with 20-dB differential gain in 90 nm CMOS," in Proc. IEEE RFIC Symp., 2006.

CHAPTER 2

Integrated CMOS Photodetecotors Characterization and Design

2.1 Introduction

Integrated optical receiver systems with data rate up to 25 Gb/s are becoming more attractive for short-range communication. The introduction of optics enables a high density of interconnection without resistive loss. Currently, optical communication with a wavelength of 1550 nm is not cost-efficient for shorter interconnections between cabinets and chips. As the 850-nm VCSEL (vertical cavity surface emitting lasers) is of low-cost for fabrication [2.1] and of high speed [2.2] for high performance computing in data centers and large bandwidth interconnects, a fiber channel with a serial data rate over 10 Gb/s at 850 nm is achievable. To drive down the cost, given the low responsivity of the CMOS photodetector compared with the other materials in Fig. 2.1, an integrated photodiode or phototransistor for the optical receiver in a standard CMOS process is highly desirable, similar to the integration of a CMOS wireless receiver. The avalanche photodetector (APD) has been studied by many researchers to realize high responsivity and high bandwidth [2.3], [2.4] by providing the avalanche gain to increase the gain bandwidth product in the avalanche region. However, the APD in the avalanche region needs a high bias voltage, typically over 10 V. Moreover, the dark DC current in the avalanche mode may be very large, typically around 1 mA, which contributes extra power dissipation.

This chapter investigates the configurations of different vertical photodetectors' structures in a 65-nm CMOS technology with normal bias voltages of 1.0 V and 3.0 V. In Section 2.2, the relationships between the responsivity (R), signal to noise ratio (SNR) and bit error rate (BER) are analyzed. In Section 2.3, CMOS photodiodes with different junction widths and implants are discussed. The structure of the n-well/p-substrate is demonstrated carefully while the differential photodiode structure to improve the high speed performance is explained. Then, the equivalent model of the photodiode is given for further simulation. In Section 2.4, phototransistors and Darlington vertical pair transistors are also implemented for higher responsivity. In Section 2.5, several issues in the fabrication are clarified. In Section 2.6, the measurement results and the simulated results with the continuous equalizer are shown and compared. Finally, a summary is given in Section 2.7.

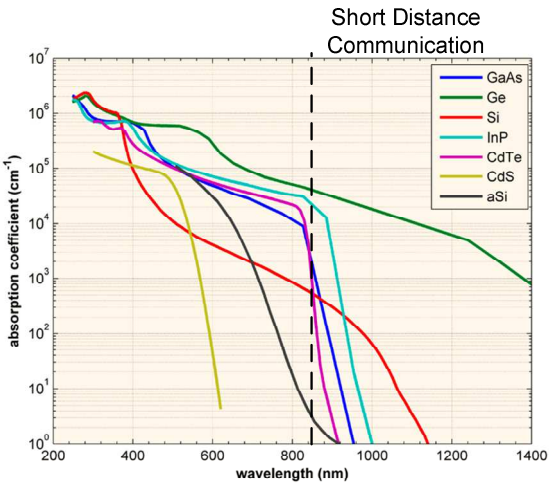


Fig. 2.1. Absorption coefficient data for different materials

2.2 Responsivity and SNR requirement

The responsivity R is defined as the ratio of the photo current I_{PD} generated from the photodetector and the input optical power P_{IN} coupled from the fiber channel,

$$R = \frac{I_{PD}}{P_{IN}}. \tag{2.1}$$

The responsivity is one of the major parameters for photodetectors. Generally, the responsivity is able to be increased by enlarging the illuminating surface area of the PD, but it will introduce much capacitance, which limits the total bandwidth of the receiver. The responsivity determines the input photo current I_{PD} and signal to noise ratio (SNR) for a given bit error rate (BER). Further discussion about the SNR will be covered in Chapter 3.

In a broadband circuit, with fixed input power, the total noise can significantly impact the detection of the data. It is important to determine how much noise can be tolerated for a given bit error rate (BER). Because the TIA converts current into voltage in the optical receiver, if the integrated noise is referred to the input of the TIA, it becomes the noise current. The total noise current I_N is the sum of the referred noise current from the receiver and the shot noise current from the PD. As calculated in detail in [2.5], the BER follows the error function

$$BER = \frac{1}{2} erfc\left(\frac{I_{PD}}{\sqrt{ISI_v^2 + I_N^2}}\right), \tag{2.2}$$

where the ISI_v represents the variance of the inter symbol interference, which is related to the bandwidth of the channel and can be minimized by proper equalization and large bandwidth. Therefore, the effect of the ISI is negligible. The SNR in this design is given as

$$SNR = \frac{I_{PD}}{I_{Noise}}. \tag{2.3}$$

Typically, the SNR is required to be larger than 7 to have the BER below 10^{-12}. Once the bandwidth of the system is settled, the responsivity of the photodetector is determined by the SNR. In the following part, the ways to increase the responsivity (R) of the PD are discussed.

2.3 Responsivity analysis and structure of the CMOS photodiode

The photodiode in the structure is a PN junction diode, which is illuminated by the light. The incident photo energy (hc/λ) penetrating into the silicon is absorbed. A part of the photons larger than the energy band gap of the material is able to incur electron-hole pairs. Due to the electrical field, the pairs are swept out to generate the photo current.

2.3.1 CMOS photodiode

Compared with the other materials' photodetectors, CMOS PDs suffer from limited responsivity and bandwidth due to their inherent limitation [2.6] of low absorption rate at wavelength 850 nm, as shown in Fig. 2.1. The speed of Si photodiodes is limited by the carrier transit time in the thick absorption layer due to the long absorption length in Si. According to the Beer-Lambert law, the absorption depth is a random variable with a probability density function (PDF) as below:

$$p_d(x) = \frac{e^{-x/d}}{d}, \tag{2.4}$$

where the variable x is the distance to the surface of the PD and d is the mean depth of the variable (penetration coefficient) dependent on the wavelength (λ) of the light and device material. For example, at $\lambda = 850$ nm, the mean depth d of the major materials for the commercial PD, Ge, GaAs, and InGaAs, is below 1 um but the d of silicon is 18 μm. And the depth of the nwell in the standard CMOS process is around 1.5~2.0 μm and the deep nwell is around 3~4 μm, as shown in Fig 2.2. The width of the depletion region W_{dep} is given as

$$W_{dep} = \sqrt{\frac{2\varepsilon}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)\left[V_R + \frac{kT}{q}\ln\left(\frac{N_A N_D}{n_i^2}\right)\right]}, \tag{2.5}$$

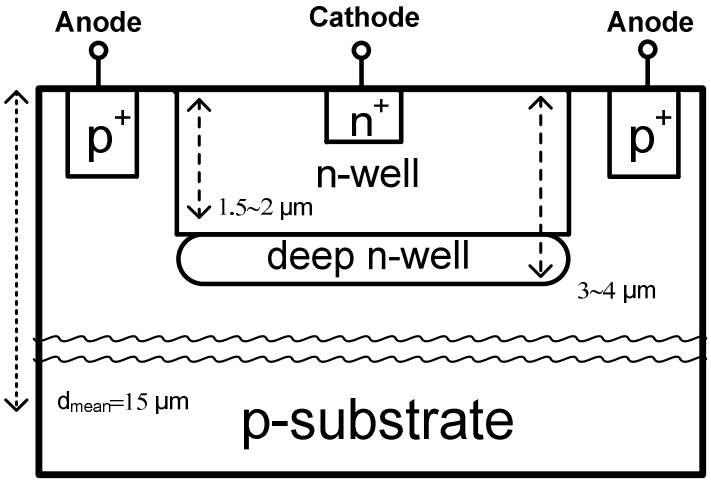


Fig. 2.2. Simplified cross section view of deep nwell/p-substrate photodiode.

where the ε is the silicon permittivity, q is the elementary charge, N_A and N_D are the doping concentrations, and V_R is the reverse manually-biased voltage. k, T, and n_i represent the Boltzmann's constant, the absolute temperature and the intrinsic carrier concentration in silicon respectively.

The doping concentrations are determined by the process. From (2.5), to maximize the width of the depletion region, one needs to minimize the doping concentrations and to maximize the reverse voltage over the junction. In this CMOS process, p+, p-substrate, n+, n-well, and deep n-well layers are available for building junctions for the photodetectors. The lowest doping p-type material is the p-substrate, and the lowest doping n-type material is the deep n-well. In this design, the basic n-well/p-substrate diode is selected for high speed application [2.7].

The analytical model of a PD can be expressed as shown in Fig. 2.2 The total bandwidth (BW_{-3dB}) can be expressed as

$$BW_{-3dB} = \frac{1}{2\pi(t_{nw} + t_{psub} + t_{dep} + \tau_{RC})} = \frac{1}{\sqrt{f_{BW\_int}^{-2} + f_{BW\_ext}^{-2}}}, \tag{2.6}$$

where t_{nw}, t_{psub} and t_{dep}, are the average time for the electrons to reach the surface from the n-well, p-substrate and depletion region respectively, and collectively, they determine the intrinsic f_{BW_int}. The τ_{RC}, representing the f_{BW_ext}, is determined by the extrinsic junction capacitance and loading resistance. Due to the low recombination rate and the short distance to the contacts, the equivalent bandwidth of the electrons in the n-well region f_{BW_well} is high. In contrast, the electrons in the p-substrate have to travel a long distance to the substrate contacts and, hence, have a higher recombination rate, which means a low equivalent bandwidth f_{BW_sub}. On the other hand, the speed of the electrons in the depletion region is higher than the p-substrate and n-well since a high electric field exists, as shown below:

$$f_{BW\_sub} < f_{BW\_well} < f_{BW\_dep.} \tag{2.7}$$

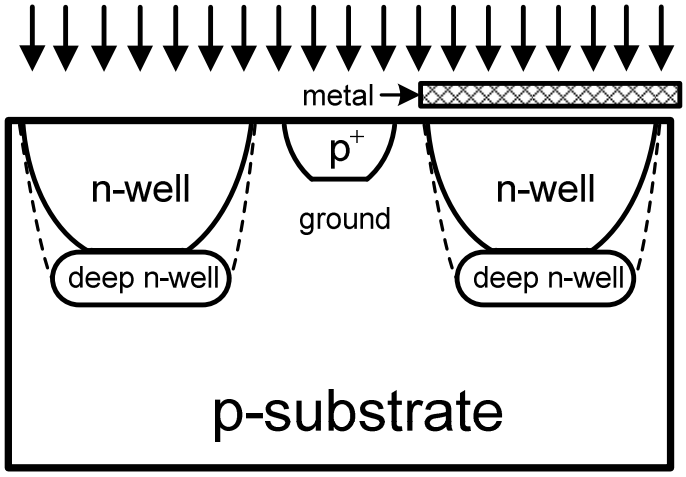
According to [2.8], the f_{BW_well} ranges from 450 to 900 MHz. The f_{BW_sub} is typically about 3 to 5 MHz, which limits the overall bandwidth. The f_{BW_dep} determined by (2.8) is up to several gigahertz:

$$f_{BW\_dep} \approx \frac{0.4\upsilon}{W}, \tag{2.8}$$

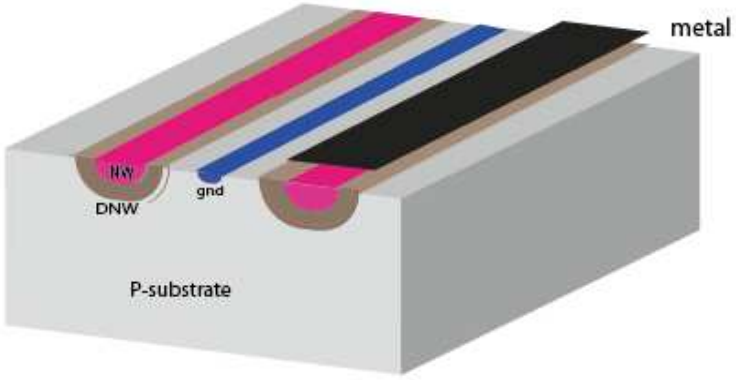
where W represents the space charge region thickness and υ is the speed of the electron. The total current is expressed as

$$I_{tot} = I_{n\text{-}well} + I_{p\text{-}sub} + I_{dep}. \tag{2.9}$$

By increasing the f_{BW_int}, W should be decreased; however, a small W introduces large capacitance, reducing the f_{BW_ext}. Therefore, there exists an optimum W for maximizing the overall bandwidth. Based on [2.9], the effect of the depletion region width is dominant and an n-well/p-substrate is utilized to make W large. Besides this, when a PD is top-illuminated, based on the Beer-Lambert's Law, it is preferred to be vertical to widen the depletion region to maximize light absorption.



(a)



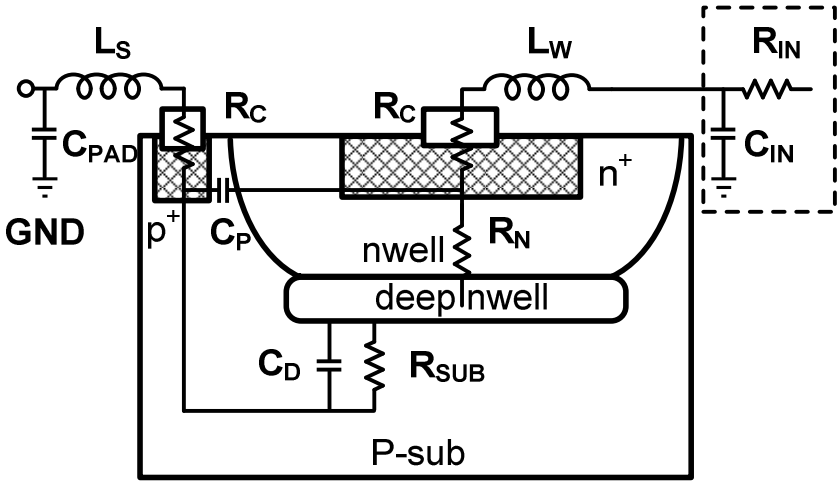
(b)

Fig. 2.3. (a) Cross sectional view of the top-illuminated differential photodiode (b) layout top and cross sectional view of the differential photodiode.

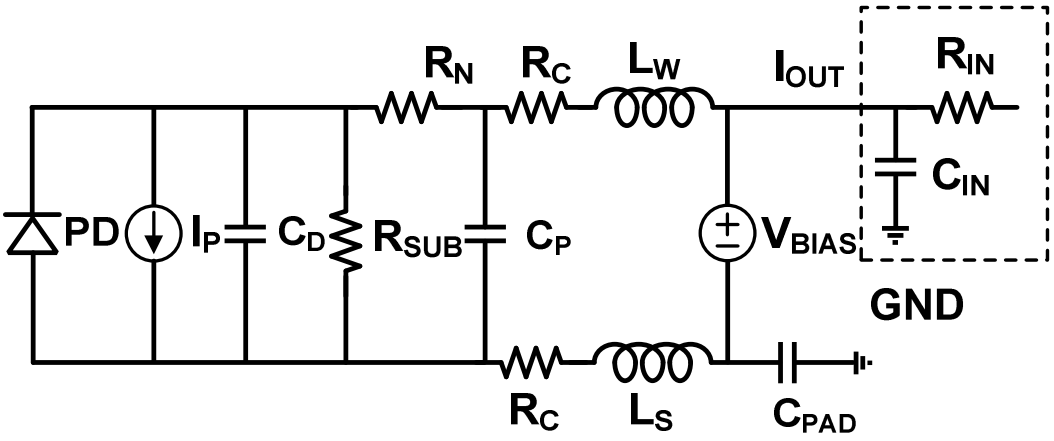
In addition to single-ended structures, differential spatially-modulated photodetectors (SMPD) [2.10] are also studied. Fig. 2.3 (a) shows its cross section. The deep n-well/p-substrate junction is deeper than the n-well/p-substrate junction, so it can absorb more 850-nm light as the absorption depth is about 15 μm below the surface. One of the paths consists of $I_{p\text{-}sub}$, $I_{n\text{-}well}$ and I_{dep} and the other side only consists of $I_{p\text{-}sub}$. Then, a differential TIA is used to remove the $I_{p\text{-}sub}$ to achieve a large bandwidth. But the illumination area is halved, as illustrated in Fig. 2.3 (b). Photodiodes without the deep n-well are also fabricated and measured for comparison.

2.3.2 Photodetector equivalent model

To facilitate the PD integration with the advanced CMOS technology, a compact and accurate photodetector model built of the resistors, capacitors and inductors from the DC to high frequency is highly needed for the circuit simulation before fabrication, as shown in Fig. 2.4.



(a)



(b)

Fig. 2.4. (a) The schematic cross sectional view of n-well/deep n-well/p-substrate photodiode (b) the equivalent photodiode model.

In this thesis, the equivalent circuit model is a modified version of the model in [2.11] for analysis, including the pad and bonding parasitic. R_N is formed by the n-well and p-substrate. R_C is the combination of the contact resistance formed by the n^+ or p^+ material and the series resistance of the bonding inductor. R_{SUB} is the resistance of the substrate to the ground. C_D is the depletion capacitance at the reverse bias voltage V_{BIAS}, and C_P is the capacitance of the anode and cathode, while the C_{PAD} is the capacitance of the bonding pad. R_{in} and C_{in} is the equivalent input impedance. During the PD measurement, the input impedance is the equipment RF 50 ohm and in the optical receiver, it becomes the input impedance of the transimpedance amplifier. The R_{in} determines the external bandwidth of the photodiode.

2.4 CMOS transistor and Darlington pairs

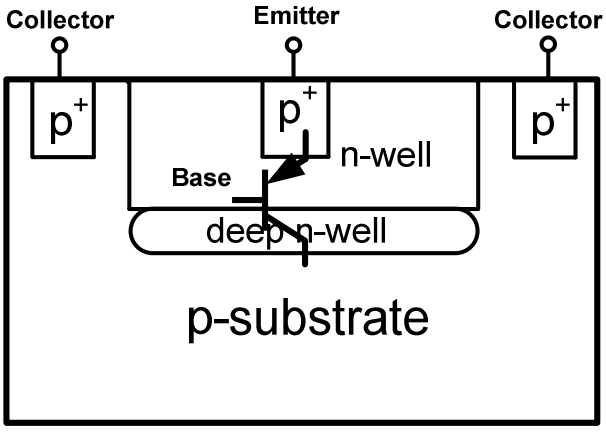
The phototransistors that used to be applied in the image sensor are modified for optical communication in this design [2.12]. As the analysis shows, the differential structure has a better bandwidth but sacrifices the current amplitude in a low frequency; the

phototransistor and Darlington pair has a larger responsivity than the photodiode. Thus, if the two points were combined, phototransistors in differential structures would have better high frequency performance. Fig. 2.5 (a) shows the vertical PNP transistor cross-section view. The electrons generated by the photons are swept out of the space charge region, forming the light current I_L. Then, the generated holes will flow into the n-type base, making it positive. The BC junction is reverse biased and the BE junction is forward biased. The collector receives the light, while the emitter amplifies the current. The relationship between I_L and I_E is given by

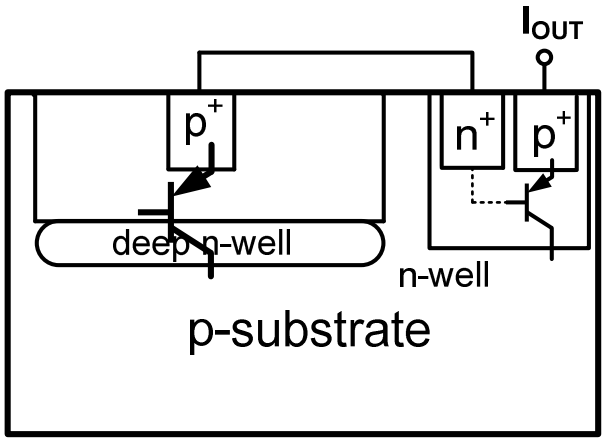
$$I_E = (1+\beta)I_L, \tag{2.10}$$

where the β is the transistor amplification coefficient. Although the phototransistor can amplify the received signal, IL is limited by the low transistor. To further enhance the responsivity, a Darlington pair is employed to achieve extra current gain [2.13] as described below

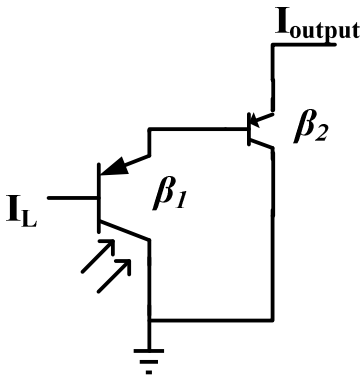
$$I_{output} = (1+\beta_1)(1+\beta_2)I_L. \tag{2.11}$$



(a)



(b)



(c)

Fig. 2.5. (a) The cross sectional view of the PNP phototransistor (b) cross sectional view of the Darlington pair (c) the equivalent circuit of the Darlington pair.

2.5 Influence of technology scaling and reflection

There are two issues which need to be pointed out. First, unlike the circuit design, the advanced process does not offer progress in the CMOS photodetector performance. The dielectric above the photodiode may cause reflection losses. For example, self-aligned-silicide is laid at the surface to reduce the contact resistance of the highly doped region (n^+ and p^+) but it hampers light absorption [2.6]. In this design, the silicide blocker is built above the exposed areas to receive light. Second, the advanced process does not bring improvement in the performance of the PD [2.14]. According to the derivation in (2.5), the increasing-doped

material and lower supply voltage bring a negative effect on the width of the depletion region, which decreases the depletion current and increases the diffusion current as well as the diode capacitance. All the issues above bring challenges to the design of the following optical receiver.

2.6 Experimental results and optical receiver simulation

Fig. 2.6 demonstrates the die photo of the seven photodetector test structures. The differential PD consists of 6 fingers, each of which is 10×60 μm^2. The distance between two adjacent fingers is 1.5 μm. The phototransistor and Darlington pair's light receiving area is 24×24 μm^2. The differential phototransistor and Darlington pairs are also fabricated for comparison.

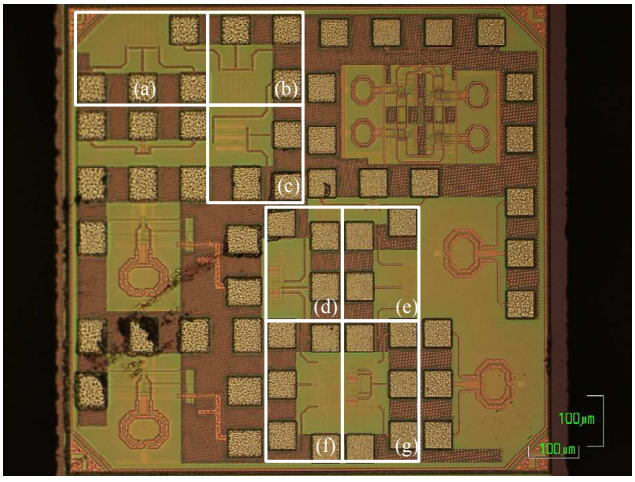


Fig. 2.6. Die photo of single-ended (a) n-well/p-substrate photodiode (b) n-well with deep n-well/p-substrate photodiode (c) PNP phototransistor (d) Darlington pair and differential (e) photodiode (f) phototransistor (g) Darlington pair.

The testing setup is shown in Fig. 2.7. The input signal is from the SDG Model 12050 programmable pattern generator Measurement under a microscope is also shown in Fig. 2.8. The 850-nm light source is produced by the Light Peak module from SAE (HK). A

commercial multi-mode fiber (MMF) from Go4fiber with a diameter of 62.5 μm is employed for illumination.

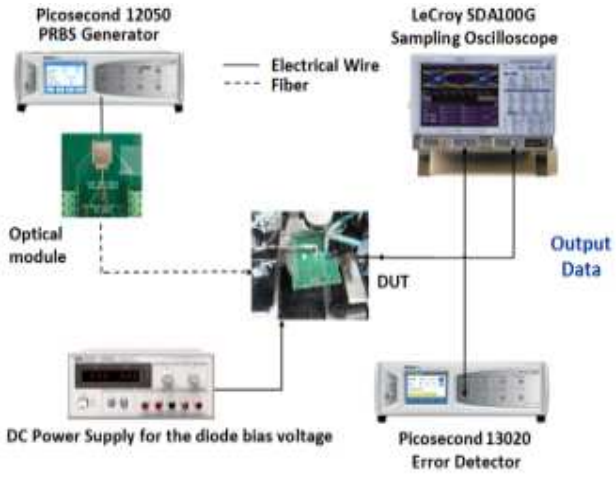


Fig. 2.7. Testing setup diagram.

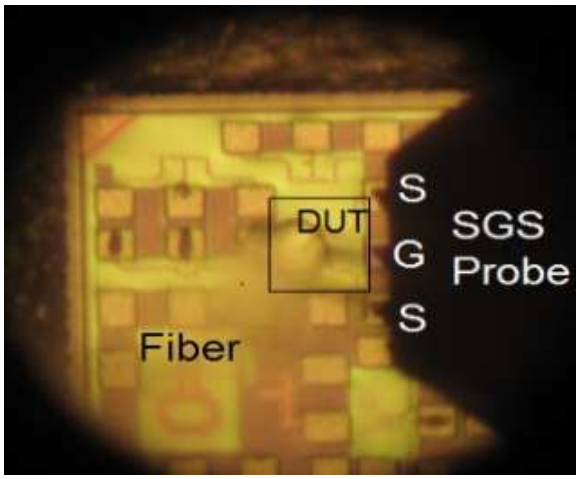
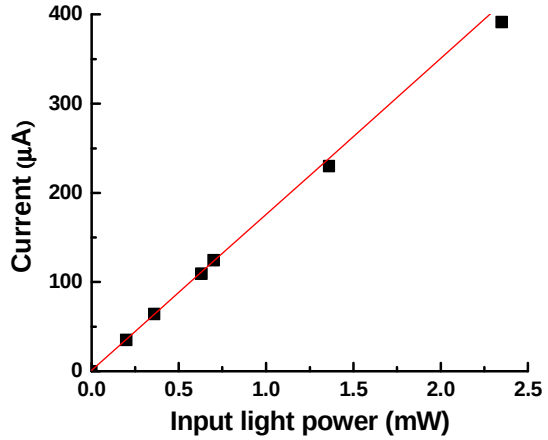
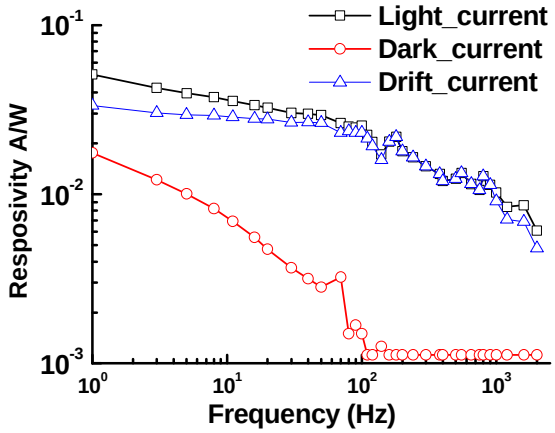


Fig. 2.8. Testing with RF probes and fiber under the microscope.

The testing on the PD has two parts. One is the DC response measurement: scanning the incident light power on the x axis and measuring the photo currents of the PD on the y axis. The slope of the curve is the average DC responsivity. The other part is the frequency response measurement: sweeping the frequency and measuring the photo current. The seven structures follow the same the measurement procedures. Fig. 2.9 shows the DC and frequency response measurements for the SMPD, also known as differential photodiodes. The DC responsivity of the SMPD is represented by the light current, which is the sum of the diffusion current and drift current, while the dark current is the diffusion current.



(a)



(b)

Fig. 2.9. (a) DC and (b) frequency response measurements for SMPD biased at 1 V.

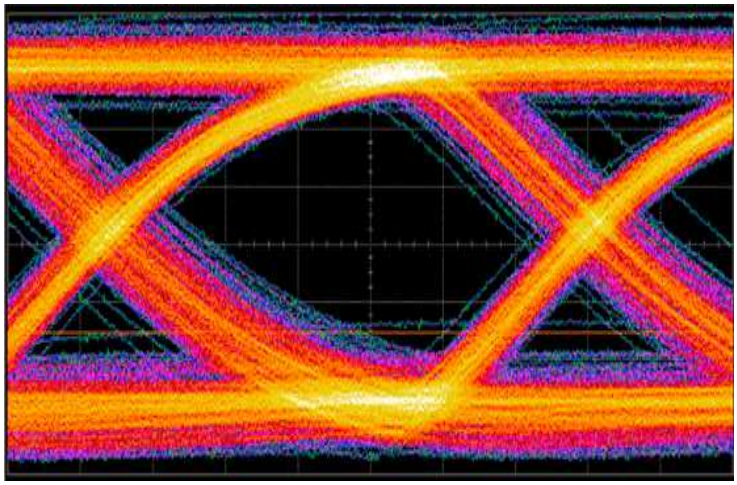


Fig. 2.10. Measured eye-diagram for a 30 Mb/s 2^{31}-1 PRBS pattern (vertical scale 25.00mV/div; horizontal scale 5.00ns/div)

Table 2.1. Summary of Measured PD Performance.

	(a)	(b)	(c)	(d)	(e)	(f)	(g)
Responsivity (R) @1MHz(mA/W)	140	170	635	1176	33.5	17.1	53.6
Normalized R ($\mu A/(W\times\mu m^2)$)	40	48	207	383	9.7	43.6	75.5
Bandwidth (MHz)	6.4	7.1	10	15	120	20	16
Roll-off (dB/decade)	4.8	4.2	18	21.3	8.6	16	19
Dark current (pA)	4	27	1000	1600	N/A	N/A	N/A
Bias voltage (V)	1	1	3	3	1	3	3

Fig. 2.10 shows the measured eye diagram of the differential photodiode, which achieves a bandwidth of 120 MHz with a PRBS 2^{31}-1 test pattern. The eye diagram can be achieved at 30 Mb/s. If the data rate is higher, there is no clear eye diagram. The reason for this is that the input the signal is too small compared with the inherent noise from the equipment. In the integrated optical receiver, the PD is followed by a typical low noise TIA and the signal at a higher rate will be much larger than the noise, which will be shown in the next chapters. Besides this, an octagonal PD will have a better responsivity while reducing the capacitance.

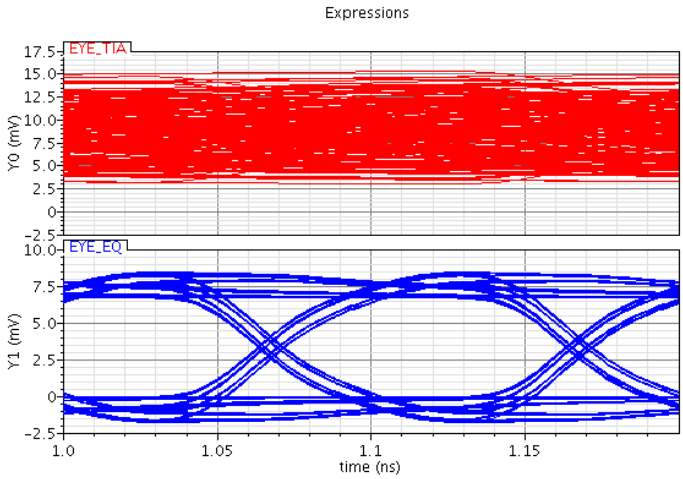


Fig. 2.11. The simulation results of the optical receiver front-end with the differential photodiode behavior model at 14 Gb/s, with and without equalizer.

Table 2.2. Performance Comparison (λ=850-nm)

	R* (mA/W)	BW* (MHz)	Roll-off (dB/decade)	CMOS Process	Date Rate for receiver
[2.7]	20	N/A	4.7	0.18-μm	10 Gpbs
[2.8]	30	2.5	5	65-nm	N/A
[2.8]	340	0.15	9	65-nm	N/A
[2.10]	N/A	0.6	4.7	0.18-μm	3 Gpbs
[2.15]	N/A	348	N/A	0.13-μm	8.5 Gpbs
This work (d)	1176	16	21	65-nm	N/A
This work (e)	33.5	120	8.6	65-nm	14 Gbps (simulation)

At the circuit level, the continuous time linear equalizer (CTLE) is designed to compensate for the high frequency loss of the CMOS photodetectors. A properly designed equalizer can compensate for the loss from the PD at high frequency, which can reach a data rate over 10 Gb/s. To further study the photodiode's performance at a high date rate, a simulation based on the extracted model of the differential photodiode is carried out. The whole system consists of the photodiode, the TIA and the equalizer. The performance at 14 Gbps random bit stream is shown in Fig. 2.11, in which the red curve is the output of the TIA and the blue eye diagram curve is at the output of the equalizer. Table 2.2 compares the PD performance with previously reported results.

2.7 Summary

Integrated CMOS photodetectors for optical communication enables customized optoelectronic communication, especially for high volume applications. The deep n-well/p-substrate PD performs better than the n-well/p-substrate PD. The phototransistor has a higher DC responsivity, but a much lower bandwidth. A PD equivalent circuit model is critical for designing the proper equalizer to compensate for the PD's limited bandwidth. According to the simulation results, an optical system with integrated photodiodes in standard CMOS technology is achievable over 10Gbps for λ=850-nm. Further work will focus on improving the responsivity of the photodetector at high frequency.

References:

[2.1] C. K. Lin and P. D. Dapkus, "Uniform wafer-bonded oxide-confined bottom-emitting 850-nm VCSEL arrays on sapphire substrates," *IEEE Photon. Technol. Lett.*, vol. 13, pp. 263–265, Apr. 2001.

[2.2] D. M. Kuchta, A. V. Rylyakov, C. L. Schow, J. E. Proesel, C. Baks, C. Kocot, L. Graham, R. Johnson, G. Landry, E. Shaw, A. MacInnes, and J. Tatum, "55Gb/s Directly Modulated 850nm VCSEL-Based Optical Link", *IPC 2012* post deadline paper PD1.5.

[2.3] H. S. Kang, M. J. Lee, and W. Y. Choi, "Si avalanche photodetectors fabricated in standard complementary metal–oxide–semiconductor process," *Appl. Phys. Lett.*, vol. 90, no. 15, pp. 151118-1–151118-3, Apr. 2007.

[2.4] M. J. Lee and W. Y. Choi, "A silicon avalanche photodetector fabricated with standard CMOS technology with over 1 THz gain–bandwidth product," *Opt. Exp.*, vol. 18, no. 23, pp. 24 189–24 194, Nov. 2010.

[2.5] J. Genoe, D. Coppee, J. H. Stiens, R. A. Vounckx, and M. Kuijk, "Calculation of the current response of the spatially modulated light CMOS detectors," *IEEE Trans. Electron Devices*, vol. 48, no. 9, pp. 1892–1902, Sep. 2001.

[2.6] T. K. Woodward and A. V. Krishnamoorthy, "1-Gb/s integrated optical detectors and receivers in commercial CMOS technologies," *IEEE J. Sel.Topics Quantum Electron.*, vol. 5, no. 2, pp. 146–156, Mar./Apr. 1999.

[2.7] S. Radovanovic, A.-J. Annema, and B. Nauta, "A 3 Gb/s optical detector in standard CMOS for 850 nm optical communication," *IEEE J. Solid State Circuits*, vol. 40, no. 8, pp. 1706–1717, Aug. 2005

[2.8] A. C. Carusone, H. Yasotharan and T. Kao, "Progress and Trends in Multi-Gbps Optical Receivers with CMOS Integrated Photodetectors," in *Proc.IEEE Custom Integrated Circuits Conf.*, pp. 1–8, Sep. 2010.

[2.9] G. Ghione, *Semiconductor Devices for High-Speed Optoelectronics.* Cambridge, UK: University Press, 2009.

[2.10] W. Z. Chen, Y. L. Cheng and D. S. Lin, "A 1.8-V 10-Gb/s Fully Integrated CMOS Optical Receiver Analog Front-end," *IEEE J. Solid-State Circuits*, vol. 40, no. 6, pp. 1388–1396, Jun. 2005.

[2.11] T. N. Swe and K. S. Yeo, *An Accurate Photodiode Model for DC and High Frequency SPICE Circuit Simulation*, Tech Proc. of the 2001 International Conference on Modelling and Simulation of Microsystems, 362-365

[2.12] L. Y. Leu, J. T. Gardner, and S. R. Forrest, "A high-gain, highbandwidth $In_{0.53}Ga_{0.47}As$/InP heterojunction phototransistor for optical communications," *J. Appl. Phys.*, vol. 69, no. 2, pp. 1052–1062, Jan. 1991.

[2.13] R. Sandage and J. Connelly, "Producing phototransistors in a standard digital cmos technology," in *Proc. Circuits and Systems, 1996*, pp. 369-372 vol.1.

[2.14] F. Tavernier and M. Steyaert, "High-speed optical receivers with integrated photodiode in 130 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 10, pp. 2856–2867, Oct. 2009.

[2.15] D. Lee, J. Han, and S. M. Park, "An 8.5-Gb/s fully integrated CMOS optoelectronic receiver using slope-detection adaptive equalizer," in *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2861–2873, Dec. 2010

CHAPTER 3

A High Speed Cherry Hooper Amplifier with Broadband Technique

3.1 Introduction

The Cherry-Hooper (CH) amplifier [3.1] traditionally consisted of bipolar transistors [3.2]. Recently, however, the CMOS Cherry-Hooper has been used in many applications, such as the adjustable delay cell in decision feedback equalizers (DFE) [3.3] and the variable gain amplifier (VGA) in 60-GHz direct-conversion receivers [3.4]. In this chapter, a modified CMOS CH amplifier with shunt peaking inductors and digital-tuned resistors is demonstrated. In Section 3.2, the performances of the inverter, NMOS common source amplifier and current mode logic (CML) amplifier at high speed are discussed. It also presents the reasons to choose the CML topology in high speed circuits. Then, several bandwidth enhancement techniques are shown in Section 3.3. Also in Section 3.3, the Cherry Hooper amplifier is explained in detail, and a small signal and noise analysis is given. A modified CMOS CH amplifier is then shown for broadband operation. In Section 3.4, a digital-tuned resistor scheme is proposed for the CH amplifier's robust operation over the effects of the process, voltage and temperature (PVT) variations. Last, a summary is included in Section 3.5.

3.2 High speed performance comparison

An inverter-based TIA is chosen in the optical receiver due to its low noise, low power and high transimpedance gain. However, after the single-ended input photocurrent is converted into voltage, the inverter, in Fig. 3.1 (a), is not suited for high speed operation for the following reasons [3.5]. Firstly, compared with the NMOS amplifier in Fig. 3.1 (b), the

gate capacitance of the inverter is almost doubled when working in amplification mode, which is not efficient. Secondly, since it works at high speed, the bonding wire effect at the supply and ground should be taken into consideration. Two series of waveforms of eye-diagrams are illustrated in Fig. 3.2 (a) (b) and (c). The left hand simulation has no bonding wire and the right hand has a bonding inductor L_s = 1.5 nH and R_s = 2.5 Ω connected to the supply and ground, respectively. The NMOS amplifier normally performs better than the inverter because the loading resistor degrades the Q-factor of the bonding inductor, while the current mode logic (CML) in Fig. 3.1 (c) almost has no ripple. According to the simulation results, a single-ended structure suffers more from the VDD and GND bonding wire effect compared to the CML. Hence, a CML-based amplifier is preferred for the high speed operation topology. Consequently, a DOC is a necessity after the single-ended TIA for the high speed optical receiver.

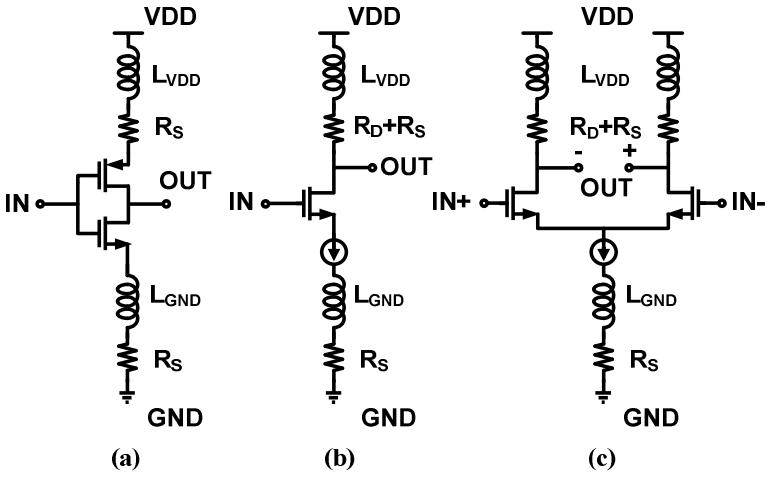


Fig. 3.1. (a) Inverter (b) NMOS amplifier (c) Current mode logic (CML).

A common-mode point is another design issue, even for a differential structure. If the common-mode point has some variance as a result of supply noise, the bounce will deteriorate the performance. Thus, a low-dropout (LDO) regulator is required for supply stability [3.6]. Inevitably, the loading resistors in the CML may introduce large offsets due to the process and temperature variations. This problem and its solutions will be explained in Chapter 4.

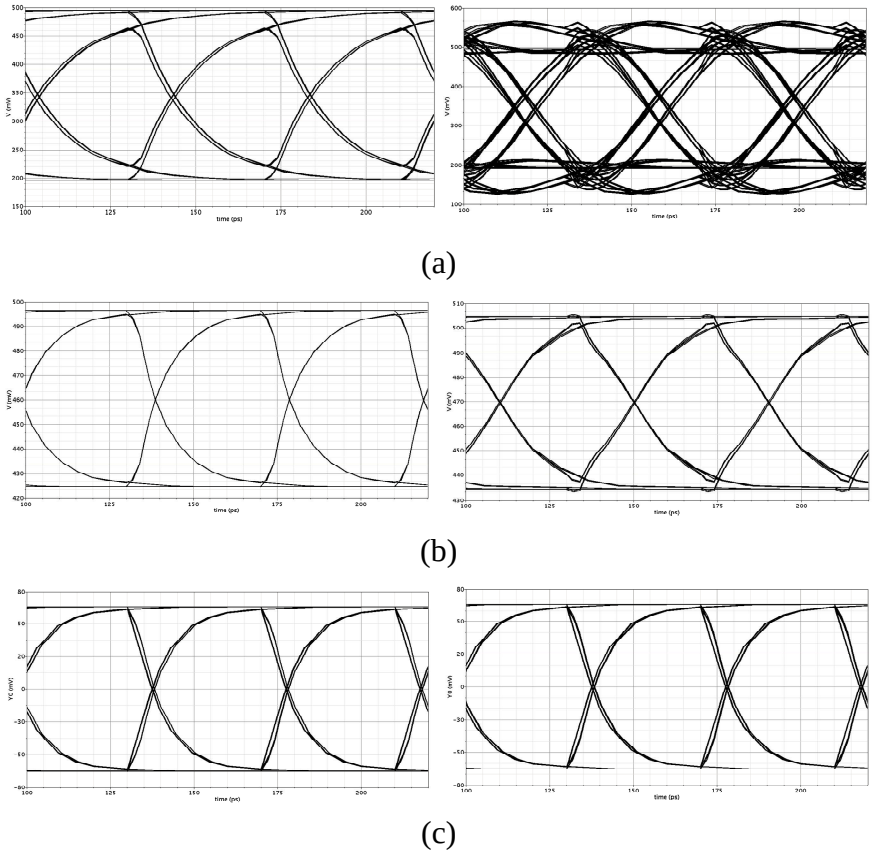


Fig. 3.2. Eye-diagram of (a) inverter wo and wi bonding effect (b) common source wo and wi bonding effect (c) CML wo and wi bonding effect.

3.3 Broad-band design techniques for high-speed amplifiers

Many design techniques are applied to achieve broadband circuits, including inverse scaling [3.7], shunt peaking and series peaking [3.8], T-coil peaking [3.9], negative resistance and capacitance bandwidth enhancement [3.10] and a passive transformer-based amplifier [3.11]. In this design, a shunt inductor is applied to broaden the bandwidth, as shown in Fig 3.3. The transfer function of the amplifier with shunt peaking is given as

$$A(s)=\frac{V_{out}(s)}{V_{in}(s)}=g_m\cdot\frac{s^2R_LLC_P+sL+R_L}{s^3R_LLC_LC_P+s^2L(C_L+C_P)+sR_LC_L+1}, \tag{3.1}$$

where C_L is comprised of the loading capacitance from the next stage and the drain capacitance, while R_L is the equivalent resistance. C_P is the summed capacitance of the loading resistor and inductor. As a CML-based differential amplifier is chosen, the differential inductor is preferred to save area in this design.

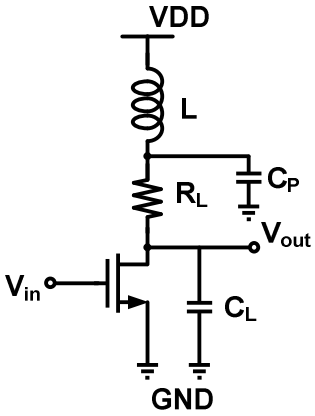
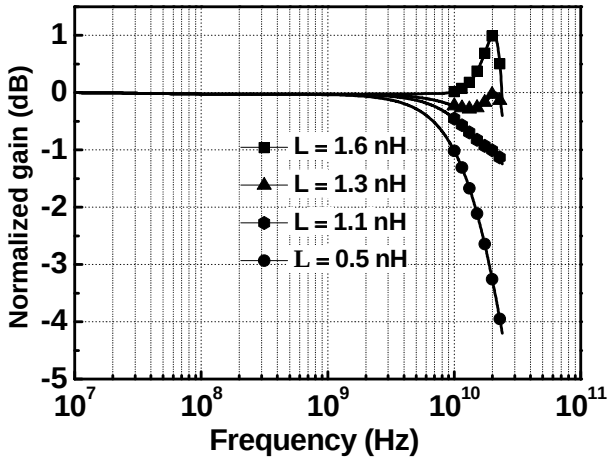
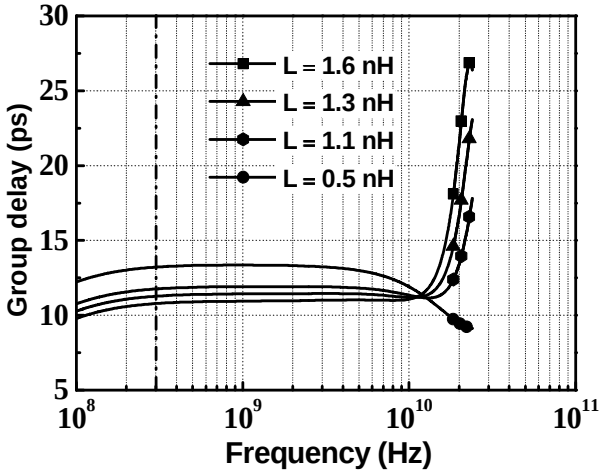


Fig. 3.3. Common source amplifier with shunting peaking inductor.

The peaking inductor value is determined according to the trade-off between the bandwidth and the group delay variation. The inductor has no optimum value, as the $m=R^2C/L$ is determined according to the trade-off between the bandwidth, maximum flatness and group delay variation [3.12], as illustrated in Fig 3.4. For a 2^7-1 data pattern at 25 Gb/s, the group delay below 200 MHz can be neglected. Thus, an inductor value of 1.1nH, with group delay variation below 10ps, is chosen.



(a)



(b)

Fig. 3.4. The simulation results of (a) normalized gain frequency (b) group delay variation.

Besides the shunt peaking, the negative miller capacitor in Fig. 3.5 (b) is also utilized to broaden the bandwidth. The negative miller capacitance C_{m} partially cancels the C_{gd} of M_1 and M_2.

3.4 Modified Cherry-Hooper amplifier and noise analysis

Based on the CML structure, the CMOS Cherry-Hooper amplifier is chosen. A conventional CMOS CH amplifier schematic and block diagram are shown in Fig. 3.5 (a) and Fig. 3.6 (a), respectively. The CH amplifier gain and bandwidth are as below

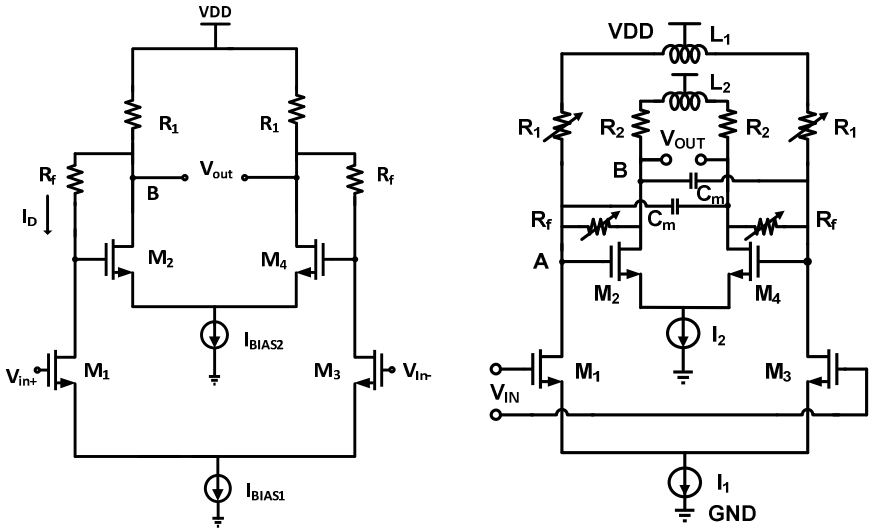
$$Gain = g_{m1}R_f \propto I_{BIAS1} \tag{3.2}$$

$$\omega_{-3dB} = g_{m2} / C_B \propto I_{BIAS2}, \tag{3.3}$$

which show that the gain and bandwidth can be adjusted independently by increasing the tail currents (I_{BIAS1} and I_{BIAS2}) in Fig. 3.5 (a). Both g_{m1} and g_{m2} can be improved to enlarge the gain and BW. However, excessive bias current will cause the output (point B) common-mode voltage to be too low due to IR drop across R_1. The CH gain can also be increased by using a

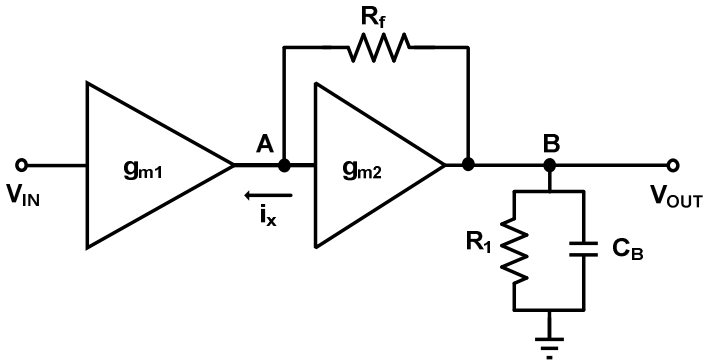
larger R_f. Nevertheless, the maximum value for $I_D R_f$ is limited by the required V_{gs} of M_2 and V_{ds} of M_1.

The modified CMOS CH amplifier, as shown in Fig. 3.5 (b), can alleviate the trade-offs between the gain, bandwidth and headroom limitation by splitting I_{BIAS1} and I_{BIAS2} into two paths with the addition of R_2. The currents can be increased to enlarge g_{m1} and g_{m2} without the sacrifice of common-mode voltage. The current through R_f and the difference between I_{BIAS1} and I_{BIAS2}, makes V_{AB} small. Therefore, R_f can be set to a large value without the limitation of the biasing condition of M_2 and M_1. Fig. 3.6 (b) shows the modified CH amplifier's block diagram.

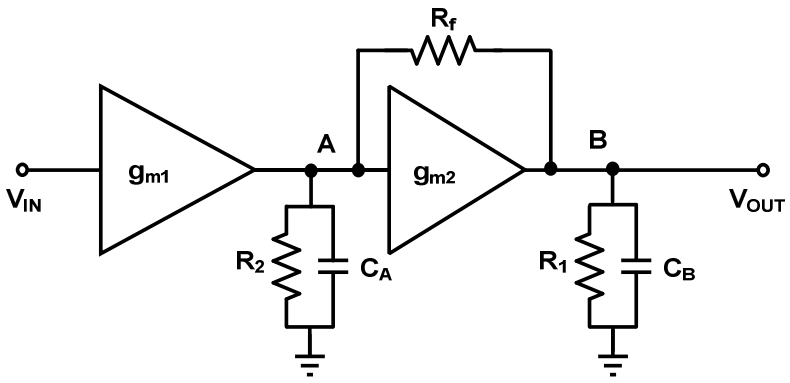


(a) (b)

Fig 3.5. Schematic of (a) the conventional CH amplifier and (b) modified CH amplifier.



(a)



(b)

Fig. 3.6. Simplified block diagram of (a) the conventional CH amplifier and (b) the modified CMOS CH amplifier.

From the simplified equivalent differential circuit in Fig. 3.6 (b), the transfer function is expressed as

$$A(s) = \frac{A_0 \omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2}, \tag{3.4}$$

where

$$A_0 = \frac{g_{m1} g_{m2} R_1 R_2 \left(1 + \dfrac{1}{g_{m2} R_f}\right)}{1 + \dfrac{R_1 + R_2}{R_f} + g_{m2} R_1 R_2 / R_f}, \tag{3.5}$$

$$\xi = \frac{1}{2} \frac{R_2 C_A + R_1 C_B + R_1 R_2 (C_A + C_B)/R_f}{\sqrt{R_1 C_A R_2 C_B (1 + g_{m2} R_1 R_2 / R_f)}}, \tag{3.6}$$

$$\omega_n = \sqrt{\frac{1 + \dfrac{R_1 + R_2}{R_f} + g_{m2} R_1 R_2 / R_f}{R_1 C_A R_2 C_B}}. \tag{3.7}$$

C_A and C_B are the summed capacitance of points *A* and *B*.

Based on the maximally-flat Butterworth response, $\zeta = \frac{\sqrt{2}}{2}$, cell bandwidth $f_{\text{-3dB}} = \omega_n / 4\pi^2$, the GBW is expressed as

$$A_0 f_{-3dB\_BW} = \frac{g_{m1}g_{m2}}{C_A C_B}\frac{1}{f_{-3dB}}\frac{1}{4\pi^2}\left(1+\frac{1}{g_{m2}R_f}\right). \tag{3.8}$$

As the $f_T \approx G_{m1}/2\pi C_1 \approx G_{m2}/2\pi C_2$, (7) can be written as

$$A_0 f_{-3dB\_BW} = \frac{f_T}{f_{-3dB\_BW}}\left(1+\frac{1}{g_{m2}R_f}\right) f_T . \tag{3.9}$$

Z_A and Z_B are the equivalent impedances of points A and B. Compared with the impedance at A and B of the common CML topology, Z_A and Z_B are lower:

$$\frac{1}{Z_A(s)} = g_{m2} - \frac{1}{R_1} + (sC_A - \frac{(g_{m2}R_f+1)sC_B}{sC_B(R_2-R_f)+1}), \tag{3.10}$$

$$\frac{1}{Z_B(s)} = \frac{1}{R_2} + \frac{1}{R_f} + (sC_B + \frac{g_{m2}-\frac{1}{R_f}}{sC_A R_f + \frac{R_f}{R_1}+1}). \tag{3.11}$$

From this result, the GBW is increased beyond the original f_T by $f_T(1+1/g_{m2}R_f)/f_{-3dB\_BW}$ times. The impedance of points A and B is reduced to increase the bandwidth. [3.12] uses active feedback to replace the passive R_f, which achieves a small mismatch and parasitic capacitance, but consumes more power and the headroom is not sufficient for a 1-V supply voltage to achieve high gain and bandwidth in this design.

Although the SNR of the receiver is mostly decided by the TIA, the noise of the limiting amplifier impacts the jitter. The model in Fig. 3.7 is built to gain the total input equivalent noise:

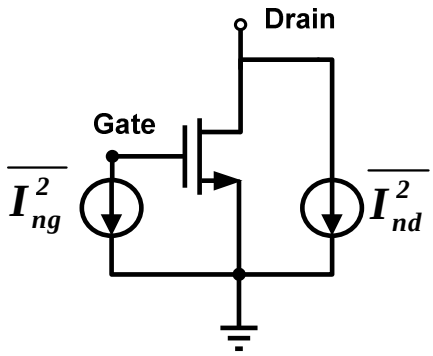


Fig. 3.7. Noise model of van der Ziel.

$$I_{no\_d}^2 = 4kT\gamma g_{ds}\ ,\ I_{no\_g}^2 = 4kT\delta g_g\ , \tag{3.12}$$

where k is the Boltzmann constant, γ is the coefficient of the channel thermal noise and δ is the coefficient of the gate noise. The gate noise is related to the ω as follows:

$$g_g = \frac{\omega^2 C_g^2}{g_{d0}} = \frac{\omega^2 C_g^2}{g_m + g_{mb}}\ , \tag{3.13}$$

where g_{d0} is the drain conductance under zero bias and it almost equals g_m+g_{mb} in a short-channel condition. To better understand the noise distributions, all the mean-square noise voltages are referred to the output first and then the total noise power is referred to the input. The mean-square noise voltages of M_1 and M_2 are derived as

$$\overline{V_{no\_M1,2}^2} = 2\left[\overline{V_{no\_d1}^2} + \overline{V_{no\_g1}^2}\right], \tag{3.14}$$

$$\overline{V_{no\_d1}^2} = \overline{I_{no\_d1}^2} Z_A^2 G_A^2, \tag{3.15}$$

$$\overline{V_{no\_g1}^2} = \overline{I_{no\_g1}^2} Z_{IN}^2 G_O^2 . \tag{3.16}$$

In the same way, the mean-square noise voltages of M_3 and M_4 are also given:

$$\overline{V_{no\_d3}^2} = \overline{I_{no\_d3}^2} Z_B^2 , \tag{3.17}$$

$$\overline{V_{no\_g3}^2} = \overline{I_{no\_g3}^2} Z_A^2 G_A^2 , \tag{3.18}$$

$$\overline{V_{no\_M3,4}^2} = 2\left[\overline{V_{no\_d3}^2} + \overline{V_{no\_g3}^2}\right], \tag{3.19}$$

where Z_A, Z_B and Z_{IN} are the impedances at point A, B and the input. G_A, G_B and G_O are the gain from point A, B and the output to the input, respectively. The noise contribution of the resistors is also considered:

$$\overline{V_{no\_R}^2} = 2 \times 4kT \left(\frac{Z_A^2}{R_A} G_A^2 + \frac{Z_B^2}{R_B} \right), \tag{3.20}$$

where R_A and R_B are the equivalent resistances of point A and B,

$$R_A = \frac{R_F}{1 + g_{m2} R_2} // R_1 \quad , \quad R_B = \frac{R_2}{1 + g_{m2} R_2} . \tag{3.21}$$

The total noise is summed and referred to the input:

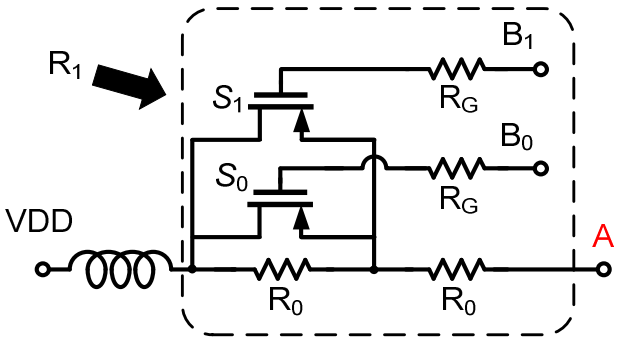
$$\overline{V_{no\_output}^2} = \left[\overline{V_{no\_M1,2}^2} + \overline{V_{no\_M3,4}^2} + \overline{V_{no\_R}^2}\right] \tag{3.22}$$

$$\overline{V_{no\_input}^2} = \frac{\overline{V_{no\_output}^2}}{Z_{LA}^2}. \tag{3.23}$$

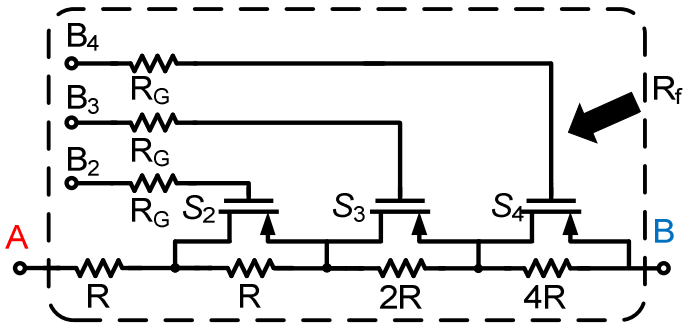
From the equations (3.12) to (3.23), the noise can be reduced by minimizing the impedance of each point. In terms of the receiver system, the noise of the CH amplifier is less important than the gain and bandwidth.

3.5 Digital control variable resistors

Due to the fact that resistive loadings are used in every stage, the offset caused by process, voltage and temperature (PVT) variation may fail the circuit. To relieve this problem, an approach is to apply a digital control scheme to adaptively adjust the loading resistors and feedback resistors to keep the gain and bandwidth stable. Moreover, as discussed in derivation (3.1), since the shunt peaking is subject to the variance of the loading resistor and the paralleled capacitance, the peaking level and flat gain of the amplifier is able to be controlled by the programmable resistor. Therefore, digitally tunable resistors are applied in loading resistors R_1, which serves as fine tuning, and the feedback resistor R_f, which serves as course tuning.



(a)



(b)

Fig. 3.8. (a) Fine tuning R_1 and (b) coarse tuning R_f.

To maintain a large bandwidth sufficiently, the capacitance tolerance of points A and B is around 10 fF. Thus, the size of the switch is limited and has to be set at the minimum length. The higher the number of fingers is, the wider the tunable range achieved, even though the capacitance will become larger. The R_f and R_1 are the inner feedback resistance and loading resistance in one path, as depicted in Fig. 3.5 (b). Because the A and B voltages are close to the VDD, the PMOS transistor is used for a switch. The designs of the fine and coarse tuning switches are proposed in Fig. 3.8 (a) and (b). The series resistance R_G introduces high impedance at the gate and reduces the swatches' capacitance. Compared with the binary-weighted switching [3.13] unit cell, the proposed digital switch saves the transistors and reduce parasitic capacitances although the tuning range is sacrificed. The control bit $B_5B_4B_3B_2B_1$ from 00000 to 11111 assigns 32 logic levels by steering the control switch S_4 to S_0.

The fine and coarse tuning resistor values are shown below:

$$R_{00} = 145.7\,\Omega,\ R_{01} = R_{10} = 154.6\,\Omega, R_{11} = 166.9\,\Omega\ , \tag{3.24}$$

$$\begin{aligned} &R_0 = 727.9\,\Omega \qquad \Delta R = 130.73\,\Omega \\ &R_{000} = R_0 = 727.9\,\Omega \\ &R_{001} = R_0 + \Delta R = 858.63\,\Omega \\ &\cdots\cdots \\ &R_{111} = R_0 + 7\Delta R = 1643\,\Omega \end{aligned} \tag{3.25}$$

The simulation and measurement results will be shown in the next chapter.

3.6 Summary

This chapter reveals that the CML topology has better performance than an inverter cell for high speed amplification. The modified Cherry-Hooper amplifier enlarges the GBW

to extend the bandwidth. Besides this, the topology is suitable for a low supply voltage. A programmable reconfiguration is proposed to relieve the PVT sensitivity, which will be explained in Chapter 4. Thus, the Cherry Hooper amplifier has the potential to be one cell stage for a wideband amplifier.

References:

[3.1] E. M. Cherry and D. E. Hooper, "The Design of Wide-band Transistor Feedback Amplifiers," *Proc. Inst. Elec. Eng.*, vol. 110, pp. 375–389, 1963.

[3.2] C. Holdenried, J. Haslett, and M. Lynch, "Analysis and Design of HBT Cherry-Hooper Amplifiers with Emitter-follower Feedback for Optical Communications," *IEEE J Solid-State Circuits*, vol. 39, pp. 1959–1967, Nov. 2004.

[3.3] M. Kargar and M. Green, "A 10 Gb/s Adaptive Analog Decision Feedback Equalizer for Multimode Fiber Dispersion Compensation in 0.13 ìm CMOS," in *ESSCIRC '10. Proceedings of 2010*, pp. 550 – 553

[3.4] D. Cai, Y. Shang, H. Yu and J. Ren, "Design of Ultra-Low-Power 60-GHz Direct-Conversion Recievers in 65-nm CMOS", *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 9, pp. 3360 – 3372, September 2013.

[3.5] M. Green and U. Singh, "Design of CMOS CML circuits for high-speed broadband communications", *IEEE International Symposium on Circuits and Systems*, pp. 204-207, May 2003.

[3.6] S. Huang, W. Chen, Y. Chang, and Y. Huang, "A 10-Gb/s OEIC with meshed spatially-modulated photo detector in 0.18-μm CMOS technology," *IEEE J. Solid-State Circuit*s, vol. 46, no. 5, pp. 1158–1169, May 2011.

[3.7] E. Sackinger and W. C. Fischer, "A 3-GHz, 32-dB CMOS limiting amplifier for SONET OC-48 receiver," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1884–1888, Dec. 2000.

[3.8] J. Jiang, et al., "100Gb/s Ethernet Chipsets in 65nm CMOS Technology" *ISSCC Dig. Tech. Papers*, pp.120-121, Feb. 2013

[3.9] S. Galal and B. Razavi, "40 Gb/s amplifier and ESD protection circuit in 0.18- μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 39, pp. 2389–2396, Dec. 2004.

[3.10] D. Lee, J. Han, G. Han, and S. M. Park, “An 8.5-Gb/s fully integrated CMOS optoelectronic receiver using slope-detection adaptive equalizer,” *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2861–2873, Dec. 2010.

[3.11] C. Li and S. Palermo, “A Low-Power 26-GHz Transformer-Based Regulated Cascode Sige BiCMOS Transimpedance Amplifier,” *IEEE J. Solid-State Circuits*, vol. 48, pp. 1264 - 1275, May. 2013.

[3.12] S. Galal and B. Razavi, “10 Gb/s Limiting Amplifier and Laser/Modulator Driver in 0.18-μm CMOS Technology,” *IEEE J. Solid-State Circuits*, vol.38, pp. 2138-2146, Dec. 2003

[3.13] H. Nguyen et al., “A binary-weighted switching and reconfiguration based programmable gain amplifier,” *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 56, no. 9, pp. 699–703, Sep. 2009.

CHAPTER 4

An Energy-efficient Programmable Limiting Amplifier

4.1 Introduction

High speed and low power optical communication systems have become highly attractive for short distance LANs due to the proliferation of data in multimedia and data center networks. A designed optical front-end receiver is shown in Fig. 4.1. A transimpedance amplifier (TIA) converts the small photocurrent from the photo detector (PD) into voltage. Next, a DC offset cancellation (DOC) Buffer circuit is required to reduce the DC offset and to convert the single-end signal to differential. Before the equalizer (EQ) compensates for the loss in high frequency from the PD, the main amplifier increases the amplitude of the signal but retains its linearity to protect the TIA from the noise of the EQ. A limiting amplifier (LA) is leveraged to amplify the signal further to meet the input sensitivity requirement of the clock and data recovery (CDR), and then the CDR recovers the signal and clock for further DEMUX processing.

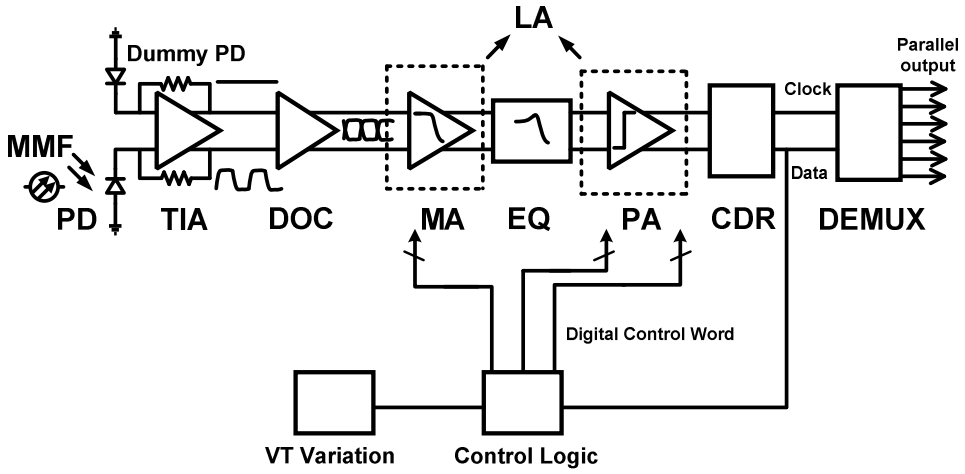


Fig. 4.1. Architecture of the optical receiver with digital control.

Generally, a TIA is designed to have the minimum bandwidth required for the highest input data rate, while its gain is maximized to suppress the noise from subsequent stages. Unfortunately, the gain contributed by the TIA alone is not sufficient to obtain a large output swing to drive the CDR since the achievable unit-gain-bandwidth is limited by the process in use. Furthermore, when the EQ is enabled, it will sacrifice the DC gain for high frequency equalization. As a result, an LA is indispensable to provide enough gain for the whole receiver. At the same time, the bandwidth of the LA should not degrade the system bandwidth, while its power efficiency is supposed to be maximized. This accommodates high gain, large bandwidth and low group delay variation to achieve a large enough swing for the correct operation of the CDR and low inter-symbol interference (ISI) and the jitter for the low bit error rate BER of the system. Besides this, the supply voltage and temperature variation effects on the LA are also critical for a robust operation of the high speed system.

In this chapter, a cascaded architecture with offset cancellation is introduced first. Then, the main amplifier (MA) and post amplifier (PA) implemented in the modified Cherry-Hooper structure, which is described in detail in Chapter 3, are shown in Section 4.2. In Section 4.3, the programmable gain control feature of the presented LA is also included to relieve the temperature and process dependency, as shown in Fig. 4.1. Section 4.4 demonstrates the output buffer design to compensate for the PCB trace loss. Section 4.5 summarizes the experimental results and compares them with published works, and conclusions are given in Section 4.7.

4.2 Cascaded amplifier design and offset cancellation

The total integrated noise is proportional to the bandwidth of the receiver. However, limited bandwidth incurs the effect of ISI [4.1]. Thus, the trade-off between ISI and noise is

determined by the bandwidth. Moreover, the error is a function of the ratio of the bandwidth and data rate.

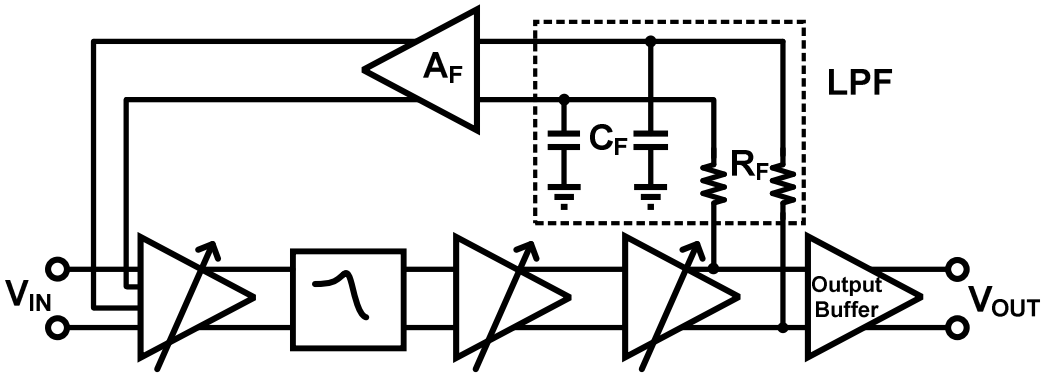


Fig. 4.2. Main amplifier and post amplifier architecture.

The cascaded amplifier with offset feedback loop is depicted in Fig. 4.2. Because the MA and PA share the same topology, the MA in this design is treated as the first stage of the limiting amplifier and the EQ's effect is ignored for simplicity analytically. The PA emphasizes the large bandwidth and limiting function. The first stage amplifier MA is targeted to make the TIA immune from the noise of the EQ, acting as a low noise amplifier (LNA) in the wireless system:

$$NF = 1 + (NF_{MA} - 1) + \frac{NF_{EQ} - 1}{A_{MA}}, \tag{4.1}$$

where the NF represents the noise factor and A_{MA} is the gain of the main amplifier. The total gain A_{tot} and bandwidth BW_{tot} of the n-stages amplifier is given by

$$BW_{tot} = \sqrt[m]{\sqrt[n]{2} - 1}\, BW_0, \tag{4.2}$$

$$A_{tot} = A_0^n, \tag{4.3}$$

where m/2 is the order of the amplifier. A_0 and BW_0 are each cell's gain and bandwidth. The gain bandwidth product for a single cell GBW_0 is derived as

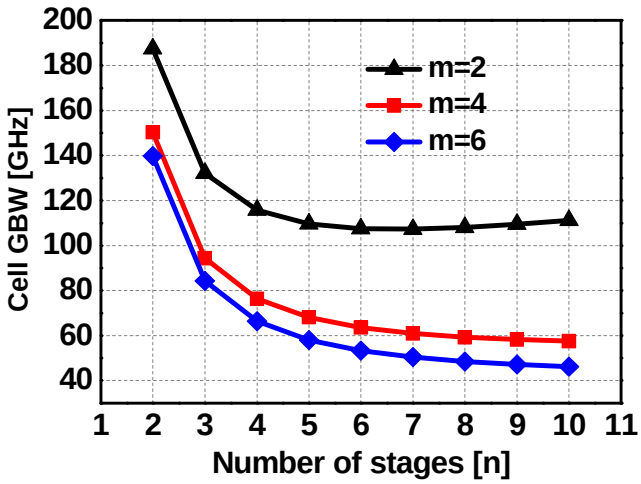


Fig. 4.3. Simulated results of the cascaded amplifiers with different stages.

$$GBW_0 = A_0 BW_0 = \frac{GBW_{tot}}{A_{tot}^{(1-\frac{1}{n})} \cdot \sqrt[m]{2^{1/n}-1}} \cdot \tag{4.4}$$

Based on the system and data rate requirement, the overall gain $A_{tot} = 30$ dB and bandwidth $BW_{tot} = 22$ GHz are needed. For the specifically required overall gain and bandwidth, a trade-off between the value of n, m and the cell gain-bandwidth for each stage exists, as Fig. 4.3 plots. In this design, $m = 4$ and $n = 3$ are selected. Therefore, one cell gain A_0 is 11 dB and cell bandwidth BW_0 is 29.4 GHz. The cell amplifier is made up of the Cherry Hooper topology described in Chapter 3.

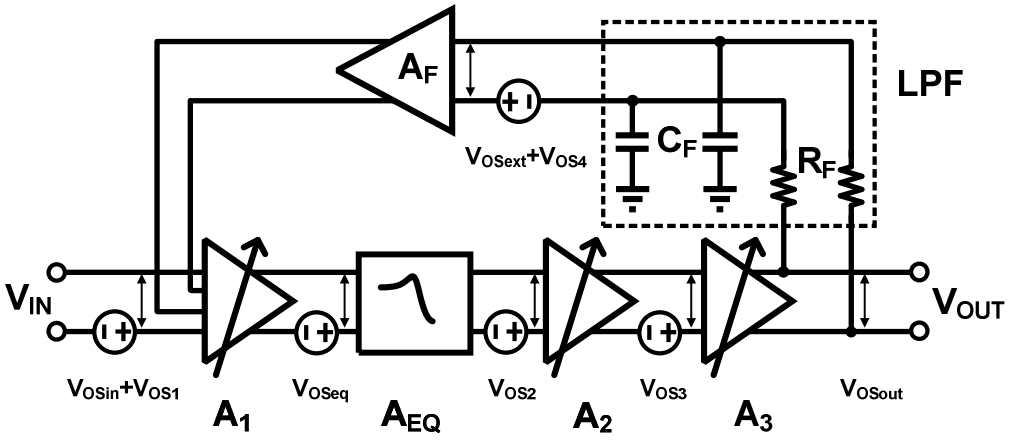


Fig. 4.4. Limiting amplifier and equalizer with offset calculation estimation.

DC offset is another important issue since the signal from the off-chip photodetector is single-ended, while the on-chip signal path is differential. Even with a DOC circuit following

the front-end TIA, the input signal to the limiting amplifier is not perfectly differential. Thus, the LA is supposed to reject or suppress the remaining offset. Otherwise, the offset can cause incorrect saturation at the LA output due to its large voltage gain and limiting function. Furthermore, the offset also enlarges the signal jitters by shifting the common mode point of the differential pairs in the LA. In general, any signal distortion at the LA output will degrade the decision threshold and accuracy of the CDR circuit.

There are two commonly-used ways to cancel the offset. The first one is AC coupling, which is simple and effective, but its parasitic capacitance reduces the bandwidth dramatically and occupies a large area. The other way is a feedback cancellation network, incorporating an amplifier A_F and a low pass filter (LPF), as demonstrated in Fig. 4.4. The feedback loop eliminates the input-referred offset of the following blocks by adjusting the biasing current of the input differential pair of the MA. Assuming that V_{OSin} is the offset from the DOC's imperfect differential output and V_{OSext} is from the off-chip components, V_{OSi} is the offset from each amplifier stage. The output offset voltage V_{OSout} is derived as below:

$$\begin{aligned} V_{OSout} &= (V_{OS1} + V_{OSin}) A_1 A_2 A_3 + (V_{OSeq} A_{EQ} + V_{OS2}) A_2 A_3 + V_{OS3} A_3 \\ &\quad + V_{OSext} + V_{OS4} - (V_{OSext} + V_{OS4}) A_1 A_2 A_3 A_{EQ} A_F \\ &= V_{OSout0} - V_{OSext} A_1 A_2 A_3 A_{EQ} A_F \end{aligned} , \qquad (4.5)$$

where A_1, A_2, A_3, A_F and A_{EQ} are the corresponding flat gains of the main amplifier, post two amplifiers, feedback amplifiers and equalizer. V_{OSout0} is the offset at the output point of the LA without the offset cancellation loop, and as the derivation in (4.5) shows, the DC offset can be greatly reduced.

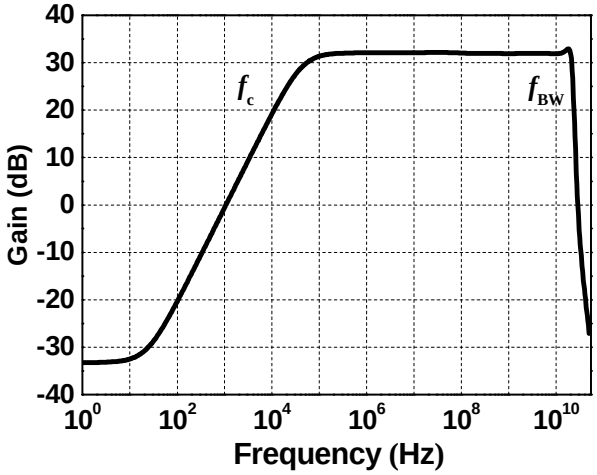


Fig. 4.5. Limiting amplifier frequency response with offset cancellation.

As the feedback loop is utilized, the low cut-off frequency f_c of the high-pass filter in Fig. 4.5 is introduced:

$$f_c = \frac{A_1 A_{EQ} A_2 A_3 A_F + 1}{2\pi C_F R_F}, \tag{4.6}$$

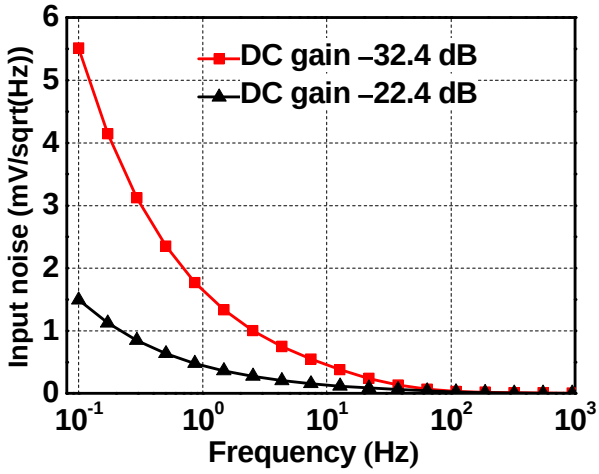
where C_F and R_F form the low pass filter (LPF) in the feedback loop.

To prevent the deterioration of the data eye-opening in the presence of a long bit sequence of consecutive "0's" or "1's", fc should be made as low as possible. Typically, fc is set at 3 kHz to make the VDD droop below 0.2 dB for a 25-Gb/s 2^{15}-1 PRBS data pattern [4.1]. An 8B/10B code can be applied in the data to alleviate the problem brought by consecutive identical data.

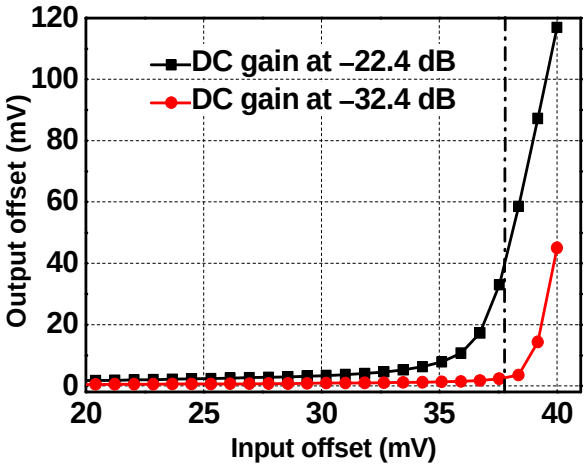
However, the offset cancellation loop degrades the low-frequency gain and introduces additional noise. Furthermore, a low f_c scarifies the offset cancellation range [4.2]. In other words, as the DC gain of the closed loop system is lowered, the offset cancellation range is enhanced, but the input-referred noise is increased. This in turn scarifies the input sensitivity. For example, with f_c = 43.17 kHz and DC gain at −32.4 dB, the input-referred integrated noise is 4.97 mV. But if the DC gain is increased by 10 dB to −22.4 dB and f_c remains the same, the input-referred integrated noise is reduced by about 3 times, to 1.59 mV. At the same time, the offset cancellation range is reduced, as shown in Fig. 4.6 (a). For the case with lower DC gain,

at −32.4 dB, the output offset is maintained at below 5 mV by the cancellation loop for input offset up to 37 mV. However, for the offset loop with higher DC gain, at −22.4 dB, when the input offset is over 35 mV, the output offset grows rapidly. For input offset at or above 37 mV, as marked by the dotted line in Fig. 4.6 (b), the output offset becomes larger than the input offset, which will lead to erroneous output. In conclusion, if the DC gain is low enough, the offset cancellation range becomes larger, but the input referred noise is worse and scarifies the input sensitivity. Based on this trade-off, f_c at 15 kHz is chosen for the system. In this work, an off-chip capacitor C_F and on-chip R_F are adopted to minimize the f_c for the low pass filter in Fig. 4.4.

Moreover, a lower f_c means a longer amplifier's settling time, which is a key feature for the MUX, where the receiver is switched between multi-channels in burst mode application [4.3].



(a)



(b)

Fig. 4.6. (a) Input equivalent noise (b) offset cancellation range.

4.3 PVT variation and digital control recovery

Due to the resistive loadings in use in every stage, the offset caused by the PVT variation may fail the circuit. From −10ºC to 70ºC, the resistance is varied by ± 8%. The simulated gain and bandwidth variations under different process corners and temperatures are shown in Fig. 4.7.

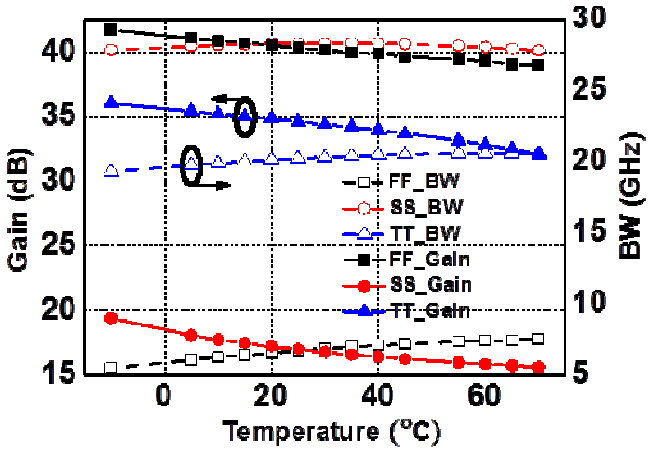


Fig. 4.7. Simulated temperature and process variation effect on the limiting amplifier.

The gain and bandwidth are susceptible to the process and temperature change. The solid line represents the simulated gain, while the dashed line represents the simulated bandwidth. As the simulation results demonstrate, the LA's performance is very sensitive to the process variation. The effect on the bandwidth caused by the temperature variation can contribute to large jitters for the whole system. To relieve the PVT sensitivity, an automatic constant gain bias circuit regulates the current source to control the swing [4.4]. However, this costs much power consumption and area. Another approach is to apply a digital control scheme to adaptively adjust the loading resistors and feedback resistors to keep the gain and bandwidth stable. Moreover, a tunable amplifier holds for the different off-chip PDs' responsivity and bandwidth.

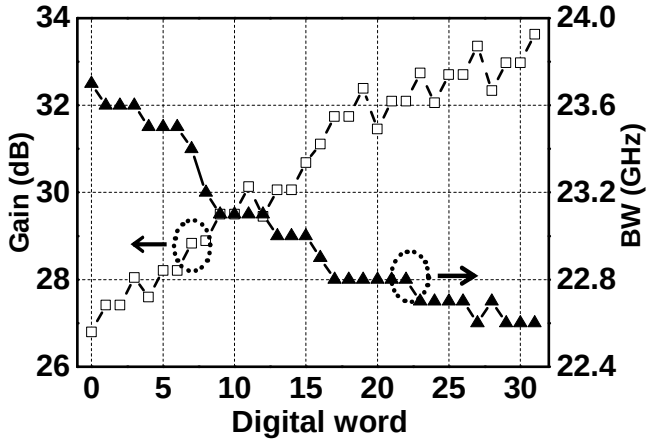


Fig. 4.8. Gain and bandwidth with different control words.

To provide a precise gain and bandwidth for the system, a programmable gain amplifier (PGA) is designed with a flat gain tuning range ± 5 dB and gain step below ± 0.8 dB. The simulation results show that the variable range covers the 7.6 dB where control bit $B_5B_4B_3B_2B_1$ from 00000 to 11111 assigns 32 logic levels by steering the control switch S_0 to S_4. The minimum gap between two adjacent control bits is below 0.8 dB, as shown in Fig. 4.8. The bandwidth is over 22 GHz with all control bits.

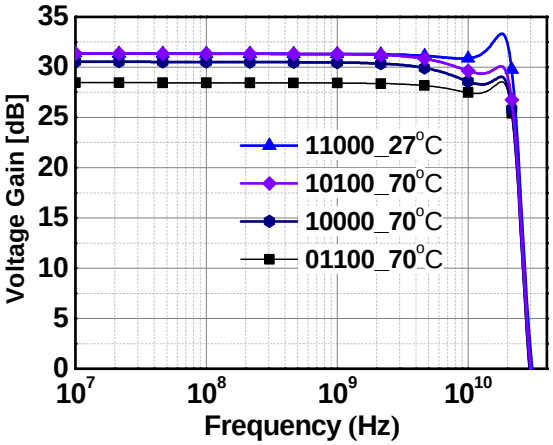


Fig. 4.9. Measured gain tuning range with different control words at 27 ºC and 70ºC.

To prove the functionality of the digital tuning, a simulation results under different temperatures are shown in Fig 4.9. All the resistor values are obtained under a TT corner at

27ºC. If the temperature is set to 70ºC, the bandwidth and gain are recovered by digital control.

4.4 Output buffer design

The schematic of the output buffer design is shown in Fig. 4.10. The output buffer accommodates the requirements to drive a one inch PCB trace. The PCB trace will introduce around a 3-dB loss at the Nyquist frequency. Therefore, an equalizer is built in to compensate for the loss. The signal after the LA becomes a large signal and the requirement for the output buffer is to not degrade the speed of the signal and to drive the PCB trace with the equipment at 50 ohm. The output buffer consists of one buffer stage for the LA's loading and a second stage with a large current to drive the PCB trace. Besides this, the built-in equalizer and tunable resistor compensate for the PVT variations to maintain a broadband 50-ohm matching.

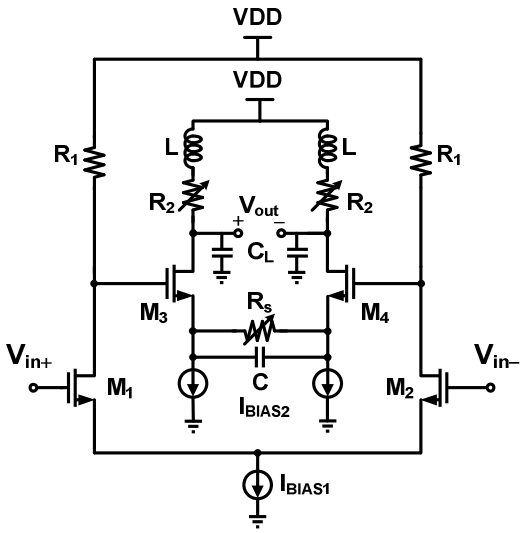


Fig. 4.10. Output buffer schematic.

The input at the buffer is not a small signal any more, so the analysis should follow the large signal design. The maximum single-ended output is limited to the drop voltage on the resistor:

$$V_{swing} = I_{BIAS2} R_2 . \tag{4.7}$$

The minimum input of the operation at saturation mode has the transistor fully switched and the swing is derived as

$$V_{\min} = \sqrt{\frac{2I_{BIAS2}}{\mu_n C_{ox}\frac{W}{L}}}. \tag{4.8}$$

At this point, the equivalent small signal gain is given as

$$A_v = R\sqrt{\mu_n C_{ox}\frac{W}{L}I_{BIAS2}} \tag{4.9}$$

$$\frac{V_{swing}}{V_{\min}} = \frac{A_v}{\sqrt{2}}. \tag{4.10}$$

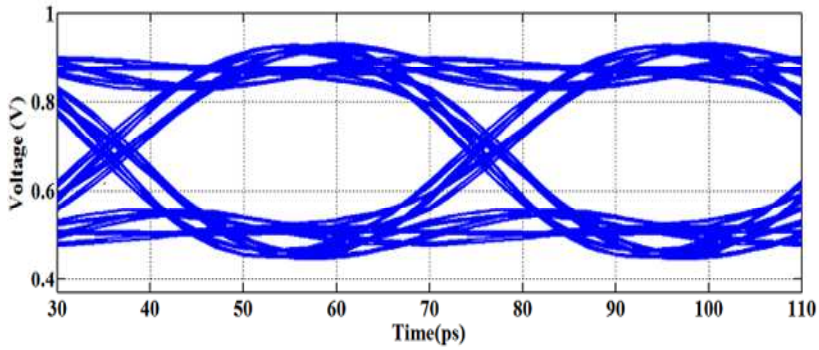
To minimize the time constant τ and maintain a large swing, the V_{min} is supposed to be large, while the transistor size remains small, which means the differential pair needs a high transistor current density. For example, to make sure the transistors are fully switched, the output swing should be larger than the minimum input, which means A_V is above 2. If the R_2 is increased by a factor of X, while the I_{BIAS2} remains unchanged, the W of the transistor is decreased by X^2 and still remains fully switched. Subsequently, the loading capacitance is decreased by X, and the speed of the circuit is increased. Thus, the current density of the transistor is to be set as high as possible, based on the bias condition. The sizes of the components in the output buffer are characterized in Table 4.1.

Table 4.1. Parameters of the output buffer

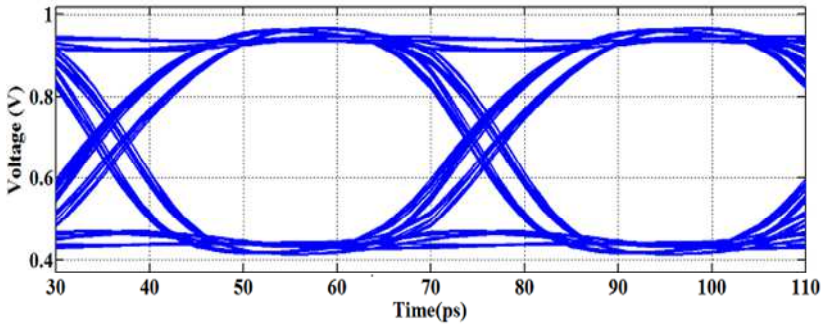
$M_{1,2}$	24 μm/60 nm
$M_{3,4}$	36 μm/60 nm
V_{DD}	1.2 V
I_{BIAS1}	10 mA
I_{BIAS2}	10 mA
R_1	85 ohm

The simulated eye-diagram with different input signal levels is shown in Fig. 4.11. With different inputs, the output swings remain almost the same, a single-ended output around 500 mV_{pp}, which shows that the signal is limited at the buffer output. The jitter becomes better with increasing input amplitude. On one hand, the signal to noise ratio (SNR) becomes better, and as discussed above, a large SNR (larger than 7) indicates a better BER.

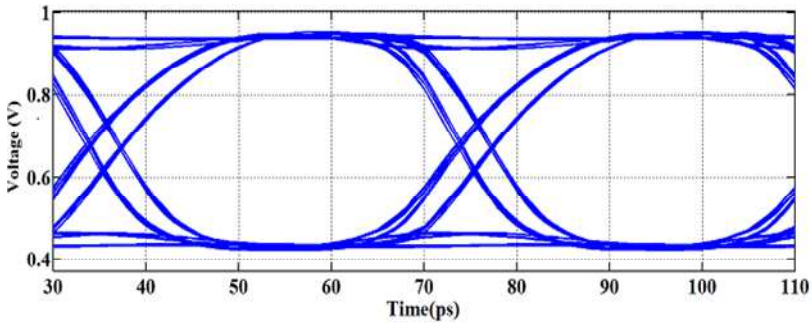
On the other hand, as the degree of the limiting is increased, the high and low level of the signal droop is improved.



(a)



(b)



(c)

Fig. 4.11. Post layout simulation with input (a) 12 mV_{pp} (b) 36 mV_{pp} (c) 100 mV_{pp} with 25 Gb/s 2^{15}–1 PRBS.

4.5 Measurement results of the limiting amplifier

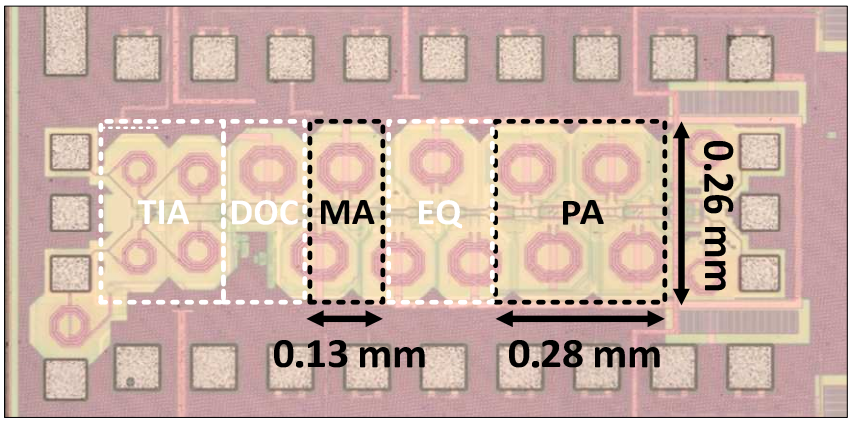


Fig. 4.12. LA's microphotograph.

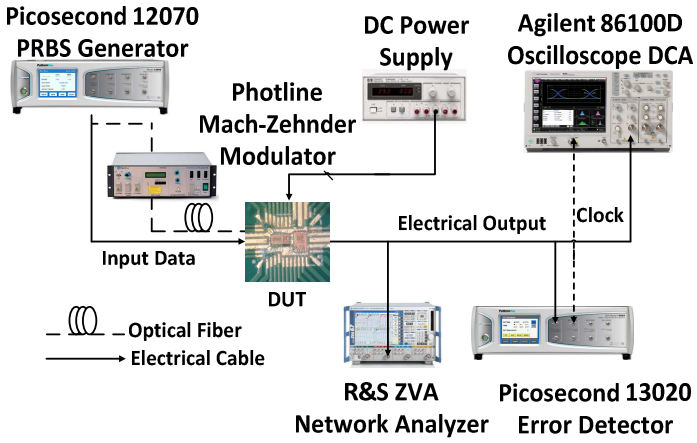


Fig. 4.13. Receiver's measurement testing setup.

The limiting amplifier is tested with the PD, TIA and EQ in both electrical and optical measurement. Implemented in 65-nm CMOS, the LA occupies about 0.12 mm^2, as shown in Fig. 4.12. In this design, the RC low pass filter comprises the on-chip 1M-ohm R_F and off-chip 68-nF C_F. Fig. 4.13 shows the overall measurement setup. The optical signal is generated by an 850-nm laser source with Mach-Zehnder modulator and it is focused by a lensed fiber for top illumination on the PD, which is wire-bonded to the TIA input on a chip-on-board module. The trans-impedance gain of the system is tuned by programmable control words, as shown in Fig. 4.14. The measured tunable range is 10.6 dB, larger than the simulated results due to the process variation of the resistor, while the maximum gap is below 1 dB, which is close to the simulation results. The curve in Fig. 4.15 shows the measured BER as a function of the light input power at 25 Gb/s. The sensitivity at a BER of 10^{-12} is around –7.3 dBm. The

resulting bathtub curve at 25 Gb/s is shown in Fig 4.16, which is verified with a 2^{15}–1 input pattern.

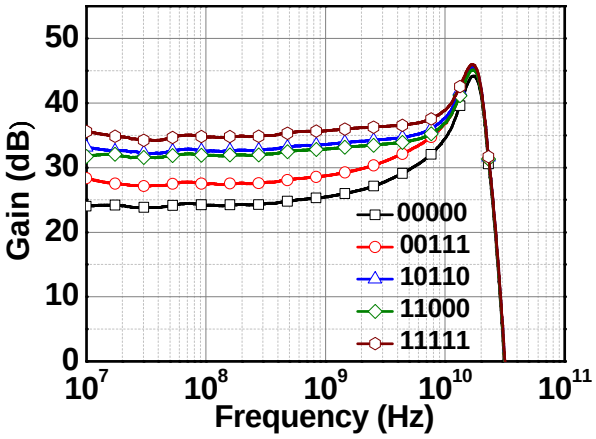


Fig. 4.14. The frequency response with the programmable control bit.

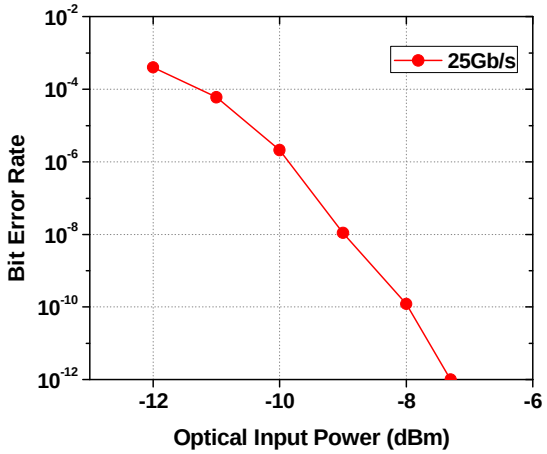


Fig. 4.15. BER performance of the Rx with different input powers.

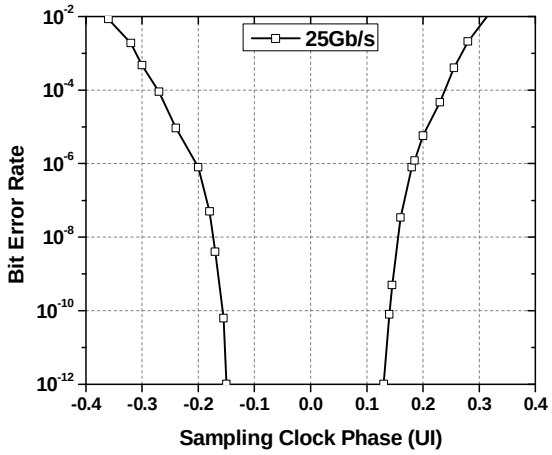
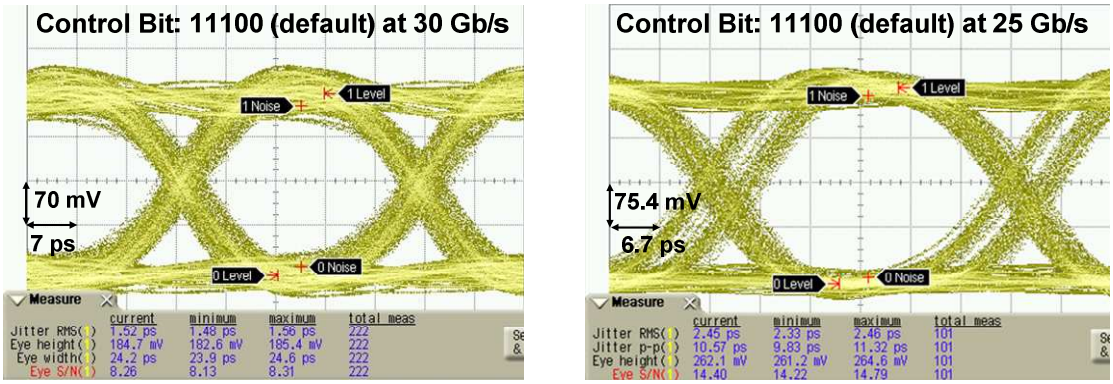
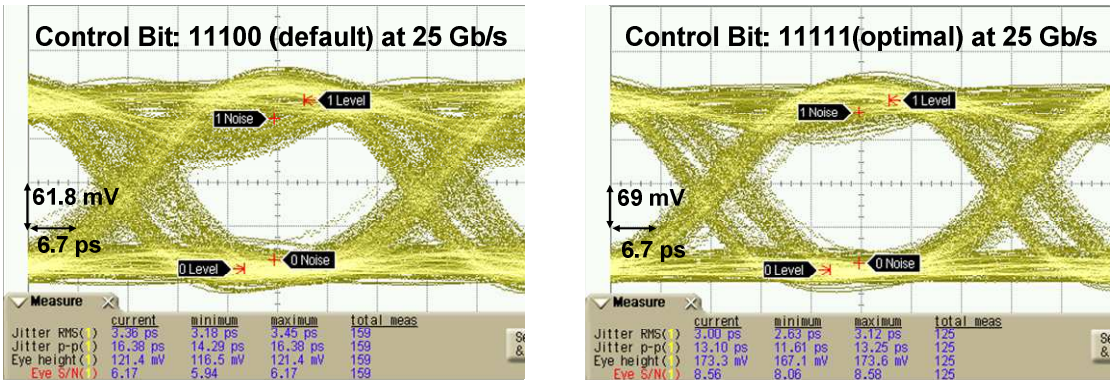


Fig. 4.16. The bathtub curve of the output at 25 Gb/s 2^{15}–1 PRBS data pattern.



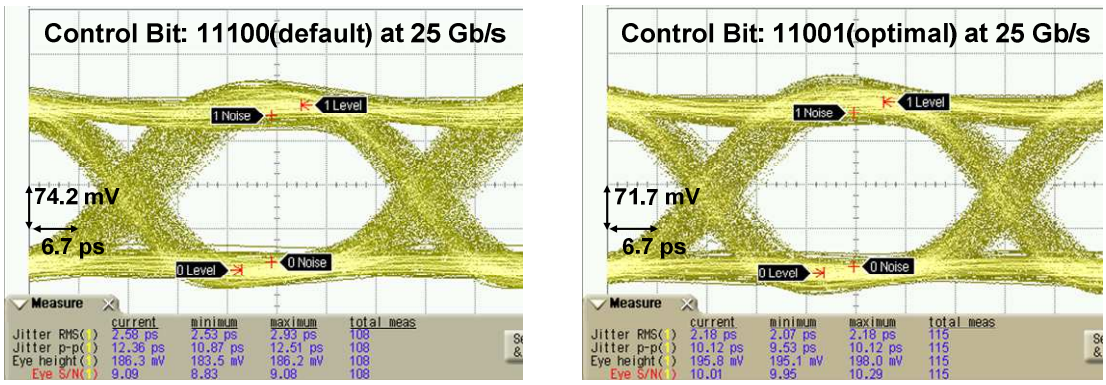
(a) (b)

Fig. 4. 17. The measured eye-diagram of (a) 30-Gb/s electrical input (b) 25-Gb/s optical input



(a) (b)

Fig. 4.18. Compensation for supply variation under V_{DD} = 0.9 V.



(a) (b)

Fig. 4.19. Compensation for temperature variation at 80ºC.

The LA is tested both on a wafer-probing for electrical measurement and a board for optical measurement. Fig. 4.17 shows the receiver's measured eye-diagrams under a 30-Gb/s

electrical and 25-Gb/s optical test with 2^{15}–1 PRBS input. The measured electrical and optical RMS jitters are 1.52 ps and 2.45 ps, respectively.

Table 4.2. Summary of the digital tuning scheme for compensating for VT variations.

Meas. Data Eye	Fig. 4.17(b)	Fig. 4.18(a)	Fig. 4.18(b)	Fig. 4.19(a)	Fig. 4.19(b)
Control bit	11100 (Default)	11100 (Default)	11111 (Optimal)	11100 (Default)	11001 (Optimal)
V_{DD} Supply (V)	1	0.9	0.9	1	1
Temp. (ºC)	27	27	27	80	80
SNR (Linear)	11.5	6.17	8.56	8.9	10
RMS Jitter (ps)	2.45	3.36	3.00	2.58	2.18
Output (mV)	278	277	310	345	337

When the supply voltage drops from 1.0 V to 0.9 V, the RMS jitter is degraded from 2.45 to 3.36 ps (37%), with the default control setting 11100. By changing the control word to 11111, the measured RMS jitter is improved to 3 ps and the degradation is reduced from 37% to 22%, as shown in Fig. 4.18. Fig. 4.19 shows that at 80ºC, the data eye SNR and RMS jitter can be improved by 12% and 16%, respectively, with the optimal digital control (11001). To maintain a BER below 10^{-12}, the SNR needs to be above 6.8 (or 8.3 dB) based on our measurements. Fig. 12 plots the measured SNR versus digital control words, with the markers showing the settings that can meet this requirement. It is observed that the optimal setting at 27ºC under 1-V V_{DD} is 11101, which is close to the default setting. At 80ºC, the optimal setting is 11001.

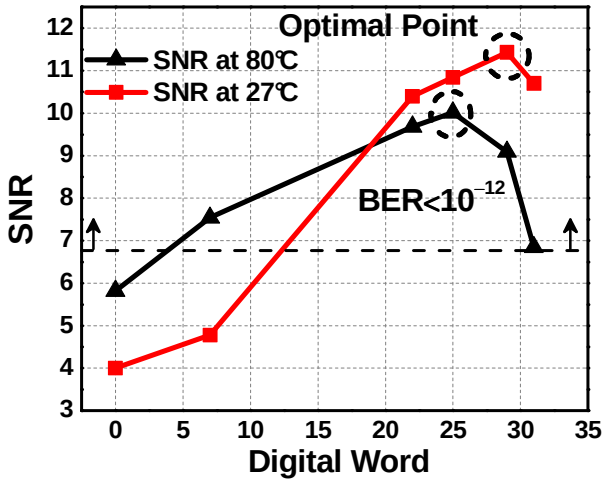


Fig. 4.20. Measured SNR versus digital control settings from 00000 (0) to 11111 (31) at 27ºC and 80ºC under 1-V V_{DD}.

Table 4.2 summarizes the function of the programmable configuration under different temperatures and supply voltages. The programmability by digital tuning improves the system performance in terms of jitter and SNR. If the supply voltage and temperature can be detected, the corresponding digital word will be assigned to the LA to achieve the optimal point manually, as demonstrated in Fig. 4.1. Table 4.3 summarizes the measured performances of the LA and compares them to other works.

Table 4.3. Comparison of recently published LAs.

Ref.	Process	Bit Rate (Gb/s)	Gain (dB)	BW (GHz)	Supply (V)	Power (mW)	Area (mm^2)
[4.5]	0.25μm BiCMOS	40	53 dBΩ	26	2.5	8.2	0.75
[4.6]	65nm CMOS	28	22.6 (simulated)	24.3 (simulated)	1.0	38.4	NA
[4.7]	90nm CMOS	NA	19	44	1.0	57	0.02
[4.8]	0.13μm CMOS	35	38	26.2	1.5	125	0.65
[4.9]	65nm CMOS	40	31.5	NA	1.2	44	NA
[4.10]	90nm CMOS	40	20	NA	1.0	80	0.033
This work	65nm CMOS	30	31.3	22.07	1.0	24.3	0.12

4.6 Summary

A power-efficient high-speed limiting amplifier is presented. With digital programmability, the LA is able compensate for the performance degradation due to PVT variations. Compared with previous results, the presented LA achieves high speed and gain at

relatively low power consumption, which makes it suitable for integration in low-power high-speed optical receivers.

From the simulation and measurement results, Equalization in the NRZ modulation is a feasible technique to meet the need for high speed serial links without complicated coding, modulation schemes and error correction.

References:

[4.1] B. Razavi, *Design of Integrated Circuits for Optical Communications*. New York: McGraw-Hill, 2003.

[4.2] Z. Hou, Y. Wang, Q. Pan and C. P. Yue, "A 25-Gb/s 32.1-dB CMOS Limiting Amplifier for Integrated Optical Receivers" in *Proceedings of IEEE International Conference on ASIC*, 2013

[4.3] E. Crain and M. Perrot, "A 3.125 Gb/s limit amplifier in CMOS with 42 dB gain and 1 us offset compensation," *IEEE J. Solid-State Circuits*, vol. 41, no. 2, pp. 443–451, Feb. 2006.

[4.4] K Wu et al, "A 2 x 25Gb/s receiver with 2:5 DMUX for 100Gb/s Ethernet" *IEEE Journal of Solid-State Circuits*, vol. 45, pp. 2421-2432, Nov. 2010.

[4.5] C. Li and S. Palermo. "A Low-Power 26-GHz Transformer-Based Regulated Cascode SiGe BiCMOS Transimpedance Amplifier," *IEEE J. Solid-State Circuits*, vol. 48, pp. 1264 - 1275, May. 2013.

[4.6] T. Takemoto et al., "A compact 4 25-Gb/s 3.0 mW/Gb/s CMOS-based optical receiver for board-to-board interconnects," *IEEE J. Solid-State Circuits*, vol. 28, pp. 3343–3350, Dec. 2010.

[4.7] J. Weiss et al., "A DC to 44-GHz, 19-dB gain amplifier in 90-nm CMOS using capacitive bandwidth enhancement," *Proc. IEEE ISSCC*, 2006, pp. 514-515.

[4.8] C.-H. Lee and S.-I. Liu, "A 35-Gb/s limiting amplifier in 0.13-um CMOS technology", *Symp. VLSI Circuits Dig. Tech. Papers*, pp. 152–153, Jun. 2006.

[4.9] J. Jiang , et al., "100Gb/s Ethernet Chipsets in 65nm CMOS Technology " *ISSCC Dig. Tech. Papers*, pp.120-121, Feb. 2013.

[4.10] J. R. M. Weiss, M. L. Schmatz, and H. Jaeckel, “A 40 Gb/s, digitally programmable peaking limiting amplifier with 20-dB differential gain in 90 nm CMOS,” in *Proc. IEEE RFIC Symp.*, 2006.

CHAPTER 5

Conclusions and Future Work

Integrated optical receiver systems with data rates up to 25 Gb/s are becoming more attractive for short-range communication. In this thesis, the primary goal is to implement a high-speed, power-efficient and robust limiting amplifier in a 25 Gb/s optical receiver for 100GbE communication.

First, CMOS photodetectors (PDs) are characterized and analyzed. Totally, there are seven types of photodetectors designed and verified. The differential deep nwell/p-substrate photodiode has a bandwidth of 120 MHz and responsivity of 0.04 A/W. Although the CMOS PDs suffer from low responsivity and narrow bandwidth, the simulation results show that, by proper equalization in the receiver, they can achieve a 14 Gb/s data communication rate. The complete integration of the CMOS PD and receiver saves the cost and the parasitic capacitance and inductance from the bonding inductor.

Second, a modified Cherry Hooper amplifier, which alleviates the headroom issue, is designed for the cell of the limiting amplifier in the optical receiver. Shunting peaking inductors and negative capacitance are also employed in the amplifier. According to the simulation results, the CH amplifier is suitable for high speed operation under low voltage supply.

Finally, PVT variations affect an LA's robust high speed operation, and the gain and bandwidth are subject to the PVT variations. To overcome this problem, with low power consumption, a digital tuning scheme is proposed to compensate for these effects. The measurement results show that the LA has an advantage in power consumption and robust operation over the voltage and temperature variations in a 25 Gb/s optical receiver system.

It is worth pointing out that inthe measurement, it is found that the bonding inductors, especially the bonding inductor from the off-chip photodetector to the input pad, have a negative effect on the performance of the high speed circuits. To overcome the variance of the bonding inductor, the receiver has to sacrifice performance. Thus, in the future, if the bonding technique could be improved, which means that accurate and small bonding wire is offered, the overall design would improve. Otherwise, flip-chip mounting would be a better choice.

The future work of this thesis can be divided into three parts. The first part is the further improvement of the power efficiency of the receiver by operating at a lower supply voltage. The second is that the DFE and FFE will be implemented and compared with the continuous linear equalizer. And the final part is that the CDR and DEMUX will be integrated with the front-end receiver operated at 25 Gb/s, or at an even higher data rate.