A Mixed-mode Co-simulation Platform for Millimeter-Wave Broadband Receiver IC Design

by

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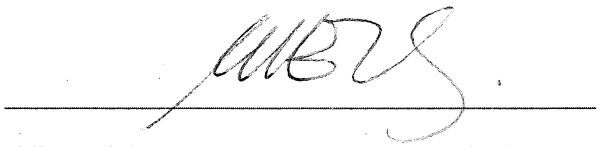

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10 June 2020

To my parents

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Abstract

As the overwhelming demand for the wireless mobile data traffic continues to grow dramatically, multiple mm-wave frequency bands have been specified and investigated for 5G mobile networks to deliver ultra-high-speed wireless backhaul connectivity [1]. The 24.25-29.5 GHz and 37-43.5 GHz bands are the most promising ones for 5G early deployments. For instance, mainland China and Japan have selected 24.75-27.5 GHz and 27.5-29.5 GHz, respectively, for licensed use [2]. Highly integrated mm-wave transceiver systems have been actively studied and investigated to support multi-Gb/s data rate in wireless communication. This thesis also focuses on the design of a mm-wave transceiver for 5G communication.

In the first part of this work, we present a co-simulation platform to link the base-band digital signals and the RF front-end to evaluate the performance of circuit blocks in transceiver systems. M-QAM OFDM modulation scheme is implemented for BER and constellation check. This platform is based on the MATLAB, ADS, Cadence, and EMX, and it supports the mm-wave receiver IC design from system specifications to circuit implementations. In the second part, we propose a mm-wave direct conversion receiver

front-end, with a focus on developing an LNA in the 24-32 GHz to meet the gain, noise figure, linearity, bandwidth, and area requirements, simultaneously. A novel compact three-coil transformer is employed to perform single-ended to differential conversion, broadband input matching, gm-boosting, and noise suppression at the LNA input. The proposed LNA is further integrated with an IQ mixer, a VGA, and output buffers to build a broadband receiver front-end. In the last part, we evaluate the circuit performance in the co-simulation platform. The proposed receiver front-end features a 3-dB bandwidth of 7.5 GHz, centered at 27.5 GHz. The simulated noise figure is below 5 dB. With 1 GHz signal bandwidth and 16-QAM modulation scheme, it achieves a 3.76 Gb/s data rate, a 3.8% EVM, and a BER of less than 10-6. This co-simulation platform can be further implemented to support varieties of transceiver IC design. Such as, power amplifiers, antennas, and other circuit bloc

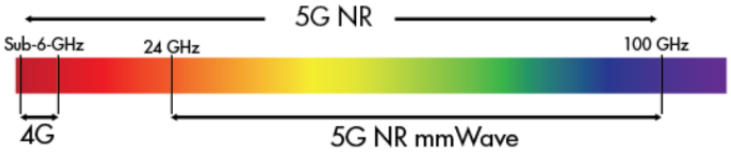
Contents

Chapter 1

Introduction

In this chapter, a brief introduction to the millimeter wave (mm-wave) band is given and its potential applications are demonstrated. The higher order quadrature amplitude modulation (QAM) and receiver design specifications for high data rate 5G communication system will be covered.

With the development of mobile communications, the demand for wireless data transmission rate is also increasing. One of the big challenges from the 1st to 5th generation of wireless communication systems is using limited bandwidth in the frequency range to support ultra-high-speed wireless communication. Multiple mm-wave bands have been proposed and evaluated for 5G mobile networks for early deployments, since the spectrum resources in the lower frequency bands is limited [3]. The frequency range of 30-300GHz with the corresponding wavelength of 0.1-10mm is called the mm-wave band. The abundant spectrum available at mm-wave frequency bands can deliver extreme data speeds and capacity. With hundreds of megahertz of wireless transmission bandwidth available at center frequencies allocates in mm-wave band, such as, 24, 28, and 38GHz, extremely low latency and high data rate could be reached. So, development of mm-wave communication systems for 5G becomes the hot topic for researchers. However, transmissions at mm-wave bands suffer from path loss and susceptibility to blockage. In addition, power constraints and high cost of base stations are also challenging parts. [4] Fig. 1- 1 shows the 5G frequency spectrum and the frequency bands for early deployment of 5G mm-wave systems.



(a)

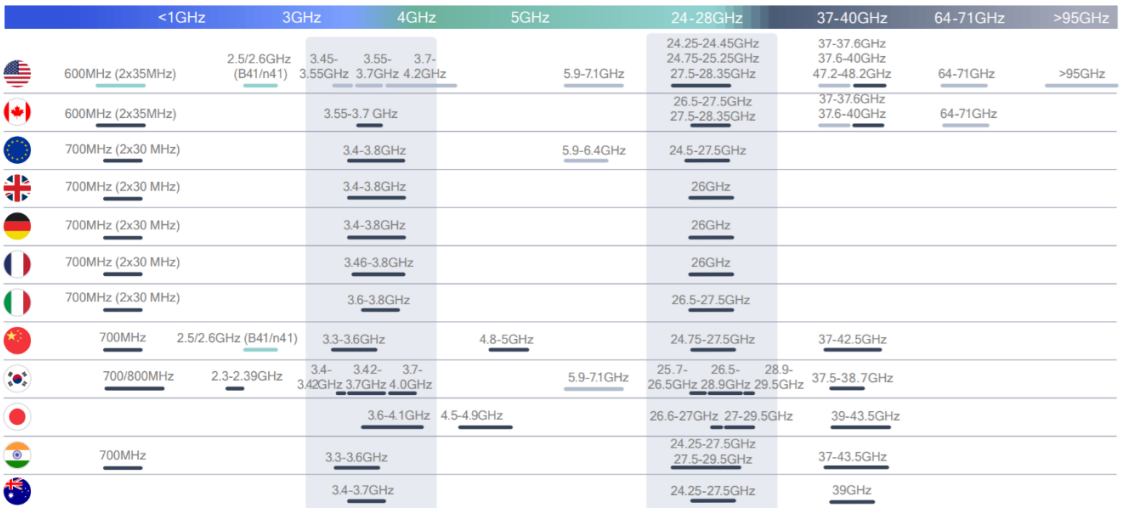


Fig. 1- 1 (a) The 5G frequency spectrum (b) Frequency bands for early deployment of 5G mm-wave systems [4]

There are many applications at mm-wave band, such as high-speed wireless communications, mm-wave imaging for security system, and mm-wave radar for automotive [5-8]. Some of the usage scenarios for 5G are shown in Fig. 1- 2. The Mobile Broadband (MBB) service and Internet of Things (IoT) will be the two main drivers in the future mobile network development. The overall vision is depicted in Fig. 1- 3.

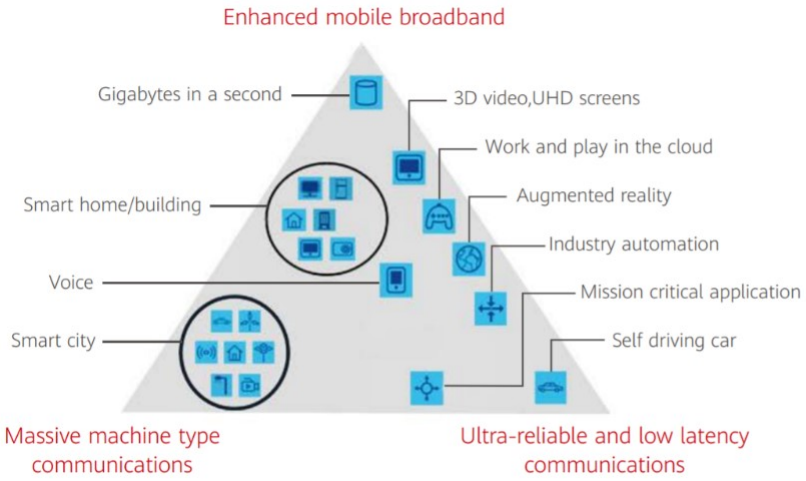


Fig. 1- 2 5G usage scenarios [3]

Fig. 1- 3 Overall vision of 5G [9]

Today, because of the advancement of the semiconductor industry, analog circuit designers are benefiting from scaling and improvement of the frequency response of the nano-scaled CMOS transistors, which makes people more interested to design and implement circuits and systems at mm-wave frequencies. There are several features of make the mm-wave band attractive for analog system design become attractive, which is large bandwidth, higher propagation loss, and smaller size of passive circuits.

For data transmission, higher order quadrature amplitude modulation (QAM) can provide significant benefits. With the cost of noise margin, the order of the QAM signal

can be increased. Therefore, a higher data rate could be achieved with higher order modulation scheme [10-12]. The Fig. 1- 4 shows the constellation diagram for a variety of modulation formats.

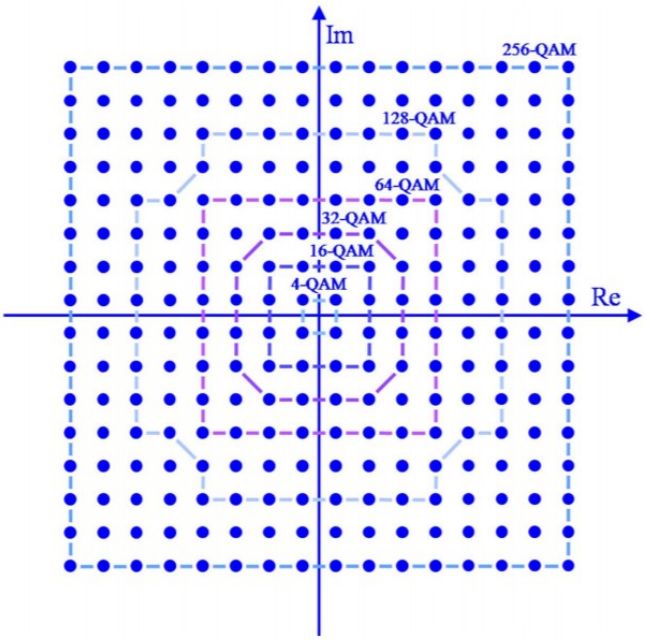


Fig. 1- 4 M-QAM constellation diagrams [10]

With the limited bandwidth, the higher data rate can be achieved by increasing the modulation order. However, the possibility of data error, which known as bit error rate, will also increase due to the distance between different points on the constellation decreases. To minimize the data error, a good signal to noise ratio per bit need to be considered for communication system design. So, the trade-off needs to be done between the maximum achievable data rate, order of QAM, power, and the acceptable bit error rate (BER) [13-15].

Modulation	Bits per symbol	Symbol rate	Spectral efficiency
BPSK	1	1 x bit rate	1 b/s/Hz
QPSK	2	1/2 x bit rate	2 b/s/Hz
8PPSK	3	1/3 x bit rate	3 b/s/Hz
16QAM	4	1/4 x bit rate	4 b/s/Hz
32QAM	5	1/5 x bit rate	5 b/s/Hz
64QAM	6	1/6 x bit rate	6 b/s/Hz

Table 1- 1 Comparison of QAM formats and spectral efficiency

As shown in Table 1- 1, a higher order of modulation means one symbol can carry more bits of information. Such as, QPSK only has 2 bits per symbol, but 64-QAM allows 6 bits per symbol. As the modulation order can even go higher to 256-QAM and so on, the data rate can be increased further. The relationship between the bit rate and the symbol rate depends on the order of modulation. The spectral efficiency also goes up with the modulation order increases.

To meet the design requirements for 5G mm-wave wireless communication systems, each building block in the transceiver systems needs to be implement and evaluate properly. Fig. 1- 5 shows the main circuit blocks of the transceiver systems. The typical circuit blocks on transmitter side are consist of the up-converting mixer, filters, and power amplifier (PA). And the receiver front-end mainly consists of the low noise amplifier (LNA), and down-converting mixer. Another important circuit block for transceiver system is the local oscillator (LO) signal generation part, such as phase locked loop (PLL) and quadrature voltage-controlled oscillator (QVCO) [16-22]. For different application scenarios, other circuit blocks can be added to form a transceiver front-end which meet the system specifications [23-25].

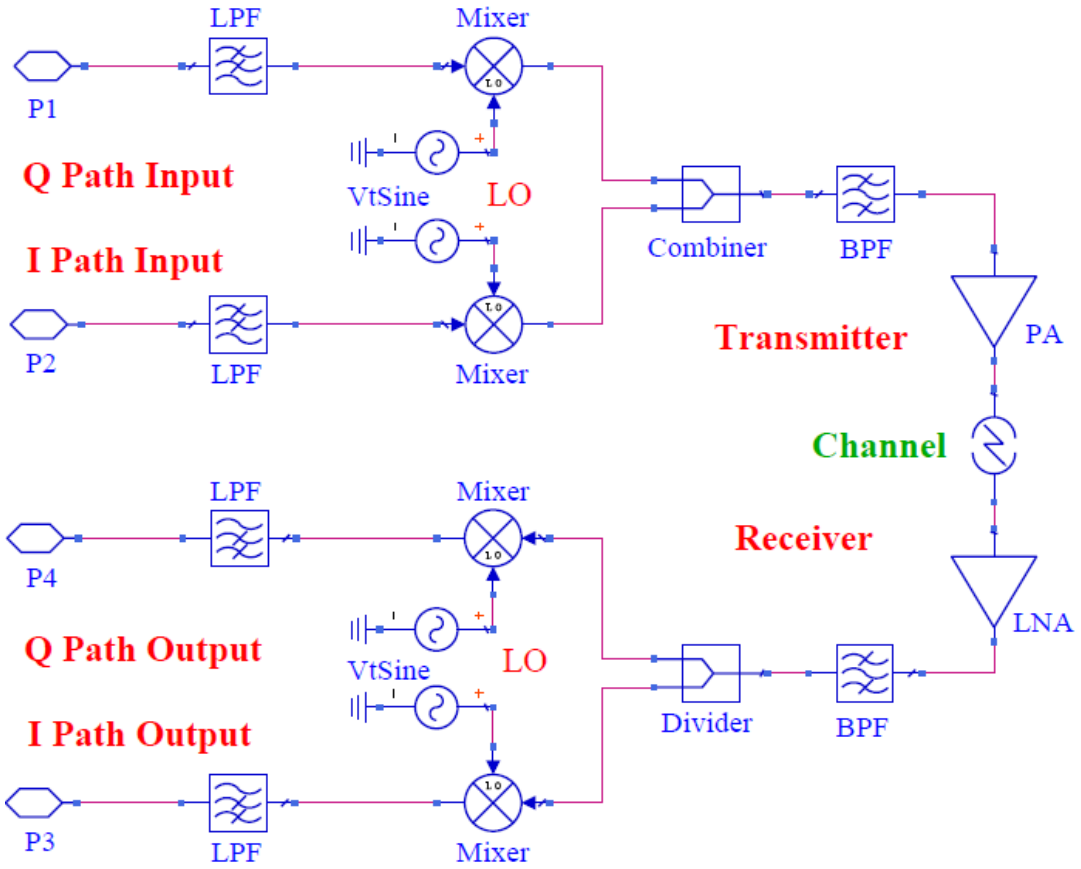


Fig. 1- 5 The circuit blocks of the typical transceiver system

Since mm-wave transceiver has inherently two signal channels, namely the in-phase (I) and quadrature-phase (Q) using the cosine and sine wave of the carrier, it becomes natural to directly modulate the PAM4 signal on the I and Q carriers which results a 16-QAM mm-wave signal. Other order of modulated signals, such as 64-QAM and 256-QAM can be implemented in the same way.

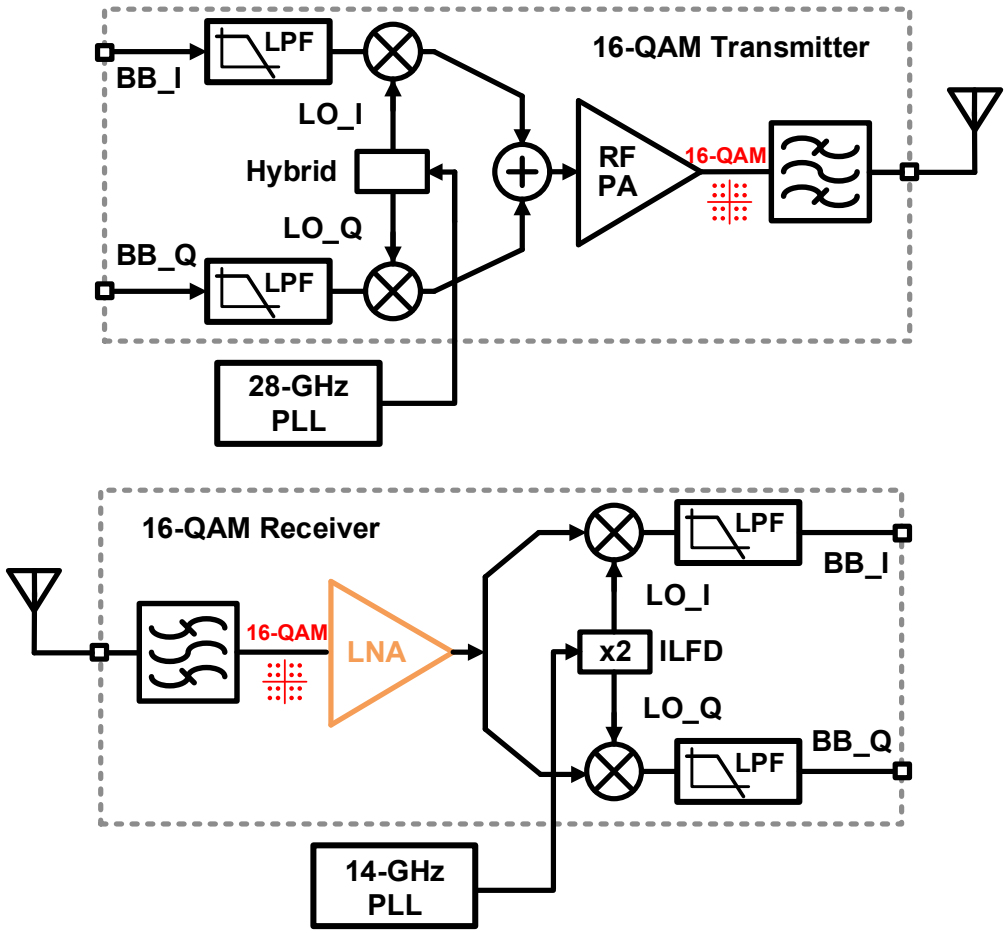


Fig. 1- 6 System diagram of the transceiver front-end with 16-QAM signal

Fig. 1- 6 shows a typical mm-wave transceiver front-end architecture. A 65-nm CMOS mm-wave 16-QAM transmitter, which could support a 16 Gb/s peak data rate for mm-wave 5G applications is demonstrated recently [26]. And this thesis mainly focuses on the receiver design. The input stage contains a low-noise amplifier (LNA) to provide a sufficient signal gain and noise suppression. The subsequent variable-gain amplifier (VGA) stage is coupled with the LNA output through an inter-stage transformer. The VGA amplifies the received signal and trades off the system overall gain and linearity. The last stage is a quadrature mixer with a folded architecture for current reuse and power saving. The mixer down-converts and separates the amplified signal into I and Q channels Low-pass filters (LPFs) are placed at the mixer outputs to remove high-frequency noise. All

passive and active components go through several layout and simulation iterations to meet the design target.

The rest of this thesis is organized as follow. In Chapter 2, the mixed-signal co-simulation platform design details is given and system-level design specifications for transceiver systems are discussed. Chapter 3 focuses on the actual receiver circuit implementation. Chapter 4 discusses the electromagnetic simulations and layout considerations for receiver integrated circuit (IC) design. The performance evaluation for receiver front-end using the co-simulation platform are demonstrated in Chapter 5. Chapter 6 makes a conclusion and summarizes the prospective of this thesis.

Chapter 2

Co-Simulation Platform

This chapter describes the design details for the mixed-mode co-simulation platform for mm-wave OFDM receiver IC. The chapter starts with the design motivation and continues with explanation of each part of the co-simulation platform. A brief introduction of OFDM is also included.

2.1 Motivation

As the overwhelming demand for the wireless mobile data traffic grows dramatically. Highly integrated transceiver systems have been actively studied and investigated to support multi-Gb/s data rate in future wireless communication. A transceiver system consists of many circuit blocks such as base band amplifiers, filters, mixers, power amplifiers (PAs) and low noise amplifiers (LNAs). Normally, it is not straightforward to simulate high performance circuit blocks together to obtain transceivers with the desired performance. It is important to make sure each sub-circuit of the transceiver cooperate well with others before fabrication. Furthermore, wideband modulated signals are always utilized in communication systems for improving the data rate and spectrum efficiency [27]. Thus, it is very meaningful and necessary to evaluate and predict the performances of transceiver systems using high-order modulated signals in the design procedure. Considering the above background, system co-simulation can be quite helpful to evaluate the performance of transceivers using high-order modulated signals [28], [29]. In [29], a hardware-software co-simulation platform was implemented for channel estimation in orthogonal frequency division multiplex (OFDM) systems. This

co-simulation platform shows great potential in speeding up the system verification process. But to date, few papers show a co-simulation platform for evaluating the transceivers of wireless communication systems.

In [30], the authors presented a co-simulation interface between MATLAB/Simulink and Xepedion/Goldengate circuit simulator. Based on this co-simulation interface, a 16-QAM (quadrature amplitude modulation) signal with a speed of 5 Mb/s was utilized to simulate a satellite communication chain [30]. However, this co-simulation interface did not show a signal demodulation process. In [31], a co-simulation platform between the MATLAB and VHDL-AMS environments was developed for the design and analysis of IR-UWB transceivers. However, the co-simulation platform in [31] did not show the signal modulation and demodulation function, and the transceiver is based on VHDL-AMS language rather than real circuit blocks.

MATLAB has been validated as a powerful candidate for signal modulation and demodulation, and the most powerful RF and mm-wave circuit design and simulation software are Advanced Design System (ADS) and Cadence. Therefore, constructing a co-simulation platform using MATLAB, ADS and Cadence will help users to easily evaluate the performances of transceivers in the design process

Considering the above background, we built a mixed-mode co-simulation platform for mm-wave receiver IC design which can be used from system specification to circuit implementation.

The co-simulation platform including signal modulation/demodulation and circuit simulation is developed for evaluating the performances of receiver. This co-simulation platform is implemented using MATLAB, ADS and Cadence software. For easily using this co-simulation plat- form, a graphical user interface (GUI) is also constructed using MATLAB. Users can validate the system performance conveniently by integrating sub-block circuit into the transceiver system. Fig. 2- 1shows the diagram of the mixed-mode co-simulation platform.

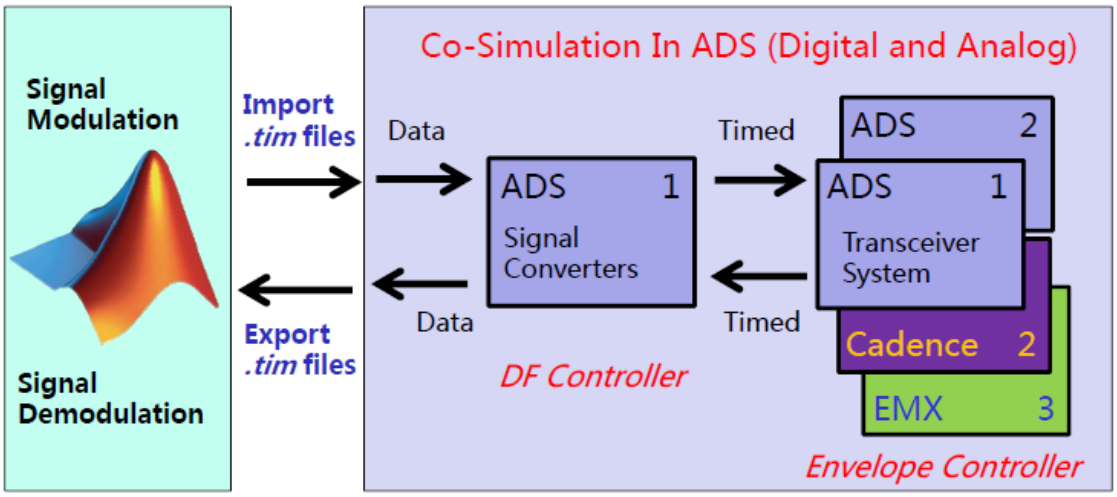


Fig. 2- 1 The diagram of the mixed-mode co-simulation platform

Based on this co-simulation platform, the co-simulation flow is as follows:

Step 1. An M-QAM OFDM signal is generated by MATLAB codes. Then the real and imaginary parts of the modulated signal are automatically saved into two .tim files. These .tim files will be dynamically imported by ADS, as shown in Fig. 2-1.

Step 2. After reading the .tim files, data flow (DF) controller in ADS is utilized to realize data conversion, generating timed I and Q path signals.

Step 3. The timed I and Q path signals are delivered to the transceiver system for simulating the transmitter and receiver.

Step 4. The output I and Q path signals of the receiver is automatically saved as two .tim files.

Step 5. The .tim files generated in Step 4 are dynamically delivered back to Matlab for demodulation and further processing.

Notice that the simulation of the transceiver system in Step 3 should use the ENVELOPE controller in ADS. Therefore, the DF and ENVELOPE controllers should be utilized simultaneously when performing co-simulation in ADS.

2.2 OFDM Modem in MATLAB

The orthogonal frequency-division multiplexing (OFDM) is used to encode digital data on multiple carrier frequencies. And It usually applicable to mobile communications and audio broadcasting [32]. In OFDM, data are parallel carried by multiple orthogonal subcarriers with specified spacing. To compared with single-carrier scheme, OFDM features a good ability to overcome severe channel conditions, such as, frequency-selective fading due to multi-path, or interference caused by narrowband. It can also provide better spectral efficiency as compared with double sideband modulation schemes. However, it requires transmitter has good linearity to overcome high peak-to-average-power-ratio (PAPR). And another drawback is due to the cyclic prefix, which can be used for synchronization, it degrades the efficiency [33]. Fig. 2- 2 shows the 16-QAM OFDM signal modulation and demodulation process.

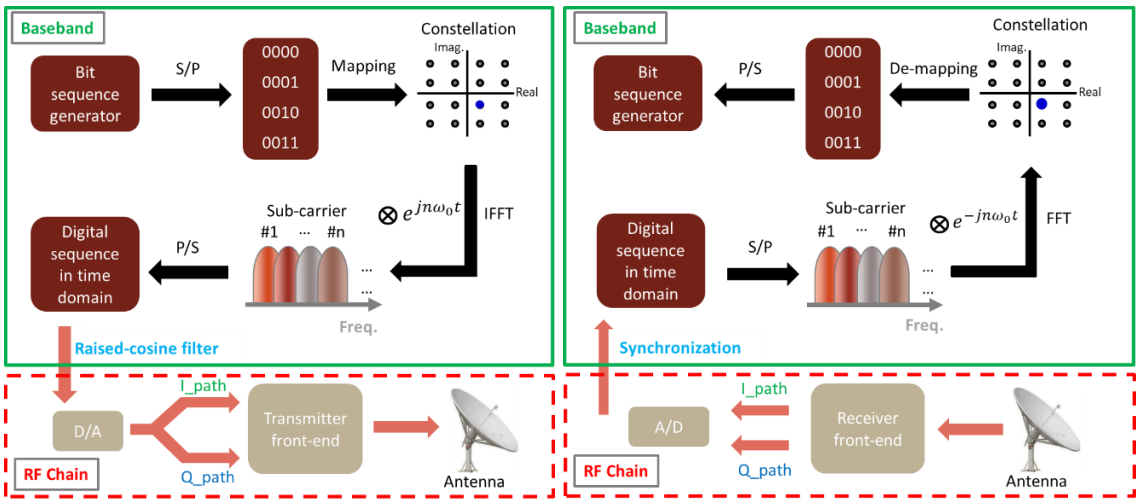


Fig. 2- 2 OFDM with 16-QAM: (a) Modulation (b) Demodulation

The co-simulation platform is based on MATLAB, and ADS and Cadence simulators.

The following shows the details of the co-simulation and the simulation results.

For signal modulation and demodulation, an M-QAM OFDM signal is adopted to perform the co-simulation because OFDM signal is widely applied in modern communication systems [34-35]. The modulation diagram of the M-QAM OFDM signal is depicted in Fig. 2-3. The modulation can be concluded as:

1) A pseudo random binary sequence (PRBS) is generated and converted to N parallel bit sequences, where N is the number of sub-carriers in OFDM signal. Then the paralleled bit sequence is mapped to M-QAM symbols.
2) N-point inverse fast Fourier transform (IFFT) algorithm is performed to the M-QAM symbols, generating the sub-carriers of OFDM signal.
3) Cyclic prefix (CP) and pilot symbols are added to each OFDM frame to avoid inter symbol interference and inter carrier interference.
3) Finally, the QAM-OFDM signal can be generated by combining all sub-carriers through a serial to parallel conversion.

The inverse process of the modulation is the demodulation, which is depicted in Fig. 2-3. Notice that synchronization should be performed before demodulating the M-QAM OFDM signal. Besides, the frequency separation can be calculated by the signal bandwidth divided by the number of subcarriers. This value is specified for different application scenarios.

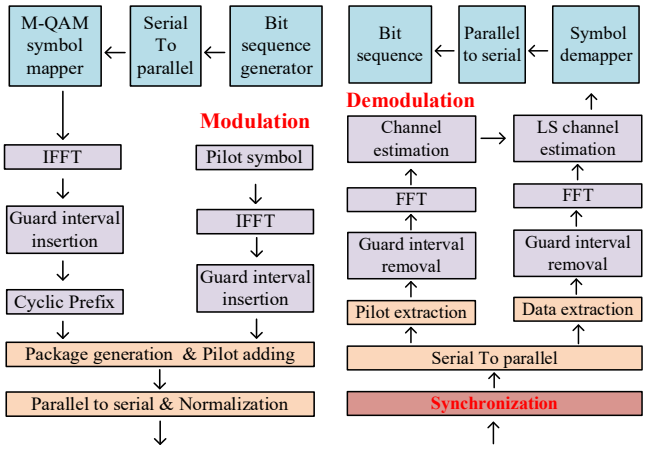


Fig. 2- 3 The diagram of signal modulation and demodulation

2.3 MATLAB GUI

For accelerating the co-simulation, a GUI is implemented, as illustrated in Fig. 2-4. This GUI includes two main parts: signal modulation and signal demodulation.

In the co-simulation, the modulation process will be triggered by clicking the Signal Modulation icon on the GUI. As shown in Fig. 2, the bandwidth and PAPR of the transmitted baseband signal will be displayed on the GUI after clicking the Signal Modulation icon. The baseband spectrum and constellation of the M-QAM OFDM signal will also be displayed on the GUI. The frequency separation in this example is 97.6 KHz. For different application scenarios, this value can be adjusted accordingly by changing the signal bandwidth and the number of subcarriers. Sampling rate is 1 Gs/s. And the time duration of OFDM symbol is 28us.

The demodulation process comes into operation after clicking the Signal Demodulation icon. Other than the spectrum and constellation, the calculated bit error rate (BER), error vector magnitude (EVM) and data rate of the received baseband signal will be shown on the GUI after demodulation.

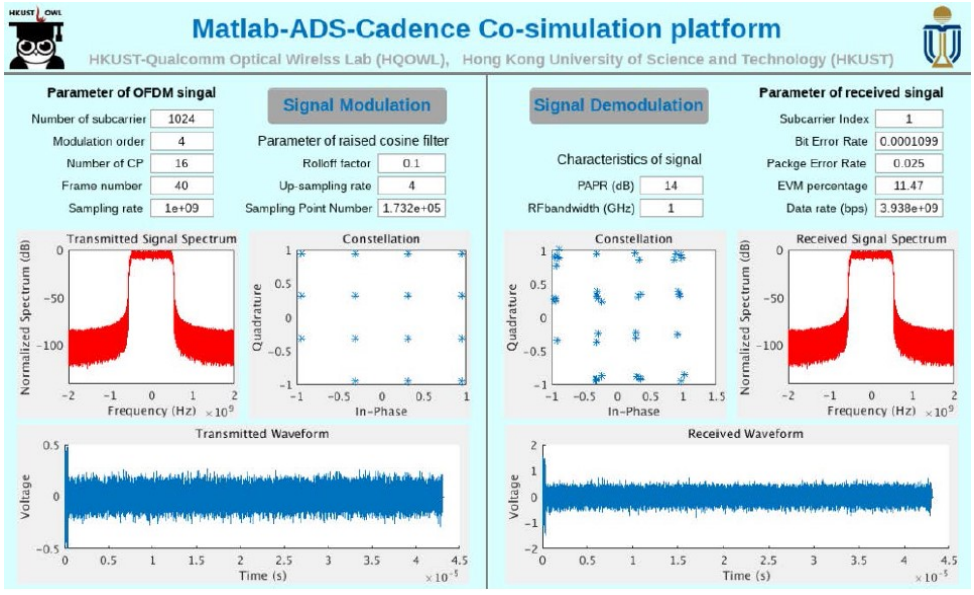


Fig. 2- 4 The graphical user interface of the co-simulation platform

2.4 Circuit Simulation in ADS and Cadence

After clicking the Signal Modulation icon on the GUI, an M-QAM OFDM signal will be generated and saved as a .tim file. Then, the simulation of the transceiver system in ADS can be started. The top view of the simulation schematic in ADS is illustrated in Fig. 2- 4.

The .tim files generated by MATLAB are read by the data access component (DAC) in ADS. The interface of MATLAB and ADS is based on discrete data points; therefore, the received data (I and Q path inputs) should be converted to a timed signal before delivery to the transceiver system. Similarly, the output signal of the transceiver should be converted to discrete data points (I and Q path outputs) again before being sent back to MATLAB. In ADS, the data conversion can be realized using a DF controller and corresponding components, as shown in Fig. 2- 5.

The system diagram of transceiver in Fig. 2- 5 are depicted in Fig. 2- 6. Both the transmitter and the receiver are based on the direct-conversion architecture. The local oscillators (LOs) are realized using voltage source blocks in ADS, and the I and Q path are combined or divided by Wilkinson power splitters. In the transceiver system, all the circuit blocks are ideal blocks in ADS. Besides, the parameters of these circuit blocks are set based on published references.

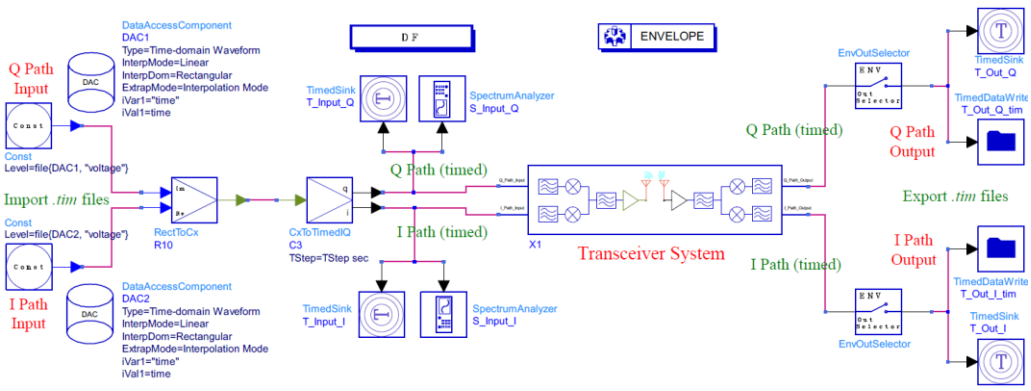


Fig. 2- 5 The top view of the co-simulation schematic in ADS

Though ADS provide users with a friendly circuit design and simulation environment, the most popular simulator for integrated circuits is Cadence software. Thus, a dynamic link between ADS and Cadence simulators is very important for integrated circuit design such as CMOS PA and LNA design. The dynamic link between the ADS and Cadence simulators is schematically illustrated in Fig. 2-7. The circuit blocks designed in Cadence simulator can be dynamically linked to ADS for simulation, as shown in Fig. 2- 7.

After finishing the simulation in ADS, two .tim files will be generated automatically. These .tim files include the discrete data points of the output of the transceiver system. Then the demodulation process can be started by clicking the Signal Demodulation icon on the GUI.

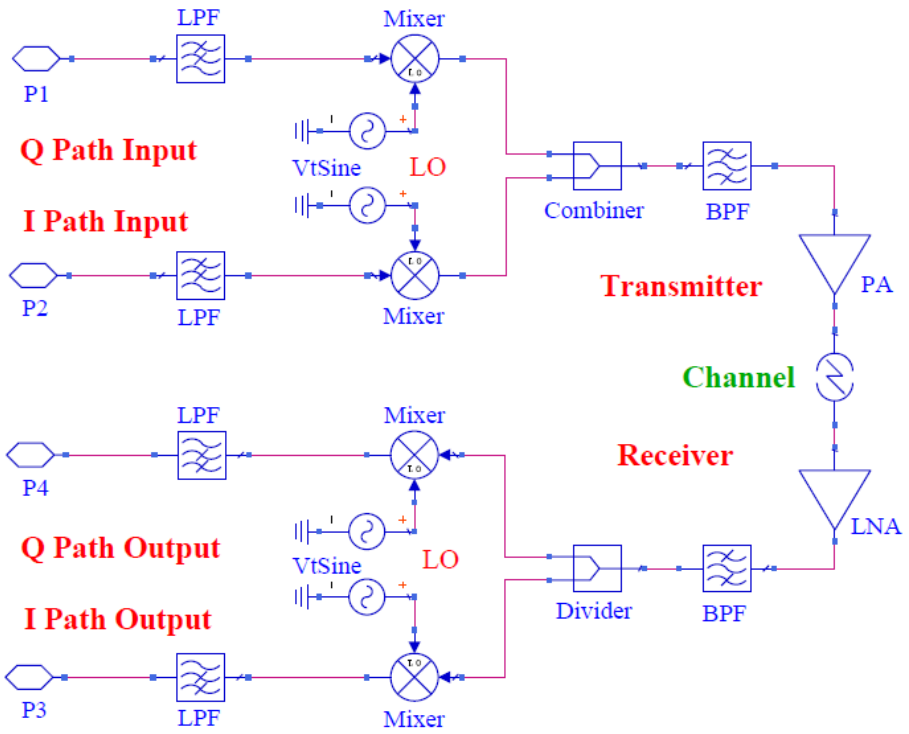


Fig. 2- 6 System diagram of transceiver with OFDM

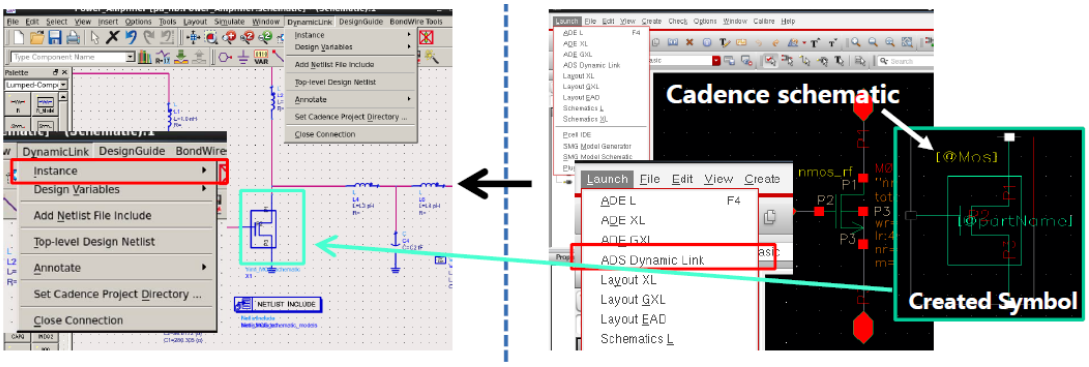


Fig. 2- 7 Dynamic link between ADS and Cadence

2.5 Co-simulation Process

2.5.1 Link budget and propagation path loss

The range of a wireless link depends on how much power the transmitter can output and the receiver sensitivity. Friis transmission formula for path loss in free space is shown below [36].

$$P_R = \frac{\lambda^2 \times G_{AT} \times G_{AR} \times P_T}{(4\pi)^2 \times d^2} \qquad PD_T = \frac{P_T}{4\pi \times d^2}$$

where:

P_R = The power received by receive antenna

P_T = The power delivered to the transmit antenna

G_{AT} = The gain of the transmit antenna

G_{AR} = The gain of the receive antenna

d = The distance between two antennas

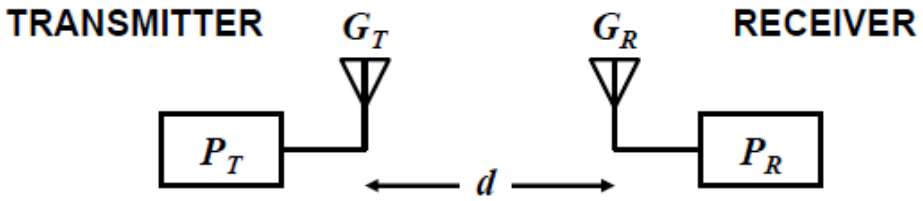


Fig. 2- 8 Wireless link

The link budget accounts all the power gains and losses that a signal experience in a communication system as shown in Fig. 2- 8. The equation is shown below:

$$P_{RX}=P_{TX}+G_{TX}-L_{TX}\_L_{FS}-L_M+G_{RX}-L_{RX}$$

where:

P_{RX} = received power (dBm)

P_{TX} = transmitter output power (dBm)

G_{TX} = transmitter antenna gain (dBi)

L_{TX} = transmitter losses (coax, connectors…) (dB)

L_{FS} = path loss, usually free space loss (dB)

L_M = miscellaneous losses (fading margin, body loss, polarization mismatch, other losses...) (dB)

G_{RX} = receiver antenna gain (dBi)

L_{RX}= receiver losses (coax, connectors…) (dB)

The diagram of the link budget is shown in Fig. 2- 9.

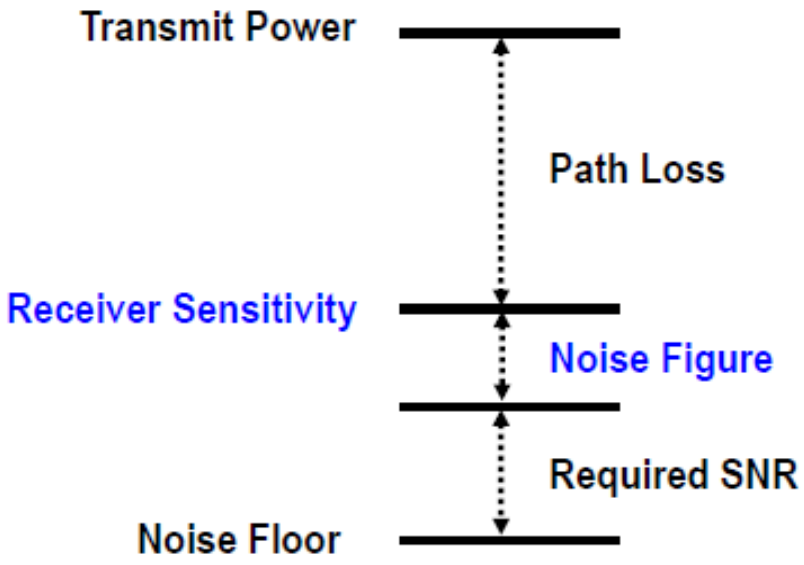


Fig. 2- 9 Diagram of link budget [28]

2.5.2 Simulation results on GUI

Based on ideal transceiver circuit blocks. The simulation results can be seen easily on the MATLAB GUI. An example is shown in Fig. 2- 10. For the transmitted baseband signal. We set the number of subcarriers as 1024. The modulation order is 4. Then, 16-QAM signal will be generated. Besides, the frame number is 40. Sampling rate is 1GHz with up sampling rate equals to 4. The total sampling point number in this example is 173200. Then this modulated signal passes through the ideal transceiver circuit blocks in ADS and the output baseband signal can be demodulation in MATLAB. The signal characteristics of the demodulation signal is shown on the right-hand side of this GUI. We can choose different subcarrier index to see the corresponding signal characteristics. The BER is 10^{-4} and the package error rate (PER) is 0.025. EVM can also be calculate as 11.47%. Data rate is approximate to 4 Gb/s as desired.

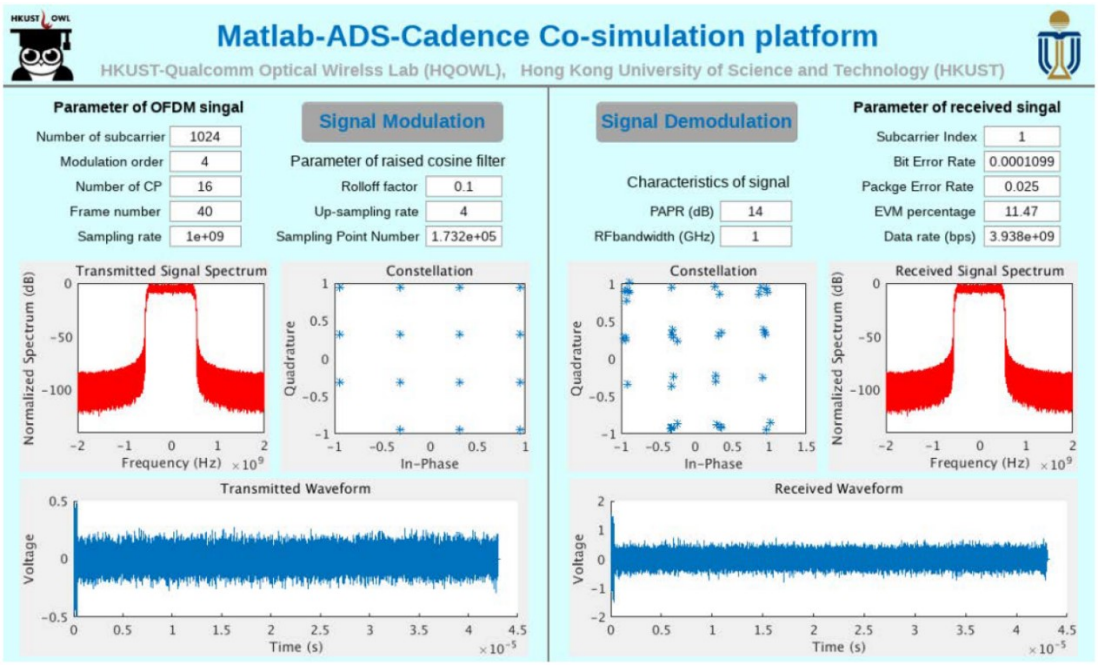


Fig. 2- 10 The GUI of the co-simulation platform

2.6 Conclusion

This chapter shows a mixed-mode co-simulation platform to realize a mm-wave receiver IC design from system specification to circuit implementation. To validate the transceiver performance, we built an OFDM modem in MATLAB for the bit error rate (BER) and constellation check. A graphical user interface (GUI) was constructed in MATLAB to in/out simulated files between MATLAB and ADS/Cadence dynamically. The platform links the baseband digital signals and the RF front-end. A GUI was constructed in MATLAB to model the baseband signals. For further implementation, A broadband receiver at 28 GHz for a high data rate 5G communication system can be implemented to replace the ideal circuit blocks. Then the performance of the receiver front-end can be tested with the OFDM signal. Besides, since the circuit part used in this transceiver simulation platform includes common transceiver circuit blocks, so this platform can support varies circuit blocks design. Users can easily replace some of the

behavior circuit blocks with actual designed circuit to verify the system level performance with baseband signal modem.

Chapter 3

Direct-Conversion Receiver Front-End Design

This chapter describes the circuit implementation of mm-wave receiver front-end.
The chapter starts with the design motivation and continues with proposed low noise amplifier. Studies and implementations of the mixer, variable gain amplifier, and output buffer are also illustrated.

3.1 Motivations

Recently, there are several mm-wave M-QAM transmitter demonstrate for high data rate wireless communication [37-40]. The design of broadband receiver at lower mm-wave band to support such high-speed communication is the main focus in this chapter. Low noise amplifier (LNA) is the first stage in RF receivers and it plays a very import role. So, the proposed receiver front-end design focuses on developing a low-power CMOS LNA in 24-32 GHz band for 5G high-speed communication.

3.2 Capacitive cross-coupling technique

The SNR of is received signal is degraded because of the thermal noise of the RX. The higher the noise figure (NF), the lower the SNR. Using an LNA helps to suppress the noise contribution of the RX building blocks with fewer overheads [41-43].

All active electronic components and some passive devices have flicker noise. It is associated with a DC current flow. In CMOS technology, flicker noise is a concern of the transceiver system due to its higher flicker noise corner frequency. To omit this issue, there should be enough gain before the baseband circuits, so the baseband circuits should be designed for low flicker noise.

The capacitive cross-coupling (CCC) as shown in Fig. 3- 1 can be used to enhance the gain and it can also be a part of the matching network [45]. In [44], it demonstrates the CCC can improve the NF of a common-gate input stage. Fig. 3-1 shows that the noise caused by cross-coupling for M_1 and M_2, namely V_{n1}^2 and V_{n2}^2. Then, the common-mode noise voltage at the output node is d1 and d2. If we assume the instantaneous polarity for noise source $V_{n1}^2$is positive and the other side is negative. Then the drain voltage of M_1 decreases when gate terminal has positive disturbance. Besides, the drain voltage of M_2 also decreases because S2 has negative disturbance. So common-mode voltages at d1 and d2 are generated because of V_{n1}^2. Noise source V_{n2}^2 can be analyzed in a similar way.

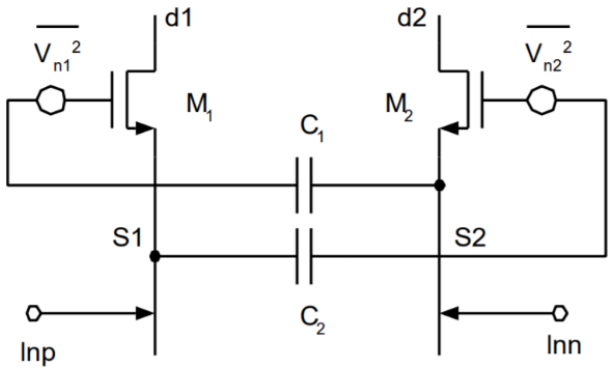


Fig. 3- 1 Capacitive cross coupling technique [44]

3.3 Proposed LNA

Common-source, common-gate, and cascode are three popular LNA topologies. Table 3-

1 summarizes a brief comparison with selected LNA design parameters.

Characteristic	Common-Source	Common-Gate	Cascode
Noise Figure	Lowest	Rises rapidly with frequency	Slightly higher than CS
Gain	Moderate	Lowest	Highest
Linearity	Moderate	High	Potentially Highest
Bandwidth	Narrow	Fairly broad	Broad
Stability	Often requires compensation	Higher	Higher
Reverse Isolation	Low	High	High
Sensitivity to Process Variation, Temperature, Power Supply, Component Tolerance	Greater	Lesser	Lesser

Table 3- 1 Comparison of three LNA topologies

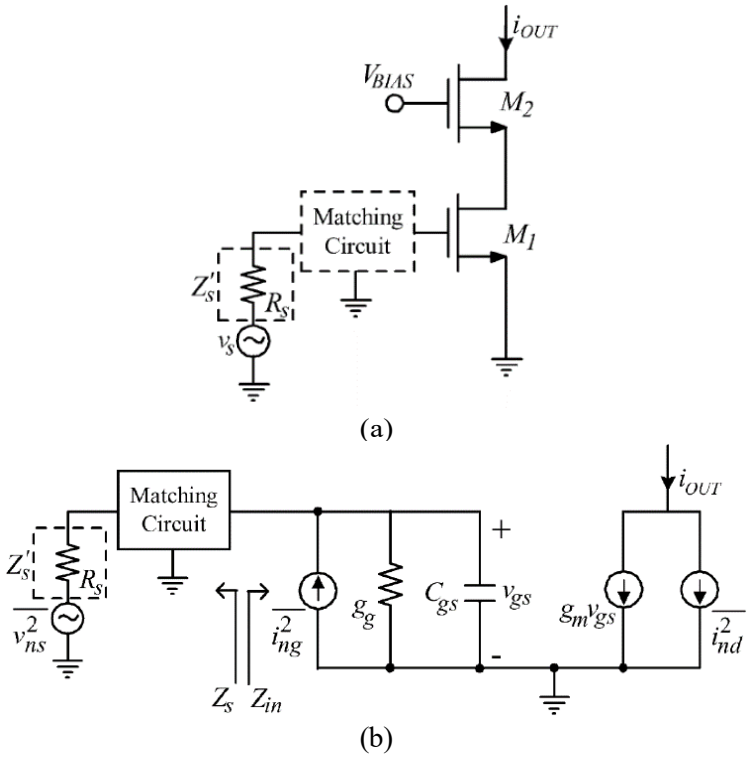
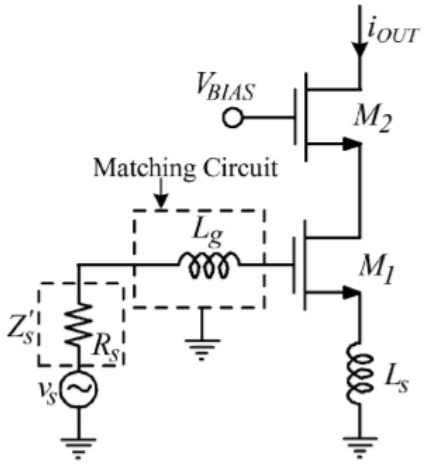


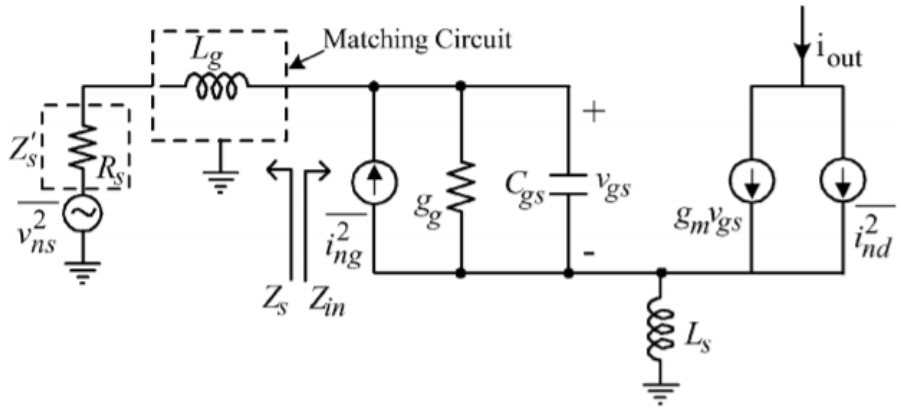
Fig. 3- 2 . (a) Schematic of a cascode LNA with classical noise matching technique (b)Small-signal equivalent circuit [46]

The classical noise matching (CNM) technique is reported in [46]. This technique is focusing on minimizing the NF by optimizing noise impedance to the given amplifiers. One way to realize this is to add a input matching circuit. Fig. 3- 3(a) shows a cascode-type LNA topology, it features wide bandwidth, high gain, and high reverse isolation.

Fig. 3- 3 (b) shows the noise analysis with simplified small-signal equivalent circuit of the cascode amplifier.



(a)



(b)

Fig. 3- 3 (a) Schematic of a cascode LNA with simultaneous noise and input matching (b)Small-signal equivalent circuit [46]

In Fig. 3- 3, i_{nd}^2 represents the mean squared channel thermal noise current, which can be calculated by the equation below [46]:

$$\overline{i_{nd}^2} = 4kT\gamma g_{d0}\Delta f$$

where:

g_{d0} = drain-source conductance ($V_{DS} = 0$)

k = Boltzmann constant

T = absolute temperature

Δf = bandwidth

$\Gamma = 1$ ($V_{DS} = 0$)

$\Gamma = 2/3$ (saturation mode)

The channel noise causes fluctuating channel potential. And the fluctuating channel potential couples capacitively into the gate terminal. It leads to a noisy gate current.

As design considerations discussed above, the proposed LNA adopts the CG structure. Since a broadband input impedance matching can be easily realized in CG structure. It can be achieved by making $g_m R_s = 1$, where g_m is the transconductance of the transistor and R_S is the source resistance. Then g_m-boosted is wildly used in LNA design because it can provide a relatively large voltage gain of $(1 + A)g_m$, where A is the inverting gain, at small current consumption. The diagram is shown in Fig. 3- 4 (a). In this condition, $(1 + A)g_m = 1$ is considered for input matching. The dominant noise in CG LNA is the noise from the drain current and the source resistance. So, the noise performance of LNA can be improved by reducing the drain current. The proposed g_m-boosted CG LNA is shown in Fig. 3- 4 (b). As to obtain a better linearity, it is a differential structure to accommodate larger signal. It consists of two main parts. A CG input stage and a source follower output buffer. The CG input stage has transistor M_1 and M2. Besides, M_3 and M_4 are a pair of cascode transistors, which helps to improve the reverse isolation. A three-coil input transformer (L_1, L_2 and L_3 is used as the input matching stage for the LNA. L_4 and L_5 forms the inter-stage matching network between CG stage and output buffer.

To realize the g_m-boosting in differential structure, a passive implementation way is capacitive cross-coupling (CXC) technique. It can improve the linearity by reducing the noise of input transistors. But the inverting gain A in this case can only be smaller than 1. Because it has a capacitor divider effect between the cross-coupled capacitors and the C_{GS} of the input transistors. Considering the conditions above, this work propose a three-

coil transformer together with the XC to enhance the gm-boosting and the noise suppression. This three-coil transformer also realizes a single-ended to differential conversion and a broadband input impedance matching at the same time.

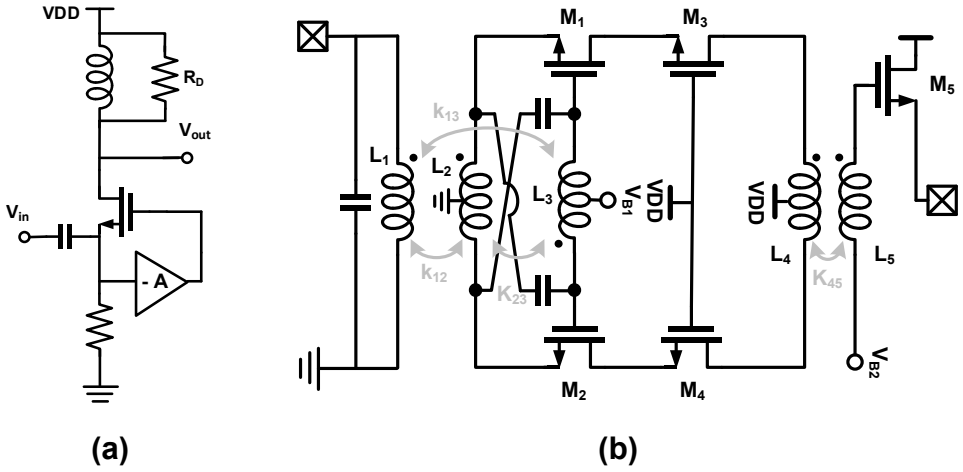
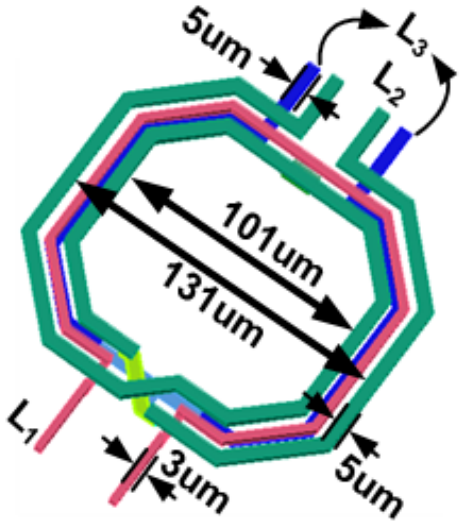
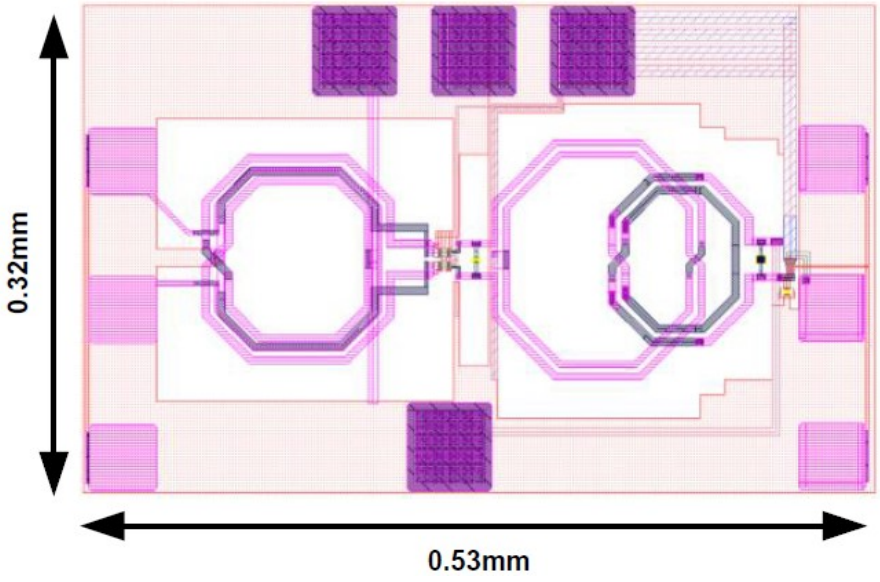


Fig. 3- 4 Circuit schematics: (a) g_m-boosted CG LNA, and (b) proposed LNA

Fig. 3- 5 shows the layout of the proposed three-coil transformer. The detailed consideration for layout and electromagnetic simulation steps will be discussed in the next chapter.



(a)



(b)

Fig. 3- 5 (a) The 3-D view of the three-coil transformer (b) layout of proposed LNA

To ease the matching condition of the LNA's output, a source follower is used as the output stage to connect the 50Ω load. It can achieve a broadband output impedance matching because the output resistance of the source follower is approximately $1/(g_m + g_{mb})$, where g_{mb} is body effect. By tuning the biasing current, the impedance matching condition can be improved. One disadvantage of source follower is that it degrades the LNA's linearity. Then the signal may suffer distortion problem. One way to compensate this issue is to increase the biasing current, but the power consumption increases also. However, the first CG Stage with good linearity can provide some tolerance for linearity degradation caused by output stage. For a stand-alone LNA, the source follower is meaningful as the output stage. When the LNA integrated with VGAs and mixers to form a receiver front-end, then the source follower is no longer a necessary circuit block. So, the LNA itself can remain a good linearity for further integration, which means it is suitable to support a higher order modulation scheme, e.g., 16-QAM.

L_4 and L_5 forms an inter stage transformer, it can improve the bandwidth of the LNA by acting as a multi-peak resonator [47]. Besides, this transformer also converts the differential output signal to single-ended signal which can be used to drive the source follower. When the transformer acts as a multi peak resonator, the positions and amplitude of two gain peaks can be adjusted by changing the parameters related to the transformer. Such as, inductances and quality factors of L_4 and L_5, coupling factor of transformer. To achieve our design target, the first peak and the second peak designed to be around 25 GHz and 31 GHz, respectively. It features an 8.9 GHz 3-dB bandwidth. The bandwidth can be further increased by sacrificing the in-band gain ripple. So, the trade-off between flatter gain and larger bandwidth can be done by adjusting the parameters related to the transformer as discussed before.

With 65-nm CMOS technology, the simulated results of the proposed LNA is shown in Fig. 3- 6. The peak gain is 15 dB with 8.9 GHz 3-dB bandwidth centered at 27.8 GHz as shown in Fig. 3- 6 (a). Fig. 3- 6 (b), (c), (d) show the matching condition, the linearity, noise figure, and the reverse isolation accordingly. Both the input and the output achieve good matching condition with S_{11} and S_{22} below -10 dB withing desired bandwidth. With two-tone 10 MHz separation simulation, the IIP_3 is -1.7 dBm. Without the output buffer, LNA itself features 1dBm IIP_3. Then the NF is below 4 dB within the 3-dB bandwidth. The reverse isolation is simulated as S_{12}, and it is lower than -53 dB. S_{12} is very good due to the two cascode transistors, which help to improve the reverse isolation.

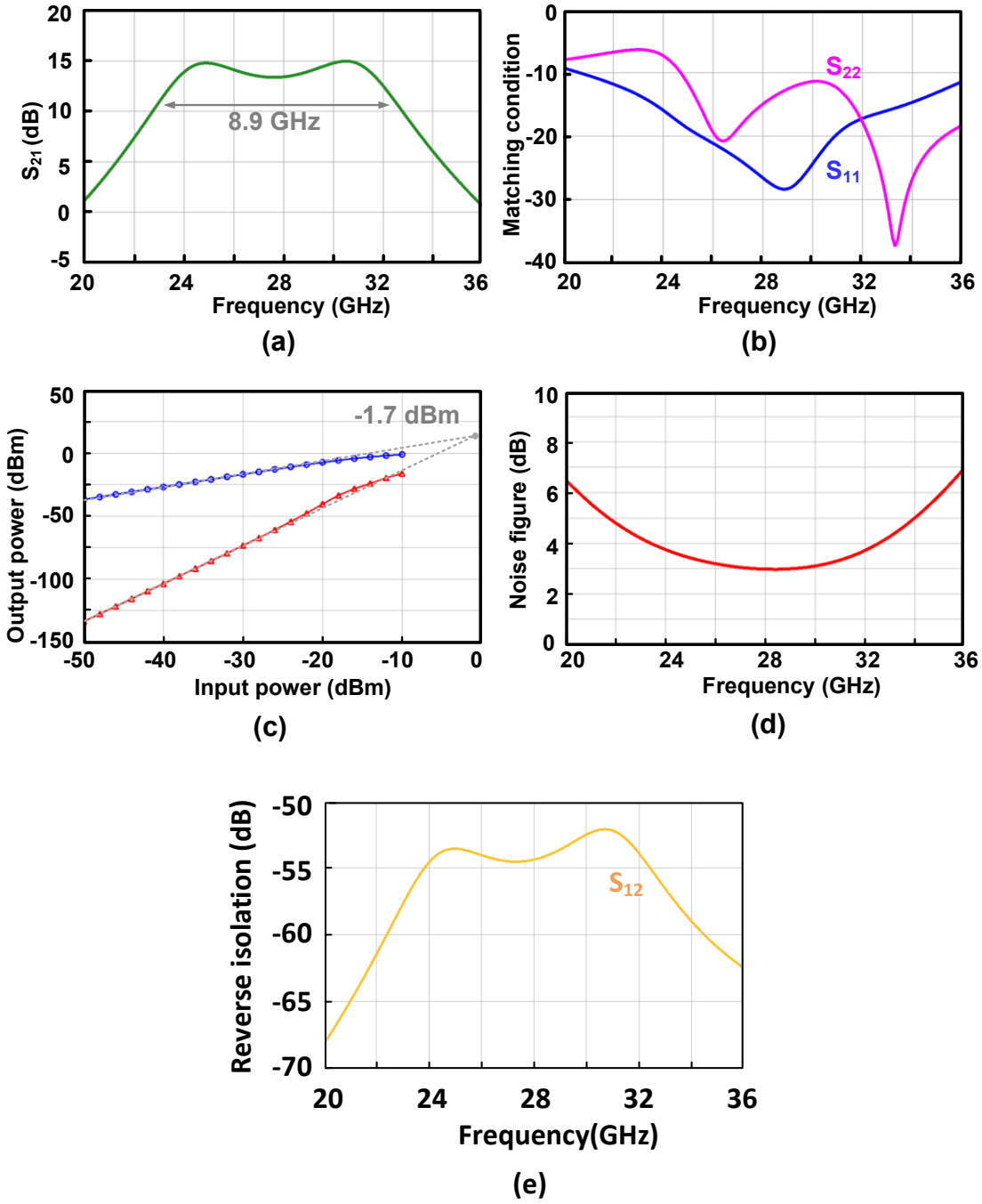


Fig. 3- 6 Simulated results of the proposed LNA: (a) gain, (b) matching condition, (c) IIP_3, (d) noise figure, and (e) reverse isolation.

3.4 Mixer

3.4.1 Functionality

Mixers is another essential building block in transceiver system. The main function of

it is to shift the frequency spectrum of the input signal. Fig. 3- 7 shows a circuit symbol for a mixer with three ports.

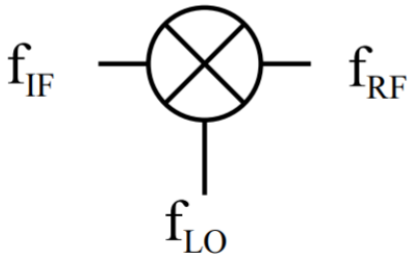


Fig. 3- 7 Mixer circuit symbol

3.4.2 Passive mixer and active mixer

The design of mixers usually considers the conversion gain, local oscillator (LO) power, linearity, noise figure, port-to-port isolation, voltage supply, and current consumption [48-50]. With desired conversion gain, the LO power required for active mixers is smaller than passive mixers. However, the linearity of passive mixer is good because the transistors are either “on” or” off”. To avoid SNR degradation, the linearity needs to be good. Moreover, the double balanced mixers achieve good port-to-port isolation making the double balanced structure to be suitable for integrated circuit design [51].

3.4.3 Gilbert cell

Gilbert cell mixer is a popular choice in integrated circuit design. The main body consists of a stack of three transistors, and a load resistor [52-53]. It uses a differential pair to achieve the trans-conductor implementation. Fig. 3- 8 shows the schematic of a typical Gilbert cell.

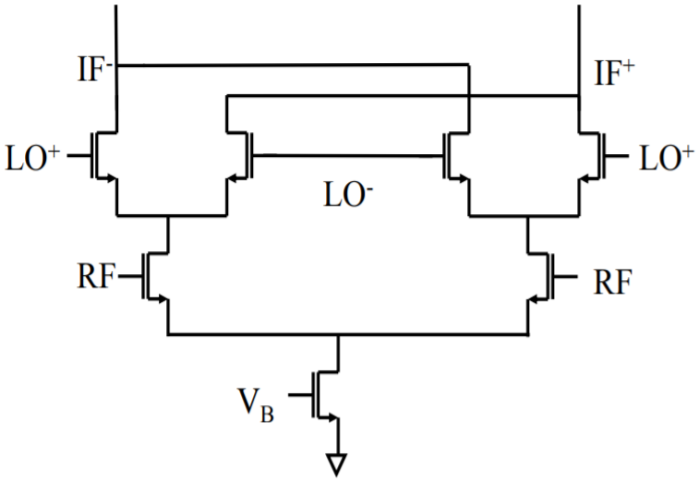


Fig. 3- 8 Schematic of a double-balanced mixer

To have a balanced signal. The DC component of RF and LO signals need to be zero. The unbalanced RF input causes LO feedthrough and unbalanced LO signal causes RF feedthrough. Transistors require a DC bias. Then balanced LO signal can be achieved by DC biasing. Fig. 3- 9 shows the combining of 180 degree out of phase LO signals in two mixer paths [51].

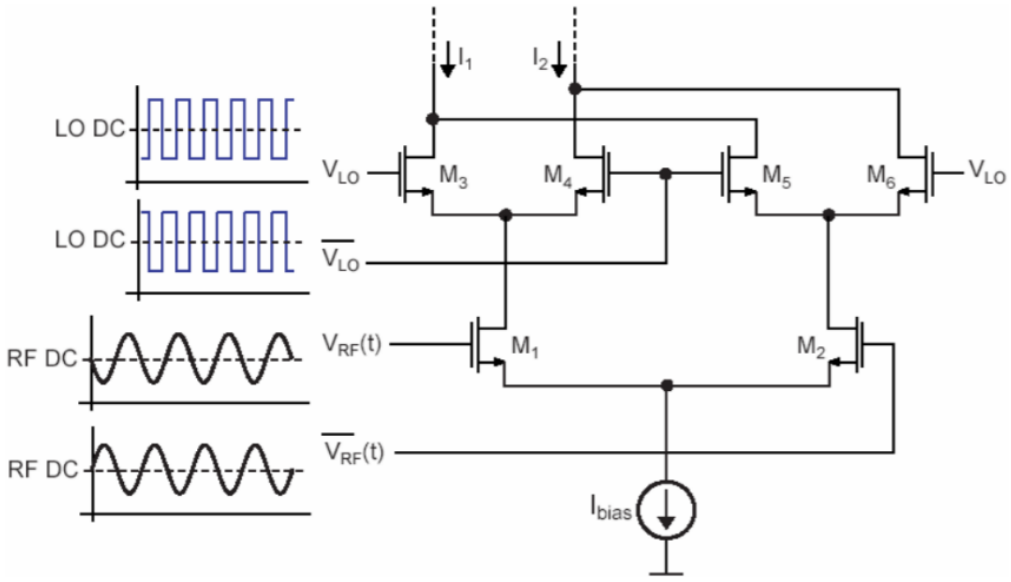


Fig. 3- 9 Signal flow of the double-balanced mixer [51]

To suppress the DC offset and thermal noise, the bias current for the switches should be minimized. The value of V_{GS} for the LO switches should be close to V_t. It helps to make the LO amplitude within a reasonable range for current commutation. Another good point of using smaller bias current is that the load resistance can be large. Then the CG can be increased without sacrificing large IR drop from the limited voltage headroom. The RF chokes present a high impedance for desired bandwidth [52].

It is very important to consider the DC offset problem in mixer design. In direct conversion receiver, the receiver becomes saturation if the DC offset is too much. Besides, device mismatch causes static DC offset. In fully balanced structures, mismatch is the main contributor to the DC offset.

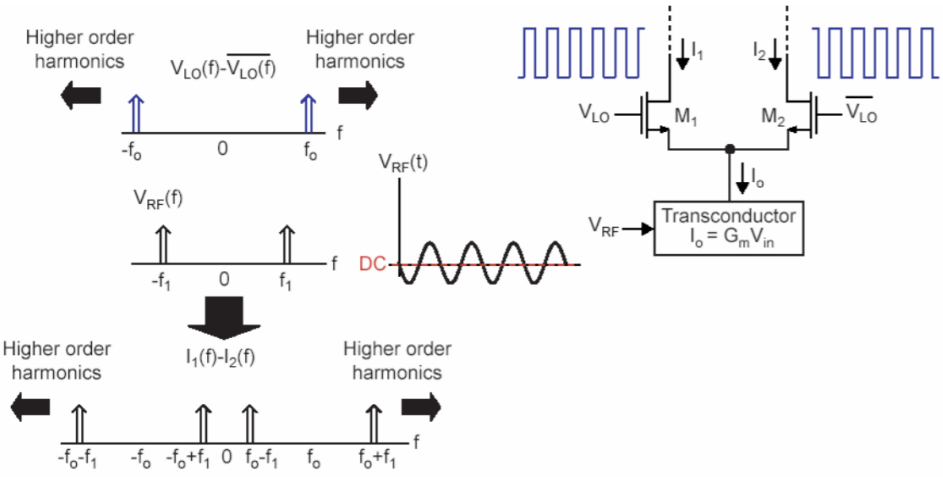


Fig. 3- 10 Behaviors of ideal double-balanced mixer [51]

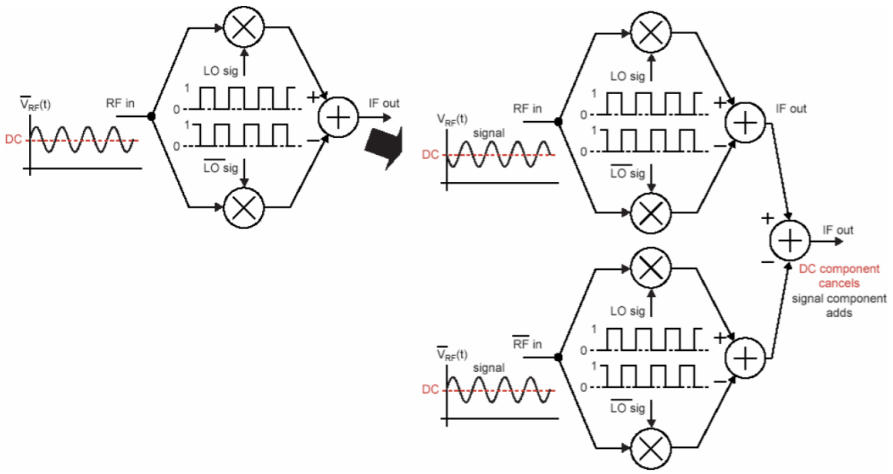


Fig. 3- 11 Achieving balanced RF signal with Biasing [51]

To optimize the mixer performance, the biasing condition for the input stage needs to be well designed. And there are three contributors to mixer noise:

- Switching pairs
- Load resistance
- Transconductance stage

Noise contributors: loads (1/f noise), transconductance transistors (1/f noise and white noise), switch noise. The SNR due to the switch noise is shown below:

$$signal = G_m \times V_{in} = \frac{2g_m V_{in}}{\pi}$$

$$SNR = \frac{2g_m V_{in}}{\pi} \frac{1}{\frac{1}{\pi}\frac{IV_n}{A}} = \frac{2A}{V_{GS} - V_T} \frac{V_{in}}{V_n} \qquad g_m = V_{GS} - V_T$$

The SNR can be improved by increasing LO swing, trading off with frequency, reducing over-ride voltage, adjusting transistor size.

3.5 Variable gain amplifier

The variable gain amplifier (VGA) is employed to maximize the overall system dynamic range. For design specifications, we prefer stable gain for wide bandwidth, low noise, low distortion, and low power. There are several techniques for VGA design, multipliers, transconductance ratio amplifiers, and source degeneration. In this mm-wave receiver front end design, we used a simple multiplier-based VGA. Gain can be linearly controlled by V_{cont}.

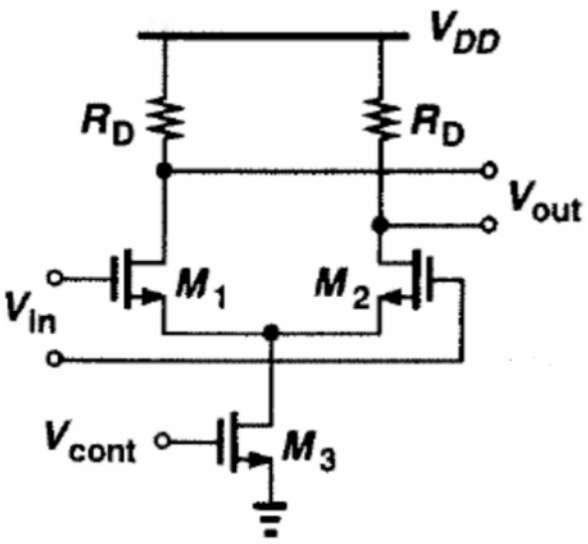


Fig. 3- 12 schematic of multiplier-based VGA [54]

Below are the equations for analysis the behavior of the VGA shown in Fig. 3- 12.

$$A_v = g_{m1} R_D$$

$$g_{m1} = \sqrt{\mu C_{ox} \left(\frac{W}{L}\right)_1 I_3}$$

$$I_3 = \frac{\mu C_{ox}}{2} \left(\frac{W}{L}\right)_3 (V_{cont} - V_T)^2$$

$$g_{m1} = \sqrt{\frac{(\mu C_{ox})^2}{2} \left(\frac{W}{L}\right)_1 \left(\frac{W}{L}\right)_3 (V_{cont} - V_T)^2} = \mu C_{ox} (V_{cont} - V_T) \sqrt{\frac{1}{2} \left(\frac{W}{L}\right)_1 \left(\frac{W}{L}\right)_3}$$

$$A_v = \mu C_{ox} (V_{cont} - V_T) \sqrt{\frac{1}{2} \left(\frac{W}{L}\right)_1 \left(\frac{W}{L}\right)_3} R_D$$

From the equation above, we can see the gain can be linearly controlled by V_{cont}. And the circuit only operate with positive by V_{cont}.

3.6 Simulated results of the receiver front-end

The LNA discussed in 3.1 is adopted as the first stage and followed by a conventional double-balanced Gilbert cell. The LO signal is generated ideally in ADS, and it can be further implemented with a quadrature voltage-controlled oscillator (QVCO) and phase-

locked loop (PLL) to meet the communication system specifications. A typical bias-T circuit is implemented as the output buffer to ease the matching for the output port. Fig. 3-13 shows the schematic of the proposed receiver front-end.

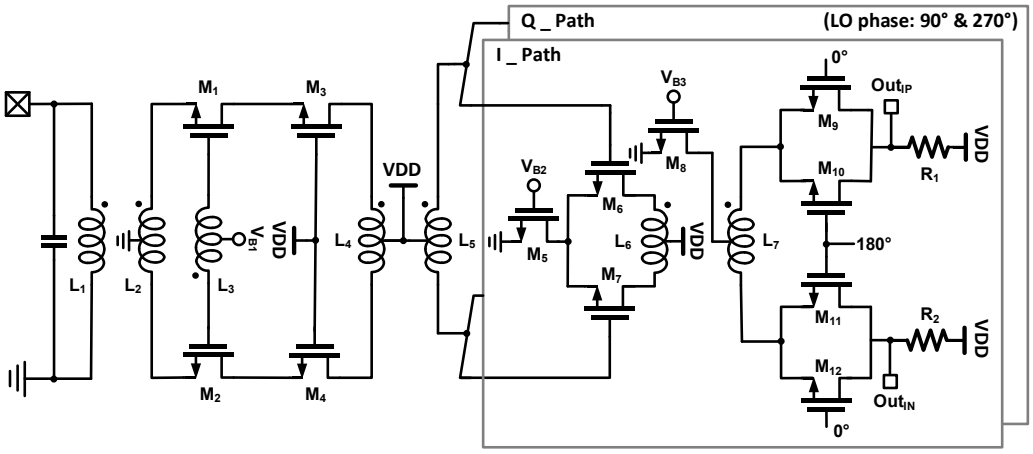


Fig. 3- 13 Circuit schematics of proposed receiver front-end

The proposed receiver front-end implements 40-nm CMOS with 0.9V V_{DD} for simulation. All the circuit simulation part is designed and simulated in ADS and Cadence. Fig. 3- 14 shows a schematic of the output buffer in cadence view. And it can be linked to ADS as a symbol for system level simulation.

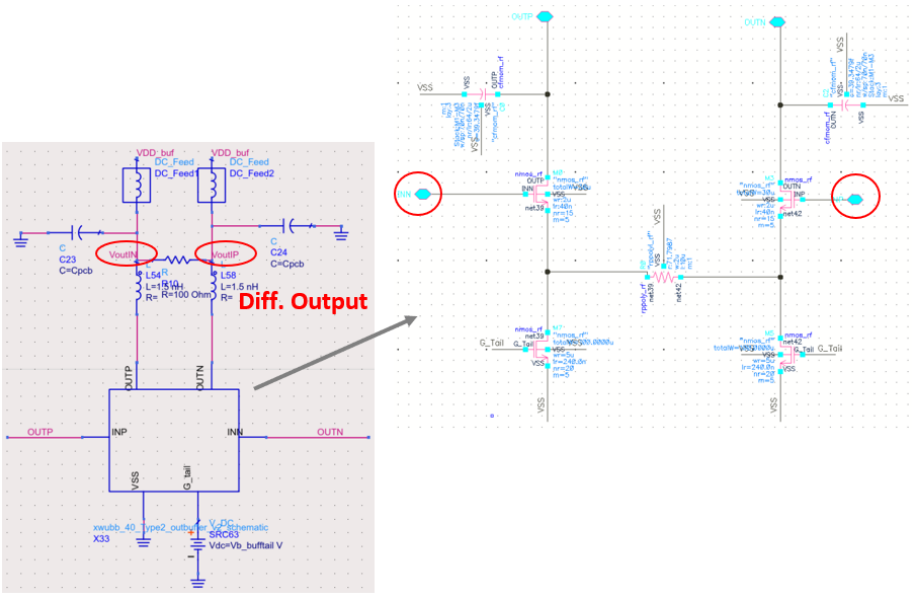


Fig. 3- 14 schematic of the output buffer in Cadence view.

The electromagnetic simulation for receiver front-end is done by EMX. And the detailed simulation considerations for layout will be discussed in the next chapter. Fig. 3- 15 shows the floorplan of the proposed receiver front-end. The layout is highly symmetric with the input signal flows in from the most left-hand side and the output signal flow to the right.

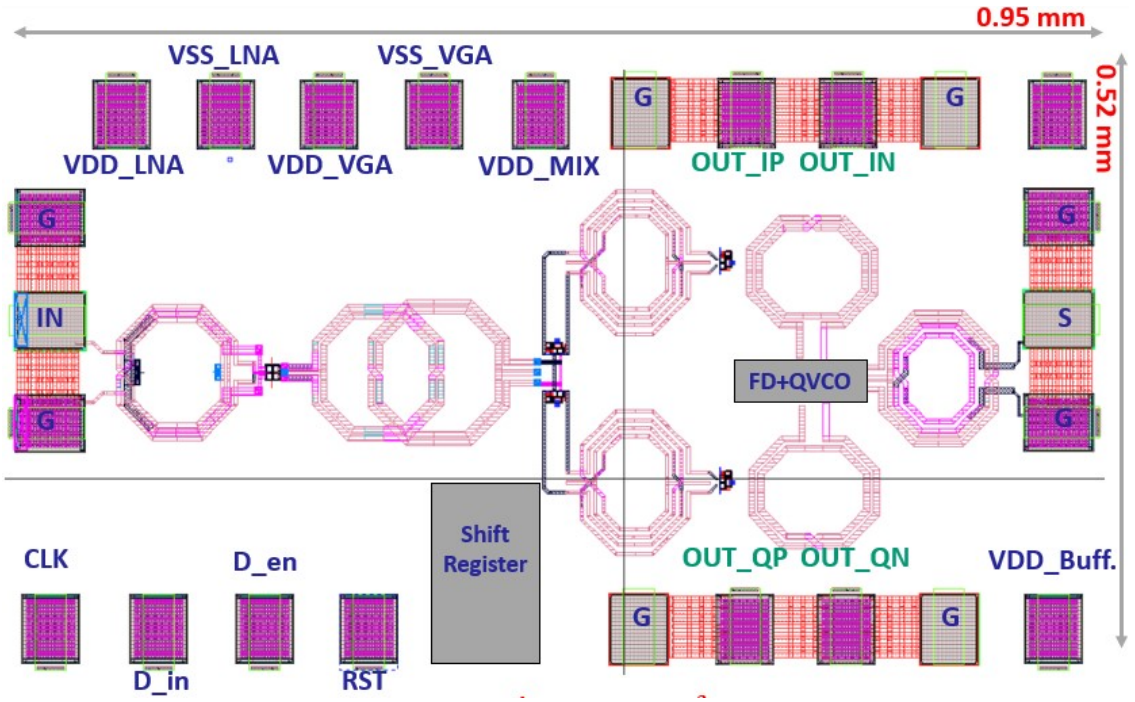


Fig. 3- 15 Floorplan of proposed receiver front-end

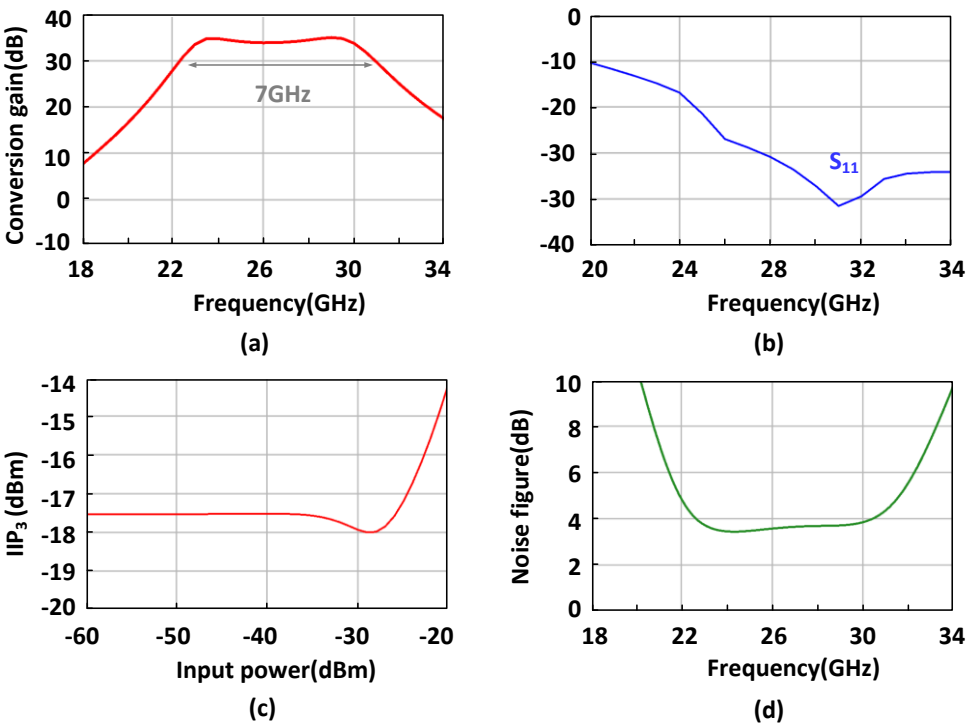


Fig. 3- 16 Simulated results of the proposed receiver front-end: (a) Gain, (b) Input matching condition, (c) IIP3, and (d) noise figure

Fig. 3- 16 shows the simulated results for the proposed receiver front-end. The receiver front-end has a peak gain 35 dB at 29 GHz with 3dB bandwidth from 23 GHz to 30.5 GHz. Within the 7.5 GHz RF bandwidth, the input return loss, which shown in Fig. 3-16 (b) remains below -10 dBm. A good input matching is achieved successfully within the desired bandwidth. Noise figure is shown in Fig. 3-16 (d). The minimum noise figure is 3.4dB at 24GHz, and the value remains to be lower than 5dB within the 3dB bandwidth. Besides, A two-tone simulation with a 10MHz separation at 27 GHz is performed to check the linearity. According the simulation as shown Fig. 3- 16 (c), IIP3 is -17dBm. The mainly degradation of linearity is caused by the mixer part. The linearity of the LNA is shown in Fig. 3- 17 with the output loading considered as the input of the VGA. One way to improve the overall linearity is to decrease the gain or increase the power consumption of the output buffer. Mixers with linearity improvement technique can also be considered for the future work.

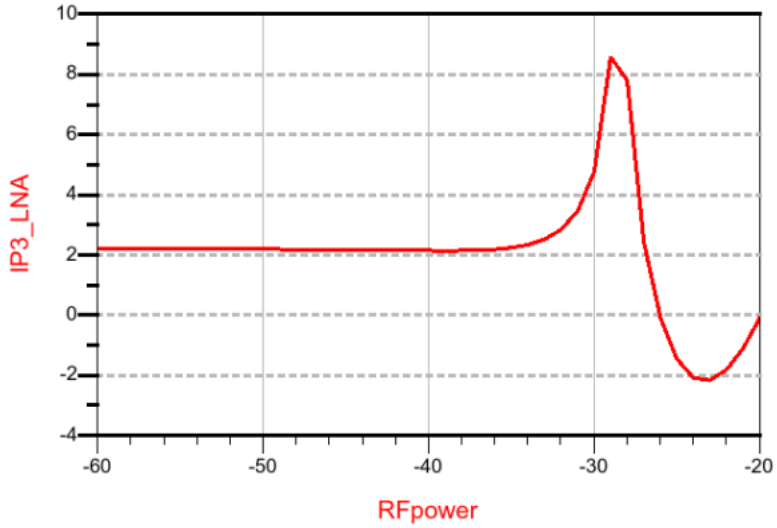
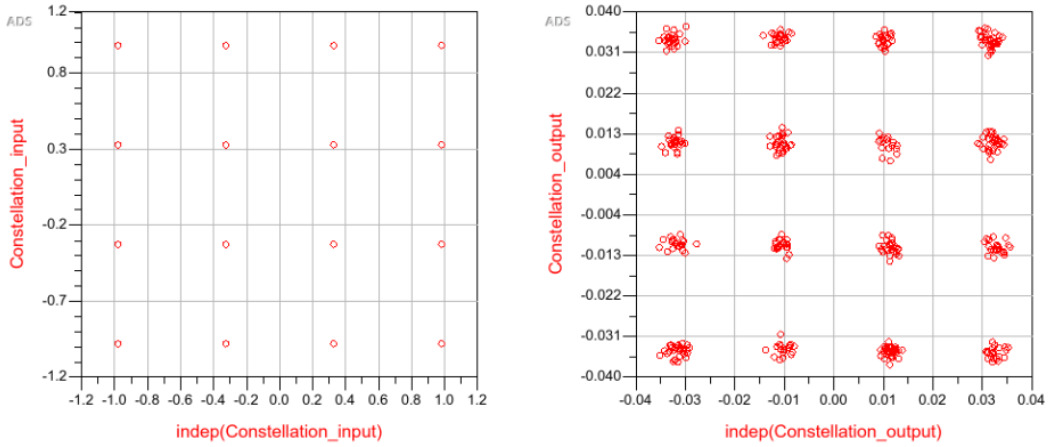
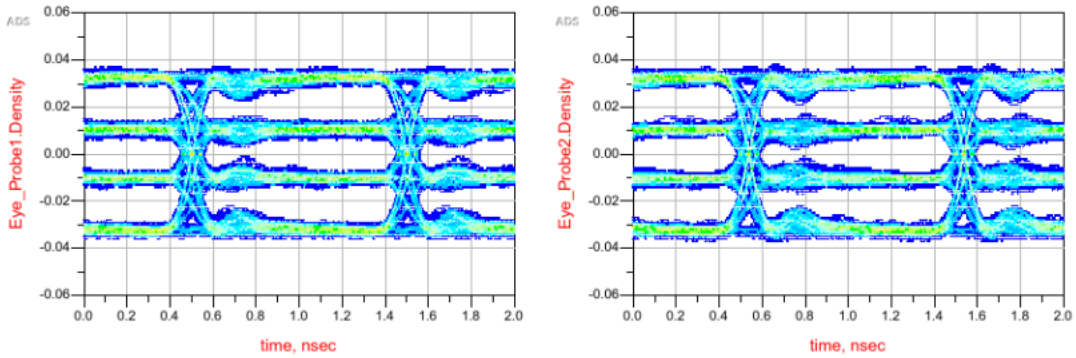


Fig. 3- 17 Simulated results for the IIP3 of the LNA

To evaluate the receiver front-end performance, 16-QAM and 64 QAM signal are implemented to see check the constellation, eye-diagram, and EVM. Fig. 3- 18 shows the constellation and eye-diagram with 16-QAM input signal. The RF input power is -50dBm. Then, the EVM for the output constellation is 4.7 %.



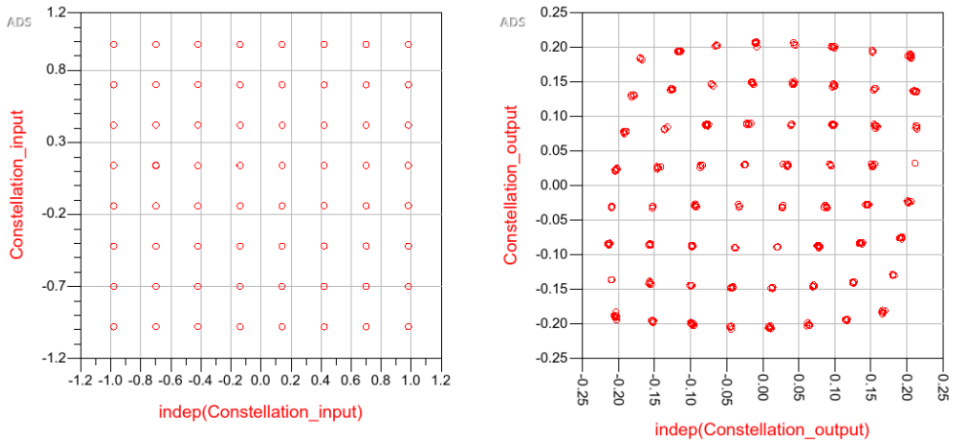
(a) (b)



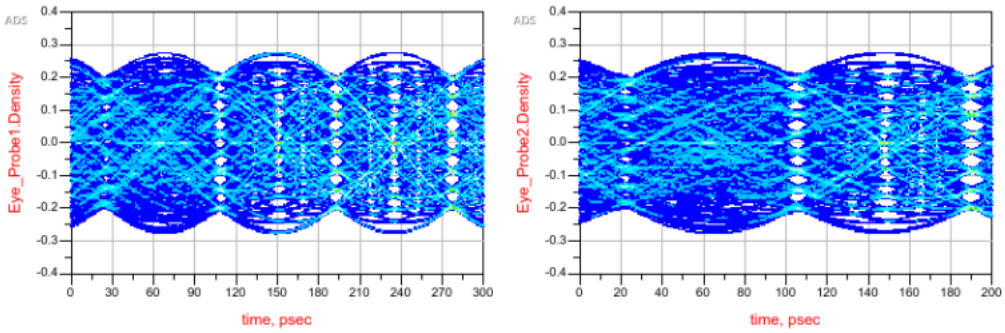
(c) (d)

Fig. 3- 18 Simulated results of (a) constellation for the input 16-QAM signal, (b) output constellation, (c) I-path eye-diagram, and (d) Q-path eye diagram

Fig. 3- 19 shows the constellation and eye-diagram with 64-QAM input signal. The RF input power is -40dBm. Then, the EVM for the output constellation is 2.7 %. And the eye-diagram for I-path and Q-path is shown in (c) and (d) respectively.



(a) (b)



(c) (d)

Fig. 3- 19 Simulated results of (a) constellation for the input 64-QAM signal, (b) output constellation, (c) I-path eye-diagram, and (d) Q-path eye diagram

3.7 Conclusion

This chapter describes the analysis of the circuit implementation of mm-wave receiver front-end. The performance and design considerations of the LNA, mixer, and VGA has been discussed in previous sections. The gain, matching condition, linearity, and noise figure are simulated to check the receiver performance. Besides,16-QAM and 64-QAM signals are implemented to check the eye-diagram and constellation.

Chapter 4

EM Simulations

This chapter describes the steps and considerations for electromagnetic simulation with EMX.

The chapter starts with the design details of the triple coupling input transformer and continues with the explanation of steps to build the equivalent circuit model. Layout considerations for receiver front-end are also included.

EMX is an accurate and efficient 3D full-wave Electromagnetic simulator developed by Integrand Software [55]. It can used to simulate the high-frequency, RF, and mixed-signal IC. EMX integral equation solver uses a very accurate representation of Maxwell's equations. It features:

- 3D conductors and vias
- true volumetric currents to accurately account for skin effect
- accurate sidewall capacitances
- layered and lossy substrate effects
- substrate and inter-component coupling.

4.1 Inductor simulation

The naming of the ports for the custom device needs to match the naming and the order of the ports for the EMX models. The port names and order of EMX custom devices can be found in —EMX models in the symbol view. For this

example, we can use a center-tapped inductor with four ports PLUS, MINUS, TAP and GND and the pin layers need to be marked accordingly. Pins have an orientation which can describe the current flow and these need to be set appropriately as shown in Fig. 4- 1.

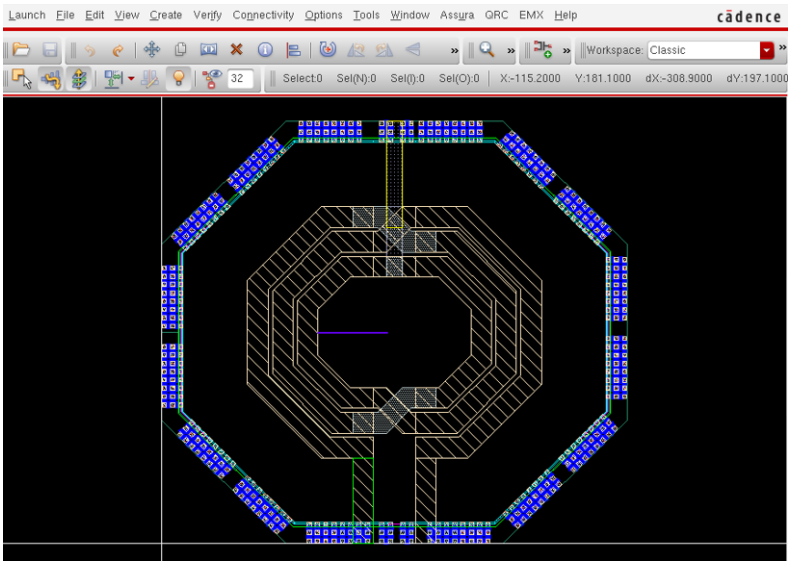


Fig. 4- 1 Simulated results of (a) constellation for the input 64-QAM signal, (b) output constellation, (c) I-path eye-diagram, and (d) Q-path eye diagram

Then we need to add pins for 4 ports of this inductor for EM simulation. Such as, PLUS, MINUS, TAP, and GND. The pins need to be created on the metal layer where they are located. Fig. 4- 2 shows the settings as below:

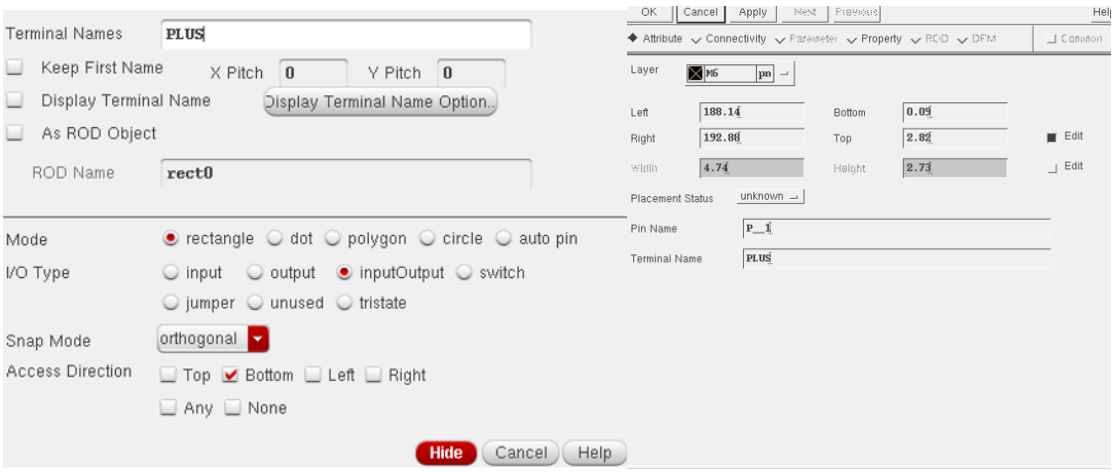


Fig. 4- 2 Settings for pins of the inductor

The pins need to be located near the edge of the layout as shown in Fig. 4- 3.

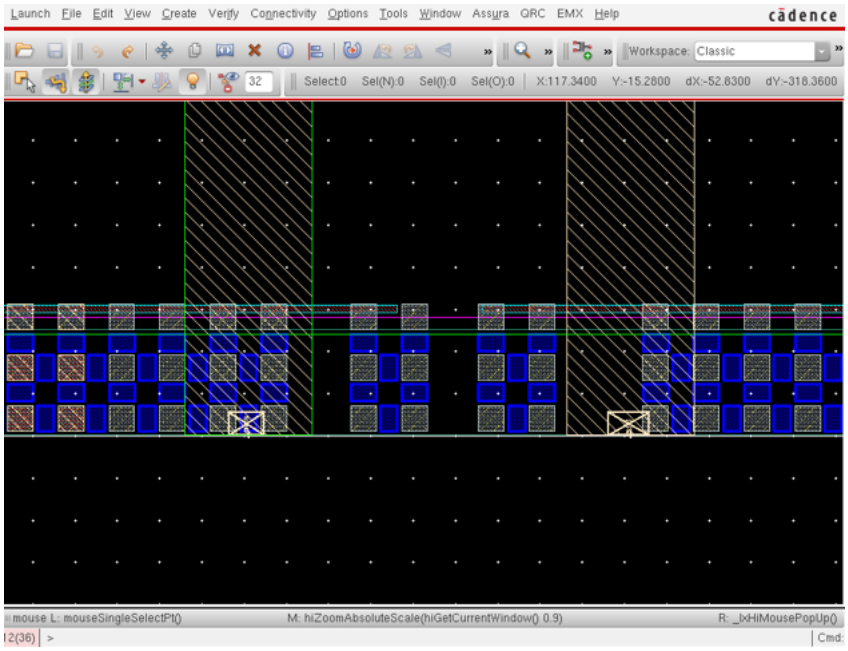


Fig. 4- 3 Location of the pins

Then we can run EMX and create models and generate a symbol and schematic

view for Spice level simulation. Choose Layout – EMX – Simulate. This will pop up the EMX GUI interface in Fig. Choose the TSMC process file. Fill in the signal fields “PLUS MINUS TAP” to identify the signal ports. Fill in the ground field “GND” to identify the ground port. For model type choose, we can use “N=port” or “Center-tapped-inductor (common-mode)”. The setting details are shown in Fig. 4- 4. Besides, other settings can be applicable for different design targets. The format of the output file can be changed, such as “Touchstone” or “Spectre” for compatibility consideration.

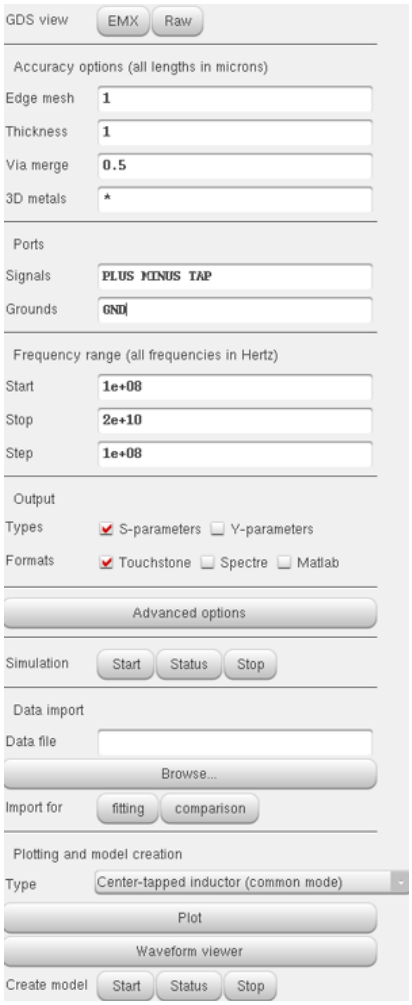


Fig. 4- 4 EMX GUI settings for inductor

EMX uses TSMC’s iRCX technology file for simulation. The technology file is

converted to the EMX.proc format by a parser. This parser is provided by Integrand and is provided on request by the user. The technology file can be viewed using EMX. EMX can also be used for half node simulation by using scaling factor in the EMX option of the advanced menu. Then we can see the GDSVIEW to check the layout and pin labels for simulation. Fig. 4- 5 shows an example of the GDSVIEW of a inductor.

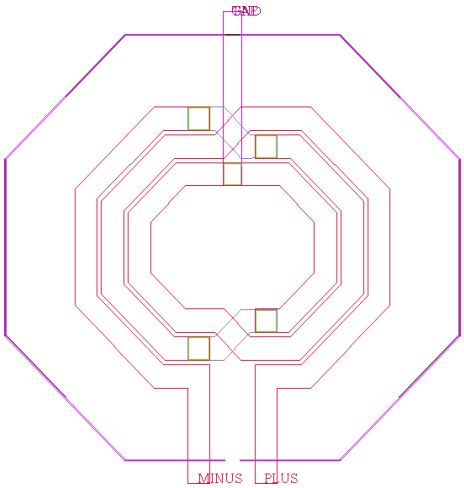


Fig. 4- 5 GDSVIEW of the simulated inductor

After the simulation is run the model is generated. Then the symbol and schematic view are also generated. The model playback should agree well with the EMX simulation. Fig. 4- 6 shows the inductance “L” and quality factor “Q” comparison between inductor simulation results and the SpiceModel datasheet.

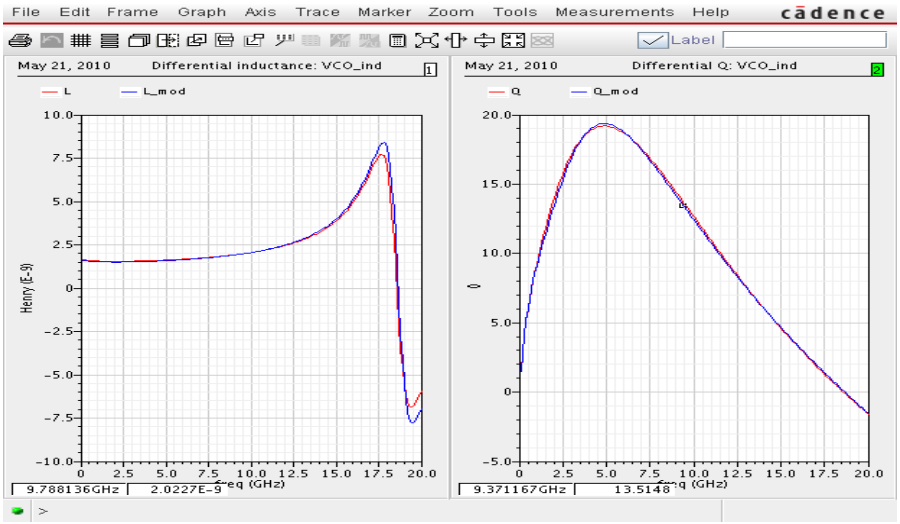


Fig. 4- 6 Comparison between inductor simulated results and Spice Model

4.2 Three coil input transformer and equivalent circuit model

With the design experience above. Fig. 4- 7 shows the layout of the proposed three-coil transformer. The Q-factor of inductors are preferred to be higher, so the parasitic series resistance needs to be smaller. Then the top thick metal layers (M_{10}, M_9) are primarily chosen for inductor main body, and the lower metal layers (M_8, M_7) are only employed for the crossovers. The size of the three-coil transformer is comparable to a conventional two-coil transformer, because three inductors overlapped with each other. The gain enhancement factor "A" can be controlled by adjusting the ratio of turns between L_3 and L_1. Besides, the magnetic coupling between L_2 and L_3 should be anti-phase to provide an inverting gain for gm-boosting. L_1 and L_2 have smaller inductance compared with L_3. So only one turn coil is used for L_1 and L_2. A two-turn coil is implemented for L_3. Fig. 4- 7 (b) shows the simplified equivalent differential circuit model of the three-coil transformer. The initial values of the parasitic components can be obtained by the model fitting function in the EMX software. And the values are listed in Fig. 4- 8 (a). One of the reasons for finding the equivalent model is to save the iteration time. The values for the parasitic components can be assumed to be unchanged when tuning the inductance value. Then, if

the inductance needs to be changed at the design stage, it saves the time to redo the layout and redo the EM simulation. The parameters can be easily controlled in the equivalent model. When the inductance is confirmed, then the layout and EM simulation can be done as the last step. Another reason is for the time-domain simulation. EM simulation provides S-parameter results, and it is not applicable to time-domain simulation. Equivalent models are stable and passive, so it can ensure that the noise behavior is correct. To find the component values inside the equivalent model, Z-parameters are used to do the comparison. As shown in Fig. 4- 8 (b), (c), and (d), Z-parameters of the layout and the equivalent model are well matched. The simulated inductances and coupling factors are shown in Fig. 4- 9. At 28 GHz, the inductances, which include self-inductance and mutual inductance, of L_1, L_2 and L_3 is 558 pH, 395 pH and 1.39 nH, respectively. The coupling factors, K_{12}, K_{13} and K_{23} is 0.76, 0.75 and 0.82, respectively. The size of the three-coil transformer is 182 × 141 um^2.

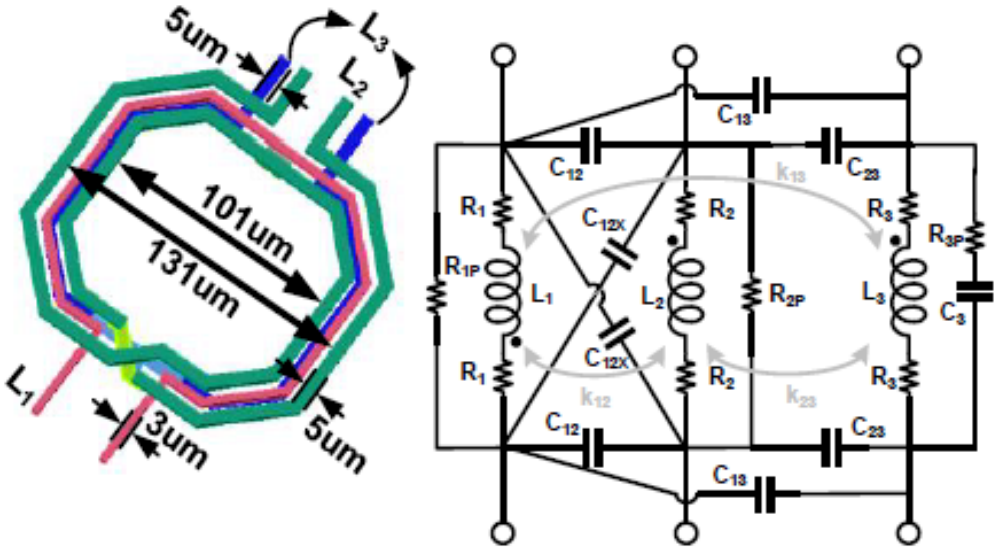


Fig. 4- 7 Three-coil transformer: (a) 3-D view (b) simplified equivalent differential circuit model

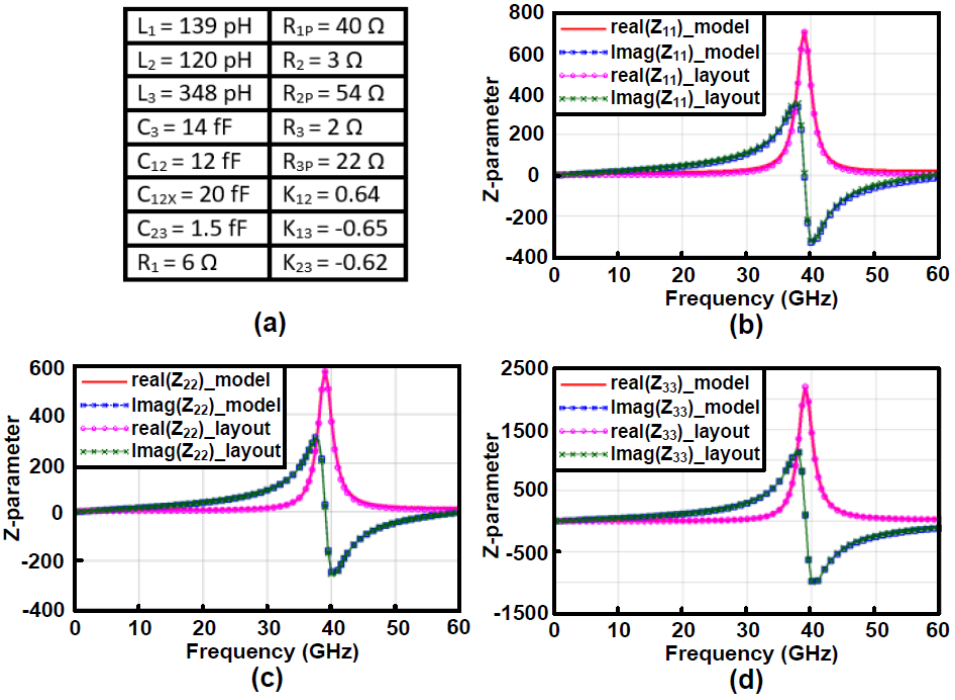


Fig. 4- 8 Equivalent differential circuit model: (a) values of components (b) comparison of Z_{11} (c) comparison of Z_{22} (d) comparison of Z_{33}

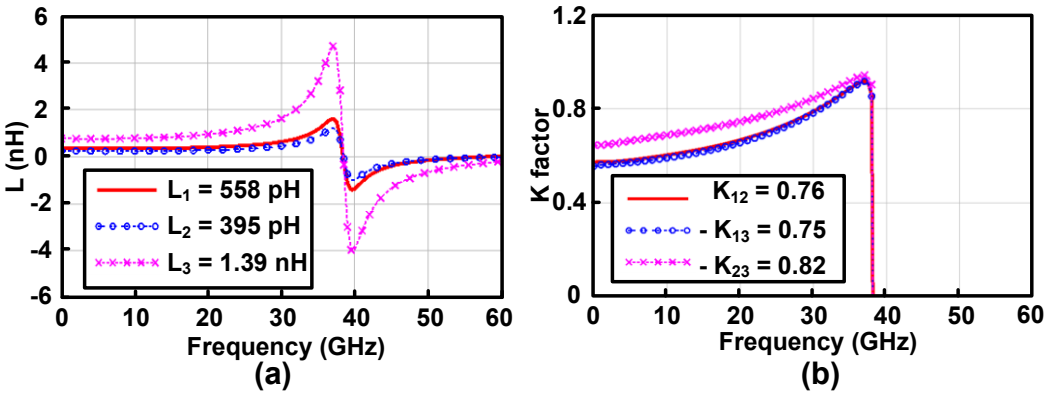


Fig. 4- 9 Simulated results of the tree-coil transformer: (a) inductance, and (b) coupling factor between each of the two coils

4.3 Receiver front-end layout considerations

Based on the design experience in LNA. The most size consuming parts for the mm-wave receiver IC are the transformers. So, the optimization needs to be done by adjusting the coupling factor between two inductors and the Q factor of each inductor itself. For high frequency inductor design, the tradeoff between the size and self-resonance frequency also needs to be considered. When the layout of the turns for the inductor increases, the size of the inductor itself decreases. However, it leads the self-resonance frequency becomes lower. So, before integrating two inductors to form a transformer. Each of them is preferred to be design with a higher self-resonance frequency. Because when two inductors combine to form a transformer, the magnetic coupling between these two inductors will change the characteristic for both. Usually, the self-resonance frequency will decrease further. And the inductance will increase due to the coupling. One way to solve this tricky problem is to skew the center of two inductors. The layout of the main parts in the receiver front-end is shown in Fig. 4- 10. The two inductors which forms the transformer between the LNA, and VGA has different center point. Then the coupling factor can be reduced, and the bandwidth of the receiver font-end will not be limited. Besides, the distance between two different transformers also needs to be optimized to make sure they do not have undesired coupling effect. Table 4- 1 shows the list of pads used in the layout.

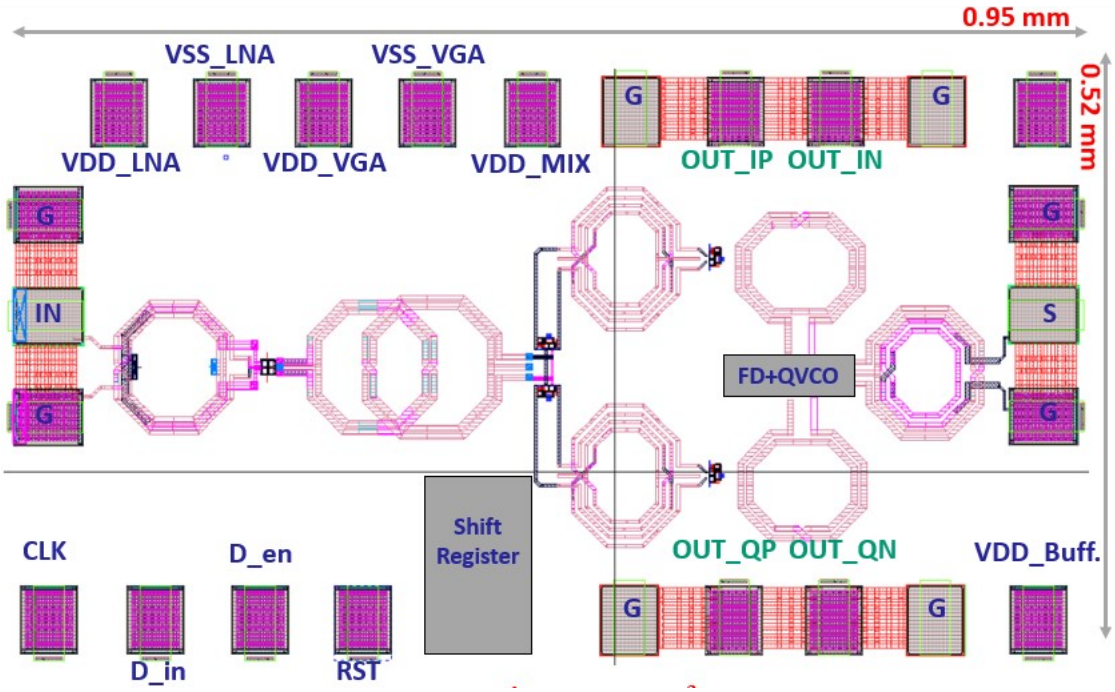


Fig. 4- 10 Layout of the proposed receiver front-end

Type	Function	Pad name
Digital signal	Shift register	CLK
		D_in
		D_en
		RST
GSG	RF input	GSG_in
	LO input	GSG_lo
Analog signal	Baseband I	OUT_IP
		OUT_IN
	Baseband Q	OUT_QP
		OUT_QN
	FD+QCVO	TBD

Type	Function	Pad name
Power pin	LNA power	VDD_LNA
		VSS
	VGA power	VDD_VGA
		VSS
	MIX power	VDD_MIX
		VSS
	ILFD power	VDD_FD
		VSS
	Buffer power	VDD_BUF
		VSS

Table 4- 1 List of pads

4.4 Conclusion

This chapter mainly focuses on the discussion of receiver front-end layout considerations for EM simulations based on the EMX. Start with the simple simulation for inductor, the triple coupling input transformer, and the layout for the receiver front-end has also been discussed step by step.

Chapter 5

Performance Evaluation in Co-simulation Platform

This chapter describes the performance evaluation of the proposed receiver front-end with the mixed-mode co-simulation platform. The simulated results is shown on the GUI in MATLAB.

A graphical user interface (GUI) was constructed in MATLAB to in/out simulated files between MATLAB and ADS/Cadence dynamically as discussed in chapter 2. To validate the proposed receiver front-end, 16-QAM OFDM modem in MATLAB is used for BER and constellation check.

5.1 Receiver front-end

The baseband 16-QAM OFDM signal is generated in MATLAB as discussed in the previous chapter. In this case, the number of sub-carriers is 256, frame number is 50 with 1GHz bandwidth. The total sampling point number is 57560. And the simulation time for circuit part in ADS is 2 hours. These parameters can be changed according to different specifications on the left-hand side in the GUI. After the signal passes through the receiver front-end, which simulated in ADS, then the output baseband OFDM signal can be demodulated in MATLAB. And the demodulated signal characteristics are shown on the right-hand side in the GUI. The signal bandwidth is 1GHz, and the data rate is 3.765 Gbps. Both the BER and FER are zero with 3.815 % EVM. The subcarrier index can be changed

to see the signal performance for different subcarrier. Fig. 5- 1 shows the OFDM signal modem GUI for proposed receiver front-end.

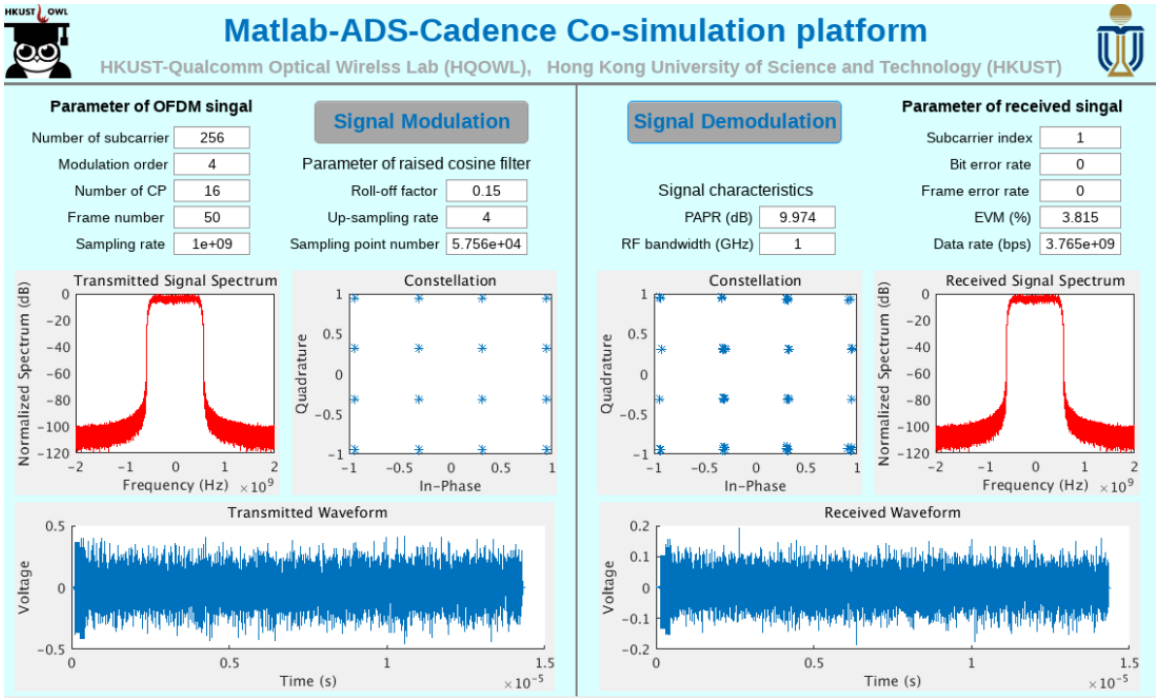


Fig. 5- 1 OFDM signal modem GUI for proposed receiver front-end

In this co-simulation, 10 prefixes are utilized to synchronize the transmitted and received baseband signals. Fig. 5- 2 shows the simulation results of the synchronization. Ten peak correlation values clearly appear. This means the demodulation can find the actual start time of the received baseband signal accurately.

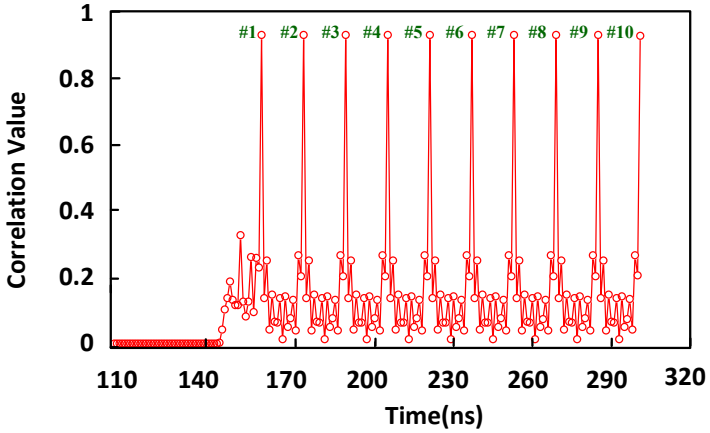


Fig. 5- 2 The correlation value of the synchronization in the demodulation process

The input signal spectrum for the direct-conversion receiver front-end is shown in Fig. 5- 3. According to recent publications, the gain for PA in transmitter is set to be 20 dB. With loss considered in the channel, the average input power of the receiver front-end is -44 dBm. This value can be controlled by adjusting the behavior circuit blocks for the transmitter and the channel.

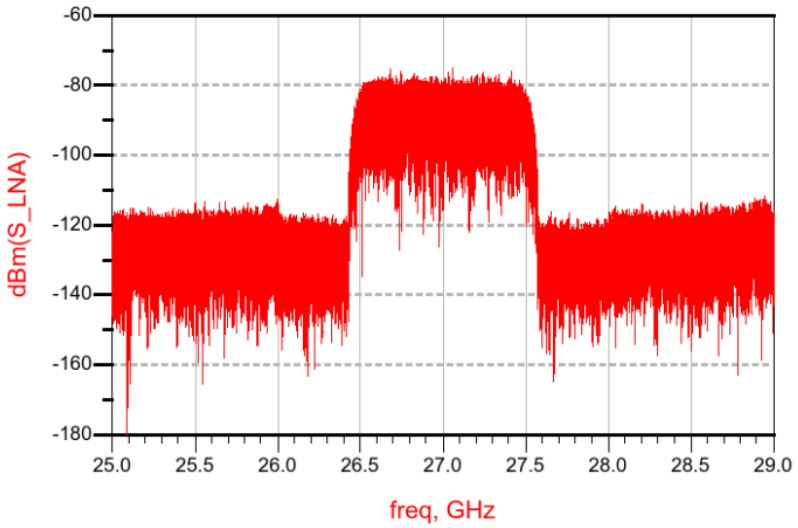


Fig. 5- 3 The input spectrum for the direct-conversion receiver front-end

5.2 Parameter setting for other behavior models

As discussed in chapter 2, the circuit blocks in the transceiver system are based on the behavior models. For different design target, the behavior models can be changed to schematic or post simulation files to support the design from system specification level to actual circuit implementations. The circuit part for the proposed platform contains common circuit blocks inside transceiver, as well as a simple model for the channel between transmit antenna and receive antenna. The parameters of all behavior circuit blocks can be controlled easily. And actual designed circuit can be further implemented inside to replace behavior blocks for different design target. The MATLAB GUI can be

customized to control the parameters of the models in the circuit (which simulated in ADS) directly. Fig. 5- 4 shows that the "Data Access Component" in ADS can help to link the GUI with the models in ADS. Then by setting the "VAR" in ADS accordingly, the desired variables of the ADS Models can be changed directly in GUI.

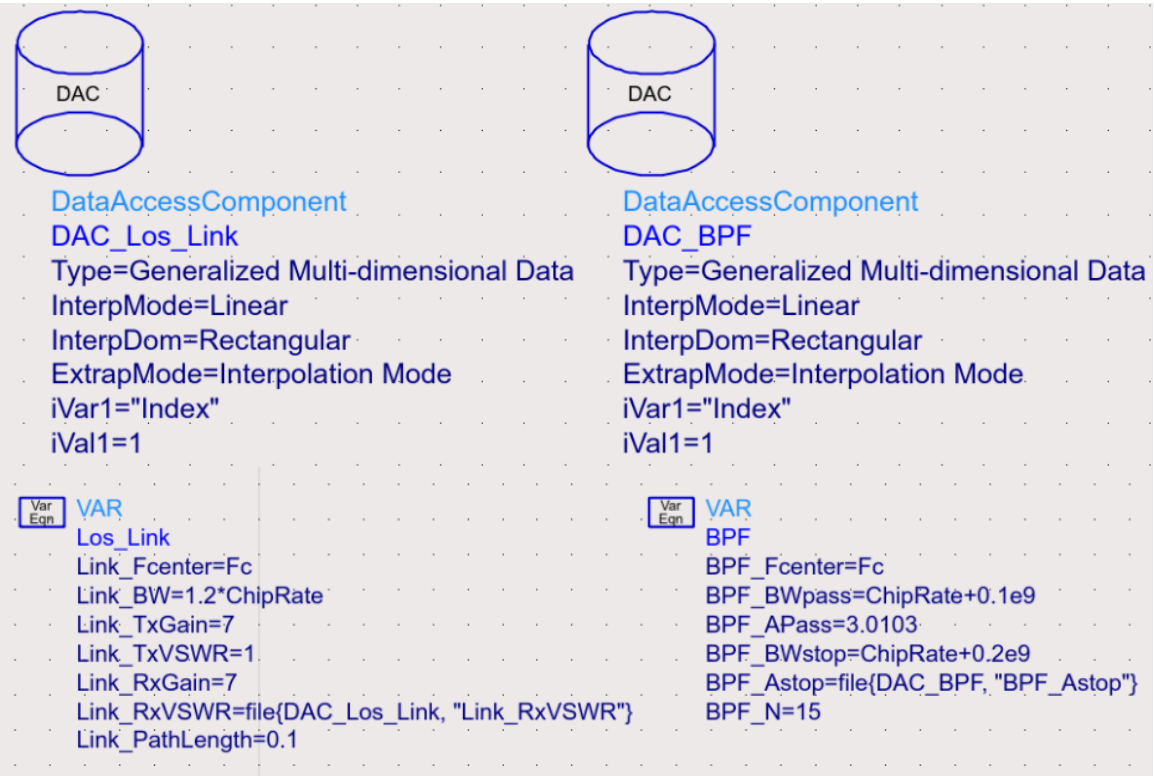


Fig. 5- 4 Parameter controllers for behavior models in the transceiver system

5.3 Conclusion

This chapter shows the performance evaluation of the proposed receiver front-end with the mixed-mode co-simulation platform. Not only for the receiver front-end, this mixed-mode co-simulation platform can be implemented for the whole transceiver system design. And the GUI can be modified accordingly depends on the different design targets.

Chapter 6

Conclusion and Prospective

Based on the development of the 5G communication networks. This thesis focuses on the design of a mixed-mode co-simulation platform for broadband mm-wave receiver IC design. The co-simulation platform is based on MATLAB, ADS, Cadence and EMX to support the receiver front-end design from system specification to circuit implementation. For the receiver front-end design, the work focuses on developing a low noise amplifier (LNA) in the 24-32 GHz to meet the gain, noise figure, linearity, bandwidth, and area requirements, simultaneously. A novel compact three-coil transformer is employed to perform single-ended to differential conversion, broadband input matching, gm-boosting, and noise suppression at the LNA input. The proposed LNA is further integrated with mixer, variable gain amplifier (VGA) and the output buffer to form a broadband receiver front-end at 28GHz to support high data rate communication system. Each of the circuit blocks in the proposed receiver front-end is detailed discussed in the previous chapters. The performance for the post-simulation of the proposed receiver front-end is evaluated by the mixed-mode co-simulation platform.

The future work can be focused on the LO signal generation circuit design, or the mm-wave transmitter design. The typical behavior models for the transceiver front-end are built in ADS as discussed in chapter 2 and chapter 5 to realize the transceiver IC design from system specification to circuit implementations.

List of Figures

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