Digital Baseband Design Utilizing Advanced Modulation Scheme for Visible Light Communication System

by

Jian KANG

A Thesis Submitted to
The Hong Kong University of Science and Technology
in Partial Fulfillment of the Requirements for
the Degree of Master of Philosophy
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April 2021, Hong Kong

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Abstract

In recent years, with the development of new technologies like smart driving, internet of things, and virtual reality, wireless communication systems with excessive data transfer capacity are increasing needed. For conventional radio frequency (RF) communication systems, spectrum congestion has become the biggest bottleneck for increasing the transmission speed. Therefore, visible light generated by light emitted diodes (LEDs) or laser diodes (LDs) is employed for high-speed data transfer. This is called visible light communication (VLC). Simultaneous illumination and data transmission, unlicensed visible light spectrum, low cost for the frontend, and radio sensitive environment applications are the advantages of VLC compared to traditional RF communication. The wide use of LEDs has further promoted the application of VLC technology.

The bandwidth limitation of LEDs limits the improvement of VLC systems. Various techniques applied to hardware and algorithms have been developed to increase the data transfer capability. For example, The VLC system bandwidth can be significantly extended by employing pre-equalization and post-equalization in both the time and frequency domain. In addition, advanced modulation schemes, such as pulse amplitude modulation (PAM), carrier-less amplitude phase (CAP) modulation and orthogonal frequency division multiplexing (OFDM), can be utilized to improve the spectrum efficiency. In this thesis, we

design and implement circuits of the digital baseband, utilizing advanced modulation schemes and supporting equalization technologies.

The first work presents a real-time visible laser light communication (VLLC) system with a baseband design in a field programmable gate array (FPGA) platform using an 8B/10B encoding and non-return-to-zero on off keying (NRZ-OOK) modulation scheme. Based on the proposed system, a video can be transmitted through the system at a data rate of 500 Mbps over a 2-meter distance in real-time.

The second work presents a novel RGB PAM-4 transceiver employing a digitally-controlled asymmetric feed forward equalizer (FFE) and cascaded continuous time linear equalizer (CTLE). The PAM-4 signal with a one-tap FFE is composed of six OOK signals with different delays in the optical domain. Delay control is implemented in the digital baseband and no digital-to-analog converter (DAC) is needed in the system. The transceiver achieves a 250% increase in the bandwidth extension ratio in the VLC links using ordinary RGB LEDs by allowing independent PAM-4 eye-height tuning.

The third work designs and implements a VLC transmitter baseband circuit supporting OFDM with bit and energy allocation (BEA) on an FPGA. The training sequence and the pilot subcarrier are also added for frame synchronization, symbol synchronization, channel estimation, and sampling offset compensation. The test result shows that the transmitter can generate the OFDM signal supporting BEA and the signal can be synchronized and demodulated. Compared with modulation with a fixed bit number and energy on each subcarrier, the proposed transmitter increases the data rate from 15 to 20.5 Mbps when the bit error rate (BER) equals 3×10^{-3} and transmission distance is 0.3 m.

Dedicated to my family

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I spent an unforgettable four years at the Hong Kong University of Science and Technology. I cannot forget the freshness and happiness of coming to Hong Kong for the first time, the excitement of the first successful experiment, and the sense of accomplishment when my first article was accepted. I have gradually grown up and become a graduate student who can experiment independently and write articles independently.

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CHAPTER 1. BACKGROND AND MOTIVATION

1.1 Research Background

With the development of the Internet of things (IoT), artificial intelligence (AI) and high-definition display technology, excessive data transfer capacity is needed. Much of the internet transmission at the backbone is handled by optical fiber infrastructure that can achieve data speeds in the order of Tbps [1]. However, wireless communication is needed to solve the final problem from data center to terminals or terminals to terminals. Radio frequency (RF) is the most commonly used component of the electromagnetic spectrum for wireless communication due to its broad area coverage and small interference [2]. Spectrum congestion has become a bottleneck of conventional RF communication, which uses sub 30 GHz frequency. The millimeter waveform, whose frequency ranges from 30 to 300 GHz, is a trending solution of the next generation wireless communication. But there are also some limitations, such as high cost for precision manufacturing components, limited communication range due to atmospheric attenuation, reduced range capability in adverse weather and so on [3]. The optical spectrum is considered to be a promising solution for the development of future high-density and high-capacity networks. Wireless connectivity based on the optical spectrum including visible light, infrared and ultra-violet is termed optical wireless communication (OWC) [4]. Visible light communication (VLC), light fidelity (LiFi), optical camera communication (OCC), free space optical communication (FSOC) and light detection and ranging (LiDAR) are different OWC technologies, which are used in different application scenarios.

VLC uses visible light generated by light emitted diodes (LEDs) or laser diodes (LDs) as the light source for high-speed data transfer. There are certain advantages of VLC compared with traditional radio frequency communication. First, LEDs can be used for both illumination and wireless transmission simultaneously, and the output power is not a constraint for the employment of high-order modulation schemes. Second, the visible light spectrum is unlicensed and is currently largely used for communication [5]. Third, the frontend structure of both the transmitter and receiver is simple because of the intensity modulation and direct detection (IM/DD) usage. VLC can also be used in some radio sensitive environments, like underwater and in hospitals [6, 7]. In recent years, LEDs have been widely used because of they have high energy-efficiency, high luminescence and a long-life span. This has further promoted the application of VLC technology [8].

1.2 Motivation

Communication by flame from board sentry stations to distant command offices on the Great Wall in ancient China is the earliest VLC system [9]. Nowadays, the flame has been replaced by LEDs or LDs, and people's eyes have been replaced by the photodetectors (PDs). Information is modulated in the light by the transmitter and is recovered by the receiver from the light received by the PD. How to transfer more information in the limited time is the primary goal of VLC system design. Non-ideal factors such as bandwidth limitation, non-linearity, and noise brought by LEDs, PDs, the channel and so on limit the throughput of the whole system.

TABLE I. RESEARCH IN THE PERFORMANCE OF VLC SYSTEMS

	Mod. Scheme	**DR (Gb/s)**	**BW Extension**	**Dis. (m)**	**VLC Light Source**		**Year**
					Type	**BW (GHz)**	
[10]	OOK	0.08	EQ	0.1	P-LED	0.045	2008
[11]	OOK	0.1	EQ	0.1	P-LED	0.014	2009
[12]	OOK	0.614	EQ	0.45	Red LED	0.0068	2012
[13]	OOK	0.33	Current Shaping	11	Red LED	0.07	2013
[14]	OOK	0.5	EQ	1.6	P-LED	0.003	2014
[15]	OOK	R:0.60 G:0.52 B:0.66	EQ	0.15	RGB LED	R:0.0057 G:0.0053 B:0.0066	2014
[16]	OOK	4	No	0.2	Blue LD	2.6	2015
[17]	OOK	2.5	No	12	Red LD	5	2016
[18]	PAM-16	0.04	No	N/A	P-LED Array	N/A	2012
[19]	PAM-4	1.1	EQ	0.46	P-LED	0.02	2014
[20]	PAM-4	2	EQ	0.6	μLED	0.15	2016
[21]	PAM-8	1.5	EQ+DNN	1.2	Blue LED	N/A	2018
[22]	CAP	1.1	EQ	0.23	P-LED	N/A	2012
[23]	CAP	3.22	EQ	0.25	RGB LED	N/A	2013
[24]	CAP	1.8	EQ	50	RGB LED	R:0.15 G:0.1 B:0.125	2015
[25]	CAP	4.5	EQ	1.5	RGB LED	0.25	2015
[26]	CAP	8	EQ	1	RGBY LED	0.32	2015
[27]	OFDM	0.513	No	0.03	P-LED	0.035	2010
[28]	OFDM	0.803	No	0.12	RGB LED	0.015-0.020(a)	2011
[29]	OFDM	1.1	EQ+MIMO	1	P-LED	0.065	2012

[30]	OFDM	3.4	No	0.01	RGB-LED	N/A	2012
[31]	OFDM	0.225 0.575	No	0.66	P-LED RGB-LED	N/A	2012
[32]	OFDM	4.22	EQ	0.01	RGB-LED		2014
[33]	OFDM	5.6	No	4	RGBA-LED	N/A	2014
[34]	OFDM	2	EQ	1.5	P-LED	0.028	2015
[35]	OFDM	1.2	No	0.4	Red-LED	0.2	2016
[36]	OFDM	10.72	EQ	1	RGBYC-LED	0.3	2018
[37]	OFDM	15.73	No	1.6	RGBY-LED	N/A	2019

Various techniques applied to hardware and algorithms have been developed to improve VLC system performance. For example, The VLC system bandwidth can be significantly extended by employing both pre-equalization and post-equalization (EQ) in both the time and frequency domain. In addition, advanced modulation schemes such as pulse amplitude modulation (PAM), carrier-less amplitude phase (CAP) modulation and orthogonal frequency division multiplexing (OFDM), can be utilized to improve spectrum efficiency. TABLE I. lists some of research results in recent years. However, most of the previous research has been more concentrated on the algorithm itself. The transmitted signal is generated by MATLAB and transformed into the analog domain by an arbitrary waveform generator (AWG) as the signal source of the LED driver. All the signal processing is done offline.

This thesis focusses on real-time digital baseband design for VLC systems, utilizing advanced modulation schemes and supporting EQ technologies. It is not only an introduction to advanced algorithms, but also how to implement these algorithms on digital circuits.

1.3 Thesis Organizations

The thesis is divided into five chapters. Chapter 1 gives the background introduction and the research motivation. Chapter 2 introduces the principle and performance analysis of the modulation schemes used in the digital baseband in the thesis. Chapter 3 shows the two digital baseband designs employing OOK and PAM-4, separately. Chapter 4 illustrates OFDM digital baseband design with a bit and energy allocation algorithm (BEA). Chapter 5 draws conclusions and points out the direction for future research.

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CHAPTER 2. THEORETICAL BASICS OF VLC MODULATION

2.1 Introduction

In VLC systems, intensity modulation (IM) and direct detection (DD) are usually employed due to the non-coherent light emission of LEDs. Therefore, VLC modulation signals must be real and positive in order to support IM/DD. This is one main difference between RF wireless signaling and optical wireless (including VLC) signaling. Various VLC modulation schemes have been investigated.

On-off keying (OOK) is a binary modulation scheme applied in many low-complexity VLC systems, which, however, suffers low spectral efficiency. To deal with this issue, PAM can be employed to support multilevel transmission, but there is a tradeoff between the system complexity and the speed improvement. In particular, PAM containing more pulse levels can achieve higher data rates with higher vulnerability to device nonlinearity. Instead of modulating the amplitude, pulse position modulation (PPM) and its variants such as multiple PPM (MPPM) and differential PPM (DPPM) convey information through shifting the signaling pulses of each symbol in the time domain. PPM with a narrow pulse is suitable for power-efficient applications while scarifying the spectral efficiency.

The unique feature of orthogonal signaling can also be exploited to further increase VLC data rates. CAP is a spectrum efficient scheme that transmits two separate bit streams in parallel in the same channel through the employment of two orthogonal filters. As a variant of quadrature amplitude modulation (QAM), CAP can achieve similar performance but with simpler implementation. OFDM is another popular technique that leverages orthogonal signaling to support high-speed communication within a limited channel bandwidth. To generate real and positive signals, various optical OFDM schemes have been proposed, including DC-biased optical OFDM (DCO-OFDM), asymmetrically clipped optical OFDM (ACO-OFDM) and pulse-amplitude-modulated discrete multitone (PAM-DMT). Since Hermitian symmetry is required, only part of the subcarriers can be modulated to transmit information. Therefore, the spectral efficiency of optical OFDM is reduced compared to conventional OFDM. High complexity is another issue for the implementation of OFDM.

The principle and performance analysis of OOK, PAM and OFDM will be illustrated in this chapter as the theory foundation of the thesis work.

2.1 On-Off Keying Modulation

2.1.1 Principle of OOK

OOK is widely used in VLC systems due to the low design complexity in both the transmitter and the receiver. In OOK VLC systems, "1" is represented by an optical pulse, while "0" is represented by the absence of the pulse. If the duty ratio of the pulse is smaller than 100%, it is called non-return-to-zero (NRZ); otherwise, it is called return-to-zero (RZ). Fig. 1 depicts the modulated waveforms using NRZ-OOK and RZ-OOK, where P_{avg} is the average optical power of the transmitted VLC signal.

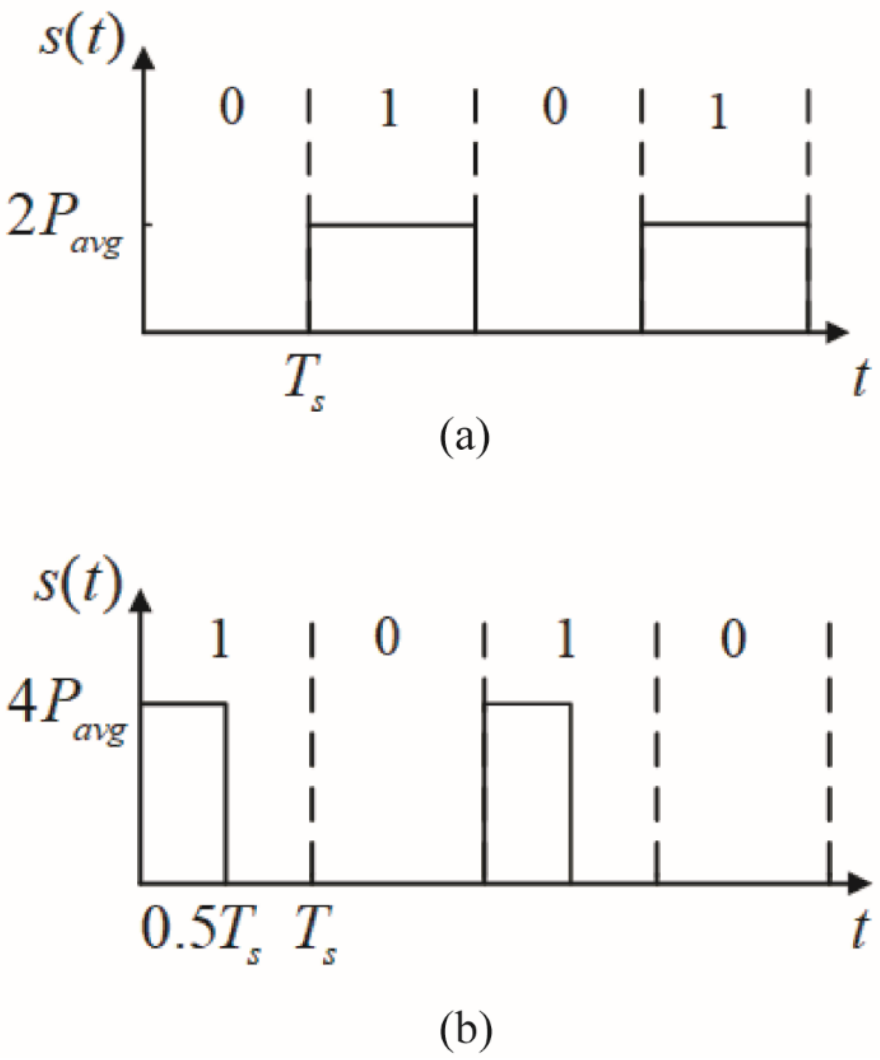

Fig. 1 Modulated waveform using (a) NRZ-OOK, and (b) RZ-OOK.

The modulated signal waveform can be expressed as Eq. (2.1):

$$s(t)_{OOK} = \sum_{k=0}^{K-1} s_m \times p(t - kT), \text{and } s_m = 0 \text{ or } 1, \tag{2.1}$$

where s_m is the bit sequence and $p(t)$ is the transmitter pulse shaping function.

2.1.2 Performance Analysis

A theoretic model for OOK VLC systems in an additive white Gaussian noise (AWGN) channel is illustrated in Fig. 2. Fading effect is ignored in this analysis.

Assuming NRZ-OOK is adopted, and a matched filter is employed in the receiver, the bit error rate (BER) of the system can be calculated as

$$P_e = Q\left(\sqrt{\frac{\varepsilon_b}{N_0}}\right) \tag{2.2}$$

$$Q(x) = \frac{1}{2}\operatorname{erfc}\left(\frac{x}{\sqrt{2}}\right) = \frac{1}{\sqrt{2\pi}}\int_x^{\infty} \exp\left(-\frac{u^2}{2}\right) du \tag{2.3}$$

$$2\varepsilon_b = i_s^2 T_s \tag{2.4}$$

$$\frac{N_0}{2} = \sigma_N^2 T_s \ , \tag{2.5}$$

where N_0 is the spectrum density of the channel noise, ε_b is the average bit energy, i_s is the received photocurrent, T_s is the symbol width, and σ_N^2 is the noise power.

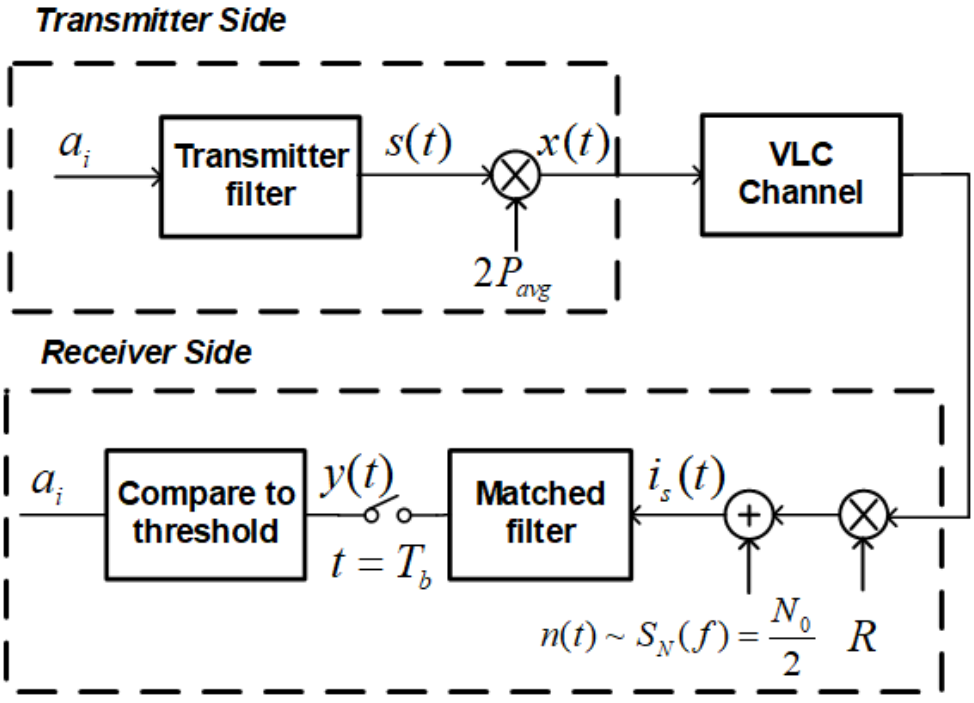

Fig. 2 Theoretic model of an OOK VLC system.

Based on the above equations, the way to improve the BER of VLC systems for a fixed data rate is either increasing the transmitted optical power or reducing the channel noise. In reality, the reduction of the channel noise can be achieved by suppressing the input-referred noise power of the VLC receivers.

2.2 Pulse Amplitude Modulation

2.2.1 Principle of PAM

To compensate for the limited LED bandwidth and improve the VLC data rates, various higher-order modulation schemes with increased spectral efficiency have been developed. Among these, PAM is a one-dimensional multilevel modulation scheme, meaning there is no complex-to-real conversion in the signal domain. In addition, PAM does not require Fourier transform (unlike OFDM). Therefore, the implementation complexity is relatively low. Since the transmitted VLC signal should be positive (because of intensity modulation), DC bias can be added into a bipolar PAM signal to generate a unipolar PAM waveform.

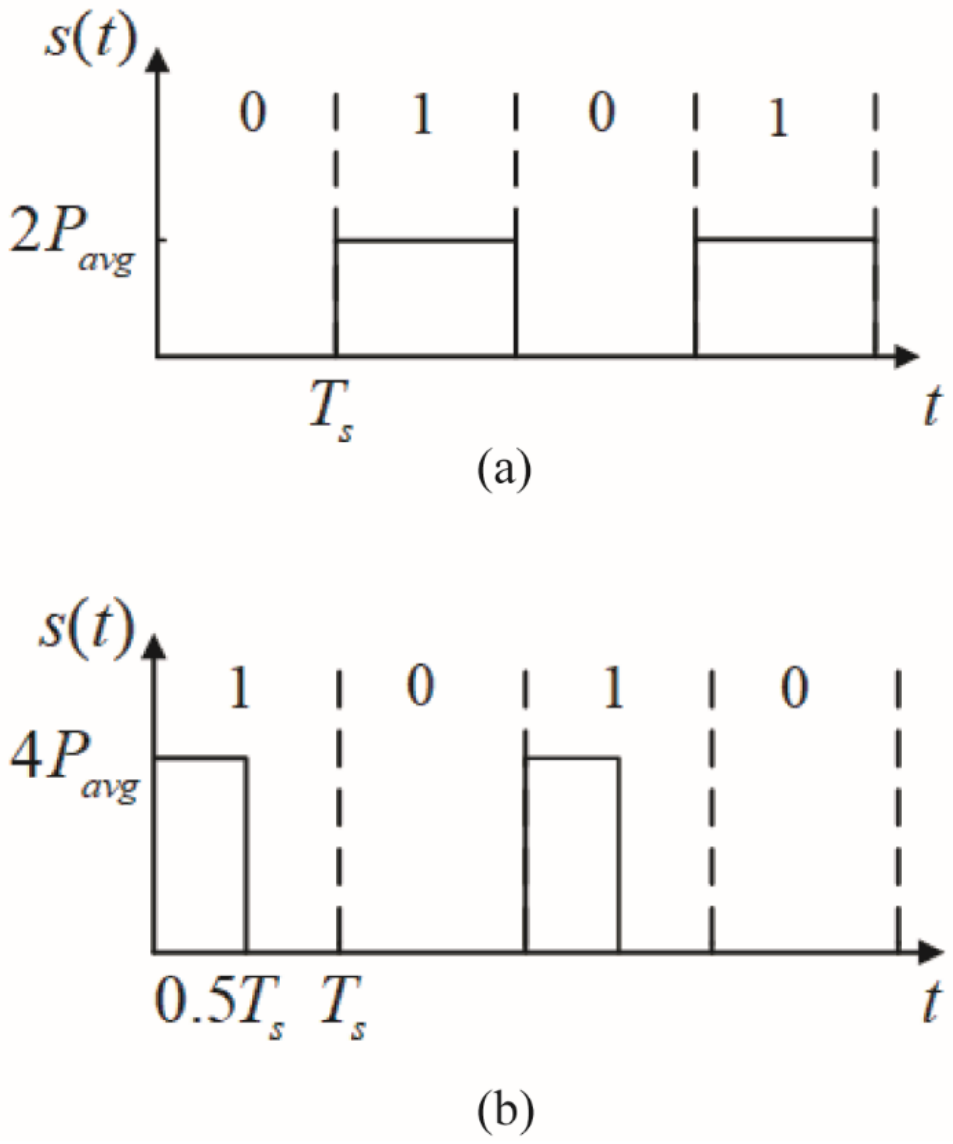

Fig. 3 Modulated waveform using (a) NRZ-OOK, and (b) PAM-8.

The improved spectral efficiency of PAM is achieved by transmitting more than one bit of data during each symbol period. Assuming the optical pulse in a PAM VLC system has

$M = 2^N$ different levels, where N is transmitted bit number within one symbol, the transmitted PAM signal with K successive transmissions is expressed as Eq. (2.6). Here, $p(t)$ is a rectangular pulse with a width of T_s.

$$s_m(t)_{PAM} = \sum_{k=1}^{K} s_m \times p(t), \text{ and } s_m = 0,1,2,\cdots,M-1 \tag{2.6}$$

Fig. 3 shows the difference in the modulated waveforms using PAM and NRZ-OOK for the same bit rate, where $M = 8$ in PAM.

2.2.2 Performance Analysis

Assuming the channel is an AWGN channel and a matched filter is used in the receiver, then the modulated PAM signal in a signal vector space can be written as Eq. (2.7):

$$s_m(t) = s_m\sqrt{\varepsilon_p}\phi(t), (s_m = 0,1,2,\cdots,M), \tag{2.7}$$

where $\phi(t) = \frac{p(t)}{\sqrt{\varepsilon_p}}$ is the normalized basis function, $p(t)$ is the shaping pulse with a width of T_s, and ε_p is the energy of $p(t)$.

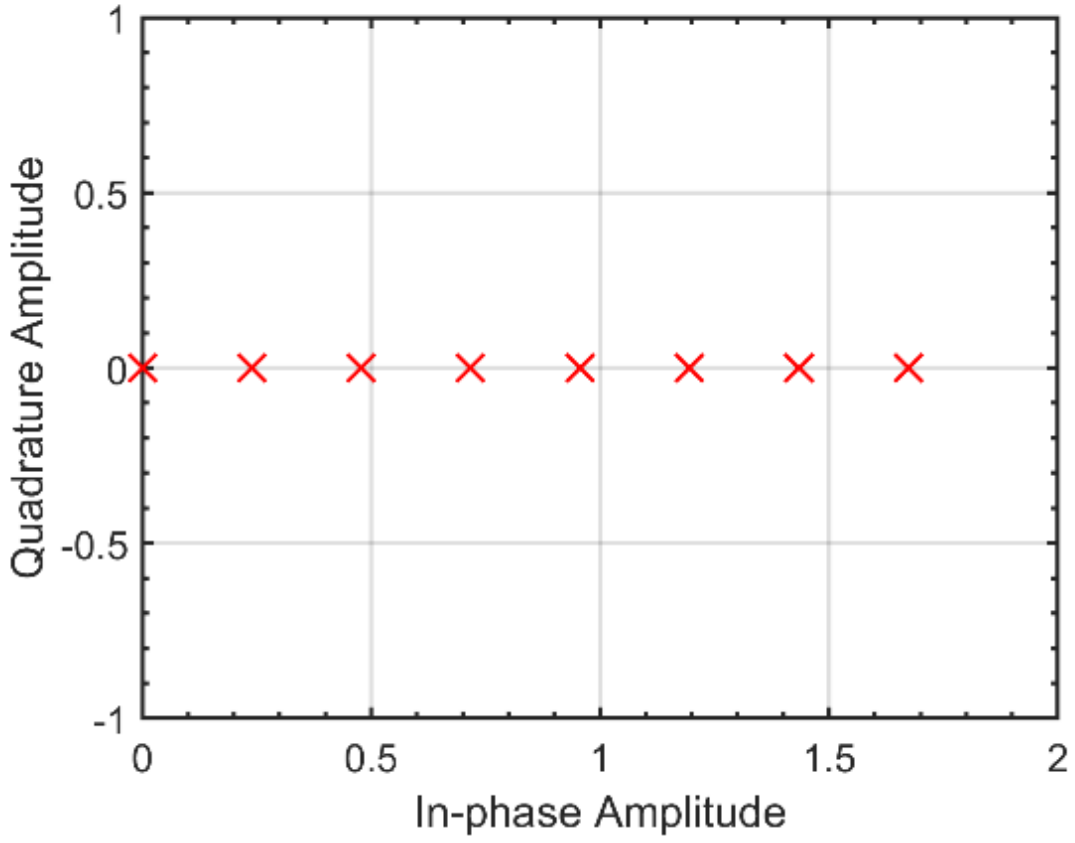

Fig. 4 Signal constellation of PAM-8.

Fig. 4 illustrates the signal constellation of PAM-8. The minimum distance between two adjacent points can be expressed as Eq. (2.8):

$$d_{min} = | s_{m+1} - s_m | \sqrt{\varepsilon_p} = \sqrt{\varepsilon_p} \ . \tag{2.8}$$

The symbol error rate of PAM can be analyzed with Eq. (2.9):

$$P_e = \frac{1}{M} \sum_{m=1}^{M} P(error \mid msent) = 2 \frac{M-1}{M} Q\left(\frac{d_{min}}{\sqrt{2N_0}} \right) . \tag{2.9}$$

Eq. (2.9) can be further revised as below [1]:

$$P_e = 2\left(1 - \frac{1}{M}\right) Q\left(\sqrt{\frac{3log_2 M}{(M-1)(2M-1)} \text{SNR}} \right) , \tag{2.10}$$

where

$$\text{SNR} = \frac{\varepsilon_{bavg}}{N_0} \tag{2.11}$$

$$\varepsilon_{bavg} = \varepsilon_p \frac{(M-1)(2M-1)}{6log_2 M} \ . \tag{2.12}$$

2.3 Orthogonal Frequency-Division Multiplexing

2.3.1 Principle of OFDM

OFDM is a multiple-carrier technique to transmit data in several parallel narrowband sub-channels. It can deal with the ISI issue caused by the multipath effect and facilitate channel equalization in wireless communication. Moreover, BEA algorithm can be employed in OFDM to optimize the data rates of different sub-channels. In order to generate a real signal for IM/DD in VLC systems, extra constraints have to be imposed at the input of the inverse fast Fourier transform (IFFT) in OFDM [2] and it will be introduced in Section 2.3.2.

In wireless communication, if there exists multipath effect, then several copies of the same transmitted symbol will reach the receiver with different delays. Therefore, the earlier symbol will affect the receiving of the following symbols and cause ISI. In OFDM, since the input data stream is split for simultaneous transmission in multiple narrowband sub-channels, the speed of the data stream in each sub-channel is significantly reduced, and thus the system is more reliable with the existence of ISI. To improve the spectral efficiency, all the subcarriers in OFDM are orthogonal to each other to support frequency overlapping between two adjacent sub-channels. The spectrum of an OFDM signal that contains several orthogonal subcarriers is shown in Fig. 5.

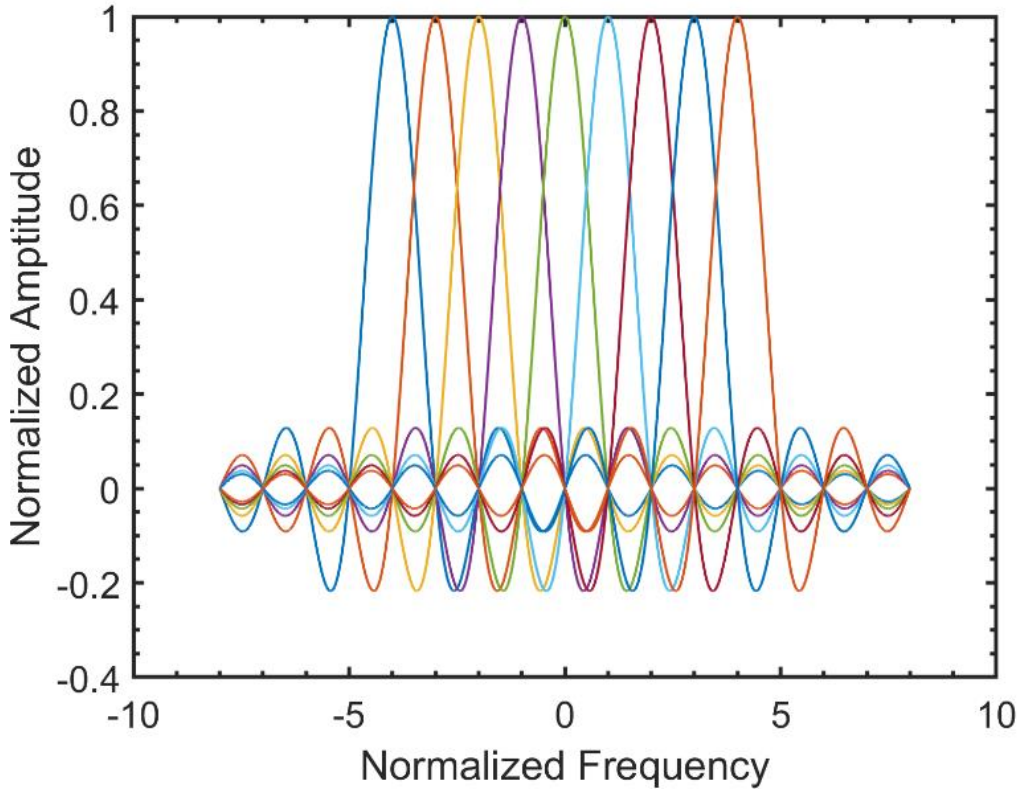

Fig. 5 Spectrum of an OFDM signal containing several orthogonal subcarriers.

An OFDM symbol can be represented as

$$s(t) = \sum_{k=0}^{N_{sc}-1} c_k s_k \tag{2.13}$$

$$s_k = e^{j2\pi f_k t}, 0 \le t \le T_s \ , \tag{2.14}$$

where c_k is the mapped symbol in each sub-channel, N_{sc} is the total number of sub-channels, f_k is the frequency of the subcarriers, and T_s is the symbol period in the sub-channels. To have orthogonal sub-channels, Eq. (2.15) must be equal to 0:

$$\delta_{kl} = \frac{1}{T_s}\int_0^{T_s} s_k s_l^* dt = \frac{1}{T_s}\int_0^{T_s} e^{j2\pi(f_k - f_l)} dt \ . \tag{2.15}$$

This is satisfied when

$$f_k - f_l = \frac{n}{T_s}, n = 1, 2, \cdots, N_{sc} - 1 \ . \tag{2.16}$$

In the digital domain, if $s(t)$ is sampled at a rate of N_{sc}/T_s, then Eq. (2.17) can be derived:

$$s_m = \sum_{k=0}^{N_{sc}-1} c_k e^{j2\pi \frac{km}{N_{sc}}}, 0 \le m \le N_{sc} - 1 \ . \tag{2.17}$$

2.3.2 Modified OFDM for VLC

In order to generate a real and positive output for IM/DD in a VLC system, extra constraints have to be imposed on OFDM. Therefore, various modified OFDM schemes have been proposed, including DCO-OFDM, ACO-OFDM and PAM-DMT [3]. The implementation details of these OFDM schemes are illustrated in Fig. 6, Fig. 7, and Fig. 8, respectively. Assuming QAM is employed in both DCO-OFDM and ACO-OFDM, N-point IFFT is employed in all schemes, and N is even.

As shown in Fig. 6, the input of DCO-OFDM is mapped to $N/2-1$ independent data symbols (from X_1 to $X_{N/2-1}$) according to the QAM constellation, and the other $N/2$ symbols (from $X_{N/2}$ to X_N) are generated based on the following relationship to meet Hermitian symmetry. In particular, X_0 is set by the DC bias to avoid signal clipping.

$$X_k = X_{N-k}^*, k = N/2+1, \cdots, N-1 \tag{2.18}$$

$$X_{N/2} = 0 \ , \tag{2.19}$$

where the symbol "*" denotes the conjugate operation. DCO-OFDM is spectrally efficient, but its power efficiency is low due to the employment of a high DC bias.

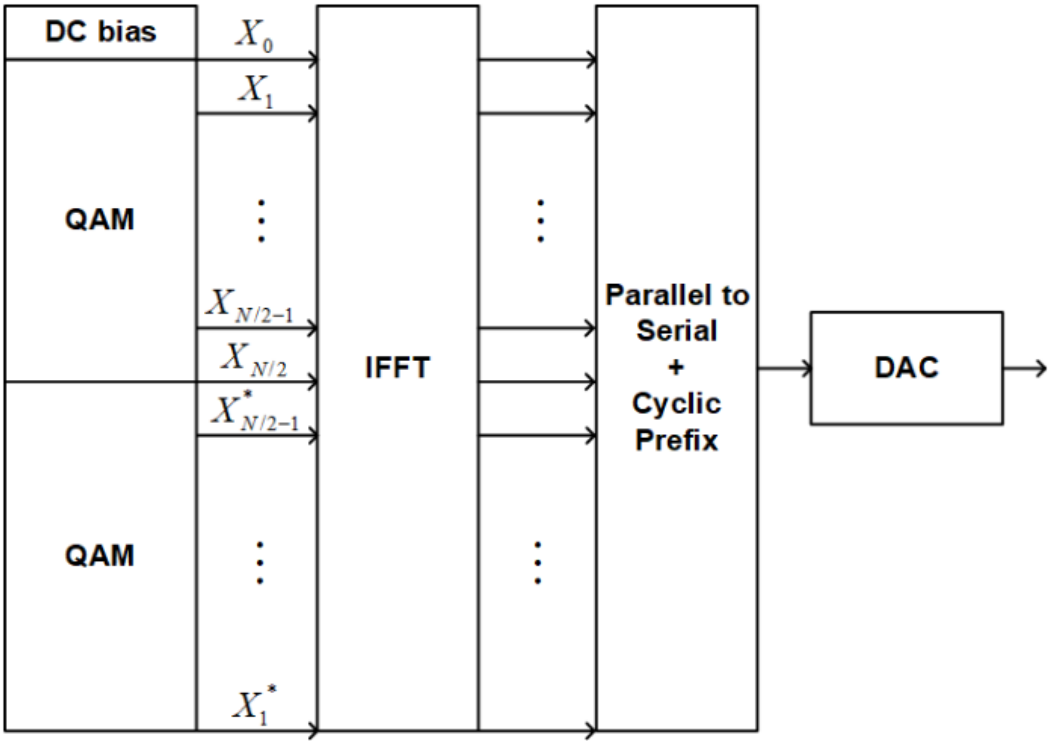

Fig. 6 Block diagram of DCO-OFDM.

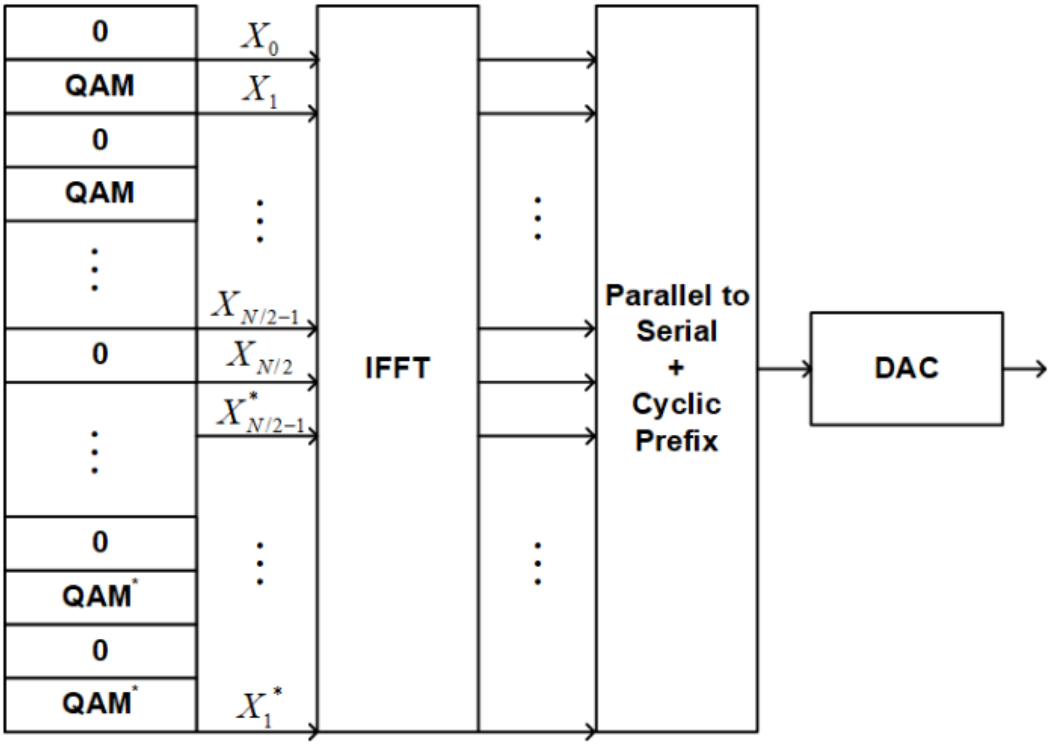

Fig. 7 Block diagram of ACO-OFDM.

In order to improve the power efficiency, ACO-OFDM has been proposed, as shown in Fig. 7. Compared to DCO-OFDM, ACO-OFDM only utilizes the odd subcarriers of the first N/2 to contain information, while setting the input symbols of the even subcarriers to 0. Therefore, every negative output of IFFT can find a positive replica [4], and the missing

information due to clipping can be recovered with the help of the positive replica. In other words, a high DC bias is not necessary in ACO-OFDM, and thus its power efficiency can be significantly improved. However, the spectral efficiency of ACO-OFDM is reduced by about half compared to DCO-OFDM since no even carrier can be utilized to carry information.

Similar to ACO-OFDM, PAM-DMT is another OFDM scheme that can accommodate clipping distortions and it avoids the employment of a high DC bias. As shown in Fig. 8, only the imaginary part of the input symbols of the subcarriers in PAM-DMT is utilized to carry information, and the real part of the input symbols is set to zero. Therefore, complex data symbols generated by QAM are not supported in this scheme. PAM-OFDM can achieve better power efficiency compared to DCO-OFDM, but its spectral efficiency is limited since only PAM is employed.

The DCO-OFDM scheme is used in this thesis work. The detailed derivation explaining why the output signal is real is inducted in Chapter 4.

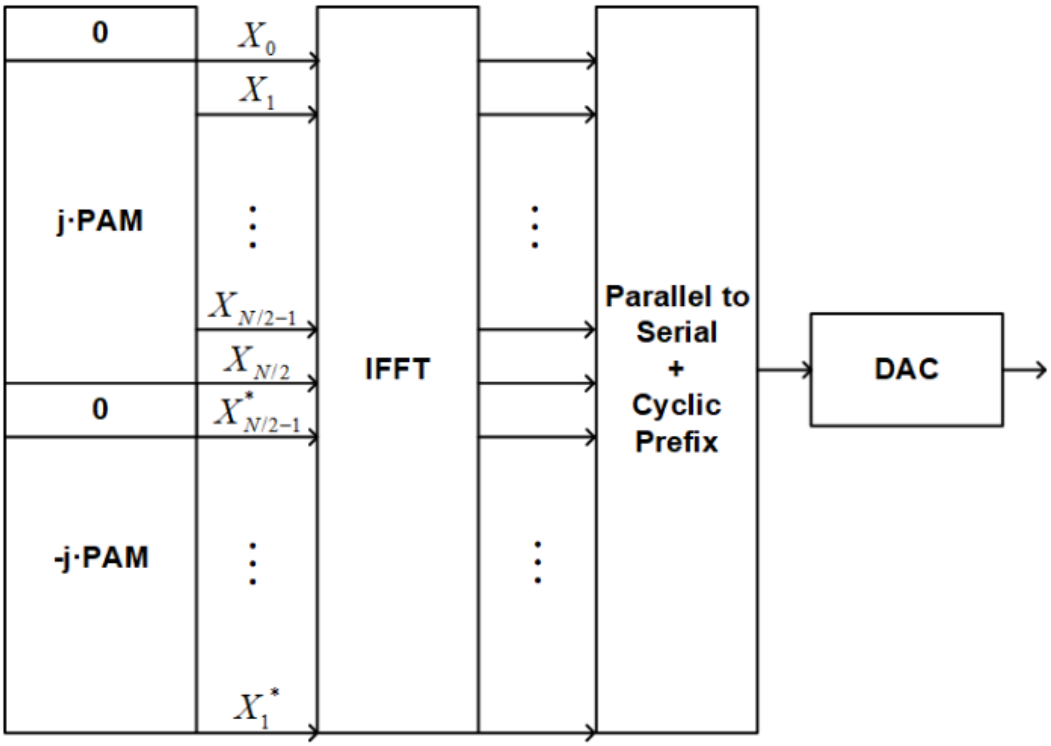

Fig. 8 Block diagram of PAM-DMT.

2.4 References

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CHAPTER 3. SINGLE SUBCARRIER VLC BASEBAND DESIGN

3.1 Introduction

Compared with a multi-subcarrier communication system, the complexity of a single-subcarrier system is significantly low. Therefore, single-subcarrier modulation schemes like OOK, PAM and CAP are still widely used in VLC systems.

The bandwidth limitation of the light source and other front-end analog devices are the bottleneck of improving the transmission speed. The most intuitive method to increase the transmission speed is improving the bandwidth of the LEDs. The bandwidth of the convention phosphor coated LED and RGB LED can only reach 3-5 MHz and 15-35 MHz, respectively [1], while the GaN-based micro-LED can reach several hundreds of MHz [2, 3]. Some systems even use laser as the light source for VLC, which is called visible laser light communication (VLLC). The bandwidth of the laser can reach a few GHz easily. Another technology to increase the bandwidth is equalization technology, which includes pre-equalization at the transmitter [4], post-equalization at the receiver [5] and pre- and post-equalization applied at the same time [6]. The equalization technology can be applied in both the time domain [7] and the frequency domain [8]. Some equalizers are implemented in the analog frontend [4] and others are in the baseband [6]. Besides increasing the bandwidth of the system, the improvement of spectrum efficiency can also enhance the throughput of the VLC system. Therefore, PAM and CAP is employed to increase the data rate under the fixed bandwidth of the whole system.

Therefore, in Section 3.2, a laser with a high bandwidth is used. A relatively simple OOK modulation scheme is used but the speed is high enough to transmit video streams. In Section 3.3, a commercial RGB LED with a narrow bandwidth is used. The pre- and post-equalization is used to improve the bandwidth of the system, and PAM-4 is used to increase the spectrum efficiency to increase the throughput of the system further.

3.2 OOK VLLC for High-Definition Video Transmission

3.2.1 Introduction and Motivation

Most of the previous research only uses high-cost off-the-shelf equipment to do the off-line measurement. Their study is lacking on the real-time high speed VLC system design with practical baseband implementation.

In this work, we propose a real-time visible laser light communication system capable of supporting high-definition video transmission at up to a 500 Mbps data rate. In order to process data in real-time, a digital baseband is implemented on Xilinx Field Programmable Gate Arrays (FPGAs). The digital baseband collects data packages from the ethernet, encodes the received data using an 8B/10B scheme and controls the laser diode driver using an NRZ-OOK modulation scheme. The transmitted optical signal is recovered by the receiver front-end and baseband. The recovered data is transmitted through the ethernet and finally displayed on a monitor in real-time. Because UDP/TPC protocol is used, text, audio can also be transmitted. Different applications employing VLLC can all be tested and evaluated effectively in our proposed system.

3.2.2 System Architecture

A block diagram of the proposed system is shown in Fig. 9. The system consists of three parts: data source, digital baseband, and optical frontend.

Two personal computers (PCs) with a 1 G Ethernet port are the data source, which is to interpret transmitted data and package received data under the constraint of user datagram protocol (UDP). A digital baseband implemented on an Artix-7 FPGA evaluation board exchanges real-time data with a data source through the 1 G Ethernet port. The digital baseband design is the most import part in the proposed system and it will be introduced separately. The frontend of the transmitter consists of a driving circuit and a laser diode transforming the signal from the electrical domain to the optical domain. A photodetector and electronic amplifier in the receiver side recover and amplify the received signal.

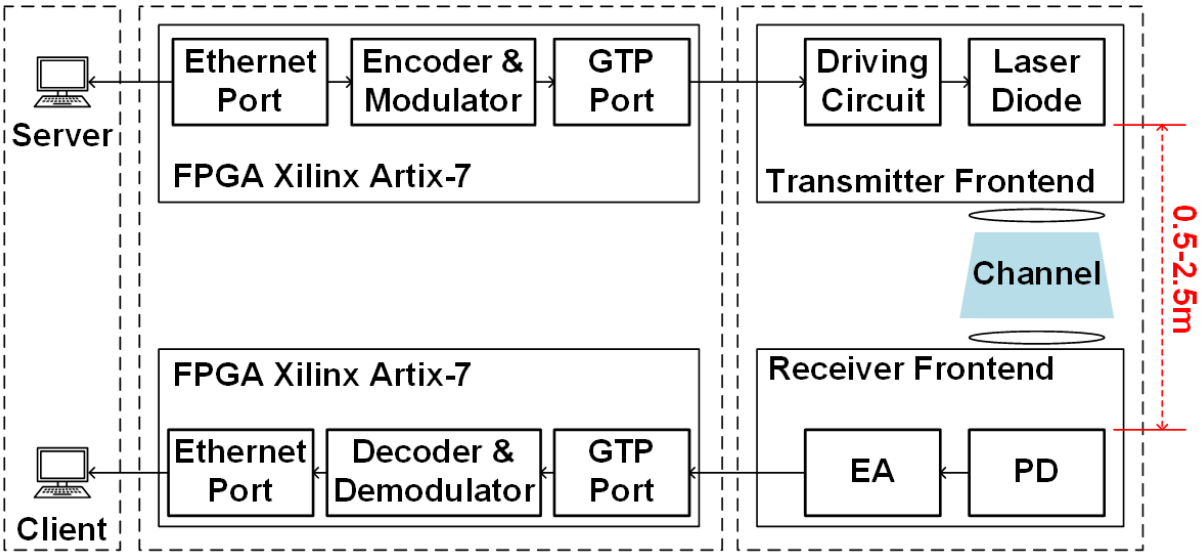


Fig. 9 Block diagram of the proposed system.

The schematic of the baseband design is presented in Fig. 10. A clock generation module is built on the phase-locked loop (PLL) in the FPGA chip to satisfy the different frequency requirements of each module. Reset signals are generated by a reset generation module to reset the whole system in the appropriate order when necessary to ensure the robustness of the system. The clock and reset network connect to every module in the system to control them to work normally.

A datalink in the baseband is built based on the clock and the reset network. On the transmitter side, Ethernet packages from the data source are captured by an Ethernet physical layer chip and sent to the FPGA chip. A media access control layer (MAC) built on an FPGA extracts data and puts them in a first in, first out memory (FIFO). Then, the encoder and modulator module picks data in FIFO. The encoder includes not only error correction coding but also 8B/10B coding to equalize the number and distribution of bit 1 and 0 in the data sequence to achieve DC balance and provide enough state changes to allow reasonable clock recovery. A tail and head are added to each data frame then for synchronization. FIFO is added between the MAC and modulator to support the burst transmission.

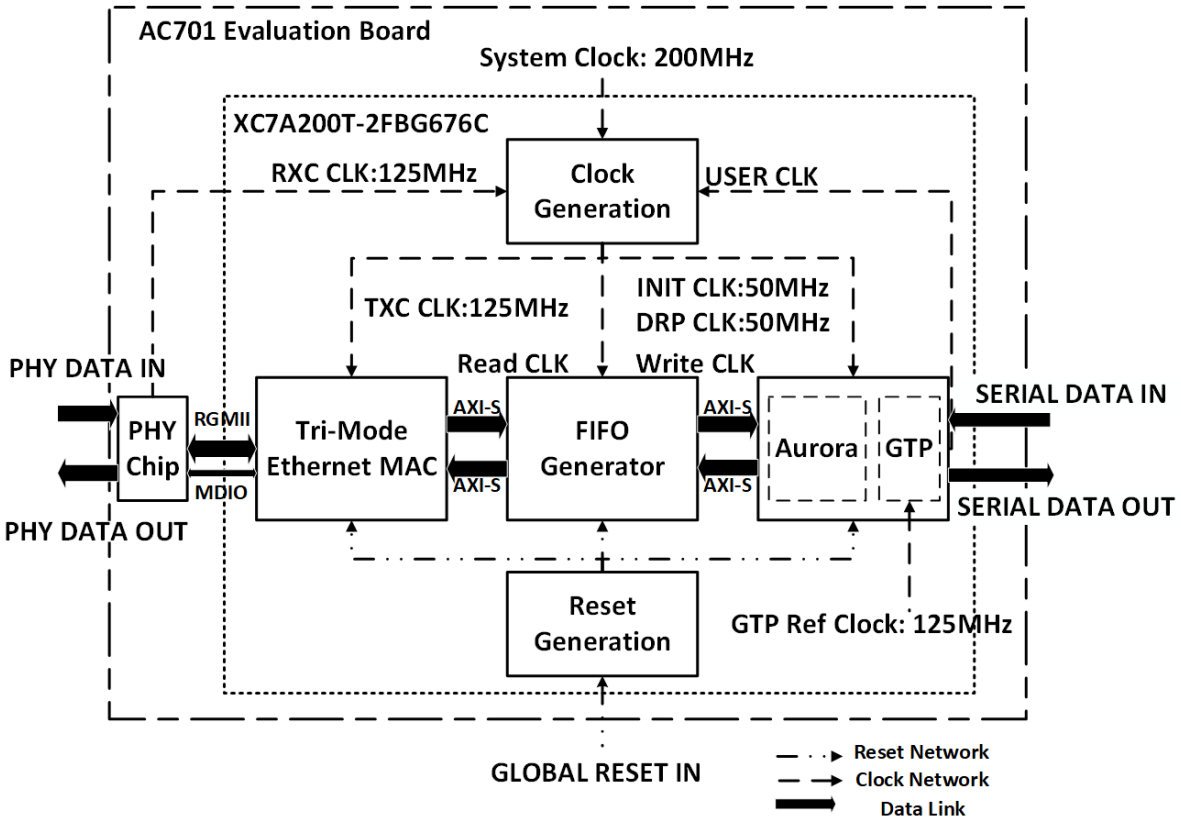


Fig. 10 Schematic of the baseband design.

When there is no data to transmit, a specific sequence will be sent for the clock recovery in the receiver side. NRZ-OOK modulation is chosen in our system, in which the positive

voltage level stands for logical 1, and negative for logic 0 so there is no digital to analog converter (DAC) needed between the digital baseband and the laser diode driver. The modulated signal is transmitted to the laser driver through the GTP port, which is one kind of high-speed transceiver interface provided by the Xilinx FPGA chip. The whole process is based on the Aurora protocol, which is proposed by Xilinx for high-speed serial transmission. The coding and modulation are realized by utilizing IP core resource provided by the FPGA [9].

3.2.3 Implementation and result

Fig. 11 shows the experimental setup and the corresponding equipment models are detailed. The distance between the LD and PD is 0.5 to 2 meters. The system can work normally in this range.

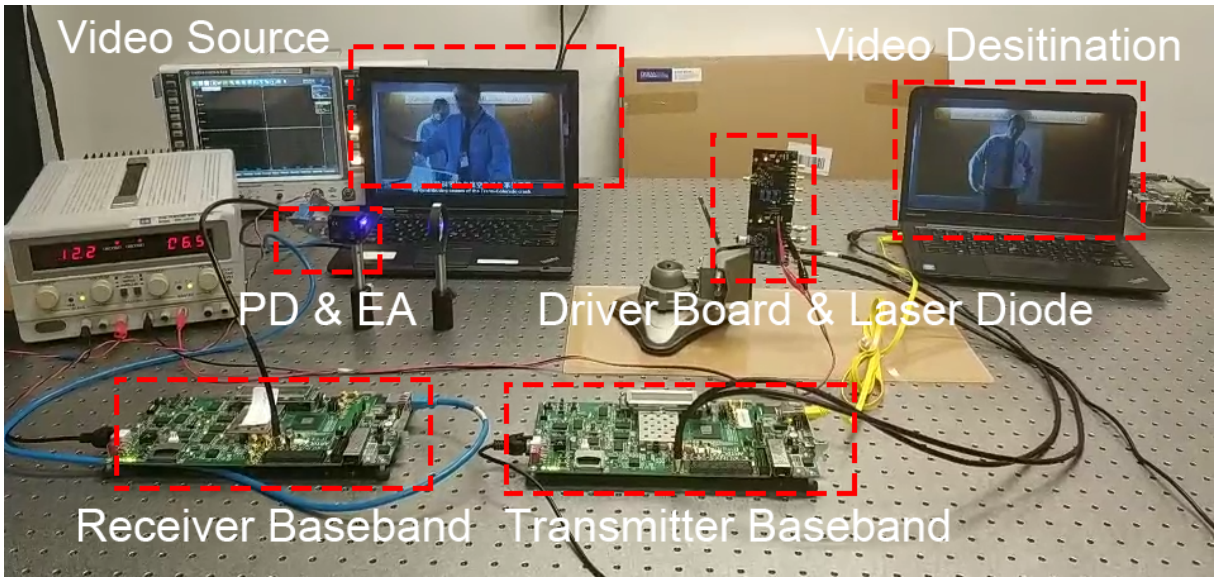


Fig. 11 Experimental setup of the proposed VLLC-based video transmission system.

The I-V curve of the used blue laser diode is firstly measured and is shown in Fig. 12, and Fig. 13 and Fig. 14 is the eye diagram of GTP output and the PD output signal, respectively.

TABLE II. SUMMARY OF THE SYSTEM CONFIGURATION

Device	Values
PC:	ThinkPad S3 S440
FPGA:	XC7A200T-2FBG676C 500Mpbs
LD Driver:	Maxim 3869 2.5Gbps
LD Diode	PLT5 450B
PD	DET025A/M
EA	LNA2-3G-40DB

Finally, one 1080P resolution video is streamed by video streaming software named VLC and is transmitted smoothly through the proposed system. We also test text and audio

transmission through our system. All multi-media source can be transmitted without obvious mistake.

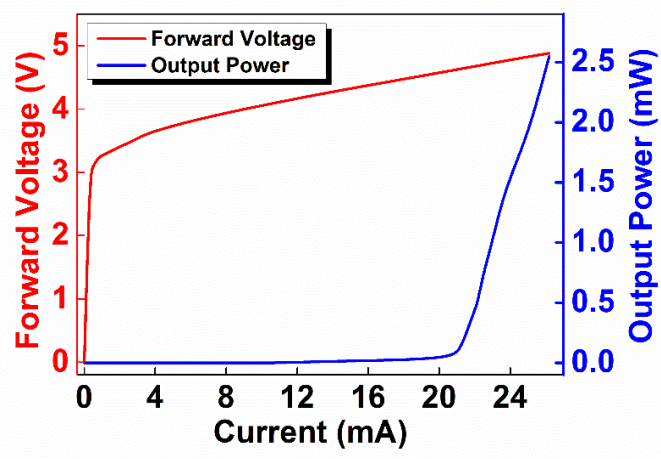


Fig. 12 I-V curve of the LD source.

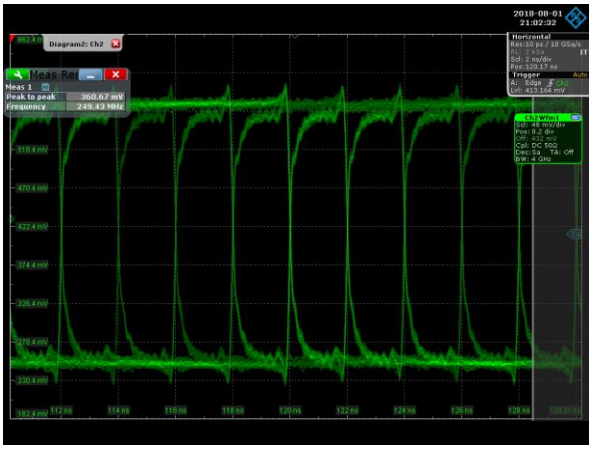


Fig. 13 Eye diagram of the GTP output.

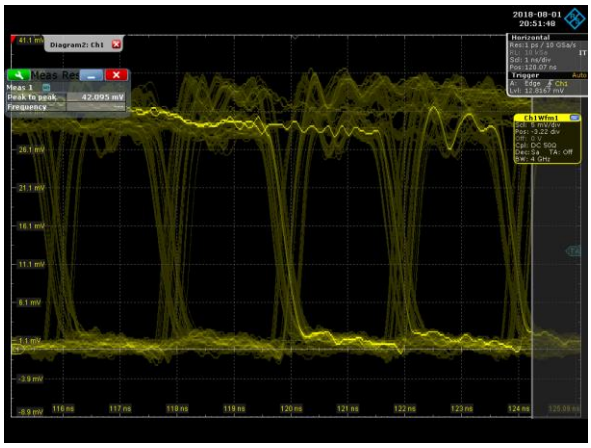


Fig. 14 Eye diagram of the PD output.

3.2.4 Conclusion

This work presents a complete real-time VLLC system design with a baseband implementation on an FPGA platform using 8B/10B encoding and NRZ-OOK modulation

scheme. An experimental platform is built to test the VLLC system performance, which verifies that real-time high-definition video transmission can be achieved at a data rate of 500 Mbps over a 2-meter distance in real-time.

3.3 RGB PAM-4 VLC Supporting FFE Equalization

3.3.1 Introduction and Motivation

When a high-level modulation scheme such as PAM-4 is applied in a real-time VLC system, there are several physical layer challenges that severely limit the data transmission quality, such as the nonlinearity of optical responses to the driving current and the limited bandwidth of LEDs. So far, there has been a lack of investigation into the practical and compact implementation of the transceiver front-end design supporting PAM-4 modulation to serve as an electrical-to-optical and optical-to-electrical interface.

In Section 3.3, we propose a complete system-on-board RGB PAM-4 transceiver design with feed-forward equalization (FFE) and cascaded continuous-time linear equalization (CTLE). The PAM-4 optical signal is constructed by linearly combining the three serial NRZ optical signals from the red, green, and blue LEDs in the optical domain. The transceiver design can tune the three eye-heights of the PAM-4 optical signal independently to compensate for the differences in the LED optical responses. Experimental results of the RGB PAM-4 system demonstrate that PAM-4 data transmission can be achieved with high quality, and the LED bandwidth can be extended 2.5 times using pre- and post-equalization.

3.3.2 System Architecture and Digital Baseband Design

The system architecture of the proposed RGB PAM-4 VLC system is presented in Fig. 15. The transmitter system consists of a baseband encoder implemented in a FPGA and a transmitter circuit board with 1-tap FFE function. The baseband encoder receives two serial bits: one most significant bit (MSB) and one least significant bit (LSB). The MSB and LSB serial bits are encoded into three channels of serial data, which separately contribute to the three eyes of the PAM-4 signal. For each of the three channels, the data is duplicated into two paths, with one data path going through an inverter and a digitally controlled asymmetric rising and falling delay. On the transmitter circuit board, three serial data-pairs control the main and 1-tap FFE drivers of each of the red, green, and blue LED. The output NRZ optical signals from the red, green, and blue LEDs are linearly combined in the optical domain and generate the PAM-4 optical signal, with each NRZ optical signal contributing to one part of the PAM-4 eye. On the receiver side, the PAM-4 optical signal is converted into an electrical signal using a photo detector and a transimpedance amplifier (TIA). The converted electrical PAM-4 signal is then

equalized using a three-stage cascaded CTLE to compensate for the limited bandwidth and is delivered to the output with a unit gain buffer.

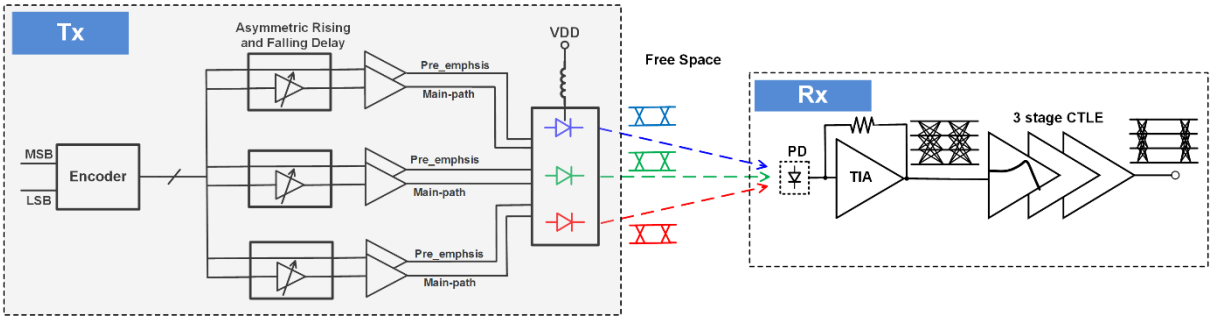


Fig. 15 System architecture of the proposed PAM-4 VLC system.

Fig. 16 shows the detailed structure of the digital baseband design. There are two clock domains in the transmitter digital baseband design. The frequency of the slow clock decides the data rate of the transmitter, and the ratio between the fast and the slow clock decides the resolution of the FFE path delay time. A pseudorandom binary sequence (PRBS) is generated by an inner PRBS generator as the source information. The output of the PRBS generator is two bits width paralleled data. A unary code encoder encodes the two bits paralleled data into three bits width thermometer code. The corresponding relationship between the input and output of the encoder is shown in TABLE III. The encoded result is duplicated. The original three bits is outputted to drive the main path. The duplicated three path is transmitted into the fast clock domain. The rising and falling edge of the signal are detected by the fast clock. Then, the inverted and delayed signals are recovered by the rising/falling edge delay module using the detected edges combined with the delayed fast clock cycles provided by the delay control module. The delayed and inverted signal are used to drive the FFE path.

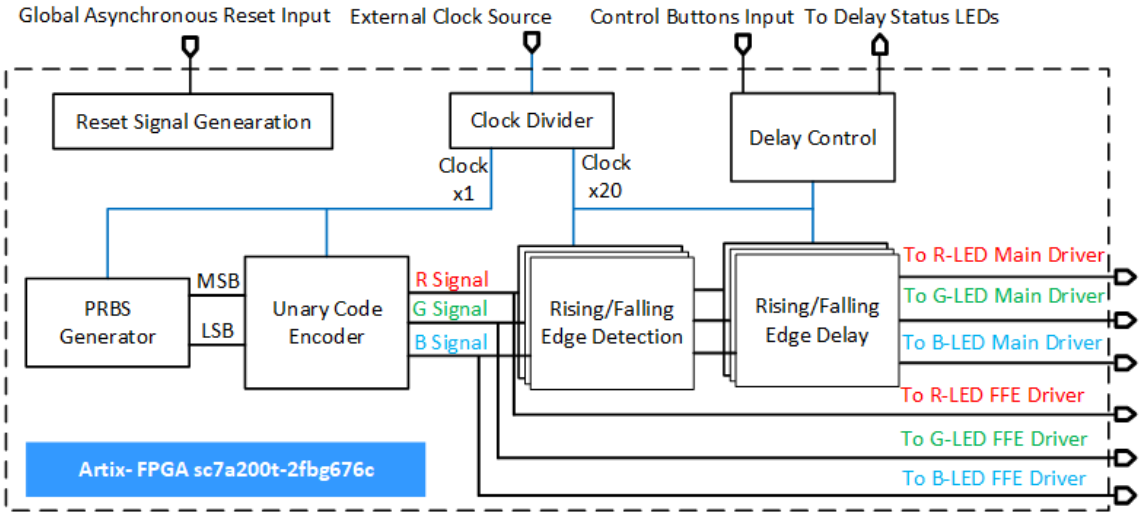


Fig. 16 Structure of the digital baseband of the transmitter.

TABLE III. INPUT AND OUTPUT OF THE UNARY CODE ENCODER

Encoder Input	Encoder Output
00	000
01	001
10	011
11	111

The main path and FFE path signals are combined in the electrical domain to form three reshaped waveforms. The high frequency part energy of the generated signal is pre-emphasized compared with the original signal. Fig. 17 illustrates how the reshaped waveform is generated in our designed circuit.

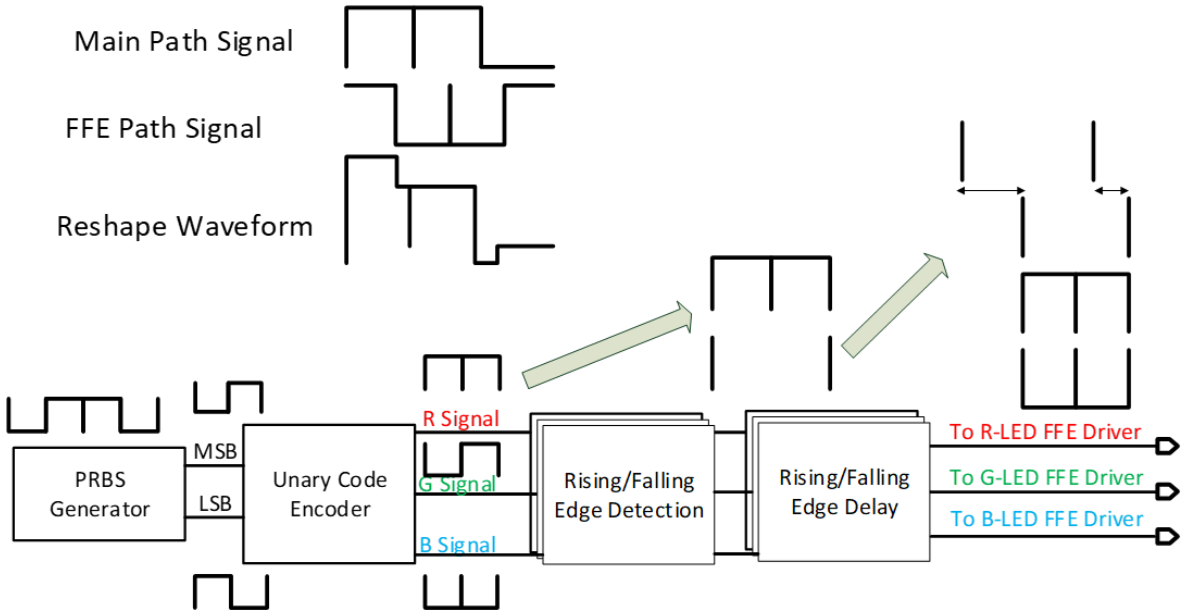


Fig. 17 Generation of the transmitted waveform.

The light source employed here is a commercially available RGB LED with each of the red, green, and blue LEDs capable of providing a maximum of 0.5 W output light. The optical responses and bandwidths of the three LEDs are different, which causes the eye-widths to be unequal and the eye quality to be degraded. To solve this problem, three VLC drivers with independently driving current controls and FFEs with asymmetric digitally controlled edge delays are separately implemented for the red, green, and blue LEDs. The delays for the rising and falling edges of the FFE data path can be controlled separately using digital code to compensate for the asymmetric rising and falling times of the LEDs, as shown in Fig. 18. The driving current of the three drivers are carefully adjusted so that the three eye heights of the PAM-4 signal are equal. On the receiver side, a three-stage-cascaded CTLE with an RC degeneration structure is implemented to compensate for the bandwidth limitation of the RGB

LED and the TIA. The cascaded CTLE features variable peaking frequency, height, and slope, which can provide compensation to a wider bandwidth.

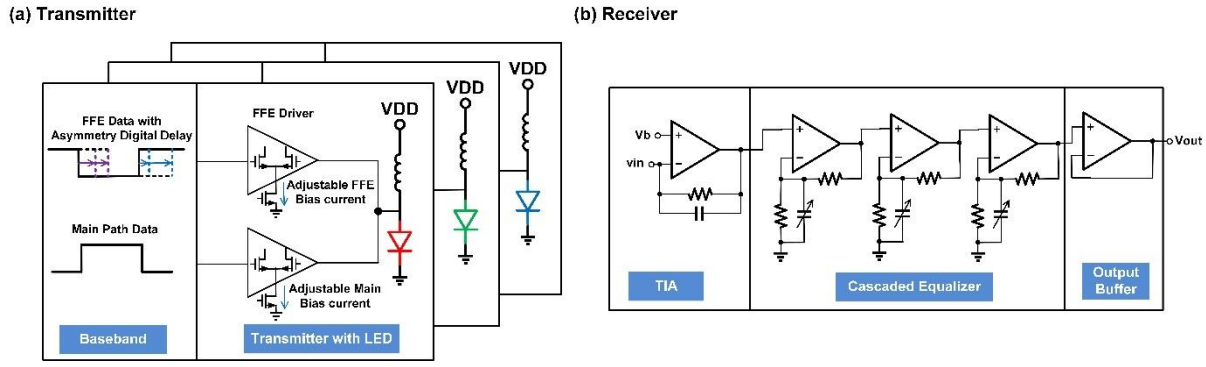


Fig. 18 Analog frontend design of the transmitter and receiver.

The red, green and blue light are mixed in the optical domain. The white light is generated for illumination and the PAM-4 signal is generated for communication. The relationship between the status of the three LEDs and the waveform of the PAM-4 signal is shown in Fig. 19.

PAM-4 symbol	0	1	2	3
Red Light	0	1	1	1
Green Light	0	0	1	1
Blue Light	0	0	0	1

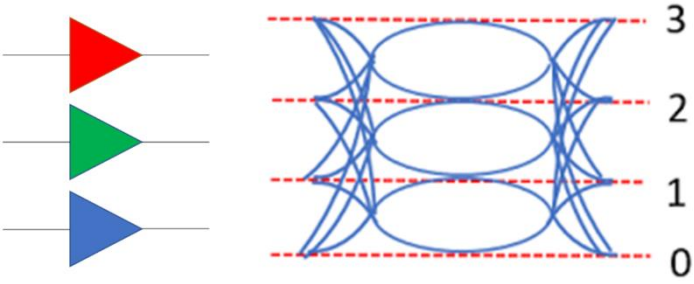


Fig. 19 The relationship between LED status and the output waveform.

3.3.3 The System Setup and Experiment Result

Based on the designed RGB PAM-4 VLC transmission system, the data transmission performance was verified at a 5-cm transmission distance by measuring the bit-error-rates (BERs), bathtub curve (BC) and eye diagrams. The measured BERs versus data rate under the conditions of red LED NRZ transmission, PAM-4 without EQ, PAM-4 with FFE only, PAM-4 with one stage CTLE, and three stage CTLE are plotted and compared in Fig. 20. Compared to NRZ data transmission, by applying the PAM-4 modulation scheme, the highest achievable data rate was increased from 22 Mbps to 32 Mbps, which was further extended 2.5 times to 80 Mbps using the FEE and CTLE functions. The FFE on the transmitter side and the cascaded CTLE on the receiver side contributed to a 2.1- and 1.2-times extension ratio, respectively. The bathtub curve at 68 Mbps shows a 0.3–UI margin for a BER less than 3.6×10^{-3}, which is shown

in Fig. 21. The eye diagrams under the three different equalization conditions are shown in Fig. 20, which demonstrate the functions of the pre- and post-equalizations.

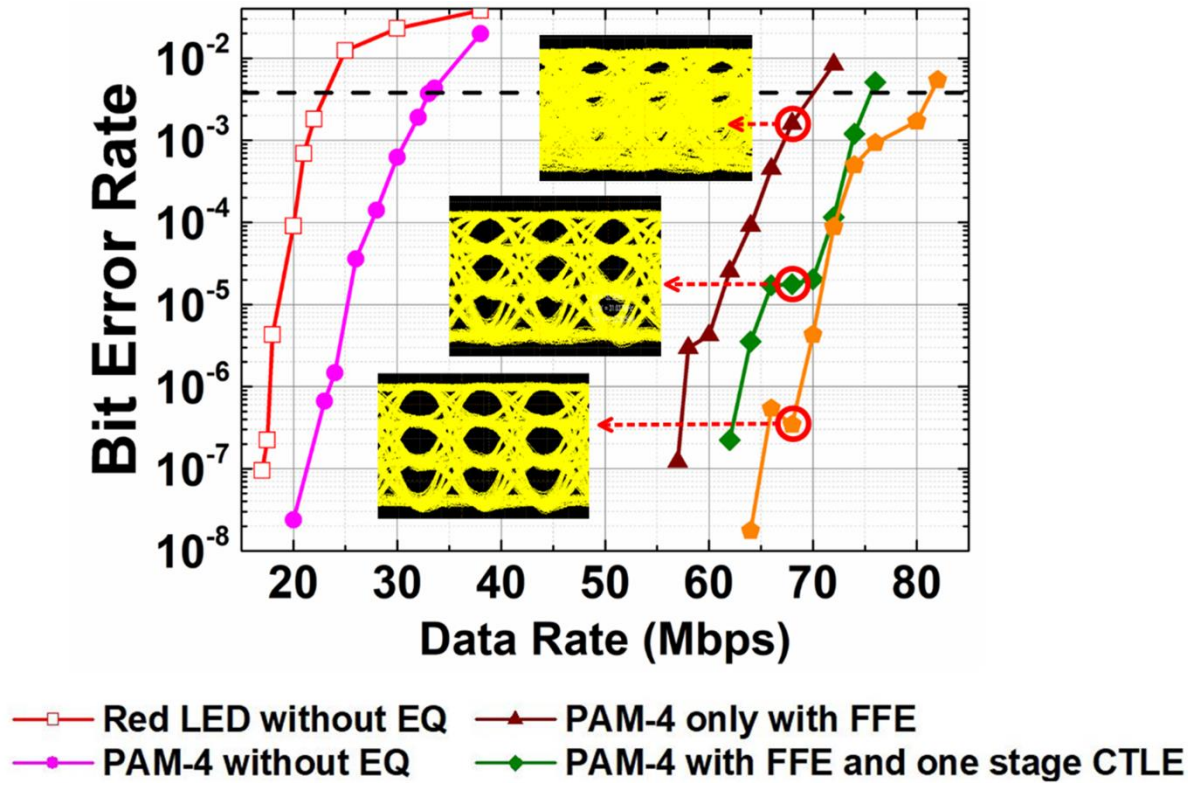


Fig. 20 Measured BER versus data rate for a red LED without EQ, PAM-4 without EQ, PAM-4 with only FFE, PAM-4 with FFE and first stage CTLE, PAM-4 with cascaded CTLE, and eye diagrams at 68 Mbps for the three different equalization conditions.

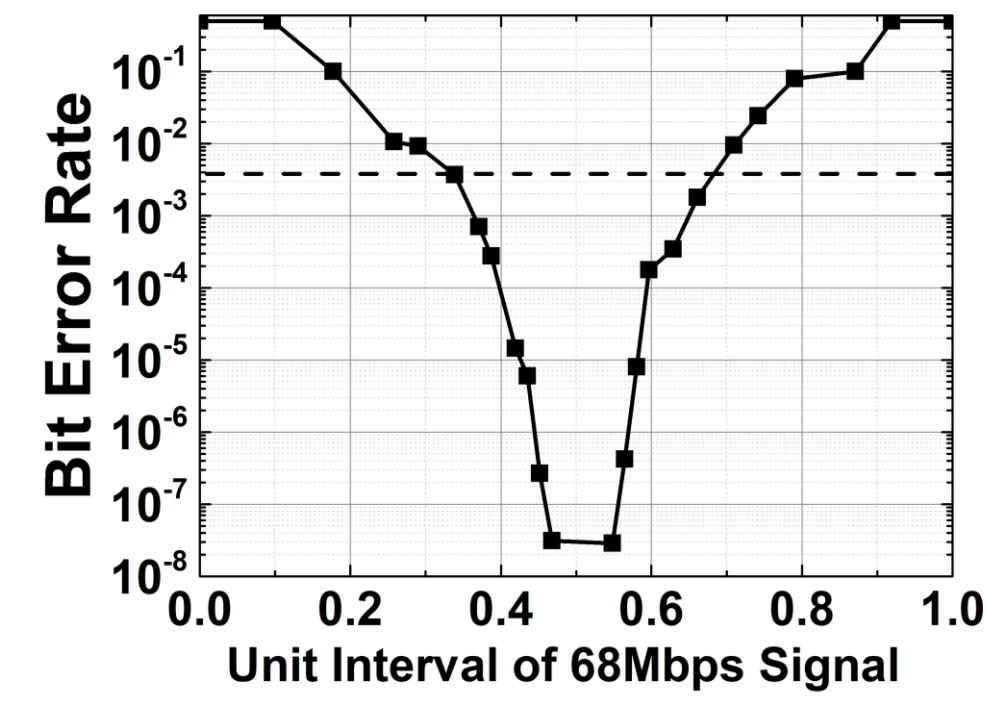
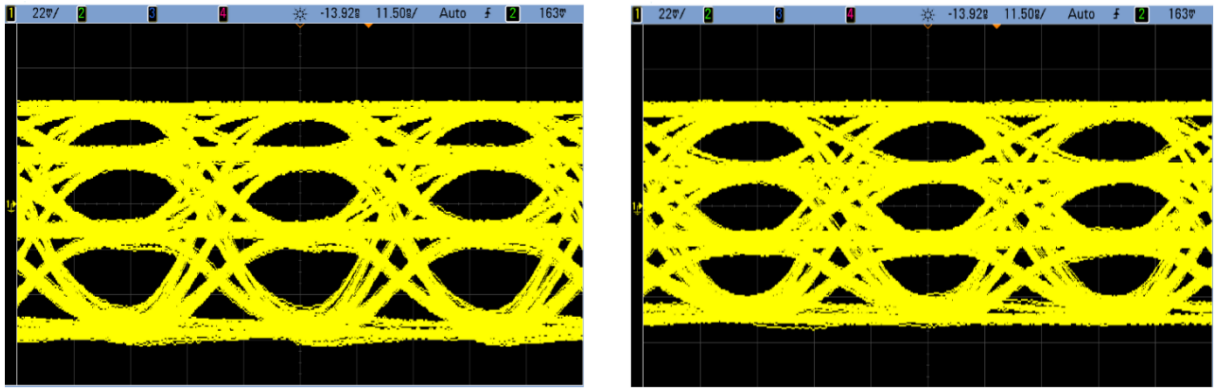


Fig. 21 Measured bathtub curve at 68 Mbps.

Due to the different optical responses of the red, green, and blue LEDs, the three eye-heights of the received PAM-4 signal were uneven, as shown in Figure 22 (a), and thus led to a very narrow decoding margin. By tuning the driving current of the RGB LEDs independently, a much-improved PAM-4 data eye with almost equal eye-heights can be achieved, as shown in Fig. 22 (b).



(a) (b)

Fig. 22 Measured eye diagram (a) without independent driving current tuning, and (b) with independent driving current tuning.

3.3.4 Conclusion

An RGB PAM-4 VLC transceiver system with a 1-tap FFE and three-stage-cascaded CTLE was presented. The PAM-4 optical signal is constructed by linearly combining three independent NRZ signals from the respective RGB LEDs. The experimental results validate that the independent eye-height tuning feature enables high-quality PAM-4 signal transmission resulting in a 2.5-times increase in bandwidth extension ratio.

3.3 References

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CHAPTER 4. MULTI SUBCARRIER VLC BASEBAND DESIGN

4.1 Introduction

Compared with the single subcarrier system used in the previous section, the structure of a multi subcarrier system is more complex. However, a multi subcarrier system like OFDM has the ability to resist multipath interference and frequency selective fading. Because the data in the OFDM system is spread between many subcarriers, the effect of multipath interference is weakened. In addition, the inter symbol interference can be completely eliminated, even if a cyclic prefix is used as the guard interval. When OFDM is used in a VLC system, a dynamic BEA algorithm is always used to achieve the maximum bit rate. The transmission bit rate is maximized by selecting the various subcarriers, the number of bits in each symbol, as well as the power allocated to each subcarrier. Therefore, the spectrum efficiency can be improved further when OFDM with a BEA algorithm is used. Additionally, by joint coding each subcarrier, a strong anti-fading capability can be achieved. OFDM technology itself has made use of channel frequency diversity [1].

This section proposes a completed VLC system utilizing DCO-OFDM with a BEA algorithm. The system structure and algorithm are studied firstly. Then the real-time system is implemented and measured.

Section 4.2 shows the construction of a VLC transceiver employing DCO-OFDM with BEA. The mathematical principle of DCO-OFDM, signal to noise ratio (SNR) measurement and the BEA algorithm are also shown in this section. On the theoretical basis of Section 4.2, Section 4.3 designs a real-time VLC transmitter employing DCO-OFDM supporting the BEA algorithm. The design is implemented on an FPGA platform. A VLC system is then constructed combining the designed baseband circuit and other frontend modules. The performance of the system is finally measured to show the effectiveness of the BEA algorithm.

4.2 Transceiver Structure and Mathematics Principle

This section presents the theoretical basis of the VLC transceiver utilizing DCO-OFDM. In Section 4.2.1, the structure of the whole system is firstly illustrated. Then, the data flow of the baseband of the transmitter and receiver is shown. Section 4.2.2 explains the mathematical principle of DCO-OFDM. Section 4.2.3 shows how the SNR of each subcarrier is measured. Section 4.2.4 introduces how the BEA algorithm is used in the proposed design based on the measured SNR in Section 4.2.3.

4.2.1 System Structure

Section 4.2.1 gives a brief introduction of the VLC system employing DCO-OFDM including both the digital baseband and the analog frontend.

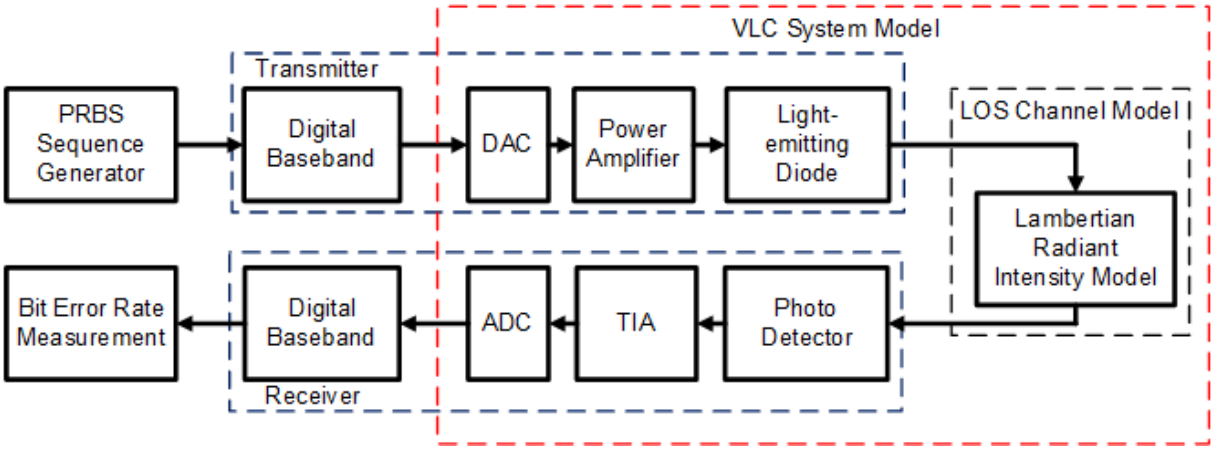

Fig. 23 System diagram of the VLC system

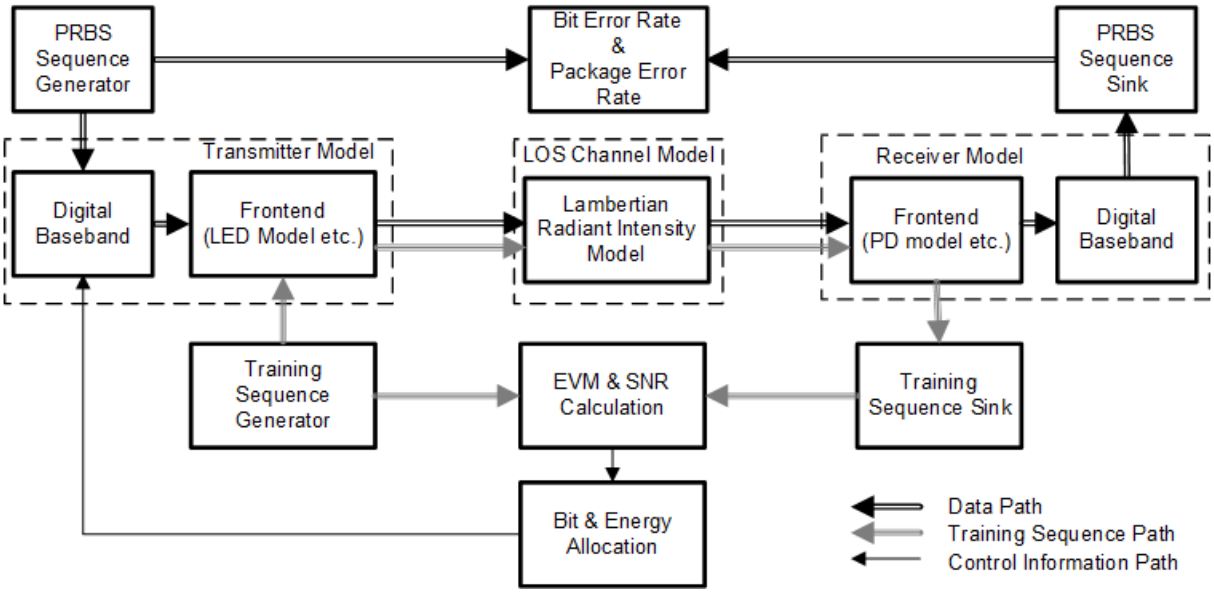

Fig. 24 System diagram with SNR measurement and the BEA algorithm

Fig. 23 shows the system diagram of the proposed system. On the transmitter side, a PRBS is generated and fed into the digital baseband for encoding and modulation. The baseband output is then sent to the DAC to perform digital-to-analog conversion, and the output of the DAC is further amplified by the power amplifier and is biased by a DC signal to form the LED driving current. The LEDs convert the driving current into an emitted optical signal. Then, the optical signal goes through an LOS channel with power loss and other effects. On the receiver side, a PD is employed to convert the detected optical power into current. The noise of the PD and TIA [2] is also added to the received current. The output current of the PD and TIA is then digitalized through an analog to digital converter (ADC), which is demodulated and

decoded by the receiver's digital baseband. Finally, the PRBS sequence is recovered and is compared with the original PRBS sequence to calculate the BER and the symbol error rate (SER).

Based on the previous system, the SNR measurement and BAE algorithm can be added as shown in Fig. 24. In addition to the forward transmission of the data package mentioned previously, a feedback path is added to transmit the BEA result from the receiver to the transmitter. Before the data package transmission, a training sequence, which is known by the transmitter and receiver, is transmitted for the EVM and SNR calculation. The method of EVM and SNR calculation is introduced in Section 4.2.3. Then, the calculated SNR is provided to the BEA module to calculate the number of BEA scaling factors of each subcarrier. The detail of the allocation algorithm is presented in Section 4.3.4.

4.2.2 Principle of DCO-OFDM

Different from conventional OFDM used in RF communication, real and positive output is needed for the VLC system because IM/DD is used. Section 2.3.2 introduces many modified OFDMs for the VLC systems. DCO-OFDM is used in our proposed system because of the higher spectrum efficiency compared with ACO-OFDM and PAM-DMT, but a DC bias is needed to make sure the output is positive. Section 4.2.2 gives the mathematical derivation to show why the output of DCO-OFDM is real and what the output is.

N points IFFT is used in the proposed transmitter, which means there are $(N-1)/2$ subcarriers in each OFDM frame. To make it is easier to understand, the modulation scheme of the 1st, 2nd, 3rd and $N/2-2$ subcarrier is assumed to be 1024, 256, 64 and 2 QAM, respectively, and there is no bits loading on the $N/2-1$ subcarrier. The energy scaling factor of each subcarrier is e_n, where n is the subcarrier index.

$$B=\begin{bmatrix} b_1 & b_{11} & b_{19} & \cdots & b_K & 0 \\ \cdots & \cdots & \cdots & \cdots & \cdots & 0 \\ b_7 & b_{17} & 0 & \cdots & 0 & 0 \\ b_8 & b_{18} & 0 & \cdots & 0 & 0 \\ b_9 & 0 & 0 & \cdots & 0 & 0 \\ b_{10} & 0 & 0 & \cdots & 0 & 0 \end{bmatrix} \tag{4.1}$$

The bit sequence is written as $B=[b_1,b_2,b_3,\cdots,b_k,\cdots,b_K]$, where b_k equals 0 or 1 and K is the total bit number in one OFDM frame. Then, the sequence is paralleled according to the modulation scheme of each subcarrier. The paralleled matrix is shown in Eq. (4.1), where the row number is the maximum bit number of each symbol and the column is the subcarrier

number. If the required bit number of a specific subcarrier required is less than the maximum bit number, zero is padded. The effective bits of each row are mapped into the symbol according to the constellation of the corresponding modulation scheme. The average energy of each subcarrier is set to one in the digital processing, and then the energy scaling factor is applied on the modulated symbols to complete the energy loading. The symbols of one OFDM frame are shown in Eq. (4.2):

$$X = [\sqrt{\frac{e_1}{2}}X_1, \sqrt{\frac{e_2}{2}}X_2, \cdots, \sqrt{\frac{e_n}{2}}X_n, \cdots, \sqrt{\frac{e_{N/2-1}}{2}}X_{N/2-1}] \ . \tag{4.2}$$

A typical data package structure before IFFT and Hermitian symmetry is illustrated in Fig. 25, where the x- and y-axis represents the time and frequency domain, respectively.

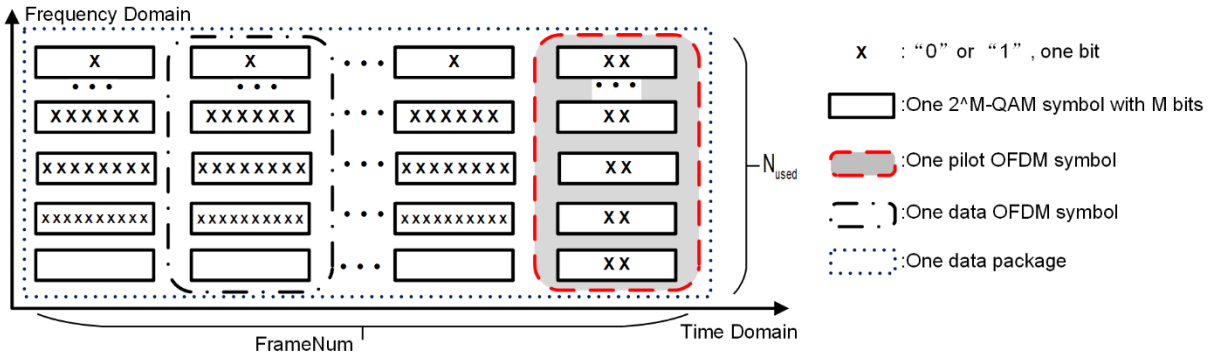

Fig. 25 Data package in the time and frequency domain.

Then, a vector of length N is constructed based on the symbols of one OFDM frame. We call this process Hermitian symmetry. The structure of the constructed vector is shown in Eq. (4.3):

$$X = [0, \sqrt{\frac{e_1}{2}}X_1, \cdots, \sqrt{\frac{e_{N/2-1}}{2}}X_{N/2-1}, 0, \sqrt{\frac{e_{N/2-1}}{2}}X^*_{N/2-1}, \cdots, \sqrt{\frac{e_1}{2}}X^*_1] \ . \tag{4.3}$$

After that, N point IFFT is applied to transform the signal from the frequency domain to the time domain. Then, a cyclic prefix with length N_{CP} is added to avoid the ISI and synchronization offset compensation. The OFDM frame in the time domain can finally be presented as Eq. (4.4):

$$x(k) = \frac{1}{N}\sum_{n=0}^{N-1} X(n) e^{\frac{-j2\pi n \times mod(k,N)}{N}} \ , \tag{4.4}$$

where k is the sampling index ranging from 0 to $N + N_{CP} - 1$.

Fig. 26 shows the data flow of the transmitter. The generated PRBS data sequence is reshaped into $B_{total} \times FrameNum$, where B_{total} is the total bit number in one OFDM symbol and can be calculated by Eq. (4.5):

$$B_{total} = \sum_{n=1}^{N/2-1} b_n \ , \tag{4.5}$$

where b_n is the bit number on the n_{th} subcarrier and B_{total} is the total OFDM symbols number in one data package. Then, the bits on each subcarrier used are mapped into a QAM symbol with 2^{b_n} modulation order. The dimension of the output matrix becomes $(N/2-1) \times FrameNum$. After performing Hermitian symmetry, IFFT, cyclic prefix (CP) insertion and matrix reshaping again, the generated sequence combined with the pilot sequence is output by the digital baseband on the transmitter side.

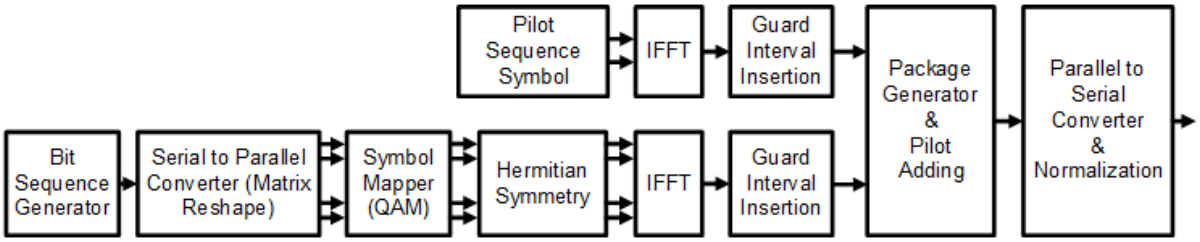

Fig. 26 Data path of the transmitter baseband.

The data path of the receiver is presented in Fig. 27. The pilot and the data sequence are firstly separated. Then, the pilot sequence is used for synchronization and channel estimation, and the result of the channel estimation is used to recover the transmitted data sequence based on the received signal.

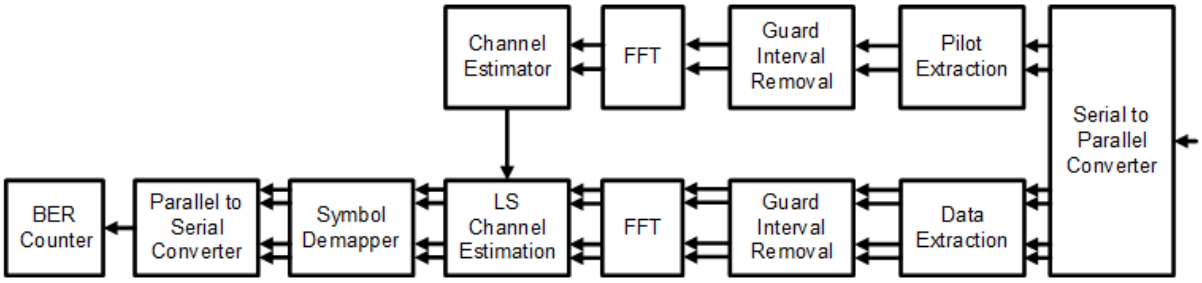

Fig. 27 Data path of the receiver baseband.

The mathematical explanation of why the IFFT output of the sequence after Hermitian symmetry is real is given below. In order to make it easier to understand, the influence of N_{CP} is temporarily ignored in the following derivation.

The relationship between the time domain and frequency domain signal is shown in Eq. (4.6):

$$x(k)=\frac{1}{N}\sum_{n=0}^{N-1}X(n)e^{\frac{j2\pi kn}{N}}\ , \tag{4.6}$$

where $x(k)$, $X(n)$ and N is the sampling signal in time domain, the signal in the frequency domain and the number of DFTs, respectively. Eq. (4.6) can be split into two parts, as shown as Eq. (4.7):

$$x(k)=\frac{1}{N}[\sum_{n=0}^{N/2-1}X(n)e^{\frac{j2\pi nk}{N}}+\sum_{n=N/2}^{N-1}X(n)e^{\frac{j2\pi nk}{N}}]\ . \tag{4.7}$$

A DCO-OFDM symbol structure after Hermitian symmetry in time domain is

$$X=[0,X(1),\cdots,X(N/2-1),0,X(N/2+1),\cdots,X(N-1)], \tag{4.8}$$

where $X^*(N-n)=X(n), n=1,2,\cdots,N/2-1 \, or \, n=N/2+1,\cdots,N-1$. Substitute Eq. (4.8) into Eq. (4.7), we can get Eq. (4.9):

$$x(k)=\frac{1}{N}[\sum_{n=1}^{N/2-1}X(n)e^{\frac{j2\pi nk}{N}}+\sum_{n=N/2+1}^{N-1}X^*(N-n)e^{\frac{j2\pi nk}{N}}]\ . \tag{4.9}$$

Let $k'=N-k$, and Eq. (4.9) can be rewritten into Eq. (4.10):

$$\begin{aligned} &x(k)\frac{1}{N}[\sum_{n=1}^{N/2-1}X(n)e^{\frac{j2\pi nk}{N}}+\sum_{n'=1}^{N/2-1}X^*(n')e^{\frac{j2\pi k(N-n')}{N}}] \\ &=\frac{1}{N}[\sum_{n=1}^{N/2-1}X(n)e^{\frac{j2\pi nk}{N}}+\sum_{k=1}^{N/2-1}X^*(n)e^{-\frac{j2\pi nk}{N}}] \end{aligned}\ . \tag{4.10}$$

Then let $X(n)=\mathbf{Re}(X(n))+\mathbf{Im}(X(n))$, so we get

$$X^*(n)=\mathbf{Re}(X(n))-\mathbf{Im}(X(n))\ . \tag{4.11}$$

And according to Euler rules,

$$\begin{aligned} e^{\frac{j2\pi nk}{N}}&=\cos(\frac{2\pi}{N}kn)+j\sin(\frac{2\pi}{N}kn) \\ e^{-\frac{j2\pi nk}{N}}&=\cos(\frac{2\pi}{N}kn)-j\sin(\frac{2\pi}{N}kn) \end{aligned}\ . \tag{4.12}$$

Substitute Eq. (4.11) and Eq. (4.12) into Eq. (4.10) and then simplify to get Eq. (4.13):

$$\begin{aligned} x(k)&=\frac{1}{N}\sum_{n=1}^{N/2-1}[(\mathbf{Re}(X(n))+j\mathbf{Im}(X(n)))(\cos(\frac{2\pi}{N}kn)+j\sin(\frac{2\pi}{N}kn)) \\ &+(\mathbf{Re}(X(n))-j\mathbf{Im}(X(n)))(\cos(\frac{2\pi}{N}kn)-j\sin(\frac{2\pi}{N}kn))] \\ &=\frac{2}{N}[\sum_{n=1}^{N/2-1}(\mathbf{Re}(X(n))\times\cos(\frac{2\pi}{N}kn))-\sum_{n=1}^{N/2-1}(\mathbf{Im}(X(n))\times\sin(\frac{2\pi}{N}kn))] \end{aligned}\ . \tag{4.13}$$

Therefore, the time domain signal after IFFT is real and can be used in the VLC system employing IM/DD transmission.

4.2.3 SNR Estimation Algorithm

A training sequence is employed to estimate the SNR in our design. The SNR is defined as the ratio of the signal power and the noise power, and it can be approximated by Eq. (4.14) when the measured symbol number is much larger than the categories of the modulation symbols:

$$\mathrm{SNR} = \frac{P_{signal}}{P_{noise}} = \frac{1/N\sum_{n=1}^{N}(V_{I,n})^2 + (V_{Q,n})^2}{1/N\sum_{n=1}^{N}(n_{I,n})^2 + (n_{Q,n})^2}, \tag{4.14}$$

where N is the total number of measured symbols, $V_{I,n}$ and $V_{Q,n}$ is the in-phase amplitude and the quadrature signal amplitude, respectively, of the M-ary modulation, and $n_{I,n}$ and $n_{Q,n}$ is the in-phase amplitude and the quadrature noise amplitude, respectively, of the complex noise being considered [3].

An error vector is a vector in the I-Q plane between the ideal constellation point and the point received by the receiver. It is measured using Eq. (4.15):

$$EVM_{RMS} = \left[\frac{1/N\sum_{n=1}^{N}|I_n - I_{0,n}|^2 + |Q_n - Q_{0,n}|^2}{1/M\sum_{m=1}^{M}[(I_{0,m})^2 + (Q_{0,m})^2]}\right]^{1/2}, \tag{4.15}$$

where $\mathrm{I_n} = (\mathrm{V_{I_n}})|\mathrm{A}|$ and $Q_n = (V_{Q_n})|A|$ is the normalized in-phase voltage and quadrature voltage, respectively, for the measured symbols, $I_{0,m} = (V_{I_{0,m}})|A_0|$, and $Q_{0,m} = (V_{Q_{0,m}})|A_0|$ is the normalized in-phase voltage and quadrature voltage, respectively, of the ideal symbols in the constellation.

When $N \gg M$, which means the number of the measured symbols is much larger than that of the modulation symbol categories, Eq. (4.16) can be derived. In the proposed model, Eq. (4.15) is employed to calculate the EVM and Eq. (4.16) is then applied to get the SNR of each subcarrier.

$$\mathrm{SNR} \approx \frac{1}{\mathrm{EVM}^2} \tag{4.16}$$

4.2.4 Bit and Energy Allocation Algorithm

Using the SNR result in Section 4.2.3, the bit number and energy scaling factor can be decided, which can be abstracted as an optimization problem. According to the different constraints and objective function, this problem can be divided into three situations for discussion, and the three situations correspond to different algorithms.

The first case is bit error rate adaptive (BA), which means the minimum bit error rate for a fixed data rate and transmit energy, as in Eq. (4.17):

$$\min(BER), \text{subject to } \sum_{n=1}^{N_{used}} e_n(b_n) \le E_{target} \text{ and } \sum_{n=1}^{N_{used}} b_n = B_{total} \ . \tag{4.17}$$

The second case is rate adaptive (RA), which means the maximum data rate for a fixed energy constraint, as in Eq. (4.18):

$$\max(B_{total}) = \max\left(b \in Z_+^N, \sum_{n=1}^{N_{used}} b_n \right), \text{subject to } \sum_{n=1}^{N_{used}} e_n(b_n) \le E_{target} \ . \tag{4.18}$$

The third case is margin adaptive (MA), which means the maximum energy margin for a fixed rate constraint, as in Eq. (4.19):

$$\min(E_{total}) = \min\left(b \in Z_+^N, \sum_{n=1}^{N_{used}} e_n(b_n) \right), \text{subject to } \sum_{n=1}^{N_{used}} b_n = B_{target} \ . \tag{4.19}$$

TABLE IV. lists different kinds of allocation algorithms and their categories. In our proposed system, when the analog frontend is determined, the output energy of the signal is constraint. Therefore, both the BA and RA can be used.

TABLE IV. ALGORITHM FOR BIT AND ENERGY ALLOCATION

Algorithm Name	Category	Complexity
Water pouring [4]	RA/MA	-
Hughes Hartogs [5]	MA	$O(N \times B_{total})$
Chow Cloffi [6]	MA	$O(N \times \text{Iterate}_{\max} + 2N)$
Jorge Campello [7-9]	MA	$O(N)$
Robert Fischer [10]	BA	-
Levin Campello	MA/RA	$O(N)$

BA is finally used in the proposed system. Both the transmission energy and rate are constrained, and the bit and energy scaling factor are allocated on each subcarrier to minimize the bit error rate. The basic principle of the algorithm is briefly introduced below.

Considering N_{used} subcarriers are used as independent channels, as shown in Fig. 28 (a), where e_n is the normalized energy, N_n is the noise variance and n is the index of the subcarrier used, the symbol error rate of the n_{th} subcarrier can be calculated with Eq. (4.20):

$$\mathrm{Pr}_n = K_n \times Q\left(\sqrt{\frac{d_n^2/4}{N_n/2}}\right) \tag{4.20}$$

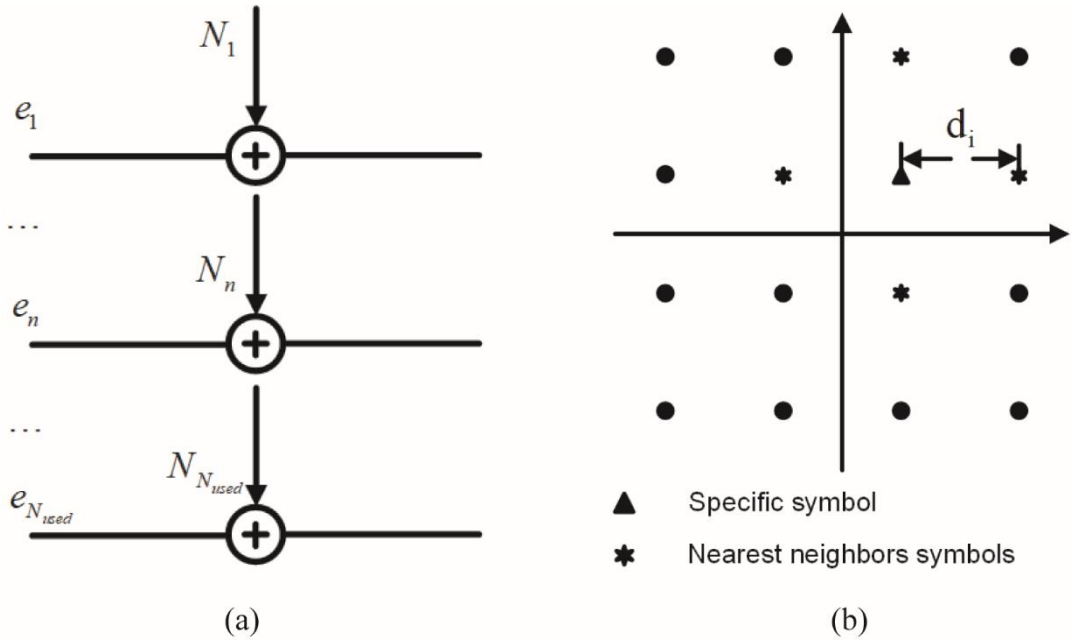

Fig. 28 (a) Equivalent independent channels of each subcarrier. (b) Signal constellation of one subcarrier.

The optimum situation is that all subcarriers have the same bit error rate. When K_n is assumed to be equal for all used subcarriers, the optimum situation can be expressed as Eq. (4.21):

$$\frac{d_n^2/4}{N_n/2} =: SNR_0 \overset{!}{=} const., \quad i = 1, 2, \cdots, N_{used} \ . \tag{4.21}$$

Therefore, the BEA algorithm is transferred to an optimization problem, which is given by Eq. (4.22):

$$\frac{V_n^2}{N_n/2} = SNR_0 \rightarrow max \ , \tag{4.22}$$

where $V_n = d_n^2/4$ under the constraint of Eq. (4.23) and Eq. (4.24), where

$$B_{total} = \sum_{n=1}^{N_{used}} b_n \overset{!}{=} const. \tag{4.23}$$

$$E_{total} = \sum_{n=1}^{N_{used}} e_n \overset{!}{=} const. \tag{4.24}$$

After the continuous approximation and Lagrange optimization, we can get the allocated bit number on each subcarrier as in Eq. (4.25):

$$b_n = \frac{B_{total}}{N_{used}} + \frac{1}{N_{used}} \times log2(\prod_{l=1}^{N_{used}} N_l / N_n^{N_{used}}) \ . \tag{4.25}$$

In the above calculation, the subcarrier whose b_n is non-positive will be discarded, and the calculation is repeated until the b_i of all the subcarriers used are positive. The number of subcarriers finally used is denoted as N_{used}, and the corresponding indices are compromised in the set L. Then b_n is quantized to be an integer as shown with Eq. (4.26):

$$b_{Qn} = \begin{cases} b_{max} & b > b_{max} - 0.5 \\ INT(b + 0.5) & 0.5 \le b \le b_{max} - 0.5, n \in L \\ 0 & b < 0.5 \end{cases} . \tag{4.26}$$

Under the constraint of Eq. (4.22), the energy allocated on each subcarrier finally used can be calculated as Eq. (4.27):

$$e_n = \frac{E_{total} \times N_n \times 2^{b_{Qn}}}{\sum_{l \in L} N_l \times 2^{b_{Qn}}}, n \in L \ . \tag{4.27}$$

4.3 Real-time Transmitter Design and Implementation

4.3.1 Introduction

In Section 4.3, we focus on how to design a digital circuit to realize the OFDM supporting BEA algorithm in real-time with the lowest time delay. Relying on the handshake protocols and ping-pong operation through dual-port random access memories (RAMs), the OFDM frame can be generated without any interruption when the bit number and energy scaling factor on each subcarrier is determined. Additionally, the training sequence and the pilot subcarrier is also added for frame synchronization, symbol synchronization, channel estimation and sampling offset compensation. The frontend circuit consisting of the discrete components is also designed to build a VLC transceiver system for the experiment.

The system structure, clock tree and reset tree design are elaborated in Section 4.3.2. The detailed circuit of the key modules inner transmitter and the behavior simulation result are presented in Section 4.3.3. The implementation of the experiment setup for the designed transmitter testing and the experiment result are shown in Section 4.3.4.

4.3.2 System Structure

This section introduces the system architecture of the proposed transmitter. The bit sequence to be transmitted is the input and the signal sample to the digital to analog converter (DAC) is the output. After a whole picture of the proposed transmitter is draw in this section, the details of each submodule of the transmitter, especially the modulator and Hermitian symmetry module supporting the DCO-OFDM with BEA in different subcarriers, which are different from the conventional design, are presented in the following section.

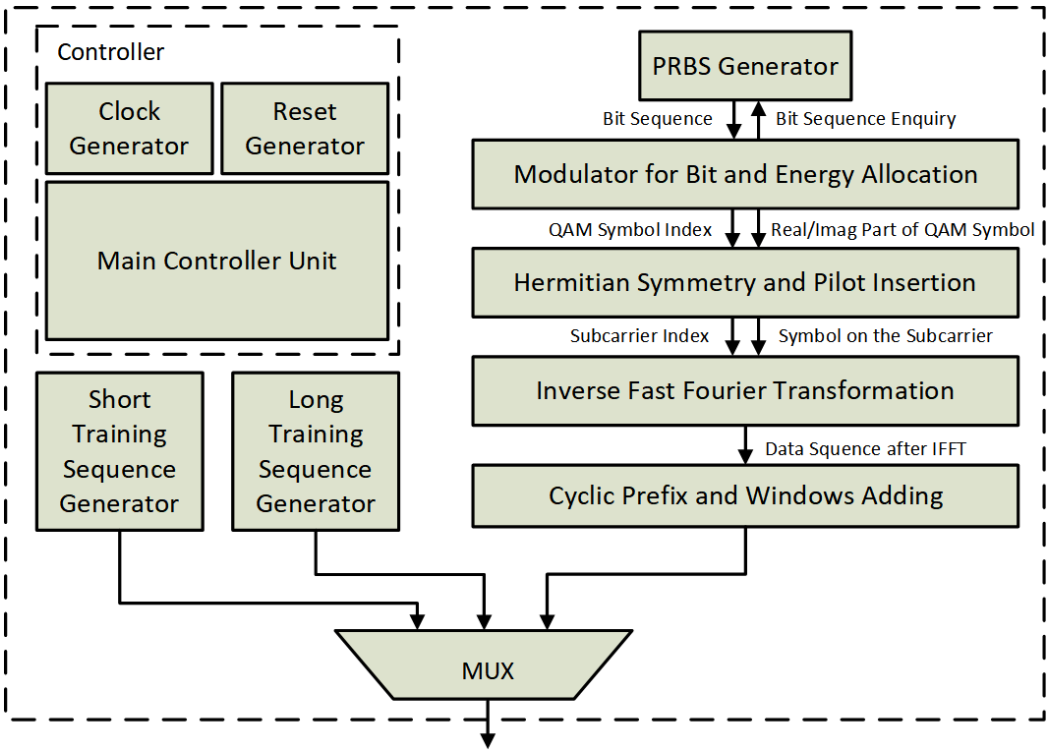

Fig. 29 The system diagram of the proposed transmitter.

Fig. 29 shows the structure of the proposed transmitter. The input of the transmitter is the bit sequence loading effective information. A PRBS generator is used for performance evaluation. The generated PRBS sequences is firstly paralleled for constellation mapping. The amplitude of the constellation is decided by the energy scaling factor. The modulation scheme and the energy scaling factor are both decided by the result of the BEA algorithm from the receiver side. Then, Hermitian symmetry needs to be done on the symbols of the OFDM frame. After that, an IFFT transforms the symbols from the frequency domain to the time domain. Finally, CP and windows are added to reduce the inter symbol interference (ISI) and band leakage. The submodules communicate with each other through an AXI stream bus. The AXI stream protocol means the data on the bus cannot transmit until both the data valid signal from the master side and the data ready signal from the slave side are active, which ensures the stability of data transmission.

The highest modulation scheme supported by the proposed transmitter is QAM-1024, which means there are up to 10 bits on each subcarrier. Therefore, the clock frequency of the serial sequence is ten times the symbol clock frequency. After Hermitian symmetry, the symbols number of each OFDM frame is doubled, which means the clock frequency is also doubled. The serial, symbol, and system clock signals with a specific frequency relationship are generated by a clock generator from external clock source for different parts of the transmitter. The synchronous reset signal is also needed for the different clock domains, which are generated by the reset generator when the global asynchronous reset input is active or when the transmitter is rebooted. The clock and reset tree are shown in Fig. 30.

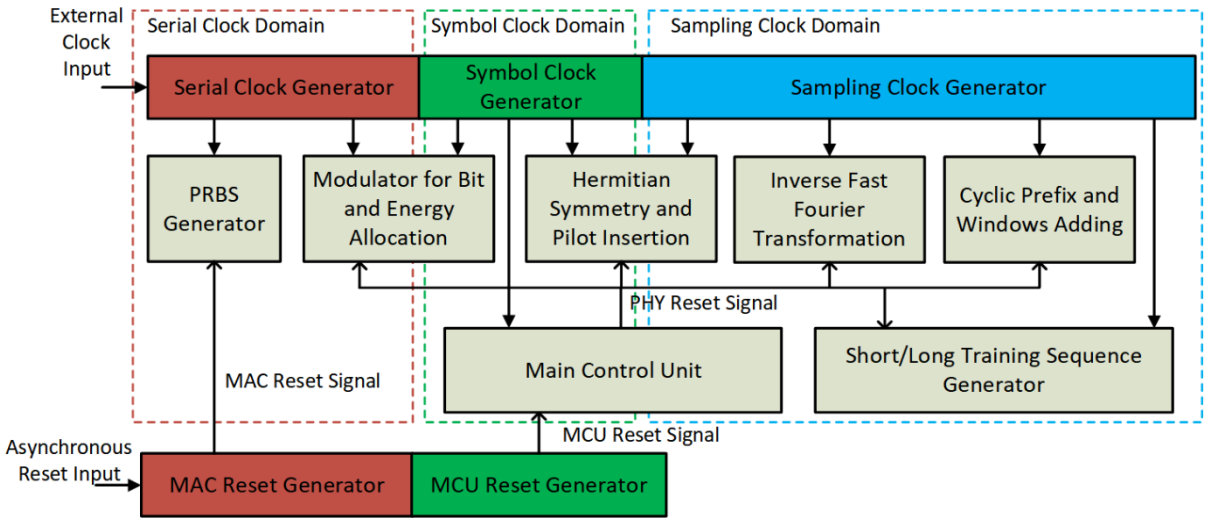

Fig. 30 Clock and reset tree of the transmitter.

Fig. 31 shows the structure of the main control unit (MCU) in our proposed transmitter. An finite-state machine (FSM) with three states is the core of the MCU. When 'SEND ENABLE' is active, the state of the FSM transits from 'IDLE' to 'Transmitting'. 'PHY RESET' is firstly active to reset other submodules. Then, the counters begin to work to generate the request signal in the correct sequence. 'STS REQ', 'LTS REQ' and 'DATA REQ' is used to order the short training sequence generator, long training sequence generator and data sequence generator to begin to work, separately. The state of FSM transits to 'Transmission Done' when the 'TRANSMISSION DONE' is active, which is generated by the data sequence generator. Then, the state transits to 'IDLE' again to wait for the next transmission. The clock and reset generator and MCU constitute the controller unit.

The training sequence including short training sequence (STS) and long training sequence (LTS) are transmitted before data package transformation. The STS is used for frame synchronization and the LTS is used for symbol synchronization and channel estimation. The

STS, LTS and data package are connected to the output of the transmitter through a multiplexer which is controlled by the MCU.

The structure of the STS in the frequency domain is shown in Eq. (4.28):

$$\begin{aligned} X_{STS} &= \sqrt{21/8} \times \\ &[0,0,0,0,0,0,0,1+j,0,0,0,-1-j,0,0,0,1+j,0,0,0,-1-j,0, \\ &0,0,-1-j,0,0,0,1+j,0,0,0,0,0,0,-1-j,0,0,0,-1-j,0,0,0, \\ &1+j,0,0,0,1+j,0,0,0,1+j,0,0,0,1+j,0,0,0,0,0,0,0,0] \end{aligned} \quad . \tag{4.28}$$

There is a symbol every three zeros in the frequency domain, which ensures the periodicity of the generated sequence in the time domain. After the Hermitian symmetry and IFFT transformation on Eq. (4.4), a sequence consisting of four repeated short sequences is generated. There are totally ten repeated short sequences in the STS we used, and the coefficient is multiplied to each symbol in the frequency domain to ensure that the total power of STS is consistent with the following signal [11].

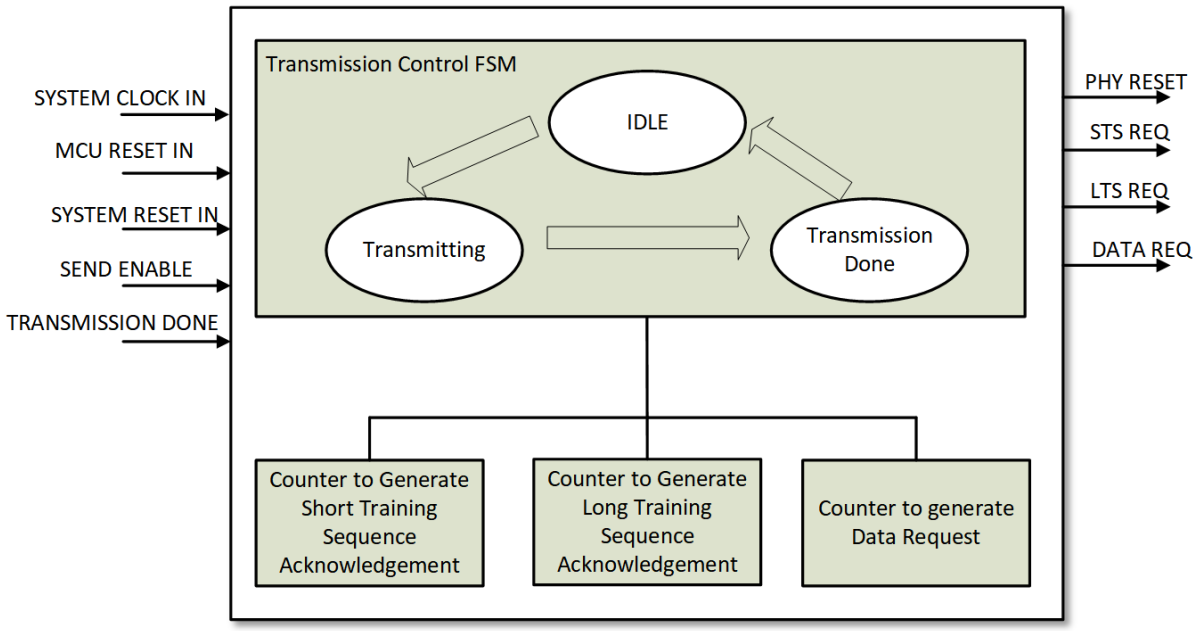

Fig. 31 Structure of the main control unit.

Due to the easy implementation and low power to average ratio (PAPR), a Shapiro-Rudin sequence is generated as the LTS in the frequency domain [12]. The sequence begins with the array, $X_{LST} = [1,1]$, and repeatedly concatenates a copy of this array but changing the sign of its second half until the length we want. For example, $X_{LST} = [1,1,1,-1,1,1,-1,1]$ when the length is 8.

The Hermitian symmetry and IFFT calculation for both STS and LTS are pre-calculated and the result is stored in two single-port RAMs. Counters with specific conditions are used to

generate the address to pick the calculated result in the correct order repeating for a specified number of times. Then the training sequence is generated.

4.3.3 Module Implementation and Behavior Simulation Result

The most significant innovation of the proposed transmitter design is supporting OFDM with bit and energy allocation in real-time. Therefore, how to design a modulator to generate symbols employing different modulation schemes and energy scaling factors for a specific subcarrier of one OFDM frame is the most challenge part of the whole transmitter design. Additionally, the proposed transmitter is designed for VLC, so the final output from the digital baseband must be real. Therefore, a Hermitian symmetry module supporting consecutive input and output streaming without interruption is another essential part. This section illustrates the working principle and detailed structure of these two modules. The behavior simulation results are also presented to show the effectiveness of the proposed design.

4.3.3.1 Modulator Design

The schematic of the detailed structure of the modulator with an inner PRBS generator is shown in Fig. 32. The whole transmitter consists of three main functional blocks. An FSM with two states receives the data request signal from the MCU then controls the workflow of the modulator. A 10 bits shift register with serial input and parallel output is used to transform the bit sequence from serial into parallel and adds 0 padding when the required bit number of the specific subcarrier is less than 10. The final block is used to map the parallel bits into a QAM symbol and multiply the scaling factor to the mapped symbol according to the allocated energy scaling factor result. Except for the three functional blocks, two dual-port RAMs are also included to store the bit number and energy scaling factor for each subcarrier. A feedback shift register is also included to generate the PRBS sequence to do the design verification performance testing.

This part describes how to generate one OFDM frame after receiving the data request signal from the MCU. When the data request signal is low, the FSM state keeps in ‘IDLE’, which means all blocks do not work. When the FSM detects high level on the data request wire, the state is transformed from ‘IDLE’ to ‘TRANS’. Then, the bit counter and subcarrier counter in the FSM begin to count. The bit counter counts from zero to nine. The subcarrier adds one when the bit counter completes one cycle counting. The subcarrier counts from zero to the number of used subcarriers predefined. The result of the subcarrier counters is used as the reading address of the RAM storing the bit number of each subcarrier. Then, the reading data of the RAM is compared with the delayed bit counter result. When the delayed bit counter result is

less than the bit number of the subcarrier, it means a new bit is needed. The data in ready signal for the PRBS generator is pulled high. The PRBS generator receives the signal and transmits one bit into the lowest bit of the shift register. When the delayed bit counter result is larger than the bit number of the subcarrier, the data in ready signal is pulled low. The PRBS generator stops to generate the bit and pulls down the data in a valid signal to control the multiplexer transmitting zero into the shift register as the padding. When the bit counter counts to zero again, which means all the bits of the shift register are refreshed, the data load enable signal is active to control the shift register to output all bits in parallel. Then, the subcarrier counter is updated and the bit counter counts from zero again until the subcarrier counter counts to the number of used subcarriers, which means the generation of one OFDM frame is done.

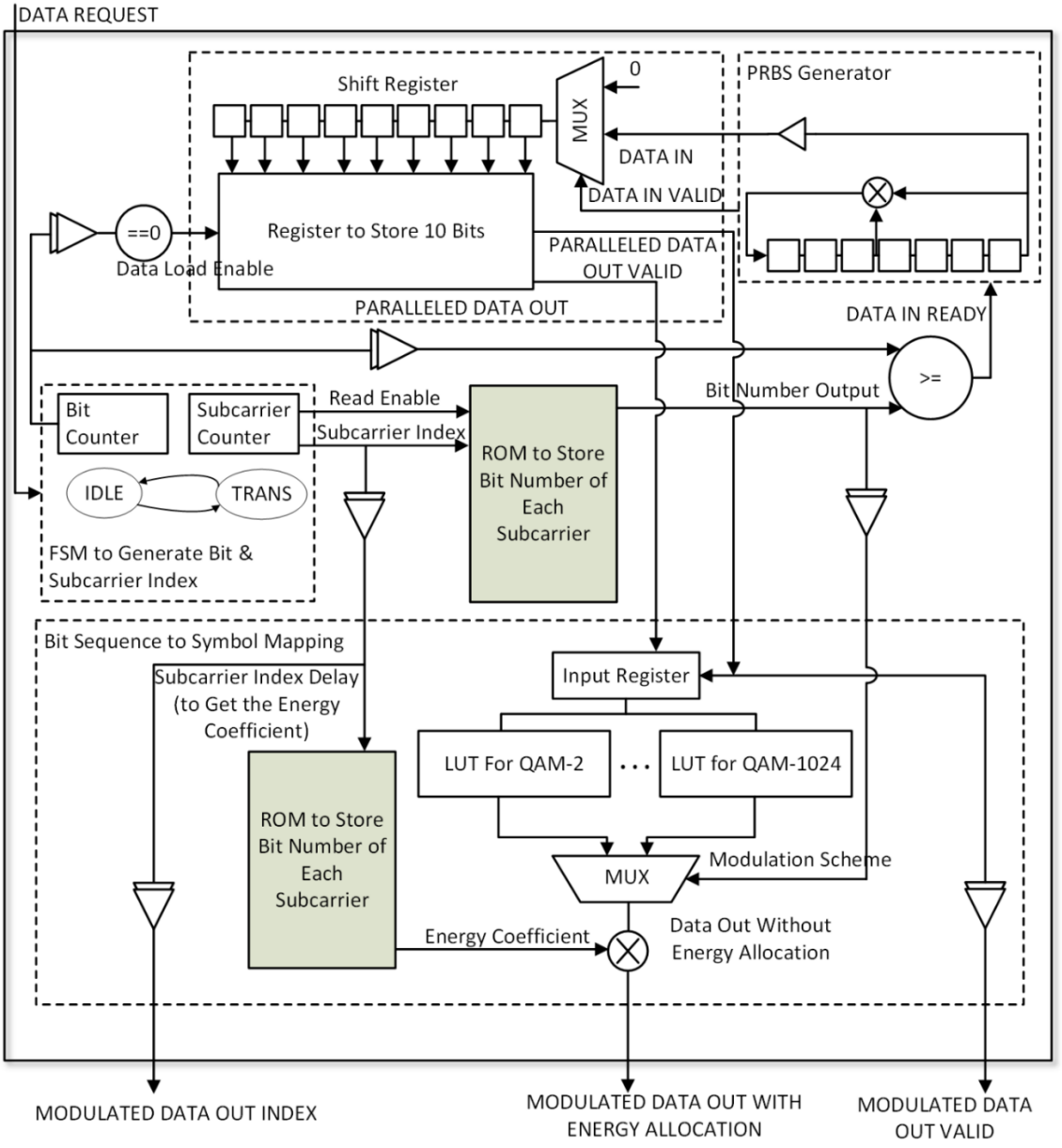

Fig. 32 Schematic of the proposed modulator.

The paralleled bits of each subcarrier are mapped into the signal symbol through the look up table (LUT) according to the modulation scheme, which is decided by the bit number of each subcarrier. Then, the mapped symbols multiply with an amplitude scaling factor decided by the energy scaling factor. The scaling factor is pre-written into another dual-port RAM. The reading address of the RAM is the output of the subcarrier counter with several clock cycles delay making the scaling factor align with the corresponding mapped symbol. The result of the multiplication is the modulation symbol with bit and energy allocation.

The behavioral simulation is done to verify the functional correctness of the proposed design. Fig. 33 shows the result of the simulation. After receiving the data request signal, the serial bit sequence begins to transmit with the active data in a valid signal. Then, the bit sequence is paralleled and then mapped to the modulated signal multiplied with the corresponding amplitude scale factor. The first nine subcarriers employ 64, 16 and 4 QAM separately with an amplitude scaling factor of 1. The last three subcarriers use 4 QAM with an amplitude scale factor 0.5.

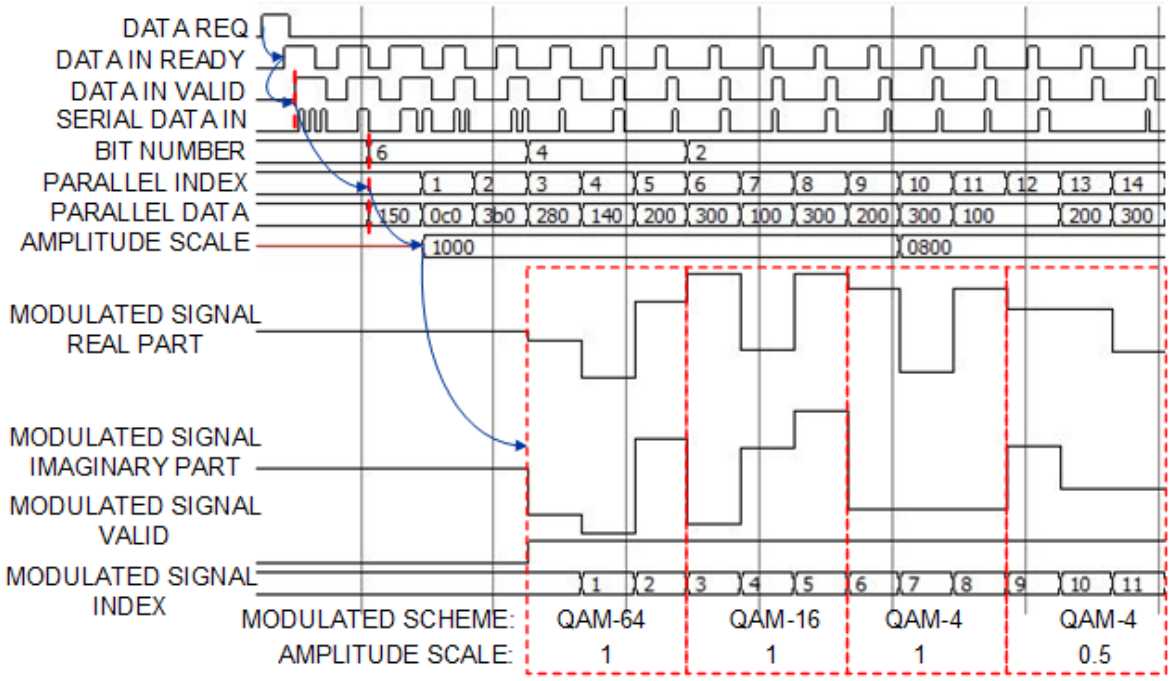

Fig. 33 Behavior simulation result of the proposed modulator.

4.3.3.2 Hermitian Symmetry Module

The symbol generated by the modulator presented by the last subsection is a complex number including a real and imaginary part. If the complex result is passed to the IFFT module directly, the IFFT result in the time domain is still complex, which cannot be transmitted through the LED channel employing IM/DD. Therefore, it is necessary to make the symbols in one OFDM frame meet the conjugate symmetry with $N/2$ as the center before IFFT.

In the proposed transmitter, 128-IFFT is used, which means 63 subcarriers are used in one OFDM frame. 4 out of 63 subcarriers are used to carry pilots in the frequency domain for sampling frequency offset compensation. In one OFDM frame period, there are totally 59 symbols streaming in from the modulator. After the DC subcarrier padding, pilot insertion and Hermitian symmetry, a vector with 128 symbols is streamed out for IFFT calculation.

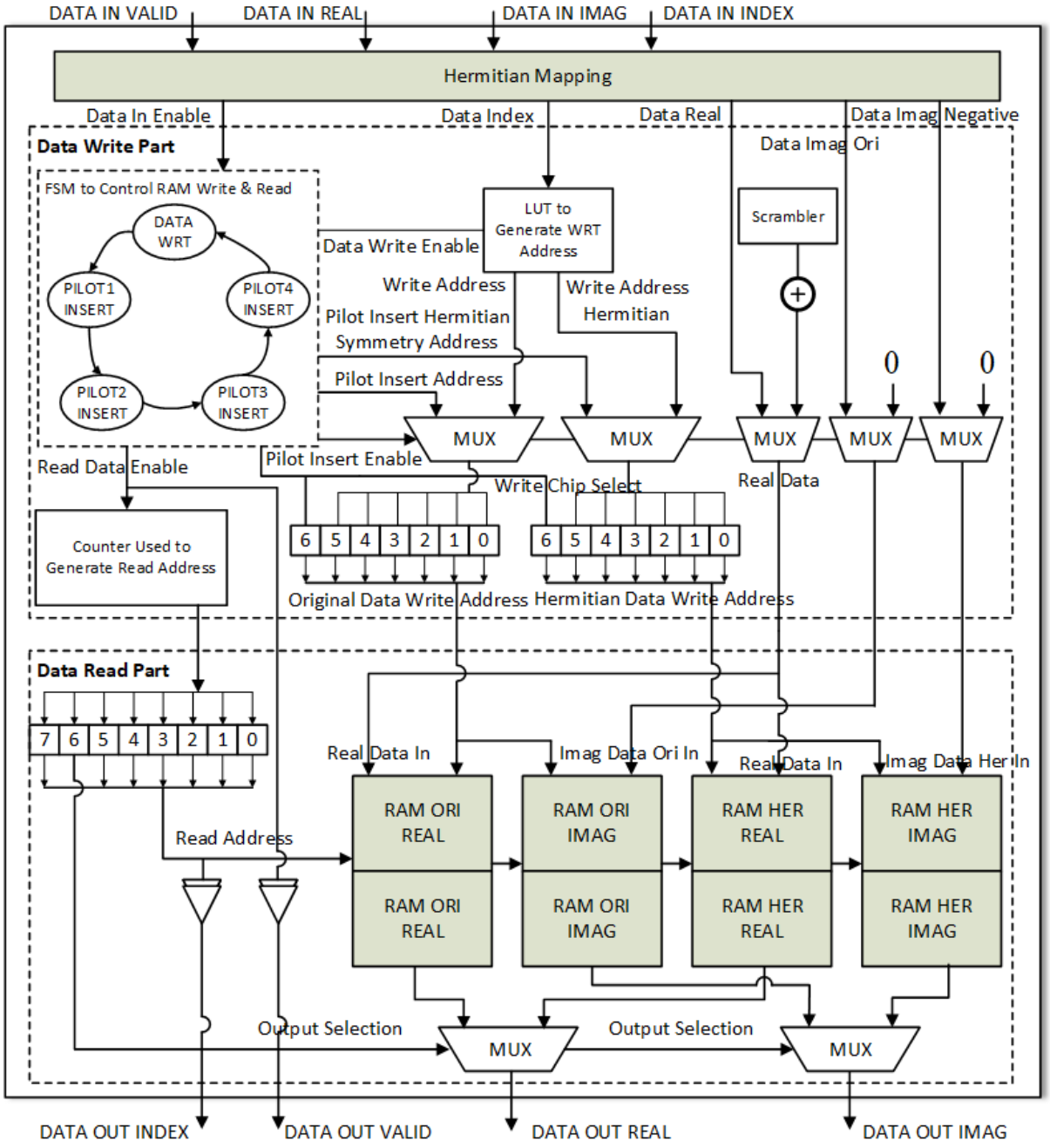

Fig. 34 Schematic of the proposed Hermitian symmetry module.

The detailed structure of the Hermitian symmetry module is shown as Fig. 34. The module consists of three main blocks. The Hermitian mapping block maps the complex input into its conjugate symmetry, which means the real part remains unchanged while the imaginary

part is inverted. The data writing block writes the original symbols, conjugate symmetry symbols and pilots to a specific location in the dual-port RAMs at a specific time. The data reading bock reads the symbols from the dual-port RAMs in order so the symbols meeting conjugate symmetry are streamed out. Four dual-RAMs with 128 depth are used to store and reorder the symbols. Two are used for the real and imaginary part of the original symbols and the other two are used for the conjugate symmetry symbols. Each RAM is divided into two parts with 64 depth so one half can read data at the same time the other writes.

After the functional block's introduction, this paragraph shows how these blocks cooperate with each other to complete one OFDM frame processing. There are 64 symbol clock cycles for one OFDM symbol. The data is transmitted in the first 59 cycles with the corresponding data index ranging from 0 to 58 and the data in valid signal active. The inverted imaginary part of the input is generated after the Hermitian mapping block while the other signals remain unchanged. The data in valid signal drives the FSM from the 'IDLE' to 'DATA_WRT' state. The data index is mapped to the lower 5 bits of RAM writing address through an LUT. For an example, the data index $[0,1,2,3,4,5,6,7,8\cdots]$ is mapped into $[1,2,3,4,5,6,8,9,10\cdots]$ for the RAM storing the original symbol input because address 0 is reserved for the DC subcarrier and address 7 is reserved for the first pilot in the frequency domain. It is mapped into $[64,63,62,60,59,58,57,56\cdots]$ for the RAM storing conjugate symbols because address 61 is reserved for the Hermitian symmetry of the first pilot. The highest bit of RAM writing address is controlled by the chip select signal from the FSM, so the top and bottom half is used for writing in turn. After all symbols in one OFDM frame are written in, the state of the FSM transforms from 'DARA_WRT' to 'PILOT_INSERT'. The pilot insert address and pilot data are switched in through the multiplexers, which are also controlled by the FSM. After the four pilot's insertion, the symbol writing for one OFDM frame is completed. Then, the read enable signal is active to drive the reading address generation counter begin to work. The counter is driven by the system clock, which is two times faster than the symbol clock used for data writing. The total depth of the reading counter is 7 bits, which means it can count from 0 to 255. 0-127 is for the one OFDM frame reading and 128-255 is for the following OFDM frame reading, so the highest bit is used for top and bottom half choosing. In the generated vector of one OFDM frame, 0-63 symbols are from the original symbol input and 64-127 symbols are from the conjugate symmetry result. Therefore, the second highest bit of the counter is used for switching the output between RAMs storing the original and conjugate symmetry symbols. The lower five bits is the reading address of the half RAMs. The

reading of the first OFDM frame occurs after the first OFDM frame writes in the top half of the RAMs, while the second OFDM frame can be writing in the bottom half of the RAMs at the same time. And then the second OFDM frame is reading and the third is overwriting the first one at the same time. Therefore, consecutive input and output streaming without any waiting time is supported in this design.

Fig. 35 shows the behavior simulation result of the Hermitian symmetry module. All the subcarriers employ QAM-4 and the amplitude scaling factors are all equal to 1 in this simulation to make the waveform clear. The output streams out after a delay of one OFDM frame length. The real part of the output is symmetrical while the imaginary part is opposite to it about N as the center. Additionally, the pilot is inserted into the $[7, 21, 43, 57]$ subcarrier. The real part of the pilot is 1 or -1 and the imaginary part is 0. The valid signal of the input and output is active when there are effective data on the data wire. The last signal of the output is active when one OFDM frame generation is finished. The generated vector is transmitted to the IFFT module for the frequency to time domain conversion. The imaginary part of the IFFT result is always zero, so the signal can be transmitted through the LED channel with IM/DD.

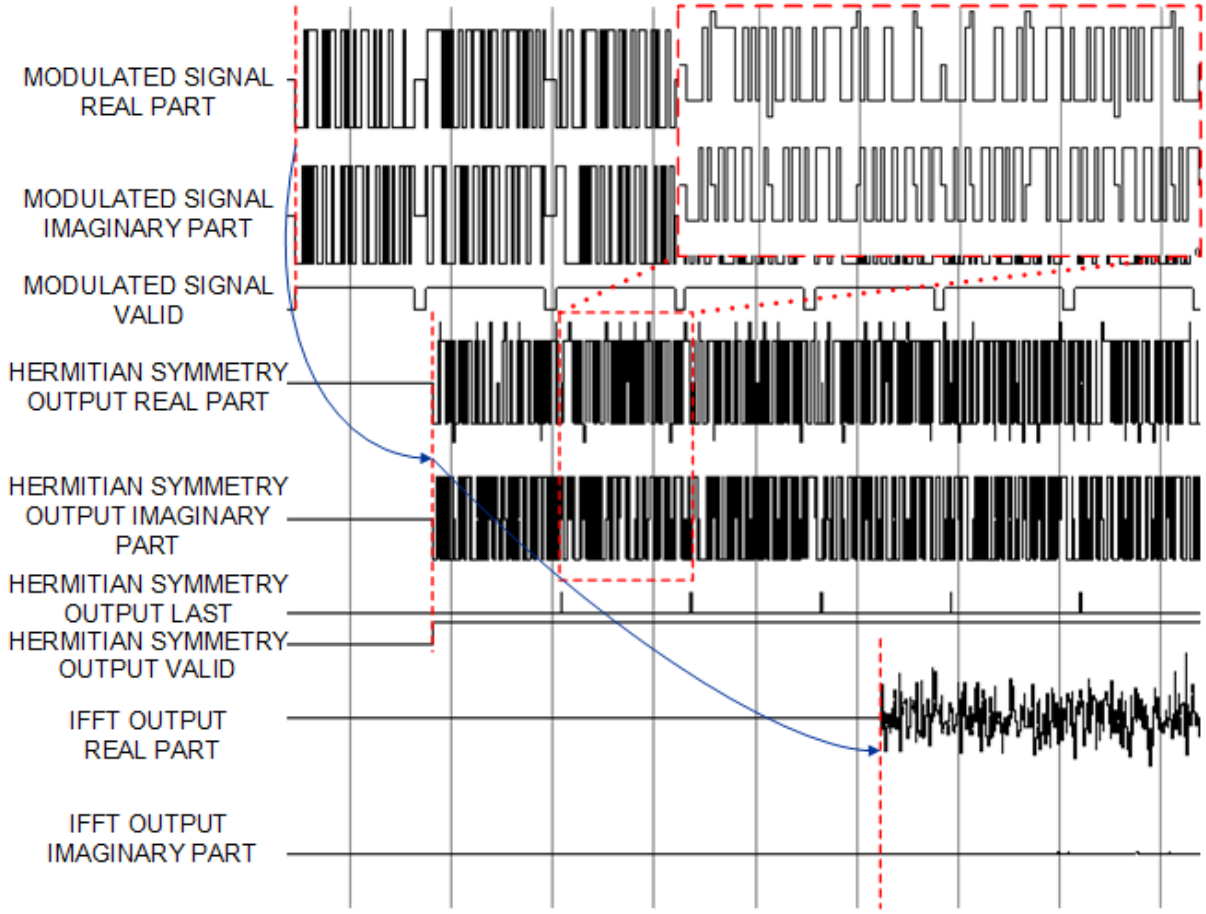

Fig. 35 Behavior simulation result of the proposed Hermitian symmetry module.

4.3.4 Experiment Setup and Result Discussion

Section 4.3.4 implements the transmitter design on FPGA. A VLC system is constructed based on the implemented transmitter. The performance of the constructed system is measured. The advantage of the bit and energy allocation algorithm usage in the DCO-OFDM VLC system is finally proved by the measurement result in the experiment.

4.3.4.1 Implementation of the Transmitter Design

The transmitter is implemented on an FPGA, which, in our experiment, is Artix-7 serials xc7a100tfgg484-2 from Xilinx. The power and resource utilization are listed in TABLE V.

TABLE V. RESOURCE UTILIZATION AND POWER CONSUMPTION

Item	Utilization	Percentage (%)
Look up table	3131	4.94
Look up table RAM	1022	5.38
Flip flops	5305	4.18
Block RAM	40	29.63
Digital processing unit	68	28.33
Power	0.23W	

4.3.4.2 The VLC System for the Experiment

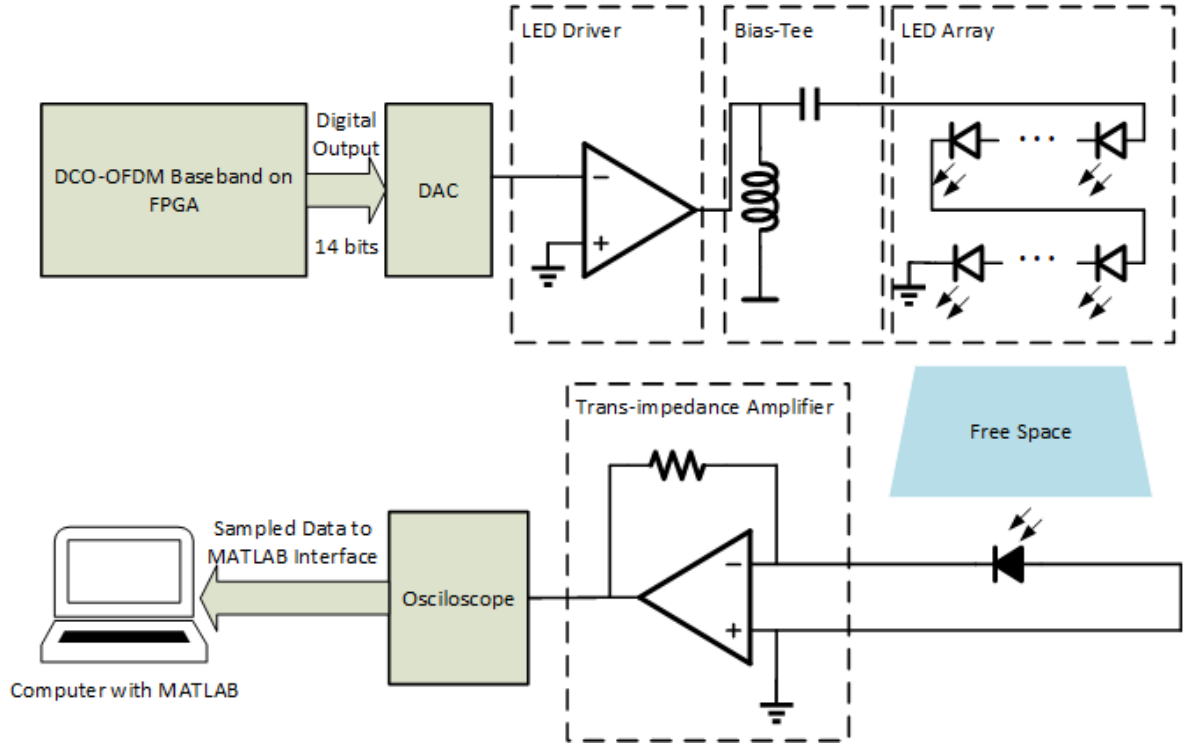

Fig. 36 System diagram of the experiment VLC system.

A real-time VLC system is constructed on the proposed transmitter. Fig. 36 is the diagram of the whole system including both the transmitter and receiver.

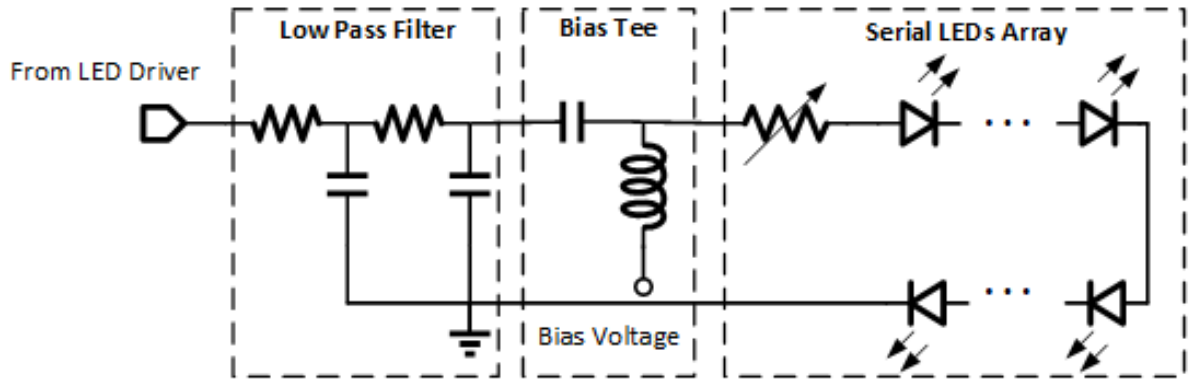

Fig. 37 Schematic of the transmitter frontend circuit

The generated digital signal from the baseband is transmitted to the DAC. Then, the analog signal is amplified by the LED driver. A DC bias is added to the amplified signal to make the LED work in the linear region. Nine LED beads are connected in series to form an LED array to transform the signal from the electrical to optical domain. Both the DAC module and LED driver are commercial products. The DC bias and LED array are integrated on a PCB. The schematic and picture is shown in Fig. 37 and Fig. 38 (a), respectively.

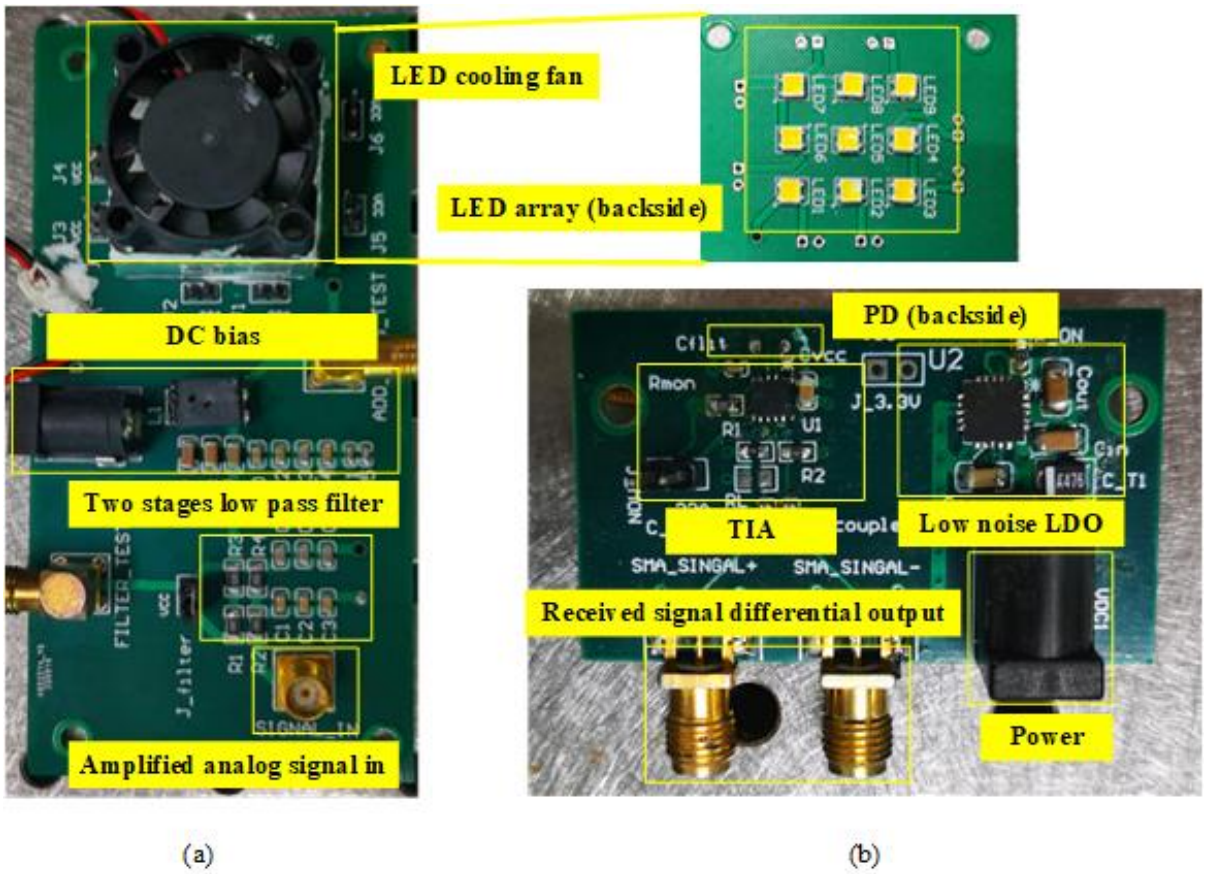

Fig. 38 Frontend Circuit of the (a) transmitter and (b) receiver.

The white light generated by the LED array goes through free space and is detected by the PD. The PD transforms the signal into current and it is amplified by the TIA. A frontend

circuit of the receiver side including PD, TIA, and a low noise LDO for the power supply are shown in Fig. 38 (b).

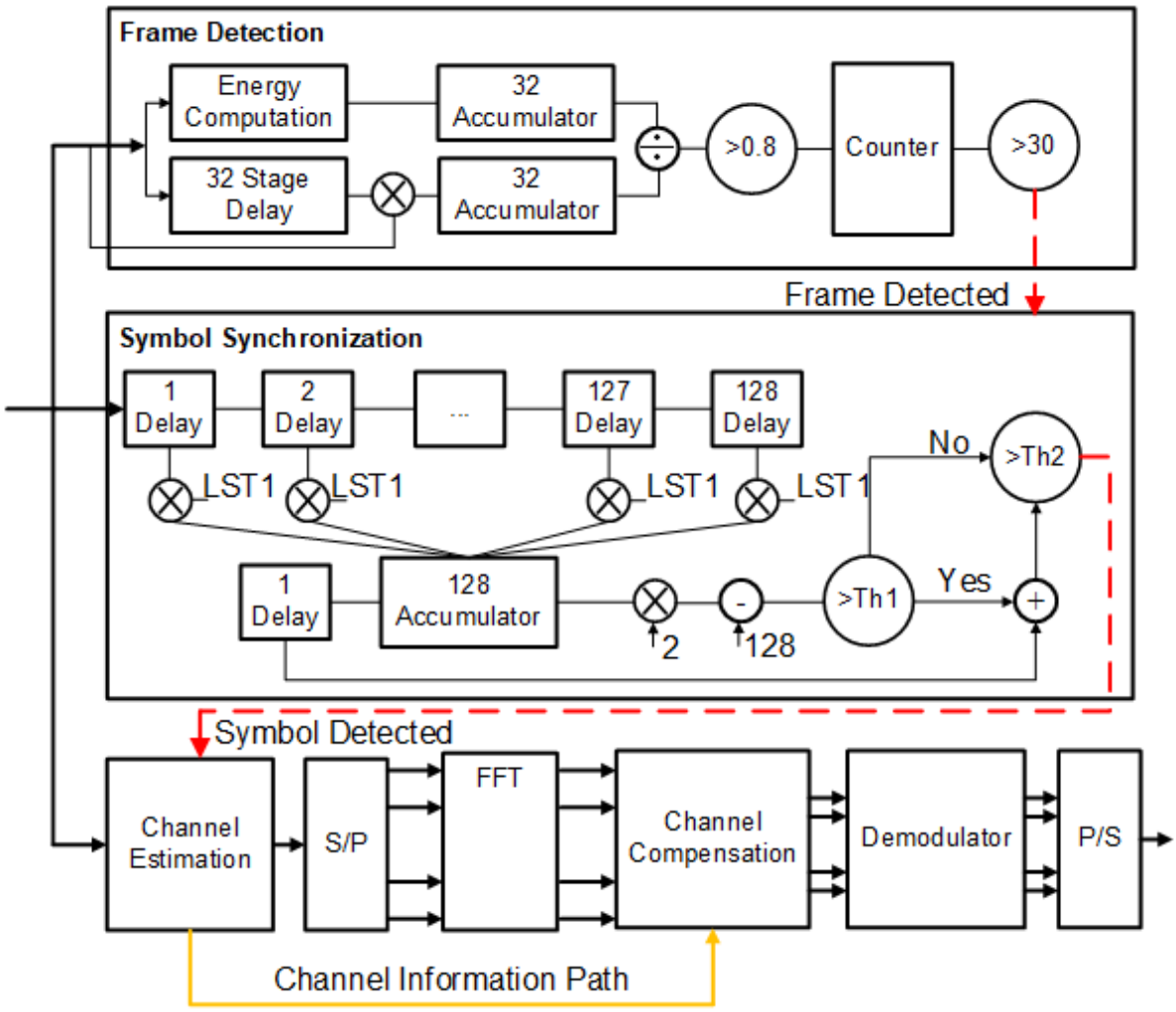

Fig. 39 Data flow of the offline receiver

The received signal after the TIA is captured and digitalized by an oscilloscope. The digitalized signal is transmitted to a laptop with MATLAB for further processing. Fig. 39 shows the flow of the data synchronization and signal processing. The frame detection module firstly detects whether there is a data package in the sampled data. The correlation is calculated between the input data and its 32-stage delay. Because the STS of the data package is periodic every 32 samples, the sum of 32 correlation results is maximum when the first 32 samples of the STS come in, and the ratio between the sum of the correlation and energy will be 1, theoretically. In our application, when the ratio is larger than 0.8 and lasts for 30 samples, we think the data package is detected. Then, symbol synchronization is activated to locate the accurate beginning place of the OFDM symbols. The sum of the 128-correlation result between the input data and LTS prestored in the receiver is calculated. A peak appears when the input sequence and the prestored 128 LTS symbols are totally matched. Then, the channel estimation,

FFT and demodulation begin to work. The bit sequence with effective information is recovered and the bit error rate can be calculated.

The experiment setup is shown in Fig. 40, and the components and equipment models are listed in TABLE VI.

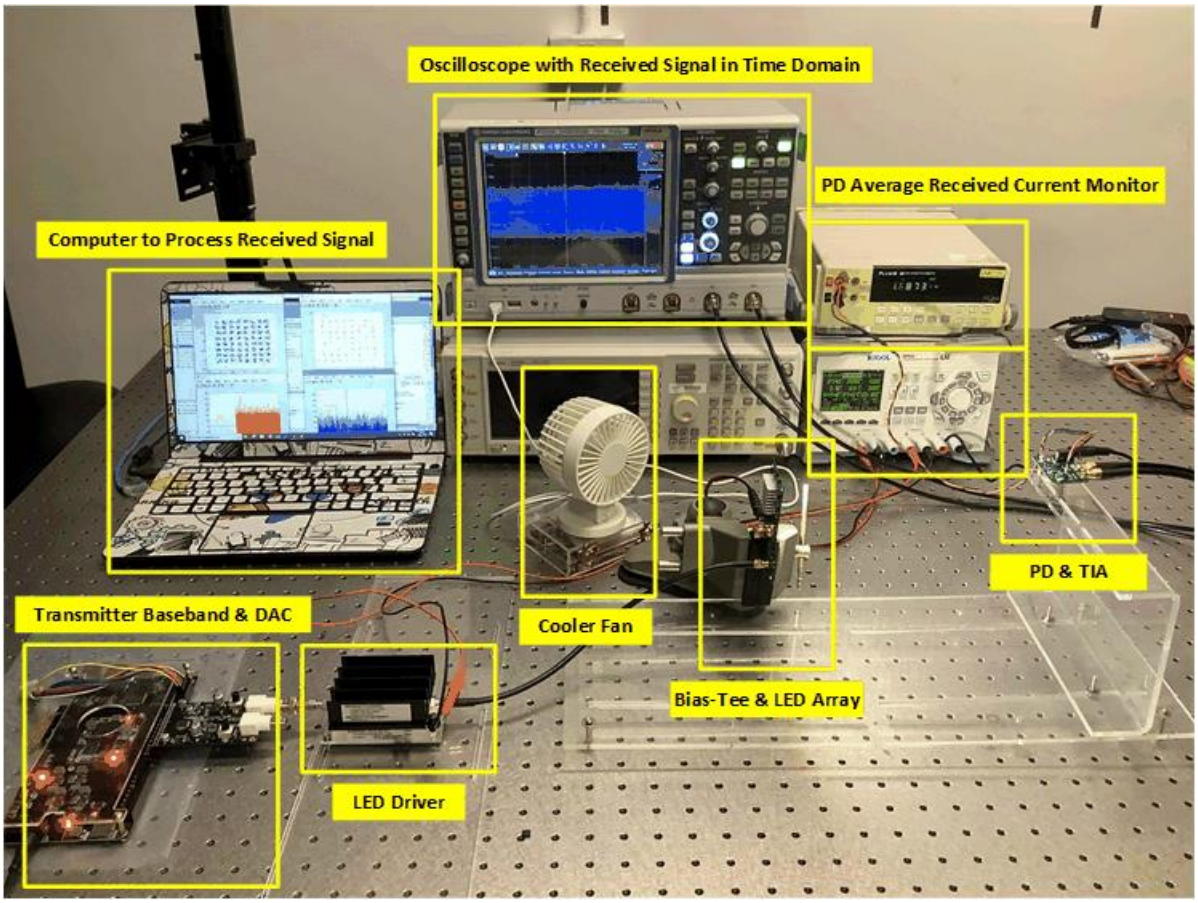

Fig. 40 Experiment setup of the DCO-OFDM VLC system

TABLE VI. SUMMARY OF THE SYSTEM CONFIGURATION

Device or Equipment	Model
FPGA Developing Board	ALINX AX7103
DAC Module	ALINX AN9767
LED Driver	ZHL-6A+
LED	Cree XLamp ML-C LEDs
LDO for TIA	Hamamatsu S10784
TIA	Texas Instruments LM317a
PD	Maxim MAX3658
Oscilloscope	Rohde & Schwarz RTO1044
Multimeter	Fluke 45
Power Supply	ROGIL DP832
Computer for Data Processing	ThinkPad S3 S330

4.3.4.3 The Measurement Result and Discussion

The measurement is done after the experiment setup is built. Firstly, the linearity and frequency response of the system frontend is measured to decide the DC bias voltage and the sample rate of the transmitter. Then, the communication performance of the system is evaluated. First, the frame detection and symbol synchronization are verified. Then, the same modulation scheme and energy scaling factor is employed on each subcarrier to measure the SNR under a specific channel. Finally, the bit and energy allocation algorithms are applied based on the measured SNR result. The allocation strategy is used on the transmitter side and the bit error rate is measured. The distance between the transmitter and the receiver is 30 cm and all nine LEDs are used.

Fig. 41 (a) shows the relationship between the DC voltage applied on the LED array and the current received by the PD. The center point of the linearity region is chosen as the value of the DC bias, which is 27 V in the proposed system.

Then, we use a different frequency sinusoidal signal as the input of the LED driver and measure the root mean square (RMS) of the received signal from the TIA of the receiver. The result is shown in Fig. 41 (b). The 3-dB bandwidth of the system is about 1.6 MHz. Therefore, the sampling rate is chosen as 20 MSa/s.

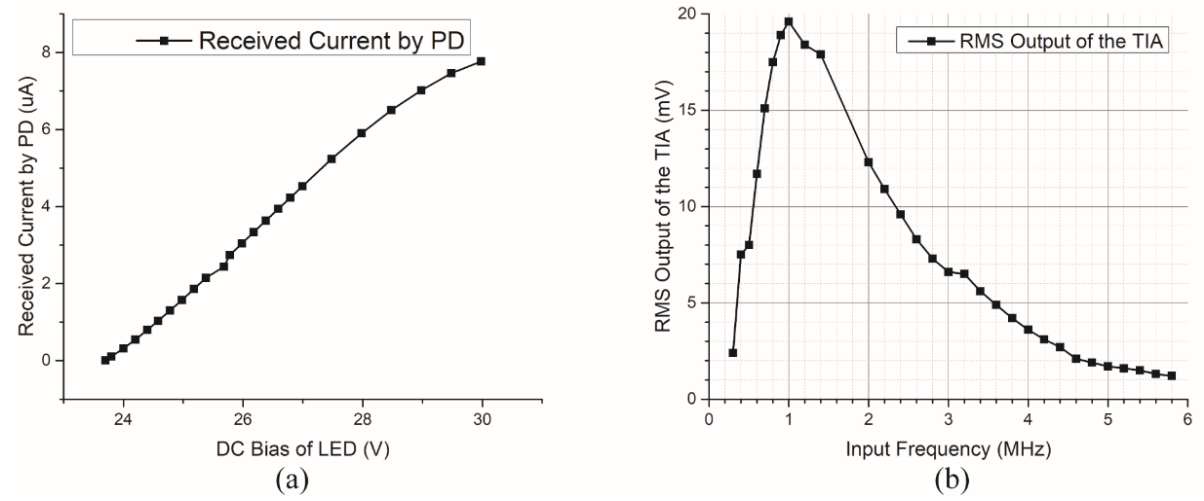

Fig. 41 (a) Linearity and (b) frequency response of the frontend.

After the voltage bias and sampling rate is identified. The performance of communication can be evaluated. Fig. 42 is the result of frame detection and symbol synchronization. There are two repeated OFDM frames of length 128, the symbol is synchronized after two peaks are detected. The effective data can be received and demodulated after the beginning of the sequence is found.

Before the data transmission employing DCO-OFDM with the BEA algorithm, QAM-4 modulation with the one-unit energy is employed on each subcarrier for SNR measurement. The SNR measurement result with signal constellation on some subcarriers is shown in Fig. 43. The quality of the constellation is relevant to the SNR of the corresponding subcarrier.

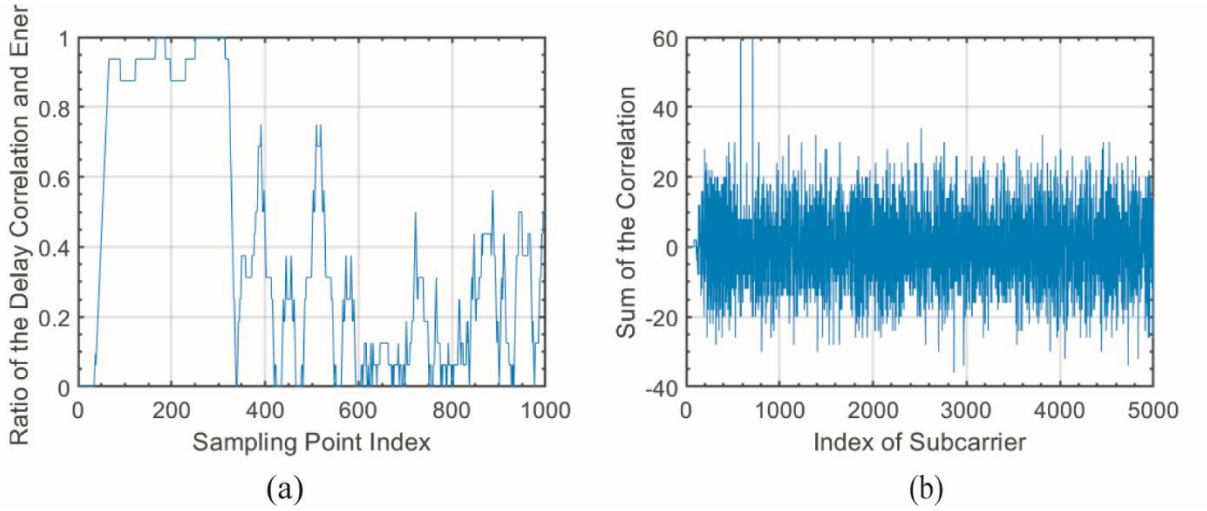

Fig. 42 (a) The ratio result for frame detection. (b) The detected peak for symbol synchronization.

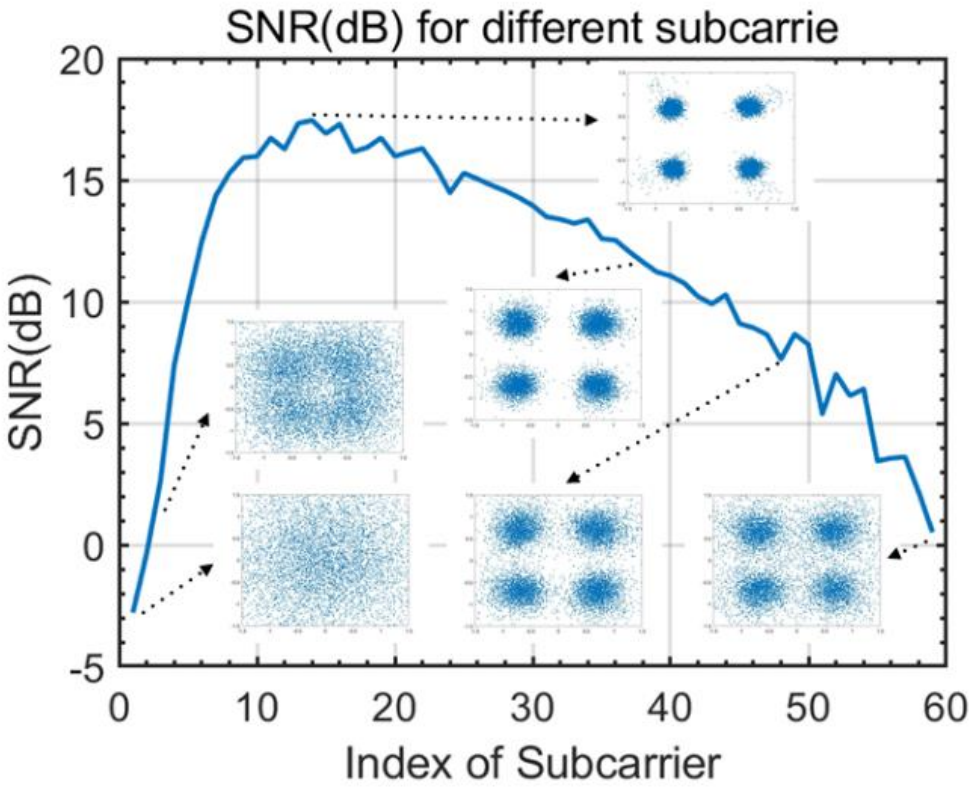

Fig. 43 Measured SNR for each subcarrier.

Finally, based on the measurement result of the SNR of each subcarrier, the BEA algorithm is running under a different data rate requirement. The bit and energy loading strategies are employed in the proposed transmitter and the bit error rate is measured. The

transmission with a fixed modulation scheme and equal energy on each subcarrier is also run for comparison. The result between the bit error rate and data rate is shown in Fig. 44. The allocation result is also shown when the data rate is about 22 Mbps.

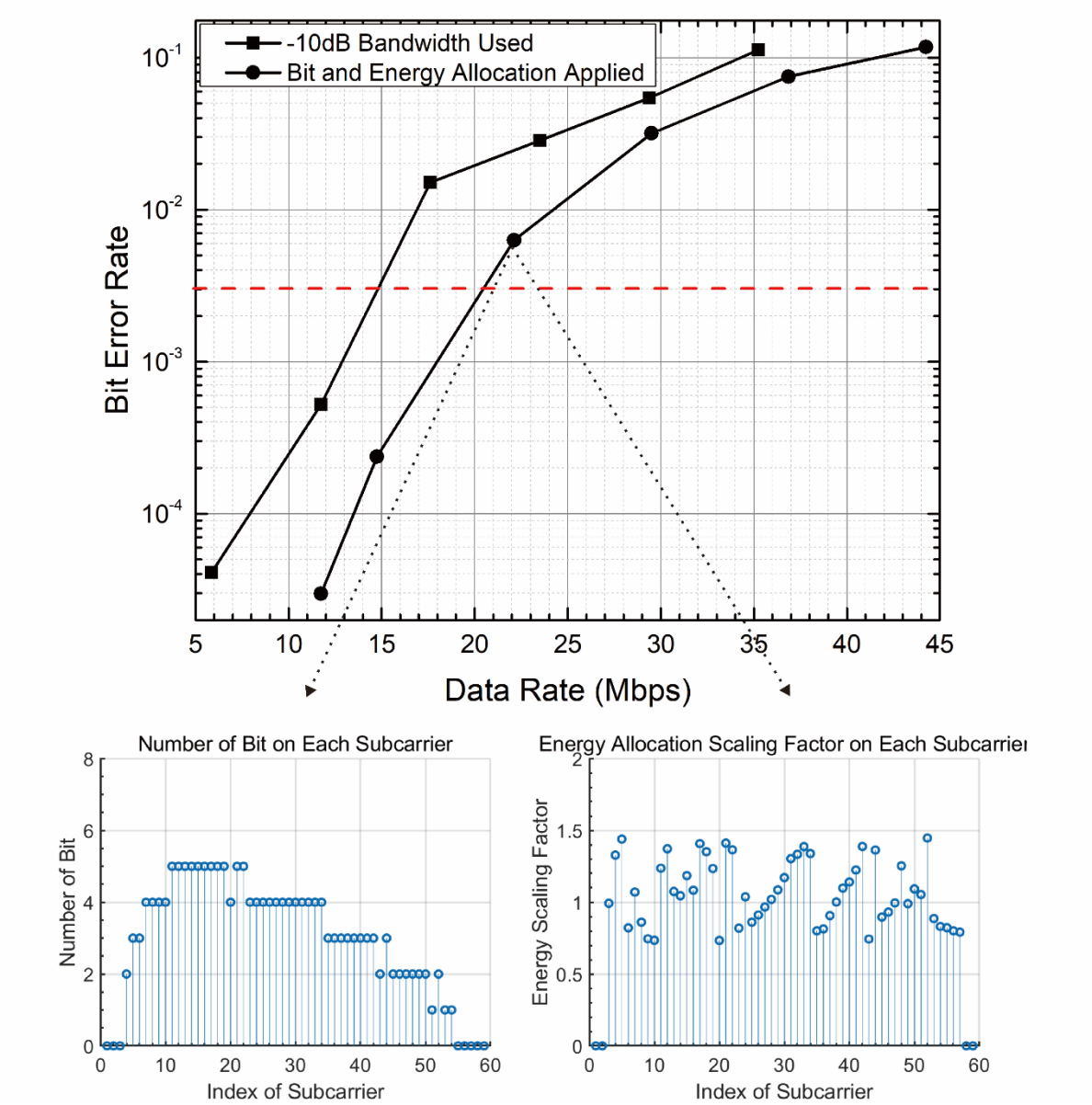

Fig. 44 Data rate and BER with and without the BEA algorithm

The BER upper limitation of the FEC is used as the standard, which is about 3×10^{-3}. The data rate is improved from 15 Mbps to 20.5 Mbps and the improvement rate is about 36.7%.

4.4 References

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CHAPTER 5. CONCLUSION AND FUTURE PLAN

5.1 Conclusion

The digital baseband employs OOK, PAM-4 and OFDM, which are designed and implemented on an FPGA for VLC system in this thesis. The 3-dB bandwidth of the analog frontend and data rate versus bit error rate are measured for system performance evaluation. The spectrum efficiency is all improved through the advanced modulation scheme and equalization technology.

The proposed OOK transceiver using laser as the light source is low complexity [1]. High resolution video transmission is supported in the system based on the designed transceiver. The data rate can be achieved to 500 Mbps over a 2-meter distance in real-time. This system can be used in the practical short distance wireless communication. But because the laser focus on the one point, VLLC cannot be used for illumination when the data is transferred. In the second and the third work, LEDs are used as the light source.

The proposed PAM-4 transmitter uses thermometer code to drive an RGB LED to generate a transmitted signal. FFE and CTLE are also supported in the baseband to extend the bandwidth of the whole system [2, 3]. The 3-dB bandwidth of the red, green and blue LED is about tens of Megahertz. The distance between the transmitter and receiver is about 5 centimeters when the measurement is done. Compared to NRZ data transmission, by applying the PAM-4 modulation scheme, the highest achievable data rate was increased from 22 Mbps to 32 Mbps, which was further extended 2.5 times to 80 Mbps using the FEE and CTLE functions.

The proposed OFDM transmitter supports a BEA algorithm to improve the spectrum efficiency. A phosphor-coated LED with low 3-dB bandwidth which is about 1.6 megahertz is used in the experiment system. The test result shows the transmitter can generate an OFDM signal supporting BAE and the signal can be synchronized and demodulated normally. When the distance between the LEDs array and the photodetector is 30 centimeters, with the help of bit and energy allocation algorithm, the data rate is improved from 15 Mbps to 20.5 Mbps when the BER equals to 3×10^{-3}. The improvement rate is about 36.7%.

The modulation schemes and equalization technologies used in the three proposed digital baseband design are different and they are used in different application scenarios with different light source. The simplest OOK modulation is used for laser diodes with high 3-dB bandwidth. PAM-4 with FFE and CTLE is employed to drive RGB LEDs for illumination and communication at the same time. DCO-OFDM with bit and energy allocation algorithm is used

for phosphor coated LEDs with very low 3-dB bandwidth LEDs to improve the data throughput as much as possible.

5.2 Future Plan

There are still some places can be improved in the proposed digital baseband designs and the corresponding VLC systems. First, the data rate of the second and the third work is tens of Mbps. It is not high enough compared with the newest WiFi standard which could reach to almost Gbps level. Second, the communication distance of the second and third system could only reach to 5cm and 30cm, separately. The distance between the roof and the users is at least 2 meters, it is necessary to increase the communication distance for our proposed system. Third, for the OOK VLLC design, both the transmitter and the receiver are implemented on an FPGA to do the real-time communication. However, for the PAM-4 and OFDM VLC design, only the transmitter is designed and implemented on an FPGA. On the receiver side, the signal is captured by the oscilloscope. The captured data is transmitted to the computer for synchronization and demodulation. Last but not the least, both the baseband developing board and the frontend structure is very big. It is not easy for the practical usage.

Now a period, some commercial LEDs are produced for visible light communication, which have higher 3-dB bandwidth. Wavelength division multiplexing [4] and multiple-input and multiple-output technology can also be used in the proposed system to increase the data throughput.

The communication distance depends on the output power of the optical signal. For the RGB PAM-4 and DCO-OFDM VLC system, the electrical power is about 0.5W and 0.6W separately. However, the electrical power of the LED bulb is about 10 to 15W. More LED beads could solve the distance problem. And lens can also be used in both the LEDs and PDs to focus light for longer communication distance.

In future, the digital baseband of the receiver needs to be implemented on an FPGA or ASIC so the transceiver can be used in the practical application. The platform for analog data sampling and transformation has already be constructed which is shown as Fig. 45. The received analog signal is captured and transformed to digital signal by ADC. The ADC capture module extract data from both the positive and negative edge of the input clock signal. Then the received data is buffered input a FIFO. The data in FIFO is stored in DDR3 SDRAM when the certain size data is received. The stored data is read by a FIFO to form UDP packages. The computer receives the UDP packages, and the data can be processed and observed in MATLAB.

In the next step, the digital baseband can be developed in this platform step by step and used with the transmitter for the real time communication.

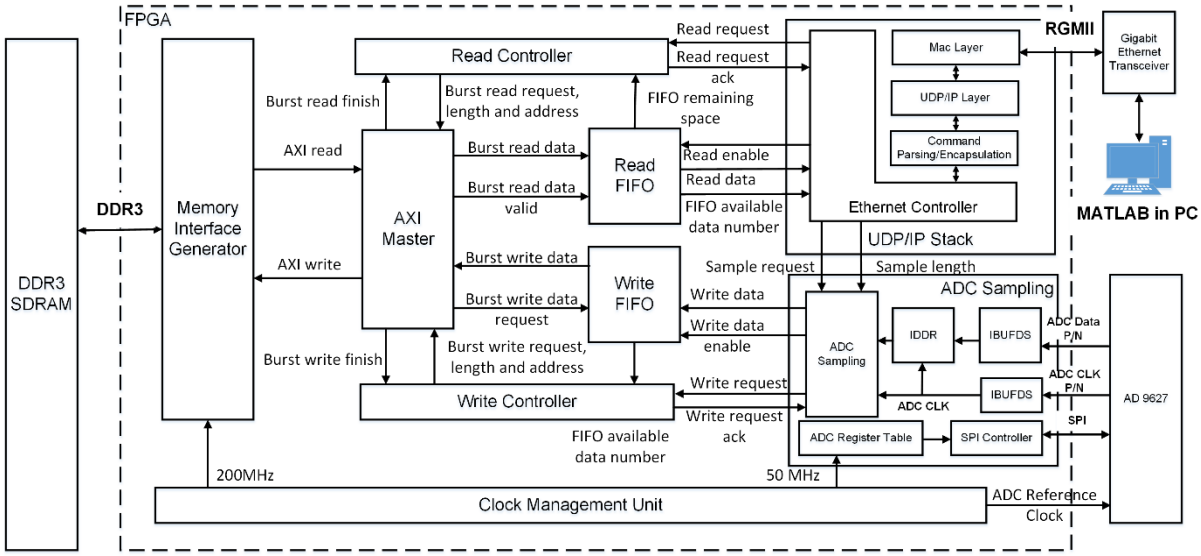

Fig. 45 System structure of real time receiver baseband design

For the last problem, both the baseband and the frontend driver can be integrated in a chip. System on chip (SOC) is the best solution for both power and size concern.

5.3 Reference

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