

Design and Implementation of Visible Light Communication Systems

by

Babar HUSSAIN

A Thesis Submitted to
the Hong Kong University of Science and Technology
in Partial Fulfillment of the Requirements for
the Degree of Master of Philosophy
in the Department of Electronic and Computer Engineering

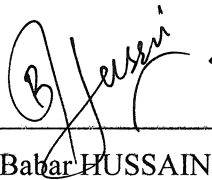
August 2015, Hong Kong

Authorization

I hereby declare that I am the sole author of the thesis.

I authorize the Hong Kong University of Science and Technology to lend this thesis to other institutions or individuals for the purpose of scholarly research.

I further authorize the Hong Kong University of Science and Technology to reproduce the thesis by photocopying or by other means, in total or in part, at the request of other institutions or individuals for the purpose of scholarly research.



Babar HUSSAIN

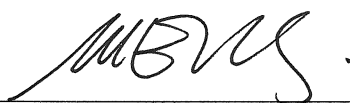
August 2015

Design and Implementation of Visible Light Communication Systems

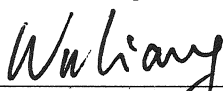
by

Babar HUSSAIN

This is to certify that I have examined the above MPhil thesis
and have found that it is complete and satisfactory in all respects,
and that any and all revisions required by
the thesis examination committee have been made.



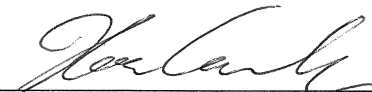
Prof. C. Patrick YUE, ECE Department
Thesis Supervisor



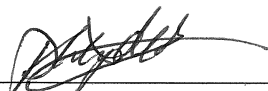
Prof. Liang WU, ECE Department
Thesis Co-Supervisor



Prof. Ross D. MURCH, ECE Department
Thesis Examination Committee Member (Chairman)



Prof. Howard Cam LUONG, ECE Department
Thesis Examination Committee Member



Prof. Philip Mok, ECE Department
Acting Head of Department

Department of Electronic and Computer Engineering
The Hong Kong University of Science and Technology
August 2015

To my mother

Acknowledgements

I would like to begin with thanking my supervisor, Prof. Patrick Yue, and my co-supervisor, Prof. Liang Wu, who took me under their wing as their MPhil student. Their consistent guidance and extreme kindness were key ingredients of my success. They also shared wonderful ideas with me and trusted my abilities in achieving my research targets. Under their supervision, I learned extremely valuable lessons and skills that will continue to help me in my future endeavors.

I am also very thankful to Prof. Ross Murch and Prof. Howard Luong for being my thesis committee members. They spent their precious time going through my research work and provided invaluable comments and suggestions to help me improve my thesis.

Gratitude goes to my friend and senior fellow Mr. Fengyu Che, with whom I spent one and a half quality years of my MPhil studies. I was very fortunate to have him working with me on the same project, for which he provided me with technical help and guidance on numerous occasions.

I would also like to extend my thanks and appreciation to Mr. Timothy Ho Man Lee, Mr. Eddie Tjon, Mr. Shengke Zou, Mr. Hugo Tian Zhang, and Mr. Derek Pengchong Wang for their respective contributions to the visible light indoor positioning project.

Further thanks go to Ms. Tania Wilmshurst for helping me proofread my thesis.

Additionally, I am thankful to my colleagues, both in and outside of my research group, for extending their technical support whenever needed and being wonderful friends. The list includes, but is not limited to, Dr. Quan Pan, Mr. Yipeng Wang, Mr. Zhengxiong Hou, Mr. Xianbo Li, Mr. Salahuddin Raju, Mr. Duona Luo, Miss Liwen Jing, Mr. Guang Zhu, Mr. Zhixin Li, Mr. Lin Cheng, Mr. Feng Zhang, and Mr. Wing Cheung Chong.

Thanks also go to my Pakistani friends, Mr. Danish Qureshi, Mr. M. Yasir Waqar, Mr. Salman Tariq, Mr. Abid Hussain, Mr. Naseer Kamal, Mr. Asad Iqbal etc., for the time and fun we had together and for the everlasting sweet memories of their friendship.

To my brother, Dr. Waseem Akhtar, I would like to express my thanks for his continued help and guidance in shaping my career.

Lastly, I am very thankful to my family members, especially my mother, for their unconditional love and support.

Table of Contents

Abstract.....	xii
CHAPTER 1 Introduction.....	1
1.1 Introduction to Visible Light Communication and its Applications	1
1.2 Recent Progress in VLC System Design and Analysis	2
1.3 Thesis Organization.....	3
References	5
CHAPTER 2 VLC System Design Considerations	6
2.1 Transmitter Design	6
2.1.1 LEDs Bandwidth	6
2.1.2 LED Illumination and Maximum Transmit Power.....	6
2.1.3 Modulation Schemes and LED Supply	7
2.2 Receiver Design	8
2.2.1 Communication Distance and Receiver Sensitivity	8
2.2.2 Required Gain and Bandwidth	8
References	10
CHAPTER 3 Optical Wireless Link Budget Analysis	11
3.1 Transmit Power	11
3.2 Path Loss	13
3.3 Received Power.....	13
3.4 Receiver Noise	14
3.5 Receiver Signal-to-Noise Ratio.....	15
References	17
CHAPTER 4 Design and Measurement of a Discrete VLC Transceiver System.....	18
4.1 System Specifications	18
4.1.1 Communication Distance	18

4.1.2	Modulation Scheme and BER Requirement.....	18
4.1.3	Data Rate	18
4.2	Transmitter Front-End Design and Analysis.....	20
4.3	Receiver Front-End Design and Analysis	23
4.3.1	Photodetector	23
4.3.2	The Amplifier Design	25
4.4	Digital Baseband Design and Implementation.....	27
4.4.1	Transmitter Baseband Design.....	27
4.4.2	Receiver Baseband Design	29
4.5	Hardware Measurements.....	30
References		33
CHAPTER 5 Design and Measurement of an IEEE 802.15.7 VLC System with CMOS		
Transmitter SoC		34
5.1	Introduction to IEEE 802.15.7 Standard	34
5.2	Target Specifications for Link Budget Verification.....	37
5.3	Design of a CMOS VLC Transmitter SoC.....	37
5.3.1	Reed Solomon (RS) Encoder.....	39
5.3.2	Interleaver	40
5.3.3	Convolutional Encoder	40
5.3.4	RLL Encoder and Modulator.....	41
5.4	IEEE 802.15.7 PHY-I Compliant Receiver Design	42
5.4.1	Demodulator	43
5.4.2	RLL Decoder	44
5.4.3	Viterbi Decoder	45
5.4.4	De-Interleaver	47
5.4.5	RS Decoder.....	48
5.4.6	Top Level MCS Controller.....	49

5.4.7	FPGA Implementation Summary	51
5.5	Hardware Measurements	51
	References	53
CHAPTER 6	Visible Light Indoor Positioning System	54
6.1	Introduction and Motivation for Indoor Positioning Using Visible Light	54
6.2	Visible Light Indoor Positioning Systems	55
6.2.1	Architecture	55
6.2.2	Smart LED Light Tubes as VLC Transmitters	56
6.2.3	Photodetector Board as VLC Receiver	58
6.2.4	Smartphone Camera as VLC Receiver	59
	References	61
CHAPTER 7	Conclusion	62
APPENDIX A	Using LightSay Smartphone Application to Decode VLC Signals	63

List of Figures

Figure 1.1 Smart LEDs as VLC Access Points.	1
Figure 1.2 A Typical VLC Transceiver System.	2
Figure 3.1 A Generic VLC Transciever System.....	11
Figure 3.2 Luminous Efficiency Function of the Human Eye.	13
Figure 3.3 Schematic of a Typical VLC Receiver Front-end.....	14
Figure 4.1 Setup for Measuring Bandwidth of White LEDs.....	19
Figure 4.2 Measured Frequency Response of Commercial White LEDs.....	19
Figure 4.3 VLC Transmitter Composed of a Baseband and 20 LEDs.	20
Figure 4.4 Measured I-V Curve of Five White LEDs.	21
Figure 4.5 Forward Current vs Luminous Intensity of White LED.	21
Figure 4.6 Setup for Measuring the Spectral Power Distribution of White LED.	22
Figure 4.7 Spectral Power Distribution of White LED.	22
Figure 4.8 Responsivity of the Photodiode.	23
Figure 4.9 Measuring the Effective Area of the PD.	24
Figure 4.10 Received Photocurrent Distribution over Different Wavelengths.	24
Figure 4.11 Simulation Circuit of Receiver Front-end.....	25
Figure 4.12 Gain-Bandwidth Response of the Transimpedance Amplifier.	26
Figure 4.13 PCB of the Receiver Front-end.	26
Figure 4.14 Data Packet Format.	27
Figure 4.15 Transmitter Baseband Architecture.....	28
Figure 4.16 Receiver Baseband Architecture.	28
Figure 4.17 Clock Data Recovery Illustration.....	29
Figure 4.18 (a) VLC Signal Swing, Measured vs Calculated.	31
Figure 4.19 Measurement Setup for Discrete VLC Transceiver System.	32
Figure 5.1 Network Topologies in IEEE 802.15.7 Standard.....	34
Figure 5.2 Modulation Domain Spectrum of IEEE 802.15.7 PHY.....	35
Figure 5.3 PHY-I Data Packet Format.	36
Figure 5.4 Architectural Block Diagram of VLC Transmitter SoC.	37
Figure 5.5 Block Diagram of IEEE 802.15.7 PHY-I Transmitter Baseband.	38
Figure 5.6 Block Diagram of RS Encoder.....	40
Figure 5.7 Rate 1/3 Convolutional Encoder.	40
Figure 5.8 RLL Encoding Operation.	41

Figure 5.9 PHY-I Modulation Schemes.	42
Figure 5.10 Frequency Response of Receiver Front-end.	42
Figure 5.11 Block Diagram of IEEE 802.15.7 PHY-I Receiver Baseband.....	43
Figure 5.12 Simulation of RLL 4B6B Decoder.	45
Figure 5.13 The Block Diagram of Viterbi Decoder.....	46
Figure 5.14 Illustration of Interleaving and De-interleaving.....	47
Figure 5.15 Block Diagram of RS Decoder.	48
Figure 5.16 Simulation of RS(15,2) Decoder.....	48
Figure 5.17 State Transition Diagram of Top Level MCS Controller Part-1.....	49
Figure 5.18 State Transition Diagram of Top Level MCS Controller Part-2.....	50
Figure 5.19 Hardware Measurement Setup for IEEE 802.15.7 Compliant Transceiver. ...	51
Figure 5.20 Measurement Results of the IEEE 802.15.7 VLC System.....	52
Figure 6.1 Block Diagram of the Architecture of the VLIP System.	55
Figure 6.2 Smart LED Light Tube with Driver, MCU and Wi-Fi Unit.	56
Figure 6.3 Block Diagram of the Smart LED Light Tube Controller.	56
Figure 6.4 Schematic of Photodetector based VLC Receiver.	57
Figure 6.5 Frequency Response of the Photodetector-based VLC Receiver.	57
Figure 6.6 Photodetector Board Connected to the Smartphone.	58
Figure 6.7 Rolling Shutter Effect of Smartphone Camera.	59
Figure 6.8 Illustration of VLC Decoding Algorithm Using Smartphone Camera.	60

List of Tables

Table 2.1 Recommended Light Levels for Indoor Conditions.	7
Table 4.1 Target Specifications for a Discrete VLC System.	20
Table 4.2 FPGA Resource Utilization Summary.	30
Table 5.1 PHY Data Rates and Potential Applications.	34
Table 5.2 Summary of PHY-I Modulation, Coding Schemes and Data Rates.....	36
Table 5.3 Target Specifications for IEEE 802.15.7 VLC Link.	37
Table 5.4 PHY-I RS Encoders and their Generator Polynomials.....	39
Table 5.5 Manchester Decoding and Erasure Signaling.....	44
Table 5.6 4B6B Decoding Table.	44
Table 5.7 Design Parameters for Xilinx Viterbi IP Core.	46
Table 5.8 FPGA Resource Utilization Summary.	51

Design and Implementation of Visible Light Communication Systems

by

Babar HUSSAIN

Department of Electronic and Computer Engineering

The Hong Kong University of Science and Technology

Abstract

Using LED lights for visible light communication (VLC) has received a great deal of interest because of a wide range of new applications such as location-based wireless broadcasting through LED lightings, signs with LED backlights and digital LED displays, as well as indoor positioning and navigation utilizing LED lights as location beacons. Recently, a number of VLC systems have been reported with focus ranging from functionality demonstration to using various modulation schemes for data rate improvement. However, systematic analysis and design methodologies for implementing a VLC system fulfilling certain specifications have been largely overlooked.

This work presents, for the first time, a systematic approach to VLC transceiver design based on an analytical study of system design considerations and optical wireless link budget analysis. To obtain the signal-to-noise ratio (SNR) at the receiver, the received signal power is predicted by modeling the transmitted optical power and the channel path loss while the input-referred noise is estimated by characterizing the noise contribution from each of the receiver building blocks. To validate the proposed approach, a VLC transceiver using discrete components has been designed, achieving a data rate of 2.5 Mb/s and a communication distance of ~ 2 m. Furthermore, another VLC system using a fully integrated CMOS transmitter SoC compliant with IEEE 802.15.7 standard is implemented. The SoC integrating a DC-DC power converter, a VLC modulator and a baseband unit measures a record energy efficiency of ~ 5 nJ/bit.

CHAPTER 1 INTRODUCTION

1.1 Introduction to Visible Light Communication and its Applications

Rising concerns over energy conservation for a sustainable environment have been driving the research and development of energy-saving green technologies. As an energy-efficient, cost-effective and reliable illumination technology, solid-state lighting using LEDs is being deployed more and more ubiquitously to replace conventional fluorescent and incandescent lights. Due to their inherent fast response, LEDs can also be switched on and off rapidly to modulate the lights for information transmission. As the modulation frequency is far beyond the flicker fusion threshold of human beings, LEDs can be utilized as light sources and visible light communication (VLC) access points simultaneously for the next-generation green infrastructure, as shown in Figure 1.1. Compared with traditional RF wireless communication, VLC is advantageous in terms of huge bandwidth in the THz range, license-free operation, no electromagnetic interference and high security due to line-of-sight (LOS) signal propagation. Thus, VLC can be used in places where RF communication is prohibited, for instance hospitals and airplanes etc. However, VLC suffers from the critical drawback that the data rate falls sharply as the distance increases, which in turn limits the communication range [1.1]. As such, VLC is being regarded as a promising technology supplementing conventional RF wireless, especially for near-field high-data-rate communications and location-based information delivery applications. Considering the ubiquity of LEDs, VLC is expected to play an important role in the Internet-of-Things (IoT).

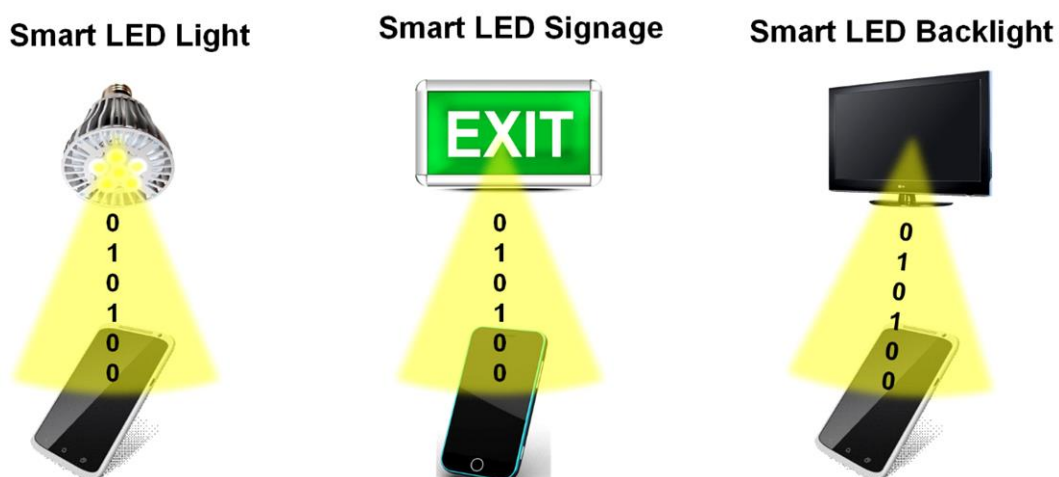


Figure 1.1 Smart LEDs as VLC Access Points.

A complete VLC system composed of a transmitter and a receiver is shown in Figure 1.2. The transmitter turns a light source on and off at such high speeds that the switching cannot

be observed by the human eye. Similar to on-off keying (OOK) modulation in conventional wireless communications, the ON and OFF states of the light source correspond to the two binary values: 0 and 1. Digital coding and modulation schemes are typically employed to achieve a certain data rate within a specified distance under various channel conditions. On the other hand, a VLC receiver detects the modulated light, converts it to electrical signal and then decodes the data. The transmitter typically includes a digital baseband, an analog front-end, an LED modulator, an LED driver and several LEDs, whereas, the receiver consists of a photodiode, transimpedance amplifier, filter and digital baseband.

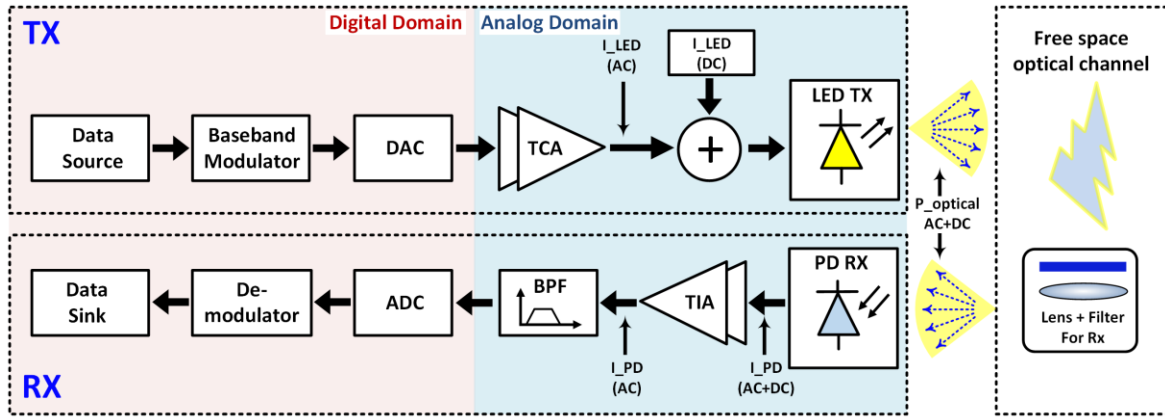


Figure 1.2 A Typical VLC Transceiver System.

1.2 Recent Progress in VLC System Design and Analysis

In recent years, there has been increasing research interest in VLC and some transceiver systems have been demonstrated. Depending on the modulation schemes used, the achievable data rate and the distance are different. In [1.2], an on-off-keying (OOK) non-return-to-zero (NRZ) modulation was employed in the VLC transmitter using a post-equalized LED, achieving a data rate of 40 Mb/s at a distance of 10 cm without an optical lens. In [1.3], rate-adaptive discrete multi-tone (DMT) modulation was proposed to obtain a data rate up to 1 Gb/s, but the distance was still limited to 15cm even with a lens to strengthen the received light signal. In these works, the main focus was either on the functional demonstration or some specific techniques to improve the data rate. However, they didn't consider a systematic approach to design and optimize the transceiver parameters according to the specifications defined by a certain practical VLC application. Thus, the power consumption of these systems is prohibitively high and the estimated energy efficiency is about 20-100 nJ/bit, which is about 100 times lower than the state-of-the-art Wi-Fi efficiency of 0.2-1 nJ/bit.

For communication system design, link budget analysis is the first critical starting point, from which the SNR margin for a receiver is derived from the maximum allowable

transmitted power, the communication distance and the receiver input sensitivity. In RF system design, link budget estimations have been studied extensively, ranging from several hundreds of MHz, such as in radio frequency identification (RFID) [1.4], [1.5] up to several THz [1.6]. Unfortunately, for VLC, there are only a few works reported that are related to the link budget analysis. In [1.7] a free-space short-range optical link was analyzed, but the system was based on a laser which features excellent directivity and is quite different from visible light. In [1.8], a VLC LOS channel model was presented, but the system was not analyzed from a link budget point of view, so some critical parameters, including the required SNR and the receiver sensitivity, were not derived. The SNR distribution inside a room was calculated in [1.9], but no hardware measurement was performed to verify the calculation. In a word, there is no link budget analysis that can be directly used to design a VLC system. However, link budget analysis is of paramount importance to design a robust VLC system fulfilling the performance specification. In the presence of various operating environments, e.g., indoors and outdoors, where the transmitted power levels as well as the path losses are different, link budget analysis would be even more essential.

In this work, an analytical optical wireless link budget study and hence a systematic approach to VLC transceiver design are presented. First, the transmitted optical power from LEDs is characterized, followed by the path loss calculation. Later, from an extensive analysis of the noise contribution by each of the building blocks in a generic receiver, its input-referred noise is derived. With the receiver SNR calculated at different distances, the corresponding BER is estimated based on the coding and modulation schemes used. After the analysis, a detailed design for two VLC systems is presented to verify the validity of the systematic design approach and the accuracy of the optical wireless link budget analysis.

1.3 Thesis Organization

The rest of the thesis is organized as follows. In chapter 2, design considerations for VLC systems are presented. The significance and trade-offs between various design parameters and choices, including LED bandwidth, transmit power, communication distance, and modulation schemes etc., are discussed. Chapter 3 describes a detailed link budget analysis for optical wireless systems by calculating the optical transmit power, path loss and receiver sensitivity etc. Chapter 4 presents the design of a discrete VLC transceiver whose performance is verified using the link budget analysis. Chapter 5 describes the design of an IEEE 802.15.7 standard transceiver system with a CMOS fully integrated transmitter SoC and presents the measurement results to both verify the link budget calculations and validate the usefulness of

system integration. Chapter 6 presents a visible light indoor positioning (VLIP) system design that includes a detailed hardware design and software interface. Finally, the thesis is concluded in Chapter 7.

References

- [1.1] A. Jovicic, J. Li, and T. Richardson, “Visible light communication: Opportunities, challenges and the path to market,” *IEEE Communication Magazine.*, vol. 51, no. 12, pp. 26–32, Dec. 2013.
- [1.2] H. L. Minh, D. O’Brien, et al., “100-Mb/s NRZ visible light communications using a postequalized white LED,” *IEEE Photonics Technology Letters*, vol. 21, no. 17, , pp. 1063–1065, Aug. 2009.
- [1.3] A. M. Khalid, G. Cossu, et al., “1-Gb/s transmission over a phosphorescent white LED by using rate-adaptive discrete multitone modulation,” *IEEE Photonics Journal*, vol. 4, no. 5, pp. 1465–1473, Oct. 2012.
- [1.4] J. D. Griffin, G. D. Durgin, A. Haldi, and B. Kippelen, “RFID tag antenna performance on various materials using radio link budgets,” *IEEE Antennas Wireless Propagation Letter*, vol. 5, no. 5, pp. 247–250, May 2006.
- [1.5] Joshua D. Griffin and Gregory D. Durgin, “Complete link budgets for backscatter-radio and RFID systems”, *IEEE Antennas and Propagation Magazine*, vol. 51, no. 2, pp. 11–25, Apr. 2009.
- [1.6] T. Schnider, A. Wiatrek, S. PreuBler, M. Grigat, and R-P Braun, “Link budget analysis for terahertz fixed wireless links,” *IEEE Trans. on Terahertz Science and Technology*, vol. 2, no. 2, pp. 250–256, Mar. 2012.
- [1.7] J. Poliak, P. Pezzei, E. Leitgeb, and O. Wilfert, “Link budget for high-speed short-distance wireless optical link,” in *2012 8th International Symposium on Communication Systems, Networks & Digital Signal Processing (CSNDSP)*, Jul. 2012, pp. 1–6.
- [1.8] K. Cui, G. Chen, Z. Xu and R. D. Roberts, “Line-of-sight visible light communication system design and demonstration,” in *IEEE Globecom Workshop on Optical Wireless Communications*, Jul. 2010, pp. 621–625.
- [1.9] Penghua Lou, et al., “Fundamental analysis for indoor visible light positioning system,” in *2012 1st IEEE International Conference on Communications in China Workshops*, Aug. 2012, pp. 59-63.

CHAPTER 2 VLC SYSTEM DESIGN CONSIDERATIONS

2.1 Transmitter Design

2.1.1 LEDs Bandwidth

Unlike in an RF design, in which the transmit antenna can be optimized to achieve a specified bandwidth, the LEDs acting as the “antenna” in a VLC system exhibit a limited bandwidth. Most commercial white LEDs are designed using a blue LED coated with a yellow phosphor layer to generate a white-light. However, the phosphor layer has a slow temporal response and thus limits the modulation bandwidth of the LED to within a few MHz [2.1]. These commercial white LEDs can be used to design low-data rate systems that have applications in indoor location based information delivery and indoor positioning.

Higher data-rate systems are implemented by extending the bandwidth of the LED. There are a few methods that can be employed for bandwidth extension, with each solution having certain drawbacks. One possible solution is using pre-equalization, which emphasizes the high-frequency components of the LED bandwidth spectrum to overcome the larger attenuation at high frequency [2.2]. However, this adds to the complexity of the overall system implementation. Bandwidth extension is also possible by employing a blue filter at the front of the receiver to attenuate the slow responding yellow components of the light [2.3]. Blue filtering, however, reduces the signal strength at the receiver and thus leads to a reduction in SNR, as will be demonstrated in the following chapters. Another possible option is to use more advanced LEDs featuring a much larger bandwidth [2.4] to simplify the modulation, but it’s at the expense of a higher system cost.

2.1.2 LED Illumination and Maximum Transmit Power

In contrast to RF transmit power, where the gain of the antenna and power amplifier can be controlled to achieve a certain transmit power, VLC transmission power is application dependent. In other words, to be compliant with the illumination while performing VLC, the maximum transmit power from the LEDs is set by the lighting standard in certain scenarios. Table 2.1 lists the recommended lighting levels for various conditions and activities. These levels are represented by the illuminance, which is measured in lumens per square meter, i.e. lux. Illuminance is a quantitative measure of what is commonly referred to as brightness.

Table 2.1 Recommended Light Levels for Indoor Conditions [2.8].

Conditions and Activity	Illuminance (lux, lumen/m ²)
Warehouse, Theaters, Archives	150
Office Work, Reading, Study	500
Supermarkets, Office Landscapes	750
Detailed Drawing Works	1500-2000

2.1.3 Modulation Schemes and LED Supply

The type of modulation scheme chosen is dependent on the required data rate. For low data rate applications, OOK is considered very efficient as it requires a simple hardware construction. With bandwidth extension methods applied, the data rates achieved with OOK modulation are in the order of 40Mb/s [2.2-2.3]. On the other hand, more complex modulation schemes are employed for designing high data rate VLC systems. For instance, it has been shown that discrete multi-tone modulation (DMT), which is quite similar to orthogonal frequency division multiplexing OFDM in RF, can be implemented to achieve data rates in excess of 500 Mb/s [2.5]. In addition, the use of carrier-less amplitude and phase modulation (CAP) can lead to data rates in the order of Gb/s [2.6]. However, these complex modulation require complicated and costly hardware implementations that include, for instance, powerful signal processors and high performance ADCs.

For the transmitter front-end, the supply should be designed to output sufficient power to drive the LEDs. To concurrently support both illumination and VLC, it is necessary to superimpose the modulation signal onto the supply. The superimposition can be simply implemented by using a bias-T, whose DC input port and AC input power are fed by the supply and the VLC signal, respectively [2.7]. Another solution is to completely switch on and off the LEDs according to the digital signal while maintaining the same duty cycle for a constant DC level.

2.2 Receiver Design

2.2.1 Communication Distance and Receiver Sensitivity

For indoor VLC systems, the required communication distance is about two meters, which represents the distance of the lighting from the top of a table in a typical office environment. On the other hand, for outdoor VLC systems, for instance, in vehicle-to-vehicle or smart traffic lights, the required communication distance is comparatively large.

Considering that the illuminance of light decreases as it travels farther from the source, the strength of the VLC signal arriving at the receiver is dependent on the communication distance. Since the maximum transmit power from VLC transmitters is usually fixed, the maximum achievable communication distance is dependent on the sensitivity of the receiver, which is represented as the signal-to-noise ratio (SNR) required to achieve a certain BER performance.

For a specified communication distance, the received signal strength can be estimated by incorporating the transmit power and signal attenuation due to path loss. On the other hand, based on the modulation and the data rate and BER requirement, the minimum required SNR can be derived from communication theory. As an example, for a simple OOK-NRZ system, the BER as a function of SNR can be expressed as [2.9]

$$BER_{OOK} = \frac{1}{2} \operatorname{erfc} \left(\frac{1}{2\sqrt{2}} \sqrt{SNR} \right) \quad (2.1)$$

where $\operatorname{erfc}(\cdot)$ is the complementary error function widely used in communications. With both the received signal strength and the SNR available, the noise requirement can be specified for the receiver.

2.2.2 Required Gain and Bandwidth

As a following step, from the input voltage swing needed by the baseband circuitry and the received power level, the required gain for the receiver can be derived. As the distance between the transmitter and the receiver varies for certain applications, variable gain may be needed to avoid signal distortion, especially for high-order modulations. For a simple modulation like OOK-NRZ, which is popular in VLC, variable gain is generally not necessary.

One more step is to determine the bandwidth of the VLC receiver based on the analog bandwidth required and the modulation used, which is similar to RF receiver design. Finally, with the receiver specifications in terms of gain, noise and bandwidth all available, the building blocks can be designed and implemented based on the analysis presented in the following chapters.

References

- [2.1] A. M. Khalid, G. Cossu, et al., “1-Gb/s transmission over a phosphorescent white LED by Using rate-adaptive discrete multitone modulation,” IEEE Photonics Journal, vol. 4, no. 5, pp. 1465–1473, Oct. 2012.
- [2.2] H. Le-Minh, D. C. O’Brien, G. Faulkner, et al., “High-speed visible light communications using multiple-resonant equalization,” IEEE Photonics Technology Letters, vol. 20, pp. 1243–1245, Jul. 2008.
- [2.3] J. Grubor, S. C. J. Lee, K.-D. Langer, et al., “Wireless high-speed data transmission with phosphorescent white light LEDs,” in European Conference on Optical Communication, Sept. 2007, pp.1-2.
- [2.4] D. Tsonev, H. Chun, et al., “A 3-Gb/s single-LED OFDM-based wireless VLC link using a Gallium Nitride μ LED,” IEEE Photonics Technology Letters, vol. 26, no. 7, pp. 637–640, Jan. 2014.
- [2.5] J. Vučić, C. Kottke, S. Nerreter, et al., “513 Mbit/s visible light communications link based on DMT-modulation of a white LED,” IEEE/OSA Journal of Lightwave Technology, vol. 28, pp. 3512– 3518, Dec. 2010.
- [2.6] F.-M. Wu, C.-T. Lin, C.-C. Wei, et al., “1.1-Gb/s White-LED-based visible light communication employing carrier-less amplitude and phase modulation,” IEEE Photonics Technology Letters, vol. 24, pp. 1730–1732, Oct. 2012.
- [2.7] H. L. Minh, D. O’Brien, et al., “100-Mb/s NRZ visible light communications using a postequalized white LED,” IEEE Photonics Technology Letters, vol. 21, no. 17, , pp. 1063–1065, Aug. 2009.
- [2.8] *Illuminance - Recommended Light Levels* [Online], Available: http://www.engineeringtoolbox.com/light-level-rooms-d_708.html
- [2.9] S. Trisno, “Design and analysis of advanced free space optical communication systems,” Ph.D. dissertation, University of Maryland, Maryland, US, 2006.

CHAPTER 3 OPTICAL WIRELESS LINK BUDGET ANALYSIS

Link budget analysis is the first critical starting point for communication system design. The analysis helps predict the performance and evaluate the viability of a communication system in a targeted scenario prior to its implementation. The analysis relies on calculating the SNR margin for a receiver from the maximum allowable transmitted power, communication distance and receiver input sensitivity.

A generic VLC transceiver system is illustrated in Figure 3.1. The transmitter consists of a digital baseband for data encoding and signal modulation, and an analog front-end to drive the LEDs. At the receiver side, there is a photodetector (PD) to convert the visible light signal to electrical current, which is then converted to voltage and amplified by a transimpedance amplifier (TIA). A high-pass filter (HPF) is used to remove the low-frequency components of the signal. After that, the signal is demodulated and the data is decoded in a digital baseband.

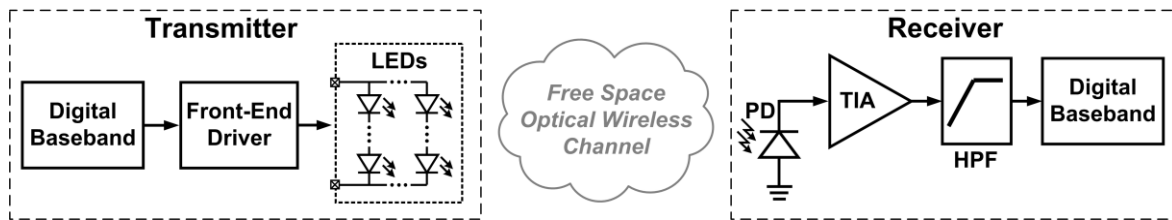


Figure 3.1 A Generic VLC Transceiver System.

Compared to the general RF wireless architecture, the VLC transceiver in Figure 3.1 looks very similar, except that the transmit and the receive antennas are replaced by an LED light source and a PD, respectively. Therefore, a similar procedure to that for RF design can be followed to perform optical wireless link budget analysis for VLC. In the analysis, the transmitted optical power from LEDs, path loss, received power, receiver input-referred noise, and receiver SNR will be derived step by step.

3.1 Transmit Power

Since an individual LED is not able to generate sufficient luminous intensity for either illumination or VLC, multiple LEDs are used as an array, in which they are connected in parallel. Their total transmit power can be calculated by linearly combining the power from each individual LED.

Commercial LEDs are generally targeted at the illumination and display markets. Therefore, the specifications and performance parameters reported in their datasheets are typically photometric quantities; i.e., their response is measured with respect to the sensitivity of the human eye. In order to calculate their radiometric power, i.e. the measure of optical radiation, a few conversions are required between the photometric and radiometric quantities. An ordinary white LED's power can be calculated by integrating the spectral response $S_t(\lambda)$ over the wavelength of the visible light λ , as shown in Eq. (3.1) [3.1]:

$$P_t = \int_{\lambda_L}^{\lambda_H} S_t(\lambda) d\lambda, \quad (3.1)$$

where λ_L and λ_H are the minimum and the maximum wavelengths of the visible light spectrum, respectively.

Usually, the absolute spectral response $S_t(\lambda)$ is not directly available but it can be calculated from the normalized spectral distribution $S_t'(\lambda)$ as

$$S_t(\lambda) = c S_t'(\lambda), \quad (3.2)$$

where $S_t'(\lambda)$ is available in the LED datasheet and c is a scaling factor to be derived in the following analysis.

In an LED datasheet, another important parameter is luminous flux Φ_V , which is defined as the photometric measure of the light power perceived by the human eye. Φ_V is a function of $S_t(\lambda)$ expressed as

$$\Phi_V = 683 \int_{380nm}^{780nm} S_t(\lambda) V(\lambda) d\lambda, \quad (3.3)$$

where 380 to 780 nm is the wavelength range of visible light, and $V(\lambda)$ is a spectral luminous efficiency function, which is the measure of the human eye's response to various wavelengths of light.

From Eqs. (3.2) and (3.3), the scaling factor can be derived as [3.1]

$$c = \frac{\Phi_V}{683 \int_{380nm}^{780nm} S_t'(\lambda) V(\lambda) d\lambda}. \quad (3.4)$$

Approximated by a Gaussian curve, $V(\lambda)$ can be expressed as [3.2]

$$V(\lambda) \cong 1.019 e^{-285.4(\lambda-0.559)^2}. \quad (3.5)$$

The normalized spectral response of the luminous efficiency function is represented in Figure 3.2. The response reveals that the human eye has different sensitivities to detect various wavelengths of light. The peak of the curve can be observed at a wavelength of 555nm, which implies that the human eye is most sensitive to green.

Finally, by substituting Eq. (3.5) to Eq. (3.4) to calculate c and then $S_t(\lambda)$, the transmit power can be derived.

3.2 Path Loss

The path loss model for the visible light is described as [3.3]

$$PL \approx \frac{(m+1)A_r}{2\pi d^2} \cos^m(\alpha) \cos(\beta), \quad (3.6)$$

where A_r is the effective area of the PD, d is the communication distance, m is the order of the Lambertian source and α and β are the transmit and receive angles, respectively. The order of the Lambertian source m is the measure of the shape of an illumination pattern and can be derived from the half-power angle $\theta_{1/2}$, which is available in the LED datasheet as [3.3]

$$\theta_{1/2} = \cos^{-1}(0.5^{1/m}). \quad (3.7)$$

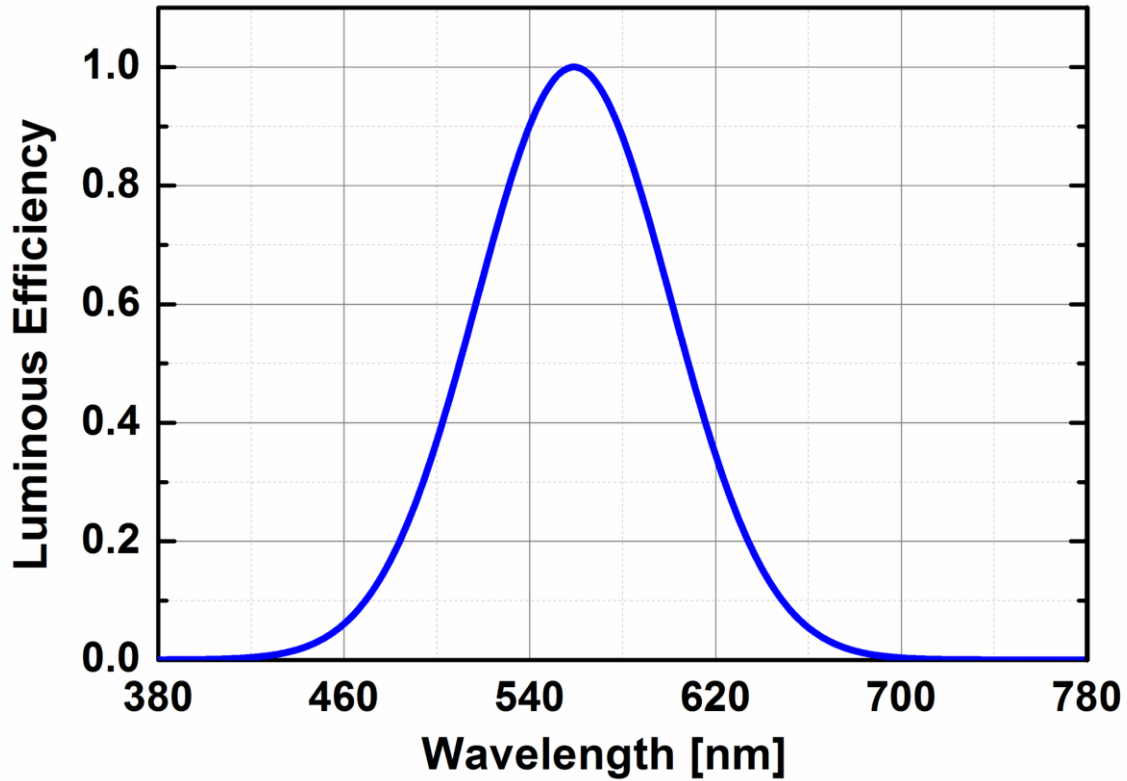


Figure 3.2 Luminous Efficiency Function of the Human Eye.

3.3 Received Power

Apparently, the received optical power can be derived by multiplying the transmit power P_t by the path loss PL in a linear scale. As mentioned above, the optical signal is converted to an electrical current by a PD. The root-mean-square (RMS) value of the output current from the PD is expressed as

$$I_{PD} = \frac{1}{2} IL \cdot \int_{\lambda_L}^{\lambda_H} S_t(\lambda) R_{PD}(\lambda) d\lambda , \quad (3.8)$$

where the integration accounts for the spectral power distribution of the LED lights and $R_{PD}(\lambda)$ is the responsivity of the PD, which can be found in its datasheet.

3.4 Receiver Noise

The schematic of a receiver front-end is shown in Figure 3.3. The TIA is implemented by an amplifier with resistive feedback. The HPF is simply constructed by an RC network. Since the low-frequency components are removed by the HPF, the DC level of the output V_{RX} is set by V_{CC} and the resistive divider. As described above, the received signal strength is expressed in the form of photocurrent at the PD output. Correspondingly, the noise power should be characterized by referring it to the TIA input. There are mainly four noise sources, namely the PD, TIA, HPF and power supply. Their noise currents are represented by I_{n-PD} , I_{n-TIA} , I_{n-HPF} and I_{n-VCC} , respectively. In the following analysis, each of them will be derived and finally they will be summed together and referred to the TIA input.

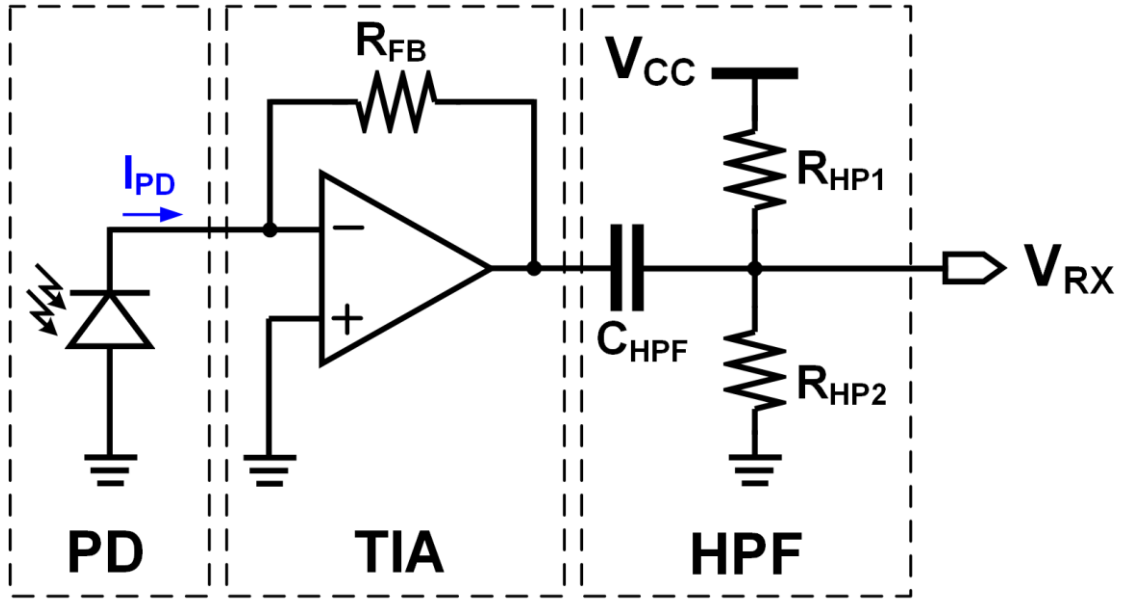


Figure 3.3 Schematic of a Typical VLC Receiver Front-end.

There are two types of noise in the PD, shot noise and thermal noise. The shot noise is generated by the statistical fluctuations of currents in the PD, while the thermal noise is due to its equivalent shunt resistance. From [3.1], I_{n-PD} can be estimated as

$$\overline{I_{n-PD}^2} = \left[2q(I_D + I_{PD} + I_B) + \frac{4kT}{R_{SH}} \right] B_n , \quad (3.9)$$

where q is the charge of an electron, and I_D , I_{PD} and I_B represent the dark current, the signal current and the current induced by the background light, respectively. R_{SH} denotes the shunt resistance of the PD and B_n represents the noise bandwidth of the system, which is equal to the -3 -dB bandwidth of the TIA.

The TIA's overall input referred noise comes from the thermal noise of the feedback resistor R_{FB} and the noise generated by the TIA itself. The TIA noise can be derived as follows [3.4]:

$$\overline{I_{n_TIA}^2} = \left[\overline{I_{n_Amp}^2} + \frac{4kT}{R_{FB}} + \left(\frac{V_{n_Amp}}{R_{FB}} \right)^2 + \frac{(2\pi V_{n_Amp} B_n C_s)^2}{3} \right] B_n, \quad (3.10)$$

where I_{n_Amp} and V_{n_Amp} represent the input noise current and the input noise voltage of the amplifier, respectively, Z_{TIA} is the transimpedance gain of the amplifier and C_s is the total capacitance at the TIA input.

The noise contributed by the passive HPF is from the thermal noise contributed by the resistance of R_{HP1} and R_{HP2} in parallel. Therefore, it can be expressed as

$$\overline{I_{n_HPF}^2} = 4kT(R_{HP1} || R_{HP2}) B_n / Z_{TIA}^2. \quad (3.11)$$

As the noise coupled from the supply depends on the hardware setup and thus cannot be simply expressed by an equation, usually it is measured by an oscilloscope.

Finally, the overall noise referred to the TIA input is derived as

$$\overline{I_{n_tot}^2} = \overline{I_{n_PD}^2} + \overline{I_{n_TIA}^2} + \overline{I_{n_HPF}^2} + \overline{I_{n_VCC}^2}. \quad (3.12)$$

3.5 Receiver Signal-to-Noise Ratio

With both the signal and noise currents calculated, the signal-to-noise ratio for the front-end can be derived. Furthermore, the input sensitivity of the baseband should be taken into account, because it sets the minimum voltage swing V_{TH} required for a correct digital decision. The threshold voltage V_{TH} needs to be referred to the TIA input and subtracted from the received signal when calculating the SNR. Consequently, the SNR is expressed as [3.5]

$$SNR = \overline{(I_{PD_RMS} - I_{min})^2} / \overline{I_{n_tot}^2}. \quad (3.13)$$

Apart from the above analysis, there are some distortions and degradations that are difficult to quantify, for instance, clock jitter, inter-symbol interference, FPGA noise, electromagnetic interference from nearby electronic equipment, parasitic resistance of PCB traces, etc. Therefore, an implementation loss IL factor is used to account for the SNR degradation caused by these unquantifiable factors. Hence, the final expression for the estimated SNR becomes

$$SNR = 10 \text{ Log } [\overline{(I_{PD_RMS} - I_{min})^2} / \overline{I^2_{n_tot}}] - IL . \quad (3.14)$$

References

- [3.1] R. Roberts and Z. Xu, "Update on VLC link budget work," *IEEE 802.15.7 VLC Standard Meeting*, Document #: 802.15-09-0635-01-0007, Sept. 2009.
- [3.2] J. M. Palmer. Radiometry and Photometry FAQ. [Online], Available: <http://fp.optics.arizona.edu/Palmer/rpfaq/rpfaq.htm>.
- [3.3] F. R. Gfeller and U. Bapst, "Wireless in-house data communication via diffuse infrared radiation," *IEEE Proceedings*, vol. 67, no. 11, pp. 1474–1486, Nov. 1979.
- [3.4] X. Ramus, "Transimpedance considerations for high-speed amplifiers," *Texas Instruments*, Appl. Rep. SBOA122, Nov. 2009
- [3.5] *Optical Communication Photodiodes and Receivers*, OSI Optoelectronics, pp. 74-81.

CHAPTER 4 DESIGN AND MEASUREMENT OF A DISCRETE VLC TRANSCIVER SYSTEM

4.1 System Specifications

A discrete VLC transceiver is designed using commercial white LEDs as transmitter, a low-cost photodiode based transimpedance amplifier as the receiver front-end and the digital baseband implemented on an FPGA. The system specifications are discussed in the following

4.1.1 Communication Distance

The proposed VLC system is targeted for indoor communication in a typical office environment that uses white LEDs for simultaneous illumination and communication. Therefore, in view of the discussions on design considerations provided in chapter 2, the desired communication distance is two meters.

4.1.2 Modulation Scheme and BER Requirement

On-off-keying (OOK) is considered quite popular in VLC systems due to its easy implementation and acceptable performance. Therefore, In order to keep the system construction simple, not-return-to-zero (NRZ) OOK is chosen as the modulation scheme.

The BER is targeted to be 10^{-6} , as it is considered a typical number for wireless communication systems. The SNR required for this BER for an NRZ-OOK system is $\sim 20\text{dB}$, which is calculated using Eq. (2.1).

4.1.3 Data Rate

The data rate is highly dependent on the overall bandwidth of the system. Generally, the bandwidth of the system is limited by the LEDs. Since the commercial white LEDs are designed for illumination purposes, their bandwidth does not support extremely high switching rates. Therefore, in order to specify an achievable data rate, the bandwidth of the LEDs must be known beforehand. Unfortunately, vendors do not provide the bandwidth of LEDs in their data sheets. Thus, the bandwidth of the LED must be measured with the help of a high speed photoreceiver.

The measurement setup for measuring the bandwidth of the commercial white LED is shown in Figure 4.1. The LEDs are switched on and off using a function generator whose frequency is manually swept. The VLC signal is received via a high speed photoreceiver (New Focus 1801) with a bandwidth of 125 MHz.

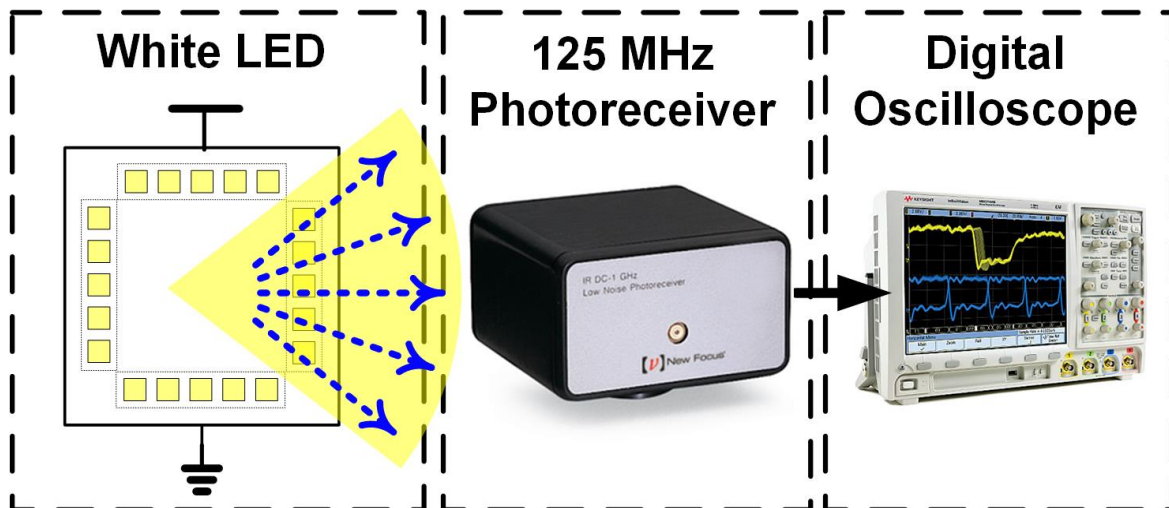


Figure 4.1 Setup for Measuring Bandwidth of White LEDs.

Figure 4.2 shows the measured frequency response curve illustrating a -3dB bandwidth of 2.2 MHz. As such, the data rate chosen is 2.5 Mb/s.

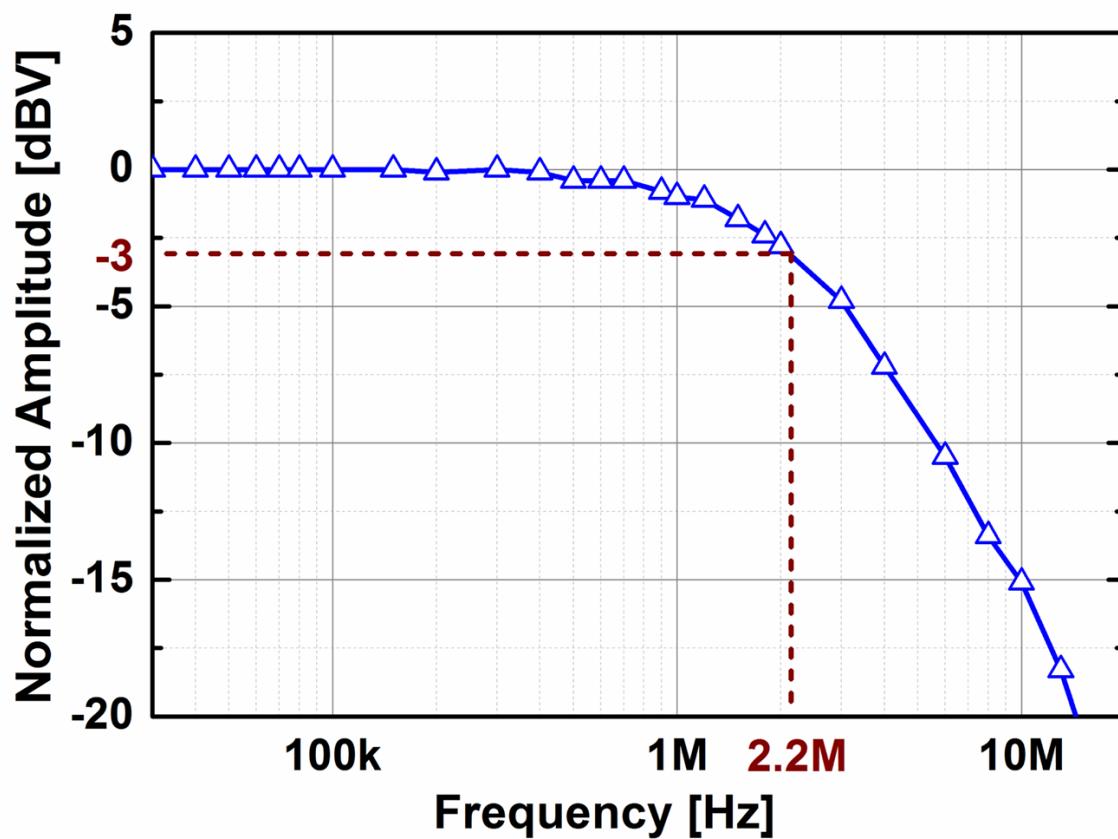


Figure 4.2 Measured Frequency Response of Commercial White LEDs.

A summary of the aforementioned specifications is provided in Table 4.1.

Table 4.1 Target Specifications for a Discrete VLC System.

Modulation Scheme	NRZ-OOK
Data rate	2.5 Mb/s
Distance	2 m
BER	$< 10^{-6}$
Min. SNR	20 dB

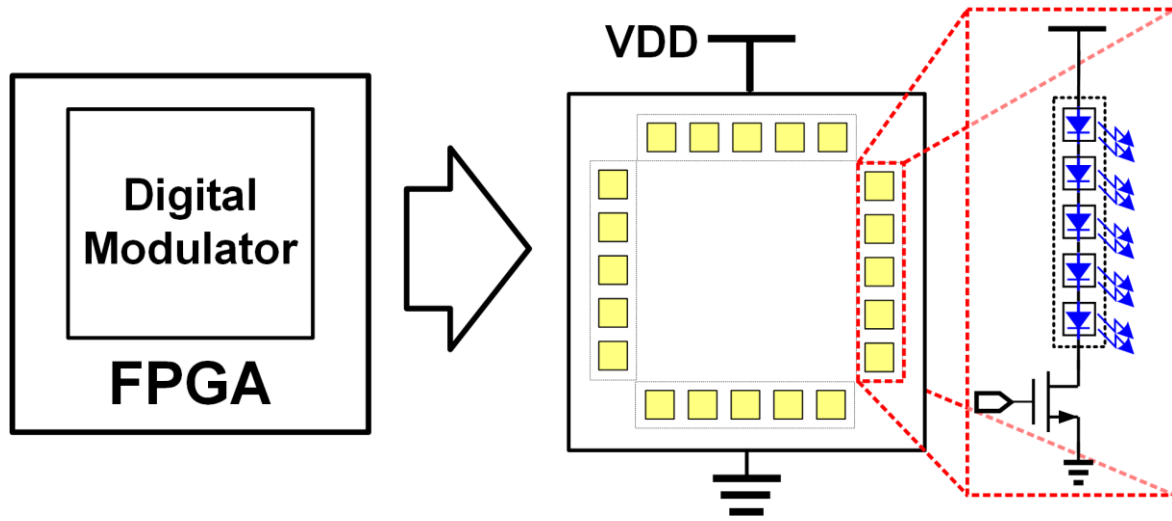


Figure 4.3 VLC Transmitter Composed of a Baseband and 20 LEDs.

4.2 Transmitter Front-End Design and Analysis

The transmitter front-end consists of an array of LEDs with NMOS switches, as shown in Figure 4.3. In the LED array, there are 20 LEDs arranged in four branches each of which is composed of five LEDs in series. The digital signal is applied to the gate of the NMOS in each branch such that the LEDs are switched on / off at the same time to modulate the emitted visible light.

The commercial white LED used in this design is a cool white LED with a color temperature of $\sim 5000\text{K}$. The I-V curve of the LED is measured to study its variation in voltage drop for a given amount of current. Figure 4.4 shows the I-V curve of the LED, which is acquired using a semiconductor parameter analyzer (Agilent 4156C). The measurement indicates that there is a $\pm 2\%$ variation in voltage drop for the same current of 80mA .

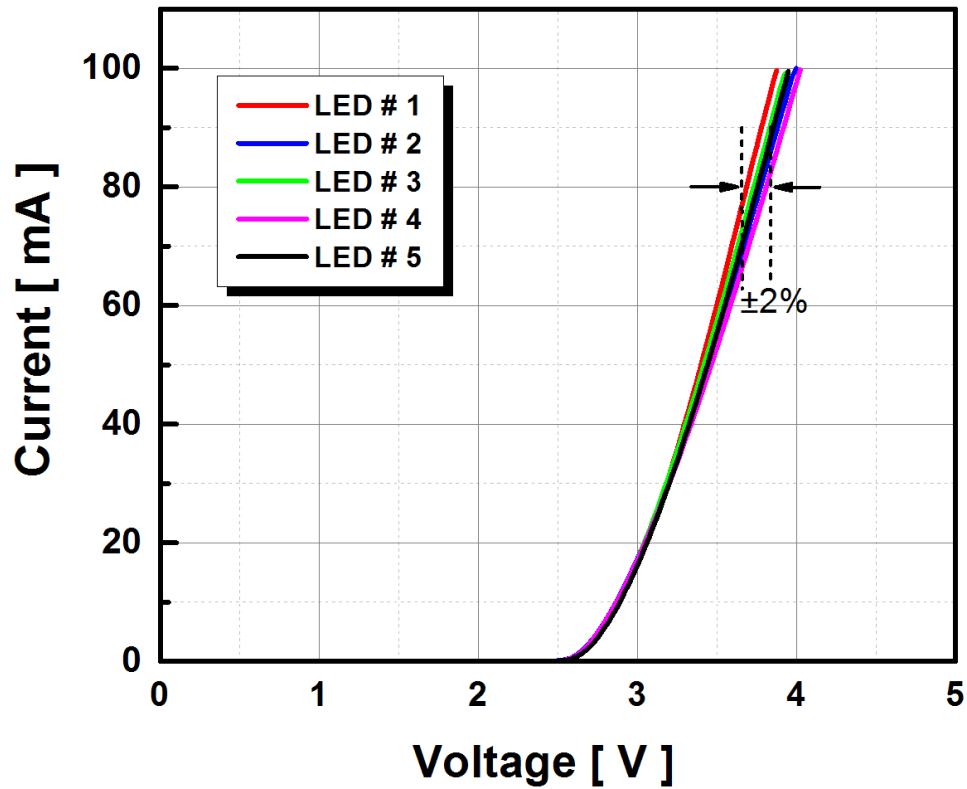


Figure 4.4 Measured I-V Curve of Five White LEDs [4.1].

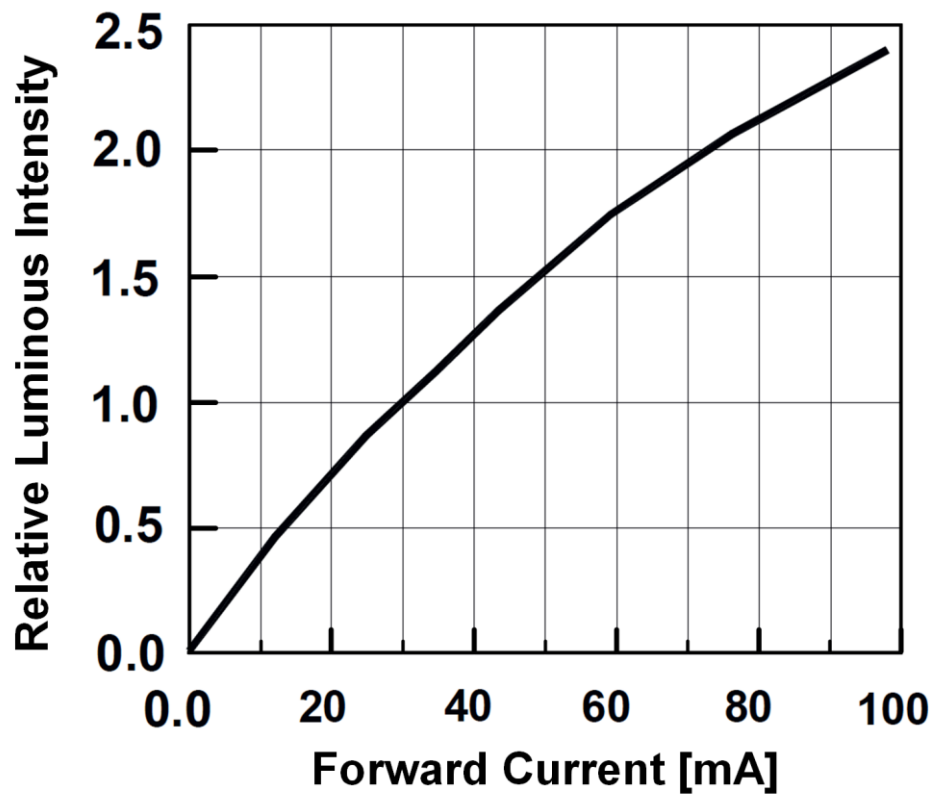


Figure 4.5 Forward Current vs Luminous Intensity of White LED.

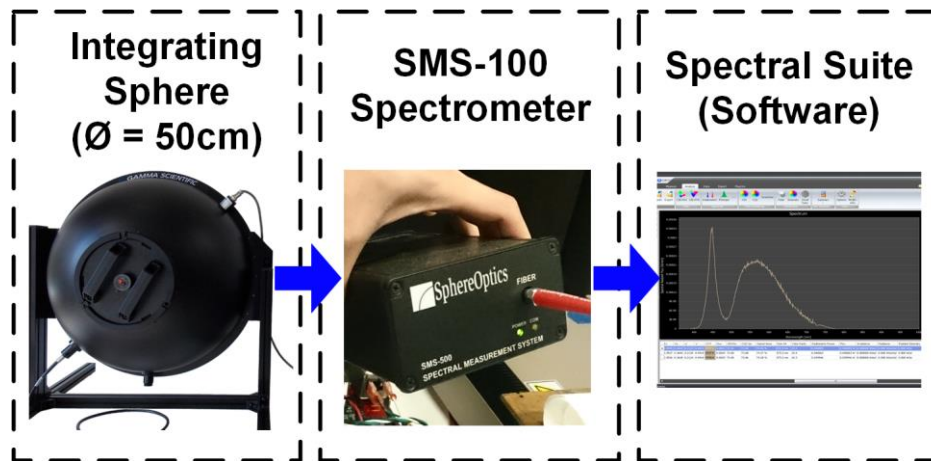


Figure 4.6 Setup for Measuring the Spectral Power Distribution of White LED.

The LED is rated to produce a luminous flux of 9.6 lm for a current of 30-mA. This luminous flux Φ_V provided by the LED datasheet is calibrated by measurement using a lux meter (Extech Easyview 33) and hence a correction factor is incorporated when estimating the transmit power. Moreover, to estimate the amount of flux produced for various amounts of current, the datasheet provides a curve for relative luminous intensities for various amounts of current, as presented in Figure 4.5.

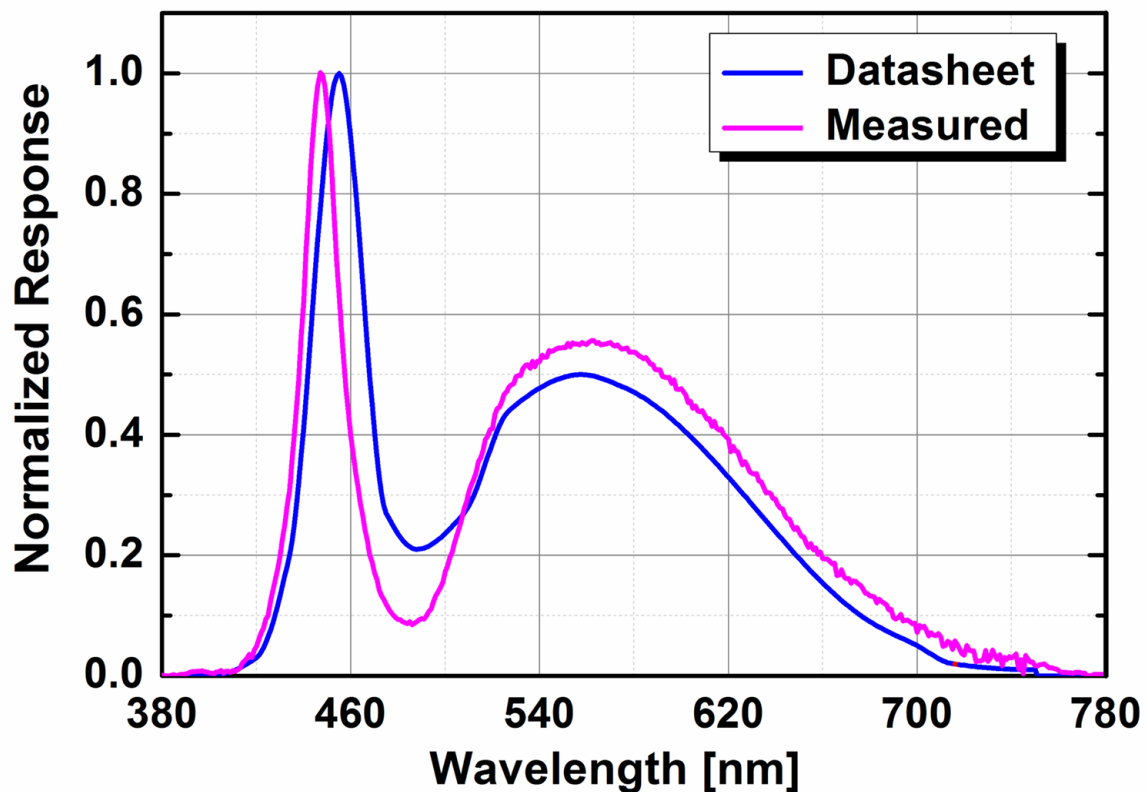


Figure 4.7 Spectral Power Distribution of White LED.

In order to facilitate the link budget calculations, the datasheet also provides a relative spectral distribution curve. However, to verify its accuracy, the spectral distribution of the LED is measured using the setup shown in Figure 4.6. The setup consists of an integrating sphere with a diameter of 50 cm and a spectrometer, SMS-100. The comparison indicates a small discrepancy, as shown in Figure 4.7.

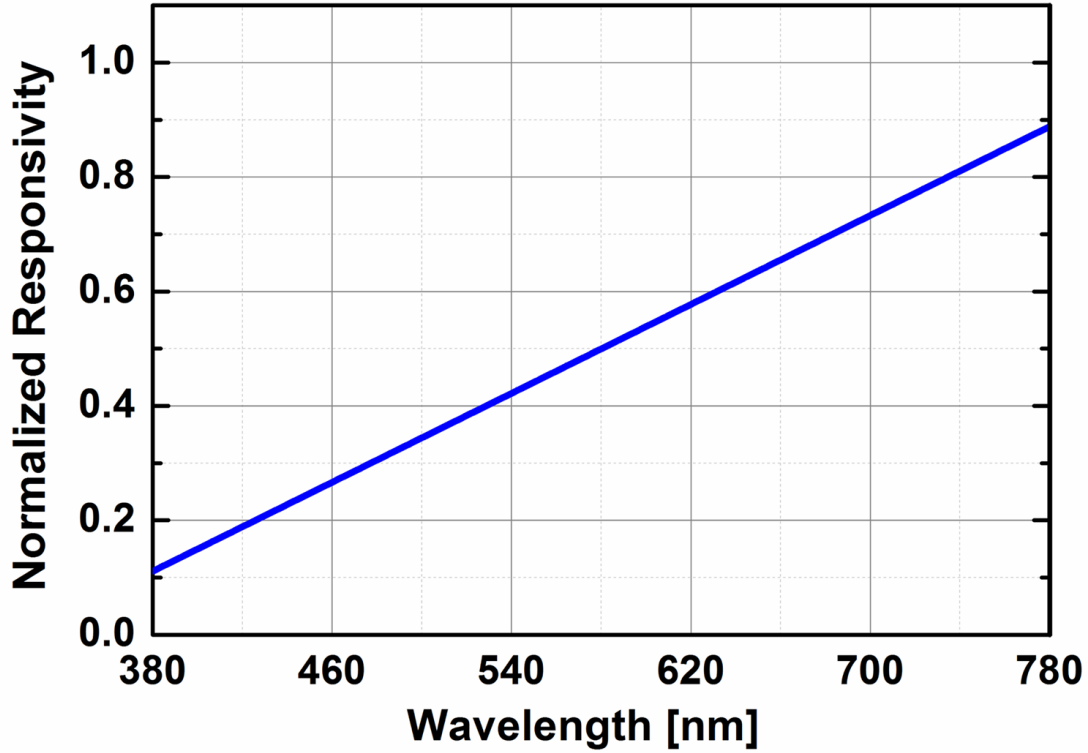


Figure 4.8 Responsivity of the Photodiode.

4.3 Receiver Front-End Design and Analysis

4.3.1 Photodetector

The receiver front-end is designed according to the schematic presented in Figure 3.3. The photodiode is used in photovoltaic mode: i.e., it has no reverse bias voltage applied across it. This mode helps in minimizing the dark current and improving precision. The photodiode offers an input capacitance of 11pF when connected in photovoltaic mode. The photodetector (PD) features a high sensitivity of 0.26 A/W at 550nm within the visible light region. The relative sensitivity plot for the photodiode in the visible region is shown in Figure 4.8. The responsivity of the photodiode decreases when going from a longer wavelength (red) to a shorter wavelength (blue).

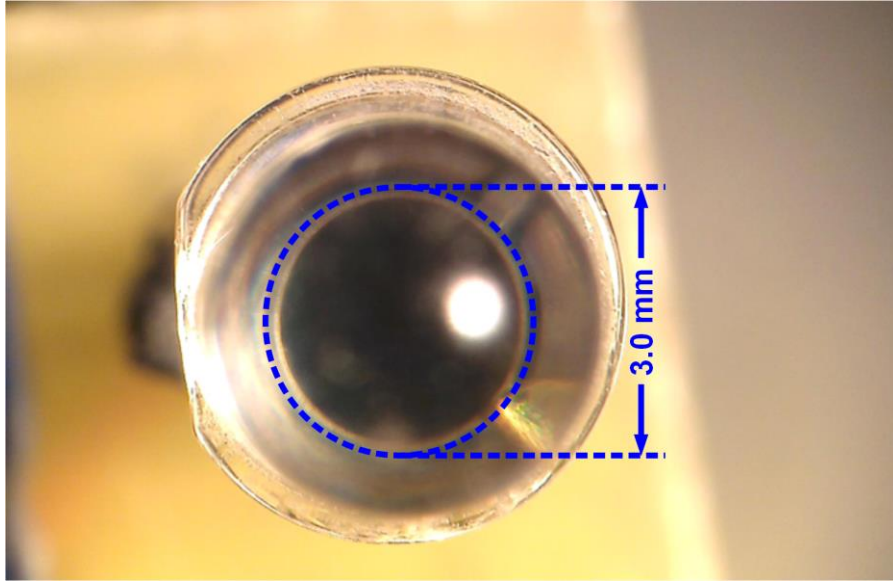


Figure 4.9 Measuring the Effective Area of the PD.

The received photocurrent can be calculated by incorporating the transmit power, PD sensitivity and area, as demonstrated in Eq. (3.8). However, the PD area provided in the datasheet does not consider the magnification effect of the glass shielding that covers the top of the PD. Therefore, the PD area is measured as shown in Figure 4.9 and found to be 7mm^2 .

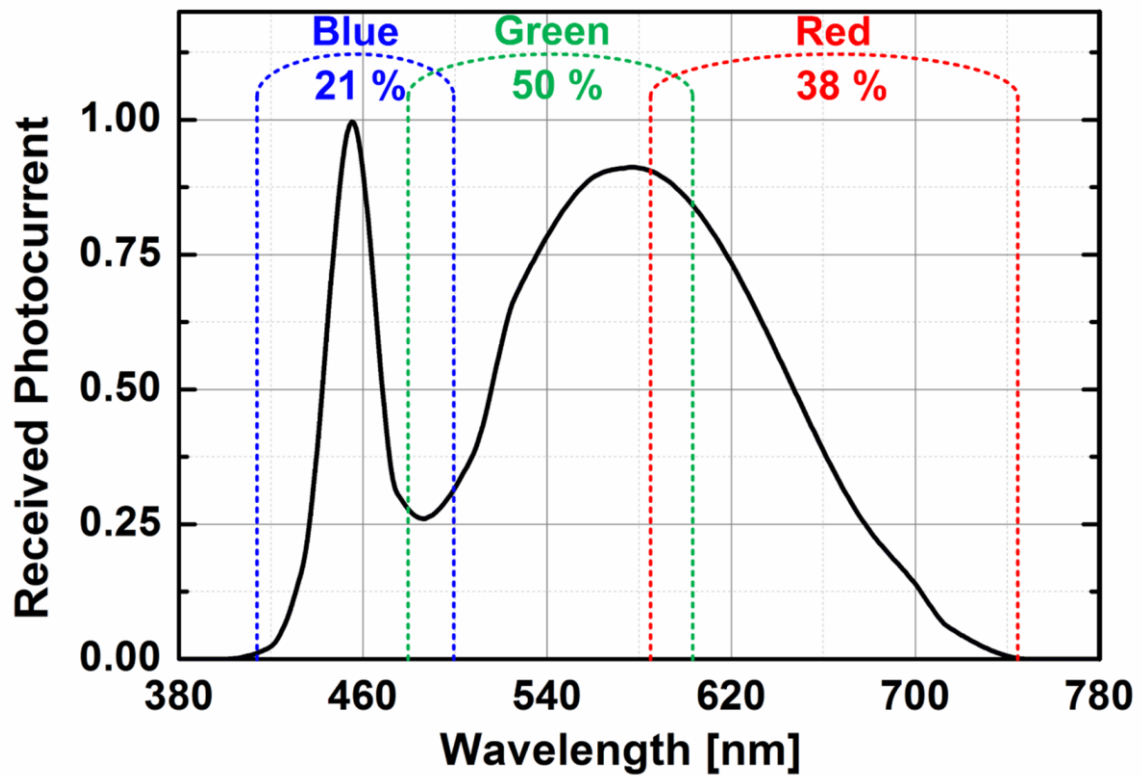


Figure 4.10 Received Photocurrent Distribution over Different Wavelengths.

The resultant photocurrent distribution is illustrated in Figure 4.10. It can be seen that around half of the received signal power is from the green light, while the remaining 21% and 38% are contributed by the blue light and the red light, respectively. Considering the blue light has a much faster response than both the green and the red one, a blue filter could be placed in front of the PD to enhance the modulation bandwidth of white LEDs by approximately five times [4.2]. However, the signal would become 6.8 dB weaker such that the communication distance would be significantly reduced. Consequently, no blue filter is employed here.

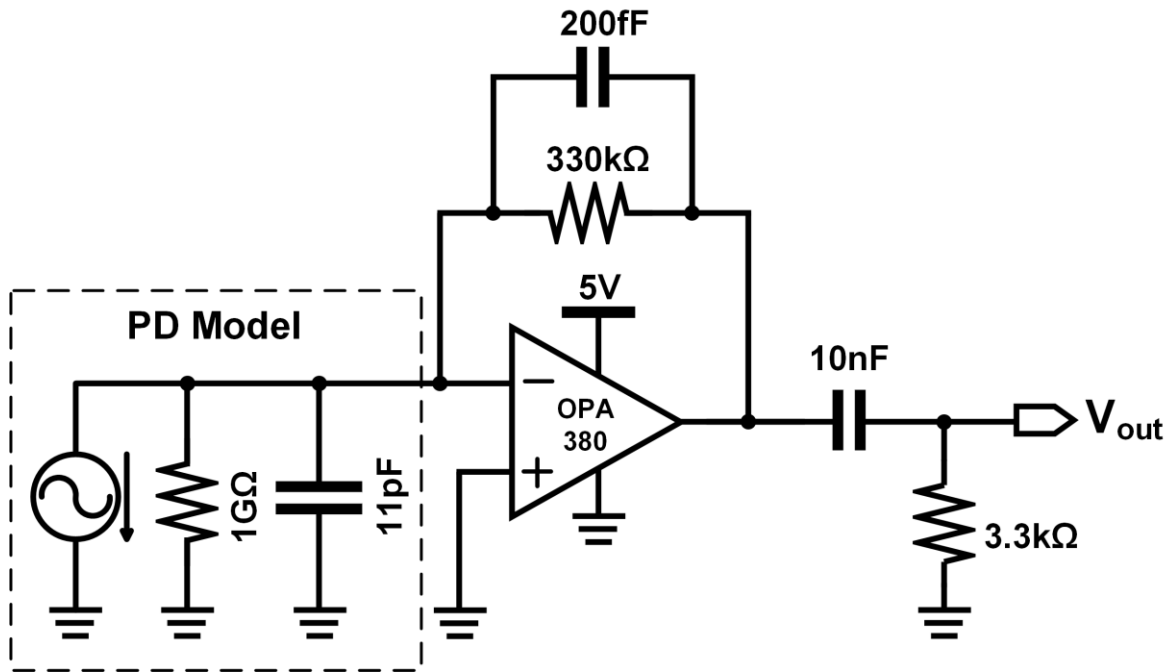


Figure 4.11 Simulation Circuit of Receiver Front-end.

4.3.2 The Amplifier Design

The amplifier is designed using a transimpedance amplifier (TIA) OPA 380 with a gain bandwidth product (GBW) of 90 MHz. The TIA can be operated with a single power supply ranging from 2.7 to 5 volts. The simulation model of the design is illustrated in Figure 4.11. A feedback resistor of 330 kΩ is used to achieve a considerable transimpedance gain of ~ 110 dBΩ with a bandwidth of ~ 2 MHz, which is sufficient for achieving the specified data rate. The gain-bandwidth plot of the design, acquired via simulation, is shown in Figure 4.12. The lower cut-off of 4.8 kHz is realized using an RC high pass filter (HPF) to attenuate low-frequency noise from ambient and florescent light sources and DC components. The output signal from the front-end is fed to the receiver baseband implemented on an FPGA for digital signal processing. The PCB board of the receiver front-end is shown in Figure 4.13.

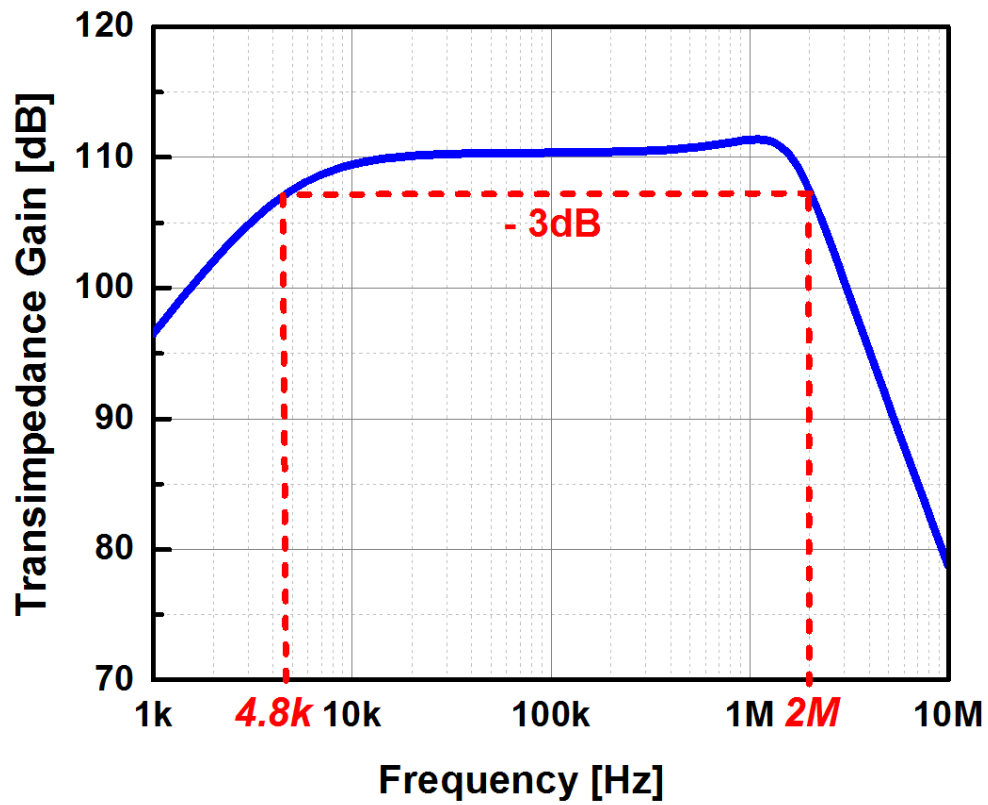


Figure 4.12 Gain-Bandwidth Response of the Transimpedance Amplifier.

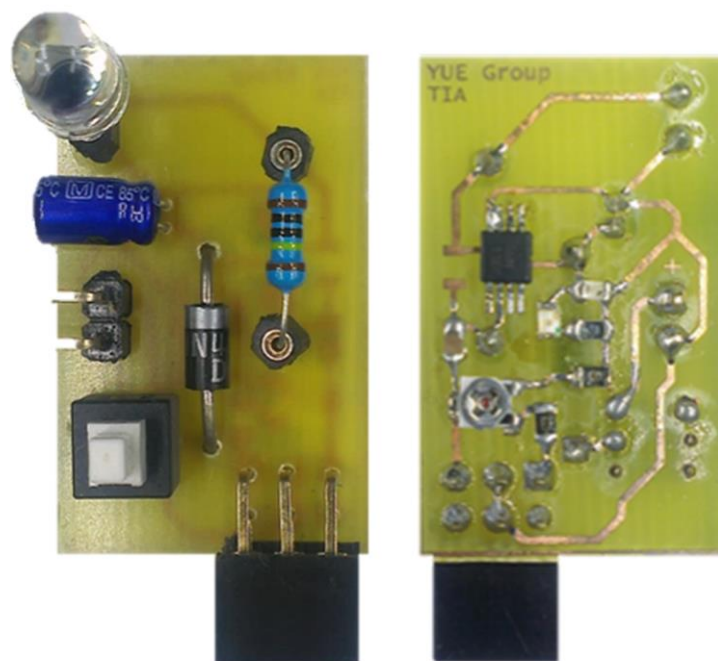


Figure 4.13 PCB of the Receiver Front-end [4.4].

4.4 Digital Baseband Design and Implementation

Both the transmitter and receiver digital basebands are implemented in Xilinx Virtex-5 xc5vlx110t FPGAs. All the building blocks are designed using Verilog HDL.

In order to facilitate the clock data recovery (CDR) circuit to lock-in the phase of the receiver clock with the incoming data, each data packet coming from the payload consists of a synchronization pattern (60-bits) and a synchronization header (16-bits). As illustrated in Figure 4.14, each data packet contains a payload of ~1.2 Kbytes of a pseudo random binary sequence (PRBS) stream, which is verified at the receiver using a local PRBS generator to evaluate the BER performance of the link. The designs of the transmitter and receiver are described in the following sections.

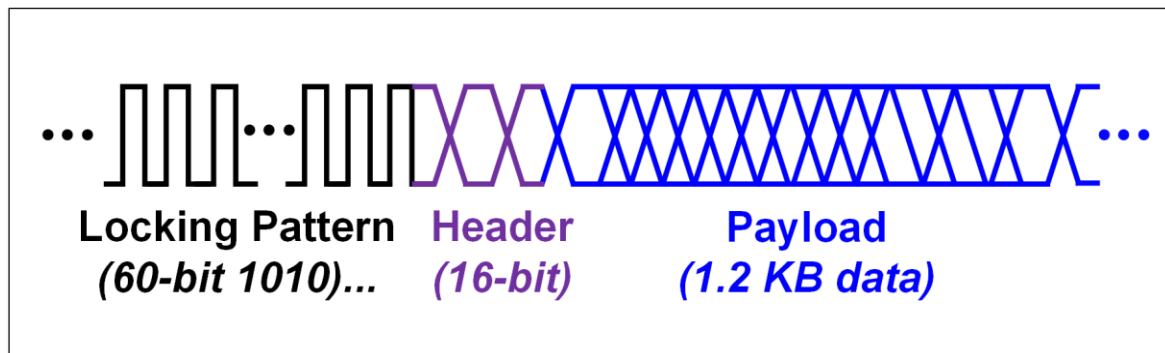


Figure 4.14 Data Packet Format.

4.4.1 Transmitter Baseband Design

The architectural block diagram of the transmitter is provided in Figure 4.15. The transmitter block predominantly consists of a PRBS stream generator whose output is stored in a payload buffer, while the status of the loading is monitored via a counter. The PRBS generator is implemented via a linear feedback shift register (LFSR) of length 7. As such, a PRBS pattern of 2^7-1 length is produced. The design runs at a 2.5 MHz clock which is acquired from a 100 MHz system clock using a /40 clock divider. All the control signals and status signals are handled via a finite state machine (FSM) controller. Once the payload is filled, the data is output via an OOK modulator after adding the header. The output data modulates the NMOS transistors of the LED array to produce the VLC signal.

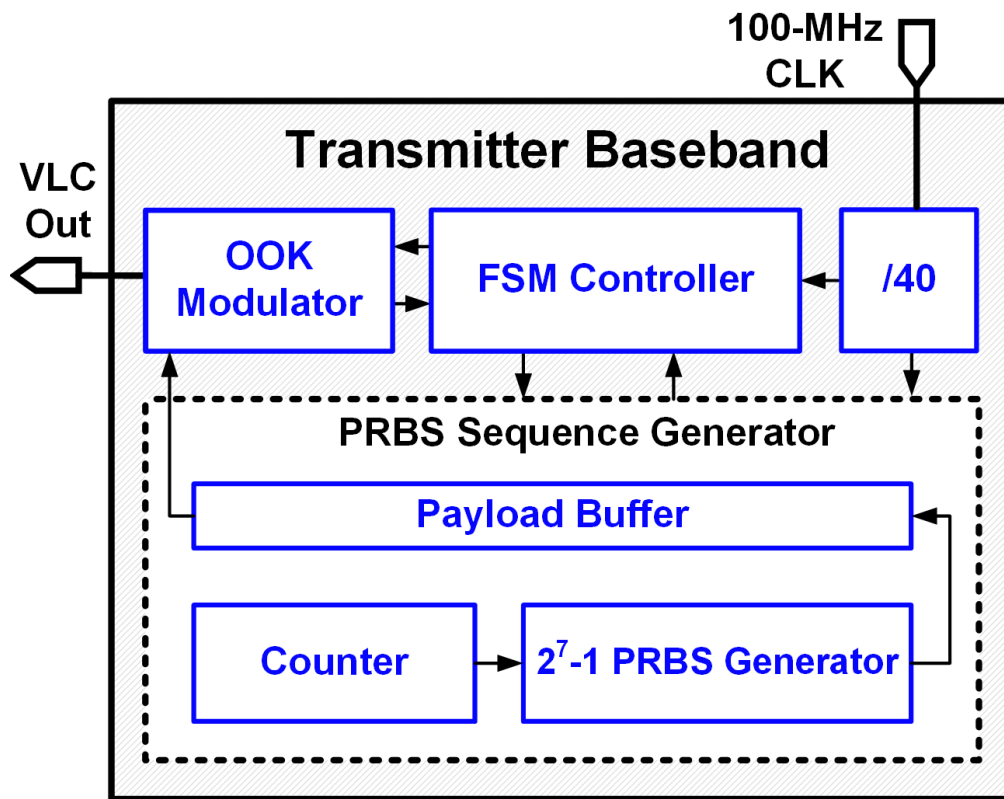


Figure 4.15 Transmitter Baseband Architecture.

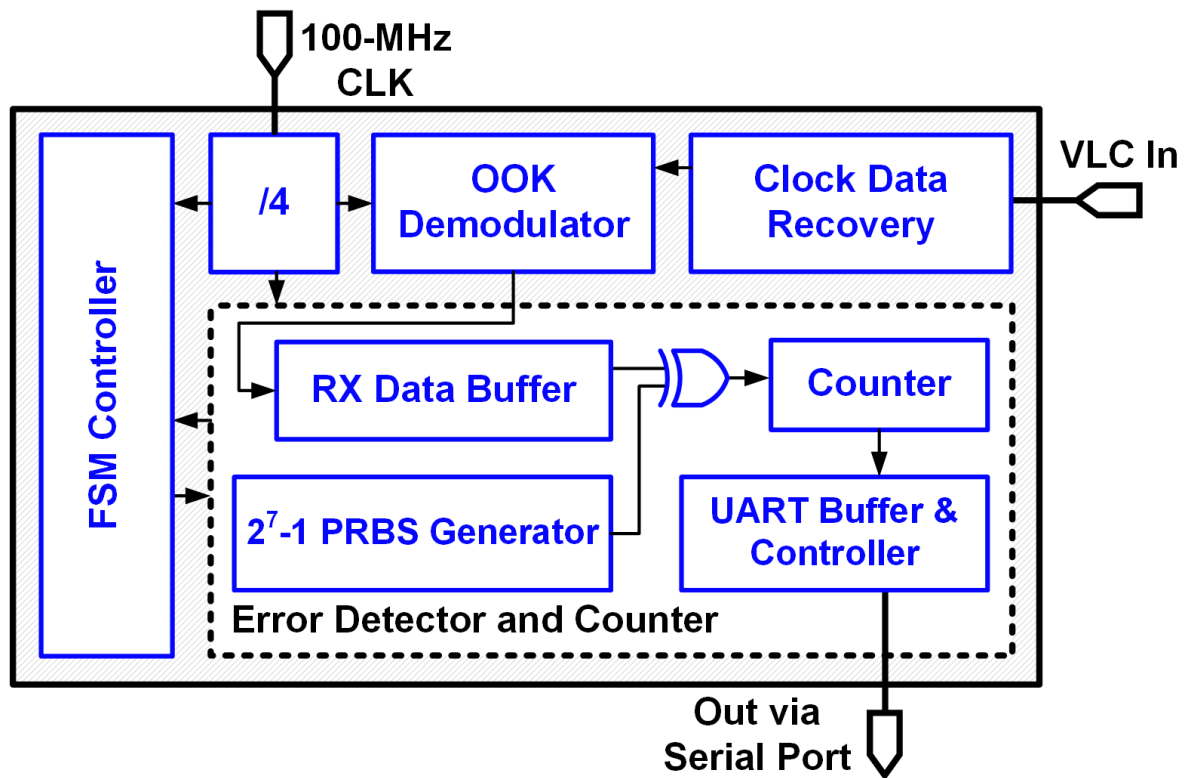


Figure 4.16 Receiver Baseband Architecture.

4.4.2 Receiver Baseband Design

The receiver consists of a CDR block, followed by an OOK demodulator and an error detector and counter module, as shown in Figure 4.16. The status and control signals are managed by the FSM controller module. The $/4$ clock divider is used to produce a 25 MHz clock, which is 10 times faster than the transmitter clock, as it is used in the CDR for oversampling.

The CDR is implemented based on the phase picking algorithm [4.3], illustrated in Figure 4.17. Three periods of received data are sampled using a 10 times faster sampling clock before being stored in a 30-bit buffer for further processing. The sample acquisition is tracked using a 10X sample counter, as shown in Figure 4.17. Following the acquisition, edge detection is performed on adjacent symbols to find the position of edges in the data. The edge information is processed by the valid edge decision block to verify whether the edge is in its correct position. Based on the position of the edge, either a skip signal is declared to skip one count for a lagging phase in the clock or a hold signal is declared to stop for one count to compensate for a leading clock phase. The counter up-counts normally if the clock phase is aligned to the data clock.

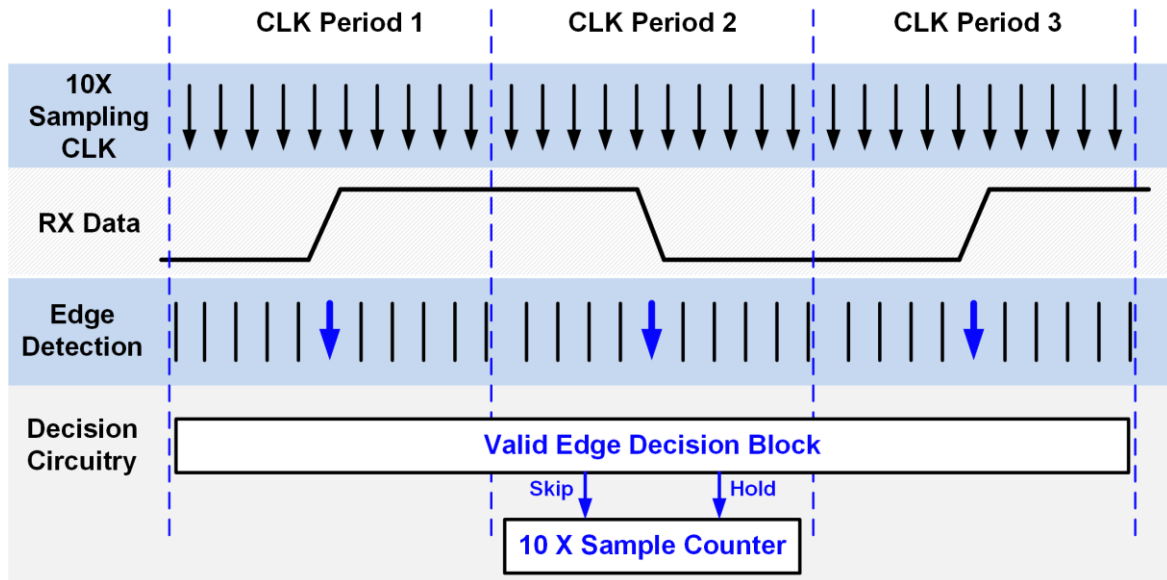


Figure 4.17 Clock Data Recovery Illustration.

The received data is decoded by the OOK demodulator and stored in the RX buffer in the error detector and counter module. A local PRBS generator is first filled with the seven bits of incoming data to make sure that both the transmitted and received PRBS streams are aligned. Once aligned, the incoming data from the RX data buffer is compared with the local PRBS stream to count the number of errors occurred during the communication. The errors and total number of bits are stored in a buffer inside UART buffer & controller module, which frames the data before sending it out via serial port. The serially transferred data is received using MATLAB on a computer for BER calculation, with a 99% confidence interval.

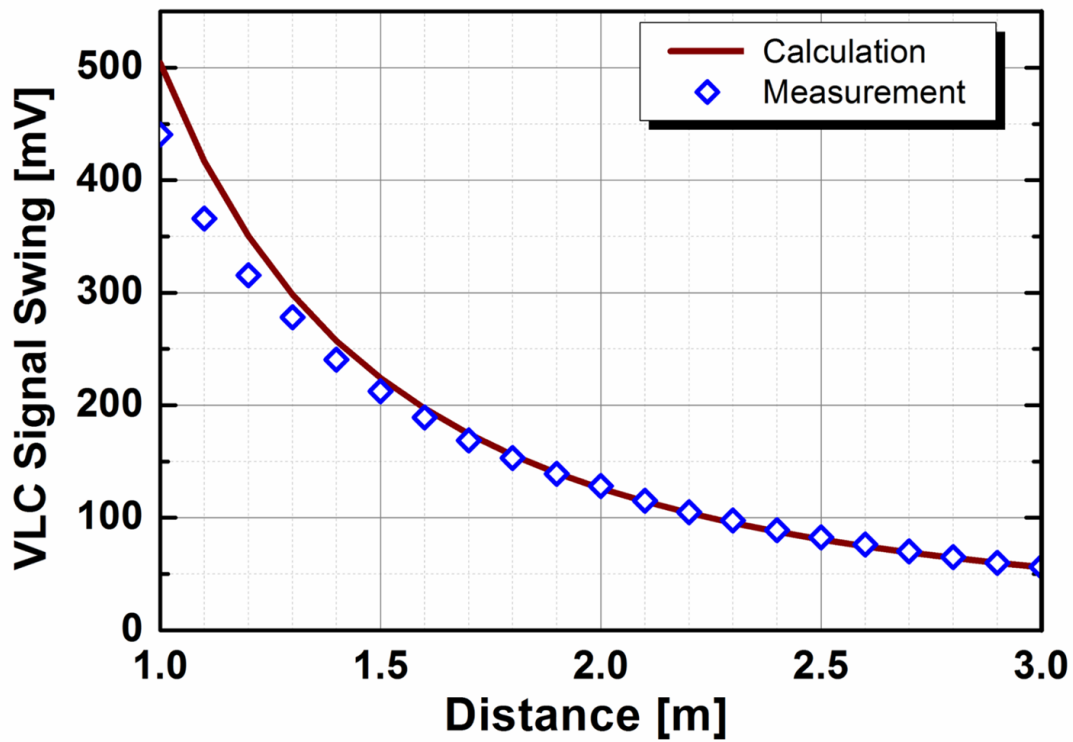
The FPGA resource utilization for both the transmitter and receiver is summarized in Table 4.2.

Table 4.2 FPGA Resource Utilization Summary.

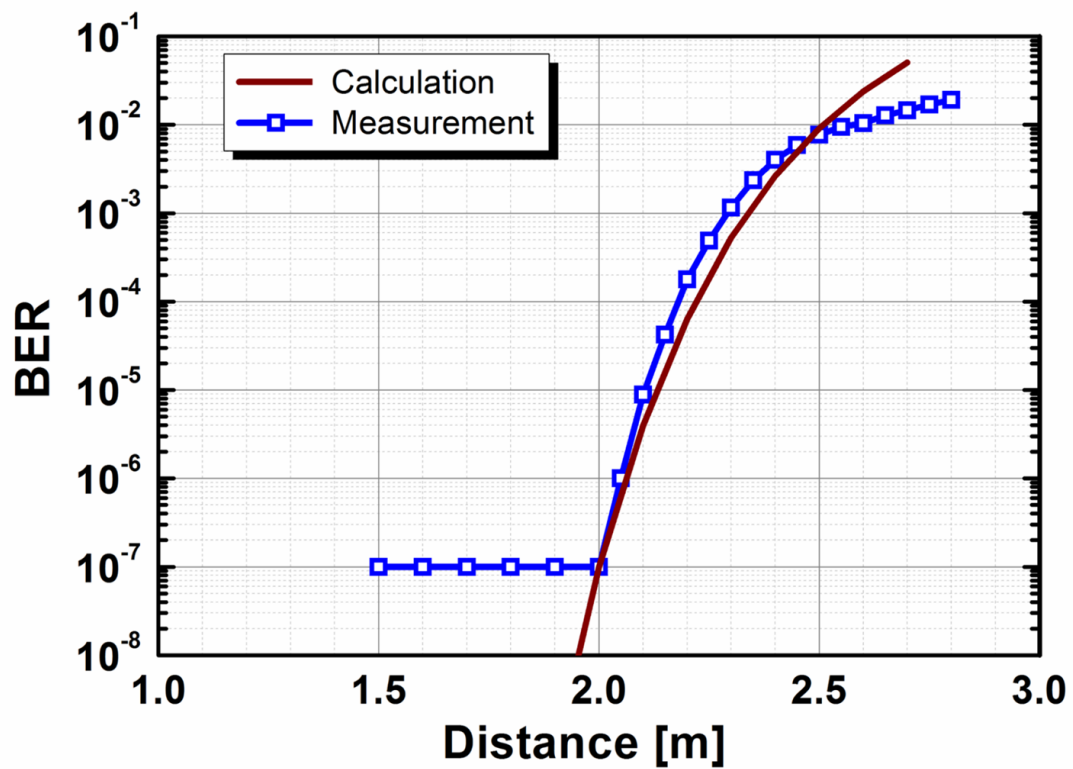
FPGA Resource	TX		RX	
	Used	%	Used	%
Slice registers	97	0.14	287	0.42
Slice LUTs	395	0.57	597	0.86
Bonded IOBs	22	3.4	13	2

4.5 Hardware Measurements

The measurement setup of the VLC transceiver system is shown in Figure 4.19. The LED array draws an average current of 200mA from a 20-V supply. The calculated and the measured VLC signal amplitudes at different distances are plotted in Figure 4.18 (a), demonstrating a good agreement. Using the link budget analysis in chapter 3 and Eq. (2.1), with an estimated implementation loss of 11 dB, the BER is calculated and plotted in Figure 4.18 (b). By programming the transmitter to send a 2^7-1 PRBS data sequence and comparing the received data with a locally generated PRBS sequence at the receiver, the number of error bits is counted and the measured BER is also plotted in Figure 4.18 (b). The data points for $BER < 10^{-7}$ are not measured because of the extremely long time required. The two BER plots agree well with each other, thereby verifying the accuracy of the optical wireless link budget analysis. Moreover, as shown by the measured BER curve, the VLC system achieves a data rate of 2.5 Mb/s with $BER \leq 10^{-6}$ at a distance of 2.05 m, fulfilling the target specification and thus demonstrating the validity of the systematic design approach.



(a)



(b)

Figure 4.18 (a) VLC Signal Swing, Measured vs Calculated.

(b) Bit Error Rate, Measured vs Calculated.

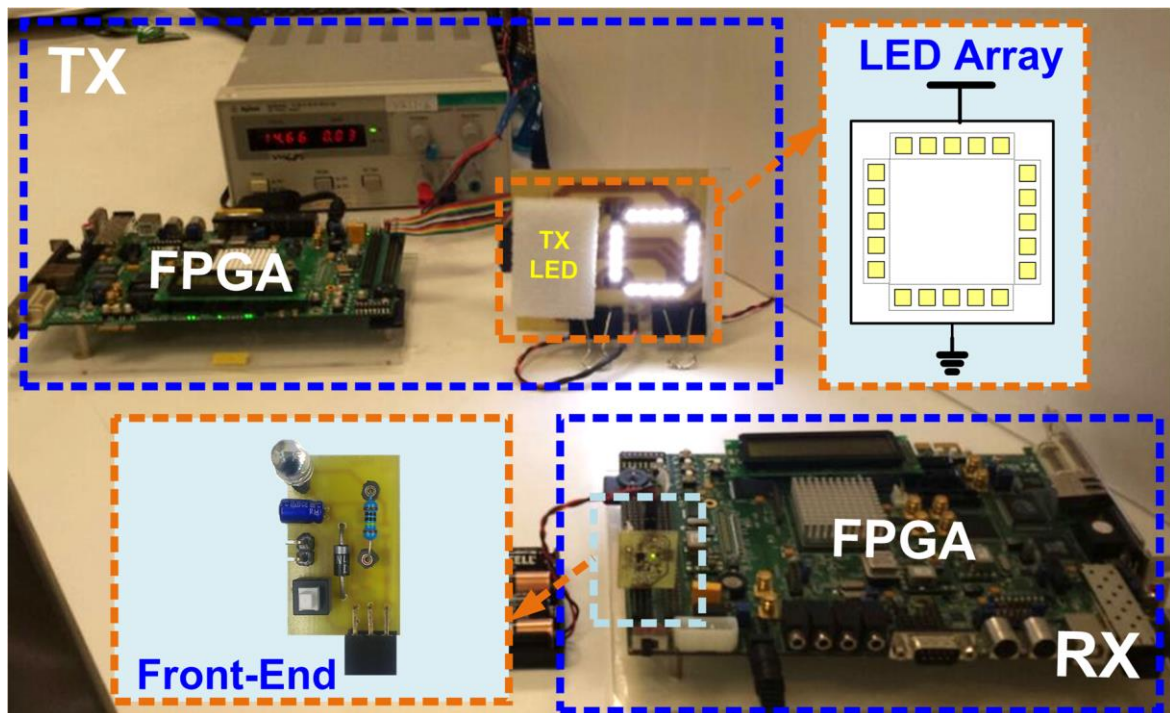


Figure 4.19 Measurement Setup for Discrete VLC Transceiver System.

References

- [4.1] F. Che, B. Hussain, X. Li, L. Wu, C. P. Yue, “A fully integrated IEEE 802.15.7 visible light communication transmitter” submitted to *Journal of Solid State Circuits (JSSCC)*
- [4.2] H. L. Minh, D. O’Brien, et al., “100-Mb/s NRZ visible light communications using a postequalized white LED,” *IEEE Photonics Technology Letters*, vol. 21, no. 17, , pp. 1063-1065, Aug. 2009.
- [4.3] C-K. K. Yang, “Design of high-speed serial links in CMOS,” Ph.D. Dissertation, Stanford University, 1998.
- [4.4] F. Che, B. Hussain, K. Qiu, M. Liu, L. Wu, C.P. Yue, “Hardware and software co-design of visible light indoor positioning systems for robotics”, presented at the 2014 *International Conference on Advanced Control, Automation and Robotics (ACAR)*, Hong Kong, Sep. 2014.

CHAPTER 5 DESIGN AND MEASUREMENT OF AN IEEE 802.15.7 VLC SYSTEM WITH CMOS TRANSMITTER SOC

5.1 Introduction to IEEE 802.15.7 Standard

The IEEE 802.15.7 standard [5.1] is a working group of IEEE 802 standards committee that is responsible for developing standards for wireless personal area networks (WPAN). The standard defines physical layers (PHY) and medium access control layers (MAC) for short-range wireless optical communication using visible light. The scope of the standard covers the visible light spectrum from 380nm to 780nm and delivers data rates sufficient to support audio and video multimedia services. The standard supports three classes of devices, infrastructure, mobile and vehicle, which differ in their operation constraints, e.g. size, mobility, data rate and communication distance etc. Furthermore, the standard defines three network topologies for communication i.e. peer-to-peer, star and broadcast topologies, as illustrated in Figure 5.1. The peer-to-peer topology is VLC communication between two standard transceivers, whereas the star topology defines a method for communicating between multiple standard transceivers whose communication is coordinated via a coordinator, and the broadcast topology describes unidirectional communication through a single transmitting device to multiple receivers.

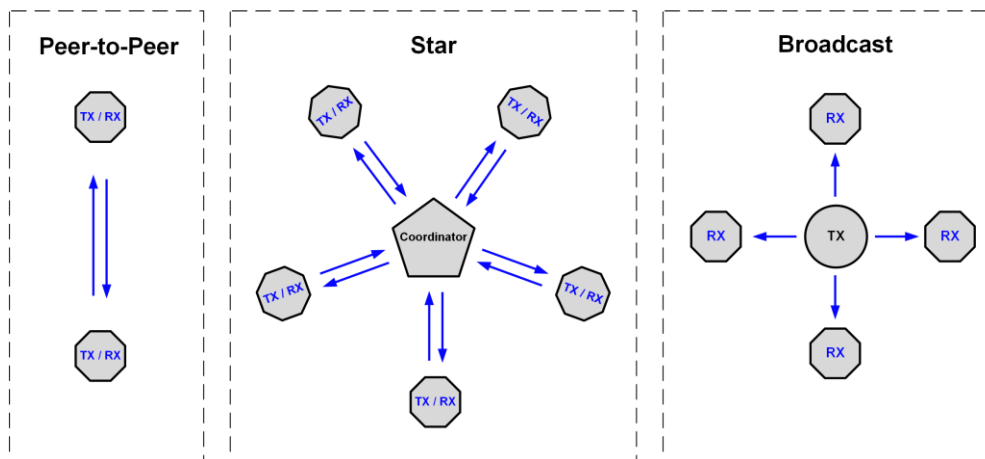


Figure 5.1 Network Topologies in IEEE 802.15.7 Standard.

Table 5.1 PHY Data Rates and Potential Applications.

	Application	Modulation	Data Rates
PHY-I	Location-Based Information Delivery	OOK & VPPM	11.67 ~ 266.6kb/s
PHY-II	P2P Wireless Data Transmission	OOK & VPPM	1.25 ~ 96Mb/s
PHY-III	P2P Wireless Data Transmission	CSK	12 ~ 96Mb/s

Table 5.1, lists the three PHYs defined in the standard along with the type of modulation scheme used, achievable data rates and potential applications. As shown in Figure 5.2, the modulation domain spectrum reveals the range of optical clock rates used in the PHY. Excluding the low frequencies below 1 kHz due to ambient light interference, the optical clock rates for PHY I range from 200 kHz to 400 kHz. Thus, the data rate of PHY-I is limited to 266 Kb/s and possible application is location based information delivery that requires relatively lower data rates. On the other hand, PHY-II and PHY-III are driven by clock rates in the order of 100 MHz and, as such, offer much higher data rates. However, as described in previous chapters, the modulation bandwidth of commercial LEDs cannot support these high clock rates without employing complex circuit techniques that will make the system construction costly and impractical. Therefore, keeping in view the limitation of LED bandwidth, PHY-I is implemented in the proposed system to support location based information transmission applications.

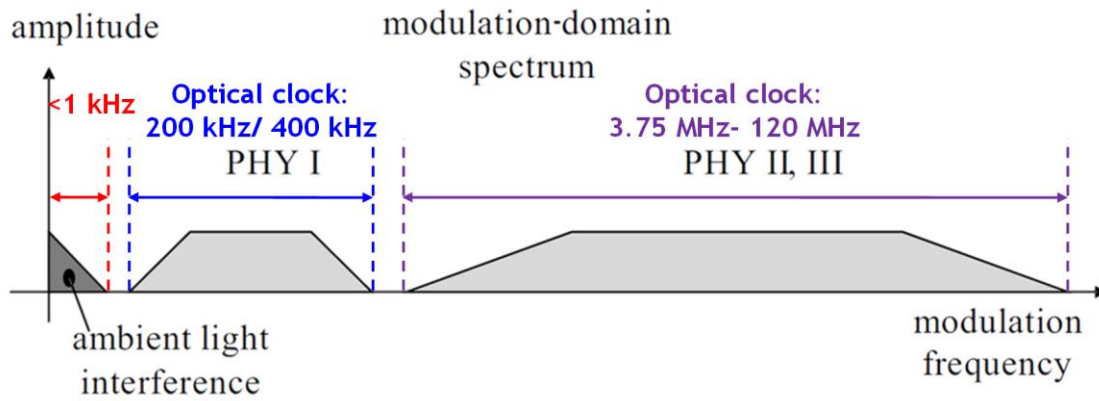


Figure 5.2 Modulation Domain Spectrum of IEEE 802.15.7 PHY.

Table 5.2, lists the modulation and coding schemes (MCS) used in PHY-I along with achievable data rates. PHY-I supports two types of modulation scheme, OOK and variable pulse position modulation (VPPM), that run at 200 kHz and 400 kHz clock rates, respectively. In addition, a run-length limiting encoder (RLL) is employed to balance the perceived brightness level from the light source and mitigate any possible flicker due to the transmission of a long stream of either 1s or 0s. Furthermore, two types of error control coder (ECC), Reed-Solomon (RS) and convolutional codes (CC), have been included to guarantee reliable transmission of data in poor channel (low SNR) conditions. Both coders have a variety of code rates that can be chosen on the basis of trade-off between achievable data rates and communication reliability.

Table 5.2 Summary of PHY-I Modulation, Coding Schemes and Data Rates.

Modulation	RLL code	Optical clock rate	RS code	Convolutional code	Data rate
OOK	Manchester	200 kHz	(15,7)	1/4	11.67 kb/s
			(15,11)	1/3	24.44 kb/s
			(15,11)	2/3	48.89 kb/s
			(15,11)	none	73.3 kb/s
			none	none	100 kb/s
VPPM	4B6B	400 kHz	(15,2)	none	35.56 kb/s
			(15,4)	none	71.11 kb/s
			(15,7)	none	124.4 kb/s
			none	none	266.6 kb/s

The standard packet format for data transmission over PHY-I is depicted in Figure 5.3. Each standard packet, also termed as a physical layer data unit (PPDU), consists of three main fields: a preamble or synchronization header (SHR), physical layer header (PHR), and payload or physical service data unit (PSDU). The SHR is transmitted first and contains a pattern of at least 64 alternate 1s and 0s called a fast locking pattern (FLP), which helps the receiver CDR lock-in phase with the transmitter's clock. FLP is followed by a series of topology dependent patterns (TDP) which indicate the type of network topology used and signal the start of a data frame. The PHR contains a PHY header and header check sequence (HCS) followed by an optional field. The PHR is always transmitted at the slowest data rate for the chosen clock rate and it contains information about the length and modulation and coding schemes (MCS) to be used in the PSDU, which carries the data to be transmitted, and, finally, the HCS is used to verify the correctness of the PHY header.

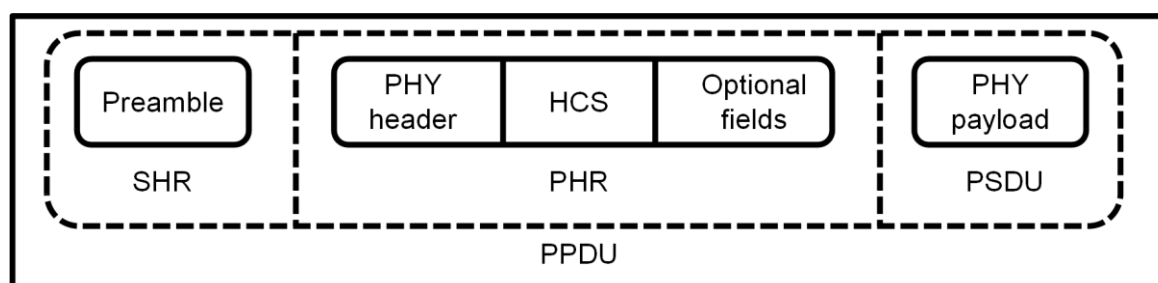


Figure 5.3 PHY-I Data Packet Format.

5.2 Target Specifications for Link Budget Verification

Without loss of generality, a medium data rate of 100 kb/s is used as the target for link budget analysis and experimental verification. Since the data rate is much lower in comparison to the discrete VLC system described earlier, the receiver gain can be increased by trading off some of the excess bandwidth. Thus, the overall sensitivity of the receiver is expected to improve and, as such, the target distance is set be 3.5m. A summary of specifications for link budget verification is given in Table 5.3.

Table 5.3 Target Specifications for IEEE 802.15.7 VLC Link.

Modulation Scheme	NRZ-OOK
Data rate	100 kb/s
Distance	3.5 m
BER	$< 10^{-6}$
Min. SNR	20 dB

5.3 Design of a CMOS VLC Transmitter SoC

A fully integrated CMOS SoC that integrates an IEEE 802.15.7 PHY-I digital baseband, a boost LED driver and a VLC modulator is used as the VLC transmitter [5.2]-[5.3]. The block diagram of the overall architecture of the SoC is presented in Figure 5.4.

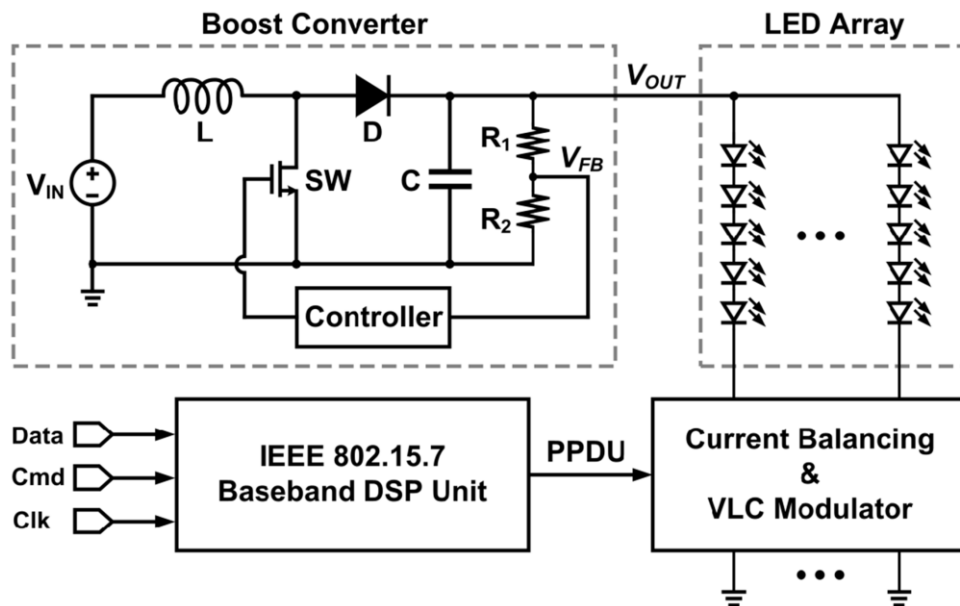


Figure 5.4 Architectural Block Diagram of VLC Transmitter SoC [5.3].

The system is targeted to be used in portable devices, and, therefore, a current-mode controlled DC-DC boost converter is used to power up the LEDs with an input supply voltage range of 3-5V from a Li-ion battery. The system drives a total of 20 LEDs connected in four branches, with each branch carrying five LEDs in series. A total of 100 mA current flows through each branch and a maximum of 20 V is required to fully turn on all the LEDs in a single branch. Therefore, the boost converter delivers a tunable output voltage of 6-20 V and maximum current of 400mA with an 8-W power rating. Measurements verify that the converter is capable of delivering a maximum efficiency of 92% while the LEDs are being modulated via the VLC signal.

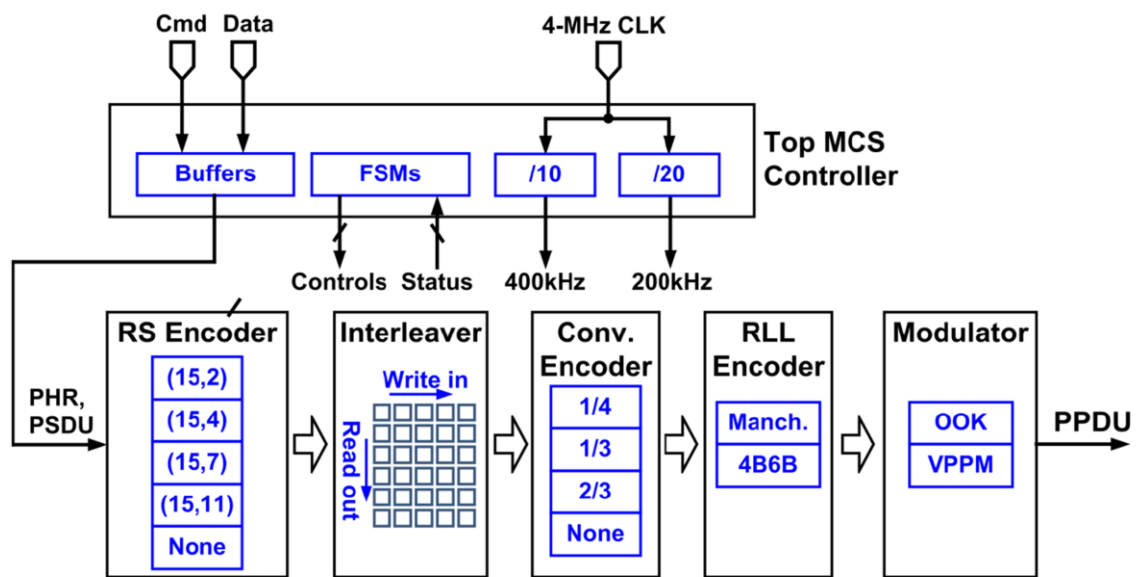


Figure 5.5 Block Diagram of IEEE 802.15.7 PHY-I Transmitter Baseband [5.3].

A VLC modulator is used to apply VLC signals to the LEDs. It consists of a fast response current pulse driver to ensure that a rise and fall time of <100ns is achieved to support the maximum modulation speed. In addition, current balancing circuitry is employed to compensate for the current variation due to the difference in turn-on voltage of the LEDs. Current balancing ensures that each branch is producing equal amounts of perceived brightness.

The digital baseband block diagram of the SoC is shown in Figure 5.5. Both the PHR, and PSDU go through a chain of signal processing blocks before being input to the VLC modulator/current pulse driver. The first three blocks serve as the ECC, where data is encoded through the RS encoder first, followed by interleaving, and thereafter encoded via the convolutional encoder. The encoded data is then fed to the RLL encoder for DC balancing before being input to the modulator for final signal shaping as either VPPM or OOK modulation. All of these processing blocks are managed by a top level MCS controller. The MCS controller, in addition to generating clocks via division, is responsible for translating input data and commands into control signals for processing blocks and keeping track via status signals from each block. The description of each processing block is provided in the following.

5.3.1 Reed Solomon (RS) Encoder

RS is a forward error correction (FEC) encoder that encodes data symbols using closed field (also called Galois field) arithmetic for parity generation. The four types of RS encoders used in the standard are listed in Table 5.4 with their respective generator polynomials $g(x)$ that determine the sequence of Galois field (GF) operations to be performed for generating the parity symbols. As specified in the standard, GF (16) arithmetic, which contains 16 symbols where each symbol is represented by a 4-bit combination, is used for RS encoding. Two types of operations namely addition and multiplication, are defined in the GF (16) and are used to generate parity symbols for the encoded data. The Reed Solomon code representation, RS (n,k), indicates the total number of symbols as 'n', and information symbols as 'k'. The remaining symbols, n-k, are the number of parity symbols which indicate the error correction capability of the encoder. The block diagram of the encoder is shown in Figure 5.6, where $M(x)$, $CK(x)$, and $C(x)$ represent the message symbols, parity check symbols, and encoded symbols, respectively.

Table 5.4 PHY-I RS Encoders and their Generator Polynomials.

(n, k)	$g(x)$
(15,11)	$x^4 + \alpha^{13}x^3 + \alpha^6x^2 + \alpha^3x + \alpha^{10}$
(15,7)	$x^8 + \alpha^{14}x^7 + \alpha^2x^6 + \alpha^4x^5 + \alpha^2x^4 + \alpha^{13}x^3 + \alpha^5x^2 + \alpha^{11}x + \alpha^6$
(15,4)	$x^{11} + \alpha^9x^{10} + \alpha^8x^9 + \alpha^4x^8 + \alpha^9x^7 + \alpha^{13}x^6 + \alpha^4x^5 + \alpha^{12}x^4 + \alpha^4x^3 + \alpha^5x^2 + \alpha^3x + \alpha^6$
(15,2)	$x^{13} + \alpha^3x^{12} + \alpha^8x^{11} + \alpha^9x^{10} + \alpha^2x^9 + \alpha^4x^8 + \alpha^{14}x^7 + \alpha^6x^6 + \alpha^{10}x^5 + \alpha^7x^4 + \alpha^{13}x^3 + \alpha^{11}x^2 + \alpha^5x + \alpha$

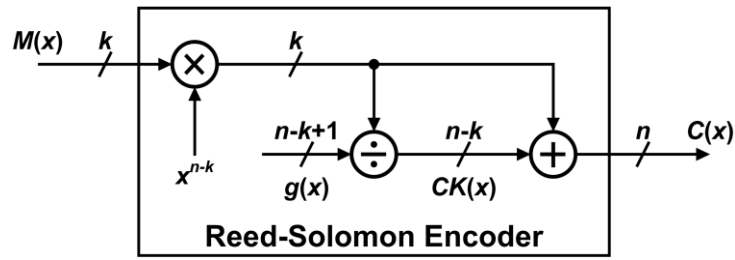


Figure 5.6 Block Diagram of RS Encoder.

5.3.2 Interleaver

An interleaver is a buffer composed of memory arrays that are used to temporarily store RS encoded symbols before reading them out in shuffled order. In other words, when RS encoded data stored in the interleaver is read out, its order is changed such that adjacent data symbols belong to different encoded packets. Thus, when a burst error occurs during the communication affecting multiple adjacent symbols, the error is evenly divided among different packets. Hence, the chance of correcting that error is maximized.

5.3.3 Convolutional Encoder

A convolutional encoder is an FEC encoder that relies on coding the information symbols by sliding a polynomial operation on a consecutive stream of bits stored in memory. The number of consecutive bits that are used in one computation is called the constraint length of the encoder. There are three types of code rate, $1/3$, $1/4$, and $2/3$, supported in the standard, and these indicate the ratio of the number of input bits to the number of output bits. All three code rates are produced via a rate- $1/3$ convolutional encoder with constraint length 7, as shown in Figure 5.7. Rate $2/3$ and $1/4$ codes can be generated by replicating and puncturing some of the output bits of the rate $1/3$ code before transmission.

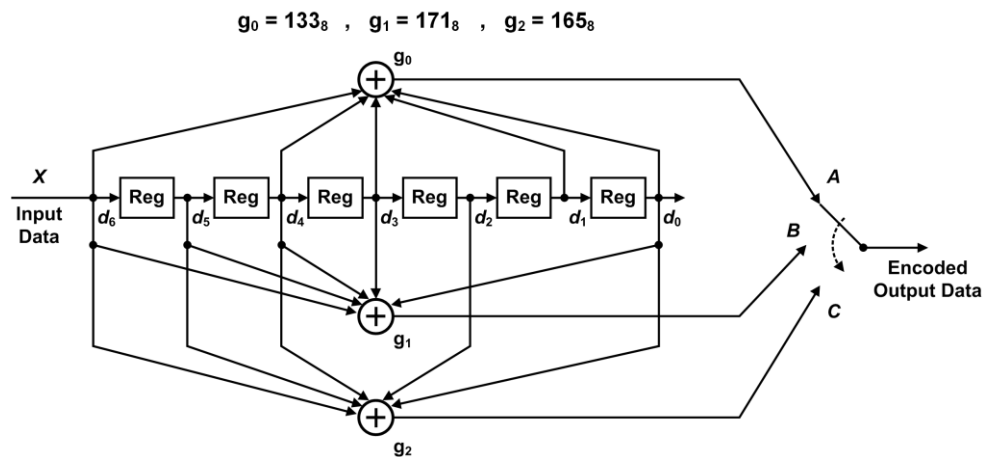


Figure 5.7 Rate 1/3 Convolutional Encoder [5.3].

5.3.4 RLL Encoder and Modulator

In addition to mitigating flicker and balancing the DC level of the LEDs, RLL encoding helps in clock data recovery at the receiver by introducing regular transitions in the data. Two types of RLL encoder, Manchester and 4B6B, which differ in terms of the overhead they inflict on the effective data rate, are employed in the standard. The Manchester encoder, which translates each input bit to either 1 to 0 transition or 0 to 1 transition, guarantees a 50% duty ratio output at the expense of reducing the data rate by half. On the other hand, 4B6B coding maps each 4-bits of incoming data to an output of a 6-bit combination, ensuring a 50% duty ratio (ratio of 1s to 0s). However, the overhead is comparatively lower, as the effective data rate is reduced by a factor of 2/3. Both the Manchester and 4B6B encoding mechanisms are illustrated in Figure 5.8.

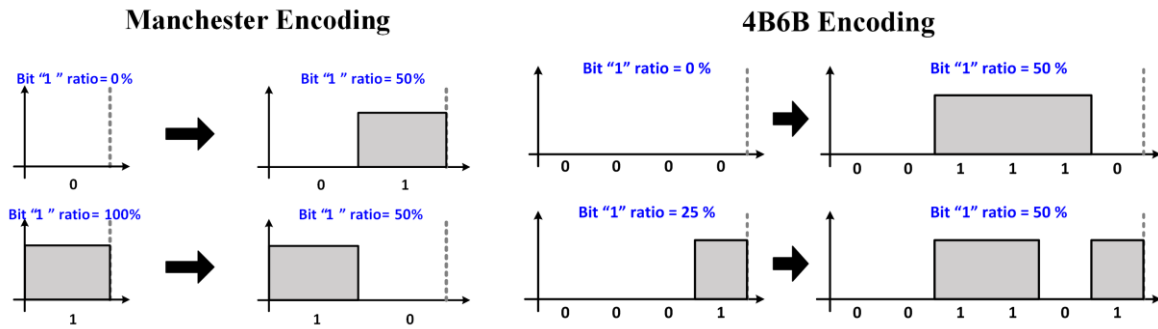


Figure 5.8 RLL Encoding Operation.

The modulator block modulates the RLL encoded data to either OOK or VPPM modulation. OOK is a simple translation of logic 1 to a high voltage level and logic 0 to a low voltage level. On the other hand, in VPPM, the data is modulated by sending a pulse at either the start of the symbol period or at the end of symbol period, i.e. to either the left or right, and hence, it is called a variable pulse position modulation. In addition, VPPM allows the direct control of LED brightness by changing the pulse width of the modulated data, as shown in Figure 5.9.

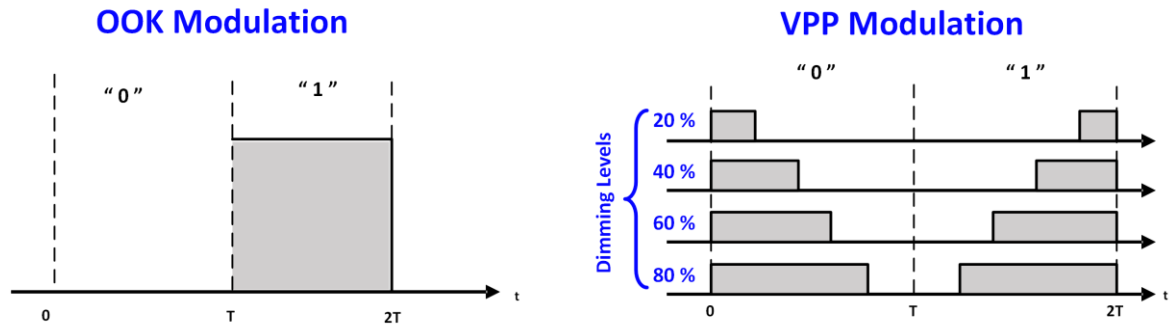


Figure 5.9 PHY-I Modulation Schemes.

5.4 IEEE 802.15.7 PHY-I Compliant Receiver Design

The receiver front end is designed using the same circuit as was used for the discrete transceiver system described in chapter 4. However, considering the bandwidth requirement is relaxed in this design, the TIA gain is increased to 114 dB. The gain-bandwidth simulation is shown in Figure 5.10.

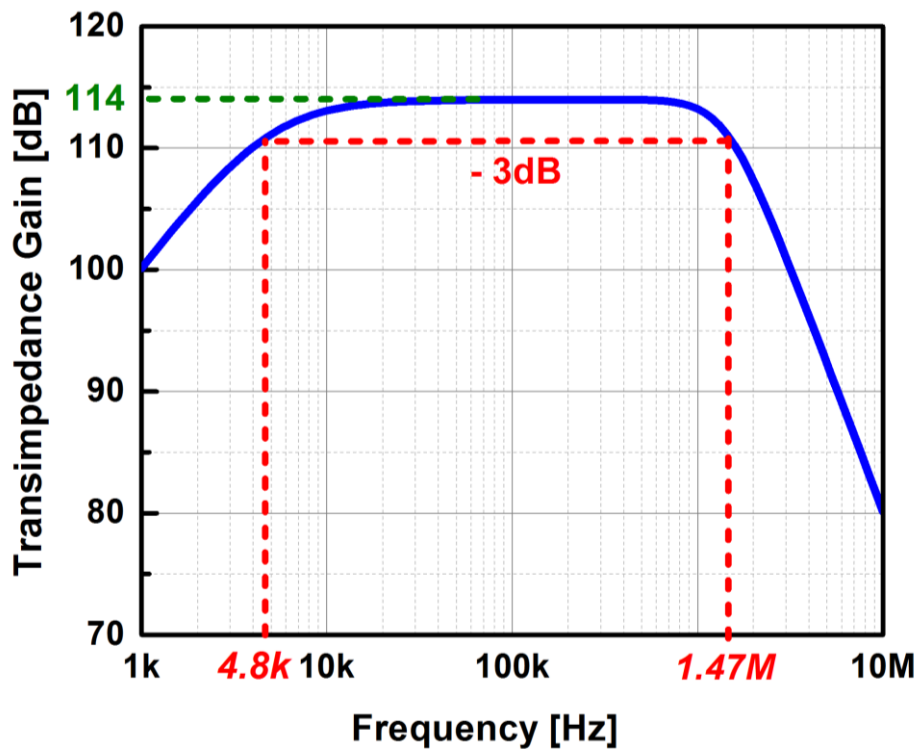


Figure 5.10 Frequency Response of Receiver Front-end.

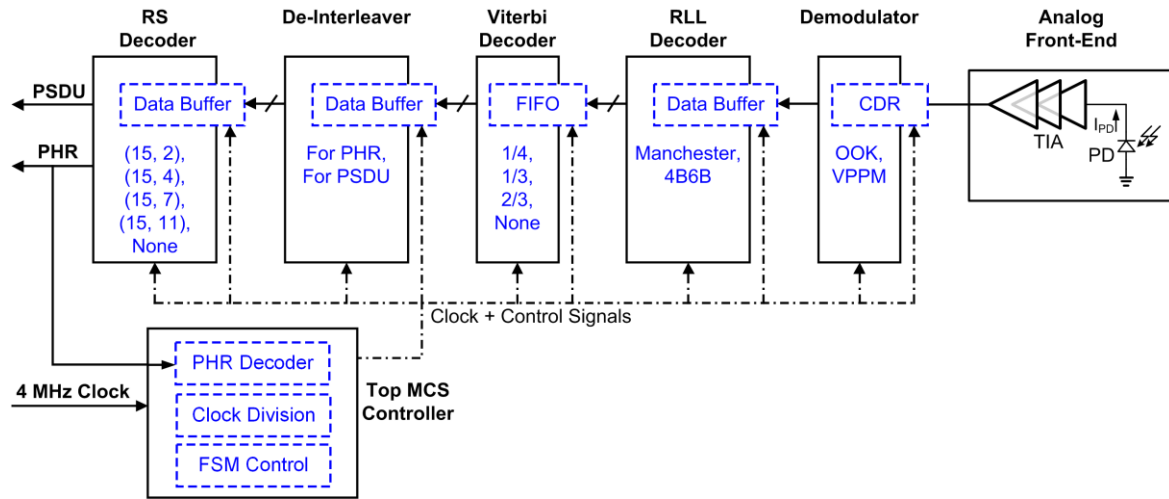


Figure 5.11 Block Diagram of IEEE 802.15.7 PHY-I Receiver Baseband.

The block diagram of the IEEE 802.15.7 PHY-I compliant receiver is shown in Figure 5.11. In correspondence to the transmitter, the receiver baseband consists of the analogous blocks in the reverse order. The received signal from the VLC front-end is first demodulated and RLL decoded before being input to the FEC chain, which consists of a Viterbi decoder, followed by a de-interleaver and and RS decoder. In addition, the control signal generation and clock management is handled by the top MCS controller. Each block is described in detail in the following sections.

5.4.1 Demodulator

The demodulator mainly consists of a CDR that works on the principle described earlier in Figure 4.17. However, in order to demodulate both OOK and VPPM, which run at clock rates of 200 kHz and 400 kHz, respectively, two oversampling clocks are generated at 2 MHz and 4 MHz, respectively. The clock selection is done based on the selected MCS. For decoding the VPPM, each period of recovered data is sorted to find the pulse location, while the phase of the clock is kept locked to the transmitter's clock by the CDR.

5.4.2 RLL Decoder

The RLL decoder consists of a Manchester and 4B6B decoder, which are used for the 200 kHz clock and 400 kHz clock rates, respectively. Considering the encoding mechanism, apparently, decoding requires a reverse mapping of the encoded bits back to the original input bits. However, in the case of receiving an erroneous bit, direct mapping is not possible. For instance, if a 10 is erroneously received as 11 or 00, a direct mapping does not exist. In that condition, the received bit is decoded as shown in Table 5.5 and marked as erasure. Where, erasure is a suspicious bit which could be a potential error. The erasure information can be input to the Viterbi decoder along with the detected bit to assist in the error correction process.

Table 5.5 Manchester Decoding and Erasure Signaling.

Received Bits	Decoded	Erase
01	1	0
10	0	0
00	0	1
11	1	1

Similarly, in 4B6B decoding, the reverse mapping table only covers 16 out of a total of 64 possibilities, as shown in Table 5.6. In that case, the hamming distance of the erroneously received code word is evaluated to find the closest possible match from the table. The simulation of the 4B6B decoder is shown in Figure 5.12.

Table 5.6 4B6B Decoding Table.

6B Received Symbol	4B Decoded Output
001110	0000
001101	0001
010011	0010
010110	0011
010101	0100
100011	0101
100110	0110
100101	0111
011001	1000
011010	1001

011100	1010
110001	1011
110010	1100
101001	1101
101010	1110
101100	1111

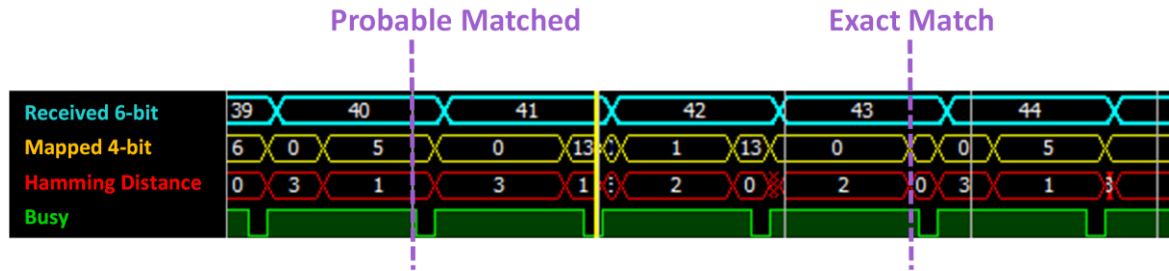


Figure 5.12 Simulation of RLL 4B6B Decoder.

5.4.3 Viterbi Decoder

The Viterbi decoder is implemented using the Xilinx IP core [5.4]. A standard type parallel architecture with reduced latency is chosen to attain a high decoding rate. The block diagram of the decoder is shown in Figure 5.13. While the PHR is being decoded, the PSDU is kept in the FIFO as the PHR carries information about the decoding and demodulation scheme to be used for the PSDU. Therefore, to reduce the depth of the FIFO and the overall decoding time of a packet, a faster architecture is chosen at the expense of larger area consumption. Also, to increase the error correction capability of the decoder, soft decision capability is enabled in the core. A summary of the IP core design parameters is provided in Table 5.7.

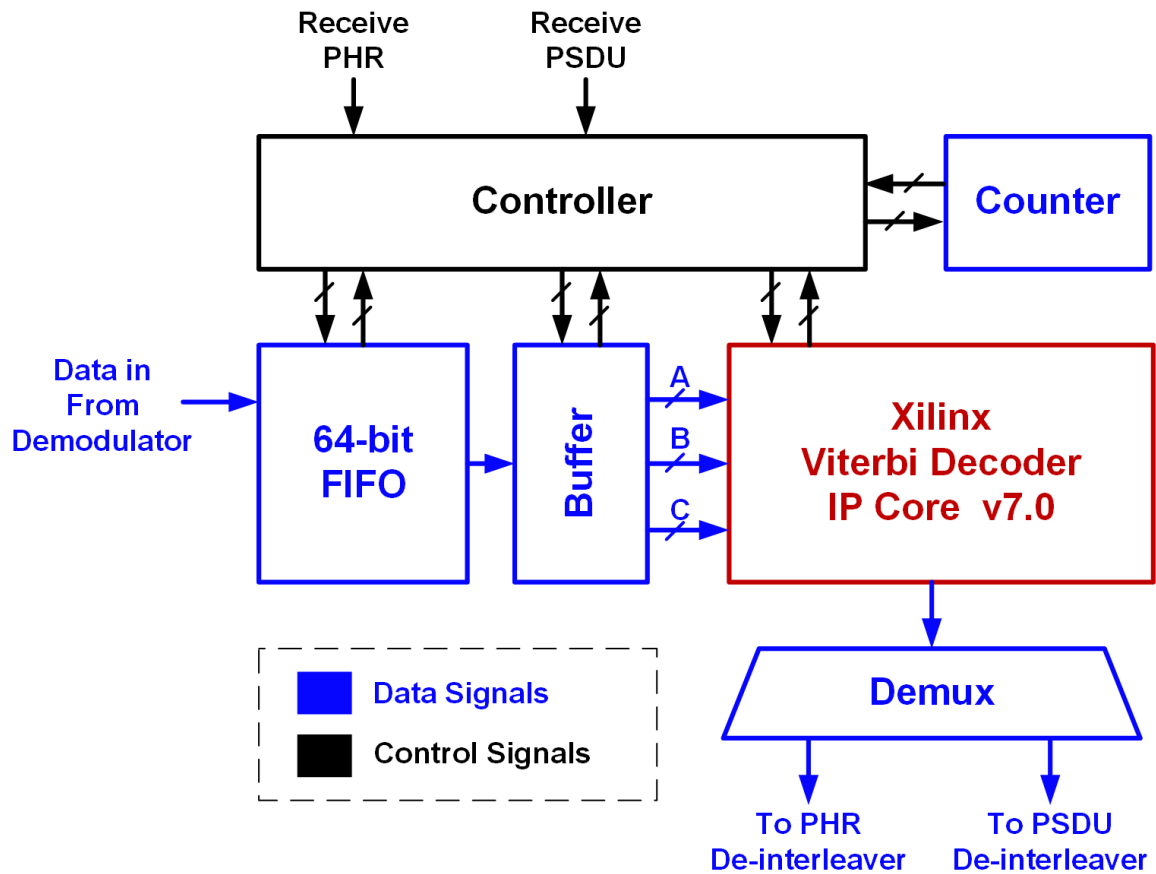


Figure 5.13 The Block Diagram of Viterbi Decoder.

Table 5.7 Design Parameters for Xilinx Viterbi IP Core.

Design Parameters	
Architecture Type	Parallel
Constraint Length	7
Traceback Length	126
Puncturing	Enabled
Output Rate	3

5.4.4 De-Interleaver

In correspondence with the transmitter, two separate de-interleavers are implemented for the PHR and PSDU. Since the de-interleaver must be compatible with the interleaver on the transmitter side, the height is fixed to be 60 bits, while the depth can be of variable size depending on the length of the PSDU and PHR used in the packet. The working principle of how the interleaver and de-interleaver can be used in burst error correction is illustrated in Figure 5.14. Each packet is composed of 15 symbols that are numbered from 1 to 15 with the last four symbols of each packet, 12 to 15, represent the parity symbols, and as such, are indicated in brown. On the de-interleaver side at the receiver, it can be observed that the error is evenly distributed thanks to the shuffled arrangement of symbols in the channel.

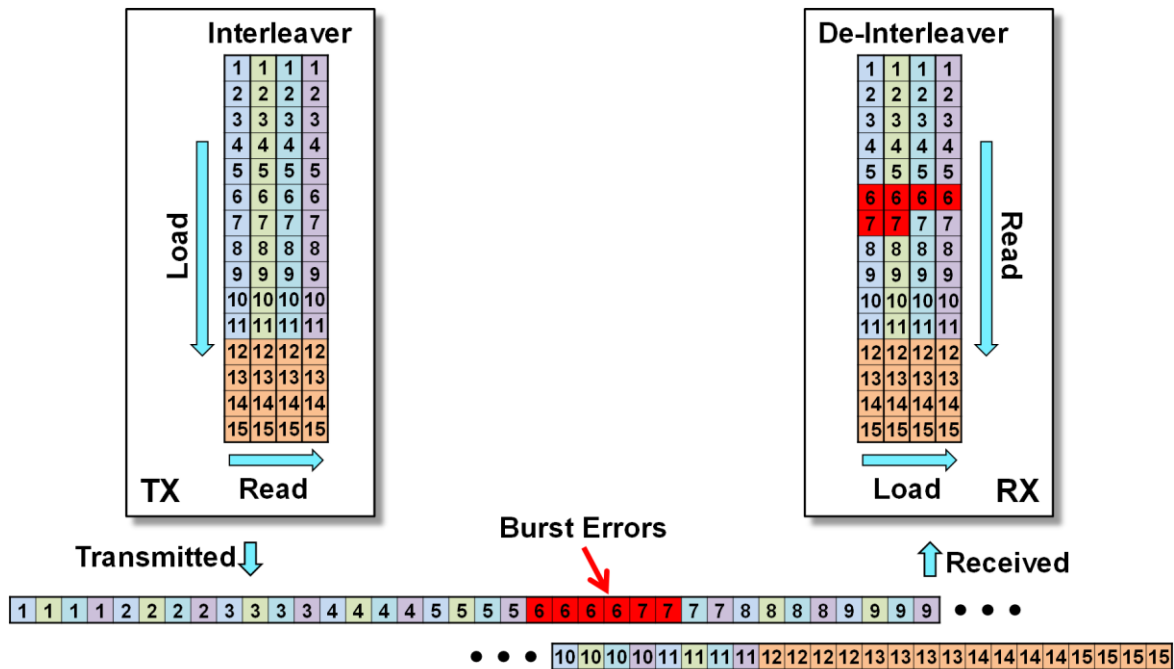


Figure 5.14 Illustration of Interleaving and De-interleaving [5.6].

5.4.5 RS Decoder

The block level architecture of the RS encoder, depicted in Figure 5.15, is based on the inverse-free Berlekamp Massey algorithm [5.5]. A large buffer stores the input data packet during the decoding stage and is finally recombined with error values to produce the corrected output. The syndrome calculator block, predominantly containing feedback adders and multipliers, begins the decoding process by producing the error syndromes. These syndromes are combined with erasures coming from the erasure generator block to produce Forney syndromes. These syndromes are used to calculate the error locator and evaluator polynomials using the Massey algorithm, which is a hardware efficient serial approach provided in [5.5]. Following that, the error locator polynomial is applied to Chien search approach which is based on feedback multiplication to find the error location. Additionally, the error evaluator polynomial is combined with the error locator polynomial using the Forney algorithm to calculate error values. Finally, the error values are combined with the stored received packet using xor to produce the final decoded output. The simulation result for the RS(15,2) decoder is shown in Figure 5.16, indicating a successful detection for various error vectors.

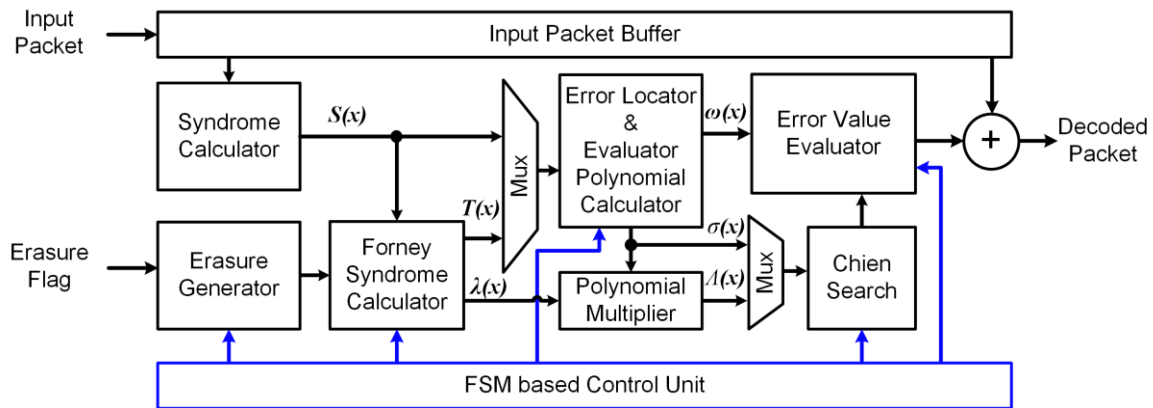


Figure 5.15 Block Diagram of RS Decoder.

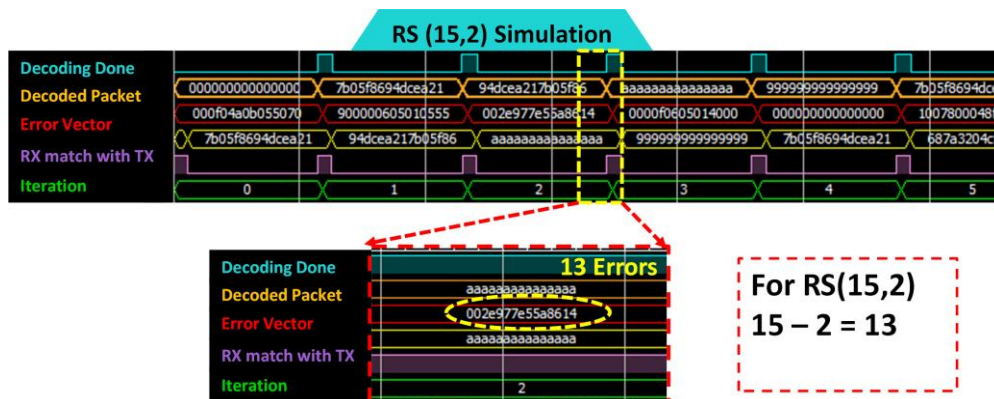


Figure 5.16 Simulation of RS(15,2) Decoder.

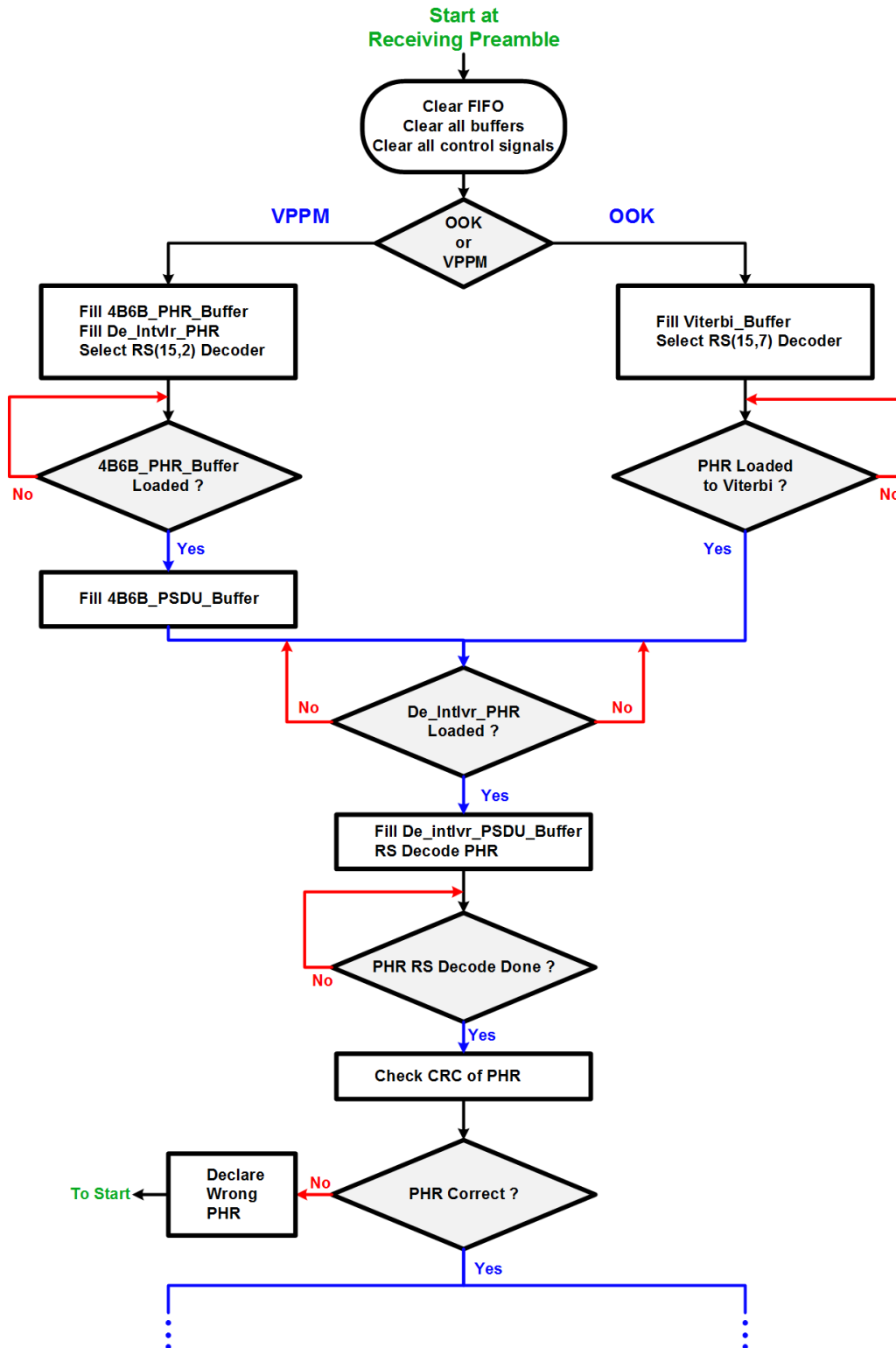


Figure 5.17 State Transition Diagram of Top Level MCS Controller Part-1.

5.4.6 Top Level MCS Controller

The top level controller is responsible for manipulating the control and status signals to manage the flow of data in the signal processing block. In addition to clock division and PHR

decoding, the controller predominantly consists of an FSM that governs the start and stop signals for each processing block. Based on the detailed description provided earlier, it is quite clear that in addition to the control signals provided by the FSM, each processing block, e.g. the RS decoder, Viterbi decoder etc., has its own local controller that monitors the filling of data buffers and FIFOs etc. These local controllers require only start signals to start processing and update their status to the main controller once the decoding is done. The state transition diagram for the top level MCS controller is illustrated in Figure 5.17 and Figure 5.18.

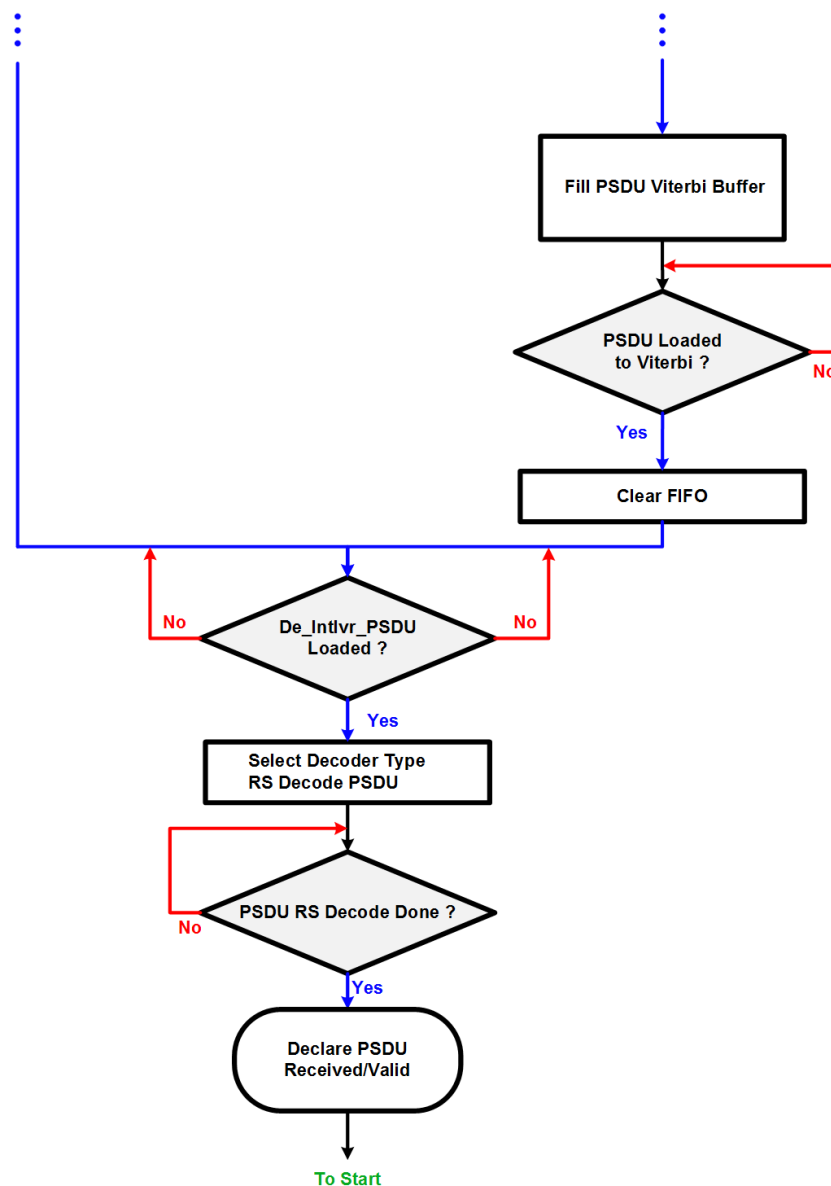


Figure 5.18 State Transition Diagram of Top Level MCS Controller Part-2.

5.4.7 FPGA Implementation Summary

The receiver baseband is implemented in a Xilinx Virtex-5 FPGA. The resource utilization is summarized in Table 5.8.

Table 5.8 FPGA Resource Utilization Summary.

FPGA Resource	Used	%
Slice Registers	8640	12
Slice LUTs	12989	18
Bonded IOBs	29	4
Block RAMs	133	89

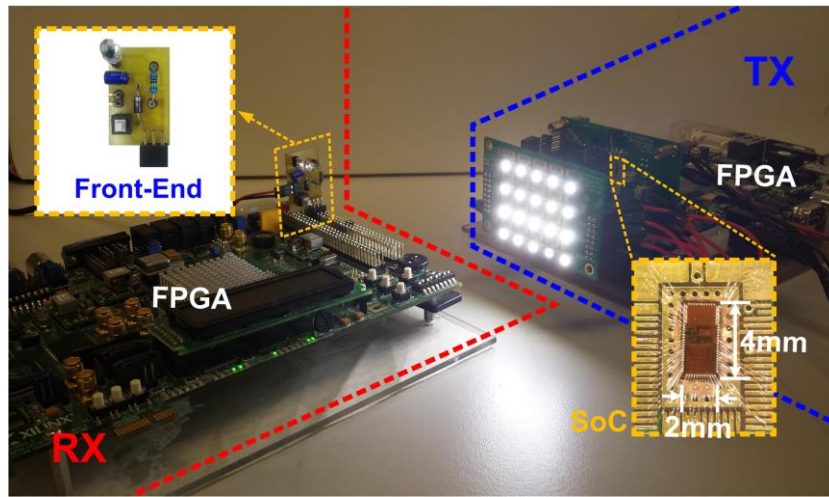


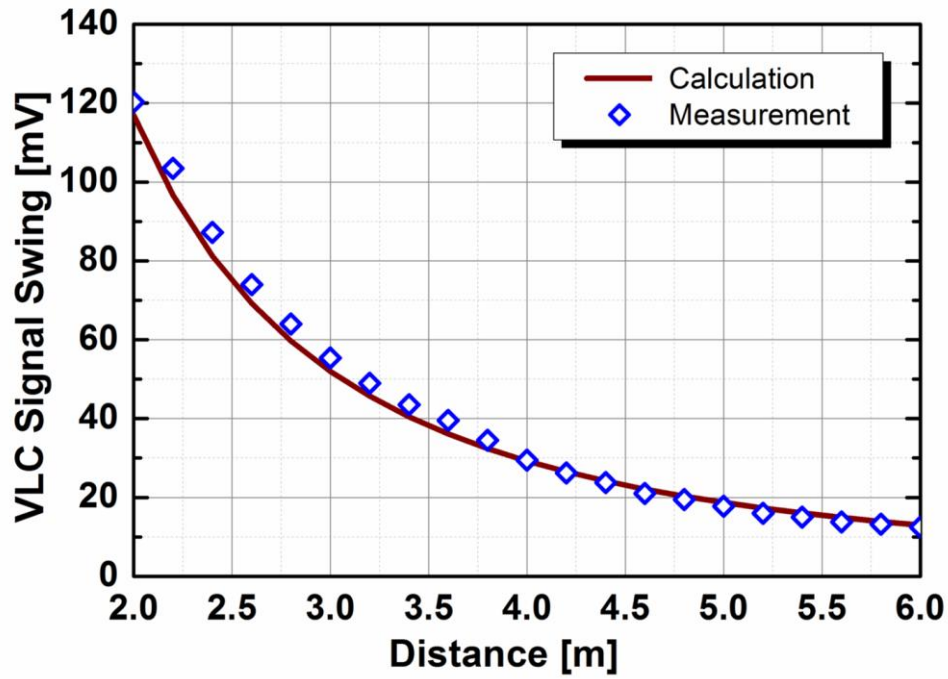
Figure 5.19 Hardware Measurement Setup for IEEE 802.15.7 Compliant Transceiver.

5.5 Hardware Measurements

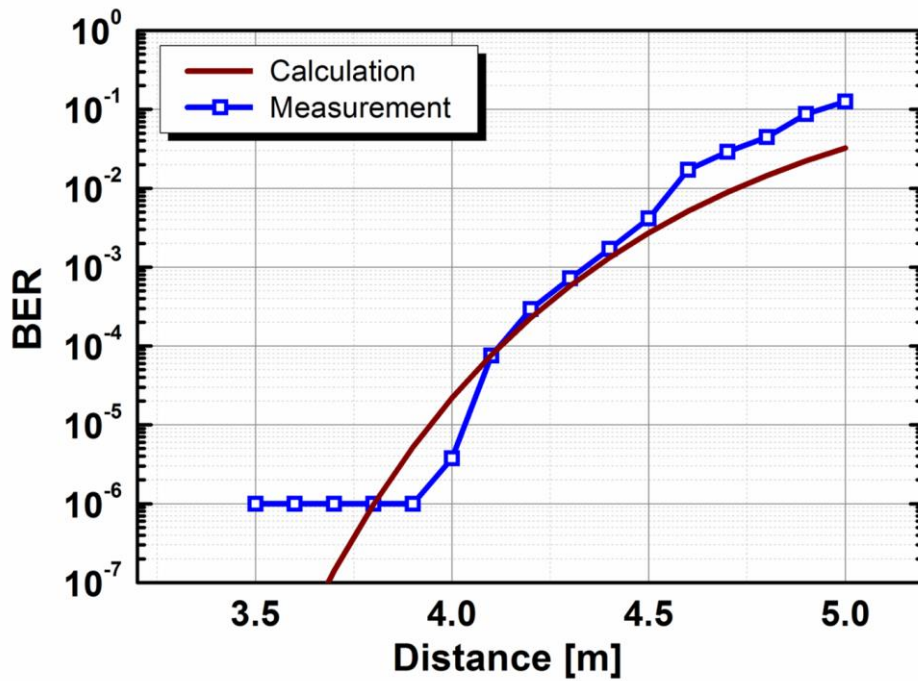
At the transmit side, the LED array is measured to consume a 100-mA current on average from a 14.4-V voltage output, which is converted from a Li-ion battery by the LED driver. Following the link budget analysis presented in chapter 3, an implementation loss of ~ 1 dB is incorporated. This is significantly lower than that of the previous discrete system design because the transmitter circuits implemented in the SoC have much tighter control and lower tolerance. This also highlights the advantage of integration for future VLC systems.

Figure 5.19 illustrates the hardware and the measurement setup. Again, both the calculated and the measured signal swing at various distances are plotted together, as shown Figure 5.20 (a). In addition, the BER curves from both the calculation and the measurement are shown in Figure 5.20 (b). The results verify the accuracy of the link budget analysis.

Furthermore, the measured BER performance indicates that the system achieves a BER of 10^{-6} up to a distance of 3.9 m, which exceeds the required specifications.



(a)



(b)

Figure 5.20 Measurement Results of the IEEE 802.15.7 VLC System: (a) VLC Signal Swing and (b) BER.

References

- [5.1] "IEEE Standard for Local and Metropolitan Area Networks--Part 15.7: Short-Range Wireless Optical Communication Using Visible Light," *IEEE Std 802.15.7-2011*, pp. 1-309, 2011.
- [5.2] B. Hussain, F. Che, et al., "A fully integrated IEEE 802.15.7 visible light communication transmitter with on-chip 8-W 85% efficiency boost LED driver," *IEEE Symposium on VLSI Circuits*, Jun. 2015, pp. 216-217.
- [5.3] F. Che, B. Hussain, X. Li, L. Wu, C. P. Yue, "A fully integrated IEEE 802.15.7 visible light communication transmitter," submitted to *Journal of Solid State Circuits (JSSCC)*
- [5.4] Xilinx LogiCORE IP Viterbi Decoder v7.0 User Guide. [Online]
Available:http://www.xilinx.com/support/documentation/ip_documentation/viterbi_ds247.pdf.
- [5.5] J. H. Jeng and T. K. Truong, "On decoding of both errors and erasures of a Reed-Solomon code using an inverse-free Berlekamp-Massey algorithm," *IEEE Trans. Commun.*, vol. 47, pp. 1488-1494, 1999.
- [5.6] F. Che, "VLC transceiver system design using LED for IEEE 802.15.7 standard," MPhil Dissertation, Hong Kong University of Science and Technology, Hong Kong, 2015.

CHAPTER 6 VISIBLE LIGHT INDOOR POSITIONING SYSTEM

6.1 Introduction and Motivation for Indoor Positioning Using Visible Light

Indoor positioning has been extensively researched and investigated due to its high value in robotics navigation and tracking and the impact it can have on providing useful indoor location based services to people. Due to the limitations of GPS (Global Positioning System) in indoor environments, several other means for indoor positioning using various techniques have been investigated, for instance, RFID, Wi-Fi, Bluetooth etc. [6.1]. However, with radio signal attenuation and interference in indoor environments, these systems cannot achieve a satisfactory level of accuracy and precision. In addition, some of these techniques, e.g. RFID, have compatibility issues with consumer electronic devices and, therefore, are hard to integrate into existing systems.

Owing to its low-cost integration in existing infrastructure and immunity to RF interference, VLC can be used for low-cost high precision indoor localization. In particular, its license free large bandwidth spectrum enables it to be used in sensitive environments, e.g. hospitals, airplanes etc. In a typical VLIP system, the location information is broadcasted via a set of LEDs, with each LED transmitting a unique signal for location identification. On the receiver side, a dedicated image sensor or photodiode based receiver is used to receive the signal. The location is estimated via comparison of the relative strength of the signal coming from each LED.

A number of VLIP systems have been investigated in recent years [6.2]-[6.3]. In [6.2] the experimental design of a VLIP system employing an LED lamp and a mobile device based receiver was presented. However, despite being low-cost, the large size of the VLC receiver made the system impractical. In [6.3], a VLIP system using a colored LED and image sensor was demonstrated. Although the system achieved a good accuracy, the use of complex image sensor based receiver and colored LEDs as the transmitter made the system high cost and impractical to be considered for commercial applications.

In this chapter, the design of a low-cost indoor VLIP system is demonstrated to address the aforementioned issues by employing a set of smart LED light tubes as transmitters or location beacons, while the receiver is implemented via a small sized low-cost photodetector based receiver and smartphone camera [6.4]. The system along with a detailed description of each building block is presented in the following sections.

6.2 Visible Light Indoor Positioning Systems

6.2.1 Architecture

The VLIP system consists of LED light tubes as smart LED transmitters. These light tubes are equipped with a VLC modulator and LED driver, which are controllable via a built-in Wi-Fi module. The signal is received in a smart phone via either its camera or with the help of an externally connected photodetector based receiver. The received signal after being decoded is sent to a server for the position estimation. The server is used for handling the positioning calculations since a large size database requiring complex computations cannot be managed by the smartphone alone. The block diagram of this system's architecture is illustrated in Figure 6.1.

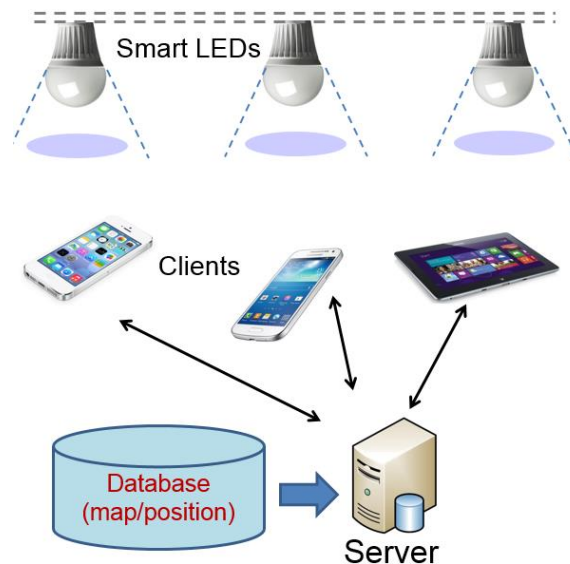


Figure 6.1 Block Diagram of the Architecture of the VLIP System.

The system is implemented using smart LED light tubes which are compatible with fluorescent light tube fixtures. The use of a smart phone as receiver and the effortless deployment of smart LED light tubes, make the system implementation low-cost and practical. In addition, the system is shown to achieve a high accuracy of $< 1\text{m}$.

In the following sections, various building blocks of the VLIP system are discussed in depth.

6.2.2 Smart LED Light Tubes as VLC Transmitters

The smart LED light tubes have been designed such that VLC capability can be achieved while maintaining compatibility with existing lighting fixtures for easy deployment. The smart LED light tube is therefore similar in size to a conventional fluorescent light tube and has similar input AC supply requirements and connections, as shown in Figure 6.2. Each LED light tube consists of a strip of 40 commercial white LEDs that are driven by an LED driver packed inside the tube. In addition, for easy programmability, a Wi-Fi module is also included which enables control of the VLC function via a smartphone using a dedicated app. The Wi-Fi module is interfaced to a microcontroller which controls the LED driver for VLC modulation according to the desired frequency and signal pattern/code. Figure 6.3 illustrates the block diagram of the light tube control module being controlled via Wi-Fi using a dedicated Android application on a smartphone.

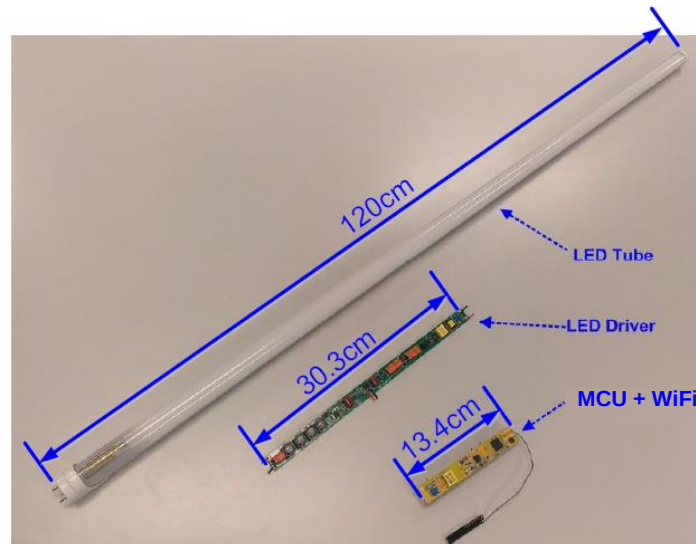


Figure 6.2 Smart LED Light Tube with Driver, MCU and Wi-Fi Unit.

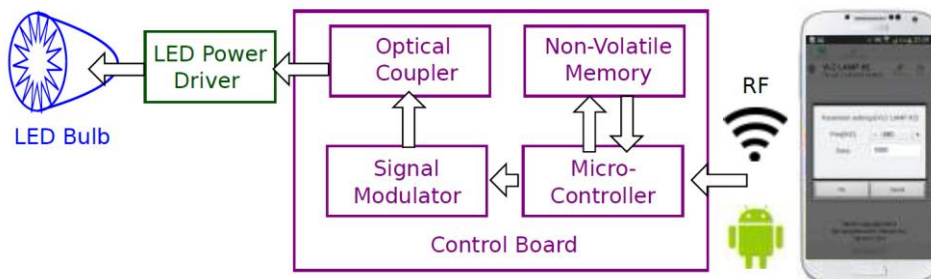


Figure 6.3 Block Diagram of the Smart LED Light Tube Controller [4].

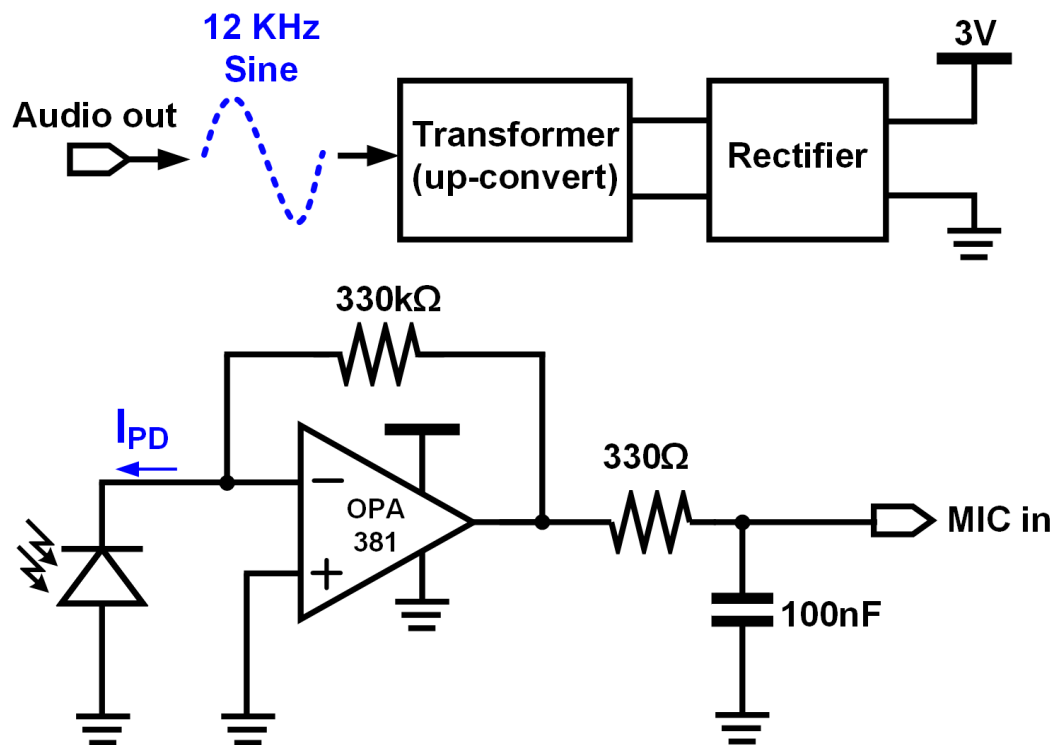


Figure 6.4 Schematic of Photodetector based VLC Receiver.

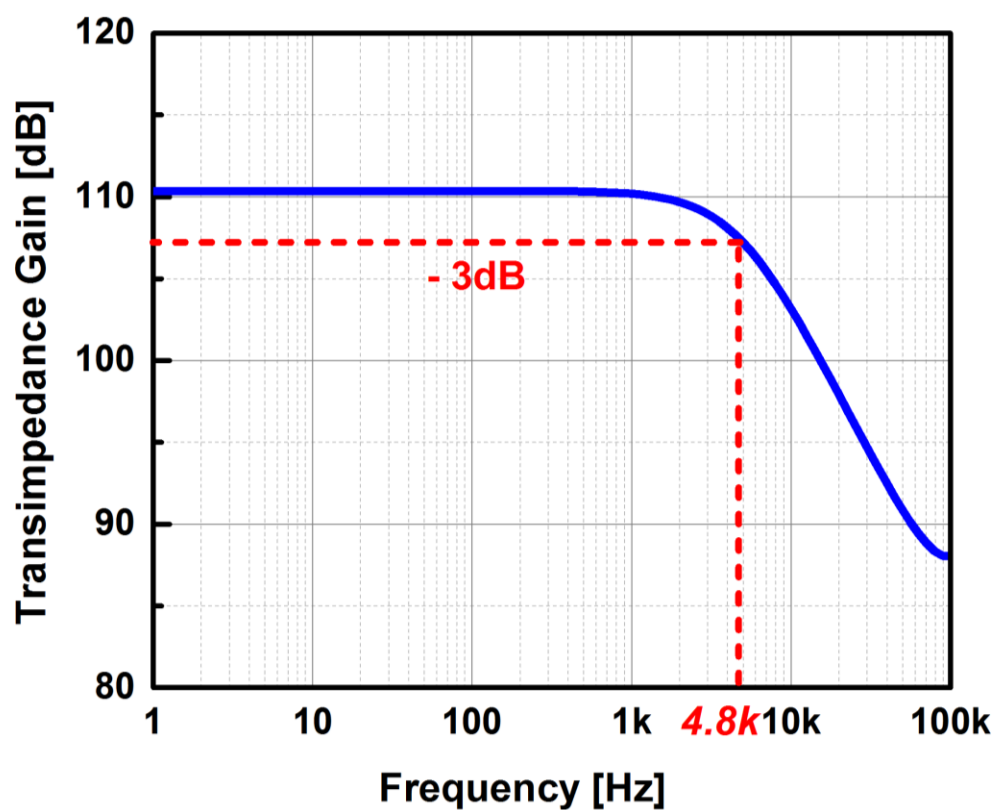


Figure 6.5 Frequency Response of the Photodetector-based VLC Receiver.

6.2.3 Photodetector Board as VLC Receiver

The photodetector based receiver is the first of the two types of receivers that can be used in a smartphone for sensing of positioning information transmitted via light tubes. The receiver is an external photodiode and transimpedance amplifier based circuit that is preferable in comparison to the smart phone camera (discussed in the following section) when a higher detection range and sensitivity is desired. The receiver is connected via the microphone input of the smartphone through a 3.5mm connector. In addition, a smaller size is realized by using on-board power harvesting circuitry which generates power from an audio signal played in the background and delivered to the board via the same 3.5 mm connector.

The schematic of the receiver is shown in Figure 6.4. The photodiode is modeled via a current source with a very high impedance of $1\text{ G}\Omega$ and a diode capacitance of 11 pF . The transimpedance gain, which is determined via the feedback resistor R_f , is chosen to be $\sim 110\text{ dB}$. In addition a low pass filter is used to roll-off the high frequency response with a 3-dB cutoff of 4.8 kHz in order to reduce the noise contribution from higher frequencies. The operating frequency of the VLIP system is 1 kHz , which is well below the cut-off point, as shown in the frequency response simulation of the circuit in Figure 6.5. The power generation block consists of a transformer, a rectifier and a filter capacitor. A 12 kHz sinusoidal signal is fed to this block via the audio output of the smartphone. This signal is up-converted via a transformer before being fed to the rectifier. The rectified signal is filtered via a large capacitor and is used as the supply voltage for the transimpedance amplifier. Figure 6.6 shows the photodetector-based receiver board connected to the smartphone, with the VLC signals waveform being recorded on the smartphone screen via the Audio Analyzer application. The board is sensitive enough to detect a VLC signal in the range of about 10 meters.

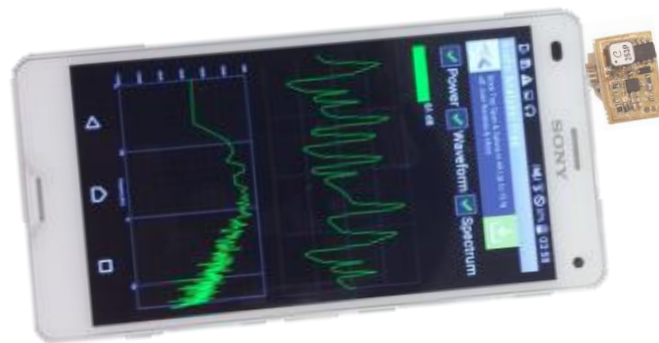


Figure 6.6 Photodetector Board Connected to the Smartphone.

6.2.4 Smartphone Camera as VLC Receiver

The readout circuit of the smartphone camera stores an image by sequentially capturing each row of pixels. This method of image capturing, which is called rolling shutter, is responsible for the detection of the modulation of LED lights. As shown in Figure 6.7, if the turn on and off times of the LEDs are comparable to the speed of the rolling shutter, the image contains a pattern of dark and bright regions, which can be processed to decode the VLC signal. The width of these dark and bright stripes can be controlled by setting an appropriate frequency. Typically, it is possible to observe a discernable pattern up to a frequency of 5kHz.

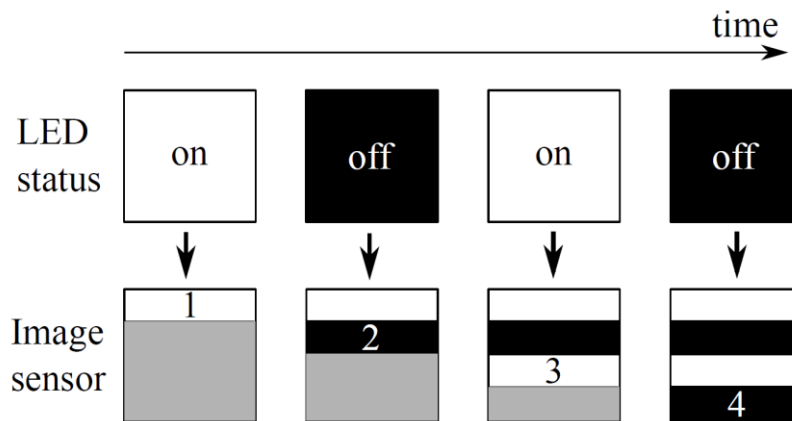


Figure 6.7 Rolling Shutter Effect of Smartphone Camera [6.4].

The image processing algorithm to decode such patterns consists of the following steps [6.4]:

- 1) The image is captured using minimum exposure compensation.
- 2) The image is preprocessed by performing gray-scale conversion followed by Gaussian blur, as illustrated in Figure 6.8 (b).
- 3) The preprocessed image is histogram equalized to enhance the contrast of the image, as illustrated in Figure 6.8 (c)
- 4) The pixel values are summed along each column to obtain the curves as in Figure 6.8 (d).
- 5) Maximum and minimum values are located on the curve and a decision threshold line is obtained. This line divides the sections in 0s and 1s, as depicted in Figure 6.8 (d).
- 6) The minimum width of consecutive 1s and 0s is detected to find the width of the stripes, which leads to the decoding of the entire pattern.

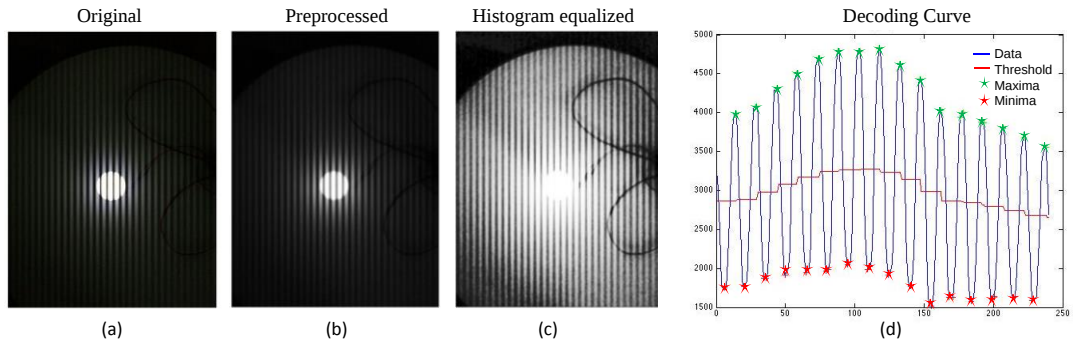


Figure 6.8 Illustration of VLC Decoding Algorithm Using Smartphone Camera.

Due to variations in the lighting conditions and non-uniform background, the signal detection via smartphone camera has limited range and performance in comparison to the dedicated photodetector based receiver presented earlier.

References

- [6.1] H. Liu, H. Darabi, P. Banerjee, and J. Liu, “Survey of wireless indoor positioning techniques and systems,” *Systems, Man, and Cybernetics, Part C: Applications and Reviews, IEEE Transactions on*, vol. 37, no. 6, pp. 1067–1080, Nov. 2007
- [6.2] G. del Campo-Jimenez, J. M. Perandones, and F. Lopez-Hernandez, “A VLC-based beacon location system for mobile applications,” in *Localization and GNSS (ICL-GNSS), 2013 International Conference on. IEEE*, 2013, pp. 1–4.
- [6.3] T. Tanaka and S. Haruyama, “New position detection method using image sensor and visible light leds,” in *Machine Vision, 2009. ICMV’09. Second International Conference on. IEEE*, 2009, pp. 150–153.
- [6.4] M. Liu, K. J. Qiu, S. Li, F. Che, B. Hussain, L. Wu, and C. P. Yue, “Towards indoor localization using visible light communication for consumer electronic devices,” in *Intelligent Robots and Systems (IROS), 2014 IEEE/RSJ International Conference on*, 2014.

CHAPTER 7 CONCLUSION

Recent research into visible light communication transceivers has been focused on functional demonstration with little to no consideration of the importance of design analysis and optimization to achieve efficient performance by utilizing available resources for developing practical systems for target applications.

This work has presented, for the first time, a systematic approach to visible light communication (VLC) transceiver design based on an analytical optical wireless link budget study. To obtain the signal-to-noise ratio (SNR) at the receiver, the received signal power is predicted by modeling the transmitted optical power and the channel path loss, while the input-referred noise is estimated by characterizing the noise contribution from each of the receiver building blocks.

Based on the design specifications, for instance, targeted bit error rate (BER), data-rate and communication distance, two VLC transceiver systems have been designed and demonstrated. Their performance is verified by comparing the measurement results with target specifications.

One system is designed and demonstrated using discrete components and FPGA as baseband, while the other system uses a fully integrated CMOS VLC transmitter compliant with the IEEE 802.15.7 standard. Both the designs have been tested and their performance verified. Experimental results show that the measured BER agrees well with the proposed model for both systems, validating our design approach and the link budget analysis.

APPENDIX A Using LightSay Smartphone Application to Decode VLC Signals

In order to decode a VLC signal using smartphone camera, the application requires us to store the detection sequence in the internal database of the application i.e. the *application cannot detect an unknown sequence*. A default library of predefined codes already exists in the application which can be deleted or modified. In addition to setting up a database, the user is required to set the *code length* and *hamming distance* separately in the application settings. Whereas, their default values are 12 and 6 respectively.

The steps to run a basic demo using the application are provided in the following.

1. Set up the light frequency and VLC modulation code/pattern using LightSay application
2. Set up the database in the Decoder section of the application.
3. Modify settings of the Decoder application
4. Use the Decoder application to detect the VLC signal

1. Setting up the Light Tube

Each light tube has a built-in Wifi module, which a user can connect to via a smartphone to program the modulation frequency and transmission sequence/pattern of the VLC signal. Each light tubes has a unique SSID which is marked on one end of the light tube as shown in Figure A.1.

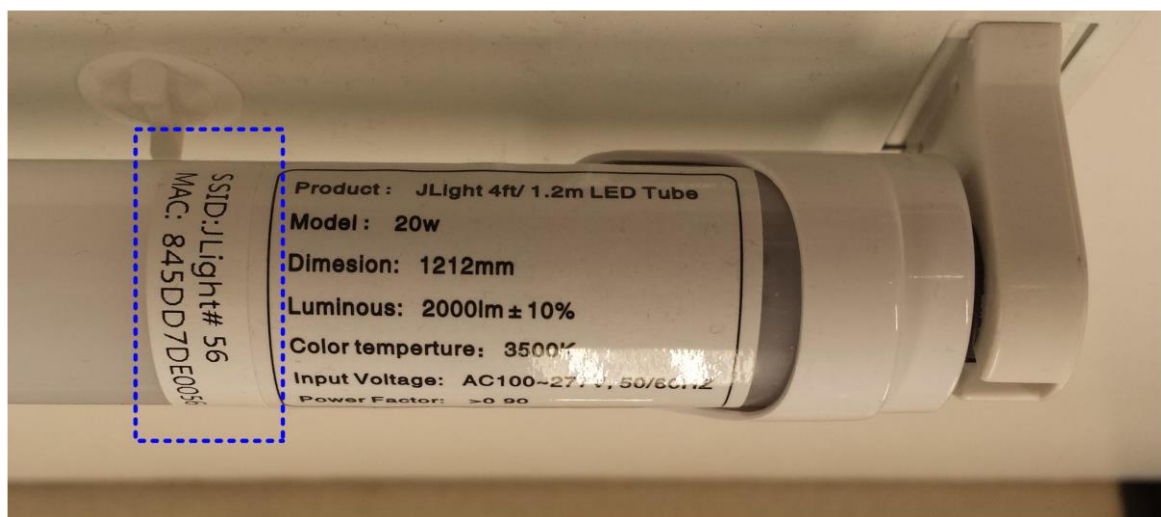


Figure A.1 Finding the SSID of the light Tube.

The user needs to connect to this network using the smart phone which has the LightSay application installed on it. Once connected to this network, the user is supposed to run the Jlight application. The interface on the application would look like as shown in Fig. A.2 (a).

Clicking the Edit button would reveal the settings for that particular light tube. The settings, as shown in Fig. A.2 (b), contain the VLC modulation frequency and VLC Data pattern input. *The frequency is recommended to be kept within ~2000Hz to ~ 800Hz*, as the current version of the VLC decoding application only works for this range. In addition, since the default settings for hamming distance and code length are 6 and 12 respectively, the VLC Data pattern used for programming here is of fixed 12 bit length with a total number of 1's (hamming distance) in the pattern being exactly 6. The pattern chosen for the demo is: 101010101010 which is exactly 12-digits in length and contains 6 number of 1's.

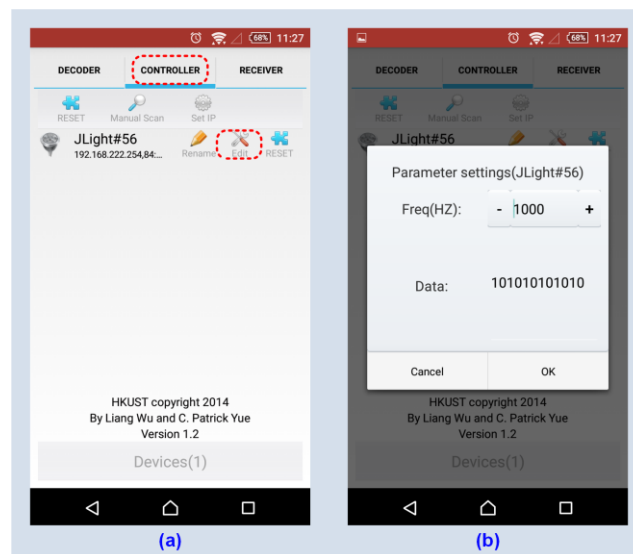


Figure A.2 (a) Controller Application Interface (b) Setting Modulation Frequency and Bit Pattern.

2. Setting Database in VLC Decode Application

After running the VLC Decode application, touching at the bottom right corner of the application (Figure A.3 (a)) reveals the selection menu, from which the 'Code' menu is selected. This menu reveals a window, as shown in Fig. A.3 (b) containing a list of currently stored codes in the database which the application is supposed to detect. As shown in Fig. A.3 (a), a code with a title 'Home' is being saved in the database. This input title can be any text which suits users naming convention. The 'Input code' box is filled with the code to be detected, which in this case is the same as was set up in the Controller section of the application. The 'Input Link' box requires us to fill in a web address which will open once a code is successfully detected.

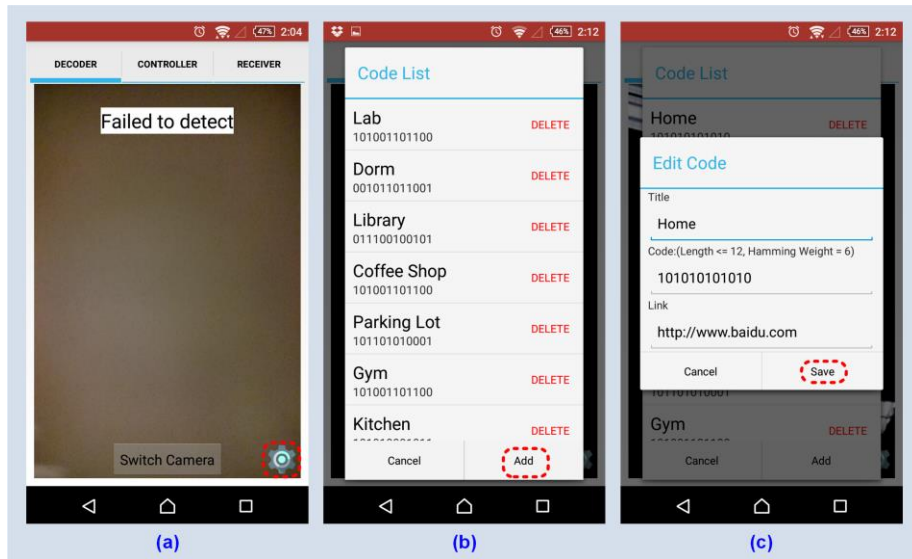


Figure A.3 Setting up the Database for the Decoder.

3. Modify Settings of VLC Decode

In addition to setting up a database, the user is supposed to select two important properties of the code i.e. hamming distance & code length, which are necessary for decoding algorithm. These settings can be modified as shown in the Figure A.4. However, it should be noted that changing these settings would mean that the application will not detect those bit patterns which do not match these specifications of code length and hamming weight, even though they are stored in the code library.

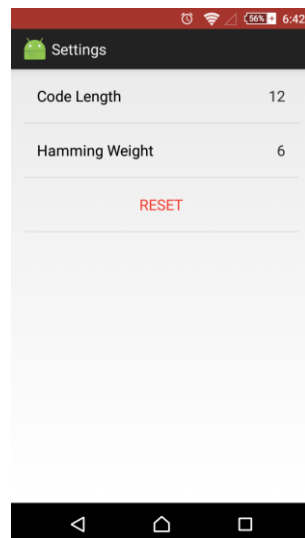


Figure A.4 Modifying Settings for Hamming Weight and Code length.

4. Detecting the VLC signal

The VLC signal is detected automatically as shown in the Figure A.5. However, the user has the option to select either the front or back camera for decoding. During the detection, the

application will show the live image from the camera. Now, as shown in Fig. A.5, if the camera is directed towards the light tube, a continuous photo-shutter pattern could be observed over the image. Once the code is successfully detected, it will appear on the screen displaying the code and its title, as is stored in the database.



Figure A.5 Detecting the VLC Signal.