High-Frequency CMOS Transmitter Circuits for Wireless and Optical Communication

by

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This is to certify that I have examined the above PhD thesis
and have found that it is complete and satisfactory in all respects,
and that any and all revisions required by
the thesis examination committee have been made.

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To my parents and my sister

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Abstract

Wireless and optical communications are promising technologies that can elevate data transfer capabilities in terms of speed and application scenarios. Wireless communication offers increased data rates and extended communication distances through the utilization of high carrier frequencies and large phased array systems in mobile communication. On the other hand, optical communication stands out for its energy efficiency, attributed to its high bandwidth and minimal signal loss. This thesis focuses on the transmitter (TX) designs, focusing on both architectural aspects and front-end circuits with enhanced signal strength and quality. This research aims to pave the way for the hybrid of wireless and optical communication.

In the first section, the Integrated System Evaluation Engine (ISEE) developed by our group is introduced. Based on MATLAB, Advanced Design System, and Cadence simulators, ISEE evaluates system performance using high-order complex modulation schemes, offering valuable design insights for circuit development. To demonstrate ISEE, a 28 GHz direct-conversion transceiver front-end system is designed and simulated using orthogonal frequency division multiplex signals with sub-carriers modulated by quadrature amplitude modulation scheme.

In the second section, a Ka-band 4-element TX in 40-nm CMOS technology, along with a co-optimized wideband chip-antenna interface for phased-array systems are presented. By employing the sliding intermediate-frequency (IF) architecture and a multiplex-and-interpolation-based IF local-oscillator (IFLO) phase shifter, the TX attains an outstanding RMS phase error

of 0.63° 0.85°, with a minimal RMS PS-induced gain error of 0.02∼0.05 dB. The proposed two-stage power amplifier reaches 18.5 dBm P1dB, 30.3% peak drain efficiency, and a power density of 1.0 W/mm² through gain peaking in the first stage and a high coupling coefficient transformer. Consequently, the phased-array TX demonstrates a leading area efficiency of 0.26 mm² per element and a peak power efficiency of 24.1%. A 2-stub matching network is introduced as the chip-antenna interface, achieving a bandwidth of 11.4 GHz.

The final section proposes a 56 Gbps PAM-4 TX for optical communication. To reduce electromagnetic interference, a common-mode (CM) filter is proposed to suppress the CM noise. Based on the delay equalizer structure, this filter provides the benefit of maintaining constant differential-mode resistance across the entire spectrum, ensuring effective matching between the off-chip transmission line and the on-chip circuit. Simulation results demonstrate an 18.85 dB reduction in CM noise while preserving the integrity of the differential-mode signal.

CHAPTER 1

INTRODUCTION

1.1 Research Background

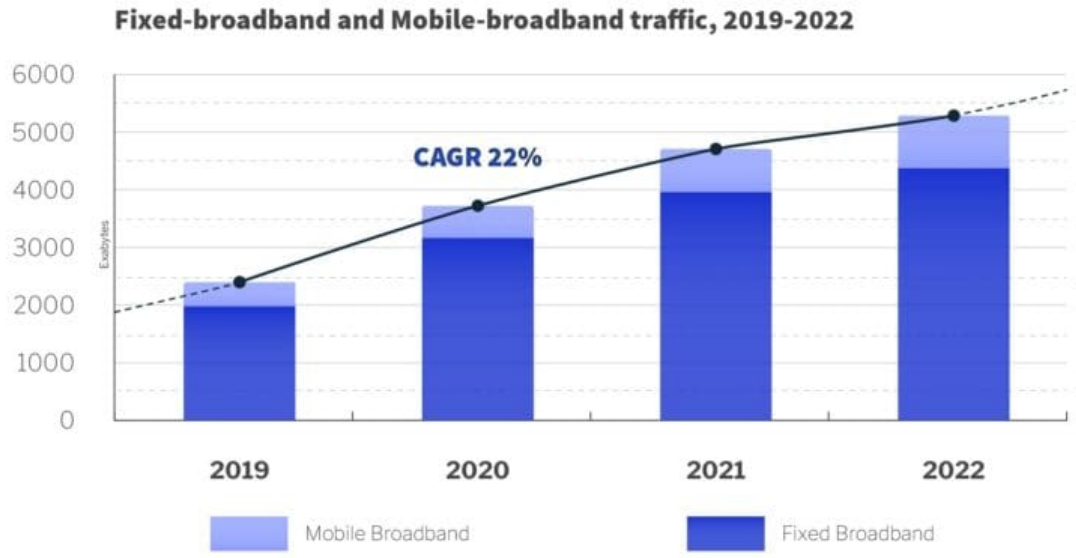


Figure 1.1: Fixed-broadband and Mobile-broadband traffic from 2019-2022 [1, 2].

The rapid expansion of mobile internet usage, multimedia streaming, and cloud computing has significantly intensified the demand for high-speed data communication. According to ITU data, global internet traffic has experienced an average annual growth rate of 22%, rising from 2,401 exabytes in 2019 to 5,291 exabytes in 2022. This trend is illustrated in Figure 1.1. Furthermore, mobile data traffic is projected to triple by 2030, driven by an influx of users in developing countries and substantial increases in consumption among existing users. This dramatic escalation in data transmission requirements places considerable strain on both wireless and wireline communication systems.

As depicted in Figure 1.2, the architecture of modern communication systems increasingly relies on millimeter-wave (mmWave) frequency bands above 24 GHz to facilitate connections for mobile users, moving vehicles. This frequency range offers the capability to deliver excep-

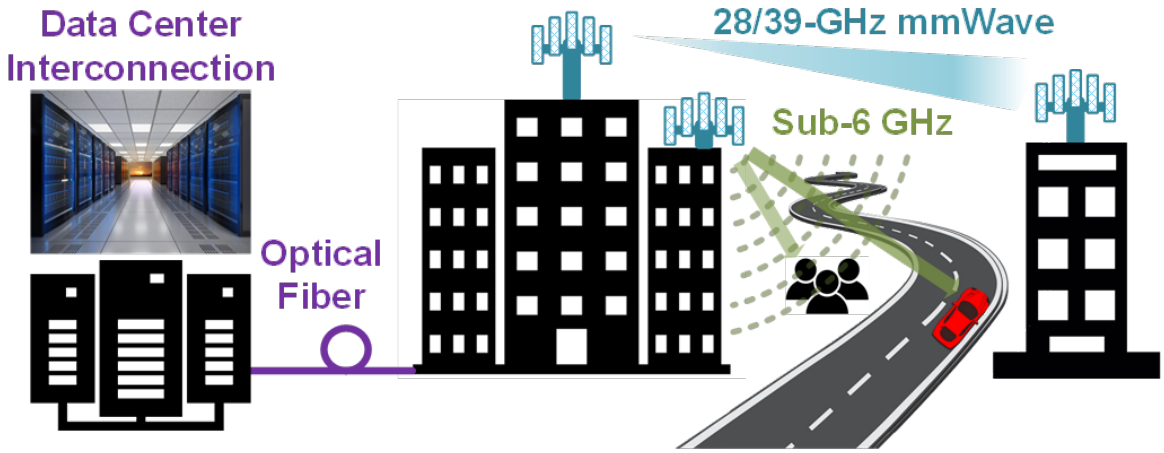


Figure 1.2: The architecture of modern communication system.

tional capacity, ultra-high throughput, and ultra-low latency, effectively addressing the stringent demands for spectrum resources in today's data-driven environment.

In addition to wireless communication, optical communication is a promising solution, particularly in data centers where vast amounts of data are processed and stored. The high bandwidth of light-emitting devices, combined with the low channel loss associated with optical fibers, enhances the efficiency of data transfer in these environments. However, as operating frequencies increase, both mmWave and optical communication systems face a variety of design challenges.

1.1.1 Wireless Communication System

Wireless communication has become an indispensable component of modern information transmission, primarily due to its extensive reach, mobility, and inherent flexibility. As the proliferation of smartphones, Internet-of-Things (IoT) devices, advanced robotics, autonomous vehicles, and satellite communication (SATCOM) continues to accelerate, millimeter-wave (mm-wave) technology, characterized by higher carrier frequencies, emerges as a pivotal player in next-generation communication systems. This is largely attributed to its capacity to provide high bandwidth, which alleviates the growing congestion of the radio frequency spectrum. However, it is crucial to acknowledge that mm-wave signals are subject to significant attenuation during transmission through the atmosphere. To counteract this challenge and facilitate communication over distances extending to several kilometers, phased array systems are frequently utilized, owing to their capabilities in beam steering and their high antenna gain.

Figure 1.3 illustrates a representative phased array system comprising a transmitter (TX) with 64 elements and a receiver (RX) with 32 elements. The antenna array is achieved by dis-

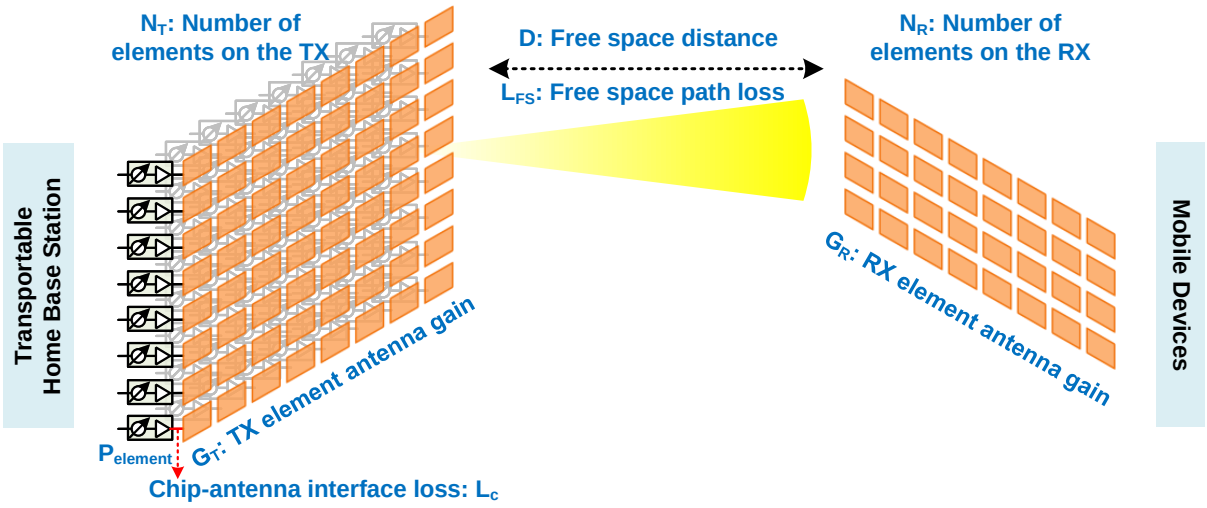


Figure 1.3: Block diagram of phased array system.

crete circuits due to its larger physical dimensions, typically at the centimeter scale, while the transceivers are realized as integrated circuits, necessitating a higher level of complexity. The adoption of Complementary Metal-Oxide-Semiconductor (CMOS) technology is advantageous, given its well-established nature and high integration levels. In this context, the output power of each individual element, denoted as $P_{element}$, is constrained to remain below 20 dBm. For the analysis presented, we consider $P_{element} = 17dBm$, an element antenna gain of 4 dBi for both the TX and RX, and a chip-to-antenna interface loss of 3 dB, leading to the calculation of the equivalent isotropic radiated power (EIRP) as follows:

$$EIRP\,[dBm] = P_{element}\,[dBm] - L_c\,[dB] + G_T\,[dBi] + 20log_{10}\left(N_T\right) = 54dBm. \quad (1.1)$$

The power received at the receiver is calculated by

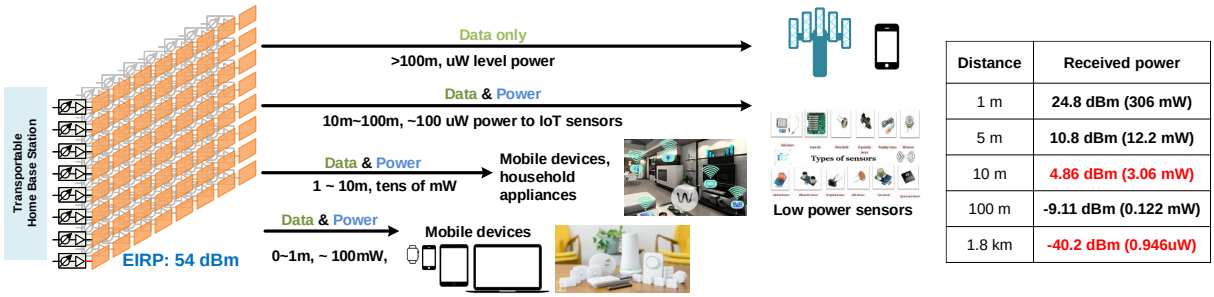
$$Power_{RX}\,[dBm] = EIRP\,[dBm] - L_{FS}\,[dB] + G_R\,[dBi] + 20log_{10}\left(N_R\right), \quad (1.2)$$

where L_{FS} represents the free space loss and is calculated by

$$L_{FS} = (\frac{4\pi d}{\lambda})^2. \quad (1.3)$$

According to regulations set forth by the U.S. Federal Communications Commission [3], the calculated EIRP of 54 dBm falls within the permissible limit of 55 dBm for transportable base stations. This elevated radiated power enables the 28-GHz phased array system, as depicted in

Figure 1.4, to achieve received power levels in the milli-watt range at a distance of 10 meters, and in the micro-watt range at 100 meters. Such capabilities facilitate simultaneous transfer of power and information over the air [4, 5]. Notably, this technology allows for the charging of mobile devices within a radius of 1 meter, household appliances within 10 meters, and IoT sensors within 100 meters. For instance, a study [6] reported that a 60-GHz transceiver received 1.22 mW of direct current (DC) power at a distance of 4 cm, while a 10-GHz phased array achieved 2 W of DC power at a distance of 1 meter [7]. In contrast to traditional wireless power transfer methods, such as inductive or capacitive coupling, phased-array transmitters have the unique advantage of directing energy at a specific angle or even to a predetermined location several meters away by modulating the phase of the electrical signals. This capability ensures true mobility for devices and facilitates energy transfer without physical contact [8, 9].



Distance	Received power
1 m	24.8 dBm (306 mW)
5 m	10.8 dBm (12.2 mW)
10 m	4.86 dBm (3.06 mW)
100 m	-9.11 dBm (0.122 mW)
1.8 km	-40.2 dBm (0.946uW)

Figure 1.4: Power estimation of phased array system for wireless power transfer.

However, the implementation of phased arrays typically necessitates a multitude of antennas and transmitting chips, which inherently drives up costs. As large-scale mm-wave phased arrays are deployed, achieving cost-effectiveness becomes a critical consideration. The overall expenses encompass not only the integrated circuits but also the discrete circuits and their necessary interconnections, which become increasingly complex as the system scales. Furthermore, the design methodologies aimed at optimizing the performance of such expansive systems—integrating both chip-level and board-level circuits—remain inadequately defined. Establishing a well-articulated design framework would provide substantial benefits to the industry, enabling efficient automated design processes, system optimization, and iterative version development.

Moreover, the successful deployment of a phased array system is contingent upon several key factors. These include a TX chip that exhibits high output power, excellent linearity, and precise phase control, alongside an antenna array characterized by low loss and wide bandwidth. The output power of the chip is inherently limited by the breakdown voltage of the MOSFETs used, while the losses incurred by the antenna array are critical to overall system performance. Given that fabrication inaccuracies in discrete circuits tend to be more pronounced than those in integrated circuits—particularly at mm-wave frequencies—it becomes essential for the antenna

array to possess a sufficiently broad bandwidth to effectively compensate for these potential discrepancies.

1.1.2 Optical Communication System

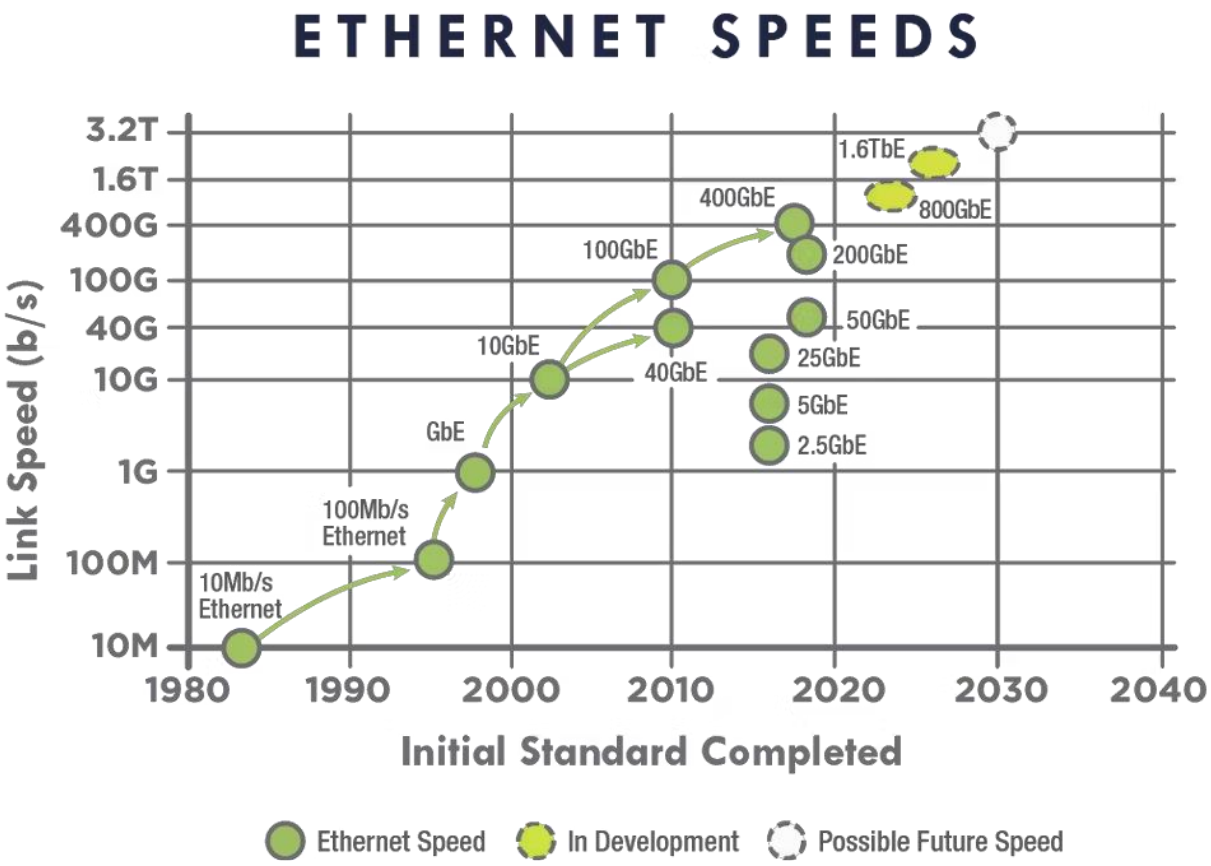


Figure 1.5: Ethernet speeds continue to rise [10].

Ethernet standards are rapidly advancing, transitioning from 100 GbE to 200 GbE and further, driven by the escalating demand for high-speed data transmission, as depicted in Figure 1.5. This illustration highlights the remarkable increase in transmission speeds over recent years.

The rising speed requirements, spurred by innovative applications, necessitate the development of high-speed and low-latency communication systems. Unfortunately, traditional electrical systems often fall short of these stringent demands due to inherent bandwidth limitations [11–15]. Although numerous equalization methods have been proposed to address these limitations [16, 17], they typically result in increased area and power consumption. In response to these challenges, optical communication systems have emerged as a viable solution, offering advantages such as higher bandwidth, reduced cross-talk, shorter delays, lower power consumption, minimized transmission losses, and a more compact and lightweight communication medium.

Optical communication standards have increasingly adopted Pulse Amplitude Modulation-4

(PAM-4) signaling for next-generation systems, primarily due to its superior spectral efficiency [18–22]. However, this comes at a cost: the signal-to-noise ratio (SNR) decreases to 9.5 dB compared to its Non-return-to-zero (NRZ) counterpart, increasing the risk of system failures due to electromagnetic interference (EMI).

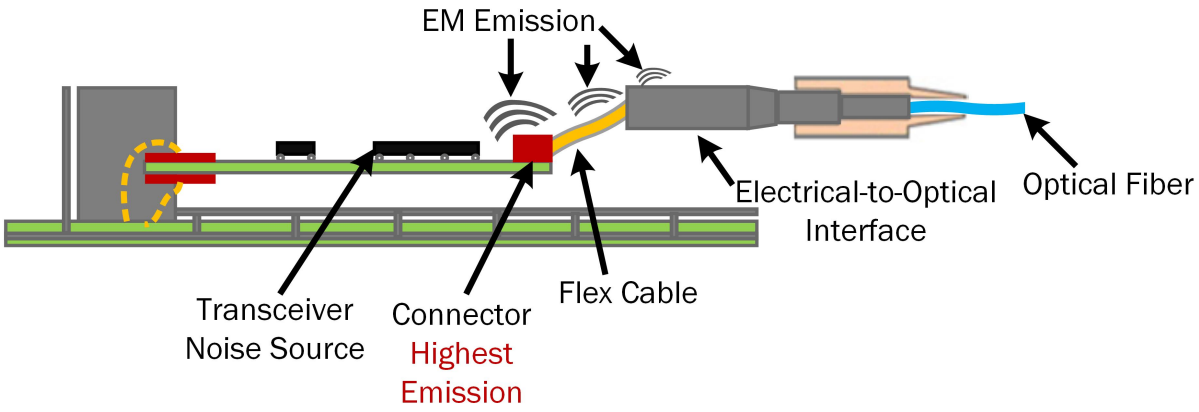


Figure 1.6: The three possible sources of EM emission for Optical transceiver module [23].

The transmitter within an optical transceiver package, despite the inherent resistance of the optical communication channel to electromagnetic interference (EMI), can still generate EMI due to its electronic components. According to measurements from [24], electromagnetic radiation primarily originates from connectors, flex cables, and the electrical-to-optical interface (EOI), as illustrated in Figure 1.6. The connector measures 2.4 mm, while the flex cable spans 2.4 cm in length. To evaluate the total radiation power (TRP) from these components, emissions were minimized using a lossy material, enabling the monitoring of emission levels. Experiments depicted in Figure 1.7 confirm that the connector is the key source of electromagnetic emissions above 15 GHz, which can disrupt weak signals received by a transceiver, potentially elevating the bit error rate (BER) and causing device malfunctions.

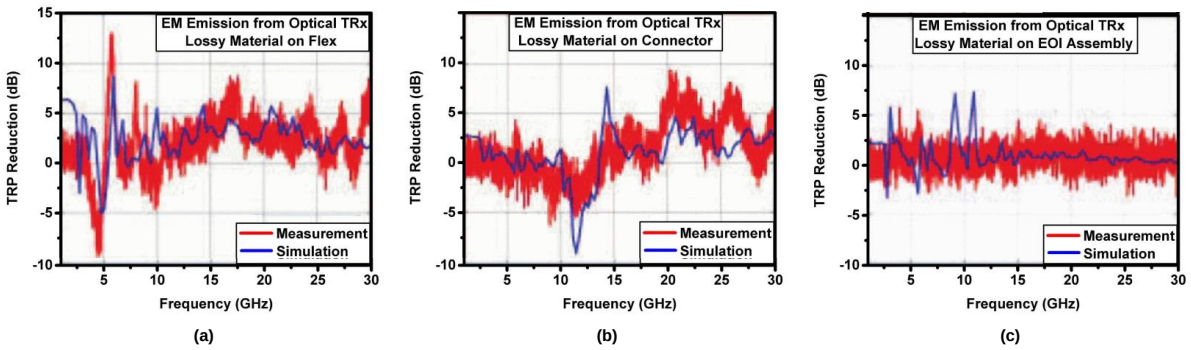


Figure 1.7: Measurement and simulation results of EM emission from optical transceiver module. (a) Reduction of TRP from optical transceiver after adding lossy material on flex cable. (b) On connector. (c) On EOI assembly [24, 25].

Moreover, inter-symbol interference (ISI) resulting from bandwidth limitations of the laser and communication channel exacerbates the degradation of the signal-to-noise ratio (SNR) at the receiver. Various equalization techniques, as utilized in [26–28], are employed to mitigate these non-linear effects. Notably, feed-forward equalizers (FFE) are highly effective in high-speed transmitters, as they preemptively distort the transmitted signal to counteract the non-linear characteristics of both the laser and the channel.

However, the implementation of FFE can negatively impact the rise and fall times of the transmitter output, exacerbating EM emissions. Additionally, advancements in technology nodes have facilitated the design of high-speed circuits. These developments allow for the scaling down of transistor sizes, which directly influences the internal parasitics of transistors. Such changes can result in mismatches in rise and fall times, generating common-mode (CM) noise within the transmitters.

Shielding is the most commonly employed off-chip technique in the industry to mitigate electromagnetic compatibility (EMC) issues [29–31]. This method typically involves increasing the number of gaskets or reducing the size of vent holes to enhance shielding effectiveness [32]. However, implementing more gaskets can be challenging in confined spaces, and smaller vent holes may adversely affect thermal performance. Additionally, absorbers are frequently used around traces or chips to minimize EMI [33], but this approach can be costly and time-consuming, as it requires precise identification of critical points for optimal placement. Moreover, absorbers can negatively impact thermal performance.

Recent advancements in on-chip technology have introduced innovative approaches to diminish CM noise associated with EMI. One strategy, as outlined in [34], involves adjusting the input signal swing and common-mode level of the driver circuit. Another method, detailed in [35], focuses on optimizing the input impedance, rise and fall times, time delays, and amplitude at the driver circuit's input. However, this technique necessitates a controller to oversee the CM noise cancellation system, potentially enlarging the system's size and power consumption. Additionally, a self-calibration method for a source-series terminated (SST) driver, aimed at CM noise suppression, has been introduced in [36, 37]. While these calibration techniques effectively reduce CM noise in driver circuits and support NRZ wireline transmitters at speeds up to 20 Gbps, they are incompatible with PAM-4 signaling or optical transmitters, resulting in heightened power consumption.

1.2 Thesis Organization

This dissertation primarily explores the design of high-frequency CMOS TX tailored for both wireless and optical communication applications.

In Chapter 2, we introduce a co-simulation platform called Integrated System Evaluation Engine (ISEE). This innovative platform is designed to evaluate the transceiver (TRX) system based on system-level specifications, thereby providing invaluable guidance for formulating circuit-level specifications for the various building blocks. To illustrate the functionality of this platform, we present the design and simulation of a 28-GHz direct-conversion TRX front-end system.

Chapter 3 delves into the comprehensive design of a 28-GHz, 4-element phased array system. This chapter encompasses the entire design process, from architectural considerations to the development of both on-chip and on-board building blocks. We demonstrate a complete TX that integrates essential components, including a local oscillator, intermediate-frequency circuits, radio-frequency circuits, an antenna array, and a chip-to-antenna interface. This design achieves high linearity while exhibiting exceptional power and area efficiency.

While Chapter 3 addresses design challenges primarily associated with narrowband circuits in wireless communication, Chapter 4 shifts the focus to the design challenges encountered in optical communication transmitters, concerning broadband circuits. This chapter introduces a CM filter specifically engineered for a 56-Gbps PAM-4 TX. The filter effectively suppresses EMI while maintaining the integrity of the differential-mode signal. Utilizing a delay equalizer structure, this solution operates within the frequency domain and does not incur additional power consumption.

CHAPTER 2

AN INTEGRATED SYSTEM EVALUATION ENGINE FOR COMPLEX-SIGNALING HIGH-SPEED SOCS

This chapter details the development of an Integrated System Evaluation Engine (ISEE), a versatile platform designed to assess the performance of wireless communication transceivers (TRX) that utilize sophisticated high-order modulation schemes. The ISEE seamlessly integrates three simulation tools: Matlab, Advanced Design System (ADS), and Cadence simulators. This integration enables comprehensive performance evaluations across multiple abstraction levels, from the intricate details of transistor-level designs to the broader scope of behavioral models. Moreover, the ISEE is equipped to incorporate experimental data from pre-fabricated modules, ensuring a robust and empirical basis for its assessments.

To illustrate the practical applications and effectiveness of the ISEE, a 28 GHz direct-conversion TRX front-end system was meticulously designed and subjected to simulation tests. The system harnesses orthogonal frequency division multiplexing (OFDM) signals, where sub-carriers are modulated using a quadrature amplitude modulation (M-QAM) scheme. This technology is pivotal for enhancing data transmission efficiency and robustness against interference. Within this TRX configuration, a Doherty transmitter (TX) is paired with three distinct receiver (RX) architectures. Each RX architecture is scrutinized through comparative analysis to unravel their respective advantages and drawbacks.

The results of these co-simulations provide a nuanced understanding of the performance characteristics inherent in each RX architecture. Such insights are instrumental in refining design decisions, particularly in optimizing RX front-end circuits for compatibility with advanced modulation formats. This thorough evaluation accentuates the ISEE's capability to manage complex simulation tasks, demonstrating its flexibility and effectiveness. Additionally, the findings contribute to the ongoing evolution of design strategies, aimed at advancing wireless communication systems by enhancing their efficiency and reliability. Through this platform, researchers and engineers are empowered to innovate and improve the next generation of communication technologies.

2.1 Introduction

The escalating demand for wireless mobile data has driven the exploration of multiple millimeter-wave (mm-wave) frequency bands. These bands are key to enabling ultra-high-speed wireless backhaul connectivity, which is crucial for the deployment of 5G and future mobile networks. The development of compact and integrated mm-wave transceiver front-ends plays a pivotal role in supporting these networks, as they are fundamental to achieving multi-gigabit per second data rates in wireless communication systems. Additionally, the use of wideband modulated signals is becoming more widespread, as they significantly enhance data rates and improve spectral efficiency. Traditionally, the simulation of RF and mm-wave circuit designs is conducted using continuous-wave (CW) signals during the early stages of development. However, the transition to using modulated signals typically occurs after fabrication. This shift can result in inconsistencies, potentially leading to performance discrepancies and inaccurate predictions during the design process. Therefore, establishing a co-simulation platform that evaluates transceiver systems with high-order modulated signals early in the design cycle is crucial to mitigate such issues.

This chapter presents the introduction of the ISEE [38], a tool crafted to enhance the simulation process by incorporating advanced modulation schemes from the onset. The ISEE leverages the capabilities of Matlab, ADS, and Cadence software to form a comprehensive framework capable of evaluating complex modulation scenarios effectively. To showcase the ISEE's capabilities, a 28 GHz transceiver front-end system is carefully developed and analyzed. This system employs orthogonal frequency division multiplexing (OFDM) signals, with sub-carriers that are modulated using high-order quadrature amplitude modulation (QAM) techniques. The comparative analysis of three different RX front-end circuits—referred to as RX-1, RX-2, and RX-3—demonstrates not only the platform's effectiveness but also its potential to provide deep insights into optimizing transceiver design strategies. This approach ensures that the design process is more aligned with real-world performance requirements, ultimately leading to more reliable and efficient wireless communication systems.

2.2 Integrated System Evaluation Engine

The ISEE is visually detailed in Figure 2.1(b), which highlights its two principal components: signal modulation/demodulation and circuit simulation. The process of modulating and demodulating the baseband (BB) signal is executed within the Matlab environment. Meanwhile, the

tasks associated with circuit simulation are handled by a suite of software tools, including ADS, Cadence, and EMX. These tools collectively enable a thorough analysis of the circuit's performance under various conditions. To ensure a seamless and intuitive user experience, a Graphical User Interface (GUI) has been developed using Matlab, as shown in Figure 2.1(a). This GUI is thoughtfully designed, featuring a parameter setting panel on the left side, which allows users to input and adjust various simulation parameters. On the right side, the GUI displays the results of the simulations, including both the modulated and demodulated signals.

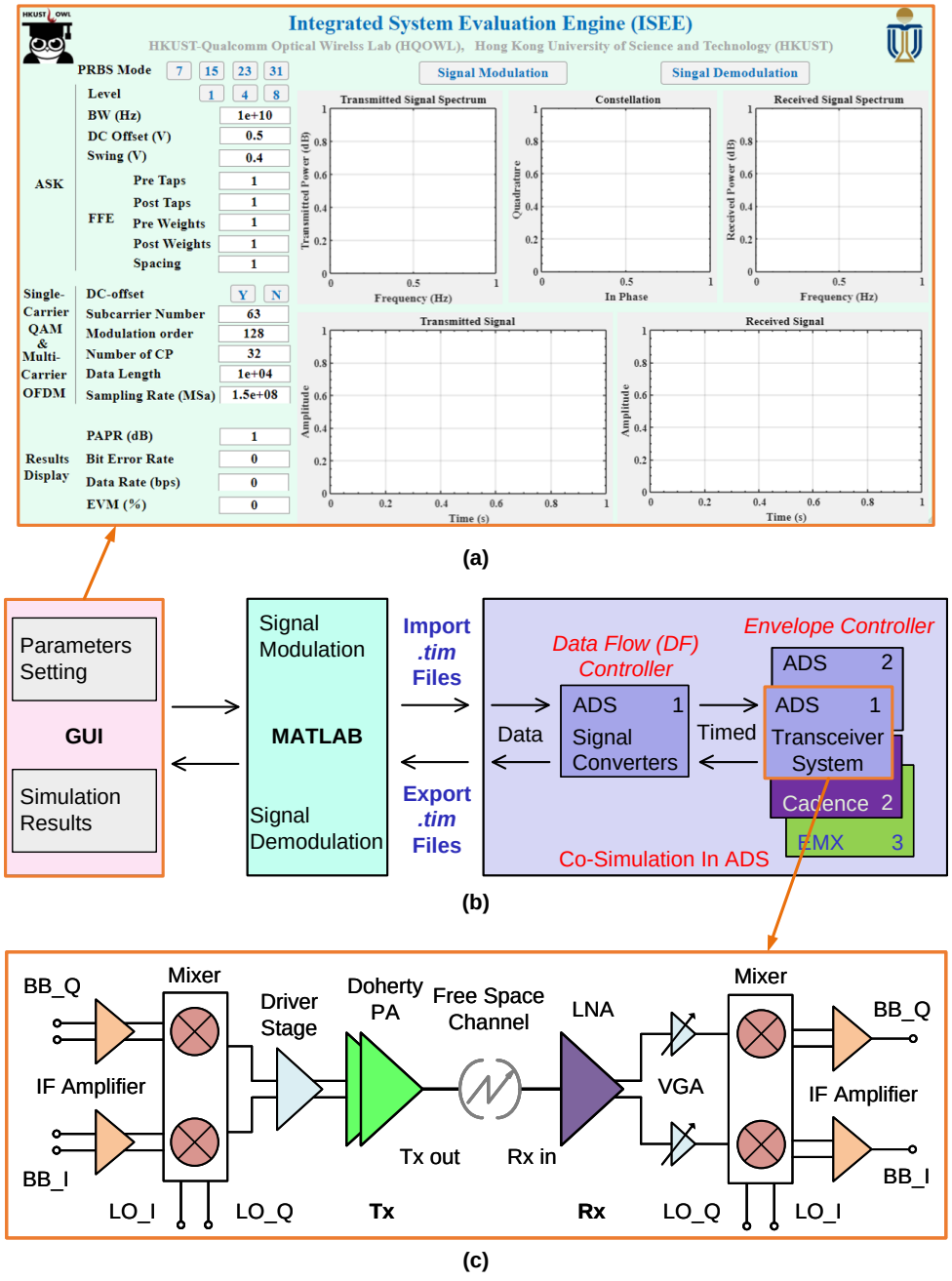


Figure 2.1: (a) The graphical user interface of ISEE. (b) Diagram of ISEE. (c) Architecture of the 28 GHz TRx front-end system.

To begin the modulation process, users can simply click on the Signal Modulation icon within the GUI. This action initiates the modulation sequence, after which the GUI provides a detailed presentation of the transmitted baseband signal's characteristics. This includes visualizations of the baseband spectrum and the constellation diagram of the M-QAM OFDM signal, offering users a clear understanding of the signal's structure and quality. When the Signal Demodulation icon is activated, the demodulation process starts. Upon completion, the GUI not only shows the demodulated spectrum and constellation but also updates dynamically to display crucial performance metrics. These metrics include the Bit Error Rate (BER), Error Vector Magnitude (EVM), and the data rate of the received baseband signal, as illustrated in Figure 2.1(a).

This dynamic and interactive GUI significantly enhances the user experience by providing immediate visual feedback on the performance and characteristics of the simulated signals. It allows users to quickly assess the impact of different parameters on signal quality and system performance, facilitating a more efficient and informed design process. By integrating these comprehensive features, the ISEE empowers users to conduct in-depth analyses and optimizations of transceiver systems, ultimately driving advancements in high-frequency CMOS IC design.

The configuration of the engineered 28 GHz direct-conversion transceiver front-end system is depicted in Figure 2.1(c). This configuration showcases the process where the BB In-phase and Quadrature (I/Q) signals, initially generated in the digital domain, are up-converted to the Radio Frequency (RF) domain using I/Q mixers. These mixers play a crucial role in shifting the frequency of the signals to the desired RF range. Once converted, these RF signals undergo amplification to ensure they possess the necessary power levels for effective transmission. The amplified signals are then emitted through an antenna, which serves as the medium for wireless communication.

To accurately simulate the interaction between the TX and RX in a real-world scenario, it is essential to consider the channel characteristics. The channel loss, which affects signal propagation, is computed using Equation 1.3. This calculation accounts for factors such as distance and frequency that may attenuate the signal. At the receiver end, the process is reversed: the incoming RF signals are down-converted back to BB I/Q signals by I/Q mixers, preparing them for digital processing and analysis.

ADS offers a user-friendly platform for circuit design and simulation, making it a preferred choice for many engineers. However, when it comes to the design of integrated circuits, Cadence provides a more comprehensive suite of tools, particularly when paired with specialized circuit design kits. For sub-circuits within the transceiver system that are designed using Cadence, integrating this software with Matlab is crucial for a cohesive design process. This integration can

be achieved through the dynamic link provided by Keysight, which supports seamless interoperability between ADS and Cadence simulators. Alternatively, data transfer between Matlab and Cadence can be managed through file exchanges, utilizing .dat and .csv formats for imports and exports, respectively.

This robust integration framework ensures a smooth transition between different simulation environments, thereby enhancing both the efficiency and accuracy of designing and testing the transceiver system. It allows for a holistic approach where the strengths of each tool are leveraged, providing a comprehensive and reliable simulation environment that supports the optimization and innovation of high-frequency CMOS IC designs for wireless communication systems.

2.3 28-GHz Transceiver Front-End Circuit

This section delves into the design and CW signal simulation results for the TX and three distinct RX front-end circuits, providing a comprehensive understanding of their configurations and performance metrics.

2.3.1 Design and CW-Simulation of Transmitter

The TX configuration is composed of several key components: two baseband (BB) amplifiers, an In-phase and Quadrature (I/Q) modulator, a driver stage, and a Doherty power amplifier (DPA), as depicted in Figure 2.1(c). The inclusion of the DPA is a strategic decision aimed at enhancing the Direct Current (DC) to Radio Frequency (RF) efficiency of the TX [39]. The I/Q modulator employs an active double-balanced Gilbert cell, a proven architecture for achieving high linearity and isolation, as shown in Figure 2.2(a). To ensure sufficient input power is delivered to the DPA, a driver stage is meticulously placed between the I/Q modulator and the DPA. The schematic of the DPA is detailed in Figure 2.2(b), with particular attention given to the parasitic effects of transistor interconnections. These effects are meticulously modeled using the EMX simulator, which is essential given the large transistor sizes used in the DPA.

The TX configuration is composed of several key components: two baseband (BB) amplifiers, an In-phase and Quadrature (I/Q) modulator, a driver stage, and a Doherty power amplifier (DPA), as illustrated in Fig. 2.1(c). The inclusion of the DPA is specifically intended to improve the Direct Current (DC) to Radio Frequency (RF) efficiency of the TX [39]. For constructing the I/Q modulator, an active double-balanced Gilbert cell is utilized, as shown in Fig. 2.2(a). A driver stage is strategically placed between the DPA and the I/Q modulator to ensure adequate

input power is delivered to the DPA. The schematic of the DPA is provided in Fig. 2.2(b), with parasitic effects of transistor interconnections accounted for using the EMX simulator, due to the large transistor sizes employed in the DPA.

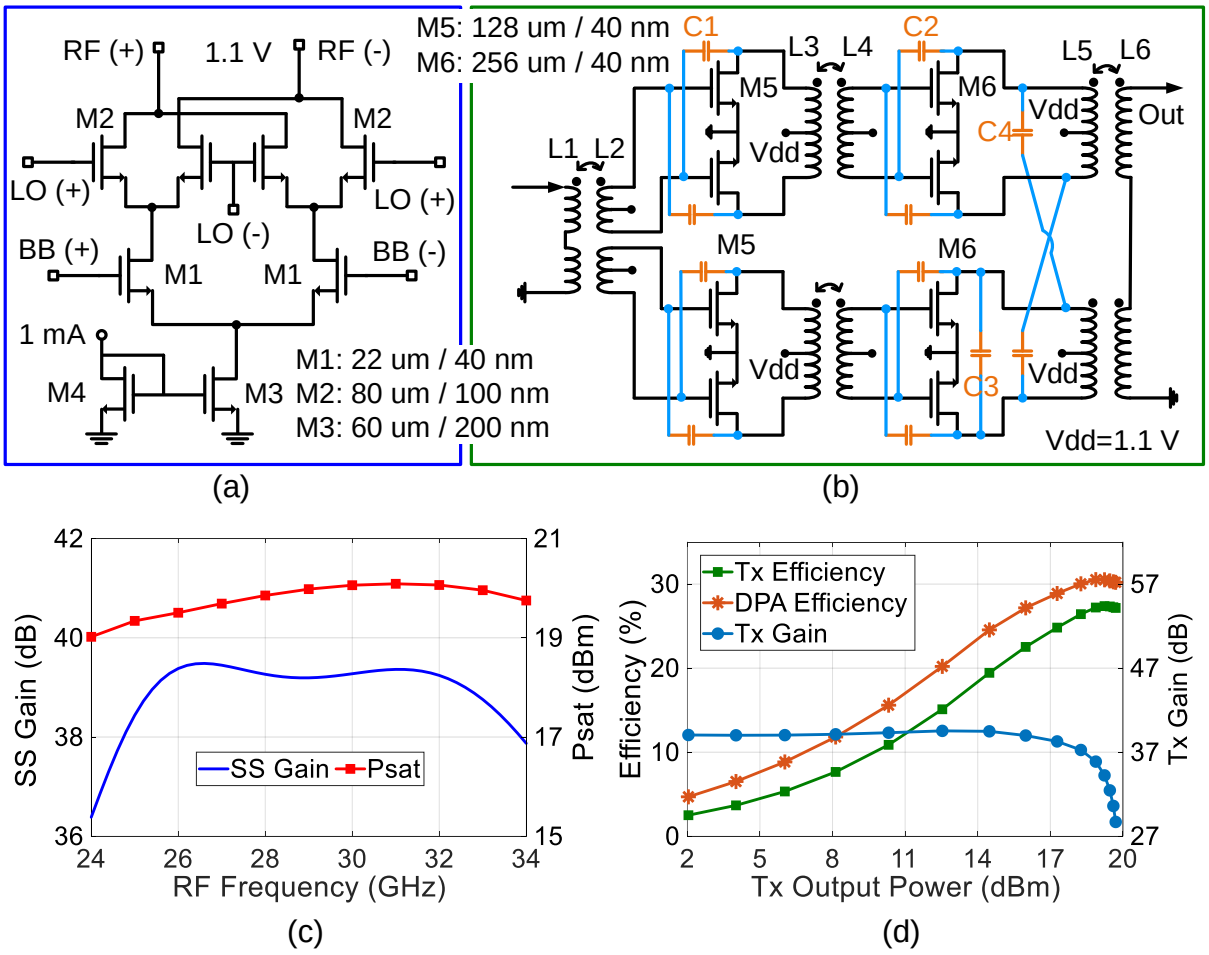


Figure 2.2: Schematics of (a) the up-conversion mixer and (b) Doherty power amplifier. (c) Simulated SS gain and Psat of the TX versus RF frequency. (d) Simulated TX efficiency and gain versus output power.

In the Doherty transmitter design, both the carrier and peaking Power Amplifiers (PAs) are built using a two-stage differential PA with neutralized capacitors. To further enhance the DPA's efficiency, a serial combining transformer is incorporated, along with cross-connected capacitors (C4). This configuration offers several benefits: firstly, the combining transformer is fully utilized when the peaking PA is inactive [39]; secondly, the symmetrical structure allows for centralization of the DC supply at the transformer's center tap; and thirdly, C4 serves a dual purpose as part of the matching network, contributing to the overall efficiency and performance of the system.

The simulation results for the TX front-end under CW signal excitation are presented in Figures 2.2(c) and (d). Figure 2.2(c) illustrates the simulated small signal (SS) gain and saturation

output power (Psat) across various RF frequencies, demonstrating that the TX achieves an SS up-conversion gain ranging from 38.4 to 39.5 dB, with a Psat between 19.3 and 20.1 dBm. At the target frequency of 28 GHz, the TX delivers a Psat of 19.7 dBm and achieves a P1dB of 17.5 dBm, as shown in Figure 2.2(d). Additionally, the figure highlights the TX's DC-to-RF conversion efficiencies, achieving 27.2% at Psat and 17.5% at 6-dB back-off power levels. For the DPA, the drain efficiencies are 30.2% and 22.5% at Psat and 6-dB back-off power levels, respectively. The 28 GHz TX front-end consumes a power of 56.6 mW from a 1.1 V supply voltage, showcasing its efficiency. During the evaluation of the three RX front-end systems that follow, the TX consistently delivers an average output power of 8 dBm, ensuring stable performance for the subsequent analyses.

2.3.2 Design and CW-Simulation of Receivers

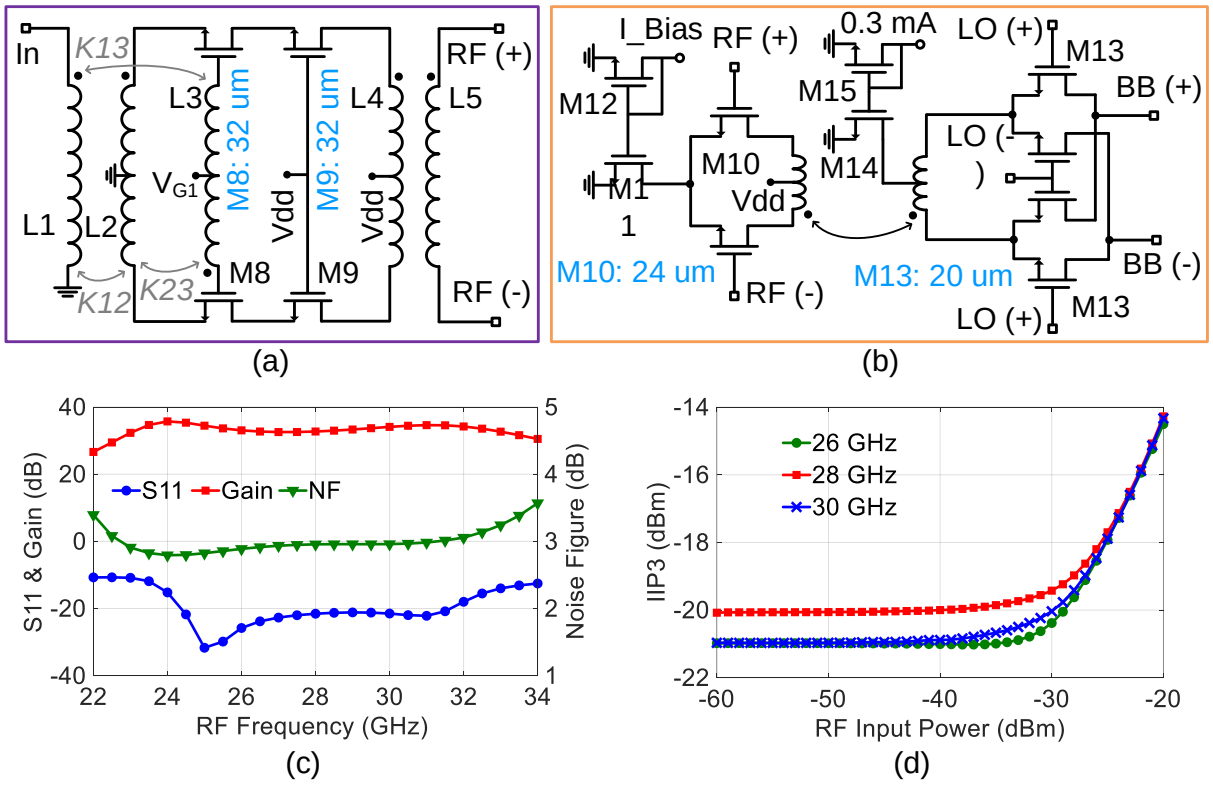
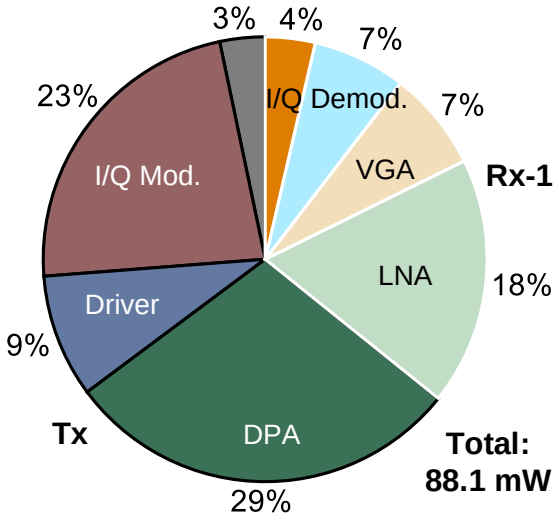


Figure 2.3: Schematics of (a) LNA and (b) VGA and I/Q demodulator of Rx-1. (c) Simulated S11, voltage gain and noise figure versus RF frequency of Rx-1. (d) Simulated IIP3 of the Rx-1 with respect to RF input power.

The broadband RX-1 configuration includes a LNA, two variable gain amplifiers (VGAs), an I/Q demodulator, and two BB amplifiers, as depicted in Fig. 2(c). Figures 2.3(a) and (b) illustrate the schematics of the LNA, VGA, and I/Q demodulator. Following the design in [40] the LNA

employs a differential gm-boosted common-gate architecture. A compact three-coil transformer is used for single-ended to differential conversion, broadband input matching, gm-boosting, and noise suppression at the LNA input. The I/Q demodulator features a folded architecture to support wideband operation.

As shown in Fig. 2.3(c), RX-1 achieves a conversion gain of 32.8 to 34.7 dB, an S11 of less than -15.1 dB, and a noise figure (NF) of 2.8 to 3.2 dB across the frequency range of 25.0 to 32.5 GHz. Moreover, using a two-tone simulation with a 20 MHz separation, RX-1 demonstrates an input third-order intercept point (IIP3) of more than -20.1 dBm at 28 GHz, as depicted in Fig. 2.3(d). The RX-1 front-end consumes 31.5 mW from a 1 V supply voltage, as shown in Fig. 2.4.



Blocks		Voltage (V)	DC Power (mW)	
Tx	IF Amp.	1.1	2.9	56.6
	I/Q Mod.	1.1	20.2	
	Driver	1.1	7.9	
	DPA*	1.1	25.6	
Rx-1	LNA	1	15.9	31.5
	VGA	1	6.4	
	I/Q Demod.	1	6.0	
	IF Amp.	1	3.2	

Figure 2.4: Power breakdown of the TX and RX-1.

To facilitate a comprehensive comparative analysis and further validate the capabilities of the ISEE, two additional receiver configurations, RX-2 and RX-3, were developed. As depicted in Figures 2.5(a) and (b), RX-2 is designed with a cascode common source stage single-ended Low Noise Amplifier (LNA) featuring inductive degeneration [41]. This LNA is coupled with two passive mixers and two BB amplifiers. Simulation results for RX-2 under a CW signal indicate a voltage gain exceeding 31.6 dB, an S11 of less than -15.3 dB, a noise figure ranging from 2.9 to 3.9 dB, and an IIP3 surpassing -17 dBm across the frequency range of 26.5 to 31.5 GHz.

The RX-3 architecture, detailed in Figures 2.5(c) and (d), incorporates an LNA, two active mixers, and two BB amplifiers. The LNA in RX-3 is identical to that in RX-2, thus its design specifics are not separately illustrated in Figure 2.5(d). RX-3 achieves a voltage gain greater than 30.7 dB, with an S11 below -11.2 dB, maintaining an NF under 3.2 dB, and an IIP3 exceeding -18.3 dBm over the frequency range of 27 to 29 GHz.

Through the development and analysis of RX-1, RX-2, and RX-3, this study provides a comprehensive evaluation of different design approaches, each with unique characteristics and advantages. These insights are instrumental in guiding future design strategies for high-frequency CMOS ICs in wireless communication, highlighting the importance of balancing gain, linearity, noise, and power efficiency. The comparative data from these receiver configurations not only demonstrate the efficacy of the ISEE but also offer a valuable framework for optimizing receiver design in next-generation communication systems.

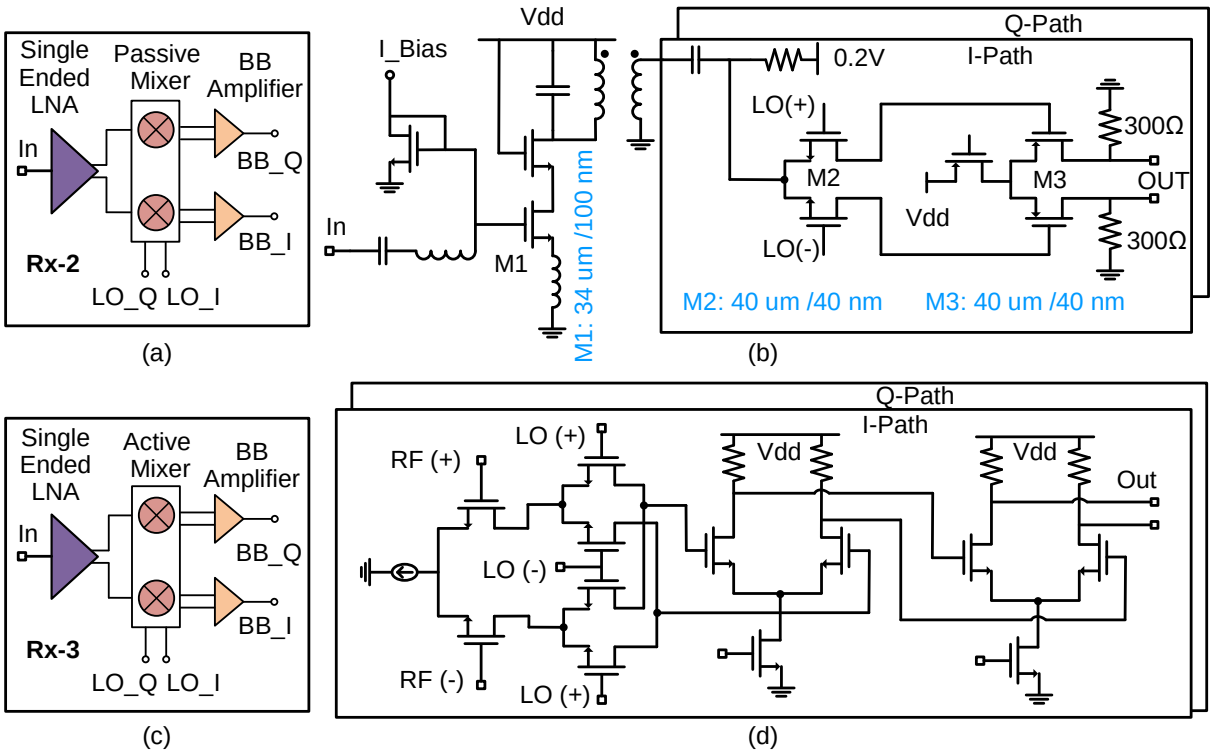


Figure 2.5:
(a) Block diagram and (b) schematic of RX-2. (c) Block diagram and (d) schematic of RX-3.

2.4 Cross-Domain Simulation Utilizing ISEE

Using the ISEE, comprehensive simulations were performed on the three RX front-end systems, leveraging a 16-QAM OFDM signal characterized by a peak-to-average power ratio (PAPR) of 7.6 dB. In these simulations, the same TX front-end circuits were utilized across all three configurations to ensure consistency in the evaluation process. Figure 2.6 illustrates the simulated performance results for RX-1 when the RX input power is configured at -45.7 dBm, using an 800-MHz QAM-16 signal. This setup provides a realistic assessment of the RX-1's ability to handle high-order modulation schemes.

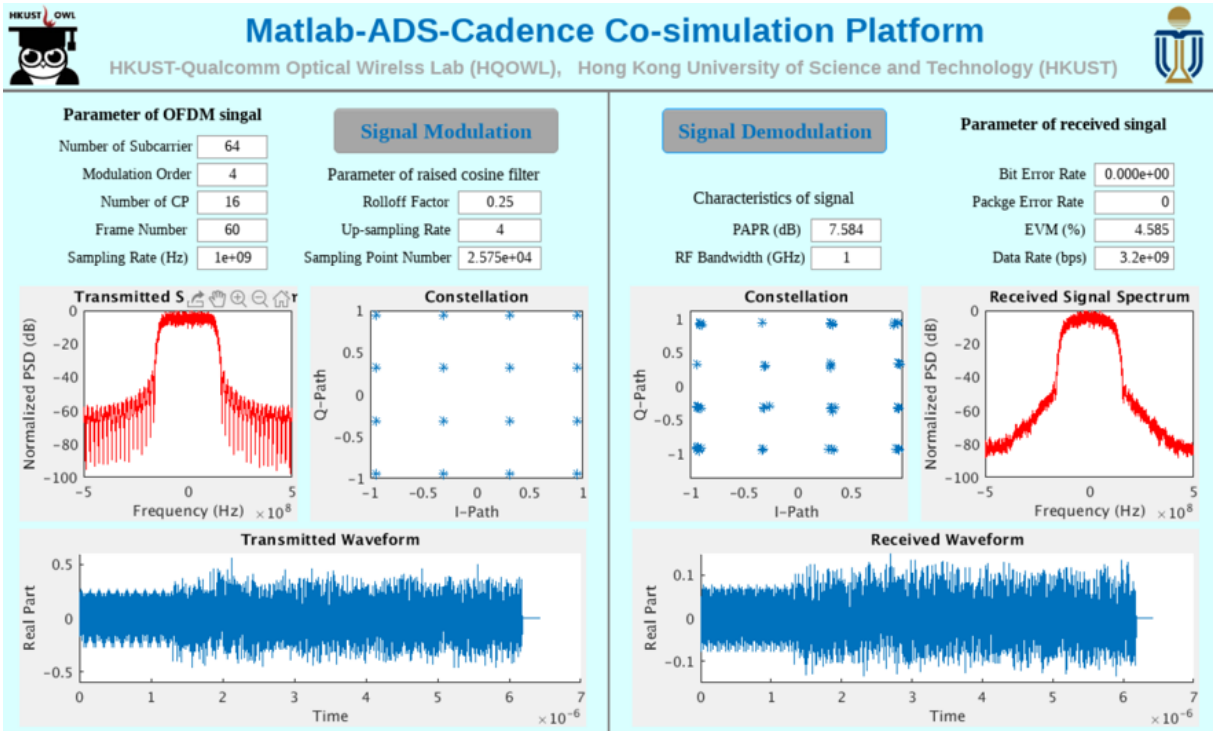


Figure 2.6: Simulation results
for TX and RX signals using 800-MHz 16-QAM signalling at a RX input power of -45.7 dBm.

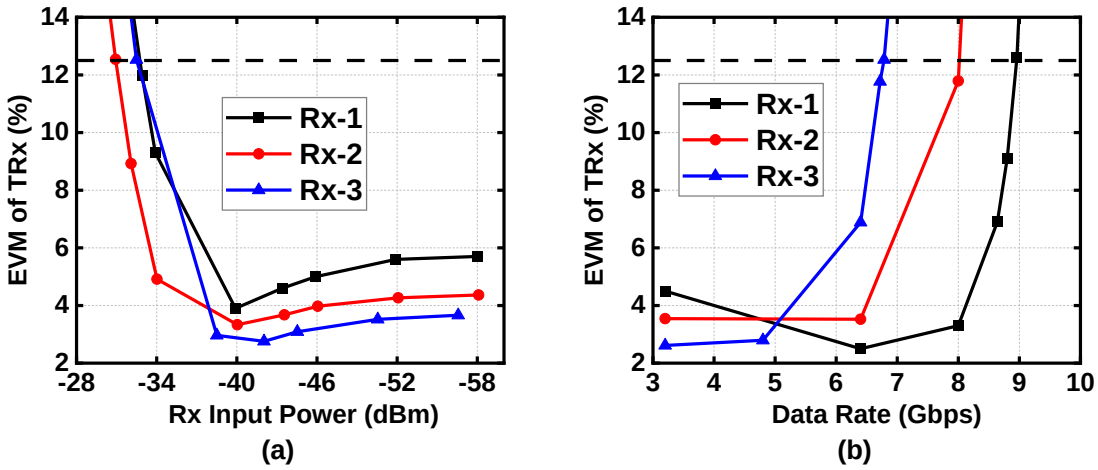


Figure 2.7:
Simulated EVM of the 16-QAM OFDM signal versus (a) Rx input power and (b) data rate.

The relationship between the received signal's EVM and the RX input power for a 1 GHz OFDM signal is depicted in Figure 2.7(a). The findings from these simulations reveal that all three TRX systems achieve peak EVM performance when the RX input power is approximately -40 dBm. This optimal input power level ensures that the receivers operate within their linear range, minimizing distortion and maximizing signal integrity. Figure 2.7(b) illustrates the simulated relationship between EVM and data rate for the three TRX systems at an RX input power

of around -41.8 dBm. With a stringent EVM requirement of 12.5% for 16-QAM OFDM signals [42], the TRX systems featuring RX-1, RX-2, and RX-3 achieve data rates of 9.0, 8.0, and 6.7 Gbps, respectively.

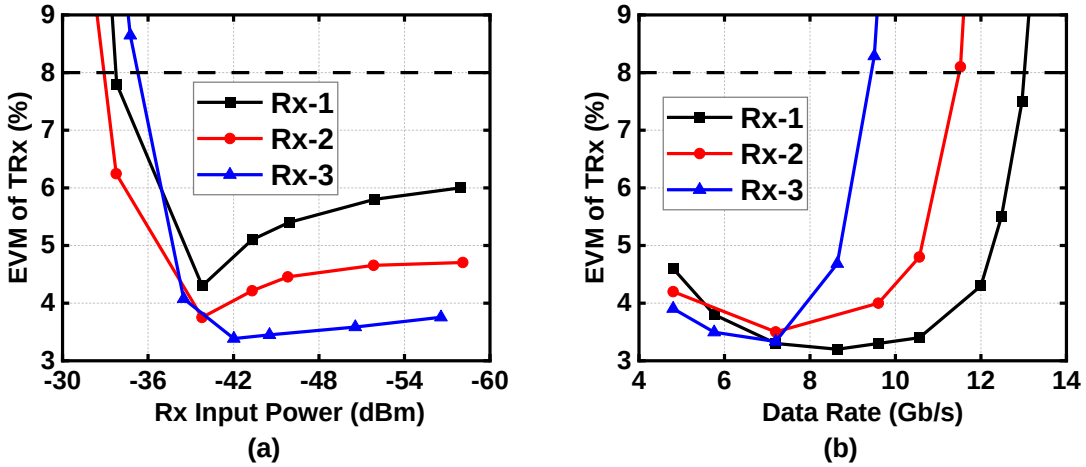


Figure 2.8:
Simulated EVM of the 64-QAM OFDM signal versus (a) Rx input power and (b) data rate.

Further evaluations of the TRX front-end systems were conducted using a more complex 64-QAM OFDM signal with a PAPR of 8 dB. The simulated EVM behavior of the three TRX systems as a function of RX input power is presented in Figure 2.8(a). Consistent with the results obtained from the 16-QAM OFDM signal, the three TRX systems demonstrate optimal EVM performance at an RX input power level around -40 dBm. Figure 2.8(b) shows the EVM versus data rate curves for the 64-QAM OFDM signal, providing a detailed view of how each system handles increased modulation complexity and higher data throughput requirements.

Table 2.1 offers a comparative performance analysis of the three RX front-end circuits. With an EVM requirement of 8% for 64-QAM OFDM signals, the TRX system utilizing RX-1 supports the highest data rate, achieving 13.1 Gbps. In contrast, RX-3 supports the lowest data rate of 9.5 Gbps, indicating a trade-off between complexity and performance. Notably, the TRX system featuring RX-2 achieves the highest Figure of Merit (FoM), primarily attributed to the low power consumption of its passive mixers. This analysis highlights the importance of balancing power efficiency with performance, especially in high-frequency applications where energy consumption can significantly impact overall system viability.

2.5 Conclusions

In this chapter, we introduced the ISEE, a tool crafted to evaluate high-speed communication systems that utilize complex modulated signals. This development addresses one of the critical challenges in IC design: the substantial costs associated with IC fabrication. By enabling comprehensive system-level evaluations pre-fabrication, ISEE provides a strategic advantage to designers. We showcased its capabilities through the design and assessment of a 28 GHz TRX system, which includes three distinct receiver (RX) configurations. This case study underscores the effectiveness of ISEE in minimizing simulation errors that typically arise from relying on simplistic behavioral models of circuit components—both passive and active.

ISEE has been meticulously designed with the needs of IC designers in mind, providing a platform that allows for the evaluation of circuits at the system level using realistic modulated signals before the physical fabrication stage. This capability significantly increases the probability of successful chip design by providing detailed insights into how the circuits will perform in real-world scenarios. Moreover, ISEE offers invaluable assistance in enabling designers to compare and select the most suitable system architectures for their specific applications. This process not only reduces the design costs associated with iterative prototyping and testing but also accelerates the overall development timeline, allowing for faster time-to-market for new technologies.

Looking towards the future, the potential for ISEE to evolve is substantial. One of the exciting prospects for its development is the ability to synthesize complex systems using a library of predefined circuit templates. Such a feature would greatly expand the utility and flexibility of the platform, offering designers a streamlined process for constructing and evaluating a wide range of systems. This evolution could transform ISEE into an even more powerful tool in the field of IC design and evaluation, facilitating innovation and enabling designers to push the boundaries of what is possible in high-frequency CMOS IC design for both wireless and optical communication. As we continue to develop and refine this tool, its integration into the design workflow promises to enhance efficiency, reduce costs, and improve the overall quality of ICs produced for cutting-edge communication technologies.

Parameters		RX-1	RX-2	RX-3
NF (dB)		2.8 – 3.1	3.0 – 3.2	2.9 – 3.9
Bandwidth (GHz)		25.0 – 32.5	26.5 – 31.5	27.0 – 29.0
Voltage Gain (dB)		32.8 – 34.7	28.9 – 31.3	31.6 – 34.5
IIP3 (dBm)		-22.3 – -19.4	-18.6 – -16.5	-20.8 – -17.6
S11 (dB)		< -15.1	< -10.1	< -15.3
Pdc (mW)		31.5	16.8	18.3
64-QAM Simulation	Number of Subcarrier	64	64	64
	Pavg (dBm)	-41.7	-41.9	-40.4
	Signal BW [GHz]	2.7	2.4	2
	Data Rate (Gbps) @ EVM (%)	13.1	11.5	9.5
		8.0	8.1	8.0
FoM* (bps/Hz)		2.0	4.8	4.0
$* FoM = \frac{Gain \times IIP3[mW] \times Data\ Rate[bps]}{Pdc[mW] \times (F-1) \times EVM \times Signal\ BW[Hz]}$				

Table 2.1: Performance comparison table of the three Rx front-end circuits.

CHAPTER 3

DESIGN AND IMPLEMENTATION OF A 4-ELEMENT 28-GHZ PHASED-ARRAY TRANSMITTER AND ANTENNA ARRAY

This chapter comprehensively introduces a Ka-band 4-element phased-array transmitter (TX), alongside a co-optimized wideband chip-antenna interface tailored for phased array systems. This system features an advanced intermediate-frequency local-oscillator phase shifting (IFLO PS) architecture, which not only demonstrates exceptional power and area efficiency but also provides highly linear gain-invariant phase shifting and phase-invariant gain control. The TX employs the sliding-IF architecture, incorporating an on-chip phase-locked loop (PLL) along with a divide-by-4 circuit. This integration effectively generates a low-phase noise 22.4-GHz RF local oscillator (RFLO) and a 5.6-GHz intermediate frequency local oscillator (IFLO), crucial for high-performance signal processing.

In the IF path, the system utilizes a multiplex-and-interpolation-based IFLO phase shifter. This approach allows the TX to achieve an outstanding root mean square (RMS) phase error ranging from 0.63° to 0.85°, coupled with a minimal RMS phase shifter-induced gain error between 0.02 and 0.05 dB. Moreover, a proposed transadmittance-transimpedance IF VGA offers a 13-dB gain control range, complemented by an RMS gain control-induced phase error of just 0.3° to 0.6°. Assisted by this advanced architecture, the TX system achieves completely orthogonal phase shifting and gain control, thus optimizing performance across various operating conditions.

The sliding-IF scheme facilitates a reduced RFLO frequency centered at 22.4 GHz, which allows for the implementation of inductor-less RFLO buffers. This contrasts significantly with the direct-conversion architecture, where a resonance-mode RFLO buffer is necessary. The proposed architecture simplifies the mmWave path by incorporating only an RF mixer and a streamlined two-stage power amplifier (PA). The first stage of the PA utilizes a class-C architecture with adjustable bias, effectively introducing gain peaking to counteract compression effects that might arise in the second stage, thereby significantly enhancing the overall linearity and robustness of the system.

A design methodology for XF-based matching networks (MN), underscored by comprehensive mathematical analysis, is proposed to improve output power and efficiency beyond what conventional simulation and intuition can achieve. The on-board matching network is strategically positioned between the bonding wire from the IC and the antenna. It employs two precisely configured short stubs to mitigate bandwidth reduction caused by the inherent inductance from bonding wires and extended transmission lines, ensuring optimal signal integrity and performance.

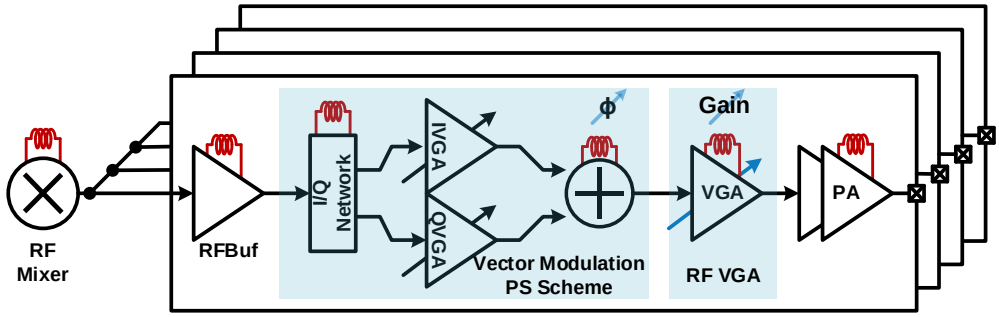
The power amplifier sets a benchmark by achieving a saturation output power of 20 dBm, a 1 dB compression point (P_{1dB}) of 18.5 dBm, and a peak drain efficiency of 30.3%. This performance represents the highest International Technology Roadmap for Semiconductors (ITRS) figure of merit known to date, highlighting the cutting-edge nature of this development. Notably, the PA attains an impressive power density of 1.0 W/mm², showcasing its efficiency and capability. As a result, the phased-array TX achieves a state-of-the-art area efficiency of 0.26 mm² per element and a peak power efficiency of 24.1%, representing a significant advancement in phased-array transmitter technology.

3.1 Introduction

In the rapidly evolving landscape of wireless communication, particularly with the advent of 5G new radio and the forthcoming 6G systems, phased arrays have become indispensable. These arrays are extensively utilized for their exceptional ability to steer beams and deliver high antenna gain, which is crucial for effectively overcoming the significant free space path loss encountered at millimeter-wave frequencies. This capability is essential as communication systems continue to push into higher frequency bands to meet the growing demands for bandwidth and data throughput [43–45].

One of the fundamental requirements for phased array systems is the precise control of phase shifting (PS) and gain. These elements are critical to ensuring that the beam steering capabilities are both accurate and efficient. Traditionally, radio-frequency (RF) phase-shifting-based phased-array TXs have relied on a vector modulation scheme, as depicted in Figure 3.1. However, the nonlinear relationship between the phase shift and the gain of in-phase/quadrature (I/Q) variable gain amplifiers (VGAs) can lead to degraded phase shift linearity. Additionally, the extensive use of mmWave modules with inductive devices leads to increased chip area and power consumption [46, 47].

Prior art 1: RF Phase Shifting-Based Phased-Array TX Architecture

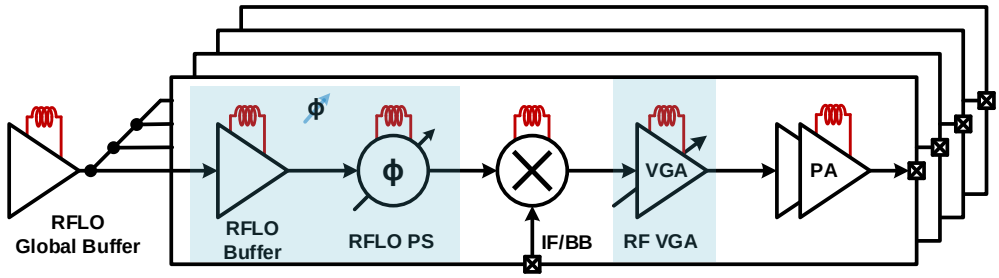


✗ Excessive mmWave blocks: power and area hungry

✗ Phase shifting (PS) based on vector modulation scheme: PS nonlinearity

✗ RF PS and RF VGA: nonorthogonal phase shift and gain control

Prior art 2: RFLO Phase Shifting-Based Phased-Array TX Architecture

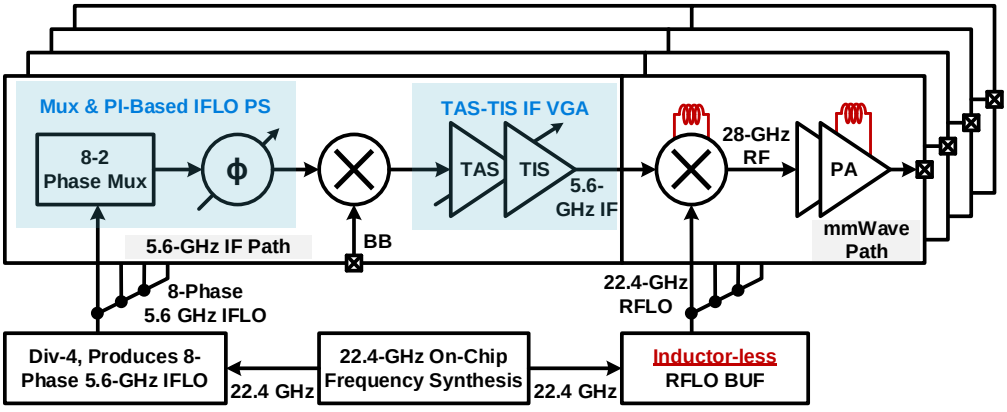


✗ Requires RFLO buffers and RF mixers in each element: power and area hungry

✓ RFLO PS scheme: linear PS & phase-invariant gain control

✗ RF VGA: gain control induces phase variation

This work: IFLO PS + IF VGA-Based Sliding-IF Phased-Array TX



✓ Concise mmWave path, ind-less RFLO buffer: superior power & area efficiency

✓ IFLO PS: power-efficient, highly-linear, and gain-invariant phase shifting

✓ TAS-TIS IF VGA: phase-invariant gain control

Figure 3.1: Comparison of prior art with the proposed IFLO PS and IF VGA-based phased-array TX.

An alternative approach is the RF local oscillator (RFLO) phase-shifting technique, which offers linear and gain-invariant phase shifting. However, this method requires additional area to accommodate the global RFLO distribution network [48]. Moreover, both traditional architectures are hindered by the use of RF VGAs, which are particularly sensitive to variations in nonlinear parasitic capacitance. These variations can cause significant phase variations as the gain is controlled, further complicating the design and operation of phased-array systems [46–49].

In response to these challenges, this work introduces an innovative phased-array transmitter based on an intermediate-frequency local-oscillator (IFLO) phase-shifting scheme, illustrated in Figure 3.1. The proposed TX adopts a sliding-IF architecture integrated with an on-chip phase-locked loop (PLL). The RFLO and IFLO are centered at 22.4 GHz and 5.6 GHz, respectively. By implementing phase shifting for the IFLO signal using a novel multiplex (mux)-and-interpolation-based IFLO phase shifter, the system achieves highly linear and gain-invariant phase shifting. This approach ensures that the phase control remains consistent across different gain settings, thereby enhancing the overall system performance.

Supporting this architecture is a transadmittance-transimpedance (TAS-TIS) IF VGA, which provides wide-range and phase-invariant gain control. The millimeter-wave path in this configuration is streamlined, consisting only of a double-balanced RF mixer and a two-stage power amplifier (PA) with a transformer-based matching network. This concise path reduces complexity, chip area, and power consumption, making it a highly efficient solution for modern communication systems.

To accommodate the ever-increasing demand for higher data rates within the limited spectrum available, communication systems often resort to complex modulation schemes. These schemes are characterized by high peak-to-average power ratios (PAPR), which place stringent demands on the transmitter (TX), particularly the power amplifier (PA). Maintaining excellent linearity at elevated output power levels becomes crucial to ensure signal integrity and minimize distortion. What is more, CMOS technology, known for its high level of system integration, stands out as the preferred choice for implementing phase array systems. However, leveraging CMOS technology for high-power applications brings its own set of challenges, primarily due to high silicon substrate loss and low breakdown voltage, which complicate efforts to achieve the desired high output power [50].

To address these challenges, several innovative strategies have been proposed. One prominent approach is power combining through multiple paths, which has gained considerable attention for its potential to alleviate the demand for high-output-power devices [51–54]. The un-

derlying principle of this technique is that by combining the output power from multiple paths, it is possible to achieve a higher total output power without relying on individual high-output-power devices. However, while the output power indeed increases with the number of combining paths, this approach introduces significant complexity to the combining network. The added complexity can result in greater losses than gains, eventually reaching practical limitations in terms of design and implementation. Moreover, the substantial area required for the combining network—exemplified by coupled lines [55] and transformers [56]—poses additional challenges, particularly in phased-array systems where space and integration are critical considerations.

An alternative strategy is the stacking of transistors, which presents a promising topology capable of withstanding higher supply drain voltages and enhancing the output swing, all while maintaining a compact footprint [57–59]. This approach allows for increased power handling capability without significantly expanding the circuit area. However, a notable drawback of stacked PAs is that their power gain tends to compress rapidly due to the combination of high gain and output swing. To mitigate this issue, our work incorporates a class-C driver stage with adjustable bias, specifically designed to extend the gain and improve the linearity of the TX. This enhancement ensures that the TX can handle high power levels while maintaining signal fidelity.

Another critical factor influencing output power is the efficiency of the output matching network (MN). Transformer-based matching networks, compared to traditional resonant LC MNs, maintain efficiency even at higher output power levels [60]. These networks are effective in decoupling direct current (DC) from alternating current (AC) and isolating even-mode noise, making them a popular choice in PA designs [61–64]. Despite their advantages, the implementation of a transformer network composed of two inductors poses challenges since such networks are not typically standard components in design libraries. This places a heavy reliance on the designer's expertise to craft custom solutions. To tackle this challenge, we propose a design methodology grounded in mathematical loss analysis, utilizing transducer gain (G_T) that accounts for parasitic impedance to evaluate the MN. This approach shifts away from traditional metrics such as power gain [60] and S_{11} parameters of ideal lossless MNs [56], aiming to enhance both output power and efficiency.

The mmWave path in our proposed design is concise, consisting only of a double-balanced RF mixer and a two-stage PA with a transformer-based matching network. This streamlined design efficiently covers the 25-30 GHz frequency range, achieving remarkable performance metrics. These include a low RMS phase error ranging from 0.63° to 0.84°, minimal PS-induced RMS gain error between 0.021 and 0.046 dB, and an RMS gain control-induced phase error

from 0.30° to 0.64°. The overall TX demonstrates a peak efficiency of 24.1%, with an area efficiency of 0.26 mm² per element. These results highlight the potential of our design to deliver high performance in a compact form factor, making it well-suited for modern, high-frequency communication systems.

In the realm of RF phased array, achieving optimal performance requires not only efficient TX but also a robust antenna system. The antenna array is crucial as it is responsible for achieving high antenna gain and wide bandwidth, essential for effective signal transmission and reception in modern communication systems [65]. However, the integration of antenna arrays with TX IC presents significant challenges, particularly when dealing with large arrays. These challenges stem primarily from stringent substrate requirements and structural complexities that can impede seamless integration.

Previously, various methods have been explored to address these integration challenges. One common approach has been the use of subminiature push-on micro (SMPM) connectors. While these connectors facilitate the connection between the antenna and the TX IC, they introduce interconnection losses, typically around 6 dB [44]. Such losses can significantly degrade the overall system performance by reducing the effective power delivered to the antenna. Another approach has involved transmission-line-based connections, as proposed in [45]. However, this method has been limited in its effectiveness, achieving a bandwidth of only 2 GHz at the simulation level. This limitation restricts the system's ability to handle broader frequency ranges, which are increasingly demanded in modern communication applications.

To overcome these limitations, our work introduces a solution in the form of a co-optimized flipped patch antenna array. This design is paired with an on-board matching network, a strategic combination that aims to enhance the system's performance. The on-board MN is engineered to provide high bandwidth and compact size, addressing the space constraints commonly associated with large antenna arrays. Additionally, this configuration is designed to compensate for parasitic effects introduced by bonding wires, which can otherwise adversely affect signal integrity and performance.

In addition to the RF integrated circuits, the antenna array is explored as a standalone circuit to achieve high antenna gain and wide bandwidth [65]. Nevertheless, stringent substrate requirements and structural complexities hinder integration with the TX IC, particularly in large arrays. Previous methods, such as utilizing subminiature push-on micro (SMPM) connectors, have resulted in interconnection losses of approximately 6 dB [44]. Another method involving transmission-line-based connections, proposed in [45], was limited to a bandwidth of only 2 GHz at the simulation level. In this work, we introduce a co-optimized flipped patch antenna

array paired with an on-board matching network, designed to offer high bandwidth, compact size, and the ability to compensate for parasitic effects from bonding wires.

What is more, phase-locked loops (PLLs) play a crucial role in providing low-jitter clock generation. These clocks are crucial for maintaining high signal integrity, especially when supporting advanced modulation schemes such as 256 QAM for 5G transceivers or 1024 QAM for sub-6-GHz bands. In these scenarios, it is imperative to maintain the RMS LO jitter below 100 fs to ensure reliable performance [66–69]. Additionally, as communication systems increasingly rely on large-scale phased-array beamformers, there is a pressing need for PLLs that not only deliver exceptional performance but also have a small footprint to facilitate seamless system-level integration [70].

In the realm of integer-N PLLs, designers focus on several key aspects to optimize performance. These include developing a voltage-controlled oscillator (VCO) with an improved phase noise (PN) to power tradeoff, balancing the PN contributions from the reference and the VCO, and minimizing in-band PN from loop components. Sub-sampling PLLs (SSPLLs) have emerged as a preferred solution for achieving these objectives [71]. The high-gain sub-sampling phase detector (SSPD) used in SSPLLs significantly reduces PN from subsequent stages, making them particularly effective in managing phase noise [72–75].

In the millimeter-wave frequency range, analog SSPLLs have demonstrated remarkable jitter-power figures of merit (FoM), achieving values better than -250 dB [76, 77]. Despite these achievements, the performance of the conventional SSPLL architecture is still hampered by several limitations. These include the requirement for substantial chip area, significant in-band phase noise from the sub-sampling charge pump (SSCP) and stability resistor, and insufficient robustness in phase noise performance.

Figure 3.2 offers a succinct overview of the phase noise and area efficiencies of commonly used SSPLL architectures. The Type-II SSPLL, depicted in Figure 3.2(a), maintains a substantial gain from the SSPD (A_{SSPD}). This gain allows for reduced contributions from the SSCP (G_{mSSCP}), loop filter, and VCO (K_{VCO}) to the overall phase noise. However, the reduced loop-filter gain necessitates the use of a small stability resistor R_{int}, which in turn requires a large loop filter capacitor C_{int} to maintain adequate phase margin. In practice, an even larger C_{int} is necessary due to the second-order loop dynamics. Moreover, the thermal noise generated by R_{int} is a significant consideration in the phase noise profile. In summary, while Type-II SSPLL architecture offers certain advantages, it is constrained by the need for bulky loop filter capacitance and noticeable in-band phase noise arising from the integration resistor and SSCP. These constraints highlight the ongoing challenges in PLL design, particularly the trade-offs between

achieving low phase noise and minimizing chip area.

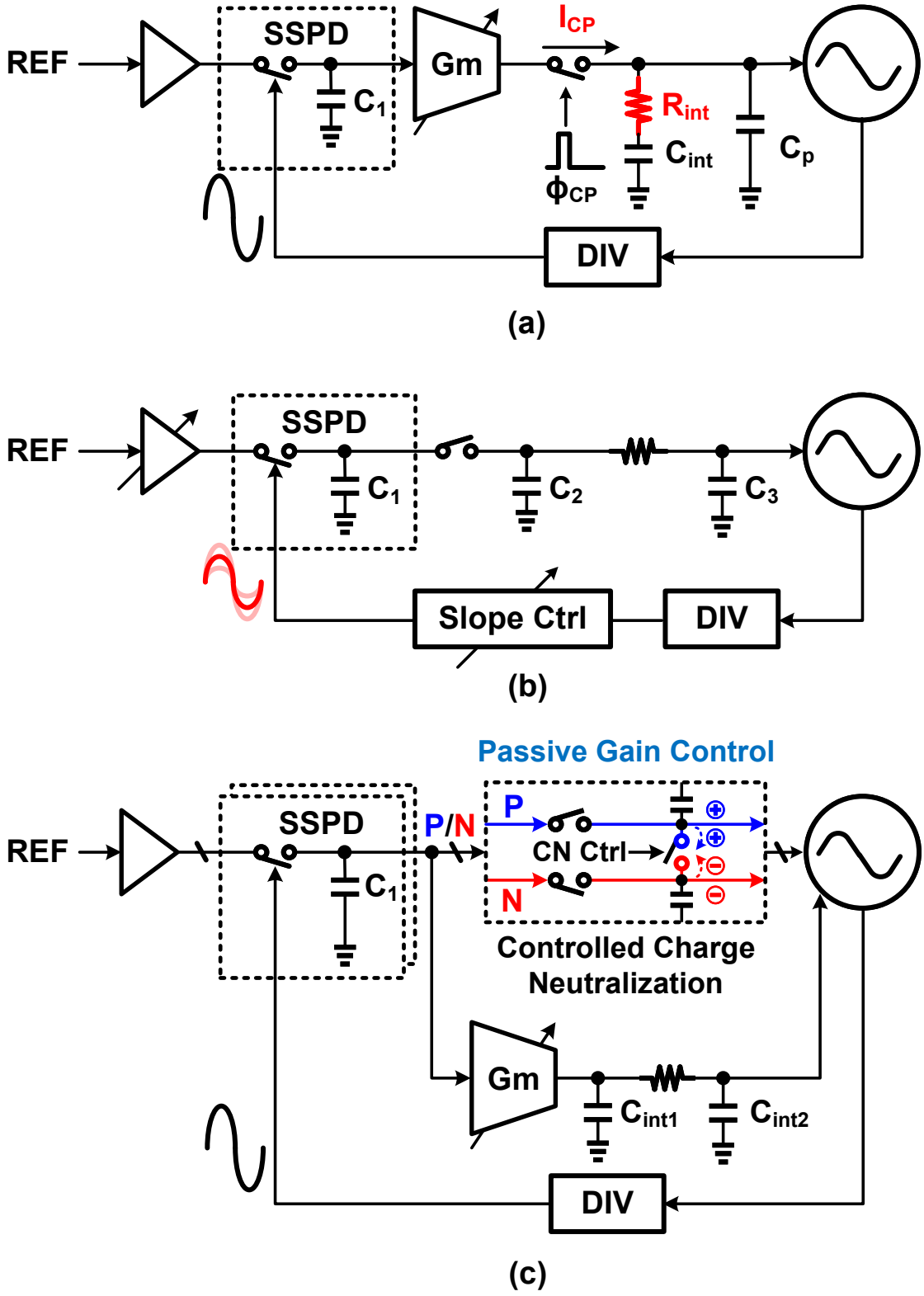


Figure 3.2: Review and comparison of
different SSPLL architectures, including (a) type-II, (b) type-I, and (c) the proposed DPSSPLL.

An alternative with enhanced area efficiency is the Type-I phase-locked loop (PLL) architecture, as illustrated in Figure 3.2(b). This architecture is advantageous as it allows for the use of small capacitance levels, measured in fF, within the SSPD and loop filter [78–83]. Additionally, the Type-I PLL supports passive implementations that leverage switched-capacitor-based loop components. This design choice avoids the extra power consumption and noise that are typically introduced by active circuits or stability resistors. However, the Type-I architecture does present certain challenges. One significant issue is that the gain of the SSPD heavily depends on the initial free-running frequency of the voltage-controlled oscillator (VCO). An offset between the target locking frequency and the free-running frequency can lead to deviations in the sampling point, causing a reduction in the SSPD gain. This reduction can destabilize the loop bandwidth and increase phase noise (PN). Moreover, in fully passive Type-I loops that lack a charge pump, controlling the loop bandwidth relies on a slope-controlled circuit, either in the feedback or reference path. The smooth slope produced by this circuit increases the windows for noise up-conversion, thereby degrading the overall phase noise.

To address these issues, a dual-path (DP) architecture is utilized, featuring a low-noise switched-capacitor-based proportional path (P-Path) and a narrow-band integration path (I-Path), as shown in Figure 3.2(c). The I-Path provides significant DC gain, ensuring a nearly constant SSPD gain, which allows the P-Path to maintain robust gain, bandwidth, and phase noise performance even in the presence of initial frequency offsets [84–87]. A low-noise charge-domain gain control scheme is introduced into the P-Path, designed to be compatible with the all-passive switched-capacitor setup. By leveraging the differential configuration of the P-Path, gain control is achieved by partially neutralizing the charge between the positive (P) and negative (N) sides in a controlled manner. This innovative approach achieves a wide 30-dB gain control range with minimal additional phase noise. Comprehensive analysis is carried out to characterize the frequency response and noise transfer behavior of the proposed switched-capacitor network. The proposed PLL achieves a compact core area of just 0.057 mm², enabled by a space-efficient I-Path loop filter and the use of an inductorless true single-phase clock (TSPC) divider as the prescaler and VCO buffer.

This chapter is organized to provide a thorough exploration of the phased array TX, especially the RF chain. Section 3.2 delves into the architecture of the phased-array TX system, examining its design and operational principles. Section 3.3 focuses on the design of critical circuits within the system, categorized into IF integrated circuits, RF integrated circuits, and RF on-board circuits. These sections detail the specific technologies and methodologies employed to optimize performance across different frequency bands. Section 3.4 presents the experimental

results for each component and the overall system, offering empirical validation of the design choices and their effectiveness in real-world applications. Finally, Section 3.5 provides a concise summary of the findings.

3.2 Architecture Design

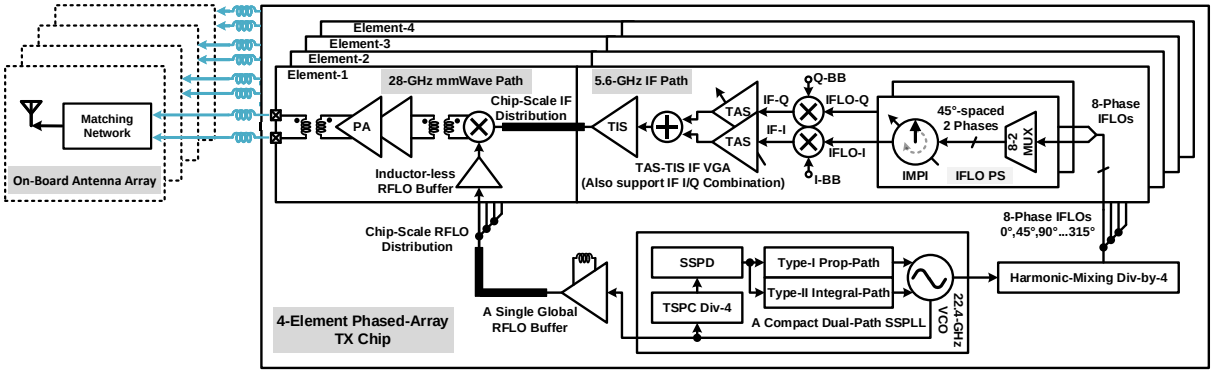


Figure 3.3: Complete system diagram of the proposed 4-element phased-array transmitter.

The proposed transmitter architecture, depicted in Figure 3.3, integrates several advanced components to achieve efficient frequency generation and signal processing. Central to this design is a phase-locked loop (PLL) equipped with a divider for generating both RF and IF local oscillators (LOs). The PLL synthesizes a 22.4-GHz RFLO using a compact dual-path subsampling PLL, which is then distributed to four RF mixers via inductor-less RFLO buffers. This architecture ensures minimal power consumption and high signal integrity. The RFLO is further divided by a factor of four using a harmonic-mixing injection-locked frequency divider (ILFD), resulting in eight equally spaced IFLO phases at 45-degree intervals (PH-0°, 45°…315°).

In the intermediate frequency (IF) path, an 8-to-2 phase multiplexer (mux) is followed by an integration-mode phase interpolator (IMPI), creating a highly linear phase shifter. This IFLO phase shifter interpolates among the eight phases generated by the ILFD to produce the IFLO-I and Q signals. These signals are then mixed with baseband signals using a double-balanced passive mixer, generating the IF-I and Q signals. A transadmittance-transimpedance (TAS-TIS) IF variable gain amplifier (VGA) first amplifies the IF-I/Q signals, then combines them, and finally distributes the combined signal to the RF mixers. This approach enhances the signal strength and ensures a seamless transition from IF to RF.

In the RF path, the 5.6-GHz IF signals are upconverted to a 28-GHz RF signal, which is subsequently amplified by a power amplifier (PA) before being delivered to the off-chip antenna.

This process ensures that the transmitted signal maintains high fidelity and sufficient power for effective communication.

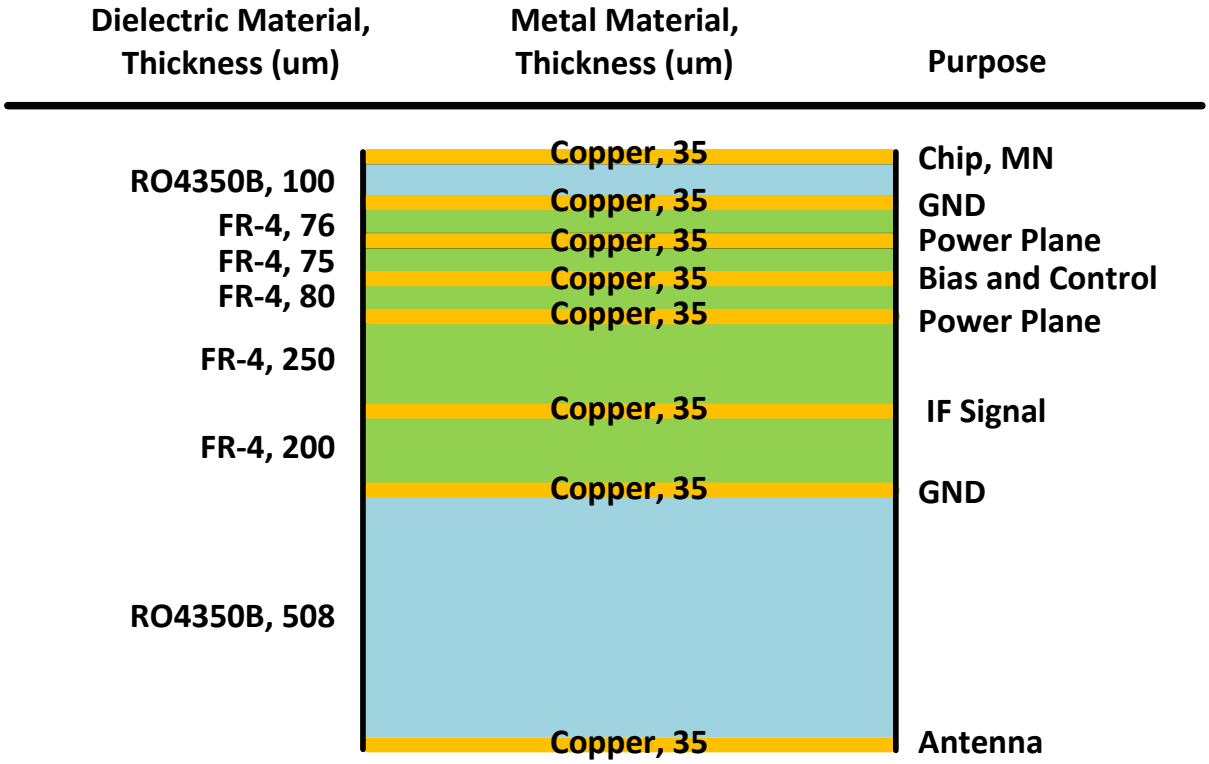
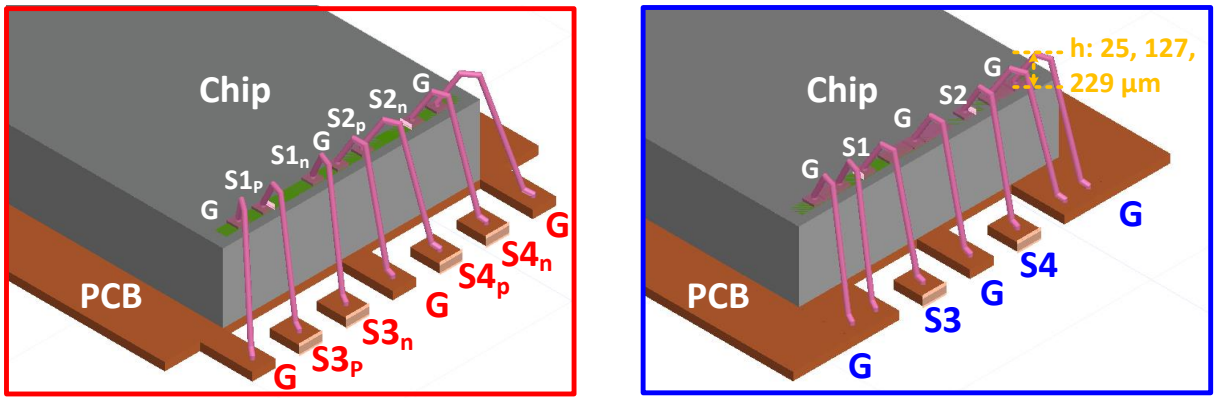


Figure 3.4: PCB layer stack-up featuring two low-loss dielectric layers.

Figure 3.4 illustrates the stack-up of a cost-effective and lightweight printed circuit board (PCB) designed to support the transmitter system. The PCB features only two low-loss dielectric layers, optimizing material costs while ensuring efficient signal propagation. The microstrip antenna array is fabricated on the bottom layer, while the integrated chips are mounted on the top metal layer. The power plane, along with bias and control signals, is distributed across five interlayers, providing a robust electrical framework. Bonding wires are used to connect the chips to the PCB, chosen for their flexibility and cost-effectiveness. However, these wires introduce inductance in the hundreds of picohenries, which can lead to load mismatches. To counteract this, PCB matching networks are meticulously designed to minimize signal reflection and ensure effective power transfer from the on-chip PA to the antenna array.



(a) (b)

Figure 3.5: 3D representations of bonding wire configurations: (a) GSSG (ground-signal-signal-ground) and (b) GSG (ground-signal-ground).

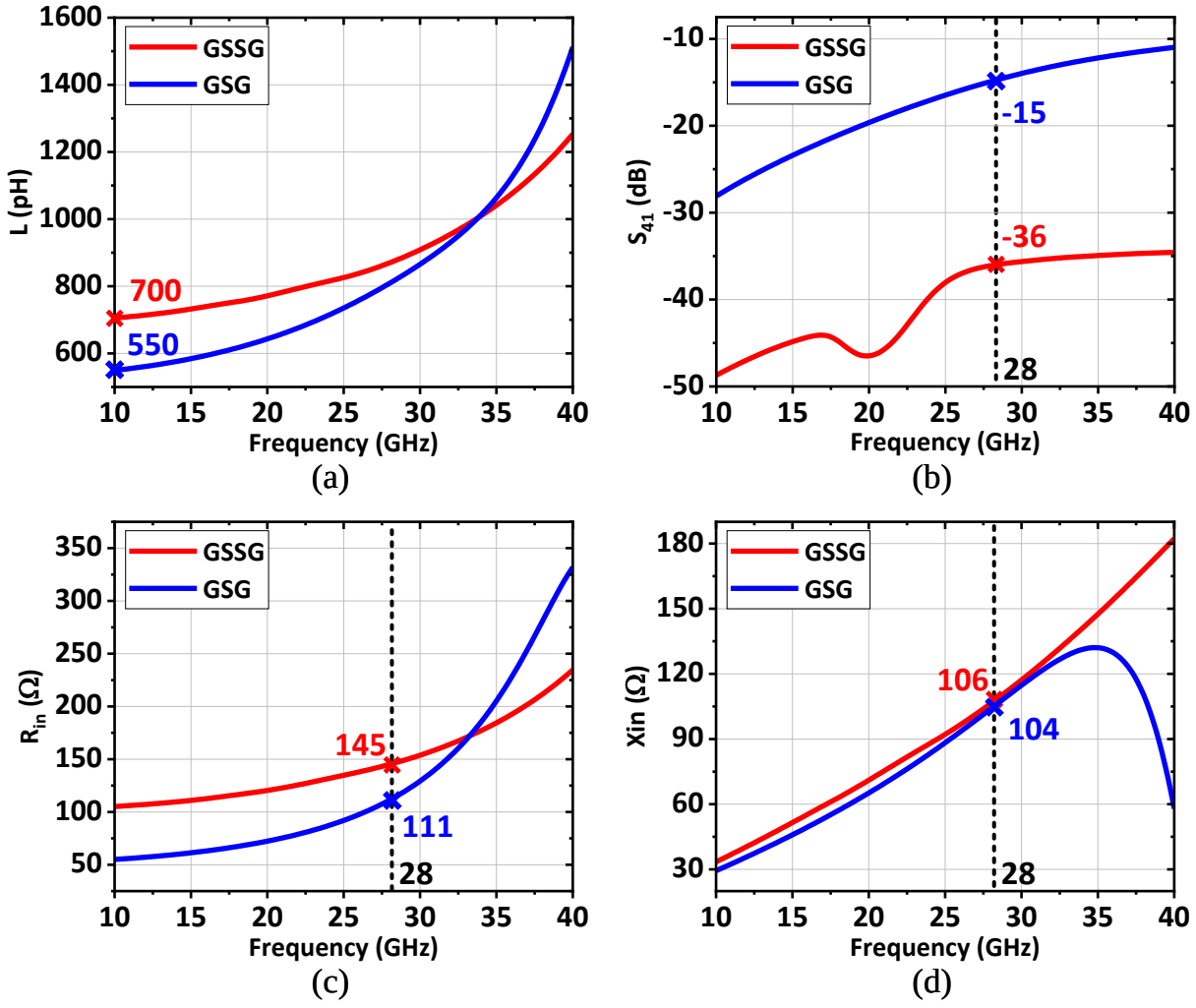


Figure 3.6: EM simulation results for GSSG and GSG bonding wires: (a) inductance values, (b) coupling coefficients between adjacent elements, (c) input resistances, and (d) input reactances.

In standalone transmitters, a single-ended output from the PA simplifies the connection to the antenna. However, in phased array systems, which feature densely packed routing strip lines and

numerous elements, coupling between adjacent elements can significantly affect performance. To address this issue, the transmitter employs a differential output configuration for the PA. This configuration mitigates coupling by utilizing a bonding wire arrangement labeled as "GSSG" for differential outputs and "GSG" for single-ended outputs, as depicted in Figure 3.5.

Electromagnetic (EM) simulation results, shown in Figure 3.6, reveal that using differential bonding wires improves coupling between adjacent elements from -15 dB to -36 dB at 28 GHz. Although the inductance of differential bonding wires increases by 27% compared to the single-ended configuration—rising from 550 pH to 700 pH—the input impedances of both setups remain closely aligned. This alignment is attributed to the reduced coupling capacitance in the differential configuration, which results in similar performance of the subsequent matching network. This careful design consideration ensures that the phased array system maintains high performance, with minimal interference and optimal signal transmission.

3.3 Key Building Blocks Design

This section delves into the detailed design of critical circuits, categorized into IF integrated circuits, RF integrated circuits, and RF on-board circuits. IF integrated circuits serve as the crucial intermediary, managing signal processing between the baseband and RF stages through amplification and phase shifting. RF integrated circuits are responsible for high-frequency operations, incorporating RF mixer and power amplifier that is designed to deliver high output power, efficiency, and linearity. Meanwhile, RF on-board circuits focus on interfacing with the antenna array, ensuring effective signal transmission while addressing key considerations like layout and bandwidth limitations. Collectively, these circuits form the backbone of a robust communication system, with each category meticulously engineered to satisfy the demands of modern high-performance technologies.

3.3.1 Intermediate-Frequency Integrated Circuits

Phase Shifter

Figure 3.7 presents the block diagram of an IFLO phase shifter, which offers a 7-bit resolution for precise phase adjustments. The phase-shifting process begins with an injection-locked frequency divide-by-4 (ILFD) circuit, which adeptly divides the 22.4-GHz RFLO signal to produce eight IFLO phases, evenly spaced at 45-degree intervals, at a frequency of 5.6 GHz. This division is crucial for creating a manageable frequency that can still effectively drive the subsequent IF

paths.

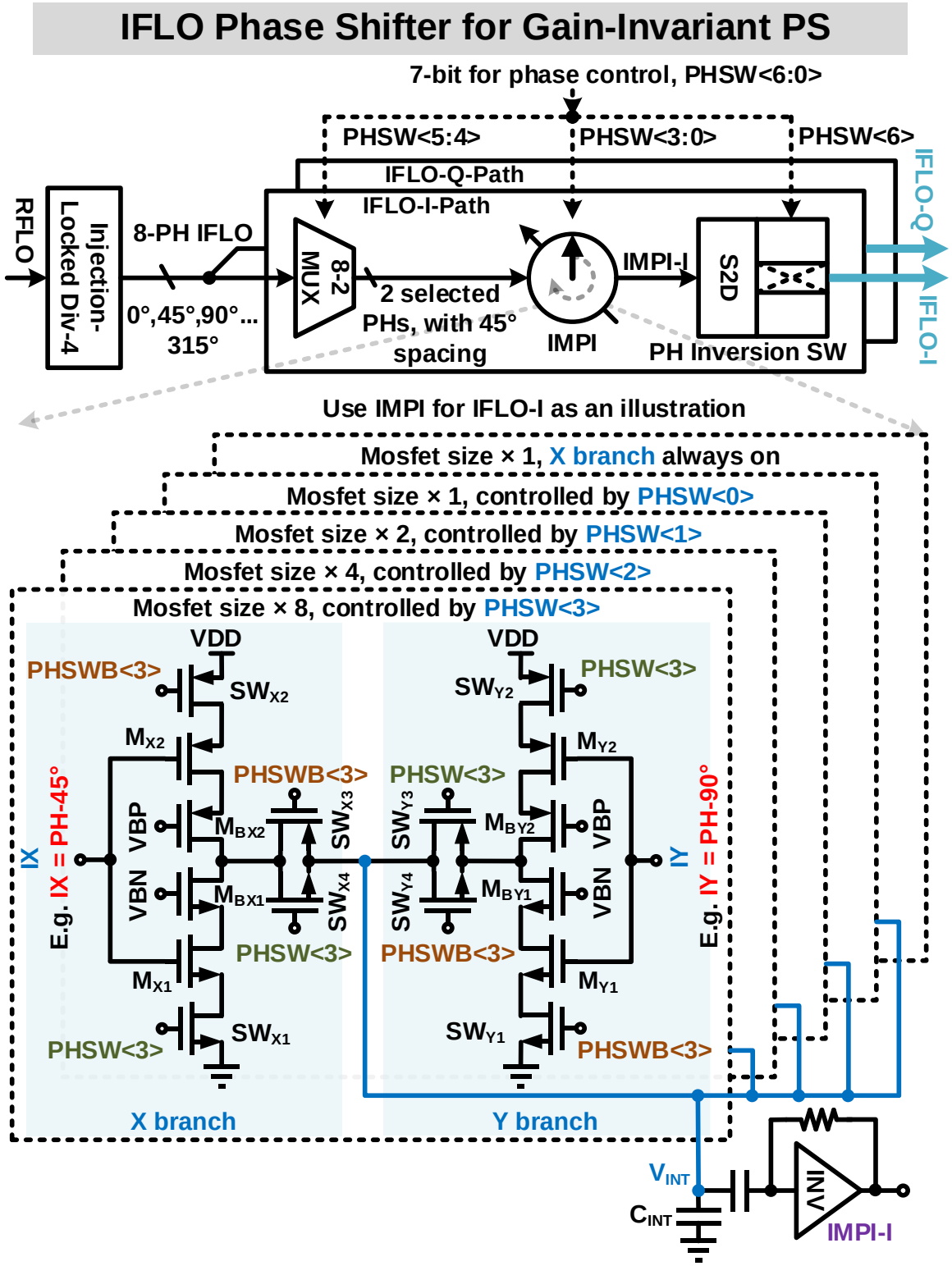


Figure 3.7: Block diagram of the proposed IFLO phase shifter and topology of the IMPI.

The IFLO phase shifter is designed with two primary paths: the IFLO-I-path and the IFLO-Q-path. Each path is equipped with a phase shifter composed of three main components: a 1-bit

phase inverter, a 2-bit phase mux, and a 4-bit integration-mode phase interpolator (IMPI). The phase inversion switch is governed by the most significant bit, PHSW<6>, and enables a 180-degree phase shift, providing the initial coarse adjustment needed for efficient phase modulation. Following this, the 8-to-2 phase multiplexer, controlled by PHSW<5:4>, selects a pair of neighboring phases from the eight produced by the ILFD. These selected phases are then directed into the X and Y branches of the 4-bit IMPI, setting the stage for fine-grained phase interpolation.

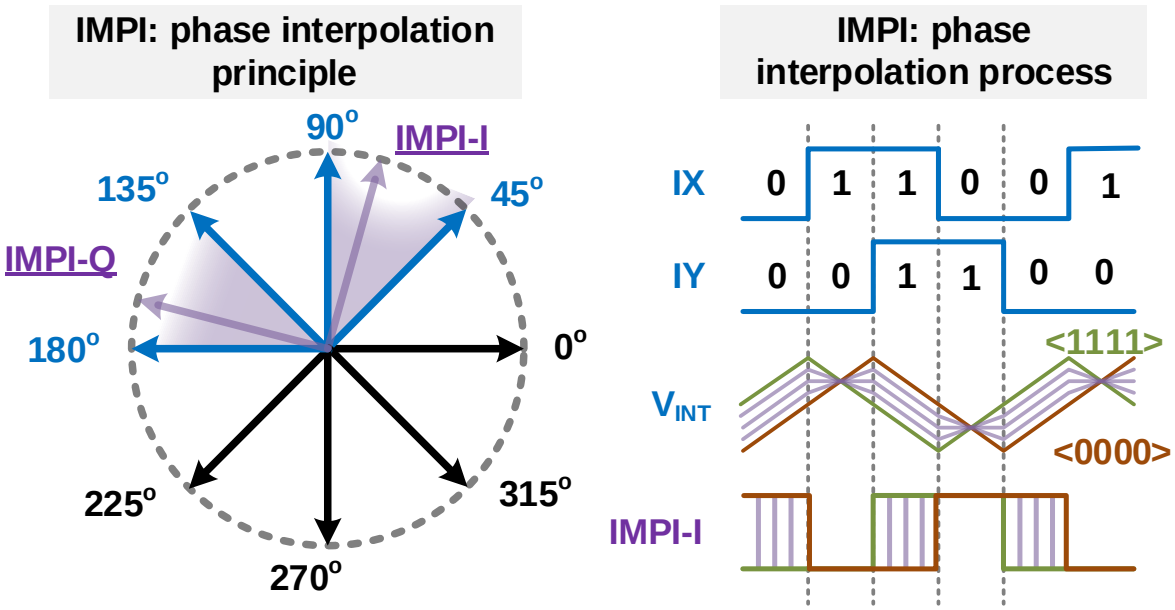


Figure 3.8: Phase interpolation principle and process.

The IMPI is a critical component that further refines the phase of the signal with a resolution of 2.875°, ensuring precision in the phase output. It comprises five segments, one fixed and four that are binarily ratioed and switchable, as depicted in Fig. 3.8. Each segment features an X branch and a Y branch, with control provided by PHSW<3:0>. In each segment, only one of the branches is activated at a time to charge the integration capacitor, C_{INT}. By adjusting the number of active branches in the four switchable segments, a linear phase shift is applied to the integrated signal, V_{INT}. This approach allows for highly accurate control over the phase adjustment.

Once the desired phase shift is achieved, an inverter-based comparator converts the V_{INT} signal into $IMPI_{OUT}$, ensuring a rail-to-rail voltage swing. This output is then transformed into a differential IFLO signal, which is crucial for driving the subsequent IF passive mixer. The differential signaling helps reduce noise and enhances the overall signal integrity, ensuring that the phase-shifted signal maintains its fidelity through to the next stages of processing.

Variable Gain Amplifier

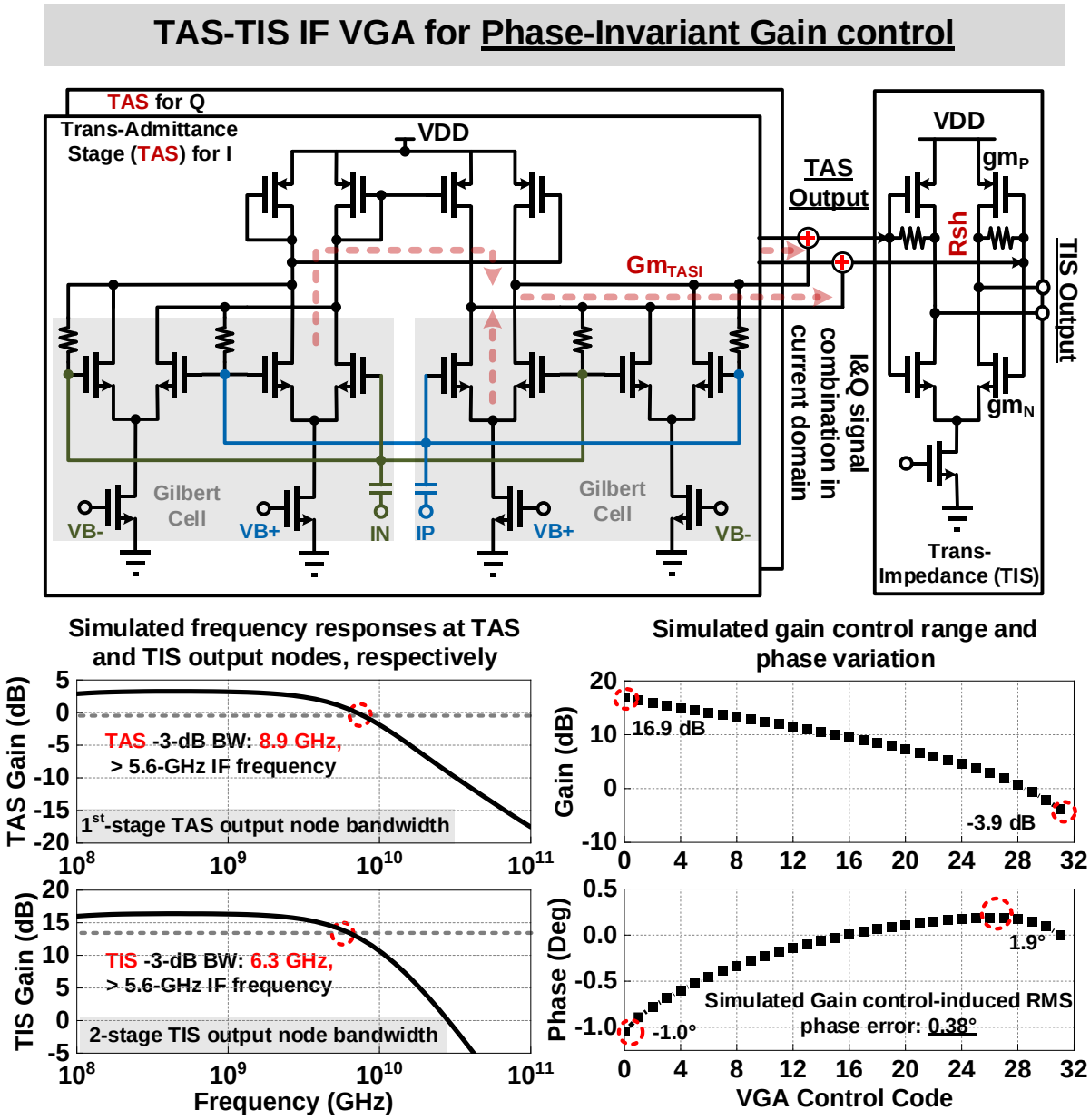


Figure 3.9: IF VGA topology, simulated frequency responses, gain control range and phase variation versus control code.

The TAS-TIS IF VGA, depicted in Fig. 3.9, is designed to maintain consistent phase characteristics across various gain levels while combining I/Q IF signals and distributing them efficiently at the chip level. Initially, I and Q-IF signals produced by the passive mixer are transformed into current signals by the first-stage TASs. These current signals are then combined by directly linking the output nodes of the two TASs, leveraging Gilbert-cell architectures within the TASs to enable adjustable gain control.

The subsequent stage features a TIS that presents a low impedance, calculated as R_{sh} divided by Gain_{TIS}, to the output node of the TAS, ensuring a broad node bandwidth of 8.9 GHz, as demonstrated in Fig. 3.9. This extensive bandwidth minimizes the effect of nonlinear parasitic capacitance changes within the Gilbert cells during the gain adjustment process, thus maintaining phase stability. The TAS's transimpedance, approximately 1 kΩ (R_{sh}), supports a maximum gain of 16.9 dB. Additionally, the TIS is characterized by a low output impedance, calculated as $1/(\text{gm}_\text{P} + \text{gm}_\text{N})$, which facilitates an overall VGA bandwidth of 6.3 GHz.

In post-layout simulation, the innovative TAS-TIS IF VGA achieves a gain tuning range of 20 dB, with a minimal phase error of 0.38° RMS induced by the VGA. This expansive bandwidth not only ensures minimal phase variation but also enhances the efficiency of distributing IF signals across the chip from the IF path to the RF mixer. This feature is crucial for maintaining signal integrity and performance in high-frequency applications, thereby advancing the capabilities of wireless and optical communication systems.

3.3.2 Radio-Frequency Integrated Circuits

In RF integrated circuits, the architecture typically comprises a RF front-end that processes the signal chain and an RF PLL to generate a low-jitter LO signal. The design of the RF front-end in this context is particularly noteworthy for its inclusion of a mixer, which is engineered to upconvert signals from the IF to RF. This mixer is strategically paired with a PA that is characterized by its high power density, ensuring that the system can handle robust signal amplification. Achieving high output power from the mixer is critical, as it ensures the PA is effectively saturated, maximizing its efficiency and performance.

After the signal is upconverted by the mixer, it passes through a two-stage power amplifier. This configuration is meticulously designed to deliver both high gain and significant output power, thereby ensuring that the signal maintains its integrity and strength throughout the transmission process. Interconnections within this system are facilitated by transformers (XFs), which play a crucial role not only between the mixer and the PA but also between the PA and the final output. These XFs are essential for optimizing signal transfer and ensuring minimal losses, contributing to the overall efficiency of the RF front-end.

To make the system suitable for implementation in a phased array, a gain extension scheme is employed. This strategy, in conjunction with XFs that boast a high coupling coefficient, enhances the linearity, efficiency, and output power of the system. Importantly, these improvements are achieved without incurring additional area costs, making the design efficient in terms of both

performance and space.

To further optimize the performance, particularly focusing on the bandwidth of the PLL, an innovative charge-neutralization-based switched-capacitor gain control circuit is introduced. This circuit harnesses the differential configuration of the type-I path, setting it apart from traditional methods that rely on slope-controlled circuits or charge pumps. The proposed approach offers a broad control range while contributing minimally to in-band phase noise, which is essential for maintaining signal integrity and stability.

Moreover, the system features a proportional-integral dual-path architecture. This architecture is complemented by an inductor-less TSPC divider within the feedback path, facilitating a more compact design. The absence of inductors simplifies the circuit layout and reduces the overall size, which is beneficial for integrating into space-constrained environments like phased arrays. This architectural choice not only streamlines the implementation but also enhances the robustness and reliability of the PLL, ensuring precise frequency control and minimal jitter.

Mixer

In this design, the absence of a VGA between the mixer and the PA necessitates that the RF mixer itself delivers substantial gain and a robust P1dB. To fulfill these requirements, the proposed RF mixer departs from traditional configurations by eliminating the tail current source. Instead, it utilizes a pair of current mirrors configured through an R-C-R network to effectively bias the MOSFETs at the input of the IF signal, as depicted in Figure 3.10. This innovative biasing technique significantly enhances the dynamic range of the mixer output, extending it by approximately 0.2 V.

Additionally, to further improve the P1dB, a XF is strategically employed to ensure optimal impedance matching. The XF matches the input impedance of the PA with the output impedance of the mixer, which is crucial for maximizing power transfer and minimizing signal reflections. This transformer, denoted as XF_1, also serves an additional purpose: it resonates with the parasitic capacitance at the mixer output. This resonance not only boosts the power gain but also effectively suppresses the IF image signal, thereby enhancing the overall signal quality and efficiency of the RF front-end.

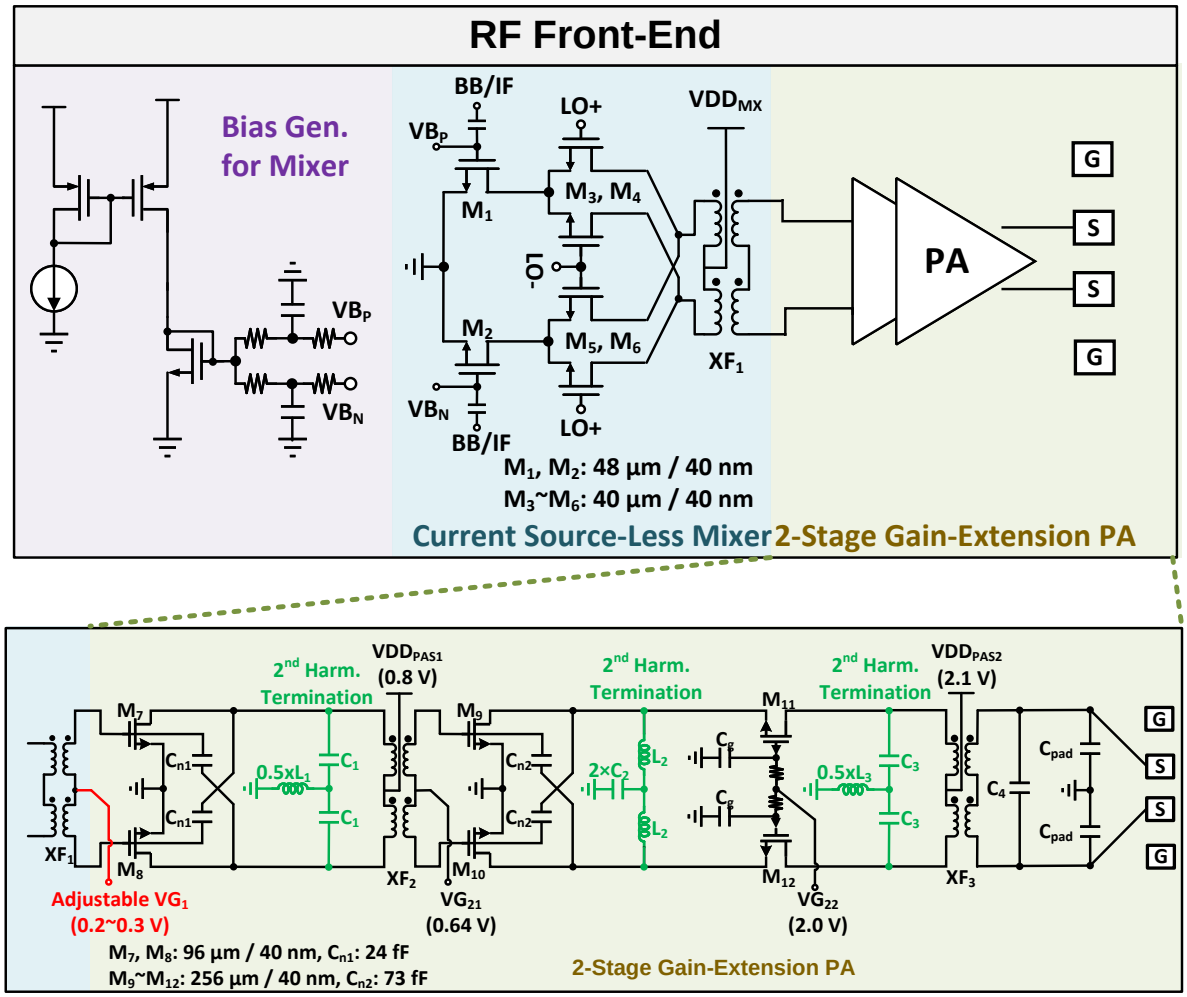


Figure 3.10: Schematic of the RF front-end incorporating a current source-less mixer and a two-stage power amplifier.

Power Amplifier

Active Stage Design of the 2-Stage PA The schematic of the proposed two-stage PA, along with its relevant parameters, is illustrated in Figure 3.10. In this design, a stacking structure is implemented in the second stage to boost the output power, bypassing the need for multiple paths typically combined using large passive networks. The stacking approach effectively doubles the output swing which is limited by the breakdown voltage of the MOSFET. This second stage is biased in class AB operation to achieve a balance of high output power and superior linearity.

Nevertheless, a challenge arises with the stacked PA: its gain rapidly compresses as the input power increases, particularly at high input levels. The gray curve in Figure 3.11 shows the simulated gain of the second stage, highlighting a P1dB of only 14.2 dBm. To address this issue and improve linearity, a class C first stage with adjustable bias voltage is introduced. By operating the MOSFETs in a partially on state at lower input levels, gain peaking is induced, which compensates for the gain compression observed in the second stage.

The circuit schematic of the proposed 2-stage PA with corresponding parameters is shown in Fig. 3.10. Stack structure is utilized in the second stage to increase the output power instead of combining several paths by the area-hungry passive networks. The stacking method doubled the output swing which is limited by the breakdown voltage of the MOSFET. This stage is biased in class AB for getting high output power and high linearity.

Simulated gains for the first stage and the overall PA, utilizing three different bias voltages for the first stage (VG_1), are presented in Fig. 3.11. With a lower VG_1, the total gain is primarily influenced by the gain peaking of the first stage and induces an additional P1dB at lower power level. Conversely, at higher VG_1 values, the total gain is dominated by the gain compression of the second stage. An optimal VG_1 of 0.32 V achieves a flat total gain and maximizes the P1dB.

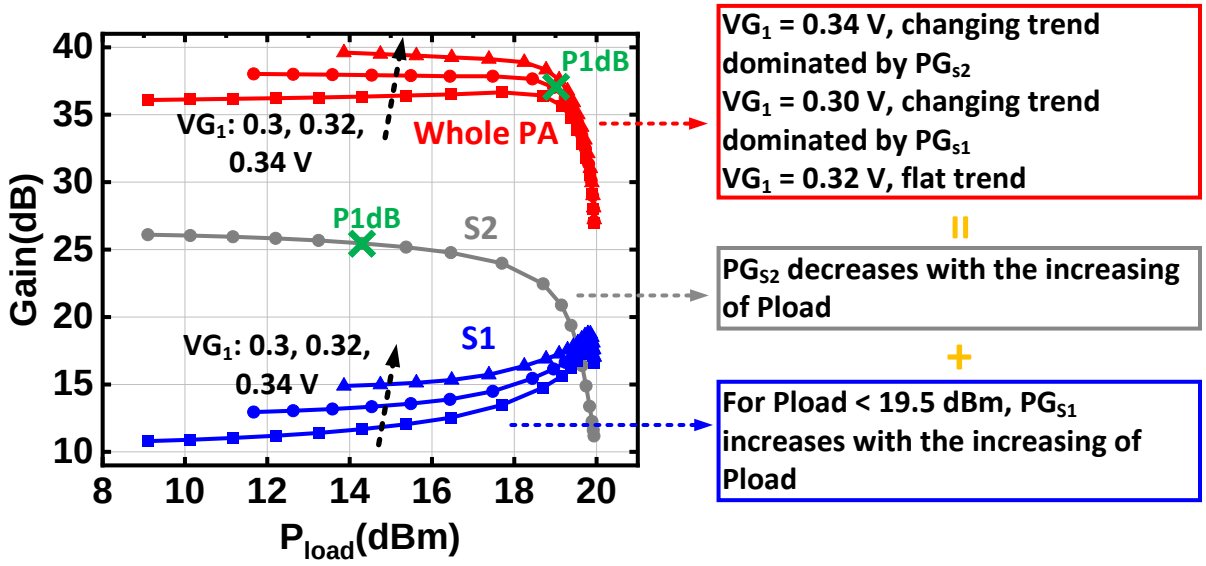


Figure 3.11: Simulated gains for class C first stage (S1), class AB second stage (S2), and the whole PA with VG_1 varying from 0.30 V to 0.34 V.

Furthermore, to enhance the stability of the PA, neutralization capacitors (C_{n1}, C_{n2}) are incorporated in both stages. These capacitors play a crucial role in stabilizing the amplifier by counteracting potential parasitic feedback. Additionally, second-order terminations are utilized in each stage to mitigate second-order harmonic feedback, which may be introduced due to the presence of neutralization capacitors. This strategic implementation not only improves linearity but also boosts the overall efficiency of the PA.

Passive XF-Based MN Design of the 2-Stage PA To efficiently facilitate power transfer to the 100-ohm load at the differential output of the PA, the implementation of MNs is crucial. These MNs are strategically placed between the second and first stages and between the second stage and the load. The choice of using XFs in these networks is particularly advantageous due to

their capability to perform impedance scaling, provide both AC and DC decoupling, and enable differential outputs, which are essential for preserving signal fidelity and minimizing loss in high-frequency applications.

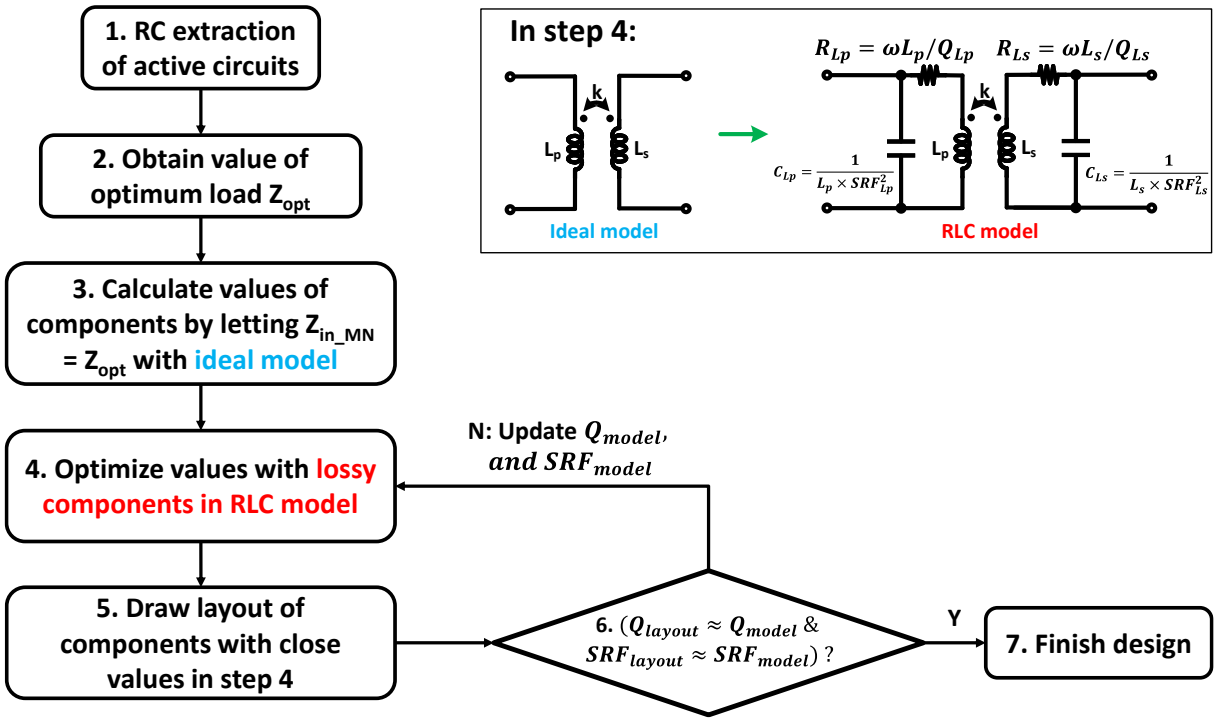


Figure 3.12: Design flow of the passive XF-based MN.

Figure 3.12 illustrates the proposed design methodology for the XF-based MN. The initial phase of this methodology involves the first three steps, which are centered on determining the initial values for three fundamental parameters of the XF: the inductance of the primary coil (L_p), the inductance of the secondary coil (L_s), and the coupling coefficient (k). This is accomplished by setting the input impedance of the MN (Z_{in-MN}), equal to the optimal impedance of the active stage (Z_{opt}). This matching is achieved using an idealized lossless XF model, which simplifies calculations and provides a starting point for further optimizations.

Transitioning into the fourth step, the design shifts from the ideal model to the lossy RLC model. This model includes parasitic elements such as capacitors and resistors, which are crucial for a realistic depiction of the XF's performance in practical scenarios. The parasitic capacitors C_{Lp} and C_{Ls} are defined by their self-resonant frequencies SRF_{Lp} and SRF_{Ls}, respectively. Similarly, the parasitic resistors R_{Lp} and R_{Ls} are characterized by their quality factors Q_{Lp} and Q_{Ls}. In this stage, self-resonant frequencies and quality factors are treated as fixed constants, typically 50 GHz and 20, respectively, to ensure that the model aligns with expected performance benchmarks.

In step 5, the focus moves to the layout development, where the goal is to closely match

the layout with the optimized parameters from the previous steps. Step 6 involves extracting constants from the layout and comparing them with those predetermined in step 4. If there are notable discrepancies, the constants are revised to better reflect the layout's actual values. This iterative refinement process—encompassing steps 4 through 6—continues until the extracted constants align with the optimized values, ensuring accuracy and effectiveness in the final design.

Step four, the optimization phase, stands out as the most complex and will be detailed further. This step involves specific optimization objectives and the calculation of initial values, both of which are integral to achieving the design targets and addressing loss analysis in the MN. By focusing on these aspects, the final XF-based MN design is poised to meet the rigorous demands of high-frequency PA applications. The strategic design and iterative refinement ensure that the MNs deliver exceptional performance, supporting the overall functionality and reliability of the PA in demanding operational environments.

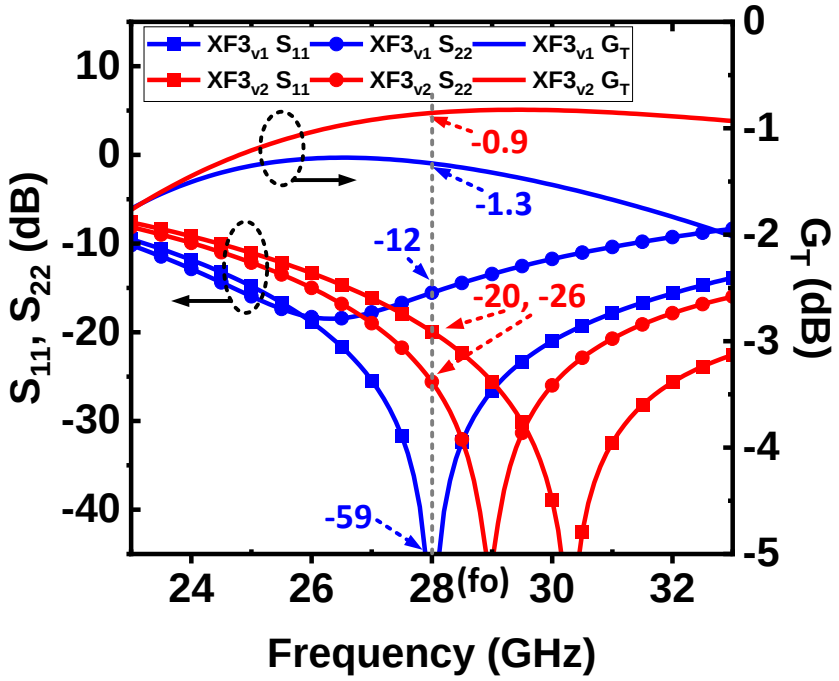


Figure 3.13: S-parameter and transducer gain G_T simulation results for the S_{11}-optimized transformer design $XF3_{v1}$ and G_T-optimized transformer design $XF3_{v2}$.

Design Target The MN plays a pivotal role in RF circuit design, particularly because the optimal impedance (Z_{opt}) of the active stage often differs from the load impedance. This discrepancy necessitates a meticulously designed MN to achieve the desired matching conditions at the input port, denoted by S_{11}. The reference impedance at the MN's input port (port 1) is set as the conjugate of Z_{opt}, whereas the reference impedance at the output port aligns with the load impedance. Achieving this alignment is covered in the third step of the design process, involv-

ing the calculation of component values using an ideal model. In this scenario, the network is assumed to be passive and lossless, rendering the S-parameter matrix unitary. Thus, when port 1 is perfectly matched, port 2 achieves perfect matching as well.

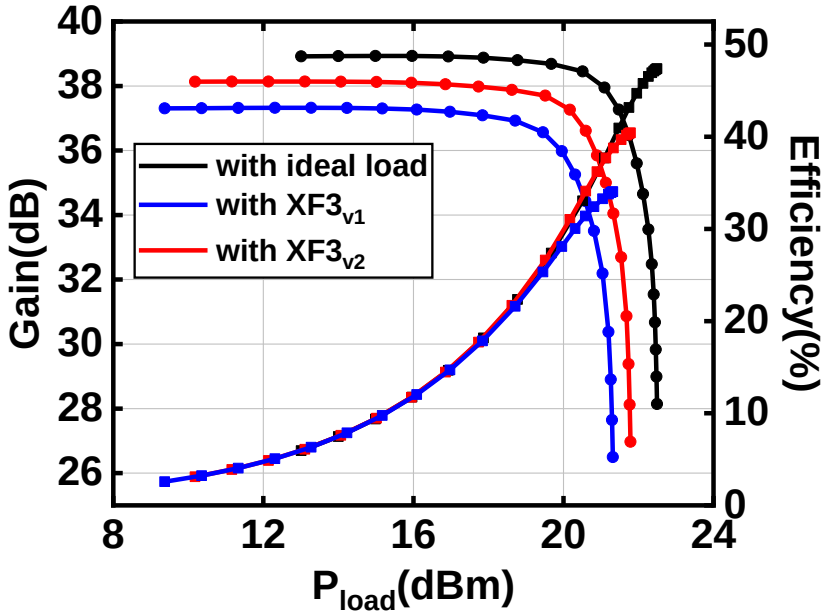


Figure 3.14: Gain and efficiency simulation results for a two-stage power amplifier incorporating $XF3_{v1}$ and $XF3_{v2}$.

However, transitioning from an ideal, lossless model to a practical, lossy RLC model introduces complexities that make S_{11} alone insufficient for a comprehensive understanding of matching conditions. Instead, the transducer gain (G_T) becomes a more suitable metric for evaluating the MN's performance. G_T is defined as the ratio of the power delivered to the load (P_L) to the power available from the source (P_{avs}), taking into account both source and load impedances. This parameter is commonly used to indicate the amplification capability of active devices. However, when applied to evaluate losses in a passive network, the value expressed in decibels (dB) will be negative.

The design process incorporates transformers XF_{v1} and XF_{v2}, each with distinct objectives: XF_{v1} focuses on minimizing S_{11}, while XF_{v2} aims to maximize G_T. Figure 3.13 illustrates the simulation results for the S-parameters of these transformers and Fig. 3.14 shows the subsequent gain and efficiency of the PA when utilizing these differing XFs. Table 3.1 provides a comprehensive summary. XF_{v1} achieves an impressive -59 dB for S_{11}; however, S_{22} is comparatively low at -12 dB at 28 GHz. In contrast, XF_{v2} demonstrates superior matching at both ports and achieves a G_T that is 0.4 dB higher than XF_{v1}. This enhancement in transducer gain results in an efficiency increase from 35% to 40% when XF_{v2} is employed. Consequently, maximizing G_T

emerges as the primary optimization goal in step four, as it facilitates improved efficiency—a critical factor in high-performance RF design.

Table 3.1: Summary of parameters and simulation results for the S_{11}-optimized transformer XF_{3_v1} and the G_T-optimized transformer XF_{3_v2}.

	XF_{3_v1}	XF_{3_v2}
Design Target	**Minimize S_{11}**	**Maximize G_T**
L_p (pH)	**272**	**238**
L_s (pH)	**331**	**491**
K	**0.62**	**0.70**
SRF (GHz)	**50**	**50**
S_{11} @ f_o (dB)	**-59**	**-20**
S_{22} @ f_o (dB)	**-12**	**-26**
G_T @ f_o (dB)	**-1.3**	**-0.9**

Focusing on maximizing G_T ensures optimal power transfer and minimizes losses, which are essential for achieving superior efficiency and performance in RF applications. This strategy underscores the importance of considering both active and passive components within the design process, demonstrating how targeted adjustments and optimizations can significantly impact the overall functionality and performance of high-frequency circuits. The iterative and detailed design methodology exemplifies a comprehensive approach to RF design, addressing the intricate balance between performance, efficiency, and practical implementation.

Loss Analysis of XF For an ideal transformer (XF), three key parameters are utilized in its modeling: the inductance of the primary coil (L_p), the inductance of the secondary coil (L_s), and the coupling coefficient (k). To account for losses, parasitic resistors are included in the model, represented as R_{Lp} and R_{Ls} in Fig. 3.15. These resistors are characterized by their quality factors Q_{Lp} and Q_{Ls}. Additionally, parasitic capacitors C_{Lp} and C_{Ls} are incorporated into the model, defined by their self-resonant frequencies SRF_{Lp} and SRF_{Ls}, respectively.

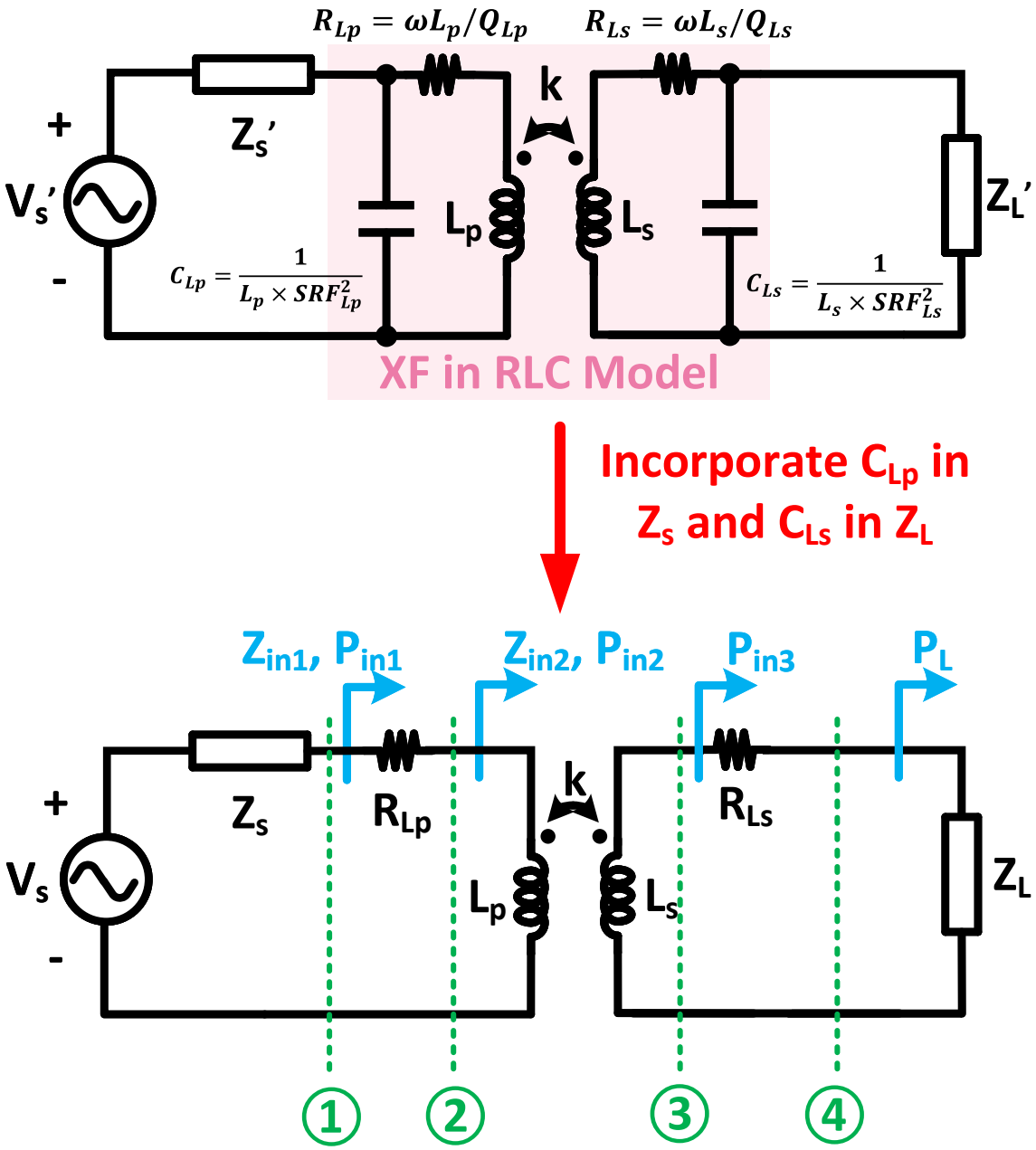


Figure 3.15:
Incorporating parasitic capacitors of XF in source and load impedances for calculating the G_T.

A voltage source V_s' with source impedance Z_s' is employed to supply power, while the load is represented by Z_L'. For simplification of the calculations, the parasitic capacitors are incorporated into the source impedance and the load impedance, respectively. The modified source and load impedances are given by:

$$V_s = V_s' \times \frac{\frac{1}{j\omega C_{Lp}}}{Z_s' + \frac{1}{j\omega C_{Lp}}} \tag{3.1}$$

$$Z_s = Z_s^{'} // \frac{1}{j\omega C_{Lp}} \tag{3.2}$$

$$Z_L = Z_L^{'} // \frac{1}{j\omega C_{Ls}}. \tag{3.3}$$

To evaluate the effect of the XF, G_T as the optimization goal is calculated and analyzed:

$$\begin{aligned} G_T &= \frac{P_L}{P_{avs1}} \\ &= \frac{P_{avs2}}{P_{avs1}} \times \frac{P_{in2}}{P_{avs2}} \times \frac{P_L}{P_{in2}} \\ &= \frac{R_s}{R_s + R_{Lp}} \times \frac{4R_{in2} \times \left(R_s + R_{Lp}\right)}{\left(R_{in2} + R_s + R_{Lp}\right)^2 + \left(X_{in2} + X_s\right)^2} \times \frac{R_L}{R_L + R_{Ls}}, \end{aligned} \tag{3.4}$$

where each impedance (Z_s, Z_{in1}, Z_{in2}, Z_L) comprises a resistor (R_s, R_{in1}, R_{in2}, R_L) and a reactance (X_s, X_{in1}, X_{in2}, X_L). The reactances associated with the coils are denoted as X_{Lp} and X_{Ls}. For example,

$$Z_s = R_s + jX_s \tag{3.5}$$

$$X_{Lp} = \omega L_p. \tag{3.6}$$

In (3.4), G_T is the product of three components. The first and third terms account for the losses induced by the parasitic resistors of the primary and secondary coils, respectively. The second term is contingent upon the impedance matching condition and reaches its maximum value of 1 when

$$R_{in2} = R_s + R_{Lp} \tag{3.7}$$

and

$$X_{in2} = -X_s. \tag{3.8}$$

R_{in2} and X_{in2} are expressed in (3.9) as following:

$$\begin{aligned} Z_{in2} &= R_{in2} + jX_{in2} \\ &= \left(R_L + R_{Ls}\right) \frac{k^2 X_{Lp} X_{Ls}}{\left(R_L + R_{Ls}\right)^2 + \left(X_L + X_{Ls}\right)^2} \\ &+ j\left[X_{Lp} - \left(X_L + X_{Ls}\right) \frac{k^2 X_{Lp} X_{Ls}}{\left(R_L + R_{Ls}\right)^2 + \left(X_L + X_{Ls}\right)^2}\right]. \end{aligned} \tag{3.9}$$

By substituting R_{in2} and X_{in2} into (3.7) and (3.8), the relationship among X_{Lp}, X_{Ls}, and k can be expressed as follows:

$$X_{Ls} = \left(X_s + X_{Lp}\right) \times \frac{R_L + R_{Ls}}{R_s + R_{Lp}} - X_L \tag{3.10}$$

$$X_{Lp} = \frac{k^2 X_{Lp} X_{Ls} \left(X_L + X_{Ls}\right)}{\left(R_L + R_{Ls}\right)^2 + \left(X_L + X_{Ls}\right)^2} - X_s. \tag{3.11}$$

After substituting (3.10) into (3.11), we derive a quadratic equation that establishes the relationship between X_{Lp} and k:

$$0 = \left(k^2 - 1\right) X_{Lp}^2 + \left[X_s\left(k^2 - 2\right) - \frac{R_1}{R_2} k^2 X_L\right] X_{Lp} - \left(X_s^2 + R_1^2\right). \tag{3.12}$$

As k ranges from 0 to 1, the two roots of X_{Lp} are derived from (3.12):

$$X_{Lp} = \frac{-X_s + X_{L1}}{2} - \frac{X_s + X_{L1}}{2} b \pm \frac{1}{2}\sqrt{A^2 b^2 - 2Bb + C^2} \tag{3.13}$$

where

$$\begin{aligned} b &= 1/\left(1 - k^2\right) \\ R_1 &= R_s + R_{Lp} \\ R_2 &= R_L + R_{Ls} \\ X_{L1} &= \left(R_1/R_2\right) \times X_L \\ A &= X_s + X_{L1} \\ B &= X_s^2 + X_{L1}^2 + 2R_1^2 \\ C &= -X_s + X_{L1}. \end{aligned} \tag{3.14}$$

Two roots can be expressed as follows:

$$\begin{aligned} X1_{Lp} &= \frac{-X_s + X_{L1}}{2} - \frac{X_s + X_{L1}}{2} b + \frac{1}{2}\sqrt{A^2b^2 - 2Bb + C^2} \\ &= -\frac{X_s}{2}(b+1) - \frac{X_{L1}}{2}(b-1) + \frac{1}{2}\sqrt{A^2b^2 - 2Bb + C^2} \end{aligned} \tag{3.15}$$

$$X2_{Lp} = -\frac{X_s}{2}(b+1) - \frac{X_{L1}}{2}(b-1) - \frac{1}{2}\sqrt{A^2b^2 - 2Bb + C^2}, \tag{3.16}$$

where

$$b = 1/\left(1 - k^2\right) \propto k \in (1, +\infty) \tag{3.17}$$

To ensure real roots exist, the discriminant must be greater than or equal to zero:

$$\begin{aligned} \Delta(b) &= A^2b^2 - 2Bb + C^2 \\ &= A^2\left(b - \frac{B}{A^2}\right)^2 + C^2 - \frac{B^2}{A^2} \geq 0. \end{aligned} \tag{3.18}$$

Given that $A^2 > 0$ and $\Delta(1) = A^2 - 2B + C^2 = -4R_1^2 < 0$, the condition (3.19) must be satisfied to ensure Δ is non-negative.

$$b \geq \frac{B + \sqrt{B^2 - A^2C^2}}{A^2} \tag{3.19}$$

For each root X_{Lp}, only positive values hold physical significance; thus, it is crucial to first determine the sign before differentiating to establish the relationship with b. For coils connected to active devices, the reactance is negative due to the parasitic capacitance of these devices. For coils linked to the source or load, the reactance is zero. Therefore, the conditions $X_s, X_L \leq 0$ and $X_sX_L \neq 0$ will be utilized in the subsequent calculations.

It is evident that $X1_{Lp} > 0$, and the derivative is given by:

$$\frac{\mathrm{d}X1_{Lp}}{\mathrm{d}b} = -\frac{X_s + X_{L1}}{2} + \frac{A^2b - B}{2\sqrt{A^2b^2 - 2Bb + C^2}}. \tag{3.20}$$

The first term in (3.20) is obviously positive, while the sign of the second term can be inferred from (3.19) as follows:

$$A^2b - B \geq \sqrt{B^2 - A^2C^2} \geq 0. \tag{3.21}$$

Thus, we conclude that:

$$X1_{Lp} \propto b \propto k. \tag{3.22}$$

Defining

$$\begin{aligned} D_1 &= -X_s\,(b+1) - X_{L1}\,(b-1) \\ &= -X_s + X_{L1} - \left(X_s + X_{L1}\right) b \\ &= C - Ab \\ D_2 &= \sqrt{A^2b^2 - 2Bb + C^2}, \end{aligned} \tag{3.23}$$

we can express $X2_{Lp}$ as $X2_{Lp} = \frac{1}{2}\left(D_1 - D_2\right)$. To determine the sign of $X2_{Lp}$, we compute (3.24):

$$\begin{aligned} &\left(D_1 + D_2\right)\left(D_1 - D_2\right) \\ =&D_1^2 - D_2^2 \\ =&(C - Ab)^2 - \left(A^2b^2 - 2Bb + C^2\right) \\ =&2\,(-AC + B)\,b \\ =&4\left(R_1^2 + X_s^2\right) b > 0 \end{aligned} \tag{3.24}$$

Given that (3.24) is greater than zero, $D_1 > 0$, and $D_2 \geq 0$, it follows that $D_1 - D_2$ must also be positive, indicating that $X2_{Lp}$ is positive.

The derivative of $X2_{Lp}$ is:

$$\begin{aligned} \frac{\mathrm{d}X2_{Lp}}{\mathrm{d}b} &= -\frac{X_s + X_{L1}}{2} - \frac{A^2b - B}{2\sqrt{A^2b^2 - 2Bb + C^2}} \\ &= \frac{1}{2}\left(-A - E_1\right). \end{aligned} \tag{3.25}$$

To ascertain the relationship between $X2_{Lp}$ and k, we evaluate (3.26):

$$\begin{aligned} &\left(-A - E_1\right)\left(-A + E_1\right) \\ =&A^2 - E_1^2 \\ =&A^2 - \frac{A^4b^2 - 2A^2Bb + B^2}{A^2b^2 - 2Bb + C^2} \\ =&\frac{A^2C^2 - B^2}{A^2b^2 - 2Bb + C^2} \\ =&\frac{-4\left(X_{L1}^2 + R_1^2\right)\left(X_s^2 + R_1^2\right)}{A^2b^2 - 2Bb + C^2} < 0 \end{aligned} \tag{3.26}$$

Since (3.26) is less than zero, and given that $-A \geq 0$ and $E_1 \geq 0$, it follows that $(-A - E_1)$ must be negative, indicating that (3.25) is negative. Thus, we conclude:

$$X2_{Lp} \propto \frac{1}{b} \propto \frac{1}{k}. \tag{3.27}$$

In summary, the first root $X1_{Lp}$, associated with the "+" symbol, exhibits a large value and is proportional to k. In contrast, the second root $X2_{Lp}$, associated with the "−" symbol, has a smaller value and is inversely proportional to k.

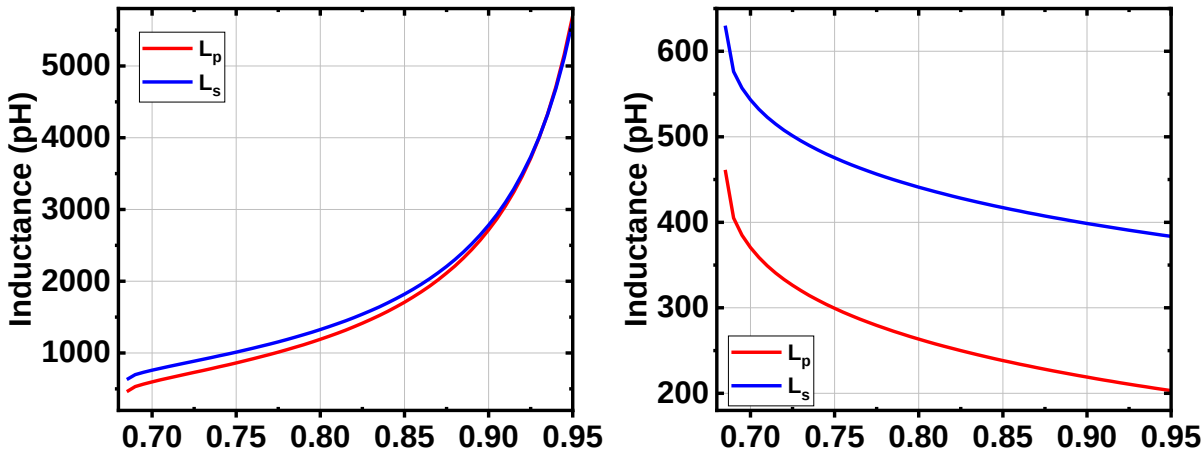


Figure 3.16: Calculated inductance values for power matching: (a) large root; (b) small root.

The larger value of $X1_{Lp}$ leads to increased inductances for both the primary and secondary coils, as X_{Ls} is proportional to X_{Lp}, as indicated in (3.10). Figure **??** illustrates the inductances corresponding to $X1_{Lp}$ and $X2_{Lp}$ for XF_3 in our designed PA as

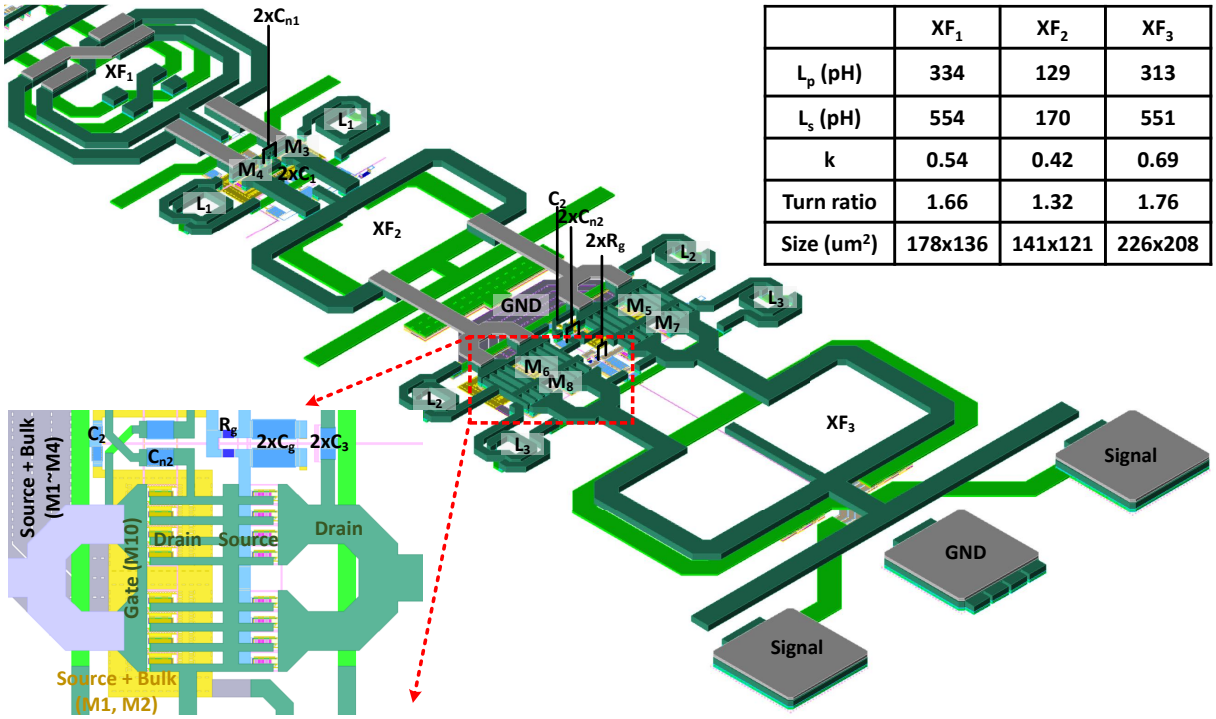
$$Z_s = 25.8 - j22.5, Z_L = 24.4 - j43.0, \tag{3.28}$$

considering the capacitors in parallel with the XF_3 and the capacitances of the output pads.

Due to the large area and the significant parasitic resistances associated with high inductance, $X2_{Lp}$, which has a smaller value, is preferred in XF design. To further reduce the losses generated by these parasitic resistors, a higher k is favored, as it allows for decreased inductances of the coils, thereby enhancing overall efficiency.

Layout of the Front-end The design of the XFs follows the proposed methodology for creating an effective MN, with key parameters highlighted in Figure 3.17. A noteworthy feature in the design is the configuration of the differential outputs of XF_3, which are crossed to achieve a coupling coefficient of 0.69. This configuration is strategically chosen to minimize losses, thereby enhancing the overall efficiency of the system. Additionally, the 3D layout of the

RF front-end is illustrated in the same figure, showcasing how the design incorporates spatial considerations alongside electrical performance.



	XF_1	XF_2	XF_3
L_p (pH)	334	129	313
L_s (pH)	554	170	551
k	0.54	0.42	0.69
Turn ratio	1.66	1.32	1.76
Size (um^2)	178x136	141x121	226x208

Figure 3.17: 3D layout of the front-end and parameters of XFs.

In the layout, the interconnections between MOSFETs M_5 and M_6 to M_7 and M_8 are minimized. This decision is driven by a need to mitigate the high losses often associated with large signal transitions, which can degrade performance. By reducing these interconnections, the design not only minimizes potential loss paths but also enhances signal integrity, which is crucial for maintaining the high-frequency performance required in RF applications.

All capacitors are deliberately positioned between the positive and negative signal paths, optimizing the circuit's overall capacitance balance and signal symmetry. Six spiral inductors are strategically designed and placed to terminate second-order harmonics, ensuring that these unwanted frequencies do not interfere with the desired signal. These inductors are symmetrically and compactly positioned on either side of the active circuit, effectively utilizing space without significantly increasing the circuit's footprint.

To further optimize the design, the reduction of parasitic coupling capacitance between signals and ground is addressed by employing metal-10 to connect signals from M_5. This choice minimizes unwanted capacitive effects, which can introduce noise and degrade signal quality. In contrast, metal-1 and metal-2 are designated as ground planes connecting the source and bulk of M_5, providing a stable grounding environment. The ground planes of M_5 and M_6 are interconnected using metal-1 through metal-4, ensuring robust grounding continuity and enhancing

the circuit's electromagnetic compatibility.

For the signal path situated above these ground connections, the aluminum (Al) pad layer is utilized to establish strong and reliable signal connections. This layer choice ensures that the signal path is well-defined and isolated from potential ground disturbances, contributing to the overall reliability and performance of the RF front-end.

Phase-Locked Loop

Architecture The proposed DPSSPLL architecture, as depicted in Fig. 3.18, comprises an dual-branch SSPD, an all-passive proportional path, an active integral path, a 20-24-GHz class-C VCO, and a TSPC divide-by-4 (DIV-4) circuit with an SS-buffer.

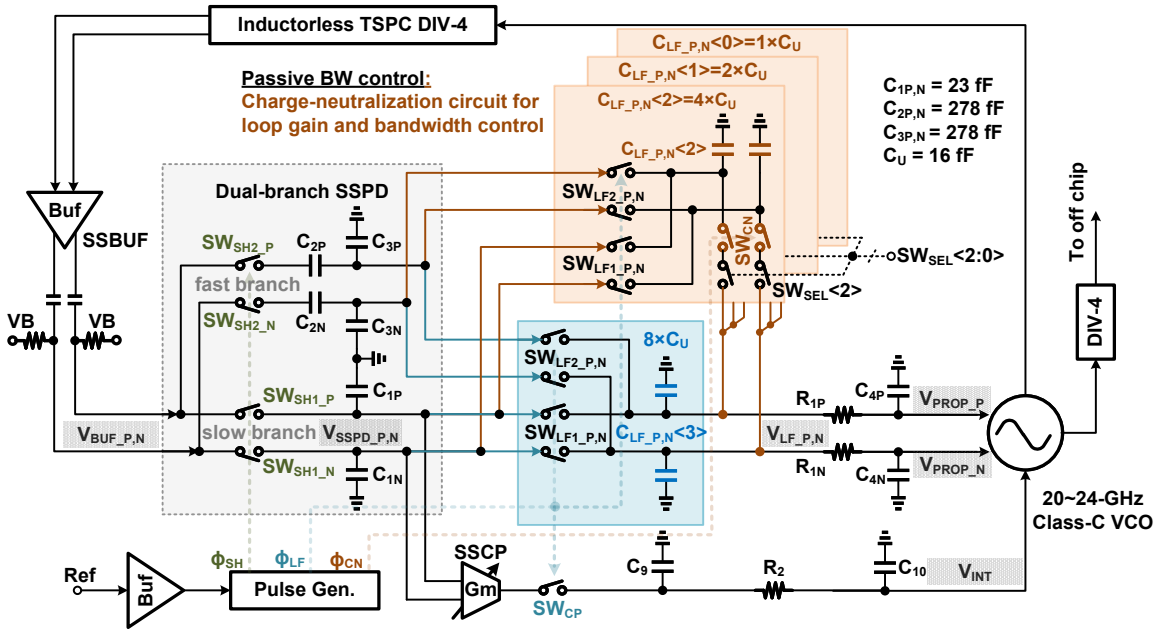


Figure 3.18:
System architecture of the proposed DPSSPLL, consisting of an all-passive proportional path with charge-neutralization-based gain control circuit, and a narrow-band active integral path.

The proportional path (as shown in Fig. 3.18) governs the overall loop dynamics, tracking phase noise and determining the PLL bandwidth. The dual-branch SSPD facilitates a substantial open loop gain with sufficient phase margin (discussed in Section III) [88]. The loop filter capacitors $C_{LF\_P,N}$ are implemented as a 4-bit capacitor bank (capbank) to support the charge-domain gain and bandwidth control function. Among the 4 bits, the most significant bit (MSB) $C_{LF\_P,N}$<3> is fixed, while the connections of $C_{LF\_P,N}$<2:0> are switchable between the P and N side to achieve controllable charge neutralization. Additionally, a low-pass filter comprising $R_{1P,N}$ and $C_{4P,N}$ aids in attenuating spur.

The integral path aims to bridge the offset between the targeted frequency and the VCO's free-running frequency. It comprises a SSCP with a small transconductance (G_{m}) and a C-R-C loop filter. A substantial DC gain (ideally close to infinity without SSCP mismatch) from the I-path effectively captures the initial frequency offset by modulating the oscillator control voltage through charging C_9 and C_{10}. This configuration results in a relatively fixed SSPD gain, ensuring robust gain, bandwidth, and phase margin for the P-path. For stability, the I-path gain should be significantly lower than that of the P-path, meaning the I-path bandwidth should be as narrow as possible. While either reducing the SSCP's G_{m} or increasing the integration capacitance of C_9 and C_{10} can narrow the I-path bandwidth, the former option is preferred to avoid bulky on-chip capacitors. Furthermore, narrowing the bandwidth aids in diminishing the phase noise contribution from the SSCP in the I-path.

For the prescaling and VCO buffering functions, an inductorless true-single phase clock-type divide-by-4 (DIV-4) circuit is utilized. This TSPC divider is not only power-efficient, but can also enhance the area efficiency compared to a resonance-mode buffer. Following the TSPC DIV-4, an inverter-based SSBUF is employed to drive the SSPD through an AC-coupled network. The AC-coupling serves to establish an appropriate biasing voltage for the SSCP in the integral path, ensuring a sufficient overdrive voltage.

The dual-path architecture, consisting of a differential proportional path and a single-ended integral path, offers two key features:

- Firstly, the I-path's high DC gain ensures that the static voltage offset between the P and N sides of the P-Path ($V_{\mathrm{PROP\_P\_DC}} - V_{\mathrm{PROP\_N\_DC}}$) approaches zero when reaching the locked state, as shown in Fig. 3.19. Consequently, the charge stored on $C_{\mathrm{LF\_P}}$<3:0> and $C_{\mathrm{LF\_N}}$<3:0> comprises the same DC components but a differential AC components.
- Secondly, the passive P-Path alone offers a maximum bandwidth of approximately 8 MHz (Section III-C), which exceeds the optimal bandwidth in most scenarios. For instance, with a 5-mW, 20-GHz VCO, the phase noise at an 8-MHz offset is -127 dBc/Hz, corresponding to a figure of merit (FoM) of 188 dB, which is equivalent to a 200-MHz reference phase noise of -167 dBc/Hz. Achieving such phase noise levels is challenging with standard crystal oscillators, buffers, and loop components.

The above two points indicate that optimizing integrated jitter typically involves narrowing the bandwidth, a process commonly achieved through a slope-controlled buffer for passive type-I implementations. However, this method smooths the reference slope, resulting in an increased noise upconversion window and degraded phase noise. Instead, this work introduces a charge-

neutralization-based gain control scheme. By recognizing that the stored charge on the P-Path's loop filter includes a common DC component and differential AC components, gain control is achieved by neutralizing part of the differential charge without affecting the DC portion. To facilitate this function, a 4-bit capacitor bank is utilized for the loop filter capacitors on the proportional path. The capacitance for the 4 bits range from $8 \times C_U$, $4 \times C_U$, $2 \times C_U$ to $1 \times C_U$, with the most significant bit (MSB), $C_{LF\_P,\,N}$<3>, fixed to the P, N side. The remaining three bits, $C_{LF\_P,\,N}$<2:0>, can be redistributed using SW_{CN} to steer the charge to the opposite sides. The amount of capacitance (charge) being involved in the neutralization process is controlled by 3-bit switches, SW_{SEL}<2:0>, as depicted in Fig. 3.18. Ensuring reasonable capacitance matching in the 4-bit capacitor bank requires a sufficiently large total loop filter value. However, conventional switched-capacitor type-I configurations cannot meet this requirement due to the stringent phase margin. To overcome this, a dual-branch SSPD is adopted to accommodate a large loop filter capacitance without compromising the phase margin.

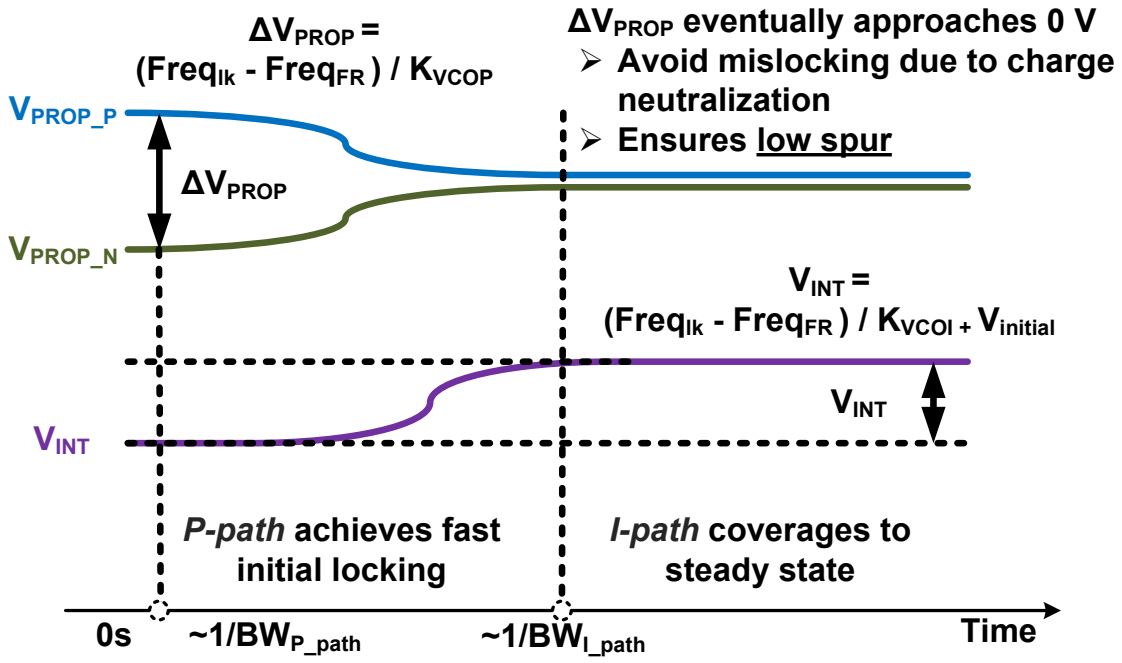


Figure 3.19: Illustration of the initial locking process of the DPSSPLL. Upon PLL stabilization, the integral path tracks the frequency offset between the target frequency and the VCO's free-running frequency. The static voltage difference between the P and N sides of the proportional path approaches 0 V ideally.

Operation Principle The operation process and waveform at different nodes of the PLL are depicted in Fig. 3.20 (a) and (b) respectively. The operation is controlled by three consecutive pulses: ϕ_{SH}, ϕ_{LF}, and ϕ_{CN}, produced by a pulse generator. The "track and hold" pulse,

ϕ_{SH}, tracks the SSBUF output at a high level and holds the sampled information on capacitors $C_{1,\,2,\,P,\,N}$ at a low level. During the subsequent loop filter control pulse, ϕ_{LF}, the sampled charge is shared with the 4-bit loop filter capacitors $C_{LF\_P,\,N}$<3:0>. The duration of the loop filter control pulse, denoted as ϕ_{LF}, is narrow but sufficient for completing charge sharing process. Next, a charge neutralization pulse, ϕ_{CN}, controls the charge neutralization switches SW_{CN} to neutralize a portion of the charge between the P and N sides of the loop. The charge sharing process, followed by the charge neutralization, leads to a narrow voltage spike on the loop filter voltage, denoted as $V_{LF\_P,\,N}$. Thanks to the narrow on-time duration of the loop filter control pulse, ϕ_{LF}, the voltage spike can be attenuated by the low-pass filter formed by $R_{1P,\,N}$ and $C_{4P,\,N}$.

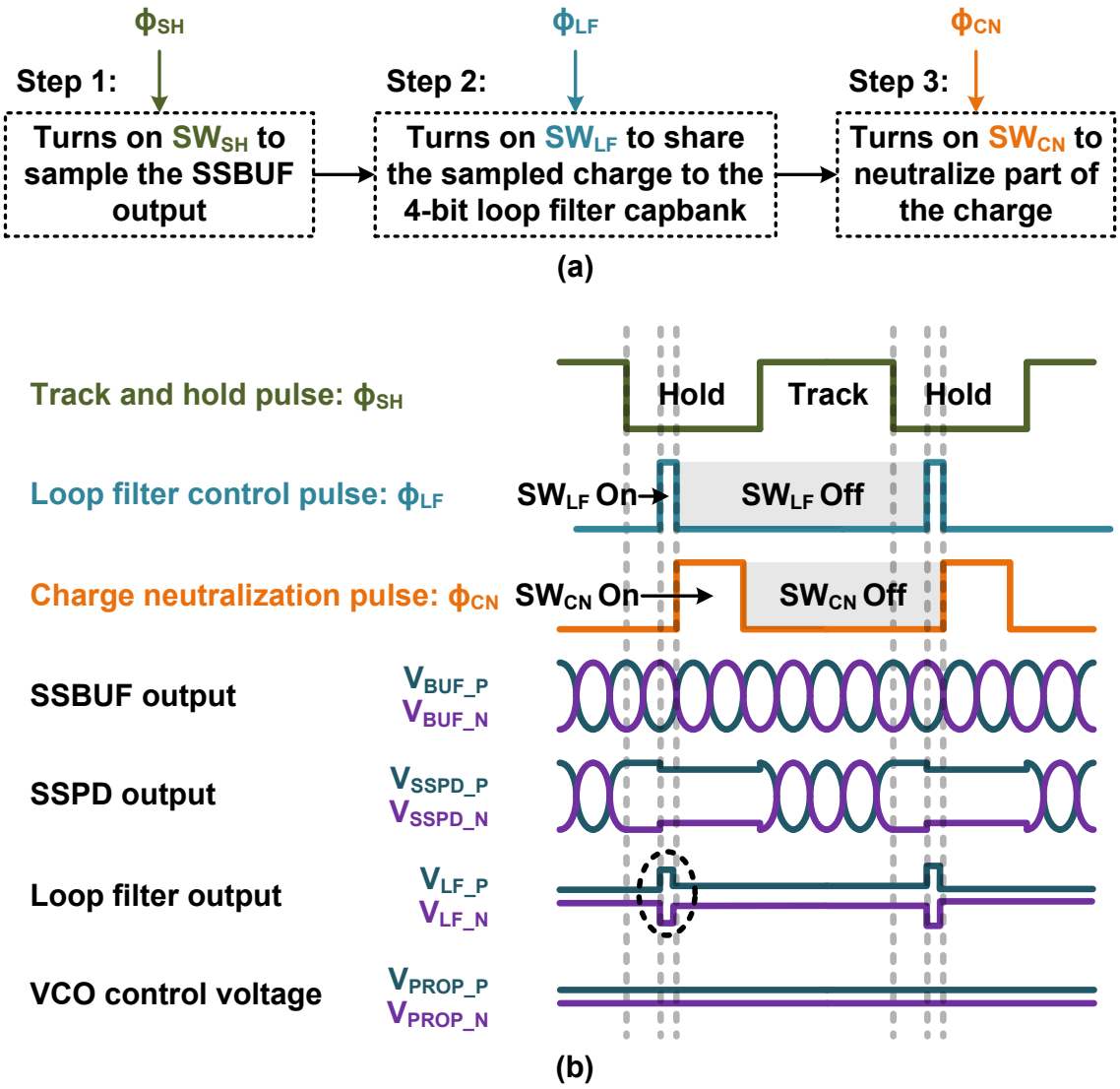


Figure 3.20: (a) The operation process of the DPSSPLL, controlled by ϕ_{SH}, ϕ_{LF} and ϕ_{CN}. (b) Illustration of waveform at critical nodes of the loop.

Locking Process Here, we introduce the locking process that begins when the PLL is powered on. First, the P-path and I-path are disabled by an on-chip initialization circuit, allowing the VCO capacitor bank to be coarsely adjusted so that the VCO's free-running frequency aligns closely with the target locking frequency. Next, both paths are enabled, with the P-path achieving locking within tens of nanoseconds, followed by the I-path converging in tens of microseconds. Once a locked state is obtained, the charge-neutralization code is adjusted to optimize the integrated jitter. In case the initial frequency is significantly far from the target locking frequency—such as tens of MHz—the initial loop gain is set to maximum, facilitating successful convergence of the oscillator control voltage in the I-path. After this, the gain state is switched to the optimal setting.

Charge Neutralization Process The charge-domain gain control process comprises two steps: charge sharing (via SW_{LF}) and charge neutralization (via SW_{CN}<2:0>), as depicted in Fig. 3.21 (a) and (b) respectively. In the first step, the stored charges from the SSPD's slow path and fast path (stored on $C_{\mathrm{1P,\,N}}$ and $C_{\mathrm{1P,\,N}}$, respectively) are combined and shared through $SW_{\mathrm{LF1,2\_P,\,N}}$ with the 4-bit loop filter capacitors, $C_{\mathrm{LF\_P,\,N}}$<3:0>. After the charge sharing process is complete, the amount of charge on the 4-bit capacitor bank, from MSB to LSB, is 8, 4, 2, and 1 unit of charge ($\mathrm{charge_{UNIT}}$), respectively. Among the 4-bit capacitor bank, the MSB, $C_{\mathrm{LF\_P(N)}}$<3>, is fixed to the P (or N) side and holds a charge of 8×$\mathrm{charge_{UNIT}}$ (8×C_{U}).

The subsequent charge neutralization process is illustrated with an example: assuming that only $C_{\mathrm{LF\_P,\,N}}$<2> with a capacitance of $4C_{\mathrm{U}}$ is activated for gain control. The activation and deactivation functions are supported using the 3-bit switches SW_{SEL}<2:0> depicted in Fig. 3.18. When ϕ_{CN} goes high, during this interval, 4 out of the total 8 units of charge on the P-side fixed capacitor $C_{\mathrm{LF\_P}}$<3> are neutralized by the charge flowing from the opposite side's $C_{\mathrm{LF\_N}}$<2>. The remaining 4 units of charge on $C_{\mathrm{LF\_P}}$<3> are then redistributed among the $12C_{\mathrm{U}}$ capacitors connected together ($C_{\mathrm{LF\_P}}$<3> + $C_{\mathrm{LF\_P}}$<2>). As a result, after charge neutralization and redistribution, the charge amount on the fixed $C_{\mathrm{LF\_P}}$, as well as the AC voltage signal on the P side is reduced to one-third of its original value. The same analysis also applies to the N side. Consequently, the overall open-loop gain is also reduced to one-third.

The charge neutralization switch, SW_{CN}, is simplified with a single switch in Fig. 3.21 (a) and (b). In the actual implementation presented in Fig. 3.21 (c), a charge neutralization switch (SW_{CN}) modulated by ϕ_{CN} is positioned in between two capbank selection switches, SW_{SEL}<N>, where N can be 0, 1, or 2. The capbank selection switches are responsible for controlling the amount of capacitance involved in the neutralization process, thereby adjusting

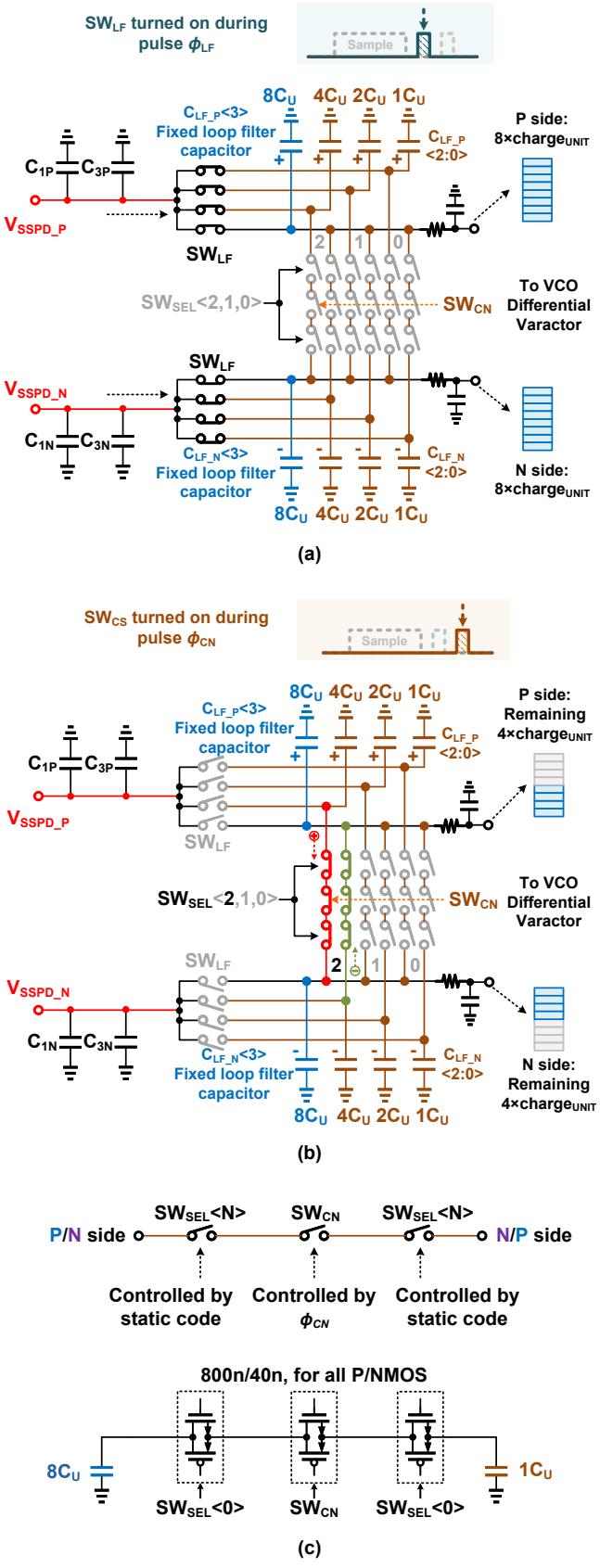


Figure 3.21: Illustration of the charge-domain gain control process. (a) First step: charge sharing from the sampling capacitors ($C_{1P,\,N}$, $C_{3P,\,N}$) to the loop filter capacitors $C_{LF\_P,\,N}$<3:0>. (b) Second step: charge neutralization between $C_{LF\_P(N)}$<3> and $C_{LF\_N(P)}$<2:0>. (c) Implementation of the neutralization and selection switches.

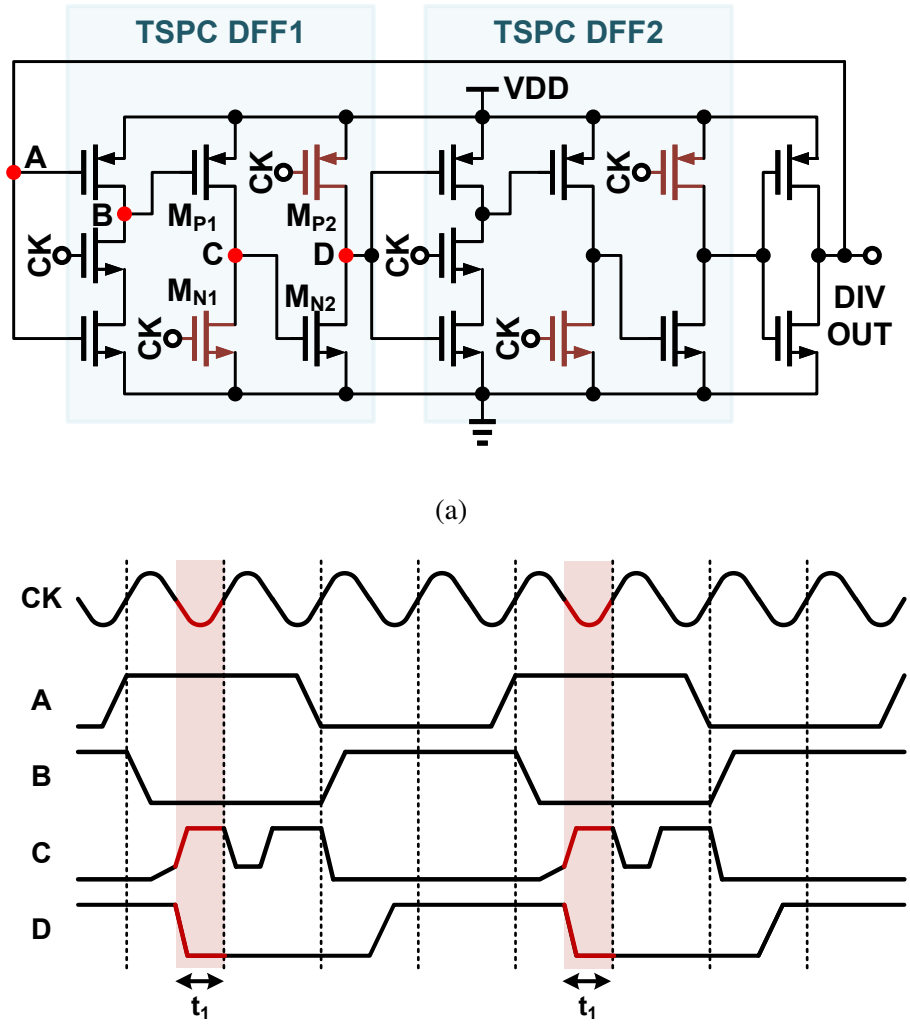
the open-loop gain. By placing the selection switches on both sides of the charge neutralization switch, the clock feedthrough from SW_{CN} can be eliminated when SW_{SEL}<N> is turned off, or attenuated when SW_{SEL}<N> is turned on. The switch parameters for controlling the LSB ($1 \times C_U$) in the capacitor bank are also depicted in Fig. 3.21 (c).

Major Building Blocks

TSPC Divider In the feedback path, TSPC logic is utilized as the prescaler and VCO buffer. This choice enhances area efficiency by eliminating the need for a resonance-mode buffer at 20-24 GHz. Additionally, the TSPC divider and subsampling buffer provide effective isolation between the VCO and the SSPD, preventing feedback during the sampling process. Several other divider options exist, including current-mode logic (CML) DIV-4 and injection-locked DIV-4. While the CML DIV-4 circuit supports high operating frequencies, it requires the highest power consumption and chip area, making it unsuitable for our design. On the other hand, the injection-locked DIV-4 offers relatively high frequencies, low power requirements, and compact area usage. However, its locking range is limited to approximately 20% under specific biasing currents, necessitating fine-tuning of the free-running frequency to achieve locking, which introduces operational complexities. In contrast, the TSPC divider provides sufficient operational frequencies, low power consumption, and a broad operating range, aligning well with our design requirements. However, this comes at the cost of reducing the open-loop gain by a factor of four. Among the various TSPC logic topologies [89], the ratioed TSPC topology is selected as it offers a superior speed [90, 91].

The TSPC DIV-4 circuit, shown in Fig. 3.22 (a), consists of two ratioed TSPC DFFs and an inverter. TSPC DFF1 takes the input signal from node A and produces an inverted output signal at node D during every falling edge of CK. TSPC DFF2, along with the inverter, forms a latch that retains the signal level on node D for one input clock cycle. As a result, a complete output cycle on DIV OUT requires four input clock cycles, achieving a divide-by-4 operation. The input clock is directly sourced from the VCO and covers a frequency range of 20-24 GHz, resulting in a divided output clock frequency of 5-6 GHz.

Figure 3.22 (b) presents the waveforms at each internal node for one of the TSPC DFFs during eight input clock cycles. The sizing of the PMOS and NMOS transistors is carefully designed to ensure proper pull-down at node D. In Fig. 3.22 (b), during period t_1, the gate node voltage for PMOS M_{P2} (CK) remains low, while for NMOS M_{N2} (node C), it stays high. To ensure correct propagation of the signal from node C to node D, the NMOS transistor should be



(a)

(b)

Figure 3.22: (a) Schematic of the TSPC divide-by-4 circuit topology. (b) Waveform illustration at each node of the TSPC D-flip-flop.

sized adequately to effectively pull down the voltage at node D. In this work, the optimal sizing, determined through simulation, is found to be 9.6µm/40nm for PMOS and 11.2µm/40nm for NMOS.

Through post-layout simulation, the simulated upper operating frequency versus the process corner is illustrated in Fig. 3.23. Under the ss corner, the divider can operate up to 26.8 GHz, which is sufficient to cover the tuning range of the PLL. Additionally, the power consumption versus CLK frequency is presented at the tt corner with VDD values of 0.8 V and 0.9 V in Fig. 3.23. At the center frequency of 22 GHz, the power consumption is estimated to be 1.22 mW when operating with the commonly used 0.9 V supply voltage.

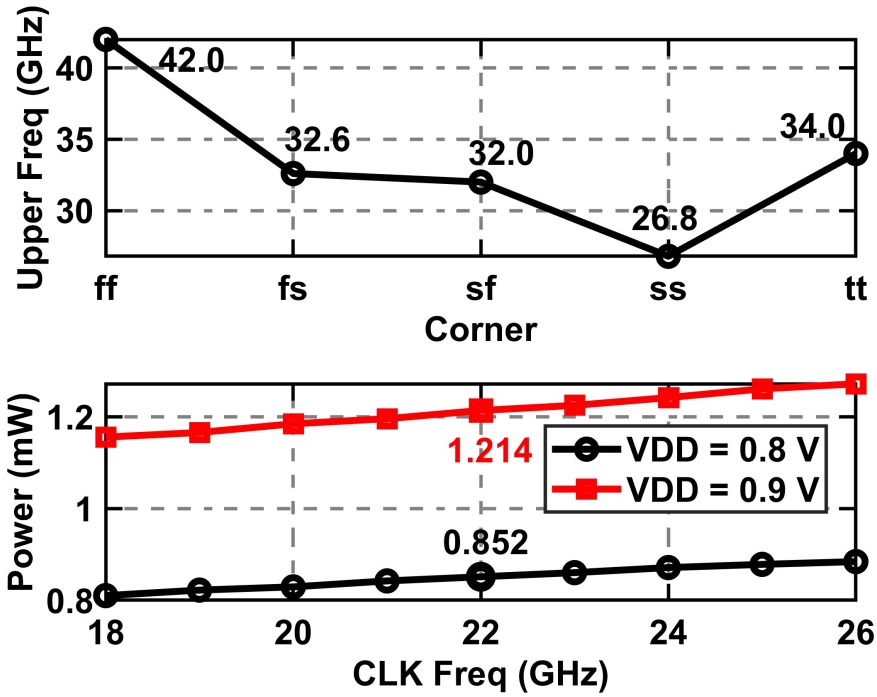


Figure 3.23: Simulated maximum operating frequency versus process corner, and power consumption versus clock frequency at the tt corner.

Pulse Generator The pulse generator shown in Fig. 3.24 is responsible for generating three control pulses: ϕ_{SH}, ϕ_{LF}, and ϕ_{CN}. Among these pulses, ϕ_{SH} is highly sensitive to additional phase noise introduced by buffers or delays, as any extra phase noise will immediately translate to the sampled phase error information. To mitigate this, the reference signal is buffered by a two-stage inverter without using any delay element, and the resulting signal is used as ϕ_{SH}.

While the phase noise of ϕ_{LF} and ϕ_{CN} are not as critical, the design of their on-time durations requires careful consideration. The lower bounds of these pulse durations are dictated by the time constants of the switch-on resistance and loading capacitance. To illustrate the time constants, we examine the least significant bit (LSB) of the 4-bit loop filter cap bank ($1 \times C_U$ = 16 fF) as an example. The on-resistance of SW_{LF} connected to $1 \times C_U$ is around 270 Ω, resulting in a time constant of 4.3 ps. For SW_{CN}, three switches are connected in series (as shown in Fig. (c)), leading to a time constant of 13 ps. Both ϕ_{LF} and ϕ_{CN} pulse durations should sufficiently exceed these time constants to ensure adequate charge redistribution.

However, an excessively long on-time for the ϕ_{LF} pulse could compromise the effectiveness of the charge-neutralization-based gain control. This gain control mechanism only becomes effective when SW_{LF} is off and SW_{CN} is on. Hence, in this design, the upper bound for ϕ_{LF} is capped at 100 ps, representing only 2.5% of the 250-MHz reference period. Regarding ϕ_{CN}, although a longer duration does not impair the loop's functionality, the on-time duration should

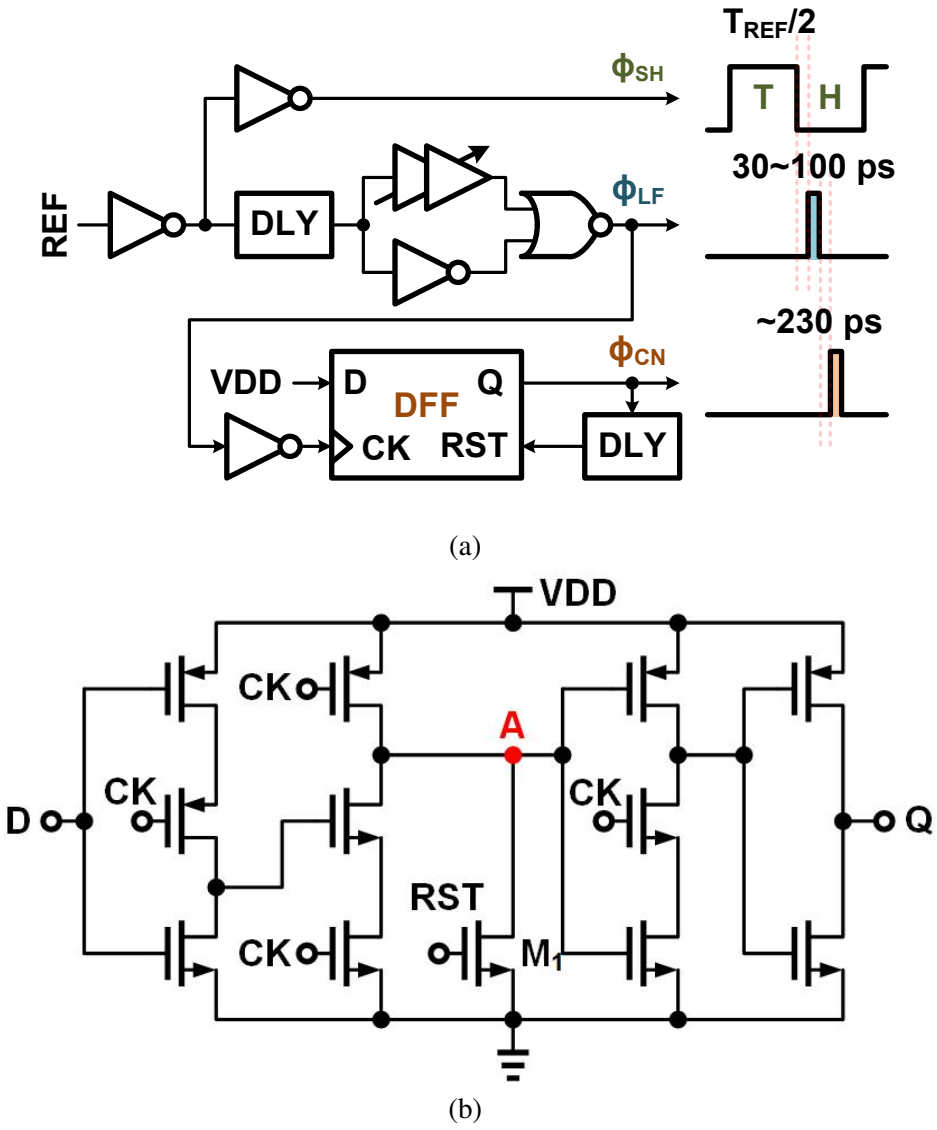


Figure 3.24: (a) Topology of the pulse generator and the on-time durations of the three pulses. (b) Circuit diagram of the TSPC DFF with reset function.

still be limited to reduce the thermal noise contribution from the switch-on resistance.

In this setup, the pulse width of ϕ_{LF} is adjustable from 30 to 100 ps, while the pulse width of ϕ_{CN} is approximately set to 230 ps. The ϕ_{LF} pulse is generated using a conventional delay-and-NOR based method. However, this approach cannot be directly used to generate the subsequent ϕ_{CN} pulse. Due to the narrow width of ϕ_{LF}, the delay-and-NOR based method may result in metastability. Therefore, ϕ_{CN} is generated by first sampling the VDD at the rising edge of ϕ_{LF} using a DFF and then resetting the output signal to ground after a short time period controlled by the DLY cell depicted in Fig. 3.24. The DFF with a reset function is implemented using TSPC topology, as illustrated in Fig. 3.24(b). The TSPC topology is well-suited for our design due to its compatibility with single-ended clock control and low complexity.

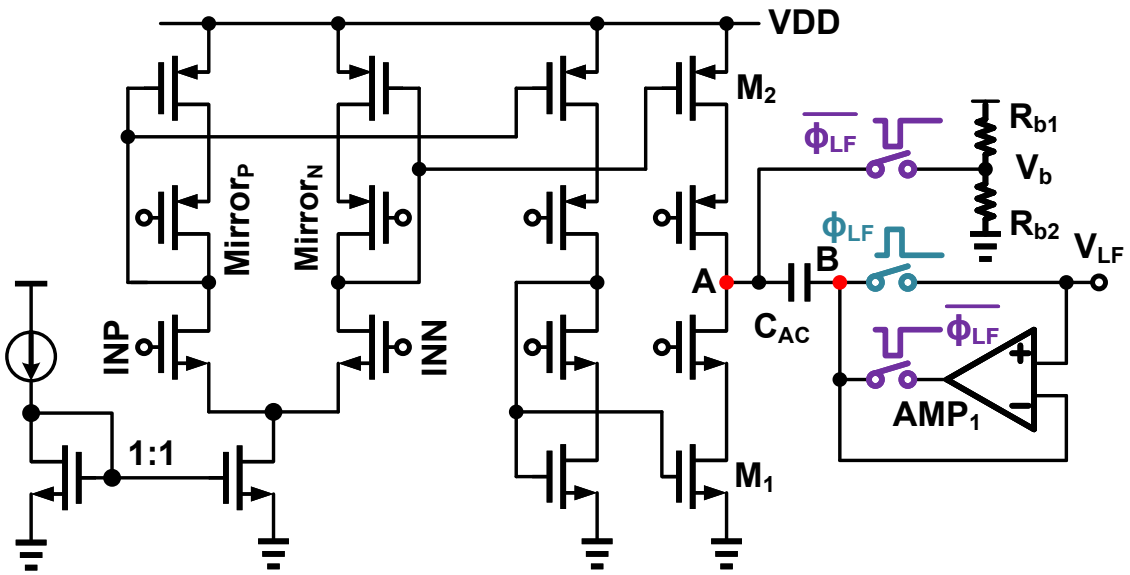


Figure 3.25: Sub-sampling charge pump topology.

Charge Pump The sub-sampling charge pump (SSCP) utilized in the I-path is depicted in Fig. 3.25. Its main objective is to provide a small transconductance (Gm) and immunity to offset current at the output node. A small transconductance allows for a more compact loop filter capacitor in the I-path, while immunity to offset current ensures a small static offset voltage between the differential P and N sides in the P-path, leading to lower spurs. Additionally, a smaller offset current enhances the gain of the SSPD.

To fulfill these design requirements, the proposed SSCP incorporates an AC-coupling capacitor to isolate the SSCP output from the following loop filter [92]. When ϕ_{LF} is turned off, node B is aligned with the loop filter voltage via a unity-gain feedback loop, while node A is maintained at V_{b}, which is in close proximity to VDD/2. This arrangement mitigates the channel length modulation-induced current mismatch, and charge sharing between nodes A and B. Consequently, the overall charge pump can achieve negligible output offset current.

The simulated nominal transconductance (Gm) of the SSCP under a biasing current of 20 uA is 0.15 mS. The VCO gain factor K_{VCO} for the integration path is approximately 200 MHz/V. With these parameters, an integration capacitance of 20 pF can narrow down the I-path bandwidth to around 600 kHz. When operating with a higher charge neutralization code (4-7), the biasing current can be reduced to achieve a narrower bandwidth, which helps ensure overall stability. The ACSSCP topology helps maintain a small offset current, even at low bias currents.The I-path's loop bandwidth is much smaller than that of the P-path, resulting in less degradation to the overall phase margin. The narrow I-path bandwidth also help attenuate the noise contribution

from the SSCP.

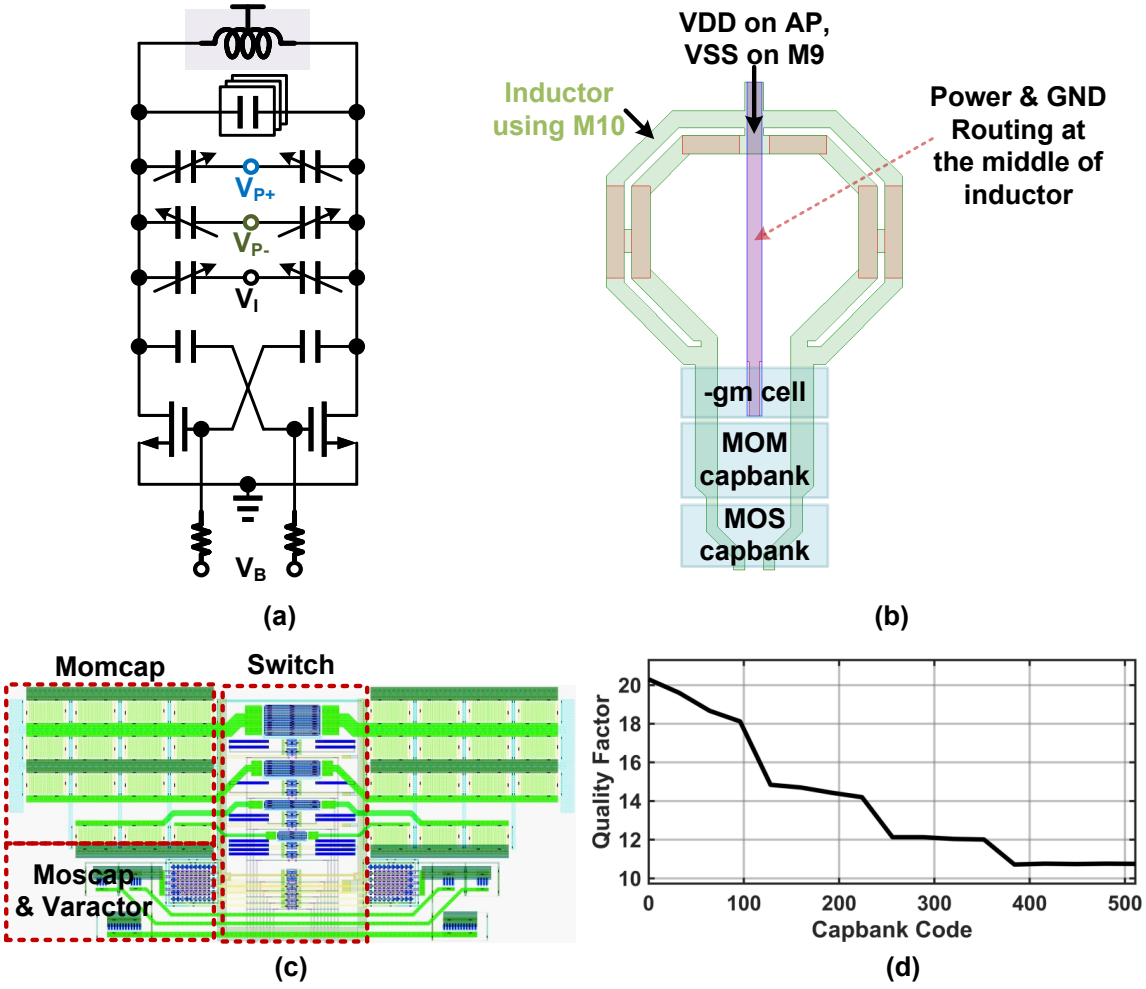


Figure 3.26: (a) Class-C VCO topology (b) layout of the inductor (c) layout of the capbank (d) Simulated capbank quality factor.

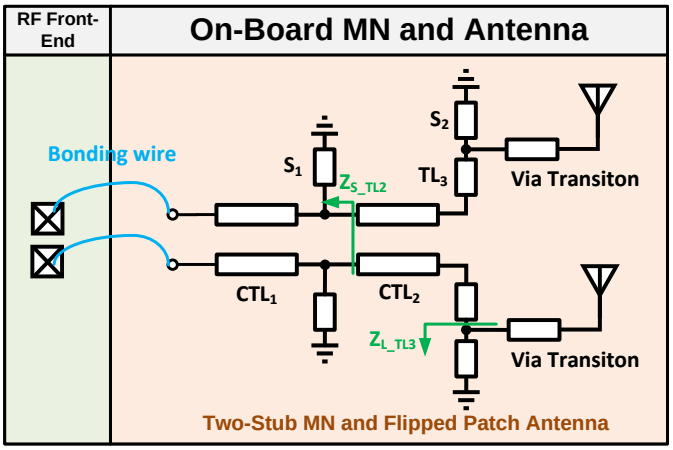
VCO The class-C VCO utilized in this study is depicted in Fig. 3.26 (a). Class-C VCOs offer favorable phase noise characteristics by operating with a bias voltage level (V_B) lower than the transistor's threshold level. This approach reduces noise upconversion and prevents the transistor from entering the deep triode region. Additionally, class-C VCOs produce relatively symmetric waveforms, reducing the contribution of flicker noise.

To accommodate the control signal (V_I) from the integral path, as well as V_{P+} and V_{P-} from the proportional path, three pairs of varactors are employed. For differential control, the two varactor pairs for V_{P+} and V_{P-} are connected in a reversed configuration.

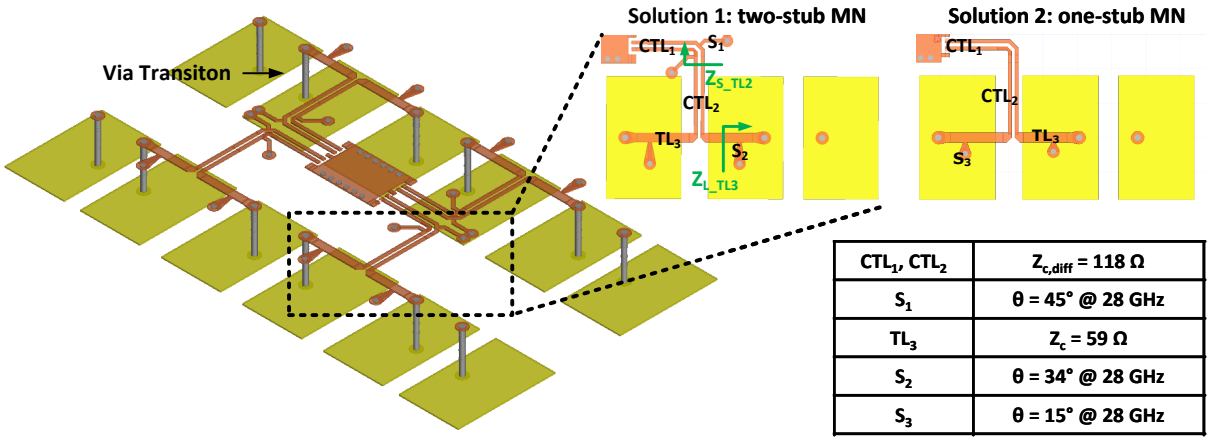
The layout of the inductor is shown in Fig. 3.26 (b). The VDD and VSS connections to the active negative gm cell are positioned directly beneath the inductor. By routing VDD and

VSS at the center of the inductor, we provide a well-defined return path for the active devices while minimizing the impact on the inductor's quality factor. To enhance the quality factor while adhering to design rule constraints, two turns of inductors, each approximately 9 µm wide, are routed in parallel. At the center frequency of 22 GHz, the simulated inductance is 168 pH, with a quality factor of 36.

The layout of the capacitor bank is shown in Fig. 3.26 (c), which is constructed using MoM capacitors for the higher bits and MOS capacitors for the lower bits. This capacitor bank facilitates a VCO tuning range of 18%. The quality factor extracted from the post-layout simulation is illustrated in Fig. 3.26 (d). As the capacitor bank code increases, more MOSFET switch resistance is added in series with the capacitors, causing the quality factor to gradually decrease from approximately 20 to 11.



(a)



CTL_1, CTL_2	$Z_{c,diff}$ = 118 Ω
S_1	θ = 45° @ 28 GHz
TL_3	Z_c = 59 Ω
S_2	θ = 34° @ 28 GHz
S_3	θ = 15° @ 28 GHz

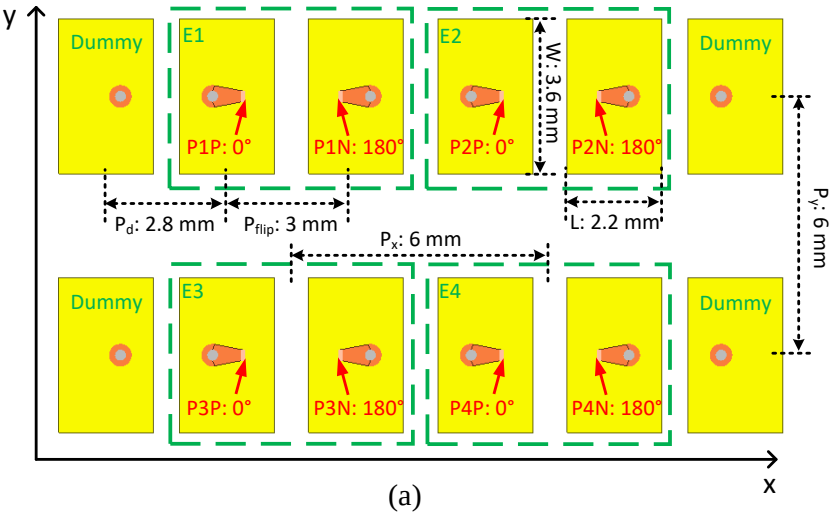
(b)

Figure 3.27: On-board MN and antenna: (a) schematic of two-stub MN; (b) Essential parameters and layouts of two-stub MN and one-stub MN.

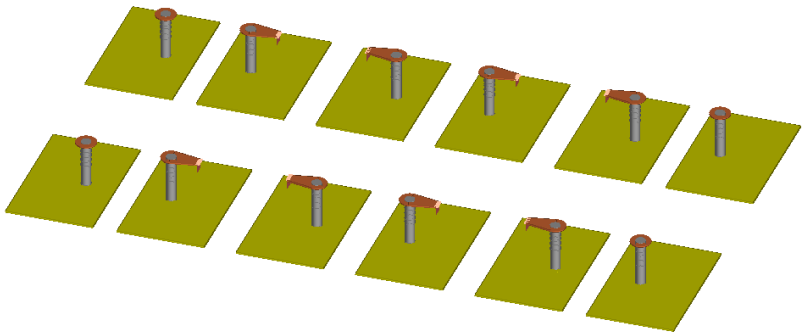
3.3.3 Radio-Frequency on-Board Circuits

In this section, we delve into the development of a robust prototype featuring a four-element flipped patch antenna array alongside a meticulously designed MN for off-chip circuits. This prototype serves as a foundational model, showcasing the potential for scalability through the duplication of its elements, thereby accommodating more extensive networks as needed. Figure 3.27(a) presents the schematic of a single antenna element. The flipped patch antenna is specifically configured with a differential input to adapt to the TX.

The connection between the on-chip circuits and the antenna array necessitates a compact and wideband on-board MN, which plays a crucial role in transferring impedance while also providing ample space for the connection of intermediate frequency (IF) and direct current (DC) signals. The two-stub MN is selected for this task due to its enhanced bandwidth capabilities compared to a simpler one-stub MN, thereby ensuring that the system maintains high signal integrity and minimal loss across a wide range of frequencies.



(a)



(b)

Figure 3.28: 4-element flipped antenna array: (a) Top view; (b) 3D view.

Flipped-Patch Antenna Array

The structural strategy aligns with the PCB stack-up illustrated in Figure 3.4, where the antenna array is tactically positioned on the bottom layer and linked to the top layer through the use of through vias. Figure 3.28 depicts the layout of the four-element flipped antenna array from both top-down and 3D perspectives, providing a comprehensive view of its spatial configuration. Each flipped antenna element is formed by combining two patches with differential inputs, which are designed to work in tandem to optimize performance. The dimensions of each patch, specifically the width (W) and length (L), along with the pitch between them (P_{flip}), are optimized to enhance the antenna gain. The optimizations are annotated in Figure 3.28, resulting in an impressive antenna gain of 4.3 dBi, as evidenced by the simulation results in Figure 3.29(a). The compact dimensions, within $\lambda/2 \times \lambda/2$, allow this flipped patch antenna to be easily arranged in a 2×2 array configuration, which is essential for beam steering capability.

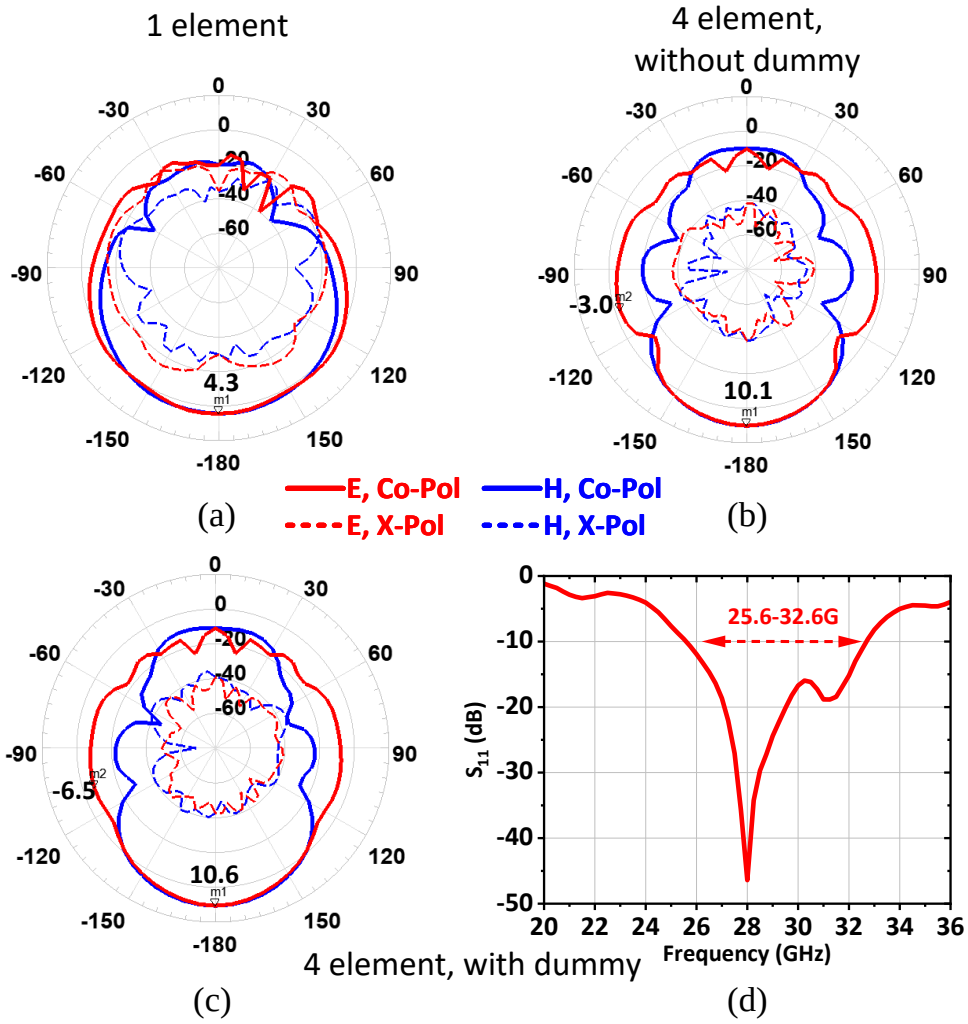


Figure 3.29: Simulated radiation pattern of (a) one flipped antenna; (b) 4-element flipped antenna array without dummy patches; (c) 4-element flipped antenna array with dummy patches; (d) Simulated reflection coefficient of 4-element flipped antenna array with dummy patches.

To further augment the performance of the array, the pitches of the flipped patch antenna are meticulously set at 0.56λ in both the x and y directions, achieving an array gain of 5.8 dB. The radiation pattern of the four-element array, depicted in Figure 3.29(b), reveals a side lobe at -3 dBi. To mitigate this side lobe effect and enhance the overall antenna gain, four dummy patches connected to the ground are strategically integrated around the array. These dummy patches play a pivotal role in suppressing the side lobe, as demonstrated by the electromagnetic (EM) simulation results in Figure 3.29(c). The introduction of these dummy patches results in a 3.5 dB reduction of the side lobe and an increase in array gain to 6.3 dB. The flipped patch antenna, along with the through vias, exhibits a -10 dB bandwidth spanning from 25.6 to 32.6 GHz, underscoring its exceptional capability in high-frequency applications.

Broadband Matching Network

Figure 3.27 provides a detailed overview of the schematic, layout, and associated parameters of both one-stub and two-stub MNs. The MNs are constructed using two microstrip coupled lines, CTL_1 and CTL_2, a single microstrip line, TL_3, and either one or two short stubs, S_3 or S_1 and S_2, respectively. The microstrip coupled lines are responsible for receiving the differential signal from the chip via bonding wires. To optimize space for control and intermediate frequency (IF) signal interconnections, the widths and spacing of CTL_1 and CTL_2 are minimized in accordance with manufacturing constraints, ensuring that the design remains compact and efficient.

The subsequent microstrip line, TL_3, plays a critical role in the signal path by separating the differential signal into two single-ended signals with a 180° phase difference. These signals are then directed into a flipped patch antenna, which is integral to the system's radiating structure. The characteristic impedance of TL_3 (Z_c) is meticulously set to half of that of CTL_2 ($Z_{c,diff}$) to ensure good impedance matching and to enhance the system's bandwidth. This impedance consideration directly influences the width of TL_3. The lengths of the three transmission lines are fixed based on the relative positioning of the antenna with respect to the chip.

In the one-stub MN, a single short stub, S_3, is inserted into TL_3. By adjusting the length and insertion position, impedance matching at 28 GHz is achieved. However, this configuration limits the bandwidth to 4.2 GHz, as illustrated in Figure 3.30. While effective for specific frequency applications, the one-stub configuration falls short in broader bandwidth requirements, prompting the need for a more versatile solution.

The two-stub MN is proposed to enhance bandwidth by reducing the total effective length of the transmission lines that induce impedance changes across frequencies. In this configuration, a short stub, S_1, is strategically inserted into the microstrip coupled lines. The primary function

of this stub is to ensure that the source impedance, denoted as Z_{S-TL2} precisely matches the characteristic impedance of CTL_2. The second short stub, S_2, is carefully positioned within the microstrip line TL_3. This stub plays a crucial role in matching the load impedance, Z_{L-TL3} to the characteristic impedance of TL_3. This configuration effectively minimizes the impact of the transmission lines between the two stubs on impedance variations, thereby supporting a wider operational bandwidth.

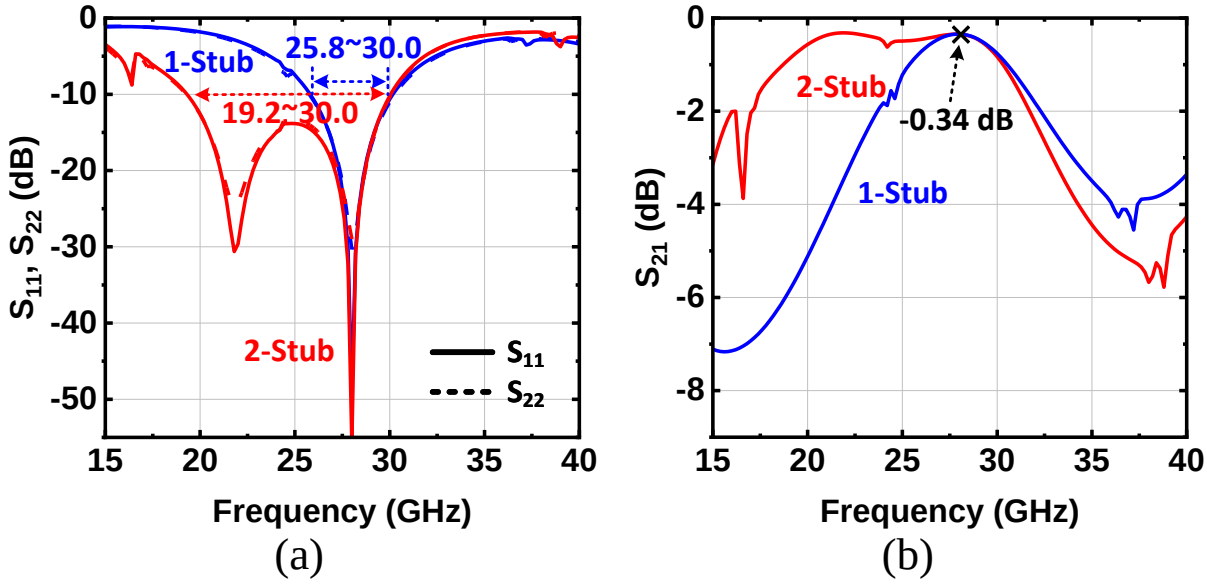


Figure 3.30: Simulated s-parameters of one-stub MN and two-stub MNs. (a) S_{11} and S_{22}; (b) S_{21}.

At a frequency of 28 GHz, the effective electrical length of the transmission lines in the two-stub matching network (MN) decreases significantly from 318° to 129°, marking a substantial reduction of 41%. This reduction directly correlates to an impressive bandwidth expansion, resulting in an 11.8 GHz bandwidth for the two-stub MN. This figure represents an increase of 2.8 times compared to the bandwidth of the one-stub MN. Notably, both matching networks demonstrate the same insertion loss of 0.34 dB at 28 GHz, indicating that the additional stub does not introduce any further loss, as illustrated in Figure 3.30(b). Given these advantageous characteristics, the two-stub structure is selected for integration into our proposed phased array system, providing enhanced performance without compromising signal integrity.

The comprehensive on-board circuits, which include the MN, antenna array, and bonding wire, undergo rigorous simulation to evaluate radiation patterns and S-parameters, as depicted in Figure 3.31. The 3D electromagnetic simulation results reveal a peak antenna gain of 8.9 dB, showcasing the effectiveness of the design in maximizing signal strength and coverage. Additionally, a -10 dB bandwidth of 6.2 GHz is achieved with a bonding wire height of 127 μm, which correlates to a simulated inductance of 0.71 nH. This height, denoted as h in Figure 3.5,

is controlled by the fabrication factory and has a high possibility of inducing performance deterioration.

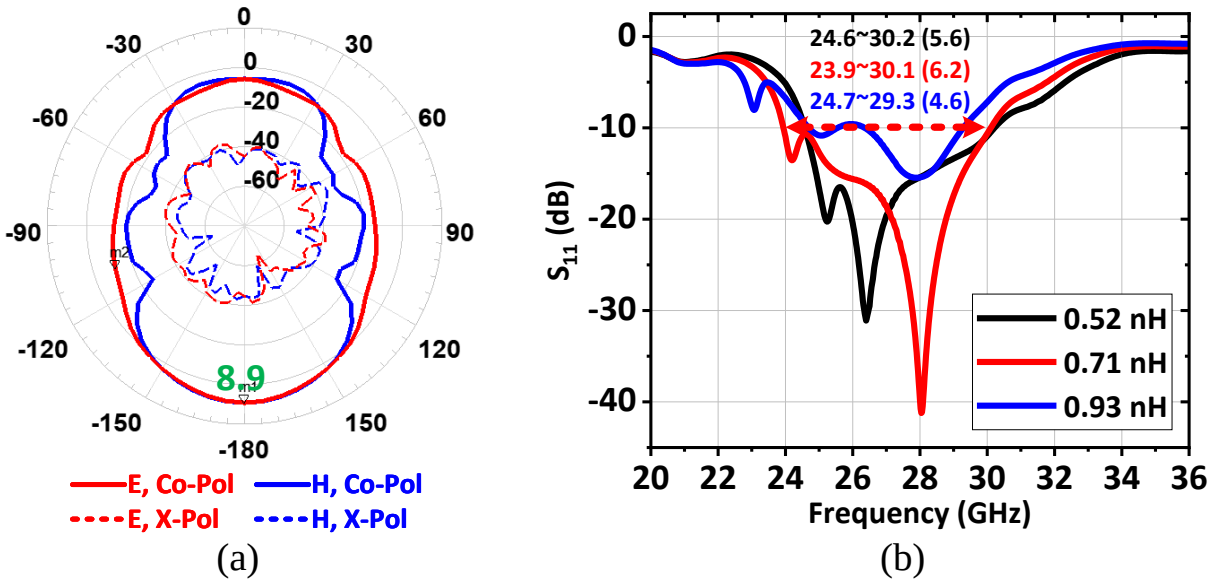


Figure 3.31: Simulation results of antenna array with two-stub MN: (a) Radiation pattern; (b) S-parameter with varying inductances of bonding wires.

To ensure the design's robustness against fabrication variances, two extreme bonding wire heights are also considered: 25 μm and 229 μm. These variations result in inductances of 0.52 nH and 0.93 nH, respectively, with corresponding bandwidths of 5.6 GHz and 4.6 GHz. The ability of the wideband MN to accommodate such variations is a testament to its design resilience. The MN and bonding wires are not the primary limiting factors for bandwidth; instead, it is the antenna array that primarily dictates the bandwidth limitations. This flexibility is particularly valuable in practical applications, where manufacturing deviations can impact the performance of high-frequency systems.

The strategic adoption of the two-stub MN not only enhances the bandwidth but also ensures that the overall system maintains high performance despite potential variations in bonding wire height. This adaptability is crucial for real-world implementations, where precise control of all parameters may not be feasible. By prioritizing a wideband design, the system can maintain its effectiveness across a range of operational conditions, reducing the need for stringent manufacturing controls and enhancing the reliability and consistency of the phased array system.

Overall, the integration of the two-stub MN within the phased array system underscores the importance of innovative design in achieving robust and flexible RF solutions. By addressing potential challenges such as variable bonding wire heights, the design not only meets performance targets but also sets a new standard for resilience and adaptability in RF circuit design.

3.4 Experimental Results

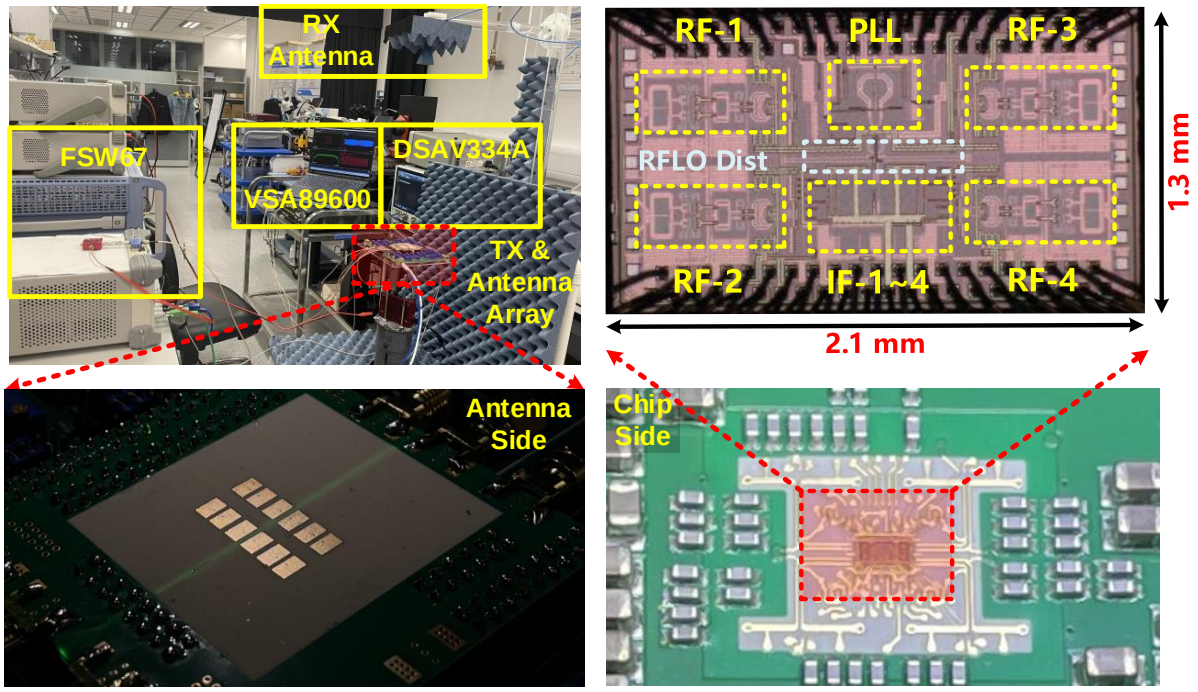
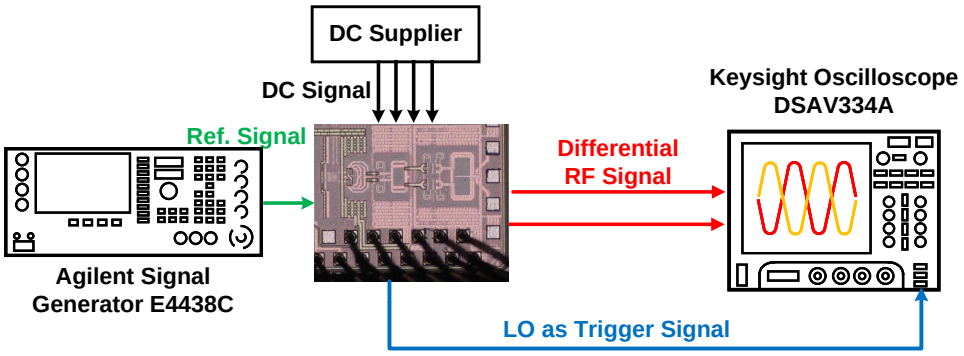


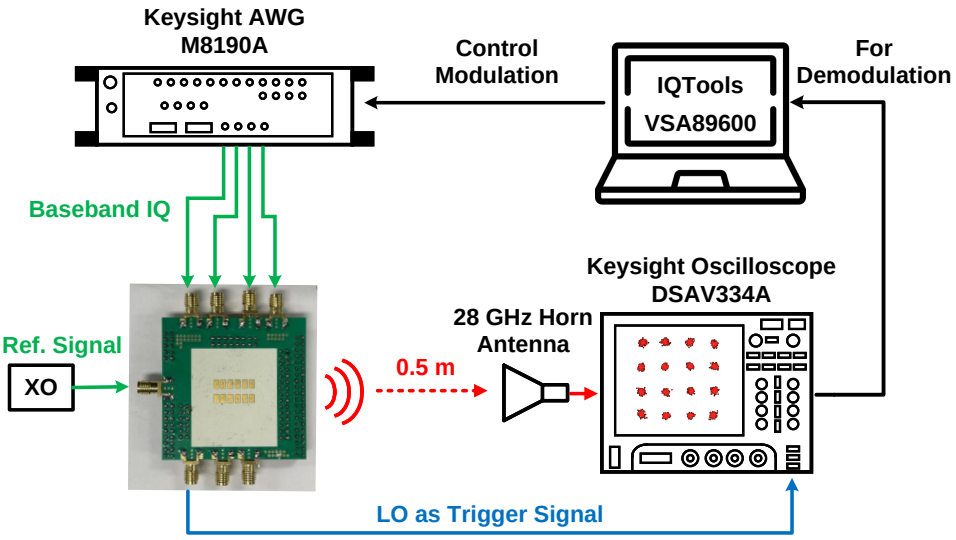
Figure 3.32: Measurement setup, chip diagram, PCB with antenna, MN, and chip packaging.

The TX was prototyped in 40-nm CMOS and measured via probing and over-the-air (OTA). The measurement setup, chip diagram, and PCB design with antenna side and packaging side are presented in Fig. 3.32. Testing involved continuous-wave (CW) measurements of the chip and on-board circuits with differential probes, along with over-the-air (OTA) modulation measurements of the entire system.

The CW measurement setup for the TX is illustrated in Fig. 3.33(a). Four channels of DC signals are provided as differential IQ inputs. An Agilent signal generator (E4438C) generates a reference signal for the on-chip phase-locked loop (PLL) to create the local oscillator signal. A SGS probe connects the differential RF signal output. The output power of the TX is measured using a Keysight oscilloscope (DSAV334A). The modulation measurement setup for the TX and on-board circuits is depicted in Fig. 3.33(b). A Keysight arbitrary waveform generator (AWG) M8190A generates baseband IQ differential signals, while a crystal oscillator (XO) supplies a low-noise 250-MHz reference for the on-chip PLL. A horn antenna receives the wireless signal at a distance of 0.5 m, with the received signal captured by the Keysight oscilloscope (DSAV334A). A computer equipped with Keysight IQ tools and VSA89600 controls the AWG and oscilloscope for modulation and demodulation.



(a)



(b)

Figure 3.33: Measurement setups for characterizing: (a) On-probe performance with CW signal; (b) OTA performance with modulated signal.

3.4.1 Key Building Blocks

PA and the Antenna Array

The measured large-signal performance of the RF front-end at 28 GHz is shown in Fig. **??**. A saturation power (P_{sat}) of 20.0 dBm is recorded, with a 1 dB compression point (P1dB) of 18.54 dBm, a peak drain efficiency (DE) of 30.2%, and an estimated gain of 30.2 dB. This efficiency accounts for additional resistances from PCB traces and bonding wires in the DC voltage supply path. The varying gain curves with changes in VB_1 are displayed in Fig. 3.34(b). The flat gain curves at VB_1 values of 0.24 V and 0.25 V indicate high linearity, confirming the effectiveness of the gain extension scheme using the class-C stage with adjustable bias.

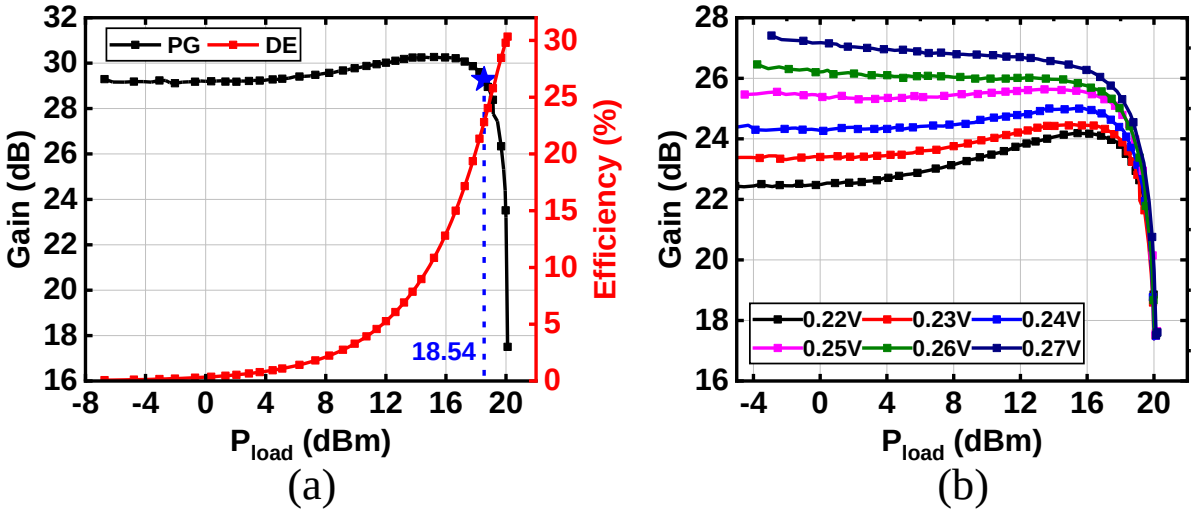


Figure 3.34: RF front-end measured results: (a) Gain and efficiency at 0.23 V of VB_1. (b) Gain versus P_{load} with VB_1 varying from 0.22 to 0.27 V.

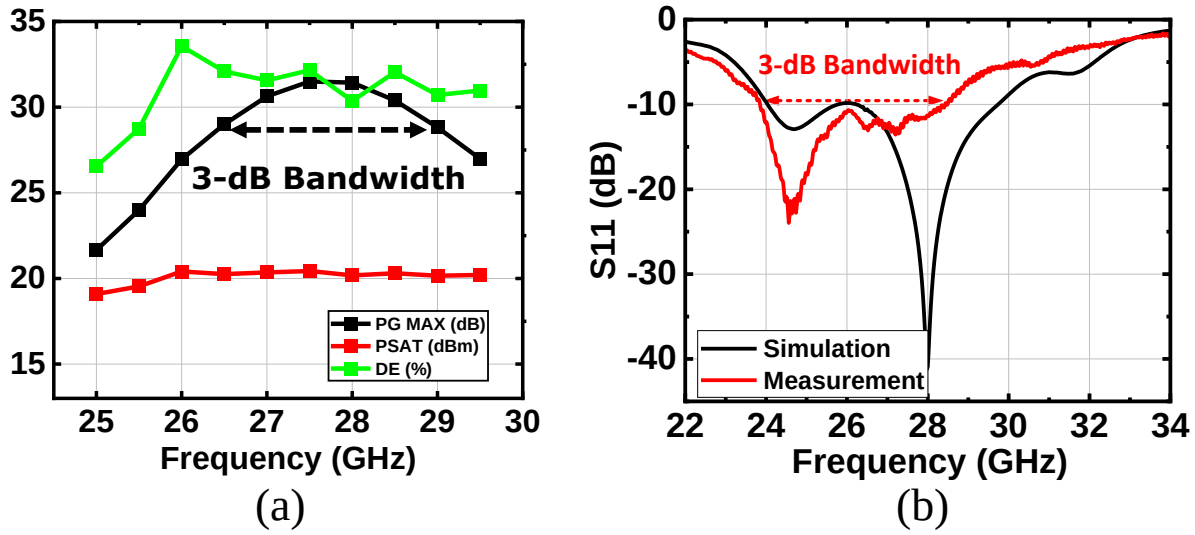
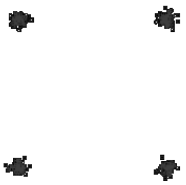
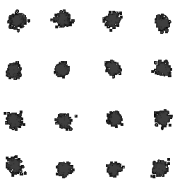
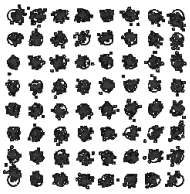


Figure 3.35: (a) RF front-end measured performance from 25.0 to 29.5 GHz; (b) Measured and simulated input matchings of 2-stub MN with the antenna.

Figure 3.35(a) illustrates the bandwidth of the TX. For assessing the large-signal performance over frequency, the reference signal was varied from 220 to 275 MHz. The TX achieves a 3-dB gain bandwidth from 26.5 to 29.0 GHz and a 1-dB P_{sat} bandwidth from 25.5 to 29.5 GHz. Figure 3.35(b) presents the bandwidth of the on-board MN with the antenna array, measured using a GSSG air coplanar probe with a 250 μm pitch. The measured 10-dB bandwidth is 4.3 GHz, spanning from 24.0 to 28.3 GHz, with results closely matching the simulations.

The demodulated constellations and corresponding EVM for various modulation schemes are summarized in Table 3.2. At an 800 Ms/s symbol rate, the EVM values are -24.9 dB (5.7%), -26.6 dB (4.7%), and -27.5 dB (4.2%) for 4-QAM, 16-QAM, and 64-QAM, respectively.

Table 3.2: Summarized constellation and EVM in 0.5-m OTA measurement.

Modulation	4-QAM	16-QAM	64-QAM
Symbol Rate	800 MS/s	800 MS/s	800 MS/s
EVM	-24.9 dB (5.7%)	-26.6 dB (4.7%)	-27.5 dB (4.2%)
Constellation			

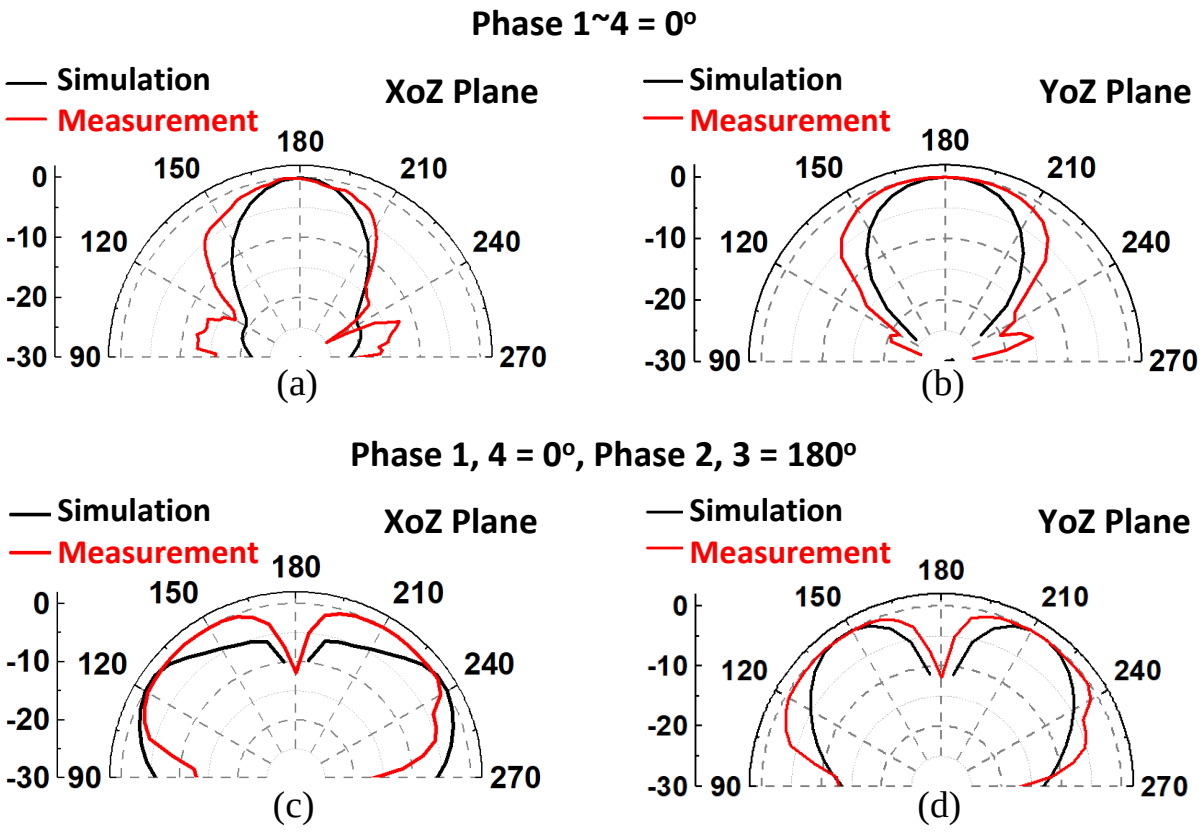


Figure 3.36: When all elements are in the same phases, the 4-element phase array radiation patterns in: (a) XoZ plane; (b) YoZ plane. When all the neighbouring elements are in opposite phases, the 4-element phase array radiation patterns in: (c) XoZ plane; (d) YoZ plane.

The radiation patterns of the 2×2 array are illustrated in Fig. 3.36. When all four elements are in phase, a beam angle of 180° is achieved. When elements 2 and 3 are 180° out of phase with

elements 1 and 4, the beam angles shift to 120° and 240°. Measurements align with simulation results, confirming a beam steering range of 120°.

Table 3.3 compares this work with state-of-the-art CMOS TX/PA performance at similar frequencies [43, 44, 93–98]. This PA, noted for its compact size, achieves the highest power gain, good output power, linearity, and efficiency. Considering P_{sat}, gain, frequency, and efficiency, this work achieves an ITRS figure of merit (FoM) of 94.0, the highest among comparable works. In terms of area, this design also achieves the highest power density.

Table 3.3: Performance Summary and Comparison with State-of-the-Art MM-Wave Silicon-Based PAs/TXs.

	RFIC'24 [92]	**RFIC'23 [93]**	**ISSCC'22 [94]**	**TMTT'21 [95]**	**ISSCC'24 [96]**	**JSSC'22 [42]**	**JSSC'21 [97]**	**JSSC'19 [43]**	**Our Work**
Technology	65 nm CMOS	45 nm CMOS SOI	55 nm CMOS	65 nm CMOS	45 nm CMOS SOI	65 nm CMOS	45 nm CMOS SOI	65 nm CMOS SOI	**40 nm CMOS**
Architecture	1-stage CS+1-stage stack	2-stage CS, 4-way	Cascode, 3-way Doherty	1-stage CS+1-stage Cascode	1-stage CS+1-stage stack Doherty	2-stage CS+1-stage Cascode	1-stage Cascode	2-stage CS	**1-stage CS+1-stage stack**
TX or PA	PA	PA	PA	PA	TX	TX	TX	TX	**TX**
Supply (V)	-	1.2	2.4	2.2	2.2	1.8	2	2	**2.1**
Freq. (GHz)	27	26	28	31	28	26	29	28	**28**
PA Gain (dB)	20.2[#]	22.7	16.1	18.9	20.0[#]	26.8[*]	19.8[*]	13.5	**30.2**[**]
Psat (dBm)	22.1	23	25.5	17.1	20.3[#]	18	22.7	17.7	**20**
P1dB (dBm)	19.4	20.2	24.3	15.0[#]	19.7[#]	17.4[*]	17.1[#]	16.1	**18.5**
Peak PAE (%)	34.4	41	25.2	38.2	30.0[#] (DE)	46.0[*]	41.3	30.6	**30.3 (DE)**
QAM Scheme	64	64	64	64	64	64	64	64	**64**
Symbol Rate (MS/s)	-	250	250	400	800	400	500	2500	**800**
Distance (m)	On-wafer	On-wafer	On-wafer	On-wafer	On-wafer	On-wafer	On-wafer	5	**0.5**
EVM (dB)	-30	-25.8	-25.2	-30	-25	-25	-25.3	-27.9	**-27.5**
PA Area (mm^2)	0.23	0.39	0.54	0.16	0.14	0.9 x 0.6[#]	0.8 x 0.6[#]	0.18	**0.5 x 0.2**
PA Power Density[***] (W/mm^2)	0.71	0.51	0.66	0.32	0.77	0.11	0.39	0.33	**1**
FOM (ITRS)[##]	86.2	90	83.9	81.7	84	89.7	87.9	89.9	**94**

[#]Estimated from figure. [*]Simulation. [**]Estimated from TX gain. [***]Power density = P_{sat}/core area.
[##]FoM (ITRS) = P_{sat} [dBm] + Gain [dB] + 20log(Freq. [GHz]) + 10log(PAE_{peak} [%])

PLL

The PLL occupies an area of 0.126 mm^2, including all loop filter capacitors. The core circuit, comprising the active circuitry, integration capacitor, and inductor, occupies an area of 0.057 mm^2. The power supplies are distributed through an on-board low dropout regulator. The VCO operates at a voltage supply of 0.8 V to improve reliability and reduce power consumption, while all other blocks are powered at 0.9 V.

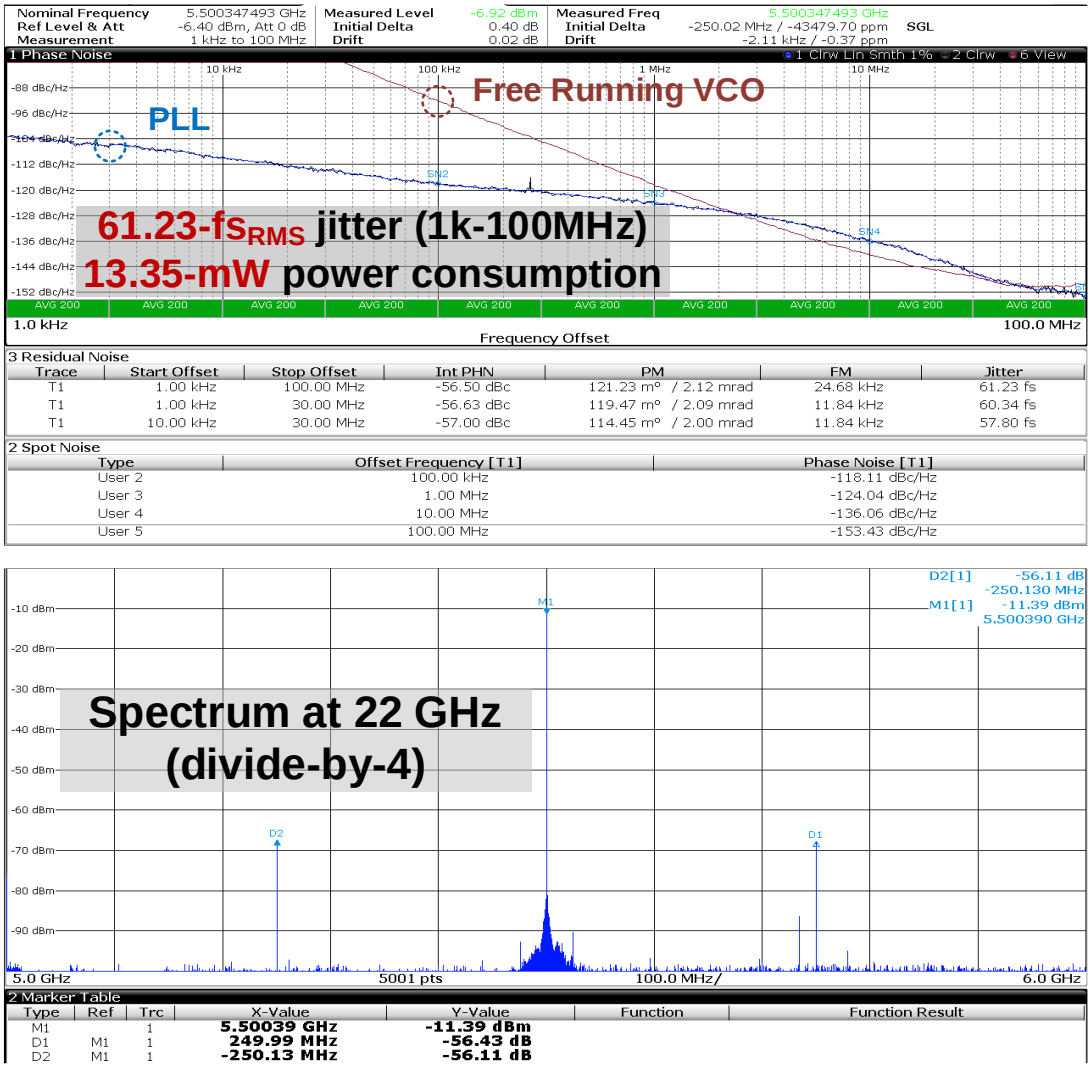


Figure 3.37: Measured phase noise, RMS jitter and spectrum.

The measured PN of the free-running class-C VCO and PLL, as well as the PLL spectrum after divide-by-4, are displayed in Fig. 3.37. The PNs of the free-running VCO at 1 MHz and 10 MHz are -106.2 and -127.9 dBc/Hz, yielding competitive VCO FoMs of 184.5 and 186.3 dB under 7.4-mW power consumption, respectively. Integrated from 1 kHz to 100 MHz, the DPSSPLL achieves an RMS jitter of 61.23 fs using a 250-MHz input reference signal. The measured spectrum shows a reference spur of -44.11-dBc at a 250-MHz frequency offset from

the center frequency. Considering both the jitter and power consumption, the PLL achieves a FoMjitter of -253.0 dB.

Figure 3.37 illustrates the spectrum at 22 GHz after passing through a DIV-4 circuit. The spectrum reveals a peak at 5.5 GHz, accompanied by two spurs offset by the reference frequency of 250 MHz. The measured spur levels are -44 dBc. Typically, spurs in the integer-N PLL can arise due to the feedback sampling signal from the SSPD, or due to voltage mismatches in the proportional path. In this work, the latter is the primary cause, as the TSPC divider and SS buffer together provide sufficient isolation between the SSPD and the VCO. Mismatches between the P and N input MOSFETs of the SSCP in the I-Path can lead to offset voltage in the SSPD output. This voltage offset manifests as a common-mode difference between the P and N sides in the P-Path. Consequently, such a common-mode difference translates to spurs in the oscillator control voltage during the neutralization process. Furthermore, since the PLL is part of a transmitter chip, the long reference distribution chain can introduce power supply disturbances that contribute to the spur levels.

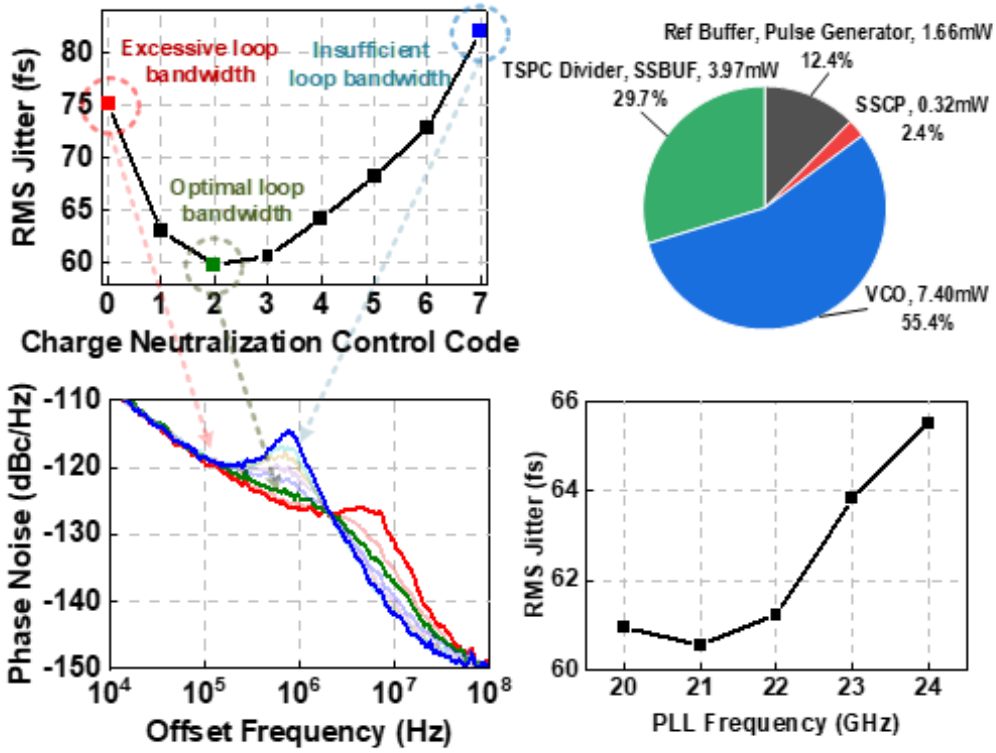


Figure 3.38: Measured RMS jitters and phase noises over different charge neutralization control codes; PLL power breakdown; RMS jitter versus PLL frequency.

To investigate the effectiveness of the proposed charge-domain gain control scheme, phase noise profiles were measured under different gain control states at 22 GHz, by varying the 3-bit

charge neutralization code from 0 to 7. The measured integrated jitter and phase noise profiles are shown in Fig. 3.38. As the charge neutralization capacitance increases, the PLL phase noise is initially dominated by reference phase noise due to excessive bandwidth (red dot in Fig. 3.38), and eventually dominated by VCO phase noise due to insufficient bandwidth (blue dot in Fig. 3.38). Optimal RMS jitter is achieved when $2C_U$ is involved in the charge neutralization, allowing for a balanced contribution of reference and VCO phase noises (green dot in Fig. 3.38). Referring to Fig. 3.38, the estimated bandwidth under this state is approximately 4 MHz.

The phase noise profiles measured across the PLL tuning range are summarized in Fig. 3.38. Throughout the tuning range from 20 GHz to 24 GHz, the integrated jitter maintains consistent performance, varying only slightly from 60.55 fs at 21 GHz to 62.02 fs at 23 GHz.

The power breakdown of the PLL is depicted in Fig. 3.38, highlighting that the majority of power consumption is attributed to the VCO. A significant portion is also allocated to the SSBUF, which is responsible for driving the sampling capacitors and achieving a high SSPD gain.

3.4.2 System

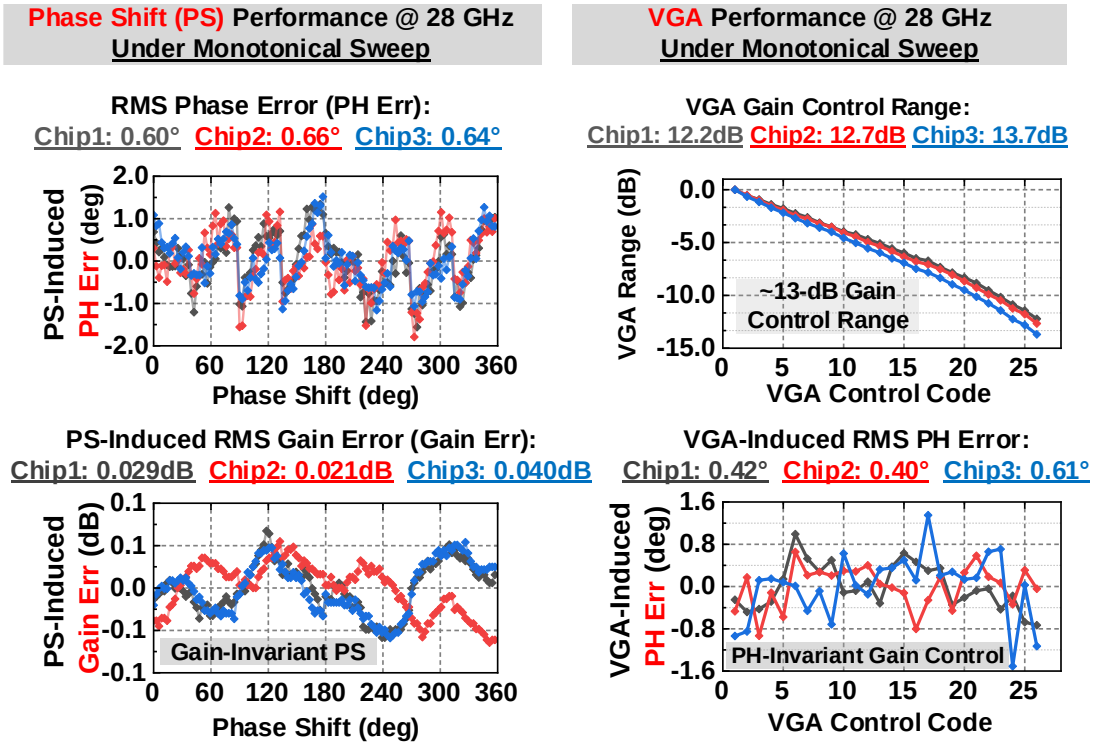


Figure 3.39:
Measured phase shifting and gain control performance under monotonical sweeping at 28 GHz.

The phase shifting (PS) and gain control performances are measured for three consecutive samples at 28 GHz in Fig. 3.39. By controlling the IFLO phase shifter to sweep across 360°/7-bit monotonically, the RMS PS-induced phase error (PH ErrRMS) and gain ErrRMS at 28 GHz are 0.63° and 0.03 dB, respectively, showcasing good linearity with minimal gain variation. By controlling the VGA, the TX achieves a gain control range of 13 dB, inducing a RMS phase variation of only 0.48° at 28 GHz. Next, by sweeping across 25 30 GHz, the TX exhibits consistent performances: a PS-induced PH ErrRMS of 0.63° 0.84°, a PS-induced gain ErrRMS of 0.021 0.046 dB, and a VGA-induced PH ErrRMS of 0.30° 0.64°, as shown in Fig. 3.40. The measurement results demonstrate that the proposed TX is capable of achieving both gain-invariant phase shifting, as well as phase-invariant gain control.

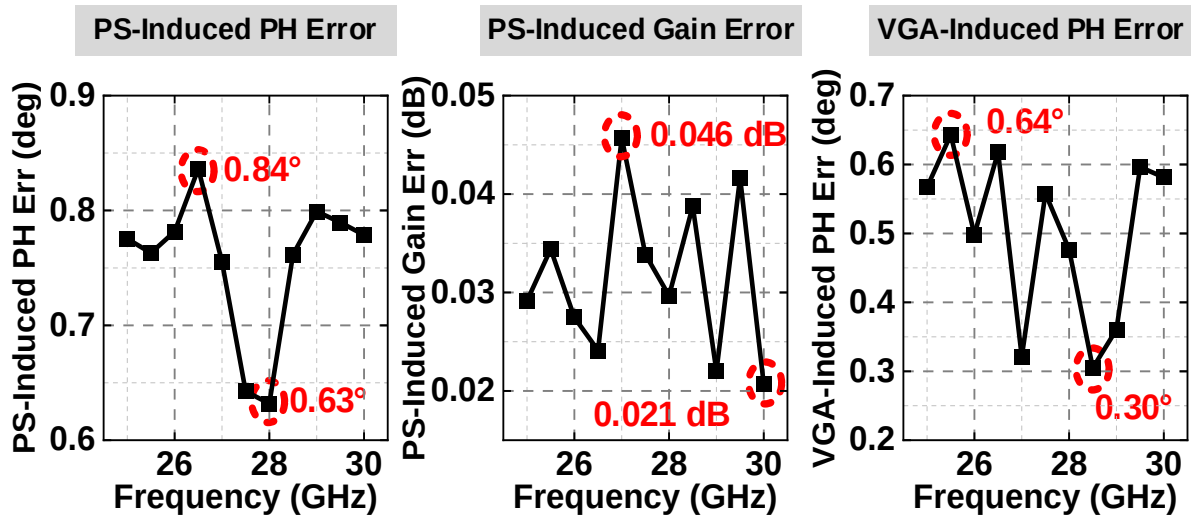


Figure 3.40: Measured phase shifting-induced phase and gain error, and variable gain control-induced phase error across 25~30-GHz frequency range.

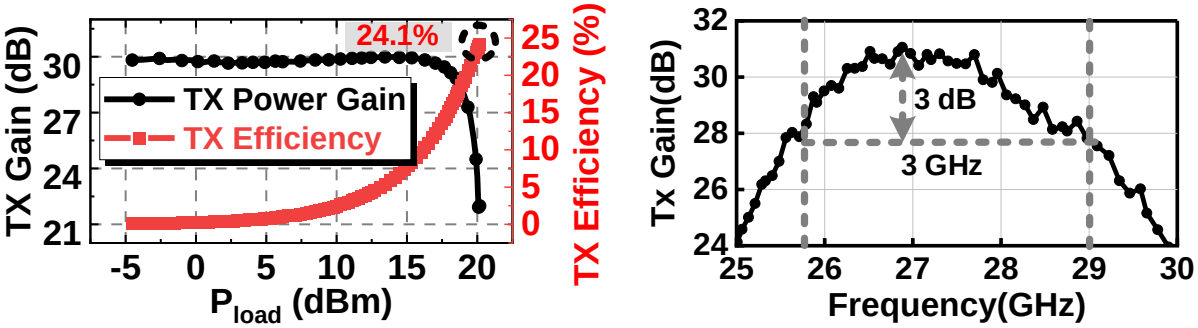


Figure 3.41: Measured TX gain and power efficiency.

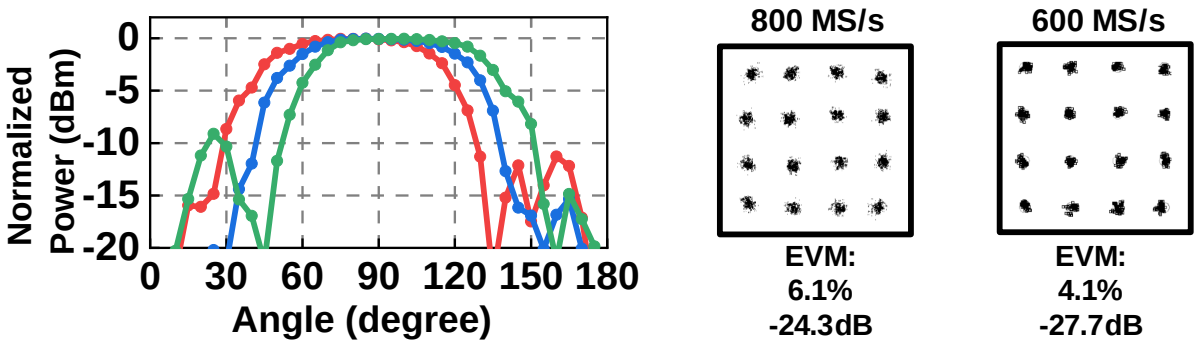


Figure 3.42: Measured
beamsteering performance, constellation diagrams under 800 MS/s and 600MS/s sample rate.

Fig. 3.41 presents the TX gain and power efficiency via on-wafer probing measurement. Thanks to the concise mmWave path, the TX achieves a peak power efficiency of 24.1%, under a saturated output power of 20.2 dBm. The measured peak gain and 3-dB bandwidth are 30.0 dB and 3 GHz, respectively. The OTA measurement results are presented in Fig. 3.42. Beam-steering patterns are demonstrated with the 2×2 array. The EVMs for 16-QAM signals at 600-MS/s and 800-MS/s sampling rates are -24.3 dB and -27.7 dB, respectively. The power and area breakdowns are shown in Fig. 3.43.

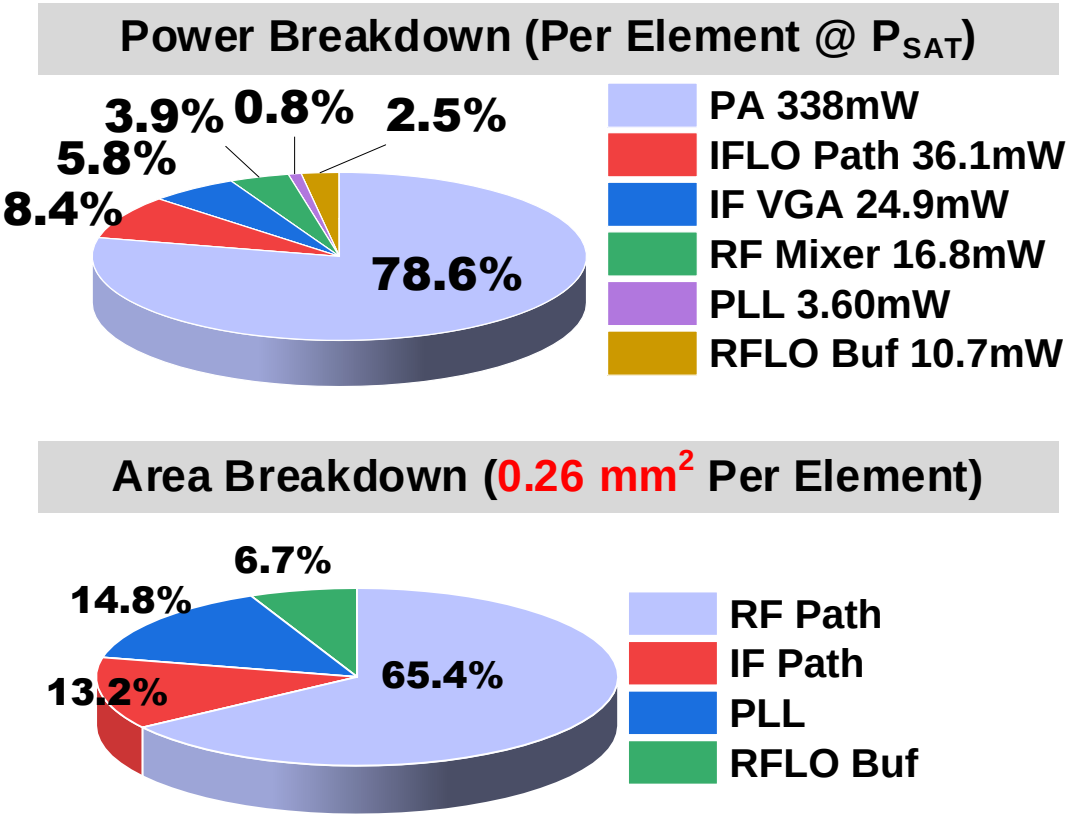


Figure 3.43: Power and area breakdown.

Table 3.4 compares this work with the state-of-the-art, showing that the proposed TX achieves

highly linear PS with minimal PS-induced gain error, and gain control-induced phase error. The TX demonstrates a superior 24.1% peak system efficiency and 0.26-mm^2/element area efficiency (IF, RF, PLL all included).

Table 3.4:
Performance Summary and Comparison with State-of-the-Art MM-Wave Silicon-Based TXs.

	ISSCC2019 [46]		ISSCC2022 [48]	JSSC2018 [44]	JSSC2019 [47]	JSSC2021 [42]	This work
Tech.	65nm CMOS		130nm BiCMOS	180nm BiCMOS	65nm CMOS	65nm CMOS	40nm CMOS
Architecture	RF PS + RF VGA		T-Line PS + RF VGA	RF PS + RF VGA	RFLO PS + RF VGA	RF PS + Passive-VGA	**IFLO PS + IF VGA**
LO Gen.	External		External	None	×6 multiplier	None	**On-Chip PLL**
PS Reso.	5	6	~5.5 bits	6 bits	15 bits	6	7 bits
RMS PH Err @ 28GHz	1.2°	1.4°	0.7°	3.7°	0.3°	1.2°	**0.63°**
RMS PH Err / Freq Range	1.0°~1.5° / 24~37GHz		1.2° / 24~30GHz	3.5°~6.4° / 24~36GHz	N/A	1.0°-2.5°	**0.63°~0.84° /25~30GHz**
PS-Induced RMS Gain Err	±0.25 dB		±0.5 dB / 22~30GHz	0.9 dB*	0.04 dB	0.4 dB	**0.021~0.046 dB /25~30GHz**
VGA-Induced RMS PH Err/ VGA Range	<1.4° / 16 dB		±1° / 12 dB 24~30GHz	<2.9° /13.8 dB	N/A	<3.5	**0.30°~0.64° /13 dB 25~30GHz**
VGA-Induced RMS PH Err Normalized by VGA Range	0.0875°/dB		0.164°/dB	0.21°/dB	N/A	<0.11°/dB	**<0.046°/dB**
TX Gain	19 dB*		25~31 dB	20 dB	10 dB	20.3~25.5	**30.0 dB**
P_{SAT} (dBm)	16*		17±0.1	12.5	18	16.8-18.0	**20.2**
TX Peak Eff.	20.3%		23% (FE)	8.9%	17.5%**	4 TRX	**24.1%**
Area (mm^2) / Element	0.67 / element TX+RX		1.2 / element TX+RX	1.64 / element TX+RX	1.85 / element TX+RX	N/A	**0.26 / element TX Core**

*Estimated from figures. **Use P_{DC} at P1dB

3.5 Conclusions

In conclusion, this chapter has detailed the development of a state-of-the-art Ka-band 4-element phased-array TX, integrating a co-optimized wideband chip-antenna interface tailored specifically for phased array systems. The innovative design leverages an IFLO architecture, which excels in power and area efficiency while maintaining linear gain-invariant phase shifting and phase-invariant gain control. The sliding-IF architecture, featuring an on-chip PLL and a divide-by-4 circuit, generates low-phase noise RF and IF local oscillators at 22.4 GHz and 5.6 GHz, respectively. This is essential for achieving high area-efficiency.

The advanced IF path, utilizing a multiplex-and-interpolation-based IFLO phase shifter, allows the TX to maintain exceptional phase accuracy with an RMS phase error between 0.63° and 0.85°, and a minimal RMS gain error of 0.02 to 0.05 dB. The inclusion of a transadmittance-transimpedance IF VGA further enhances the system with a 13-dB gain control range, and an RMS phase error of just 0.3° to 0.6°, ensuring orthogonal phase shifting and gain control. This

advanced architecture significantly decouples the phase shifting with gain control.

By implementing a sliding-IF scheme, the system reduces the RFLO frequency to 22.4 GHz, which facilitates the use of inductor-less RFLO buffers, simplifying the mmWave path. This approach contrasts with direct-conversion architectures that require resonance-mode RFLO buffers. The RF path is streamlined with a simple RF mixer and a two-stage PA, where the first stage employs a class-C architecture with an adjustable bias to introduce gain peaking. This effectively counters compression effects in the second stage, enhancing linearity and system robustness.

Additionally, the chapter introduces a novel design methodology for XF-based MN, supported by thorough mathematical analysis. This methodology advances output power and efficiency beyond conventional simulation capabilities. The strategic placement of the on-board MN between the IC's bonding wire and the antenna, along with the use of two short stubs, mitigates bandwidth reduction caused by bonding wire inductance and extended transmission lines, ensuring optimal signal integrity.

The power amplifier acheives a saturation output power of 20 dBm, a P1dB of 18.5 dBm, and a peak drain efficiency of 30.3%. This performance meets the highest ITRS figure of merit to the best of our knowledge. Moreover, the PA achieves an impressive power density of 1.0 W/mm^2. Consequently, the phased-array TX achieves an outstanding area efficiency of 0.26 mm^2 per element and a peak power efficiency of 24.1%, marking a significant leap forward in phased-array transmitter technology.

Overall, the advancements presented in this chapter represent a substantial contribution to the field of RF engineering, offering a robust, efficient, and scalable solution for future phased-array systems. These innovations pave the way for enhanced communication capabilities in wireless communication systems.

CHAPTER 4

CM FILTER DESIGN FOR HIGH-SPEED PAM-4 TX

The electromagnetic interference (EMI) is generated by the common-mode (CM) noise in differential circuits and has a high risk of degrading other circuits' performance by radiating the disturbance. This paper demonstrates an on-chip filter that suppresses the CM noise while keeping the integrity of the differential-mode (DM) signal. Based on the delay equalizer, this filter provides the benefit of whole spectrum DM constant resistance, which achieves great matching between the off-chip transmission line and the on-chip circuit. The simulation results show that the filter efficiently mitigates the EMI of a 56 Gbps PAM-4 transmitter by suppressing the CM noise up to 18.85 dB at 28 GHz with a core area of 207 μm × 125 μm.

4.1 Introduction

Differential signaling has been widely used with the increasing of the data rate owing to its inherently CM noise suppression and small crosstalk. However, the mismatch of rise and fall time caused by the imbalance in the charging and discharging paths generates CM noise in the differential circuits. That CM noise is radiated in the environment by the connectors, flex cable and electrical-to-optical interface. The interference significantly affects the weak signal of the receivers nearby, which will increase the bit error rate (BER) and caused malfunction.

The active circuit technique for automatic CM noise cancellation as one method to suppress the CM noise. However, it highly increases the complexity of the circuit and induces extra power consumption. Another method adopting off-chip filter suffers from permeability degradation over gigahertz and is hard to precisely suppress the noise at the predetermined frequency point in a high data rate communication system [99]. Benefitting from the smaller size components at high frequency and the fine accuracy of semiconductor process, the on-chip filter is a great candidate to provide suppression at specific frequencies with acceptable area consumption. In this paper, two filters with different CM resonant frequencies are designed. A constant resistance structure is used for getting all the DM signals through without attenuation. The delay equalizer provides a wide range of constant group delay, which is critical for the high-speed communication links. In the design stage, ideal components are firstly used to determine and ad-

just the value of the components. The radio frequency devices based on 40 nm CMOS technique are further utilized to fine tuning the filter. To demonstrate their effects, a high-speed four-level pulse amplitude modulation (PAM-4) transmitter [100] is introduced.

4.2 High-Speed PAM-4 Transmitter

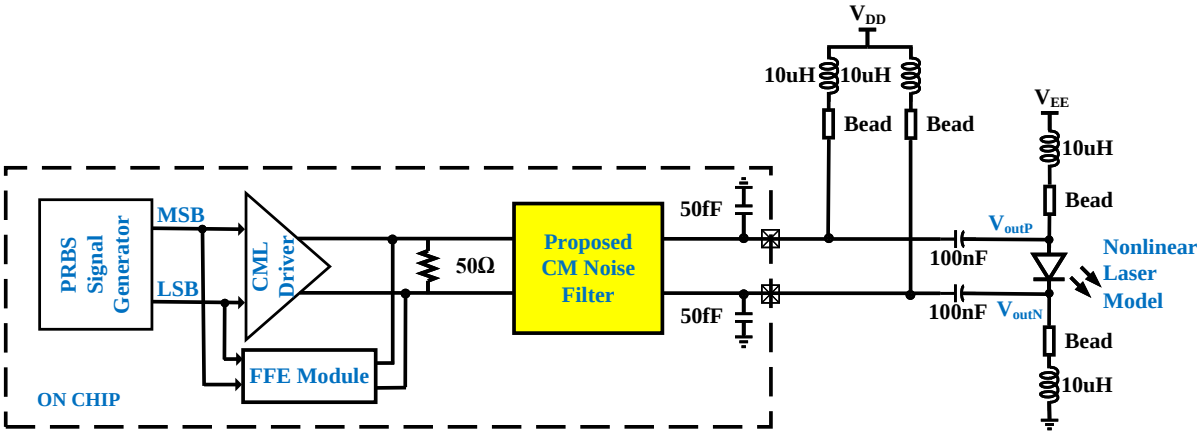


Figure 4.1: Schematic of 56 Gbps PAM-4 optical transmitter with CM filter.

In Fig. 4.1 [100], the 56 Gbps PAM-4 optical transmitter is depicted. The pseudo-random binary sequence (PRBS) generator produces binary data, partitioning it into the least significant bit (LSB) and the most significant bit (MSB). A parallel-connected two-stage common mode logic (CML) driver generates the PAM-4 signal by combining the LSB and MSB signals. Predistortion at the CML driver output is achieved through feed-forward equalization (FFE), enhancing signal quality by mitigating inter-symbol interference (ISI) arising from transient non-linearity and bandwidth constraints of the laser or the channel. Beads are utilized to suppress high-frequency signals from the power source. A differential output connects a non-linear laser model.

The equation below calculates the CM noise resulting from rise and fall time discrepancies in PAM-4 signaling.

$$N\left(2F_{Nyquist}\right)_{CML} = \frac{1}{8} R_F Amp \frac{\left|t_{rise} - t_{fall}\right|}{T_b} sinc^2\left(\frac{\pi}{2}\frac{T_{tr}}{T_b}\right). \tag{4.1}$$

The amplitude (Amp), rise time (t_{rise}), fall time (t_{fall}), data period (T_b), and data transition period (T_{tr}) are vital parameters. The dominant CM noise harmonic occurs at double the Nyquist frequency, guiding the filter design to mitigate CM noise at 28 GHz for the 56 Gbps PAM-4 transmitter.

4.3 Common-Filter

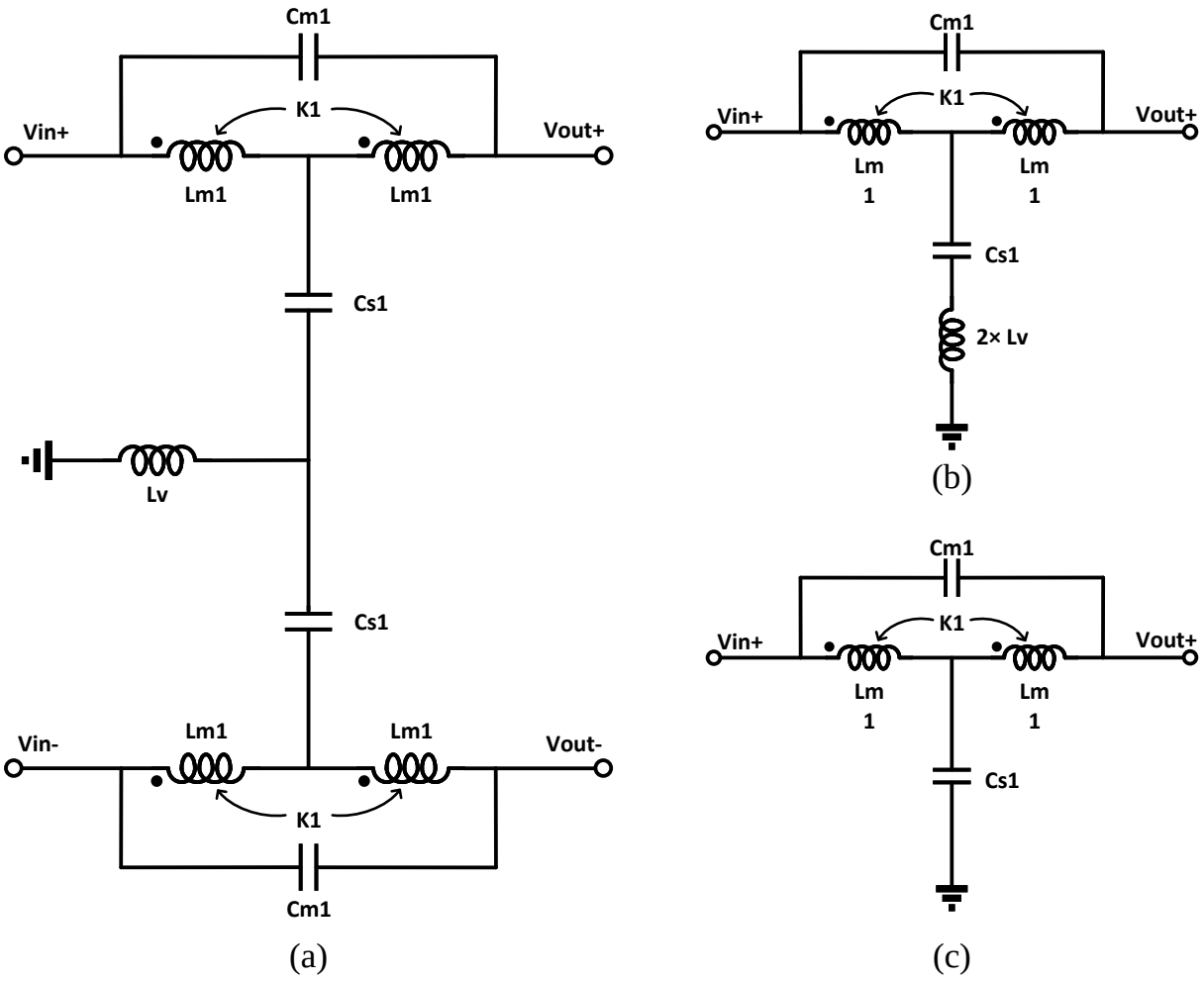


Figure 4.2: Schematics of CM filter. (a) Whole filter. (b) CM half circuit. (c) DM half circuit.

To keep the integrity of the DM signal while suppressing the CM noise at specific frequencies, a delay equalizer [101] is adopted as DM half circuit of the filter. An inductor is added in the CM half circuit path to provide two resonant valleys of the transmission coefficient. As the Fig. 4.2 shows, the filter is analyzed in CM and DM separately, which achieves CM suppression at two specified frequencies and DM constant group delay over a large frequency range.

4.3.1 DM Half Circuit Design

For the DM half circuit depicted in Fig. 4.2(c), according to the design of 2-stage delay equalizer in [101]. The elements are calculated by:

$$
\begin{aligned}
K_1 &= \frac{1-Q^2}{1+Q^2} \\
L_{m1} &= \frac{\left(Q^2+1\right)R}{2Q\omega_r} \\
C_{s1} &= \frac{2}{Q\omega_r R} \\
C_{m1} &= \frac{Q}{2\omega_r R}.
\end{aligned}
\tag{4.2}
$$

Where ω_r is the pole resonant frequency and Q is the pole that are obtained by looking up the table in [101] to achieve the image relationship between the zeros and the poles. R is the constant input impedance over the entire frequency range.

To analyze this delay equalizer, according to the Bartlett's bisection theorem, By applying the two ports with identical voltage generators and identical voltage generators with opposite polarity respectively, Z_{oc} and Z_{sc} are calculated as

$$
Z_{oc} = j\omega\left(L_{m1}+M\right) - j\omega 2M + \frac{1}{j\omega C_{s1}/2},
\tag{4.3}
$$

$$
Z_{sc} = j\omega\left(L_{m1}+M\right) // \frac{1}{j\omega 2C_{m1}},
\tag{4.4}
$$

$$
M = K_1 \times L_{m1}.
\tag{4.5}
$$

These results can be recast in terms of the resonant parameters Q, ω_r, R as:

$$
Z_{oc} = jQR\left(\frac{\omega}{\omega_r} - \frac{\omega_r}{\omega}\right),
\tag{4.6}
$$

$$
Z_{sc} = \frac{R/Q}{j\left(\frac{\omega}{\omega_r} - \frac{\omega_r}{\omega}\right)}.
\tag{4.7}
$$

This means $Z_{oc} \times Z_{sc} = R^2$, and the input impedance can be calculated by

$$
\begin{aligned}
Z_{in} &= \left(Z_{sc}+R\right) // \frac{Z_{oc}-Z_{sc}}{2} + Z_{sc} \\
&= \frac{R\left(Z_{oc}+Z_{sc}\right) + 2Z_{oc}Z_{sc}}{Z_{oc}+Z_{sc}+2R} = R.
\end{aligned}
\tag{4.8}
$$

4.3.2 CM Half Circuit Design

As Fig. 4.2(b) demonstrates, the DM half circuit is a series of the 2-stage delay equalizer and the inductor. Simply treating the delay equalizer as a section of an ideal transmission line with specific group delay τ [100], the transmission zeros can be calculated by

$$Z_{21} = \frac{R}{jsin\omega\tau} + j\omega 2L_v = 0. \tag{4.9}$$

After setting two specified transmission zeros ω_1 and ω_2, the group delay τ for the DM transmission line and L_v for suppressing the CM noise can be calculated.

4.3.3 Simulation Results

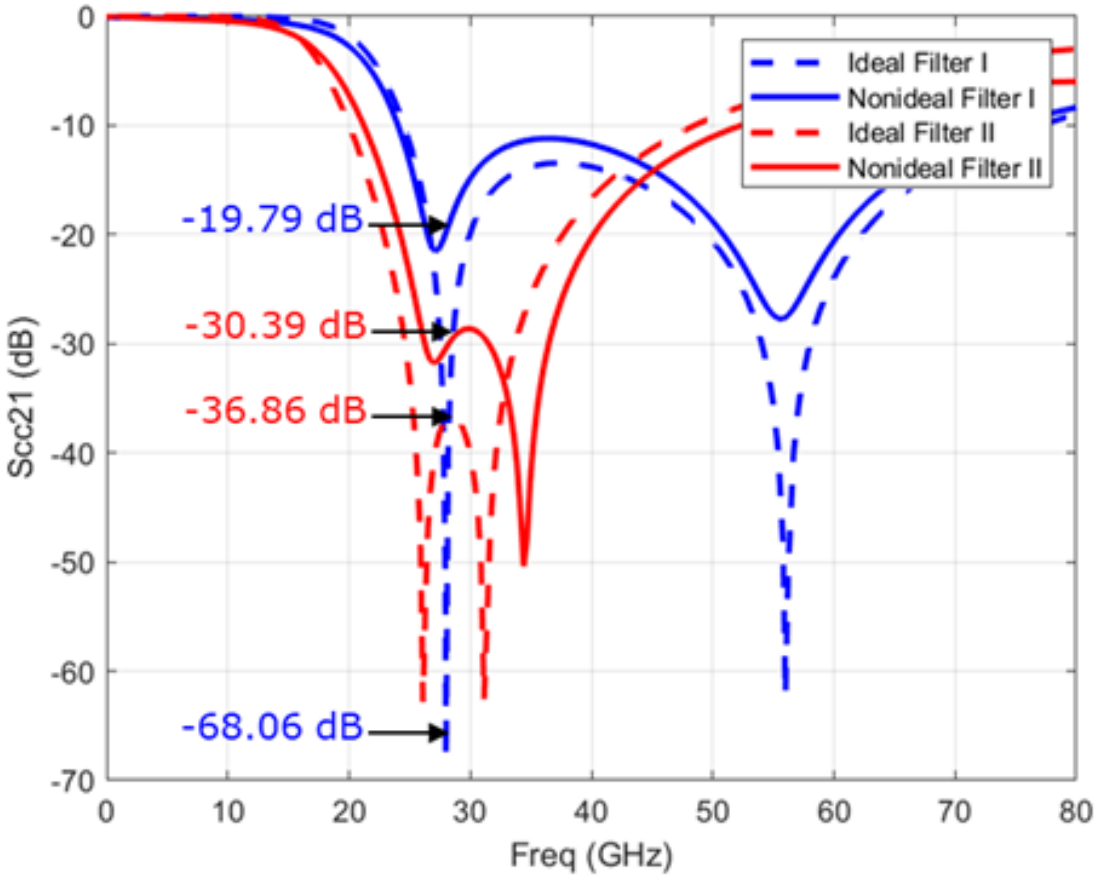


Figure 4.3: The CM transmission coefficient simulation results of filter I and filter II with ideal components and nonideal components.

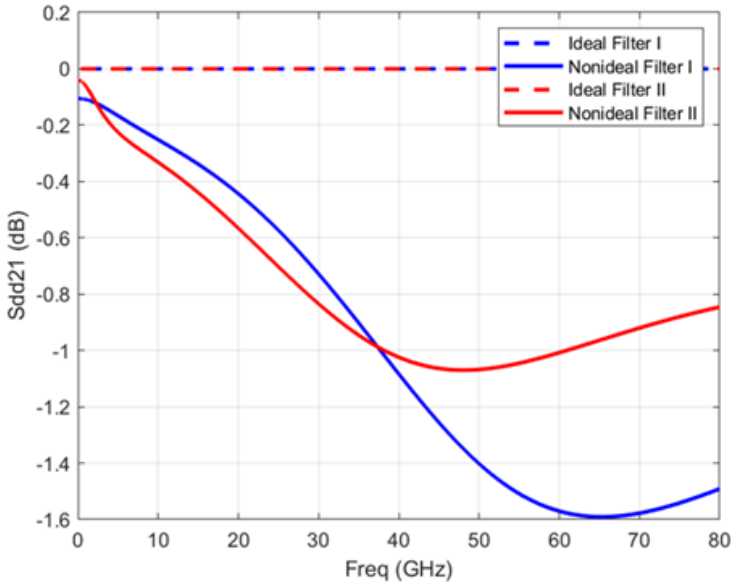


Figure 4.4: The DM transmission coefficient simulation results of filter I and filter II with ideal components and nonideal components.

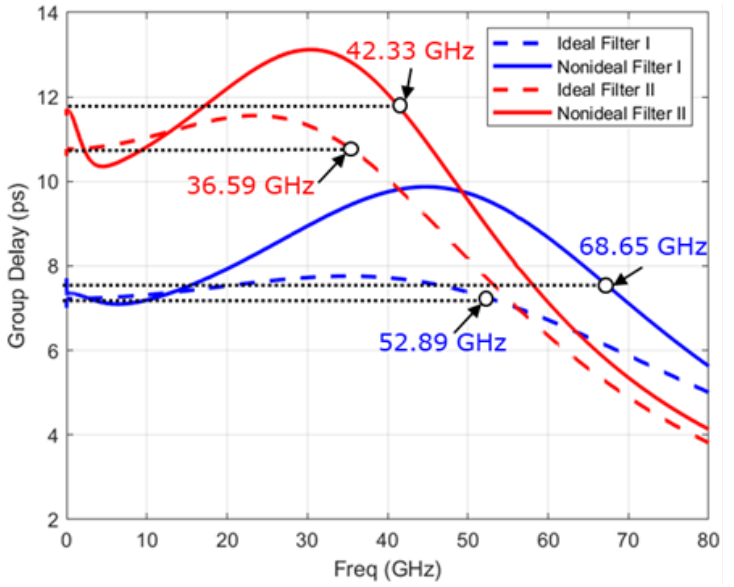


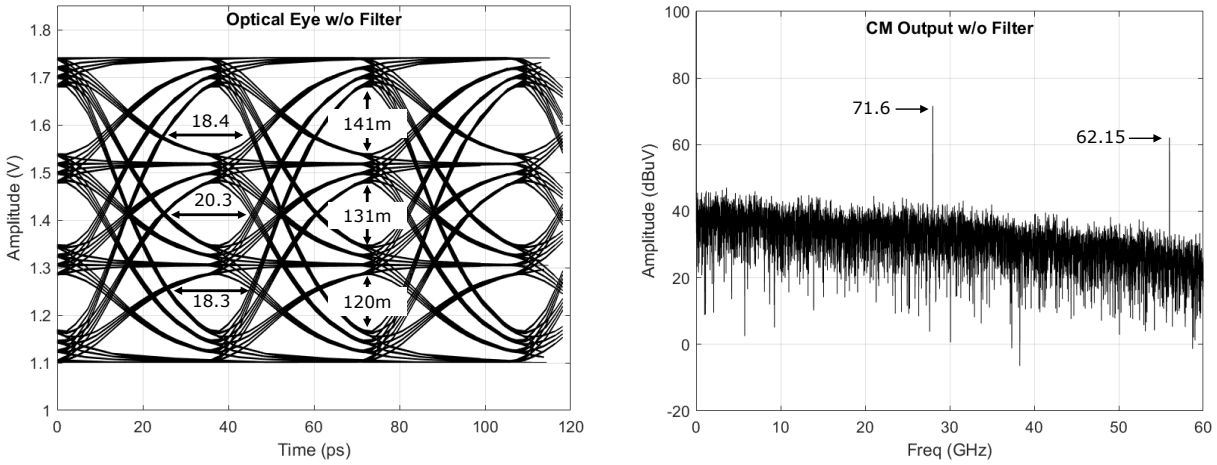
Figure 4.5: The DM group delay response of filter I and filter II with ideal components and nonideal components.

Based on the equation 4.2-4.9, filter I with the CM resonant at 28 GHz and 56 GHz, and filter II with the CM resonant at 26 GHz and 31 GHz are designed. The simulation results are depicted in Fig. 4.3-4.5.

As Fig. 4.3 shows that filter I with ideal components can achieve best suppression at 28 GHz. However, the parasitic of the nonideal components prevent the filter to precisely resonant at 28 GHz, which only provides 19.79 dB of CM noise suppression. Thus, the filter II is designed to resonate not exactly at 28 GHz, which is more tolerant of the parasitic of the components.

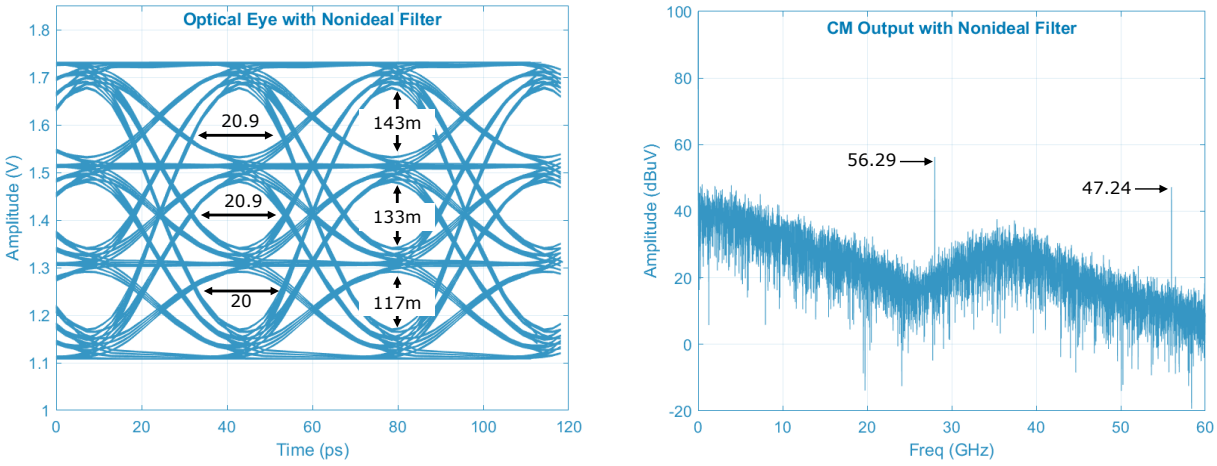
Figure 4.4 demonstrates the parasitic effect on DM transmission. Both of the two filters suffer from a severe degradation to 1 dB at around 40 GHz. The frequency range of constant group delay increases due to the parasitic but the ripple is also increased, which is shown in Fig. 4.5. And filter I has better performance in terms of the group delay, which is 68.65 GHz and can add less distortion to the DM signal.

4.4 Whole System Simulation



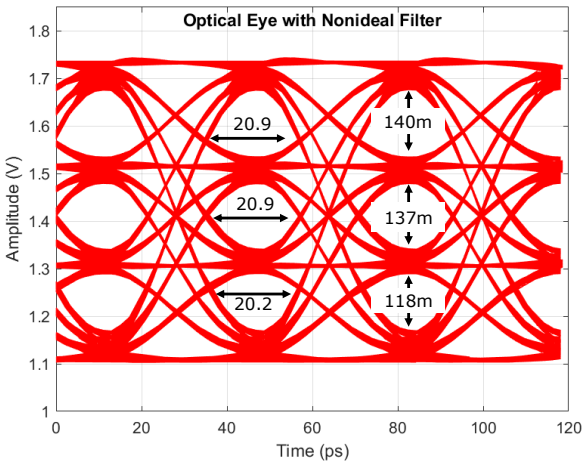
(a) (b)

Figure 4.6: The PAM-4 optical transmitter w/o FFE and filter. (a) Optical output eye diagram. (b) CM noise spectrum.

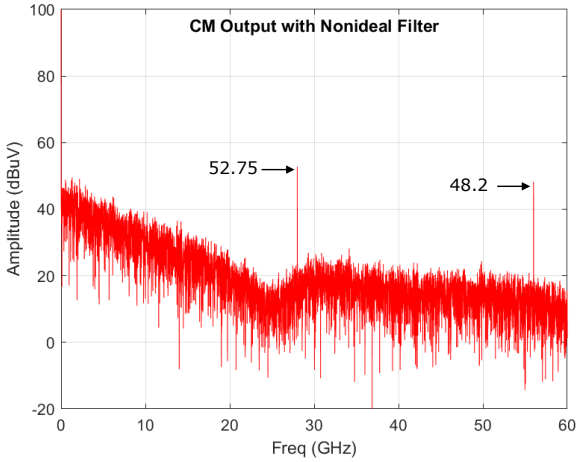


(a) (b)

Figure 4.7: The PAM-4 optical transmitter w/o FFE. (a) Optical output eye diagram with nonideal filter uppercasei. (b) CM noise spectrum with nonideal filter uppercasei.



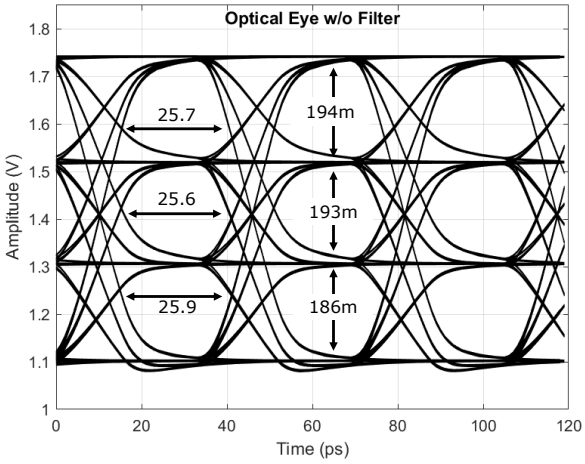
(a)



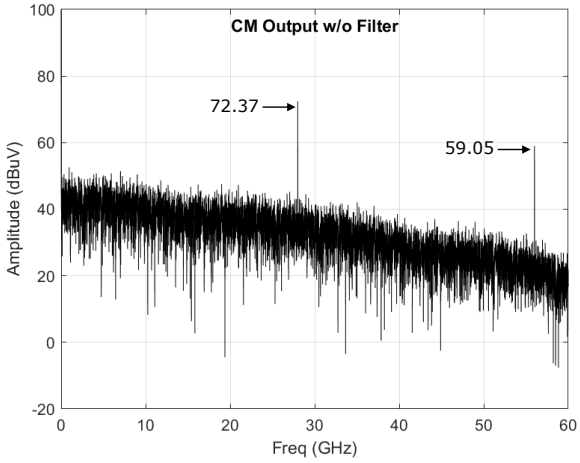
(b)

Figure 4.8: The PAM-4 optical transmitter w/o FFE. (a) Optical output eye diagram with nonideal filter uppercaseii. (b) CM noise spectrum with nonideal filter uppercaseii.

The filter is proposed between the pads and the driver output to suppress the CM noise and achieve impedance matching of the on-chip circuit and off-chip transmission line simultaneously. Eye diagram is used to evaluate the integrity of the DM signal. The spectrum of CM output presents the suppression effect of the CM noise by the filter.

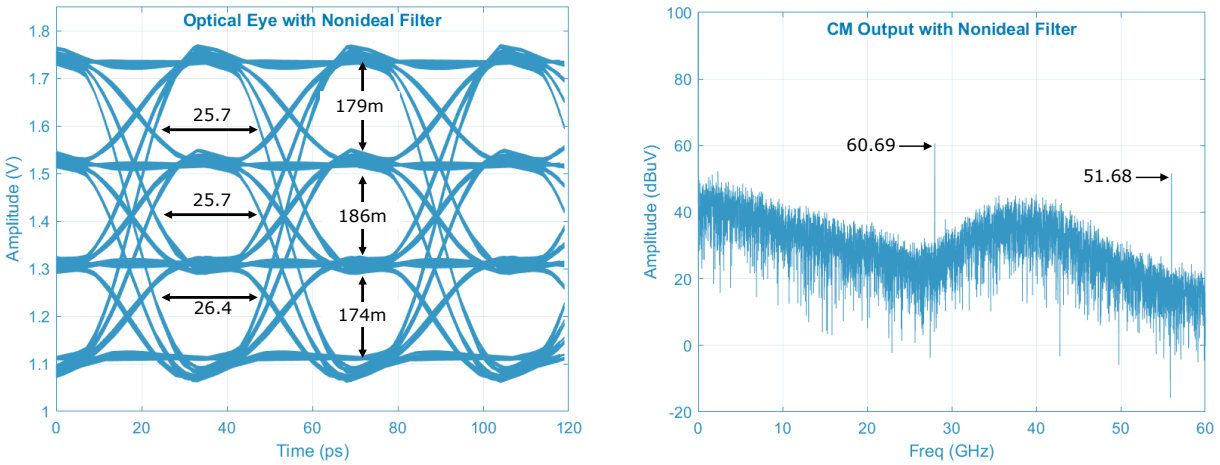


(a)



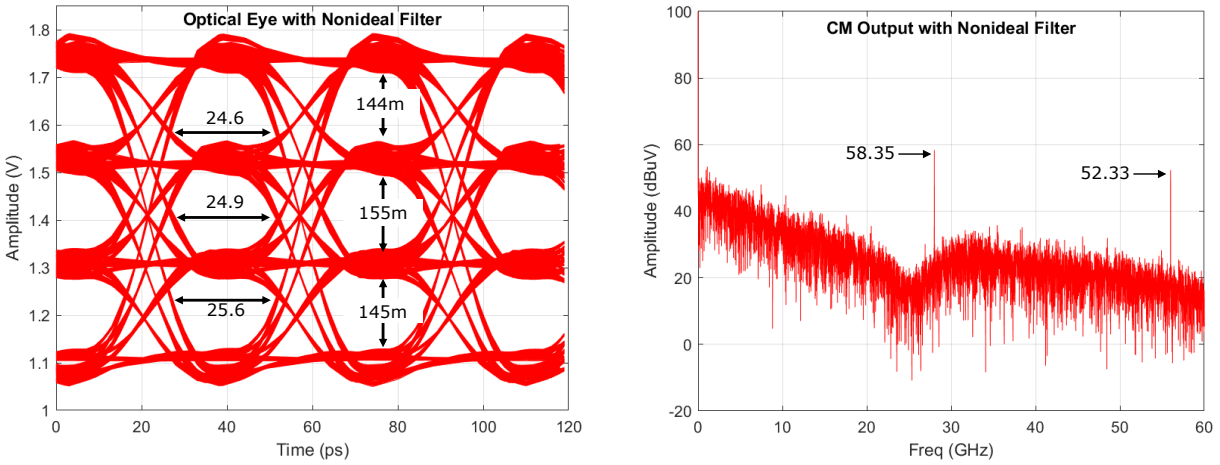
(b)

Figure 4.9: The PAM-4 optical transmitter with FFE and filter. (a) Optical output eye diagram. (b) CM noise spectrum.



(a) (b)

Figure 4.10: The PAM-4 optical transmitter with FFE. (a) Optical output eye diagram with nonideal filter uppercasei. (b) CM noise spectrum with nonideal filter uppercasei.



(a) (b)

Figure 4.11: The PAM-4 optical transmitter with FFE. (a) Optical output eye diagram with nonideal filter uppercaseii. (b) CM noise spectrum with nonideal filter uppercaseii.

Simulation results of the transmitter with or without FFE and with different filters are shown in Fig. 4.6-4.11. Table 4.1 summarizes the performance of the transmitter under different configurations. For the transmitter without FFE, both filter i and filter ii can well preserve the DM signal. While for the transmitter with FFE, filter ii distorts the DM signal due to the limited frequency range of the constant group delay. However, this situation can be compensated by adjusting the FFE circuit based on the different filters.

Filter ii achieves better CM noise suppression because of the relatively wide suppression frequency range of around 28 GHz. Due to the high-frequency port impedance mismatch, the suppression effect at 56 GHz shows less matching with the simulation results of the filter, which makes designing CM resonant around 28 GHz practical.

Table 4.1: Summary table of the transmitter under different configurations.

		Without FFE					With FFE				
		w/o Filter	With Filter I		With Filter II		w/o Filter	With Filter I		With Filter II	
			Ideal	40 nm	Ideal	40 nm		Ideal	40 nm	Ideal	40 nm
Optical Output	Eye Width (ps)	19	21.4 (+12.81%)	20.6 (+8.42%)	21.3 (+12.28%)	20.7 (+8.77%)	25.7	25.9 (+0.78%)	25.9 (+0.78%)	25.2 (-2.07%)	25.0 (-2.72%)
	Eye Height (mV)	131	149 (+14.29%)	131 (+0.26%)	156 (+19.13%)	132 (+0.77%)	191	190 (-0.7%)	180 (-5.93%)	168 (-12.04%)	148 (-22.51%)
CM Noise Output	@ 28 GHz (dBuV)	71.6	50.42	59.29	43.34	52.75	72.37	52.04	60.69	50.36	58.35
	@ 56 GHz (dBuV)	62.15	49.24	47.24	54.18	48.2	59.05	54.17	51.68	59.43	52.33

4.5 Conclusions

The proposed on-chip filter in this paper can effectively suppress the CM noise up to 18.85 dB while slightly increasing the quality of the DM signal with a core area of 207 μm × 125 μm. From the comparison among different filters, the filter that provides CM suppression over a frequency range has better performance.

CHAPTER 5

CONCLUSION AND FUTURE WORK

This thesis explores the development of high-frequency CMOS transmitters to meet the growing demand for high data-rate communication in wireless and optical systems. It thoroughly examines the challenges posed by increased system sizes and proposes architectural and circuit-level solutions to achieve the desired performance.

To enhance design efficiency and reduce the significant costs associated with IC fabrication, an integrated system evaluation engine is introduced. This engine assesses the entire system with complex modulated signals before fabrication, increasing the likelihood of successful chip design and offering valuable insights for individual components.

The thesis presents a power-efficient, compact Ka-band 4-element transmitter, alongside a co-optimized wideband chip-antenna interface that achieves orthogonality between phase shift and gain control for phased-array systems. Utilizing a sliding intermediate frequency structure and phase shifting in the intermediate frequency local oscillator signal, the transmitter achieves an impressive RMS phase error of 0.63° to 0.85° and a minimal RMS phase shift-induced gain error of 0.02 to 0.05 dB. This design reduces chip size by limiting inductor use to only the power amplifier and local oscillator buffers. Additionally, a thorough loss analysis of the transformer-based matching network and a gain extension scheme using a class-C first stage amplifier with adjustable bias enable the power amplifier to reach 18.5 dBm P1dB, 30.3% peak drain efficiency, and a power density of 1.0 W/mm². Consequently, the phased-array transmitter achieves a leading area efficiency of 0.26 mm² per element and a peak power efficiency of 24.1%.

The thesis also introduces an antenna array and on-board matching network for the phased-array system. A flipped patch antenna with a pitch of 0.56 wavelengths is designed for differential output. The differential configuration significantly reduces coupling between adjacent elements to -28 dB. By matching the input impedance to the characteristic impedance of the subsequent transmission line, the two-stub matching network achieves a wide bandwidth of 11.4 GHz and accommodates variations in bonding wire lengths.

To address electromagnetic interference issues arising from increased connection density in optical communication, an on-chip common-mode filter is incorporated before the laser driver in the 28-Gbps PAM-4 transmitter. By introducing two transmission zeros at 26 GHz and 31 GHz

in the common-mode path while maintaining the differential-mode circuit as a delay equalizer, this filter reduces common-mode noise by 19 dB at 28 GHz while preserving the integrity of the differential-mode signal.

5.1 Future Work

While the proposed transmitter (TX) for the phased array demonstrates impressive power density, it unfortunately falls short of meeting the output power requirements necessary for satellite communication applications. This limitation can largely be attributed to the intrinsic constraints of CMOS technology, which, while advantageous in terms of integration and cost, does not deliver the high output power needed for effective satellite transmission. As a result, the integration of Gallium Nitride (GaN) power amplifiers (PAs) with CMOS technology emerges as a promising solution. This hybrid approach allows us to leverage the strengths of both technologies—combining the high output power capabilities of GaN with the cost-effectiveness and integration benefits of CMOS. By doing so, we can achieve the desired high output power levels while keeping overall costs manageable.

To further enhance the efficiency of the TX, the implementation of a Doherty power amplifier (PA) configuration is particularly promising. This design, which comprises a main PA and an auxiliary PA, is known for its high efficiency, especially at the power back-off point. However, a significant challenge arises due to the large area required for passive components associated with this configuration, which can complicate the integration into a phased array system. This spatial constraint necessitates innovative design solutions to optimize the footprint of the PA while maintaining performance.

In light of these challenges, the development of a digital PA that incorporates the mixer function and is directly controlled by the baseband signal presents a highly attractive alternative. This approach not only simplifies the overall architecture but also reduces the area required for passive components. Furthermore, the digital PA has the potential to be designed with the assistance of artificial intelligence (AI), allowing for a higher level of automation in the design process. The use of AI in designing digital circuits can lead to more efficient layouts and improved performance metrics, making it a forward-thinking solution in the realm of RF design.

In addition to the challenges faced in power amplification, the implementation of on-chip filters for optical communication systems also encounters significant obstacles. The physical size associated with high-performance filters, combined with high fabrication costs, often prevents them from being effectively integrated into practical systems. To address this issue, a compact

layout for these filters is essential. A well-designed compact filter not only demonstrates the ability to meet the stringent performance requirements of optical communication but also showcases its feasibility for implementation in real-world applications. This balance between performance and size is critical for advancing optical communication technologies, ensuring that they can be effectively utilized in modern communication systems without incurring prohibitive costs.

REFERENCES

[1] *Internet traffic*, https://www.itu.int/itu-d/reports/statistics/2023/10/10/ff23-internet-traffic/ (cit. on p. 1).

[2] *Growth of Internet traffic*, https://edgeoptic.com/global-internet-traffic-growth-forecast-looking-forward-from-2024/ (cit. on p. 1).

[3] *Compliance verification/measurement method for part 30 devices*, https://www.fcc.gov/oet/ea/presentations/files/oct18/4.1-Part-30-mmW-Test-Procedure-RB.PDF (cit. on p. 3).

[4] B. Clerckx, A. Costanzo, A. Georgiadis, and N. Borges Carvalho, "Toward 1G Mobile Power Networks: RF, Signal, and System Designs to Make Smart Objects Autonomous," *IEEE Microwave Magazine*, vol. 19, no. 6, pp. 69–82, 2018. DOI: 10.1109/MMM.2018.2844018 (cit. on p. 4).

[5] B. Clerckx, J. Kim, K. W. Choi, and D. I. Kim, "Foundations of Wireless Information and Power Transfer: Theory, Prototypes, and Experiments," *Proceedings of the IEEE*, vol. 110, no. 1, pp. 8–30, 2022. DOI: 10.1109/JPROC.2021.3132369 (cit. on p. 4).

[6] M. Nariman, F. Shirinfar, A. Papió Toda, S. Pamarti, A. Rofougaran, and F. De Flaviis, "A Compact 60-GHz Wireless Power Transfer System," *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 8, pp. 2664–2677, 2016. DOI: 10.1109/TMTT.2016.2582168 (cit. on p. 4).

[7] A. Hajimiri, B. Abiri, F. Bohn, M. Gal-Katziri, and M. H. Manohara, "Dynamic Focusing of Large Arrays for Wireless Power Transfer and Beyond," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 7, pp. 2077–2101, 2021. DOI: 10.1109/JSSC.2020.3036895 (cit. on p. 4).

[8] A. A. Aziz *et al.*, "Battery-Less Location Tracking for Internet of Things: Simultaneous Wireless Power Transfer and Positioning," *IEEE Internet of Things Journal*, vol. 6, no. 5, pp. 9147–9164, 2019. DOI: 10.1109/JIOT.2019.2928313 (cit. on p. 4).

[9] A. A. Aziz, A. E. Putra, D. I. Kim, and K. W. Choi, "Drone-Based Sensor Information Gathering System With Beam-Rotation Forward-Scattering Communications and Wireless Power Transfer," *IEEE Internet of Things Journal*, vol. 9, no. 13, pp. 11 227–11 247, 2022. DOI: 10.1109/JIOT.2021.3128532 (cit. on p. 4).

[10] *The world runs on Ethernet: The future of higher speeds*, https://www.lightwaveonline.com/directory/components/optical-switches/article/14301154/the-world-runs-on-ethernet-the-future-of-higher-speeds (cit. on p. 5).

[11] J. Goodman, F. Leonberger, S.-Y. Kung, and R. Athale, "Optical interconnections for VLSI systems," *Proceedings of the IEEE*, vol. 72, no. 7, pp. 850–866, 1984. DOI: 10.1109/PROC.1984.12943 (cit. on p. 5).

[12] M. R. Feldman, S. C. Esener, C. C. Guest, and S. H. Lee, "Comparison between optical and electrical interconnects based on power and speed considerations," *Appl. Opt.*, vol. 27, no. 9, pp. 1742–1751, May 1988. DOI: 10.1364/AO.27.001742 (cit. on p. 5).

[13] R. Ballart and Y.-C. Ching, "SONET: now it's the standard optical network," *IEEE Communications Magazine*, vol. 27, no. 3, pp. 8–15, 1989. DOI: 10.1109/35.20262 (cit. on p. 5).

[14] F. Kiamilev, P. Marchand, A. Krishnamoorthy, S. Esener, and S. Lee, "Performance comparison between optoelectronic and VLSI multistage interconnection networks," *Journal of Lightwave Technology*, vol. 9, no. 12, pp. 1674–1692, 1991. DOI: 10.1109/50.108713 (cit. on p. 5).

[15] G. I. Yayla, P. J. Marchand, and S. C. Esener, "Speed and energy analysis of digital interconnections: comparison of on-chip, off-chip, and free-space technologies," *Appl. Opt.*, vol. 37, no. 2, pp. 205–227, Jan. 1998. DOI: 10.1364/AO.37.000205 (cit. on p. 5).

[16] H. Sugita, K. Sunaga, K. Yamaguchi, and M. Mizuno, "A 16Gb/s 1st-Tap FFE and 3-Tap DFE in 90nm CMOS," in *2010 IEEE International Solid-State Circuits Conference - (ISSCC)*, 2010, pp. 162–163. DOI: 10.1109/ISSCC.2010.5434005 (cit. on p. 5).

[17] M. H. Nazari and A. Emami-Neyestanak, "A 15-Gb/s 0.5-mW/Gbps Two-Tap DFE Receiver With Far-End Crosstalk Cancellation," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 10, pp. 2420–2432, 2012. DOI: 10.1109/JSSC.2012.2203870 (cit. on p. 5).

[18] J. Im *et al.*, "A 40-to-56 Gb/s PAM-4 Receiver With Ten-Tap Direct Decision-Feedback Equalization in 16-nm FinFET," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 12, pp. 3486–3502, 2017. DOI: 10.1109/JSSC.2017.2749432 (cit. on p. 6).

[19] P. Upadhyaya *et al.*, "A fully adaptive 19-to-56Gb/s PAM-4 wireline transceiver with a configurable ADC in 16nm FinFET," in *2018 IEEE International Solid-State Circuits Conference - (ISSCC)*, 2018, pp. 108–110. DOI: 10.1109/ISSCC.2018.8310207 (cit. on p. 6).

[20] L. Wang, Y. Fu, M.-A. LaCroix, E. Chong, and A. Chan Carusone, "A 64-Gb/s 4-PAM Transceiver Utilizing an Adaptive Threshold ADC in 16-nm FinFET," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 2, pp. 452–462, 2019. DOI: 10.1109/JSSC.2018.2877172 (cit. on p. 6).

[21] P.-J. Peng, J.-F. Li, L.-Y. Chen, and J. Lee, "6.1 A 56Gb/s PAM-4/NRZ transceiver in 40nm CMOS," in *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, 2017, pp. 110–111. DOI: 10.1109/ISSCC.2017.7870285 (cit. on p. 6).

[22] E. Depaoli *et al.*, "A 4.9pJ/b 16-to-64Gb/s PAM-4 VSR transceiver in 28nm FDSOI CMOS," in *2018 IEEE International Solid-State Circuits Conference - (ISSCC)*, 2018, pp. 112–114. DOI: 10.1109/ISSCC.2018.8310209 (cit. on p. 6).

[23] R. Azmat, L. Wang, K. Q. Maqbool, C. Wang, and C. P. Yue, "Sensing and Cancellation Circuits for Mitigating EMI-Related Common Mode Noise in High-Speed PAM-4 Transmitter," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 68, no. 11, pp. 4545–4555, 2021. DOI: 10.1109/TCSI.2021.3108640 (cit. on p. 6).

[24] J. Li *et al.*, "EMI coupling paths in silicon optical sub-assembly package," in *2016 IEEE International Symposium on Electromagnetic Compatibility (EMC)*, 2016, pp. 890–895. DOI: 10.1109/ISEMC.2016.7571768 (cit. on p. 6).

[25] R. Azmat, "Electromagnetic interference-related common-mode noise analysis and mitigation technique for high-speed pam-4 transmitter," English, Copyright - Database copy-

right ProQuest LLC; ProQuest does not claim copyright in the individual underlying works; Last updated - 2024-09-07, Ph.D. dissertation, 2022, p. 129 (cit. on p. 6).

[26] C.-H. Kye, H.-G. Ko, J. Lee, and D.-K. Jeong, "A 22-Gb/s 0.95-pJ/b Energy-Efficient Voltage-Mode Transmitter With Time-Based Feedforward Equalization in a 28-nm CMOS," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 28, no. 5, pp. 1099–1106, 2020. DOI: 10.1109/TVLSI.2020.2965565 (cit. on p. 7).

[27] T. Norimatsu, K. Kogo, T. Komori, N. Kohmu, F. Yuki, and T. Kawamoto, "A 100-Gbps 4-Lane Transceiver for 47-dB Loss Copper Cable in 28-nm CMOS," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 10, pp. 3433–3443, 2020. DOI: 10.1109/TCSI.2020.2993569 (cit. on p. 7).

[28] G.-S. Jeong, B. Kang, H. Ju, K. Park, and D.-K. Jeong, "A Modulo-FIR Equalizer for Wireline Communications," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 11, pp. 4278–4286, 2019. DOI: 10.1109/TCSI.2019.2923636 (cit. on p. 7).

[29] A. Talebzadeh, P. C. Sochoux, J. Li, Q. Liu, K. Ghosh, and D. Pommerenke, "Shielding Effectiveness, Coupling Path, and EMI Mitigation for QSFP Cages With Heatsink," *IEEE Transactions on Electromagnetic Compatibility*, vol. 60, no. 5, pp. 1254–1262, 2018. DOI: 10.1109/TEMC.2018.2813889 (cit. on p. 7).

[30] C. Domínguez-Palacios, P. González-Vizuete, M. A. Martín-Prats, and J. B. Mendez, "Smart Shielding Techniques for Common Mode Chokes in EMI Filters," *IEEE Transactions on Electromagnetic Compatibility*, vol. 61, no. 4, pp. 1329–1336, 2019. DOI: 10.1109/TEMC.2019.2918863 (cit. on p. 7).

[31] J. Moore, *Gasketed Collar For Reducing Electromagnetic Interference (EMI) Emission From Optical Communication Module*, US Patent 7,928,324, Apr. 2011 (cit. on p. 7).

[32] E. Chikando, E. Bodette, S. Connor, and B. Archambeault, "Vent hole size analysis for high-frequency systems chassis design," in *2010 IEEE International Symposium on Electromagnetic Compatibility*, 2010, pp. 813–818. DOI: 10.1109/ISEMC.2010.5711384 (cit. on p. 7).

[33] M. A. Khorrami, P. Dixon, T. Steigerwald, and H. Chowdhry, "Employment of microwave absorbers for EMI/RFI mitigations from high speed digital buses with signal integrity considerations," in *2016 IEEE International Symposium on Electromagnetic*

Compatibility (EMC), 2016, pp. 1–6. DOI: 10.1109/ISEMC.2016.7571564 (cit. on p. 7).

[34] D. L. J. Y. X. L. H. Y. Y. Huang, *Driver for serialization/deserialization link transmitter*, US Patent WO 2019/001,369,A1 (cit. on p. 7).

[35] B. Koh, K. Yong, W. Song, and A. K. Srivastava, "On-die common mode noise reduction solution for high speed differential IO," in *2017 IEEE International Symposium on Electromagnetic Compatibility & Signal/Power Integrity (EMCSI)*, 2017, pp. 255–260. DOI: 10.1109/ISEMC.2017.8077876 (cit. on p. 7).

[36] K. Q. Maqbool, D. Luo, G. Zhu, X. Luo, H. Yu, and C. P. Yue, "EMI common-mode (CM) noise suppression from self-calibration of high-speed SST driver using on-chip process monitoring circuit," in *2017 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2017, pp. 1–4. DOI: 10.1109/ISCAS.2017.8050879 (cit. on p. 7).

[37] K. Q. Maqbool, D. Luo, G. Zhu, and C. P. Yue, "Common-Mode (CM) noise suppression of serializer/deserializer (SERDES) transmitters based on parallel impedance scaled stages (Invited paper)," in *2017 International Conference on Electron Devices and Solid-State Circuits (EDSSC)*, 2017, pp. 1–2. DOI: 10.1109/EDSSC.2017.8126564 (cit. on p. 7).

[38] *Integrated System Evaluation Engine*, https://github.com/OWL-Integrated-System-Evaluation-Engine. (cit. on p. 10).

[39] V. Vorapipat, C. S. Levy, and P. M. Asbeck, "Voltage Mode Doherty Power Amplifier," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 5, pp. 1295–1304, 2017. DOI: 10.1109/JSSC.2017.2647954 (cit. on pp. 13, 14).

[40] X. Wu, M. Kalantari, D. H. Shin, and C. Patrick Yue, "A 24-32GHz gm-boosted LNA with Triple Coupling Input Transformer for 5G Applications," in *2019 IEEE MTT-S International Wireless Symposium (IWS)*, 2019, pp. 1–3. DOI: 10.1109/IEEE-IWS.2019.8804024 (cit. on p. 15).

[41] P. Andreani and H. Sjoland, "Noise optimization of an inductively degenerated CMOS low noise amplifier," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 48, no. 9, pp. 835–841, 2001. DOI: 10.1109/82.964996 (cit. on p. 16).

[42] 3GPP TS 38.104, "NR base-station (BS) radio transmission and reception (Release 16)," 2018 (cit. on p. 19).

[43] Y. Yi *et al.*, "A 24–29.5-GHz Highly Linear Phased-Array Transceiver Front-End in 65-nm CMOS Supporting 800-MHz 64-QAM and 400-MHz 256-QAM for 5G New Radio," *IEEE Journal of Solid-State Circuits*, vol. 57, no. 9, pp. 2702–2718, 2022. DOI: 10.1109/JSSC.2022.3169588 (cit. on pp. 24, 76).

[44] J. Pang *et al.*, "A 28-GHz CMOS Phased-Array Transceiver Based on LO Phase-Shifting Architecture With Gain Invariant Phase Tuning for 5G New Radio," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 5, pp. 1228–1242, 2019. DOI: 10.1109/JSSC.2019.2899734 (cit. on pp. 24, 28, 76).

[45] K. Kibaroglu, M. Sayginer, and G. M. Rebeiz, "A Low-Cost Scalable 32-Element 28-GHz Phased Array Transceiver for 5G Communication Links Based on a 2 × 2 Beamformer Flip-Chip Unit Cell," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 5, pp. 1260–1274, 2018. DOI: 10.1109/JSSC.2018.2791481 (cit. on pp. 24, 28).

[46] K. Kibaroglu, M. Sayginer, and G. M. Rebeiz, "A Low-Cost Scalable 32-Element 28-GHz Phased Array Transceiver for 5G Communication Links Based on a 2 × 2 Beamformer Flip-Chip Unit Cell," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 5, pp. 1260–1274, 2018. DOI: 10.1109/JSSC.2018.2791481 (cit. on pp. 24, 26).

[47] J. Park, S. Lee, D. Lee, and S. Hong, "9.8 A 28GHz 20.3%-Transmitter-Efficiency 1.5°-Phase-Error Beamforming Front-End IC with Embedded Switches and Dual-Vector Variable-Gain Phase Shifters," in *2019 IEEE International Solid-State Circuits Conference - (ISSCC)*, 2019, pp. 176–178. DOI: 10.1109/ISSCC.2019.8662512 (cit. on pp. 24, 26).

[48] J. Pang *et al.*, "A 28-GHz CMOS Phased-Array Transceiver Based on LO Phase-Shifting Architecture With Gain Invariant Phase Tuning for 5G New Radio," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 5, pp. 1228–1242, 2019. DOI: 10.1109/JSSC.2019.2899734 (cit. on p. 26).

[49] B. Sadhu *et al.*, "A 24-to-30GHz 256-Element Dual-Polarized 5G Phased Array with Fast Beam-Switching Support for >30,000 Beams," in *2022 IEEE International Solid-State Circuits Conference (ISSCC)*, vol. 65, 2022, pp. 436–438. DOI: 10.1109/ISSCC42614.2022.9731778 (cit. on p. 26).

[50] Y. Chang, Y. Wang, C.-N. Chen, Y.-C. Wu, and H. Wang, "A V-Band Power Amplifier With 23.7-dBm Output Power, 22.1% PAE, and 29.7-dB Gain in 65-nm CMOS Technology," *IEEE Transactions on Microwave Theory and Techniques*, vol. 67, no. 11, pp. 4418–4426, 2019. DOI: 10.1109/TMTT.2019.2939527 (cit. on p. 26).

[51] H. Wang, J.-H. Tsai, K.-Y. Lin, Z.-M. Tsai, and T.-W. Huang, "MM-Wave Integration and Combinations," *IEEE Microwave Magazine*, vol. 13, no. 5, pp. 49–57, 2012. DOI: 10.1109/MMM.2012.2197143 (cit. on p. 26).

[52] K. H. An *et al.*, "Power-Combining Transformer Techniques for Fully-Integrated CMOS Power Amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 5, pp. 1064–1075, 2008. DOI: 10.1109/JSSC.2008.920349 (cit. on p. 26).

[53] K. Guo, P. Huang, and K. Kang, "A 60-GHz 1.2 V 21 dBm power amplifier with a fully symmetrical 8-way transformer power combiner in 90 nm CMOS," in *2014 IEEE MTT-S International Microwave Symposium (IMS2014)*, 2014, pp. 1–3. DOI: 10.1109/MWSYM.2014.6848383 (cit. on p. 26).

[54] P. Reynaert and A. M. Niknejad, "Power combining techniques for RF and mm-wave CMOS power amplifiers," in *ESSCIRC 2007 - 33rd European Solid-State Circuits Conference*, 2007, pp. 272–275. DOI: 10.1109/ESSCIRC.2007.4430296 (cit. on p. 26).

[55] W. Zhu *et al.*, "A 1V 32.1 dBm 92-to-102GHz Power Amplifier with a Scalable 128-to-1 Power Combiner Achieving 15% Peak PAE in a 65nm Bulk CMOS Process," in *2022 IEEE International Solid-State Circuits Conference (ISSCC)*, vol. 65, 2022, pp. 318–320. DOI: 10.1109/ISSCC42614.2022.9731700 (cit. on p. 27).

[56] F. Wang and H. Wang, "A High-Power Broadband Multi-Primary DAT-Based Doherty Power Amplifier for mm-Wave 5G Applications," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 6, pp. 1668–1681, 2021. DOI: 10.1109/JSSC.2021.3070800 (cit. on p. 27).

[57] C.-W. Wu, Y.-H. Lin, Y.-H. Hsiao, C.-F. Chou, Y.-C. Wu, and H. Wang, "Design of a 60-GHz High-Output Power Stacked- FET Power Amplifier Using Transformer-Based Voltage-Type Power Combining in 65-nm CMOS," *IEEE Transactions on Microwave Theory and Techniques*, vol. 66, no. 10, pp. 4595–4607, 2018. DOI: 10.1109/TMTT.2018.2859980 (cit. on p. 27).

[58] H.-T. Dabag, B. Hanafi, F. Golcuk, A. Agah, J. F. Buckwalter, and P. M. Asbeck, "Analysis and Design of Stacked-FET Millimeter-Wave Power Amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 4, pp. 1543–1556, 2013. DOI: 10.1109/TMTT.2013.2247698 (cit. on p. 27).

[59] S. Pornpromlikit, J. Jeong, C. D. Presti, A. Scuderi, and P. M. Asbeck, "A Watt-Level Stacked-FET Linear Power Amplifier in Silicon-on-Insulator CMOS," *IEEE Transactions on Microwave Theory and Techniques*, vol. 58, no. 1, pp. 57–64, 2010. DOI: 10.1109/TMTT.2009.2036323 (cit. on p. 27).

[60] I. Aoki, S. Kee, D. Rutledge, and A. Hajimiri, "Distributed active transformer-a new power-combining and impedance-transformation technique," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 1, pp. 316–331, 2002. DOI: 10.1109/22.981284 (cit. on p. 27).

[61] H. T. Nguyen, T. Chi, S. Li, and H. Wang, "A Linear High-Efficiency Millimeter-Wave CMOS Doherty Radiator Leveraging Multi-Feed On-Antenna Active Load Modulation," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 12, pp. 3587–3598, 2018. DOI: 10.1109/JSSC.2018.2880186 (cit. on p. 27).

[62] Y. Chang, B.-Z. Lu, Y. Wang, and H. Wang, "A Ka-Band Stacked Power Amplifier with 24.8-dBm Output Power and 24.3% PAE in 65-nm CMOS Technology," in *2019 IEEE MTT-S International Microwave Symposium (IMS)*, 2019, pp. 316–319. DOI: 10.1109/MWSYM.2019.8700937 (cit. on p. 27).

[63] H.-c. Park *et al.*, "A High Efficiency 39GHz CMOS Cascode Power Amplifier for 5G Applications," in *2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2019, pp. 179–182. DOI: 10.1109/RFIC.2019.8701809 (cit. on p. 27).

[64] T.-W. Li, M.-Y. Huang, and H. Wang, "Millimeter-Wave Continuous-Mode Power Amplifier for 5G MIMO Applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 67, no. 7, pp. 3088–3098, 2019. DOI: 10.1109/TMTT.2019.2906592 (cit. on p. 27).

[65] H. Jin, A. B. Ayed, Z. He, B. Tung, and S. Boumaiza, "Embedded Near-Field Probing Antenna for Enhancing the Performance of 37–41-GHz Linear and Dual-Polarized Phased Antenna Arrays," *IEEE Microwave and Wireless Technology Letters*, vol. 33, no. 6, pp. 911–914, 2023. DOI: 10.1109/LMWT.2023.3268570 (cit. on p. 28).

[66] W. El-Halwagy, A. Nag, P. Hisayasu, F. Aryanfar, P. Mousavi, and M. Hossain, "A 28-GHz Quadrature Fractional-N Frequency Synthesizer for 5G Transceivers With Less Than 100-fs Jitter Based on Cascaded PLL Architecture," *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 2, pp. 396–413, 2017. DOI: 10.1109/TMTT.2016.2647698 (cit. on p. 29).

[67] Y. Hu *et al.*, "A Charge-Sharing Locking Technique With a General Phase Noise Theory of Injection Locking," *IEEE Journal of Solid-State Circuits*, vol. 57, no. 2, pp. 518–534, 2022. DOI: 10.1109/JSSC.2021.3106237 (cit. on p. 29).

[68] W. Wu *et al.*, "A 14-nm Ultra-Low Jitter Fractional-N PLL Using a DTC Range Reduction Technique and a Reconfigurable Dual-Core VCO," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 12, pp. 3756–3767, 2021. DOI: 10.1109/JSSC.2021.3111134 (cit. on p. 29).

[69] H. Sira-Ramírez, "On the sliding mode control of nonlinear systems," *Systems & Control Letters*, vol. 19, no. 4, pp. 303–312, 1992. DOI: https://doi.org/10.1016/0167-6911(92)90069-5 (cit. on p. 29).

[70] X. Guan, H. Hashemi, and A. Hajimiri, "A fully integrated 24-GHz eight-element phased-array receiver in silicon," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 12, pp. 2311–2320, 2004. DOI: 10.1109/JSSC.2004.836339 (cit. on p. 29).

[71] X. Gao, E. A. M. Klumperink, M. Bohsali, and B. Nauta, "A Low Noise Sub-Sampling PLL in Which Divider Noise is Eliminated and PD/CP Noise is Not Multiplied by N^2," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 12, pp. 3253–3263, 2009. DOI: 10.1109/JSSC.2009.2032723 (cit. on p. 29).

[72] X. Gao, E. A. M. Klumperink, M. Bohsali, and B. Nauta, "A 2.2GHz 7.6mW sub-sampling PLL with −126dBc/Hz in-band phase noise and 0.15psrms jitter in 0.18µm CMOS," in *2009 IEEE International Solid-State Circuits Conference - Digest of Technical Papers*, 2009, 392–393, 393a. DOI: 10.1109/ISSCC.2009.4977473 (cit. on p. 29).

[73] L. Bertulessi *et al.*, "A 30-GHz Digital Sub-Sampling Fractional- N PLL With −238.6-dB Jitter-Power Figure of Merit in 65-nm LP CMOS," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 12, pp. 3493–3502, 2019. DOI: 10.1109/JSSC.2019.2940332 (cit. on p. 29).

[74] H. Liu *et al.*, "A 265- μ W Fractional- N Digital PLL With Seamless Automatic Switching Sub-Sampling/Sampling Feedback Path and Duty-Cycled Frequency-Locked Loop in 65-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 12, pp. 3478–3492, 2019. DOI: 10.1109/JSSC.2019.2936967 (cit. on p. 29).

[75] M. Liu, R. Ma, S. Liu, Z. Ding, P. Zhang, and Z. Zhu, "A 5-GHz Low-Power Low-Noise Integer-N Digital Subsampling PLL With SAR ADC PD," *IEEE Transactions on Microwave Theory and Techniques*, vol. 66, no. 9, pp. 4078–4087, 2018. DOI: 10.1109/TMTT.2018.2840987 (cit. on p. 29).

[76] Y. Zhao, M. Forghani, and B. Razavi, "A 20-GHz PLL With 20.9-fs Random Jitter," *IEEE Journal of Solid-State Circuits*, vol. 58, no. 6, pp. 1597–1609, 2023 (cit. on p. 29).

[77] Z. Yang, Y. Chen, S. Yang, P.-I. Mak, and R. P. Martins, "16.8 A 25.4-to-29.5GHz 10.2mW Isolated Sub-Sampling PLL Achieving -252.9dB Jitter-Power FoM and -63dBc Reference Spur," in *2019 IEEE International Solid-State Circuits Conference - (ISSCC)*, 2019, pp. 270–272. DOI: 10.1109/ISSCC.2019.8662364 (cit. on p. 29).

[78] Y. Sun *et al.*, "A 2.74–5.37GHz boosted-gain type-I PLL with <15% loop filter area," in *2012 IEEE Radio Frequency Integrated Circuits Symposium*, 2012, pp. 181–184. DOI: 10.1109/RFIC.2012.6242259 (cit. on p. 31).

[79] A. Sharkia, S. Aniruddhan, S. Mirabbasi, and S. Shekhar, "A Compact, Voltage-Mode Type-I PLL With Gain-Boosted Saturated PFD and Synchronous Peak Tracking Loop Filter," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 1, pp. 43–53, 2019. DOI: 10.1109/TCSI.2018.2858197 (cit. on p. 31).

[80] Z. Yang, Y. Chen, P.-I. Mak, and R. P. Martins, "A Calibration-Free, Reference-Buffer-Free, Type-I Narrow-Pulse-Sampling PLL With −78.7-dBc REF Spur, −128.1-dBc/Hz Absolute In-Band PN and −254-dB FOM," *IEEE Solid-State Circuits Letters*, vol. 3, pp. 494–497, 2020. DOI: 10.1109/LSSC.2020.3031901 (cit. on p. 31).

[81] Y. Huang, Y. Chen, B. Zhao, P.-I. Mak, and R. P. Martins, "A 3.78-GHz Type-I Sampling PLL With a Fully Passive KPD-Doubled Primary–Secondary S-PD Measuring 39.6-fsRMS Jitter, −260.2-dB FOM, and −70.96–dBc Reference Spur," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 70, no. 4, pp. 1463–1475, 2023. DOI: 10.1109/TCSI.2023.3236309 (cit. on p. 31).

[82] A. Sharkia, S. Aniruddhan, S. Shekhar, and S. Mirabbasi, "A high-performance, yet simple to design, digital-friendly type-I PLL," in *2015 IEEE Custom Integrated Circuits Conference (CICC)*, 2015, pp. 1–4. DOI: 10.1109/CICC.2015.7338487 (cit. on p. 31).

[83] S. S. Nagam and P. R. Kinget, "A 0.008mm2 2.4GHz type-I sub-sampling ring-oscillator-based phase-locked loop with a −239.7dB FoM and −64dBc reference spurs," in *2018 IEEE Custom Integrated Circuits Conference (CICC)*, 2018, pp. 1–4. DOI: 10.1109/CICC.2018.8357091 (cit. on p. 31).

[84] M. Ferriss *et al.*, "An Integral Path Self-Calibration Scheme for a Dual-Loop PLL," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 4, pp. 996–1008, 2013. DOI: 10.1109/JSSC.2013.2239114 (cit. on p. 31).

[85] D. Sun *et al.*, "A 3.96-4.84-GHz Dual-Path Charge Pump PLL Achieving 89.7-fsrms Integrated Jitter and −250.8-dB FOMPLL," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 71, no. 4, pp. 1909–1913, 2024. DOI: 10.1109/TCSII.2023.3341143 (cit. on p. 31).

[86] Z. Zhang, G. Zhu, and C. P. Yue, "A 0.25-0.4V, Sub-0.11mW/GHz, 0.15-1.6GHz PLL Using an Offset Dual-Path Loop Architecture with Dynamic Charge Pumps," in *2019 Symposium on VLSI Circuits*, 2019, pp. C158–C159. DOI: 10.23919/VLSIC.2019.8778061 (cit. on p. 31).

[87] Z. Zhang, G. Zhu, and C. Patrick Yue, "A 0.65-V 12–16-GHz Sub-Sampling PLL With 56.4-fsrms Integrated Jitter and −256.4-dB FoM," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 6, pp. 1665–1683, 2020. DOI: 10.1109/JSSC.2020.2967562 (cit. on p. 31).

[88] A. Sharkia, S. Mirabbasi, and S. Shekhar, "A Type-I Sub-Sampling PLL With a 100 × 100 μm^2 Footprint and −255-dB FOM," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 12, pp. 3553–3564, 2018. DOI: 10.1109/JSSC.2018.2874013 (cit. on p. 54).

[89] Z. Deng and A. M. Niknejad, "The Speed–Power Trade-Off in the Design of CMOS True-Single-Phase-Clock Dividers," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 11, pp. 2457–2465, 2010. DOI: 10.1109/JSSC.2010.2074290 (cit. on p. 60).

[90] B. Chang, J. Park, and W. Kim, "A 1.2 GHz CMOS dual-modulus prescaler using new dynamic D-type flip-flops," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 5, pp. 749–752, 1996. DOI: 10.1109/4.509860 (cit. on p. 60).

[91] B. Razavi, "TSPC Logic [A Circuit for All Seasons]," *IEEE Solid-State Circuits Magazine*, vol. 8, no. 4, pp. 10–13, 2016. DOI: 10.1109/MSSC.2016.2603228 (cit. on p. 60).

[92] L. Wang, Z. Liu, and C. P. Yue, "A 24-30 GHz Cascaded QPLL Achieving 56.8-fs RMS Jitter and −248.6-dB FoMjitter," in *2023 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, 2023, pp. 1–2. DOI: 10.23919/VLSITechnologyandCir57934.2023.10185269 (cit. on p. 64).

[93] J. Lim *et al.*, "A K-Band CMOS Power Amplifier using an Analog Predistortion Linearizer with 22.1 dBm Psat and 0.9° AM-PM Distortion," in *2024 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2024, pp. 303–306. DOI: 10.1109/RFIC61187.2024.10600035 (cit. on p. 76).

[94] J. Gu *et al.*, "A 23-30 GHz 4-Path Series-Parallel-Combined Class-AB Power Amplifier with 23 dBm Psat, 38.5% Peak PAE and 1.3° AM-PM Distortion in 40nm Bulk CMOS," in *2023 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2023, pp. 197–200. DOI: 10.1109/RFIC54547.2023.10186197 (cit. on p. 76).

[95] Z. Ma, K. Ma, K. Wang, and F. Meng, "A 28GHz Compact 3-Way Transformer-Based Parallel-Series Doherty Power Amplifier With 20.4%/14.2% PAE at 6-/12-dB Power Back-off and 25.5dBm PSAT in 55nm Bulk CMOS," in *2022 IEEE International Solid-State Circuits Conference (ISSCC)*, vol. 65, 2022, pp. 320–322. DOI: 10.1109/ISSCC42614.2022.9731564 (cit. on p. 76).

[96] J. Park, S. Kang, and S. Hong, "Design of a Ka-Band Cascode Power Amplifier Linearized With Cold-FET Interstage Matching Network," *IEEE Transactions on Microwave Theory and Techniques*, vol. 69, no. 2, pp. 1429–1438, 2021. DOI: 10.1109/TMTT.2020.3040385 (cit. on p. 76).

[97] H. Oh *et al.*, "32.2 A 24.25-to-29.5GHz Extremely Compact Doherty Power Amplifier with Differential-Breaking Phase Offset Achieving 23.7% PAEavg for 5G Base-Station Transceivers," in *2024 IEEE International Solid-State Circuits Conference (ISSCC)*, vol. 67, 2024, pp. 522–524. DOI: 10.1109/ISSCC49657.2024.10454406 (cit. on p. 76).

[98] S. Li, M.-Y. Huang, D. Jung, T.-Y. Huang, and H. Wang, "A MM-Wave Current-Mode Inverse Outphasing Transmitter Front-End: A Circuit Duality of Conventional Voltage-Mode Outphasing," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 6, pp. 1732–1744, 2021. DOI: 10.1109/JSSC.2020.3038882 (cit. on p. 76).

[99] Y.-C. Huang, C.-H. Cheng, and T.-L. Wu, "A Synthesized Method for Common-Mode Noise Suppression Filters With Specified Common-Mode and Differential Mode Response," *IEEE Transactions on Electromagnetic Compatibility*, vol. 61, no. 3, pp. 893–902, 2019. DOI: 10.1109/TEMC.2018.2839264 (cit. on p. 85).

[100] R. Azmat, L. Wang, K. Q. Maqbool, C. Wang, and C. P. Yue, "Sensing and Cancellation Circuits for Mitigating EMI-Related Common Mode Noise in High-Speed PAM-4 Transmitter," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 68, no. 11, pp. 4545–4555, 2021. DOI: 10.1109/TCSI.2021.3108640 (cit. on pp. 86, 89).

[101] A. B. Williams and F. J. Taylor, *Electronic Filter Design Handbook, 4th Edition*. The McGraw-Hill Companies, Inc, 2006 (cit. on pp. 87, 88).

APPENDIX A

LIST OF PUBLICATIONS

Journal Publications

[1] Z. Liu, L. Wang, R. Ma, Z. Chen, and C. P. Yue, "A Compact 28-GHz Transmitter Front-End with Co-Optimized Wideband Chip-Antenna Interface for Next-Generation Phased Array Systems," *IEEE Transactions on Microwave Theory and Techniques*, (Under Review).

[2] L. Wang, Z. Liu, R. Ma, and C. P. Yue, "A Compact 20-24 GHz Sub-Sampling PLL with Charge-Domain Bandwidth Control Scheme," *IEEE Journal of Solid-State Circuits*, (Early Accepted).

Conference Publications

[1] Z. Liu, L. Wang, H. Fallah, Z. Chen, and C. P. Yue, "A Compact 28-GHz Transmitter Front-End with Co-Optimized Wideband Chip-Antenna Interface Achieving 18.5-dBm P1dB and 1.0-W/mm2 Power Density for Phased Array Systems," in *2024 IEEE/MTT-S International Microwave Symposium - IMS 2024*, 2024, pp. 239–242. DOI: 10.1109/IMS40175.2024.10600209.

[2] Z. Liu, L. Wang, H. Fallah, and C. P. Yue, "Design of Chip-to-PCB Matching Network for Millimeter-Wave On-Chip Transmitter and On-PCB Antenna," in *2023 IEEE 15th International Conference on ASIC (ASICON)*, 2023, pp. 1–4. DOI: 10.1109/ASICON58565.2023.10396322.

[3] Z. Liu, R. Azmat, X. Liu, L. Wang, and C. P. Yue, "On-Chip Filter for Mitigating EMI-Related Common-Mode Noise in High-Speed PAM-4 Transmitter," in *2021 IEEE 14th International Conference on ASIC (ASICON)*, 2021, pp. 1–4. DOI: 10.1109/ASICON52560.2021.9620447.

[4] L. Wang, Z. Liu, H. Fallah, R. Ma, Z. Chen, and C. P. Yue, "A 28-GHz Phased-Array Transmitter Achieving 24% Peak Efficiency, 0.26-mm2/ Element Area Efficiency with Completely Orthogonal Phase and Gain Control," in *2024 IEEE European Solid-State Electronics Research Conference (ESSERC)*, 2024, pp. 496–499. DOI: 10.1109/ESSERC62670.2024.10719557.

[5] L. Wang, Z. Liu, R. Ma, and C. P. Yue, "A 20-24-GHz DPSSPLL with Charge-Domain Bandwidth Optimization Scheme Achieving 61.3-fs RMS Jitter and -253-dB FoMJitter," in *2024 IEEE Custom Integrated Circuits Conference (CICC)*, 2024, pp. 1–2. DOI: 10.1109/CICC60959.2024.10529091.

[6] L. Wang, Z. Liu, and C. P. Yue, "A 24-30 GHz Cascaded QPLL Achieving 56.8-fs RMS Jitter and −248.6-dB FoMjitter," in *2023 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, 2023, pp. 1–2. DOI: 10.23919/VLSITechnologyandCir57934.2023.10185269.

[7] W. Shi *et al.*, "An Integrated System Evaluation Engine for Cross-Domain Simulation and Design Optimization of High-Speed 5G Millimeter-Wave Wireless SoCs," in *2021 IEEE 14th International Conference on ASIC (ASICON)*, 2021, pp. 1–4. DOI: 10.1109/ASICON52560.2021.9620456.

[8] C. Zhang, L. Wang, Z. Liu, Z. Chen, Q. Pan, X. Li, and C. P. Yue, "A 48-Gb/s Half-Rate PAM4 Optical Receiver with 0.27-pJ/bit TIA Efficiency, 1.28-pJ/bit RX Efficiency, and 0.06-mm2 area in 28-nm CMOS," in *2024 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, 2024, pp. 1–2. DOI: 10.1109/VLSITechnologyandCir46783.2024.10631502.