Energy-Efficient CMOS Fiber-Wireless Communication System-on-a-Chip

by

Yipeng WANG

A Thesis Submitted to

The Hong Kong University of Science and Technology

in Partial Fulfillment of the Requirements for

the Degree of Doctor of Philosophy

in the Department of Electronic and Computer Engineering

September 2016, Hong Kong

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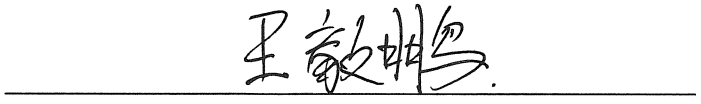

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This is to certify that I have examined the above PhD thesis
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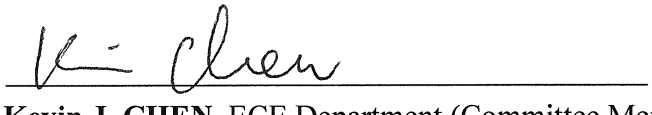

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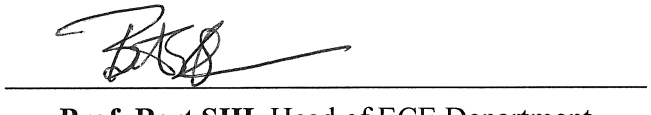

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To my parents

Abstract

The growing deployment of bandwidth-intensive multimedia applications and cloud computing continue to escalate the burden on today's mobile communication network. Meanwhile, the demand for high-performance data traffic has gradually migrated from centralized telecommunication infrastructures to cost-sensitive mobile applications and consumer electronics. Therefore, the need for cost reduction of peripheral devices in mobile networks are accelerating, as the number of such devices increases to maintain network coverage with shrinking mobile network cell size and higher user data throughput. A hybrid fiber-wireless network is a promising approach to provide a flexible and high performance solution for short-range (< 1 km) backhaul links deployment in high data traffic areas. Such systems will require the integration of optical and wireless communication transceiver circuits. To address this emerging trend, this thesis presents the design and implementation of optical-to-millimeter-wave (mmW) modulator system-on-a-chip (SoC) using mainstream CMOS technology for supporting low-cost deployment of such network.

In this thesis, an optical-to-mmW modulator SoC with a fully integrated 850-nm wavelength optical receiver front-end and a 60-GHz QPSK modulator is presented for the first time. As the first block in an optical receiver chain, the transimpedance amplifier (TIA) dictates the overall system noise and gain-bandwidth performance. An inverter-based TIA with a multiple-peaking network is proposed to address design challenges of conventional CMOS TIAs. The peaking network effective extends the TIA bandwidth by 2.8 times. A power efficiency of 0.12 pJ/bit is achieved by the optimized inverter based core amplifier. Realized in 65-nm CMOS, the overall optical receiver front-end achieves −3-dBm input sensitivity at 4 Gb/s with 10^{-12} BER. The quadrature modulator directly up-converts the de-multiplexed 2-Gb/s I&Q NRZ data to a 4-Gb/s QPSK signal at 60-GHz in the unlicensed mmW band. Our design demonstrates that a small

form factor and low-cost optical-to-mmW modulator can be realized in mainstream CMOS technology to support cost-effective implementation of fiber-wireless networks. In the optical receiver, a clock and data recovery (CDR) unit is required following the TIA front-end for generating a phase-aligned clock to de-serialize the high-speed incoming data for baseband processing. A power-efficient CDR with embedded equalization to achieve error free operation ($BER < 10^{-12}$) up to 26 Gb/s under 13-dB channel loss at Nyquist frequency has been developed. The proposed CDR could be further integrated with the fiber-wireless modulator to realize a complete fiber-wireless SoC.

The design, implementation and characterization results of prototypes are presented in this thesis along with the proposed direction of future work.

Acknowledgement

The first person I would like to thank is my supervisor Prof. Patrick Yue for giving me the opportunity of exploring high-speed IC design. His vision of technology inspired me a distinctive research area in my PhD study. His in-depth experience with startups and semiconductor industry equipped me with an exclusive mindset for my future career. His strong physique and endless energy motived me to train hard in the gym and work even harder in the office.

Besides my supervisor, I would like to thank the rest of my thesis committee: Prof. Wing-Hung Ki, Prof. Kevin J. Chen, Prof. Lilong Cai and Prof. Shiheng Wang for reviewing my thesis and giving me valuable comments to widen the scope of my research from various perspectives. I also like to thank Prof. Quan Xue for serving as the external committee member and giving me insightful guidance.

I would like to thank my mentor at UCSB Prof. Steve Long for his guidance and encouragement on both technical and personal developments. Prof. Long introduced me to high-frequency circuit design with unlimited patience and encouraged me to explore further in this area. I am deeply indebted to him for his kindness and help.

It has been my honor and pleasure working with many brilliant and dedicated researchers and staffs at HKUST. This thesis was built upon the work done by many Yue group members. I would like to thank Dr. Li Sun, Dr. Quan Pan, Dr. Yan Lu, Zhengxiong Hou, Duona Luo, Liwen Jing, Zhixin Li and Guang Zhu for all their hard work in multiple tape-outs. I also like to thank Prof. Andrew Poon and Dr. Yu Li for generously lending the BERT equipment. Also, Yue group members: Dr. Liang Wu, Fengyu Che, Xianbo Li, Babar Hussain, Haikun Jia, Liusheng Sun, Clarissa Prawoto, Salahuddin Raju, Qasim Maqbool and Xiao Wang for all the inspiring discussions and enjoyable time I had in the last four years. I am also grateful for the friendship with

other IC research groups at HKUST, especially: Dr. Yue Chao, Alvin Li and Zhiqiang Huang of Wireless Communications Integrated Circuits Lab (Analog Research Lab); Dr. Jing Guo of MIXIC Lab; Dr. Cheng Huang, Fan Yang of Integrated Power Electronics Lab and Lexi Ren of Prof. Jonny Sin's group. Thanks must also be given to all conscientious technicians and staffs at HKUST, in particular: S.F. Luk for die cutting and bonding in every project; K.W. Chan and Fred Kwok for their assistance with high frequency measurement and equipment purchase; Kenny Pang for computing server maintenance; Foner Chan for accounting assistance.

I would also like to take this opportunity to thank my friends who accompany me all the way: Songhua Chen, Zhimin Ye, Shao Huang, Naping Zheng, A-xuan Wu, Yi Huang, Dr. Wen Chen, Dr. Yang Li, Dr. Ming Li, Huiying Zhu, Xiaoyu Tan and Miao He. This adventure would be much lonelier and tougher without your support.

Last but not least, I would like to thank my parents, Jinlian Wang and Libin Qiu, for their unconditional support and endless love. Without them, I would not have the freedom and luxury to discover and pursuit my way of life.

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List of Abbreviations

BER	Bit error rate
BERT	Bit error rate tester
BS	Base station
BoF	Baseband-over-Fiber
BW	Bandwidth
BWER	Bandwidth enhancement ratio
CDR	Clock and data recovery
CO	Central office
CML	Common-mode logic
CTLE	Continuous-time linear equalizer
CH	Cherry-Hooper
CS	Common source
DCVSL	Differential cascade voltage switching logic
DFE	Decision feedback equalizer
DLL	Delay locked loop
EQ	Equalizer
EVM	Error vector magnitude
FB	Feedback
FFE	Feed forward equalizer
GbE	Gigabit Ethernet
GBW	Gain bandwidth
GDV	Group delay variation
LDO	Low dropout regulator
mmW	Millimeter wave
NRZ	Non-return-to-zero
NIC	Negative impedance compensation
OEIC	Optoelectronic integrated circuits
O/E	Optical
PLL	Phase locked loop
PI	Phase interpolator
PD	Photodetector
PRBS	Pseudorandom binary sequence
QPSK	Quadrature Phase Shift Keying
RGC	Regulated cascode
RoF	RF-over-Fiber
RZ	Return-to-zero
SoC	System-on-a-chip
SNR	Signal to noise ratio
S/H	Sample and hold
ILFD	Injection-locked frequency divider
ISI	Inter symbol interference
IRN	Input referred noise

Chapter 1 Introduction

1.1 Research Background

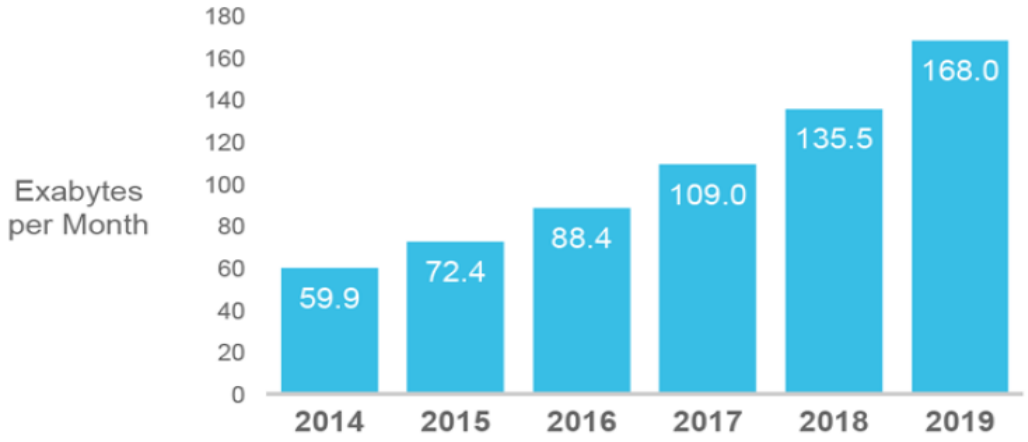


Fig. 1.1 Global IP traffic estimation by Cisco, 2014–2019 [1].

The widespread popularity of mobile internet, multi-media streaming and cloud computing has rapidly increased the requirements for high-speed data communication. According to the Cisco Visual Networking Index Forecast [1], the global data traffic is projected to enter zettabyte (10^{21} byte) era in 2016. As shown in Fig 1.1, the monthly global traffic is projected to reach 168 exabytes (10^{18} byte) in 2019 at an annual growth rate of 23%. This surge demand on data transmission puts considerable pressure on both wired and wireless communication networks.

For wireline communication systems like metropolitan area network and high-speed local area network, 100 Gigabit Ethernet (GbE) systems are widely deployed and are migrating from 10 lanes of 10 Gb/s to 4 lanes of 25 Gb/s to increase the network I/O density and power efficiency. In addition to wireline links, wireless communication networks play an equally important role in the modern life as the traffic from mobile devices is predicted to exceed the traffic from wired devices by 2016 [1]. Therefore, researchers are exploring new network architectures to meet the consistent growth of data traffic.

A. Optical Communication System

The physical transmission media of the 100GbE systems includes cooper cables and optical fibers. Cooper cables like twisted pair and twinax are usually adopted in low-cost short reach applications like rack-to-rack interconnection in data center. The performance of cooper cable is significantly constrained by its high propagation loss. Thus, sophisticated equalization techniques are usually required to achieve high data rate. On the other hand, for applications requiring a bandwidth-distance product larger than 10^4 Gb/s·km, optical fibers are almost mandatory due to its low loss property.

Traditionally, optical transceivers are implemented in expensive III-V technologies [2], [3] to achieve superior performance for high-end applications like long-haul links. In this case, the infrastructure cost is shared by a large number of end-users. However, the emerging high-speed LAN market is much more sensitive to the system cost as the demand for the high-performance data traffic has gradually migrated from telecom infrastructures to cost-sensitive enterprise applications and consumer electronics. In the meanwhile, the system form factor and power dissipation are also strictly regulated in order to fit into existing mechanical packages like SFP and CFP2. Therefore, developing a cost-effective, low power optical I/O solution is critical for next generation high-speed wireline communication network.

To achieve above mentioned criteria, optical transceivers implemented in the standard CMOS technology draw great attention in recent years. Compared to traditional optical communication systems realized in the III-V technologies, CMOS monolithic optoelectronic integrated circuits (OEICs) ensure low-cost, small system form factor and high volume manufacturing capacity. However, the performance of OEICs is usually inferior. For example, the receiver sensitivity and achievable data rate are severely constrained by the responsivity and bandwidth of the on-chip

photodetector, insufficient device transit frequency and large noise. Therefore, advancements on both circuit level and device level are required to further push the performance of OEICs.

B. Wireless Communication System

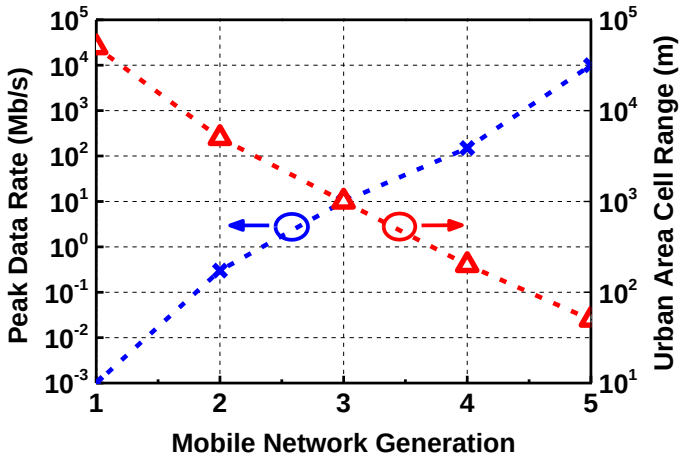


Fig. 1.2 Evolution of mobile networks.

In addition to the advancement in wireline networks, the urgent demand for the multi-gigabit wireless communication and the exhausted spectrum resource draw great attention to the next generation mobile network. Fig. 1.2 shows the evolution of the mobile network peak data rate and cell coverage range. The peak data rate rises rapidly from 300 kb/s in 2G to the proposed 10 Gb/s in 5G. To realize this exponential growth in data rate, the cell coverage range shrinks significantly from 5 km in 2G to the projected 50 m (Femtocell [4], [5]) in 5G for improving link SNR, latency, spectrum efficiency and network capacity. However, forwarding the wireless data traffic to the backhaul network is challenging when such an ultra-dense network is deployed.

Recent researches have demonstrated that the 60-GHz band could be used to accomplish mmW backhaul links [6], [7] to resolve the great challenge of forwarding wireless traffic to core networks in the 5G network. The widely available bandwidth, low latency and directional propagation property make 60-GHz band a suitable candidate for the multi-gigabit wireless

backhaul link. The high oxygen absorption characteristic can also be utilized to construct high density network without significant interference issue between cells.

C. Fiber-Wireless Communication System

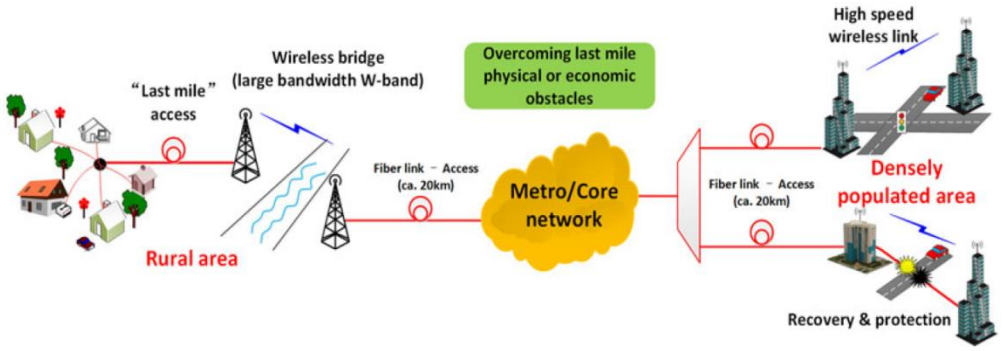


Fig. 1.3 Hybrid fiber-wireless network [4].

Over the last decade, much research has been conducted on the hybrid fiber-wireless network [7]-[9] to explore the alternative backhaul network architecture for the next generation ultra-dense mobile network. Conventionally, the use of optical backhaul link is necessary to reach the demanded data throughput between BS and pico-cells. However, wired connection between BS and pico-cells is sometimes physically impractical or costly in rural or densely populated areas as shown in Fig. 1.3. In these cases, a hybrid fiber-wireless network is desirable to provide a flexible and high performance solution for short-range backhaul links deployment.

The physical implementation of a fiber-wireless network varies considerably as shown in Fig. 1.4. For example, the RF-over-Fiber (RoF) scheme directly transmits modulated RF signal through optical links. In this architecture, the RF modulation is conducted at the central office (CO). The remote BS and pico-cells only perform optical-to-electrical (O/E) conversion and RF transmission. Even though the overhead of RF modulations is eliminated at remote cells, the RoF scheme requires high-speed high-linearity optical links, resulting in costly and bulky system. In contrast, an alternative solution is called Baseband-over-Fiber (BoF). The BoF scheme transmits

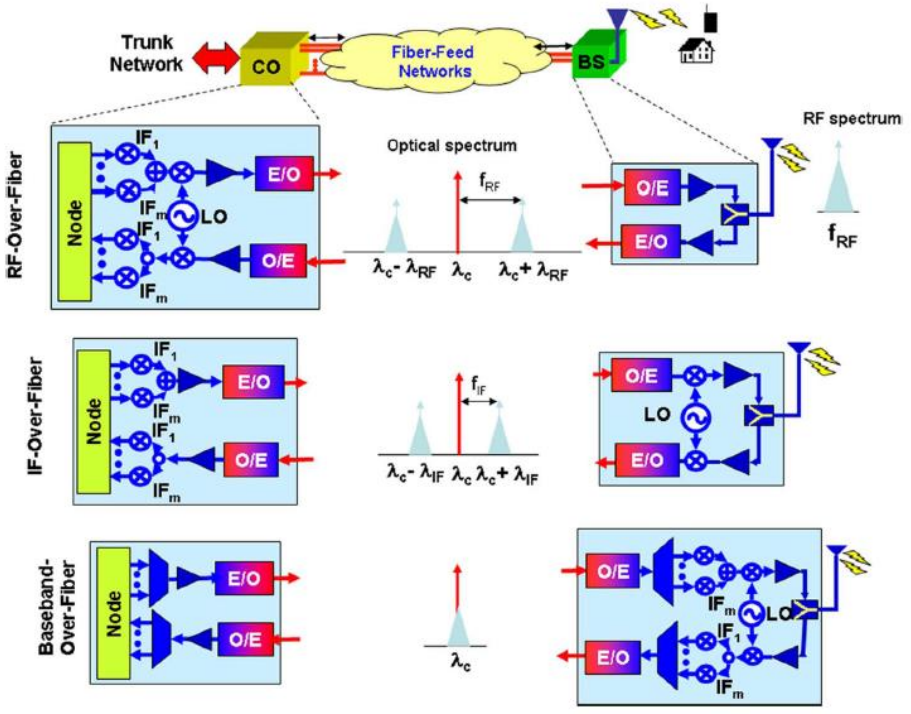


Fig. 1.4 Fiber-wireless network architectures [5].

the baseband signal between CO and BS in the optical domain and up-converts the signal to the mmW band for wireless transmission between cells. Compared to the RoF scheme, the BoF system eliminates the need for high performance optical links since only the baseband signal is transmitted in the optical domain. However, energy efficient and cost effective O/E conversion and RF transmission systems at remote cells are necessary for the BoF network to outperform the RoF network. Therefore, an integrated module capable of directly converting signals between the optical and the mmW domain is needed to reduce the overhead in system size and cost for supporting fiber-wireless backhaul links.

1.2 Thesis Organization

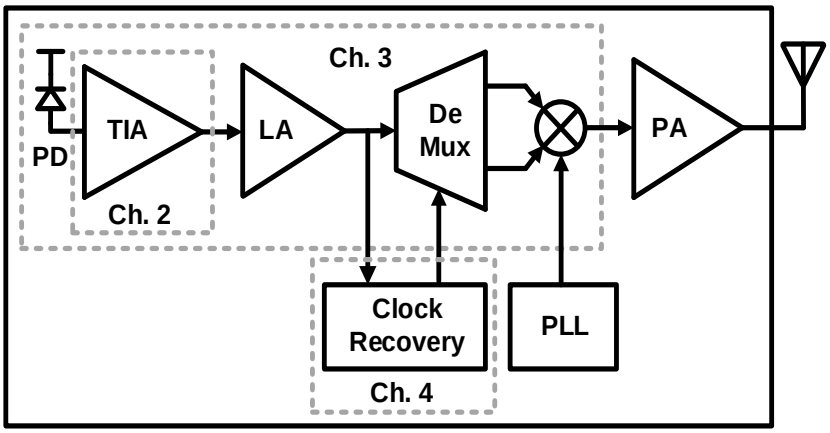


Fig. 1.5 Fiber-wireless modulator architectures.

The remainder of this thesis focuses on the design and implementation of sub-systems of a fiber-wireless modulator as shown in Fig. 1.5. Chapter 2 presents a power efficient CMOS transimpedance amplifier as the foundation of a CMOS optical receiver design. Chapter 3 focuses on a fully integrated optical-to-wireless modulator to demonstrate the feasibility of a low-cost fiber-wireless hybrid system. Chapter 4 extends the research scope to the clock and data recovery circuit which is essential for a complete fiber-wireless communication system. Finally, Chapter 5 concludes the thesis and propose directions for the future work.

A summary of target applications for TIAs presented in Chapter 2 and 3 is shown in Table I. The TIA in Chapter 2 is targeted at high-speed long reach applications like 100 Gigabit Ethernet (GbE). Therefore, it is optimized for high gain-bandwidth product and sensitivity. On the other hand, the TIA presented in Chapter 3 is part of the optical frontend in a short-reach BoF link. To achieve a compact and low-cost fully integrated BoF modulator design, this TIA is optimized for low power consumption and small chip area.

Table I Summary of TIA Target Applications

	TIA in Ch. 2	**TIA in Ch. 3**
Application	100GbE	Short reach BoF link
Data Rate (Gb/s)	25	4
Max. Distance (km)	10	0.2
Optical Wavelength (nm)	1550	850
Fiber	SMF	MMF
Target Sensitivity (dBm)	-10	-5

Chapter 2 CMOS Transimpedance Amplifier

2.1 Introduction

A transimpedance amplifier (TIA) converts an input current to an output voltage. Compared to a voltage-mode amplifier, a TIA exhibits a low input impedance to overcome the bandwidth limitation due to the large parasitic capacitance of the photodetector (PD). Meanwhile, the transimpedance gain (Z_{TIA}) for converting the input PD current to the voltage needs to be large to suppress the input-referred noise contributed by subsequent stages in the receiver. Furthermore, a TIA should be designed with a bandwidth that is just sufficiently large to eliminate the inter-symbol-interference (ISI) while avoiding excessive in-band integrated noise.

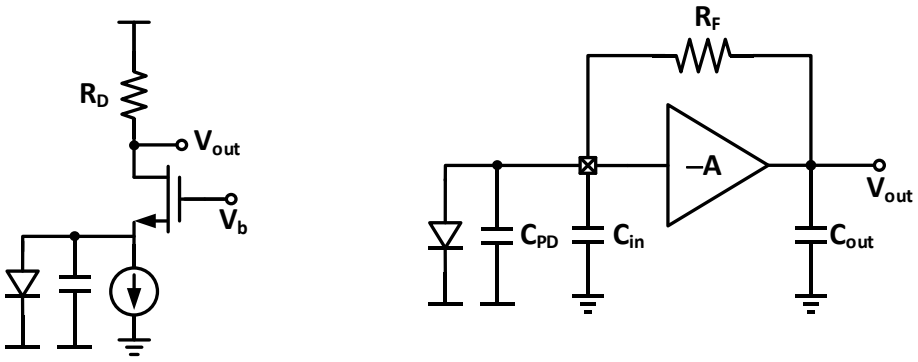
In general, TIAs can be categorized as open-loop or closed-loop architecture. The open-loop TIAs extend bandwidth by inserting a common gate transistor to provide a low input impedance and isolation between the photodetector capacitance (C_{PD}) and the transimpedance resistor. Despite its simplicity and robustness, the conventional open-loop topology suffers from a difficult trade-off between the Z_{TIA} and output voltage headroom. Even though the regulated cascode (RGC) technique [10] can be employed to alleviate such shortcomings, the added devices in the local feedback loop introduce additional noise and hence degrade input sensitivity. Moreover, in scaled CMOS technologies, the single-stage common source (CS) amplifier employed in the RGC local feedback loop can only provide moderate gain and hence making RGC design less effective. In contrast, the closed-loop TIAs utilize shunt-shunt feedback to reduce their input impedance [11]-[13]. Since the feedback resistor does not carry any bias current, the trade-off between the Z_{TIA} and output headroom is greatly relaxed. In particular, closed-loop TIAs utilizing negative impedance compensation (NIC) [11] and active feedback [12] have been reported to extend the gain-bandwidth product (GBW). However, the bandwidth boosting effect of NIC diminishes at

frequencies beyond 10 GHz while the active feedback technique suffers from excess power consumption and stability issue. Although equalization techniques [14]-[15] have been demonstrated to extend the TIA bandwidth, power penalty and ripples in the frequency response of multi-stage equalizers can be severe. Therefore, bandwidth enhancement techniques are still of great value for broadband low-power TIA design.

This section presents a low-power, broadband, inverter-based TIA design for 100GbE applications. employing input series peaking and shunt-shunt inductive feedback to boost the bandwidth by 2.8 times to 24 GHz in 65-nm CMOS process.

2.2 CMOS TIA Design Challenges

2.2.1 Supply Voltage Constrain



$$Z_{TIA} \approx R_D \qquad Z_{TIA} = \frac{A}{1+A} \cdot R_F \approx R_F$$

$$Z_{in} \approx \frac{1}{g_m} \propto \frac{1}{I_D} \qquad Z_{in} \approx R_F/A$$

(a) (b)

Fig. 2.1 Schematic of (a) open-loop CG TIA and (b) closed-loop feedback TIA.

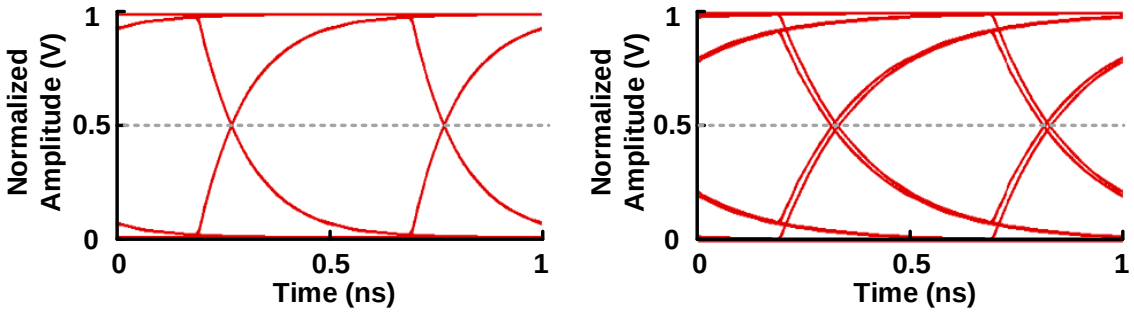
CMOS TIAs designed in advanced technologies suffer from the ever decreasing supply voltage since the transistor threshold voltage does not reduce proportionally with the supply voltage. The limited headroom significantly constrains the achievable transimpedance gain and input impedance.

Therefore, the choice of TIA architecture under various process nodes and power supply voltages could be quite different.

Fig. 2.1 shows the schematic of open-loop and closed-loop TIAs. For the open-loop architecture, the transimpedance gain (Z_{TIA}) is approximately equal to R_D at low frequencies. However, the input impedance of the open-loop TIA is inversely proportional to the common-gate device transconductance so as the bias current I_D. Therefore, a direct trade-off between Z_{TIA} and Z_{in} is observed if the supply voltage is low.

In contrast, the closed-loop TIA shown in Fig. 2.1(b) utilizes the shunt-shunt feedback to reduce the input impedance. Since the feedback resistor (R_F) does not carry any bias current, the trade-off between the Z_{TIA} and the output headroom is greatly relaxed. However, the insufficient open-loop gain of the core amplifier in advanced technology nodes limits the effectiveness of the feedback on bandwidth extension.

2.2.2 Bandwidth Requirement



(a) (b)

Fig. 2.2 Output eye diagram of a PRBS sequence after (a) $0.7/T_b$ bandwidth low-pass filter and (b) $0.4/T_b$ bandwidth low-pass filter.

The finite bandwidth of TIAs limits the maximum transition speed of the input data and degrades the time margin of the system. In time domain, the insufficient bandwidth causes a spreading of the data pulse beyond its time interval. This spreading leads to an unwanted interference between each incoming bit, which is called inter symbol interference (ISI).

A simple RC low-pass filter can be used to model the effect of ISI in the first order. The amplitude distortion of a RC network with PRBS data input is given by

$$V_o - V_{out}(T_b) = V_o e^{-T_b/\tau}, \tag{2-1}$$

where V_o is the input amplitude and V_{out} is the output amplitude after one bit period, T_b is the input data bit period and τ is the filter's RC time constant. If the filter bandwidth is chosen as $f_{-3dB} = 0.7/T_b$, the total eye closure introduced by the low pass filter is only 2.5% as shown in Fig. 2.2(a). On the other hand, the eye closure introduced by the low pass filter would be about 30% when $f_{-3dB} = 0.4/T_b$ as shown in Fig. 2.2(b).

The timing jitter introduced by the finite bandwidth can also be analyzed by the RC filter in the first order under two boundary conditions of the input data sequence. The first boundary condition is an input data sequence consists of a logic one preceded by a long consecutive sequence of logic zero. In this case, the threshold crossing time instant T_1 is

$$T_1 = \tau ln2. \tag{2-2}$$

The other boundary condition is an input data sequence consists of a logic zero in between two long consecutive sequences of logic one. Due to the insufficient bandwidth, the circuit is not capable of responding to the sudden change. Thus, the RC filter output does not have enough time to settle to the stable logic level but rise again after 1UI. This slow response makes the threshold crossing time instant T_2 happens much earlier than the T_1 in the first case and leads to timing jitter. The T_2 is expressed as

$$T_2 = \tau ln2 \left[2\left(1 - e^{-\frac{T_b}{\tau}}\right)\right]. \tag{2-3}$$

The difference between T_1 and T_2 can be considered as the peak-to-peak jitter at the crossing point.

In practice, the targeted TIA bandwidth is a trade-off between power consumption, chip area, ISI as well as total in-band integrated noise. Since practical TIA structures inevitably contain

multiple poles and experience PVT variations, a bandwidth around $0.7/T_b$ is usually chosen as the design starting point. The actual optimal bandwidth should be determined by careful time-domain simulations.

In addition to the limited bandwidth, the phase linearity of TIA frequency response also plays an important role in reducing ISI. Poor phase linearity results in distortions in the form of data dependent jitter[16]-[18]. The phase linearity is characterized as group delay given by

$$\tau = -\frac{d\emptyset(\omega)}{d\omega}. \tag{2-4}$$

In generally, the maximum group delay variation is controlled to be less than 10% of the bit period over the specified bandwidth to void introducing excessive jitter.

2.2.3 Noise and Sensitivity

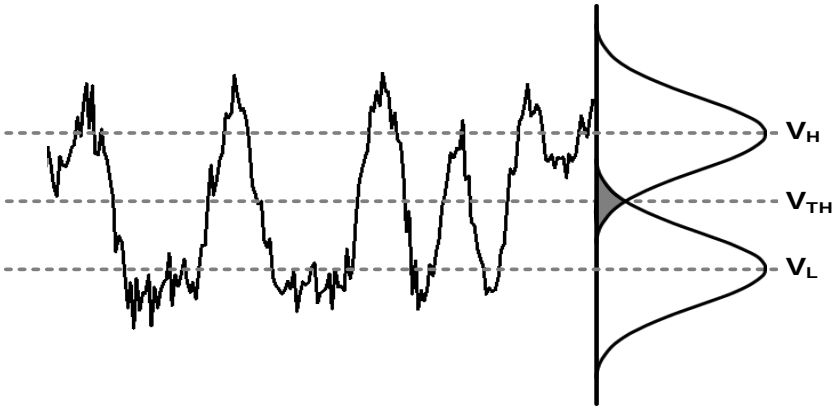


Fig. 2.3 Noisy PRBS data sequence and its amplitude PDF curves.

The noise of a TIA usually determines the achievable input sensitivity of an optical receiver since it is not degenerated by any preceding stage. The noise performance of a TIA can be quantified by its input referred noise current $I_{n,in}$ by dividing the rms output noise voltage by the squared TIA midband transimpedance gain. The influence of noise on the NRZ data can be modeled as shown in Fig. 2.3 assuming the additive noise exhibits a Gaussian distribution. Thus, a bit error occurs when the logic high or low level erroneously crosses the decision threshold (V_{TH}).

The overlapped region of the amplitude distribution PDF curves shown in Fig. 2.3 indicates the error probability. The probability of bit error can be estimated from the SNR at the TIA input node (ratio of input signal current and input referred noise current) and derived from the "Q function"[18]:

$$Q(x) = \int_{x}^{\infty} \frac{1}{\sqrt{2\pi}} exp \frac{-u^2}{2} du, \tag{2-5}$$

$$P_{tot} = Q(\frac{I_{pp}}{2I_{n,in}}) \tag{2-6}$$

where P_{tot} is the error probability, I_{pp} is the signal peak-to-peak amplitude and $I_{n,in}$ is the rms input referred noise current. Fig. 2.4 shows the calculated curve of P_{tot} versus SNR. To achieve a BER < 10^{-12}, a SNR > 7 is generally required.

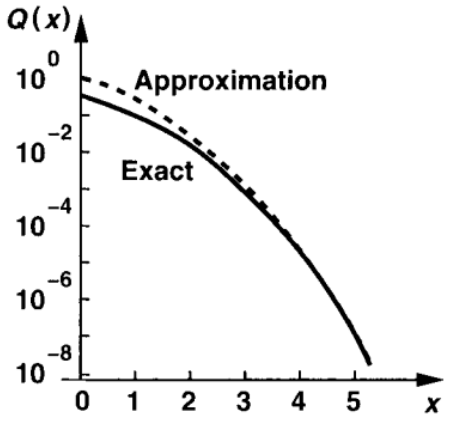


Fig. 2.4 Calculated BER versus SNR [18].

2.3 Proposed Multiple Peaking TIA

A closed-loop feedback TIA design based on an optimized inverter core amplifier and a multiple inductive peaking scheme [19] is proposed in this work. The multiple peaking scheme negates the capacitive loading of the PD input bond pad and the inverter amplifier to achieve bandwidth enhancement ration of 2.8. Moreover, an on-chip LDO with full-spectrum PSR [20] is employed to improve the TIA sensitivity by minimizing supply noise at the point-of-load and to alleviate parasitic effect due to power supply bond-wire inductance.

2.3.1 Inverter Based Core Amplifier Optimization

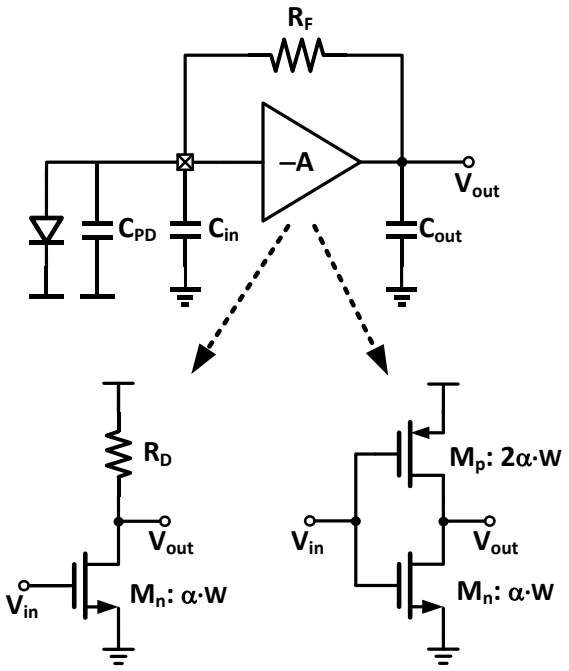


Fig. 2.5 Schematic of a feedback TIA with inverter or common-source amplifier as the core amplifier.

Table II Comparison of Inverter and Common Source Amplifier

	Low Frequency Gain	Unity Gain Bandwidth
Inv. Amp.	$2g_m \cdot (r_{on} \,//\, r_{op})$	$2g_m/(2\pi \cdot 3C_X)$
CS Amp.	$g_m \cdot R_D$	$g_m/(2\pi \cdot C_X)$

The open-loop gain of the TIA core amplifier strongly affects the effectiveness of the feedback on bandwidth extension. Therefore, it is critical to optimize the core amplifier especially under low supply voltage. Fig. 2.5 shows the schematic of a feedback TIA adopting two typical core amplifier topologies, namely, a common source (CS) amplifier and an inverter-based amplifier. To compare their properties and performance, both core amplifiers are biased under the same current and hence equal power consumption. The PMOS transistors are sized to provide the same transconductance (g_m) as NMOS transistors ($W_p = 2W_n$ in this case). A summary of the first-order gain and bandwidth expression for two core amplifiers is listed in Table I, where r_{on} and r_{op} are the output resistance of NMOS and PMOS transistors and C_X is the equivalent parasitic capacitance for each unit size transistor, respectively. Since the loading resistor R_D in the CS amplifier is usually limited to few hundred ohms when M_n is biased with high current for large g_m and f_t, the intrinsic output impedance of the inverter amplifier ($r_{on} // r_{op}$) is larger than the R_D. Thus, the CS amplifier has an inferior low-frequency gain compared to the inverter amplifier counterpart, as shown in Fig. 2.6(a). However, the extra capacitance loading from the PMOS transistor in the inverter amplifier limits its –3-dB bandwidth to be 4 times lower compared to the CS amplifier.

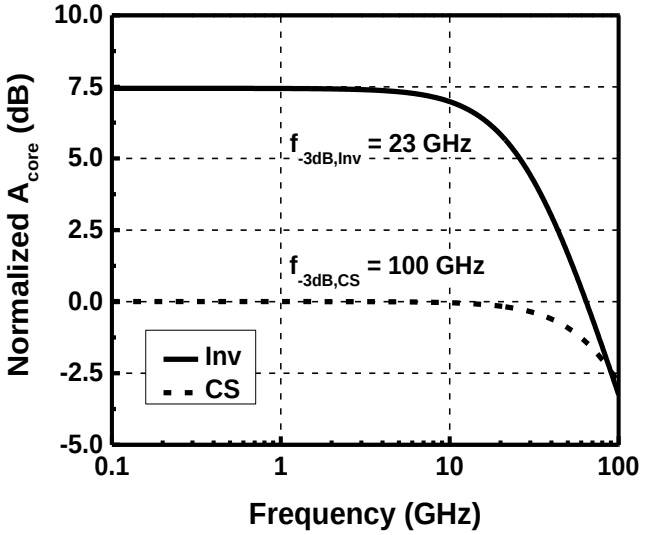
In order to analyze and quantify the trade-off between two core amplifiers, two feedback TIAs are designed based on them. The feedback TIA transimpedance gain is expressed as

$$Z_{TIA}(s) = R_F \cdot \frac{A_{core}(s)}{A_{core}(s) + sR_F C_{tot} + 1}\ , \tag{2-7}$$

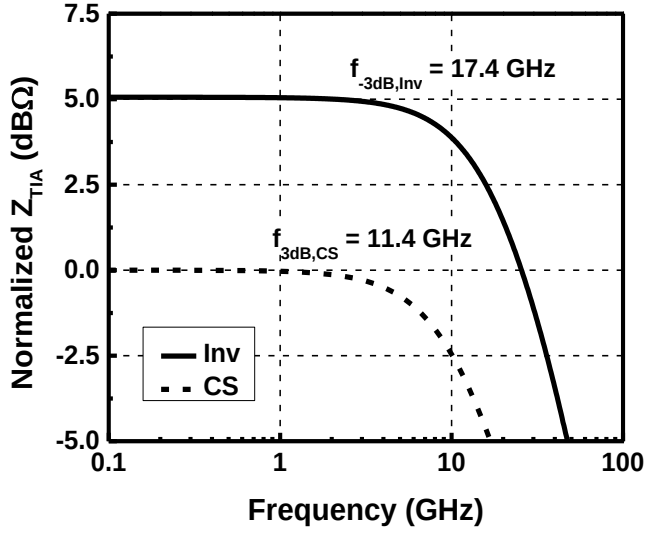
where R_F is the feedback resistor, $A_{core}(s)$ is the core amplifier's open-loop gain response and C_{tot} is the total capacitance at the input node consisting of PD capacitance C_{PD} and parasitic capacitance of the core amplifier C_{in}. Then, the TIA's –3-dB bandwidth is given by

$$f_{-3dB,\,TIA} = \frac{A_{core}}{2\pi\left(R_F C_{tot} + 1/f_{-3dB,\,core}\right)}\ , \tag{2-8}$$

where A_{core} is the core amplifier's low-frequency gain and $f_{-3dB,\,core}$ is the –3-dB bandwidth of



(a)



(b)

Fig. 2.6 Simulated frequency response of (a) core amplifier open-loop gain and (b) closed-loop transimpedance gain.

the core amplifier. Since the $R_F C_{tot}$ is usually much larger than the $1/f_{-3dB,\,core}$, Eq. (2-8) can be simplified to

$$f_{-3dB,\,TIA} \approx \frac{A_{core}}{2\pi(R_F C_{tot})} \,. \tag{2-9}$$

Eq. (2-9) leads to the design insight that A_{core} is more crucial for boosting TIA's bandwidth as long as the $f_{-3dB,\,core}$ is sufficiently higher than the dominant pole $1/2\pi(R_F C_{tot})$. Fig. 2.6(b) shows the simulated frequency response of two feedback TIAs with core amplifiers designed above (with

their frequency response shown in Fig. 2.6(a). As predicted, the –3 dB bandwidth of the TIA with an inverter amplifier outruns by 6 GHz. In the meanwhile, its transimpedance gain is also 5 dB higher than the CS amplifier counterpart. Above analysis illustrates the superiority of an inverter as a core amplifier of a feedback TIA since it provides a higher low-frequency gain with a sufficient bandwidth in advanced technology.

The optimization of the inverter sizing as the core amplifier in a feedback TIA design is studied next. To facilitate the analysis, a transistor width scaling factor α is introduced. With α, Eq. (2-9) can be rewritten as

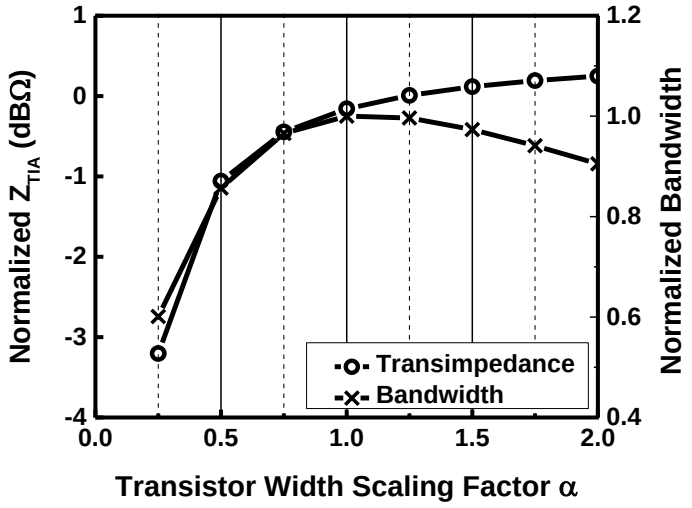
$$f_{-3dB,\,TIA} \approx \frac{A_{core}}{2\pi R_F (C_{PD} + \alpha C_{in})}\,, \tag{2-10}$$

where

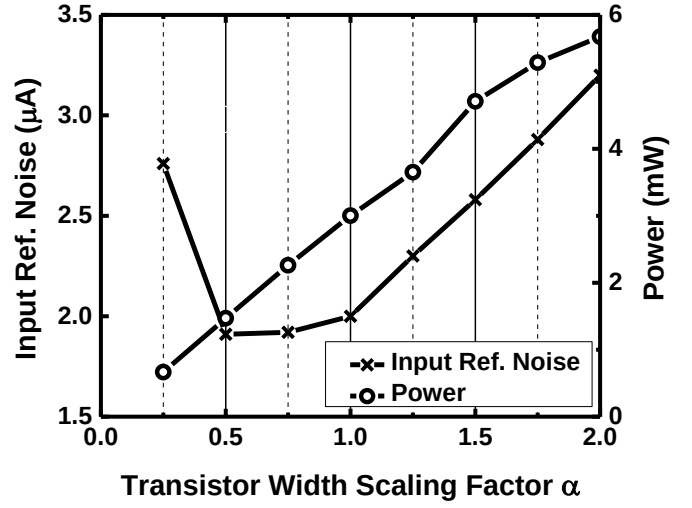
$$A_{core} = \alpha G_m \cdot \left(\frac{R_o}{\alpha} \,//\, R_F\right) \tag{2-11}$$

is the low-frequency open-loop gain of the inverter amplifier. C_{in}, G_m and R_o represent the input capacitance, small-signal transconductance and output resistance of the inverter, respectively. Although the inverter amplifier intrinsic gain ($G_m R_o$) is independent of α, the extra loading from the feedback resistor (R_F) degrades A_{core} and thus Z_{TIA} when the transistors are undersized with $\alpha < 1$. The dependence of the low-frequency Z_{TIA} on α is plotted in Fig. 2.7(a). When $\alpha > 1$, the Z_{TIA} reaches a plateau as A_{core} is saturated at $G_m R_o$. However, with $\alpha > 1$, the bandwidth suffers due to the extra parasitic capacitance. At the same time, more power is wasted, as shown in Fig. 2.7(b). Therefore, the transistor size should be optimized such that the open-loop gain is sufficiently high and thus the low-frequency Z_{TIA} saturates around R_F. For noise consideration, the input referred noise (IRN) current is plotted against α in Fig. 2.7(b). The minimum IRN is observed when $\alpha = 0.5$, below which the IRN increases due to the reduced transimpedance gain. The IRN remains near its minimum level up to $\alpha = 1$ because the total output noise and Z_{TIA} increase at nearly the same rate. Above $\alpha = 1$, the shrinkage in bandwidth causes IRN to increase as the high-

frequency noise is less suppressed when referred to the input as equivalent noise current. Using the 65-nm CMOS general purpose process device models, the optimized inverter amplifier design is achieved when $\alpha = 1$ with $(W/L)_n = 20\mu/60n$ and $(W/L)_p = 50\mu/60n$, respectively. This corresponds to the G_m/I_{bias} ratio of 7 mS/mA and $G_m R_o$ of 8.5 at a current density of 125 μA/μm in optimal bias range for maximizing f_t.



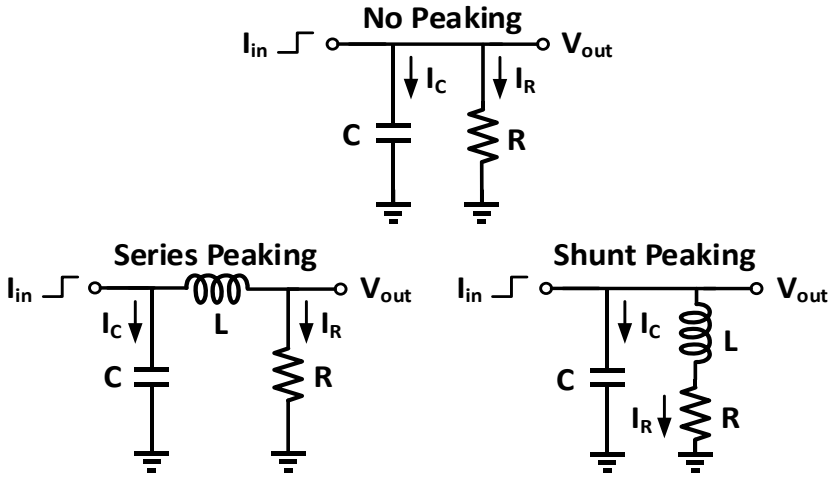
(a)



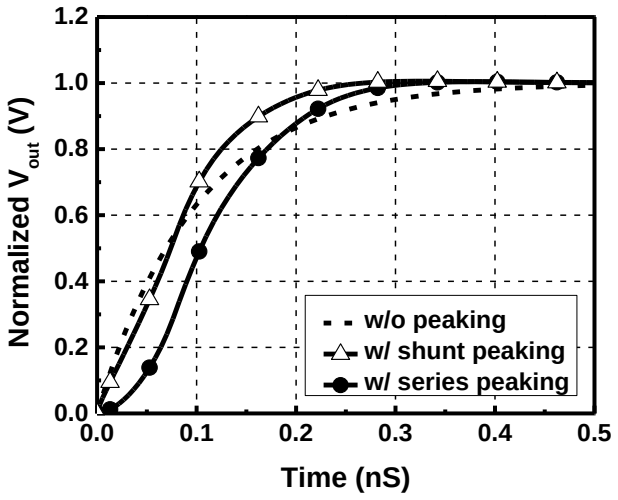
(b)

Fig. 2.7 Optimization of the inverter transistor sizing for (a) TIA gain and bandwidth and (b) IRN and power consumption.

2.3.2 Bandwidth Enhancement Technique



(a)



(b)

Fig. 2.8 (a) Schematic of first-order peaking networks and (b) simulated step responses.

The inductive peaking technique has been widely adopted to extend circuit bandwidth without power penalty [21], [22]. Before addressing the proposed multiple peaking bandwidth enhancement technique, it is beneficial to review the simple first-order series peaking and shunt peaking structures as depicted in Fig. 2.8. For a RC network stimulated by a step current input (I_{in}), the output voltage (V_{out}) takes a rising time delay (τ_r) to reach the steady-state voltage ($I_{in}R$) due to

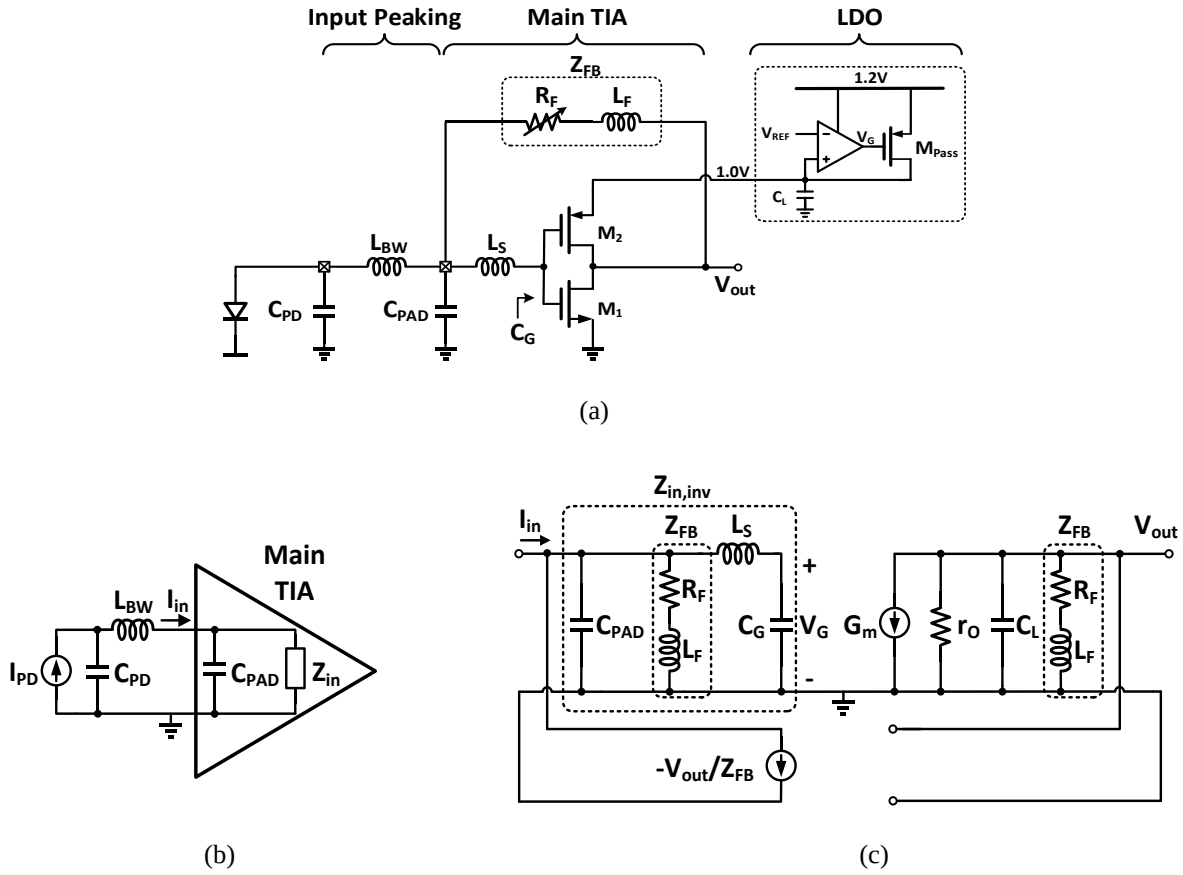


Fig. 2.9 (a) Schematic of the proposed TIA, (b) input series peaking network and (c) small-signal model of the main TIA.

the existence of the loading capacitor (*C*). Since a higher bandwidth is equivalent to having a smaller τ_r in time domain, it would be of great interest to reduce the τ_r for any broadband circuit. Consider the case that the resistor can be disconnected from the network before the capacitor is fully charged. In this way, all of the I_{in} would charge the capacitor such that τ_r is minimized to $\tau_{r1} = 0.8RC$ compared to $\tau_{r0} = 2.2RC$ in the normal case [23]. The rising time is greatly reduced by the so-called "sequential charging technique", which leads to a higher bandwidth. Despite its effectiveness of the "sequential charging technique", it is impractical to implement a switch disconnecting the resistor precisely. However, we can still imitate this method by using an inductor in series with the resistor. Since an inductor tends to resist the high-frequency current change across it, a larger portion of I_{in} would charge the capacitor instead of flowing through the resistor and

extends the effective bandwidth. Depending on the node of output, they are known as series or shunt peaking as shown in Fig. 2.8.

Based on the above understanding of first-order peaking networks, a TIA with multiple inductive peaking network is proposed to boost the TIA gain-bandwidth product. As shown in Fig. 2.9(a), the large PD capacitance is isolated by an input series peaking inductor L_{BW}. In addition, the shunt feedback inductor L_F and the second series peaking inductor L_S further extend the bandwidth of the inverter core amplifier. The proposed TIA can be analyzed in two parts: the input series peaking network and the main TIA. The total transimpedance $Z_T(s)$ is given by

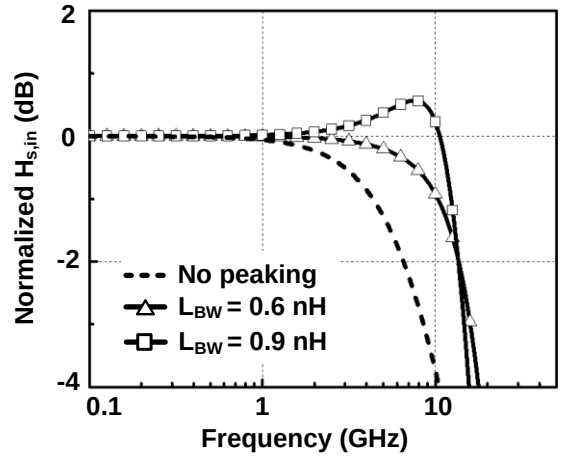
$$Z_T(s) = \frac{V_{out}}{I_{PD}} = \frac{I_{in}}{I_{PD}} \cdot \frac{V_{out}}{I_{in}} = H_{s,\,in}(s) \cdot Z_{TIA,\,main}(s), \tag{2-12}$$

where $H_{s,\,in}(s)$ is the current-mode transfer function of the input series peaking network and $Z_{TIA,\,main}(s)$ is the transimpedance gain of the main TIA.

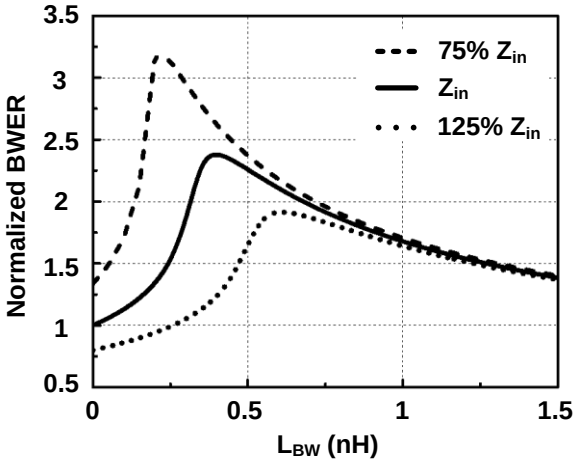
As depicted in Fig. 2.9(b), an equivalent circuit of the input series peaking network is utilized to derive $H_{s,\,in}(s)$. The series peaking inductor L_{BW} inserted at the input node of the TIA isolates the photodetector capacitor C_{PD} and the main TIA, which delays the current flowing into the main TIA and hence reduces the rising time. The transfer function from I_{PD} to I_{in} can be derived as

$$\begin{aligned} H_{s,in}(s) &= \frac{I_{in}}{I_{PD}} \\ &= \frac{sC_{PAD}Z_{in} + 1}{s^3 C_{PD}C_{PAD}Z_{in}L_{BW} + s^2 C_{PD}L_{BW} + s(C_{PD} + C_{PAD})Z_{in} + 1}, \end{aligned} \tag{2-13}$$

where Z_{in} is the effective input impedance of the main TIA. To analyze the peaking network using a generalized peaking factor m_1, Eq. (2-13) is rewritten as



(a)



(b)

Fig. 2.10 (a) Simulated frequency response and (b) BWER of the input series peaking network.

$$H_{s,in}(s) = \frac{\frac{s}{\omega_o}k_1 + 1}{\left(\frac{s}{\omega_o}\right)^3 \frac{k_1}{m_1}(1-k_1) + \left(\frac{s}{\omega_o}\right)^2 \frac{(1-k_1)}{m_1} + \frac{s}{\omega_o} + 1}, \tag{2-14}$$

where $\omega_o = 1/Z_{in}C_{PD}$, $k_1 = C_{PAD}/(C_{PAD} + C_{PD})$ and $m_1 = Z_{in}^2 C_{PD}/L_{BW}$. In our design, Z_{in} is about 60 Ω within the bandwidth of interest. Fig. 2.10 shows the simulated frequency response of $H_{s,in}(s)$ for the target range of L_{BW}. The deviation of L_{BW} introduces small bandwidth variation and less than 1-dB amplitude overshoot. Realized by the input bond-wire inductance, the designed value of L_{BW} is targeted at 0.75 nH to facilitate practical implementation while avoiding the

bandwidth enhancement ratio (BWER) peaking region that is sensitive to L_{BW} as shown in Fig. 2.10(b). The BWER is relatively stable under variation of Z_{in} for L_{BW} around 0.75 nH. In this way, the required tolerance of L_{BW} is relaxed to +/–20% which is well within the control of standard wire bonding equipment. The target range of L_{BW} (0.6~0.9 nH) can be attained using typical wire bonding process. For the L_{BW} from 0.6 nH to 0.9 nH, m_1 ranges from 1 to 1.5 in this design.

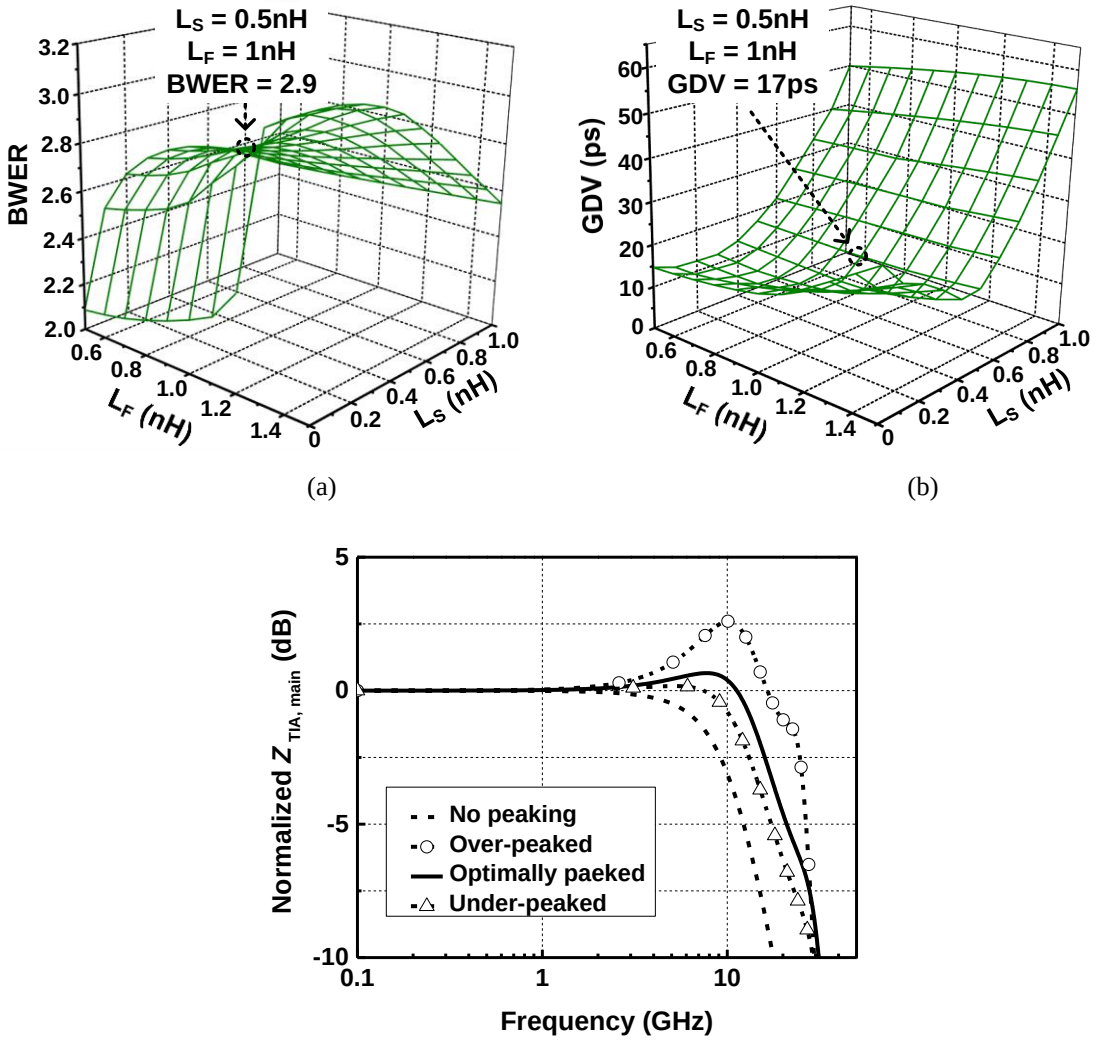
The second and third peaking are created by employing L_F and L_S at the input node of the main TIA to boost the open-loop bandwidth of the core inverter amplifier. As shown in Fig. 2.9(c), the shunt-shunt feedback can be equivalently modeled by an effective loading ($Z_{FB} = R_F + sL_F$) at the input and output of the core inverter amplifier with an added ideal feedback current source ($-V_{out}/Z_{FB}$). The Z_{FB} together with the series peaking inductor L_S form a shunt-series peaking network at the inverter input node. Based on the equivalent circuit, the inverter amplifier open-loop input impedance $Z_{in,\,inv}$ is given by

$$Z_{in,\,inv}(s) = \frac{\frac{s}{\omega_o m_2} + 1}{\left(\frac{s}{\omega_o}\right)^4 \frac{k_2}{m_2 m_3}(1-k_2) + \left(\frac{s}{\omega_o}\right)^3 \frac{k_2}{m_3}(1-k_2) + \left(\frac{s}{\omega_o}\right)^2 \left(\frac{1-k_2}{m_3} + \frac{1}{m_2}\right) + \frac{s}{\omega_o} + 1}, \quad (2\text{-}15)$$

where $m_2 = R_F^2(C_{PAD} + C_G)/L_F$, $m_3 = R_F^2(C_{PAD} + C_G)/L_S$, $k_2 = C_{PAD}/(C_{PAD} + C_G)$ and $\omega_o = 1/R_F(C_{PAD} + C_G)$. It follows that the inverter amplifier open-loop gain under a current-mode input can then be expressed as

$$A_{inv}(s) = Z_{in,\,inv}(s) \cdot G_m \cdot Z_{out,\,inv}(s), \quad (2\text{-}16)$$

where $G_m = g_{m,n} + g_{m,p}$ is the total transconductance of the inverter amplifier and $Z_{out,\,inv}(s) = R_o \,//\, 1/(sC_L) \,//\, Z_{FB}$ is the output impedance of the inverter amplifier. The proposed peaking scheme effectively expands the bandwidth of $A_{inv}(s)$ through boosting $Z_{in,\,inv}(s)$ and $Z_{out,\,inv}(s)$ at high frequencies. By combining A_{inv} and Z_{FB}, the closed-loop main TIA transimpedance can now be expressed as



(a) (b)

(c)

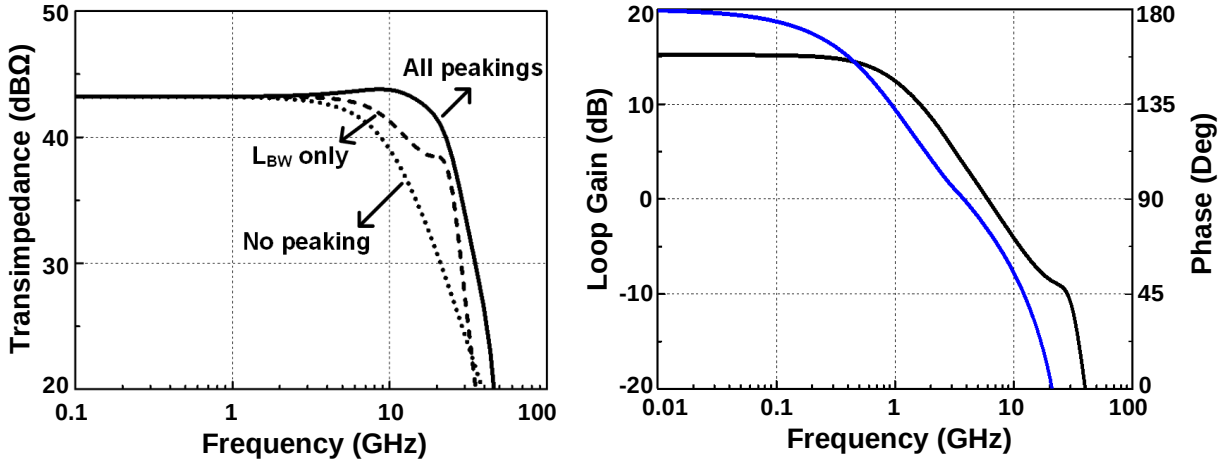
Fig. 2.11 (a) Simulated BWER, (b) group delay variation and (c) frequency response of the main TIA.

$$Z_{TIA,\,main}(s) = \frac{V_{out}}{I_{in}} = \frac{A_{inv}(s)}{1 + A_{inv}(s) \cdot Z_{FB}(s)} \,. \tag{2-17}$$

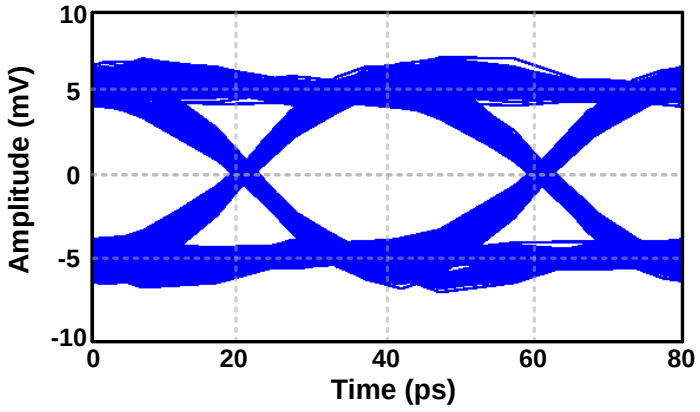
With $H_{s,in}(s)$ and $Z_{TIA,\,main}(s)$ derived, the optimization of the three peaking factors for boosting the total TIA transimpedance gain $Z_T(s)$, listed as Eq. (2-12), can be carried out. The optimization of L_S and L_F is conducted with the consideration of both BWER and group delay variation (GDV) as shown in Fig. 2.11. The high-Q series peaking inductor L_S boosts bandwidth efficiently below 0.5 nH. Further increase of L_S results in excessive amplitude overshoot, reduced

Table III Summary of Multiple Peaking Network

	m_1	m_2	m_3	Ripple (dB)	Z_T BWER
Over-peaked	0.5	1.3	2.5	3.6	2.7
Opt. peaked	1	2.6	5	0.8	2.8
Under-peaked	1	5	7.5	0	1.7



(a)



(b)

Fig. 2.12 Post-layout simulation of (a) frequency response and (b) 25-Gb/s output eye diagram with 50-μA_{pp} input current and 250-fF C_{PD}.

BWER and significant GDV. On the other hand, the bandwidth boosting from L_F is moderate due to the large series resistor R_F. However, the presence of L_F is essential for achieving sufficient BWER with low GDV. Meanwhile, L_F compensates ripples in amplitude response to reduce the

deterministic jitter. The trade-off between occupied chip area, BWER and GDV eventually limits L_F to 1 nH. As summarized in Table II, the optimal peaking factor combination (m_1 = 1, m_2 = 2.6 and m_3 = 5) yields a total BWER of 2.8 with ripple < 1 dB.

Post-layout simulations of $Z_T(s)$ for the proposed TIA are plotted in Fig. 2.12. The TIA bandwidth is improved from 7.5 GHz to 21 GHz, indicating that an overall BWER of 2.8 is achieved by the proposed multiple peaking technique. The frequency response without C_{PD} is also plotted to facilitate the comparison to electrical measurement performed without the photodetector in place. The simulated TIA output eye diagram with 50 μA_{pp} input current at 25 Gb/s indicates low deterministic jitter and low IRN. The simulated average input-referred noise current density is 16 pA/√Hz within 25 GHz. The additional noise of bond-wire inductance L_{BW} is insignificant because of its low series resistance. The noise contribution due to the parasitic series resistance of L_F is negligible because it is absorbed as part of R_F. To keep the noise of L_S to a minimal level, its inductance is set to the minimum value for the target BWER.

2.3.3 Fully-integrated LDO

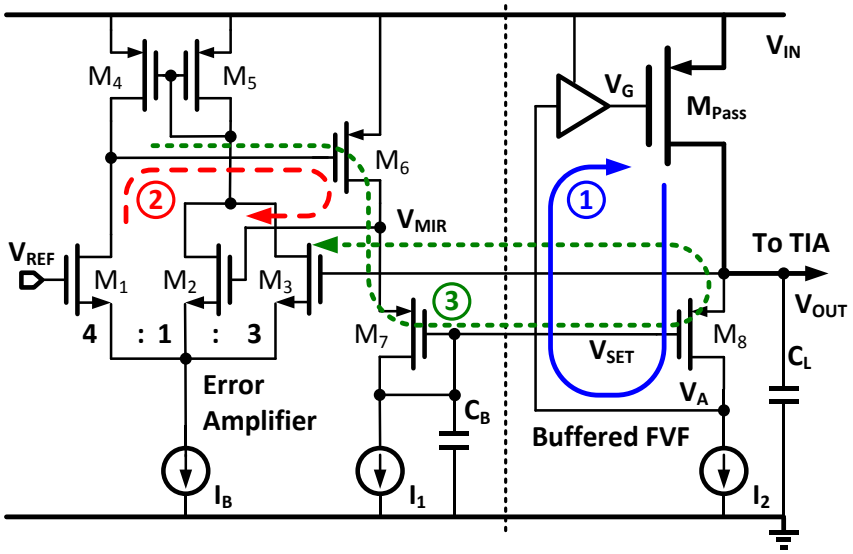


Fig. 2.13 Schematic of the integrated LDO.

Fig. 2.13 shows the schematic of the fully-integrated LDO. The TIA core is designed to operate from a 1 V supply regulated by a point-of-load LDO to reject supply noise and mitigate parasitic supply bonding wire inductance. To provide the 2.5 mA for the TIA running at 25 Gb/s, the LDO should have ultra-fast response and also large output capacitor. Since the loading current of this LDO is small comparing to other general purpose (100 mA) LDOs, it is advantageous to place the LDO dominant pole at its output node for high PSR and fast transient response. Most of the limited available capacitance (silicon area) is allocated to its output node (dominant pole), while the internal poles are pushed to frequencies higher than the unity-gain frequency by using buffer impedance attenuation and flipped voltage follower (FVF) techniques [24]. A triple-input error amplifier is proposed to improve the DC accuracy. The V_{OUT} is regulated by the control loop at low frequency, and the noise is bypassed to ground by C_L at high frequency (> 1 GHz). In the FVF based structure, V_{OUT} is mainly determined by V_{SET}. Therefore, adding a bypass capacitor C_B at the V_{SET} node can improve the PSR in the medium frequency range (around 100 MHz to 1 GHz),

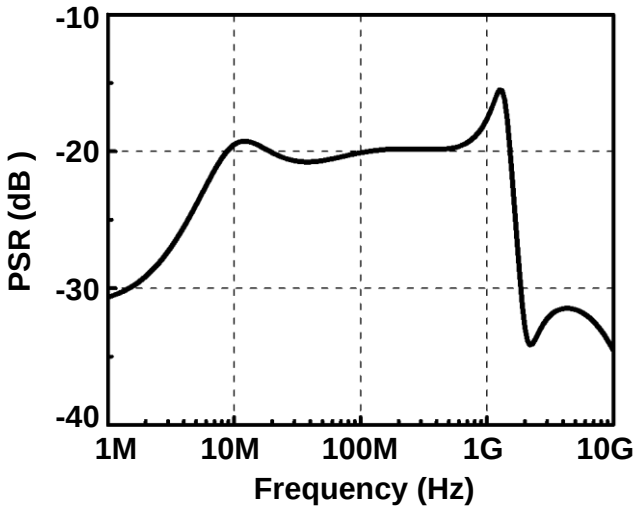
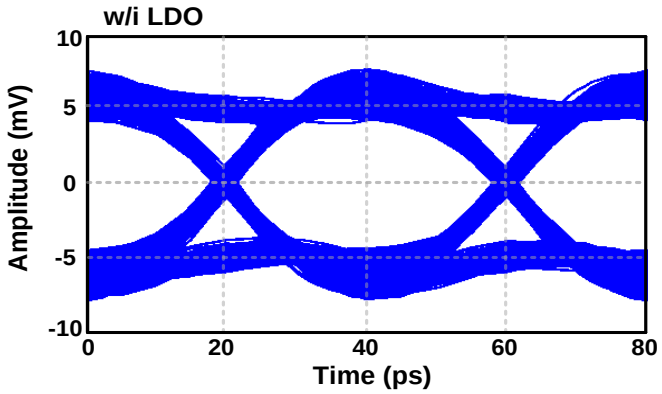


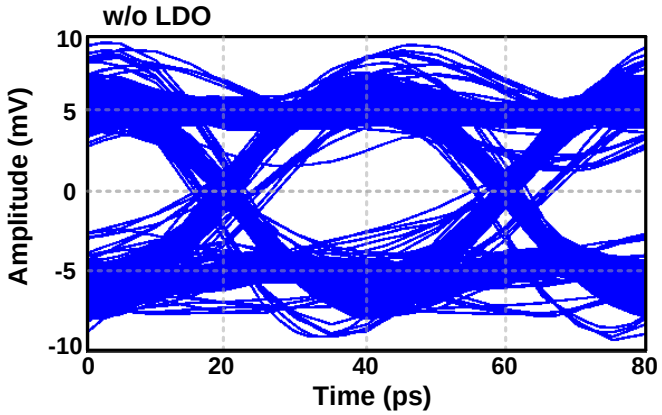
Fig. 2.14 Simulated LDO PSR.

by filtering out the ripple that comes from V_{MIR} to V_{OUT}. The total on-chip capacitance (C_B and C_L) for the LDO is less than 140 pF.

Simulated LDO PSR is shown in Fig. 2.14. The LDO has a PSR better than −19 dB at low frequencies and the worst case occurs around 1.5 GHz with −12 dB rejection. Time domain verification of the supply noise rejection is performed by applying a 100-MHz 10-mV_{pp} square-wave as the supply noise. Fig. 2.15 shows the simulated 25 Gb/s output eye diagram for TIAs with and without integrated LDO, respectively. The P-P jitter degradation of the TIA with integrated LDO is not noticeable. On the other hand, the one without on-chip LDO shows almost a 3 times P-P jitter deterioration. Above simulation results verify that the proposed fast-response integrated LDO can effectively reduce the supply noise induced P-P jitter in single-ended high-speed TIA frontend.



(a)

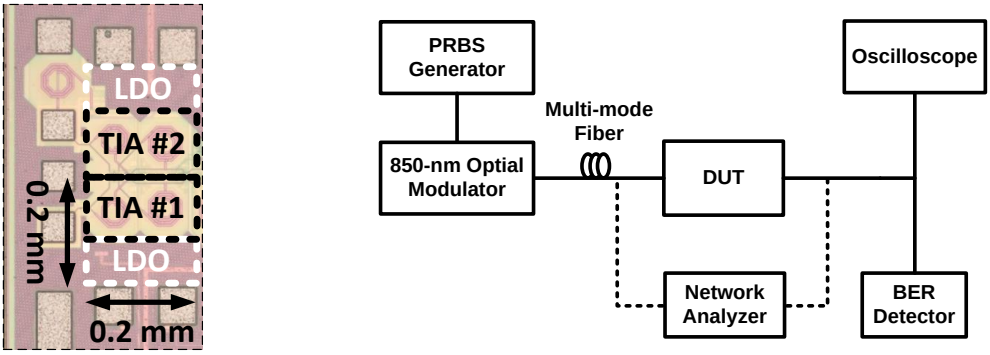


(b)

Fig. 2.15 Simulated 25 Gb/s TIA output eye diagram with 100-MHz 10-mV_{pp} square-wave supply noise: (a) with LDO and (b) without LDO.

Another practical issue in implementing the single-ended TIA is the influence of the parasitic inductance from supply bond-wires. The parasitic bond-wire inductance manifests as the impedance degeneration to the inverter core amplifier at high frequencies, which significantly reduces high frequency transimpedance gain and creates large gain ripple. This issue is alleviated by integrating an on-chip LDO to isolate the Vdd bond-wire inductance and to provide an extra low-impedance ground path through the large area substrate contact in the LDO's loading MOS capacitor.

2.4 Experimental Results



(a) (b)

Fig. 2.16 (a) TIA Chip micrograph and (b) measurement setup.

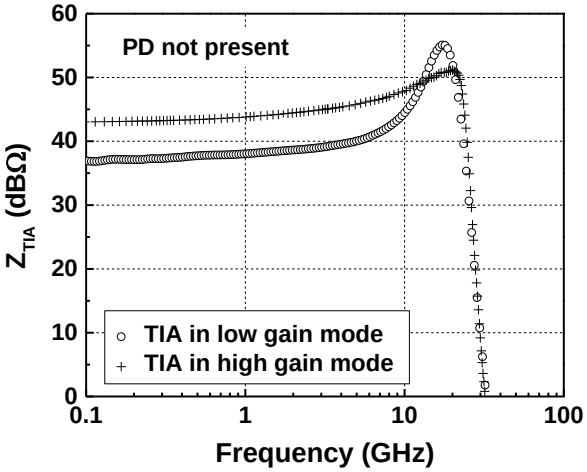
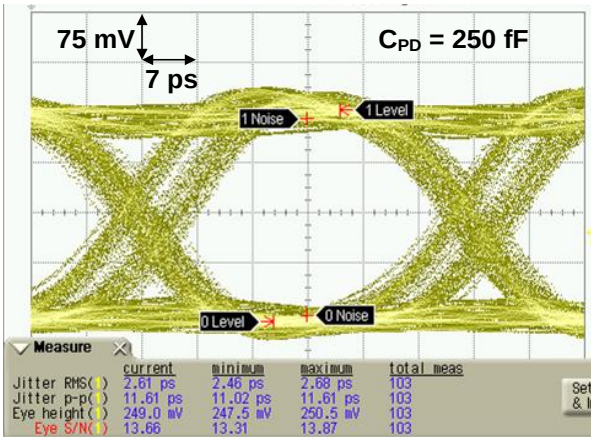
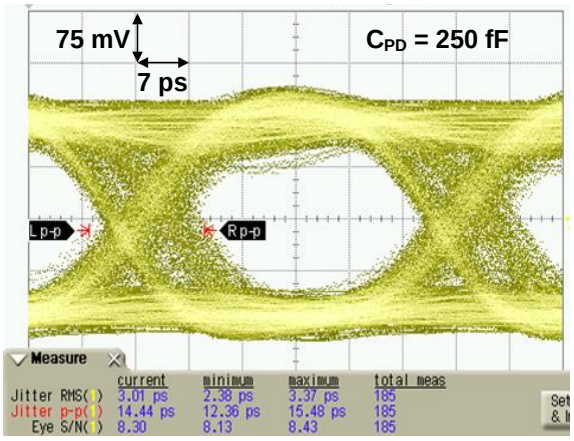


Fig. 2.17 Measured TIA frequency response by direct on-chip probing.

The receiver front-end has been designed and fabricated in a 65-nm CMOS technology. The die photo of the integrated TIA with LDO is shown in Fig. 2.16(a). The core circuit occupies 0.08 mm^2. Fig. 2.16(b) shows the measurement setup for electrical frequency domain measurement and optical time domain measurement. The frequency response is obtained by measuring the TIA's s-parameter via on-die probing. The optical input signal is generated by an 850-nm Mach-Zehnder Modulator fed with a 25-Gb/s PRBS generator. The PD used in the optical measurement has a



(a)



(b)

Fig. 2.18 Measured optical eye diagram at 25 Gb/s with (a) LDO enabled (RMS Jitter = 2.6 ps, P-P Jitter = 11.6 ps) and (b) LDO disabled (RMS Jitter = 3 ps, P-P Jitter = 14.4 ps).

responsivity of 0.4 W/A and 28-GHz bandwidth. The TIA's electrical output eye diagram is captured by a high-speed sampling scope. An error detector is used for the BER test.

Fig. 2.17 shows the frequency response of the TIA in both high and low gain mode. The frequency response is converted from the measured S-parameters based on [25]

$$Z_{TIA} = \frac{s_{21}}{(1-s_{11})(1-s_{22})} \cdot Z_o, \tag{2-18}$$

where Z_o = 50 Ω is the characteristic impedance of the equipment. A single-ended transimpedance gain of 42 dBΩ with 24-GHz bandwidth is achieved. A 4-dBΩ tuning range controlled by 4 digital

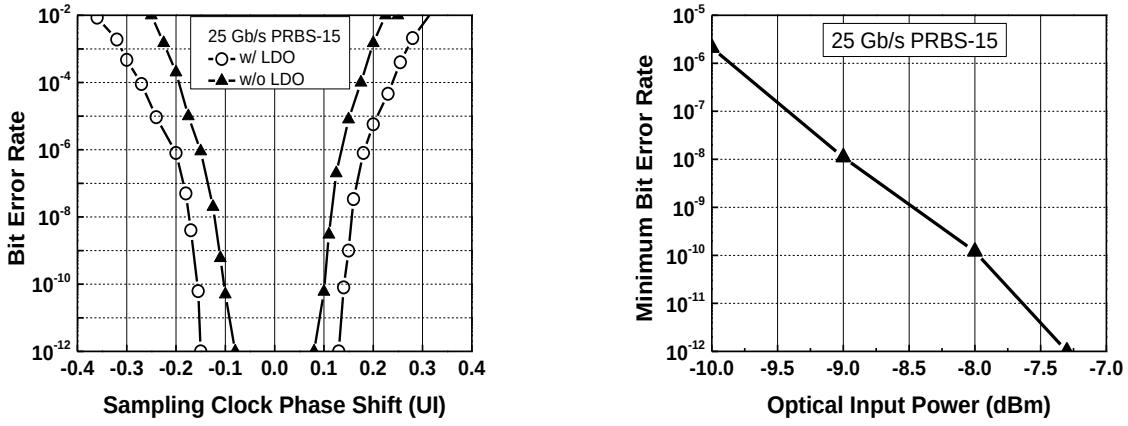
bits is designed to compensate the process and PD loading variation. The gain peaking at 20 GHz is an artifact due to the absence of the PD capacitive loading during s-parameter measurement by direct on-chip probing.

Fig. 2.18 shows the measured TIA output eye diagram with the LDO enabled and disabled respectively. The RMS and P-P jitter are improved by 0.4 ps (15%) and 2.8 ps (24%) respectively when the LDO is enabled. The reduced jitter improves the horizontal eye opening by 12% at a BER less than 10^{-12} as observed in the BER bathtub curves shown in Fig. 2.19. The relatively narrow error free open range is limited by the insufficient sensitivity of the BER tester.

Table IV summarizes the performance of the proposed TIA and compares to recently published results. To facilitate the performance comparison, a FOM defined by

$$\text{FOM} = \frac{\text{Gain} \cdot \text{Bandwidth}}{\text{Power} \cdot \text{Sensitivity}} \tag{2-19}$$

is introduced. This work achieves the highest FoM by achieving state-of-the-art GBW and sensitivity with greatly reduced power dissipation.



(a) (b)

Fig. 2.19 (a) BER bathtub curve with and without LDO enabled and (b) optical input sensitivity curve.

Table IV TIA Performance Comparison and Summary

	TIA in [14] JSSC '14	TIA in [13] ISSCC '13	TIA in [26] JSSC '13	**This work**
Topology	LBW TIA +EQ	CML FB	XFM RGC	Inv. FB
Bandwidth (GHz)	20.5^{+}	21	26	24
Data Rate (Gb/s)	25	25	27^	25
C_{PD} (fF)	80	150	150	250
Gain (dBΩ)	57.2^{+}	41	53	42
Sensitivity (μA)	59	98	93^	74
Supply (V)	1	1	1.9	1.2/1
Power (mW)	N/A	4.8	28.2	3
Technology	65-nm CMOS	65-nm CMOS	0.25-μm BiCMOS	65-nm CMOS
FOM	N/A	5.0	4.4	13.6

$^{+}$ Simulation result.

^ Electrical measurement.

Chapter 3 Fully Integrated Optical-to-Millimeter-Wave Modulator

3.1 Introduction

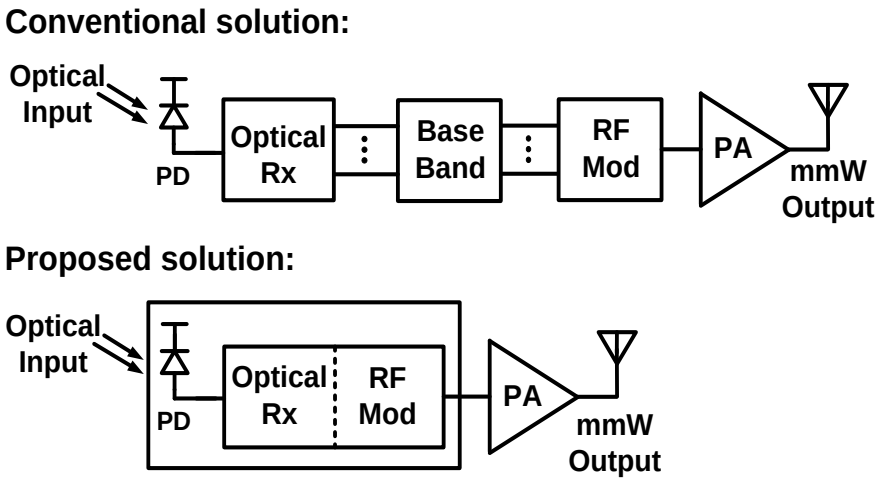


Fig. 3.1 Comparison between a conventional and the proposed fiber-wireless system

This chapter presents an optical-to-mmW modulator SoC with an integrated 850-nm wavelength optical receiver front-end for short-range backhaul connectivity in emerging fiber-wireless mobile networks. As discussed in Chapter 1, the BoF system alleviates the performance requirement on optical links since only the baseband signal is transmitted in optical domain. However, energy efficient and cost effective O/E conversion and RF transmission systems at remote cells are necessary for the BoF scheme to outperform the RoF scheme. Therefore, an integrated module capable of directly converting signals between the optical and the mmW domain is needed to reduce the overhead in system size and cost for supporting fiber-wireless backhaul links. As shown in Fig. 3.1, a conventional fiber-wireless system usually consists of discrete components and several chips to perform O/E conversion, baseband processing and RF transmission. In contrast, the proposed system integrates the photodetector on-chip and combines the optical and RF blocks to eliminate redundant baseband de-multiplexing and multiplexing, resulting in a more efficient and compact fiber-wireless system.

Compared to traditional implemented in III-V technology, CMOS monolithic optoelectronic integrated circuits (OEICs) is a promising technology to achieve low-cost, small system form factor and high volume manufacturing capacity in optical communication systems. However, the performance of OEICs is usually limited by the inferior CMOS optical components. Several techniques have been demonstrated to improve performance of CMOS on-chip PDs. A spatially-modulated PD [12] is presented to improve PD bandwidth by canceling the slow diffusion current at the price of lower responsivity. [25] presents CMOS PDs fabricated with process modification to achieve low parasitics and high bandwidth. However, extra process steps result in high cost and specific foundry limitation. To further push the performance, the CMOS on-chip PD can be biased at avalanche mode to realize over twofold improvement in responsivity and bandwidth. Nevertheless, the high bias voltage increases system design complexity and reliability risk.

The unlicensed 60-GHz band has been demonstrated to accomplish mmW backhaul links for the next generation cellular systems[6], [27]. The unique advantages of mmW frequency bands include the widely available underutilized spectrum and the line-of-sight type of communication which alleviates interference between cells. Moreover, advancements in CMOS mmW circuits in recent years ensure the integration of the hybrid fiber-wireless system. [27]-[28] have demonstrated that a multi-gigabit wireless link can be realized in 65-nm CMOS technology in the 60-GHz band.

This chapter presents the design and measured performance of a 4-Gb/s NRZ-to-QPSK modulator SoC which consists of a fully integrated optical receiver (Rx) for 850-nm wavelength input and a 60-GHz I/Q up-convertor [29]. Realized in 65-nm CMOS, the optical front-end achieves −3-dBm optical input sensitivity at 4 Gb/s with less than 10^{-12} BER. The wireless modulator directly up-converts the de-multiplexed 2-Gb/s I/Q NRZ data to a 4-Gb/s QPSK signal at 60 GHz. The SoC consumes 78 mW and produces −7.2-dBm output power with −12-dB EVM at a bit efficiency of 19.6 pJ/b. The SoC core area occupies only 0.19 mm^2. Our design demonstrates

that a small form factor and low cost optical-to-mmW modulator can be realized to support future fiber-wireless networks.

3.2 Optical-to-mmW Modulator System

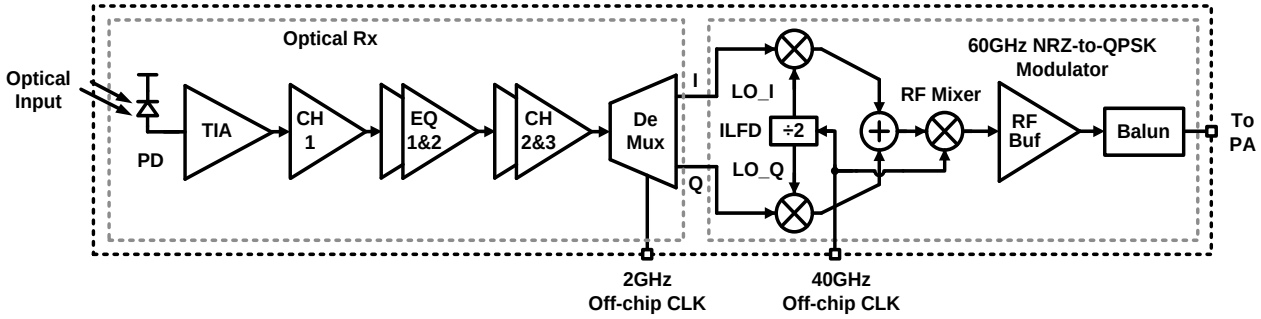


Fig. 3.2 System diagram of the proposed modulator.

Fig. 3.2 shows the system diagram of the proposed modulator. The modulator consists of a fully integrated transimpedance amplifier achieves high gain-bandwidth product without using inductive peaking. The two-stage equalizer extends the operation data rate to 4 Gb/s with a photodetector bandwidth of 0.5 GHz. Following the optical Rx, a de-multiplexer (DeMux) generates half-rate I and Q data feeding to the 60-GHz I/Q modulator. The 60-GHz modulator employs a pair of 20-GHz IF I/Q mixers and a 40-GHz RF mixer followed by a RF buffer with an on-chip balun for driving a single-ended off-chip power amplifier (PA). To avoid LO pulling and ease LO generation, the sliding IF architecture is adopted in the 60-GHz modulator. Image rejection filters are not adopted in this design because the potential image signals fall at 40 GHz and 100 GHz would be significantly rejected by the narrow-band resonant circuits.

3.3 Fully Integrated Optical Receiver

Table V: Fiber-Wireless Modulator System Performance Breakdown

	TIA	CH1	EQ1&2		CH2&3	Rx Total		IF Mixer	RF Mixer	RF Buff	Mod Total
			En.	Dis.							
Gain (dBΩ, dB)	60	10	–10	10	20	80-100	**Gain (dB)**	6	0	1	7
BW (GHz)	4.5	7	7.5	N/A	7	4	**BW (GHz)**	6 @ 20 GHz	7 @ 60 GHz	7 @ 60 GHz	5.5 @ 60 GHz
IRN (pA/sqrt(Hz))	15	4.4	3.5	2.2	1.2	24.1	**NF (dB)**	10.5	8.9	8.6	13.7
Pwr (mW)	5	7.5	7.5		15	35	**Pwr (mW)**	11	13	11	35

The optical receiver design is challenging due to the low responsivity, insufficient bandwidth and heavy capacitive loading of the on-chip PD. To achieve a compact and low-cost system, the PD is biased in standard reverse bias mode (V_{bias} = 0.5 V) instead of avalanche mode (V_{bias} = 12 V). Under this standard reverse bias condition, the on-chip PD has a responsivity of 51 mA/W and a parasitic capacitance of 480 fF with 0.5-GHz bandwidth [30]. The low PD responsivity requires a low-noise receiver front-end to achieve high sensitivity. The system input referred noise (IRN) requirement can be derived from the target sensitivity level (–3 dBm) and the PD responsivity (51 mA/W). Under the target sensitivity level, the on-chip PD generates 25.5-μA_{pp} input current for the receiver. As a rule of thumb, a signal-to-noise ratio (SNR) of 7 is required for the receiver to achieve a BER < 10^{-12} [31]. Therefore, the receiver integrated IRN must be lower than 1.82 μA, which is equivalent to 30 pA/sqrt(Hz) within 4-GHz bandwidth. As shown in Table IV, the receiver IRN is designed to be 24.1 pA/sqrt(Hz) with some margin for the actual implementation. The TIA contributes more than 60% of the total IRN because its noise is not attenuated by any preceding gain stage. To minimize the noise contribution of following stages, the TIA gain is maximized by the proposed gain-boosted inverter based core amplifier. Since the continuous-time linear equalizer (CTLE) exhibits negative gain at low to mid frequencies when it is enabled, it effectively boosts the noise contribution of subsequent amplifier stages. In order to

alleviate this noise boosting, one of three post-amplifiers is placed before the CTLE to provide 10-dB gain without saturating the equalizer. The minimum required transimpedance gain is calculated to be 80 dBΩ from the 300-mV output amplitude required to correctly trigger the DeMux.

3.3.1 CMOS On-chip Photodector

In an optical communication system, the optical input signal has to be converted to electrical signal for subsequent amplification and process. The O/E conversion is performed by a PD. The most common PD is a reverse biased p-n junction. Electron-hole pairs are generated when the incident photon energy exceeds the bandgap energy of the junction material. The generated electron-hole pairs are then drifted towards different directions by the biasing voltage and thus results in photo current. A photodiode material should be chosen with a bandgap energy slightly less than the photon energy corresponding to the longest operating wavelength of the system.

The PD responsivity is defined as the ratio between the generated current and incident optical power. A commercial PD usually behaves a typical responsivity in the range of 0.6 to 0.9A/W. However, the on-chip CMOS PD could be more than 20× worse as we will see later in this chapter. The responsivity could be significantly improved by operating the PD in avalanche mode. In avalanche mode, the electron-hole pairs generated contain so much energy that they can stimulate other electrons and holes to create a current multiplication effect.

The bandwidth of PD is mainly determined by: (1) the time it takes for the carriers to drift through the drift-field region called transit time and (2) the RC time constant arose from the parasitical resistance and junction capacitance. Therefore, the PD bandwidth can be expressed as [17]

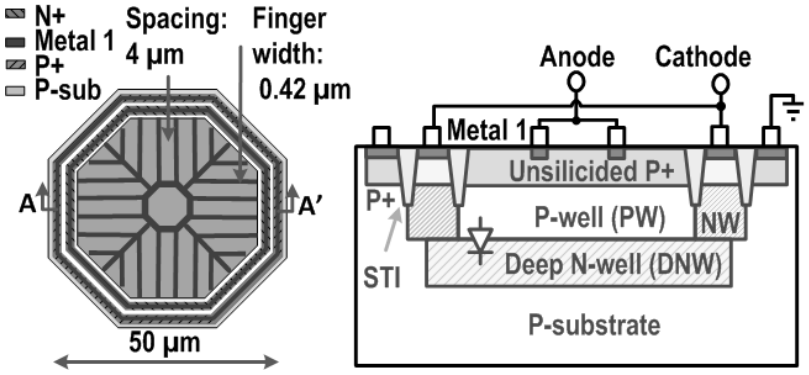
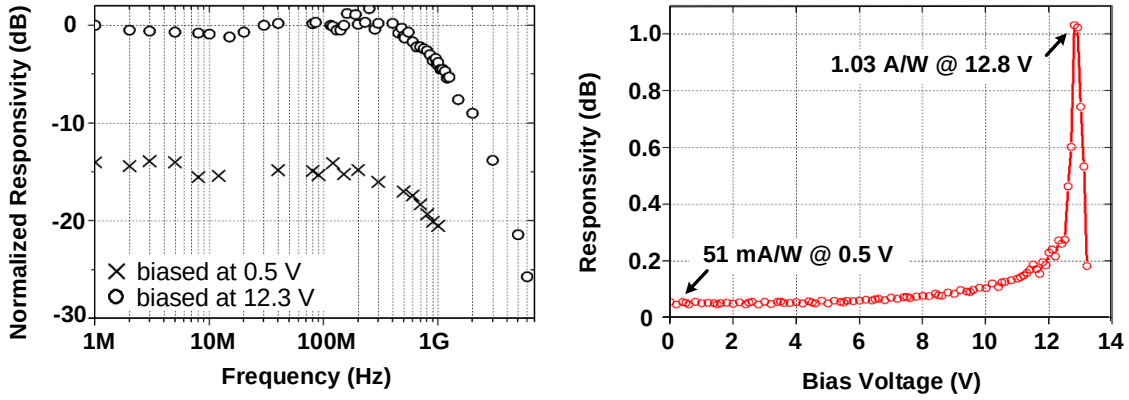


Fig. 3.3 Layout and cross-section views of the CMOS PW/DNW PD.



(b) (c)

Fig. 3.4 (a) Measured PD frequency response and (b) PD responsivity versus biasing

$$f_{PD} = \frac{1}{2\pi} \cdot \frac{1}{W/v_n + R_{PD}C_{PD}}, \tag{3-1}$$

where W is the width of the depletion region, v_n is the carrier velocity, R_{PD} and C_{PD} are the parasitical resistance and capacitance, respectively. The reverse bias voltage should be sufficiently large such that the v_n is saturated and the transit time is minimized.

The layout and cross-section views of the on-chip PW/DNW PD used in this design are depicted in Fig. 3.3 [30]. The P-well with P+ doping is used as the anode of the PD. The P+ doping is added on top of the PW to reduce the extrinsic series resistance. Meanwhile, to minimize the reflection of the incident light by the silicide layer and thus avoid responsivity degradation, one silicide blocking layer, the resist protection oxide, is used to keep P+ unsilicided, except under the metal

contact area. With these modifications, the proposed PD eliminates the slow diffusion current of the P-substrate. Moreover, the deeper and wider depletion region of the PD improves light absorption efficiency.

The measured PD frequency response is shown in Fig. 3.4(a) with the responsivity normalized to the avalanche mode low-frequency responsivity of 272 mA/W. The measured −3-dB bandwidth is 1.1 GHz and 0.5 GHz in avalanche and standard mode, respectively. In addition to the bandwidth shrinkage, the PD operating in standard mode also delivers 14-dB less responsivity of 51 mA/W compared to the avalanche mode counterpart. Despite the performance advantages when operated in avalanche mode, the required high bias voltage is usually difficult to generate in modern SoC systems. In addition, the steep bias dependency shown in Fig. 3.4(b) evidences that an adaptive control loop is necessary for robust operation in avalanche mode across PVT variations. As a result, the on-chip PD in this work is operated in standard mode to ensure a compact and reliable system, making the design of the receiver quite challenging.

3.3.2 Transimpedance Amplifier

The TIA in the optical receiver has to provide an input impedance less than 100 Ω to attain the required bandwidth, while featuring high transimpedance gain to degenerate IRN from subsequent stages. Conventionally, the shunt-shunt feedback technique is adopted in TIA designs to reduce the input impedance. However, the insufficient core amplifier gain in advanced technology nodes strongly constrains the effectiveness of feedback on bandwidth extension. The feedback TIA transimpedance gain is expressed as

$$Z_{TIA}(s) = R_F \cdot \frac{A_{core}(s)}{A_{core}(s) + sR_F C_{tot} + 1}\ , \tag{3-2}$$

where $\mathrm{A_{core}(s)}$ is the open-loop gain of the core inverter amplifier, $\mathrm{R_F}$ is the feedback resistor and

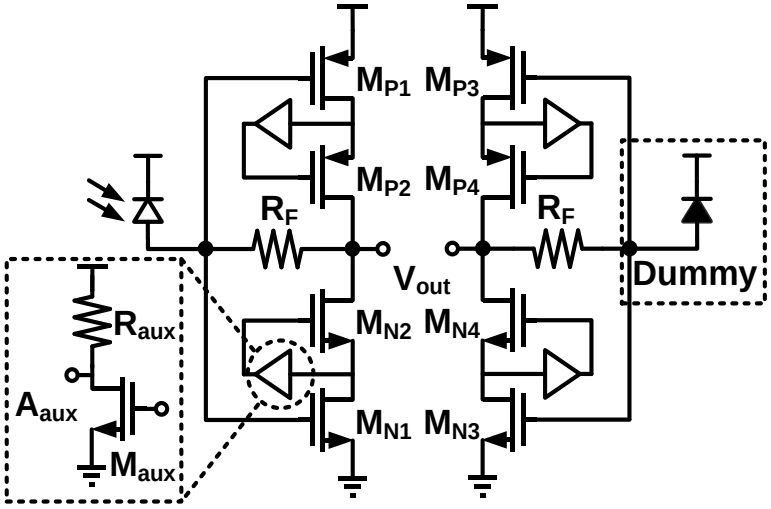


Fig. 3.5 Schematic of the TIA based on a gain-boosted inverter.

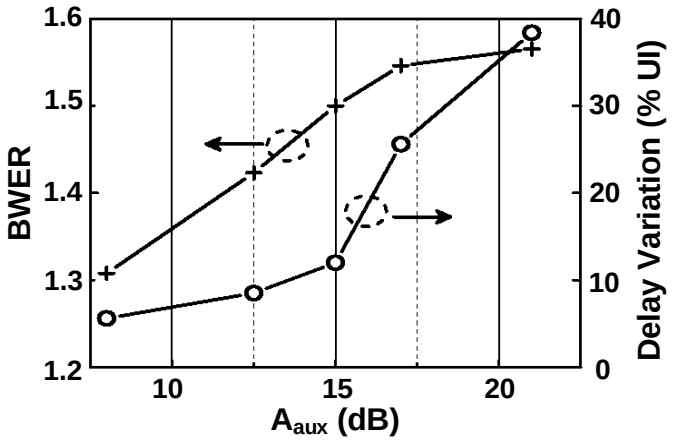
C_{tot} is the total capacitance at the input node consisting of PD capacitance and parasitic capacitance of the core amplifier. Then, the TIA's –3-dB bandwidth is given by

$$f_{-3dB,\,TIA} = \frac{A_{core}}{2\pi\left(R_F C_{tot} + 1/f_{-3dB,\,core}\right)}\,, \tag{3-3}$$

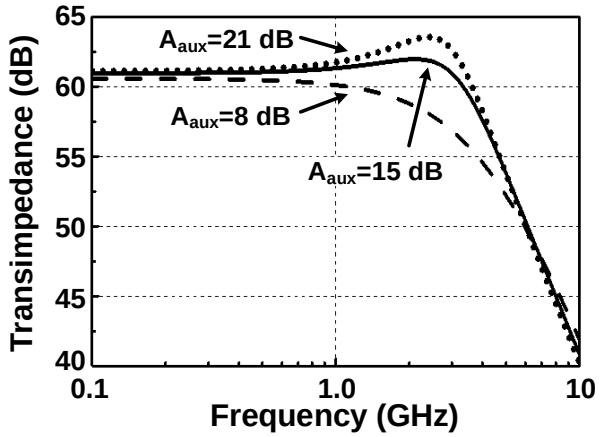
where $f_{-3dB,\,core}$ is the bandwidth of the core inverter amplifier. Since the input pole formed by $R_F C_{tot}$ (at 0.3 GHz) is much lower than $f_{-3dB,\,core}$, Eq. (3-3) can be further simplified to

$$f_{-3dB,\,TIA} \approx \frac{A_{core}}{2\pi(R_F C_{tot})}\,. \tag{3-4}$$

Eq. (3-4) indicates that A_{core} is more crucial for boosting TIA's bandwidth as long as the $f_{-3dB,\,core}$ is sufficiently higher than the frequency of the input dominant pole. However, the core amplifier output impedance usually constrains the maximum achievable open-loop gain in advanced technology when the loading effect of the feedback resistor becomes negligible as it approaches kilo-ohm. Simply increasing the inverter amplifier effective transconductance (G_m) to



(a)



(b)

Fig. 3.6 (a) BWER and group delay variation and (b) closed-loop frequency response.

compensate for the insufficient output impedance is ineffective since the inverter intrinsic output impedance declines at nearly the same rate as the increase of G_m. In order to alleviate the above trade-off and achieve high GBW and small area, a gain-boosted inductor-less feedback TIA is proposed as shown in Fig. 3.5. The TIA core consists of a cascode CMOS inverter amplifier and two auxiliary common-source amplifiers to boost the inverter output impedance and hence the TIA open-loop gain. With the auxiliary amplifiers, the open-loop gain of the core inverter amplifier is expressed as

$$A_{core}(s) = \frac{G_m \cdot ((A_{aux} \cdot r_o) \parallel R_F)}{1 + \frac{s}{\omega_o}} \tag{3-5}$$

where $$A_{aux} = g_{m,aux} \cdot R_{aux} \tag{3-6}$$

is the gain of the auxiliary amplifier, $g_{m,aux}$ is the transconductance of M_{aux} and R_{aux} is the output loading resistor. A_{aux} should be chosen carefully to attain a high BWER while avoiding excessive overshooting in the TIA closed-loop frequency response. The damping factor of the proposed TIA is given by

$$\zeta = \frac{1}{2} \cdot \frac{R_F \cdot C_{in} \cdot 2\pi f_{-3dB,\,core} + 1}{\sqrt{A_{core} \cdot 2\pi f_{-3dB,\,core} \cdot R_F \cdot C_{in}}}, \tag{3-7}$$

To achieve most bandwidth extension with overshooting less than 1 dB, the damping factor is set to 0.6 for the initial design of A_{aux}. Fig. 3.6 shows the BWER and group delay variation under various A_{aux} settings. The BWER saturates at around 1.6 while the peaking rises with the increase of A_{aux}. The bandwidth shrinkage of the core amplifier after the output impedance boosting results in insufficient phase margin in closed-loop response and thus excessive peaking. Furthermore, the group delay variation of the proposed TIA is also greatly related to A_{aux}. Similar to the inductive peaking bandwidth extension technique, an excessive peaking in gain response usually leads to severe group delay variation. As a trade-off between BWER and group delay variation, the designed TIA adopts a A_{aux} of 15 dB, attaining a BWER of 1.5 with 1-dB peaking in gain response as shown in Fig. 3.6(b) and group delay variation of 12 % UI. The overall TIA achieves 61-dBΩ transimpedance gain with 4-GHz –3-dB bandwidth and 15-pA/sqrt(Hz) IRN.

3.3.3 Continuous Time Linear Equalizer

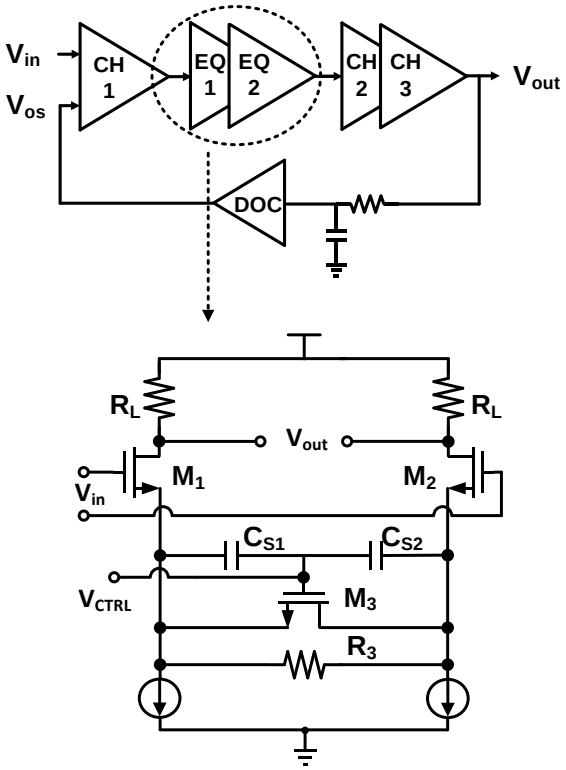


Fig. 3.7 Schematic of the continuous time equalizer.

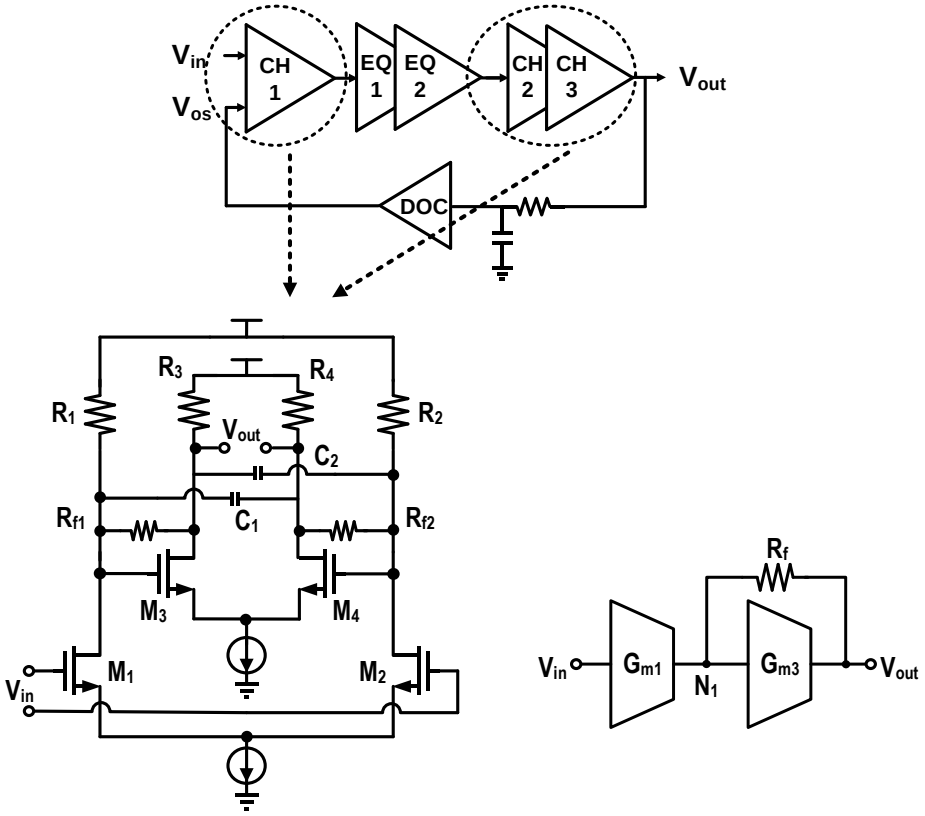
The measured optical frequency response of the standalone PD testing chip shows a slow roll-off frequency response with a slope of 5−10 dB/decade. Therefore, a continuous time linear equalizer (CTLE) with a slow roll-up frequency response is required to complimentarily compensate for the insufficient bandwidth of the on-chip PD to achieve higher data rate. The CTLE shown in Fig. 3.7(a) generates a peaking at high frequency by inserting capacitive degeneration to attenuate low frequency gain which is equivalent to creating an additional zero in the transfer function. The CTLE transfer function is given by

$$H(s) = \frac{g_m}{C_L} \cdot \frac{s + \frac{1}{R_s C_s}}{(s + \frac{1 + \frac{g_m R_s}{2}}{R_s C_s})(s + \frac{1}{R_L C_L})}, \tag{3-8}$$

where g_m is the differential pair transconductance, C_L is the CTLE output loading capacitor, R_s is the source degeneration resistance, C_s is the source degeneration capacitance and R_L is the loading resistor. The high frequency boosting capability of a CTLE is generally limited by the gain-bandwidth of the differential amplifier (the pole at CTLE output). The frequency response of a CTLE can be tuned by the degeneration resistor and capacitor. Increasing R_s effectively enhances low frequency attenuation while increasing C_s moves the zero to lower frequency. However, CTLE's roll-up slop is fixed around 20 dB/decade since the peaking is created by a single zero. Thus, a CTLE is usually only effective for compensating first order frequency roll-off. In order to achieve the required slow roll-up response, two CTLE stages in the receiver are designed with different peaking frequencies located at 1.5 GHz and 5 GHz to interpolate the positions of zeros and poles.

3.3.4 Limiting Amplifier

After the CTLE, a three-stage post amplifier is used to provide additional 30-dB gain and 300-mV output swing. The Cherry-Hooper (CH) amplifier is widely used in high-speed Rx designs due to its great gain-bandwidth performance. Fig. 3.8 shows the schematic and the equivalent circuit of the CH amplifier. A CH amplifier is effectively a two-stage amplifier with the first transconductance stage ($M_{1,3}$) acts as a V/I converter and the second stage acts as a TIA to perform I/V conversion. Compared to a traditional two-stage amplifier, the CH amplifier utilizes a build-in TIA formed by G_{m2} and R_f to reduce the impedance at node N_1 while maintaining high gain via the second stage feedback resistor R_f. To alleviate the voltage headroom issue, R_1 and R_2 are added to provide additional bias current branch. A pair of negative miller capacitance C_m is used to partially cancel the C_{gd} of the input differential pair M_1 and M_2. In this design, each CH amplifier provides 10-dB gain with 7.5-GHz bandwidth.



(a) (b)

Fig. 3.8 (a) Schematic of the Cherry-Hooper limiting amplifier and (b) equivalent small signal model.

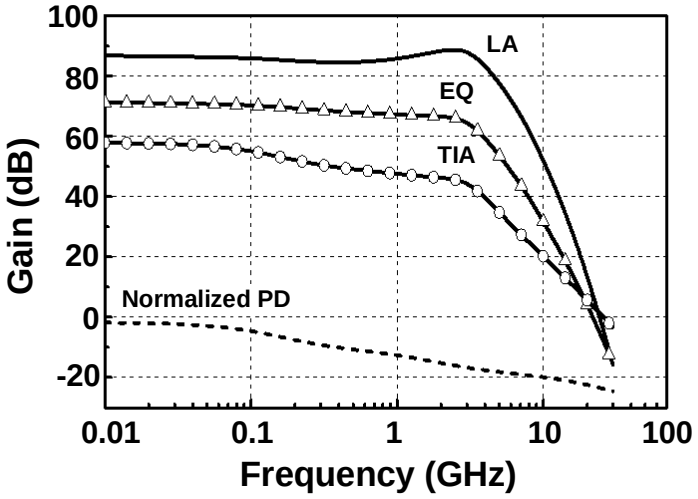


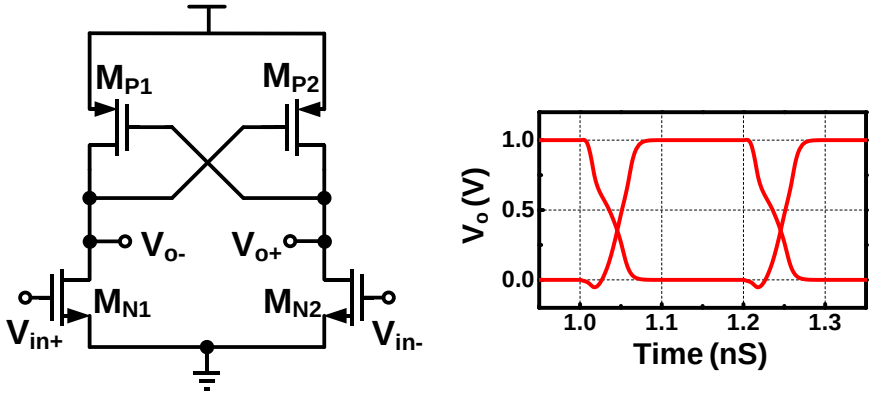
Fig. 3.9 Simulated progressive frequency response of the optical receiver.

Fig. 3.9 shows the simulated progressive frequency response of the receiver. A normalized PD transfer function model is built based on measurement results shown in Fig. 3.4 to facilitate system

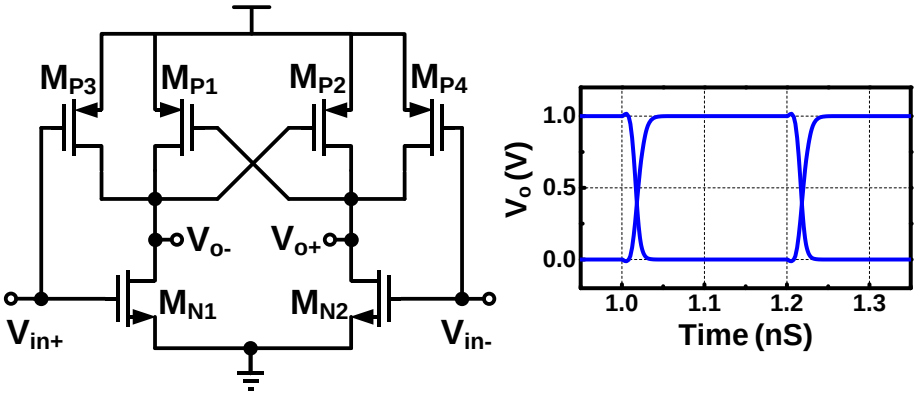
design. As depicted in the simulation, the equalizer compensates for the slow roll-off and insufficient bandwidth of the PD while the TIA provides 61-dB transimpedance gain in front to degenerate IRN. After the equalizer, the 2-stage CH amplifier delivers an additional 20-dB gain and further extends the bandwidth with a peaking allocated at 3 GHz. The differential DC offset of the amplifier chain is extracted by an R-C low-pass filter with its corner frequency set at 10 KHz to avoid output DC level droop in the presence of long consecutive bits. The feedback amplifier provides 40-dB gain for the offset cancellation loop and feeds the error to the first amplifier.

3.3.5 De-multiplexer

The last stage of the receiver is a 1:2 DeMux for de-serializing the input into two branches of half-rate I/Q baseband data. The differential cascade voltage switching logic (DCVSL) shown in Fig. 3.10 is adopted in the DeMux due to its compatibility of interfacing with CML level input without level shifter. However, the conventional DCVSL [32] shown in Fig. 3.10(a) suffers from inherent asymmetry in falling and rising propagation time. For example, when $Vin+$ switches from low to high, $Vo-$ would be pulled down by a strong M_{N1}. However, M_{N1} cannot be made excessive large in order to accommodate the low input loading feature of DVCSL. Therefore, M_{N1} has to fight with M_{P1} during the pull-down period, which results in a long high-to-low propagation delay (τ_{HL}). Even worse, the rising activity at $Vo+$ only starts when $Vo-$ is lower than a threshold voltage of M_{P2}. As a result, τ_{HL} and τ_{LH} are inherently asymmetric and limited by the size of M_{N1} and M_{N2}. To overcome this issue, Fig. 3.10(b) shows the modified DCVSL used in this design featuring an extra pair of pull-up transistors (M_{P3}-M_{P4}) slaved to the input to speed up the output transition. In contrast, the proposed modified structure utilizes two extra pull-up helpers (M_{P3} and M_{P4}) to alleviate the fighting between M_{N1} and M_{P1}. For example, when $Vin-$ switches from high to low, the pull-up helper M_{P4} aids to charge $Vo+$ before $Vo-$ is able to turn on M_{P2}, accelerating turning



(a)



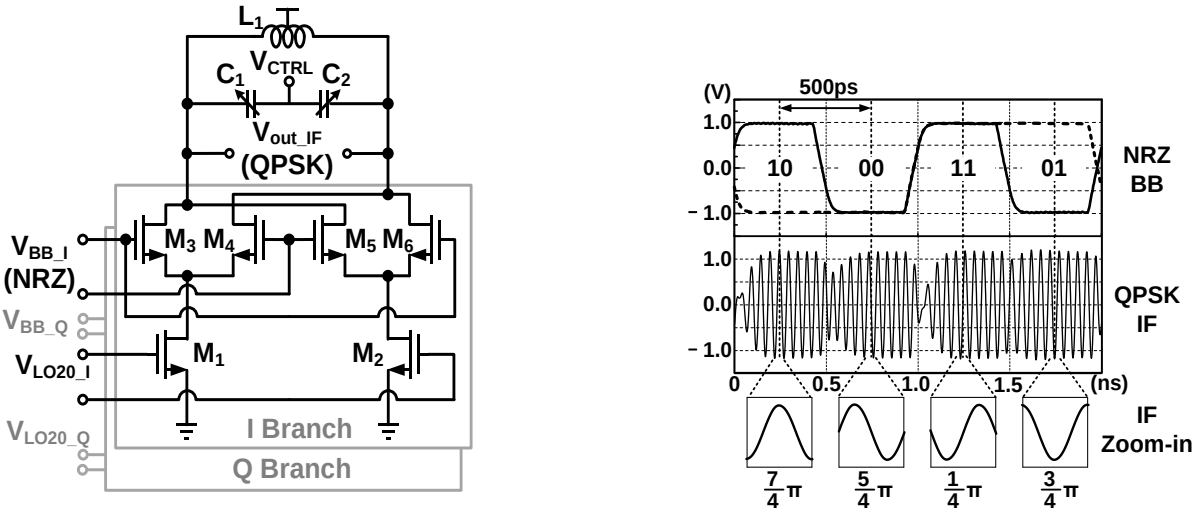
(b)

Fig. 3.10 Schematic and simulated transient waveform of (a) a conventional DCVSL inverter and (b) a modified DCVSL inverter.

off M_{P1} and pull-down transition at *Vo*–. This effectively reduces the propagation delay and output waveform asymmetry. Simulated transient waveforms shows the τ_{HL} is improved from 46 ps to 12 ps while the τ_{LH} is improved from 32 ps to 16 ps. The transition asymmetry is also greatly reduced in the modified DCVSL.

3.4 60-GHz QPSK Modulator

3.4.1 IF NRZ-to-QPSK Modulator

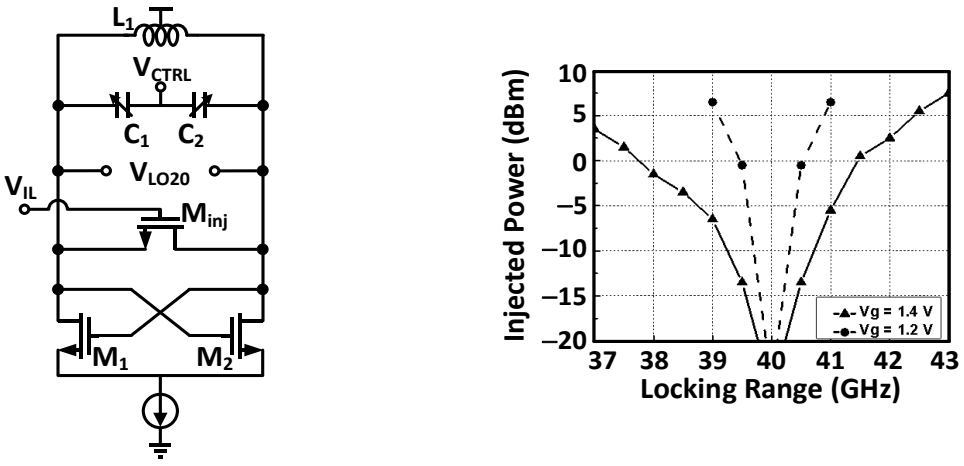


(a) (b)

Fig. 3.11 (a) Schematic of the IF NRZ-to-QPSK modulator and (b) its simulated output waveforms illustrating the four QPSK symbols.

Fig. 3.11 shows the schematic and simulated transient waveforms of the IF NRZ-to-QPSK Modulator. The large-swing NRZ baseband signals (1 V_{P-P}) from the DeMux are fed to the mixer quad-switches (M_3-M_6) while injecting the 20-GHz LO signals (0.5 V_{P-P}) as currents via the transconductance stage (M_1-M_2). As a result, both the mixer transconductance stage linearity and the frequency divider output swing requirement are relaxed and hence lower their power consumption. Simulated transient waveforms in Fig. 3.11(b) demonstrate the modulation of four NRZ symbols to quadrature signal at 20 GHz. The IF modulator provides 6-dB voltage gain while consuming 11 mW.

3.4.2 Injection-Locked Frequency Divider



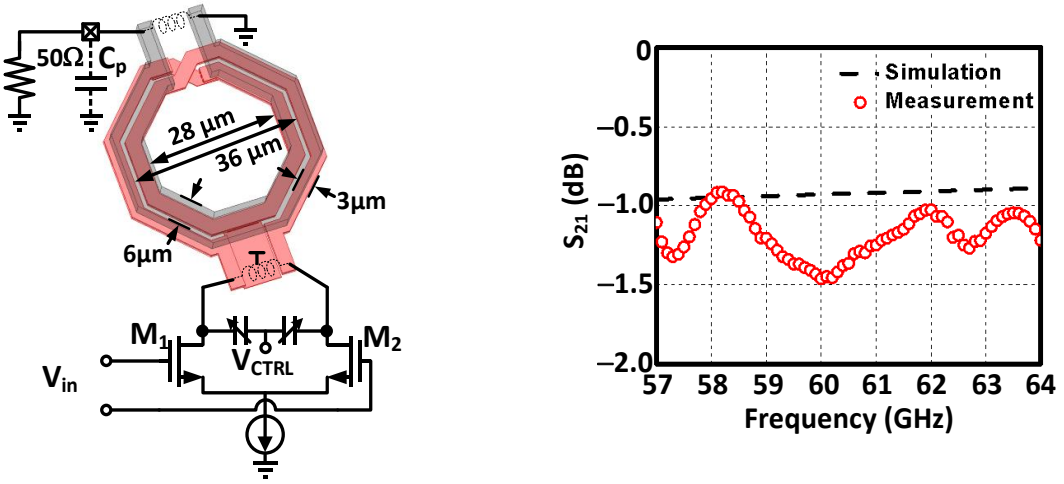
(a) (b)

Fig. 3.12 (a) Schematic of the ILFD and (b) measured locking range.

Fig. 3.12(a) shows the injection-locked frequency divider (ILFD) used to generate the 20-GHz LO for the IF modulator. Even though a static divider based on current mode logic (CML) can achieve very wide locking range and robust operation, it consumes considerable power when operated at 20 GHz. On the other hand, the LC-oscillator based injection-locked divider is more suitable for high frequency applications since its operation frequency is mainly determined by the resonance frequency of the LC-tank. However, the locking range of the ILFD is usually much narrower compared to other static dividers due to the resonance nature of the LC-tank. In order to alleviate this issue, an ILFD with direct injection technique [33] is adopted in this design to guarantee sufficient locking range. The ILFD can be treated as a traditional LC-oscillator with an additional injection device M_{inj}. This injection device performs as a mixer that mixes the incoming 40-GHz LO with the LC-VCO's output and injects the mixed current into the LC-tank. The size and bias of M_{inj} are designed to ensure the ILFD working in between the phase-limited and the gain-limited regions to maximize its locking range [33]. The measured locking range is shown in Fig. 3.12(b). When M_{inj} is biased at the optimum DC point (V_g=1.4 V), the locking range at 0-dBm

input power is extended by 3.5 times.

3.4.3 Output Buffer and Matching Network



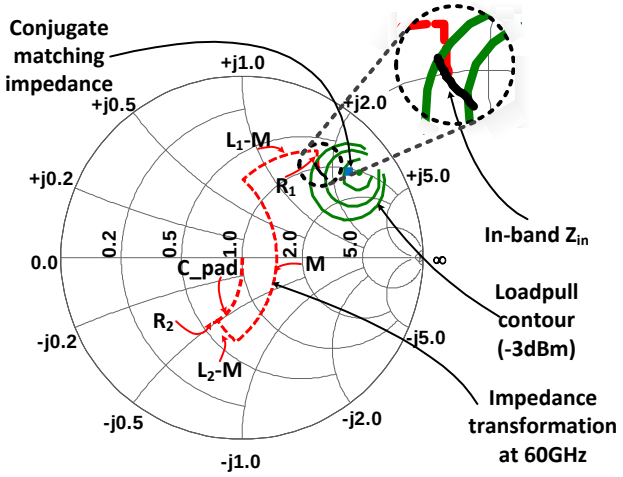
(a) (b)

Fig. 3.13 (a) Schematic of the output buffer with balun layout and (b) measured balun insertion loss.

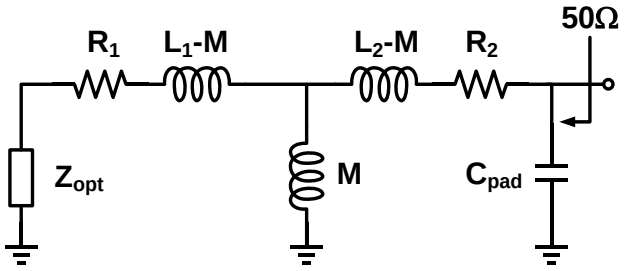
The output buffer for interfacing on-chip environment with off-chip PA 50-Ω loading is shown in Fig. 3.13 [34]. A balun based impedance matching network is adopted in the output buffer to perform impedance matching and differential to single-ended conversion for driving the off-chip PA. Compared to a transmission line matching network, the balun based matching method is more area efficient. The RF buffer provides 1-dB voltage gain with 7-GHz bandwidth centered at 60 GHz while consuming 11 mW. As shown in Fig. 3.13(b), the balun insertion loss is measured to be less than 1.5 dB over 57 to 64 GHz.

Fig. 3.14 shows the matching network rotational path and the simplified equivalent circuit schematic. The balun is required to match an off-chip 50-Ω loading to an optimum impedance (Z_{in_opt}) for the RF mixer. The Z_{in_opt} is determined from the trade-off between the conjugate matching impedance (Z_{conj}) for maximum power transfer and the maximum output power

impedance (Z_{max}). A set of load-pull contours (green circles) shown in Fig. 3.14(a) is used to determine Z_{max}. The Z_{in_opt} = (52.9 + j85.8) Ω is chosen to be within the –3-dBm load-pull contour



(a)



(b)

Fig. 3.14 (a) Matching network rotational path and (b) balun based matching network equivalent circuit.

while close to conjugate matching point to favorite power transfer. With the target input and output impedance, a transformer based matching network is designed to perform the impedance transformation as illustrated by the rotational path in the Smith chart. The component values to accomplish the impedance matching are: primary inductance L_1 = 217 pH, secondary inductance L_2 = 56 pH, parasitic resistance R_1 = 10 Ω and R_2 = 1 Ω and balun mutual inductance M = 87 pH. The black solid line in the Smith chart shows the input impedance variation from 56 GHz to 64 GHz. The balun input impedance falls within the –3-dBm load-pull contour over the desired frequency range.

3.4.4 Physical Implementation

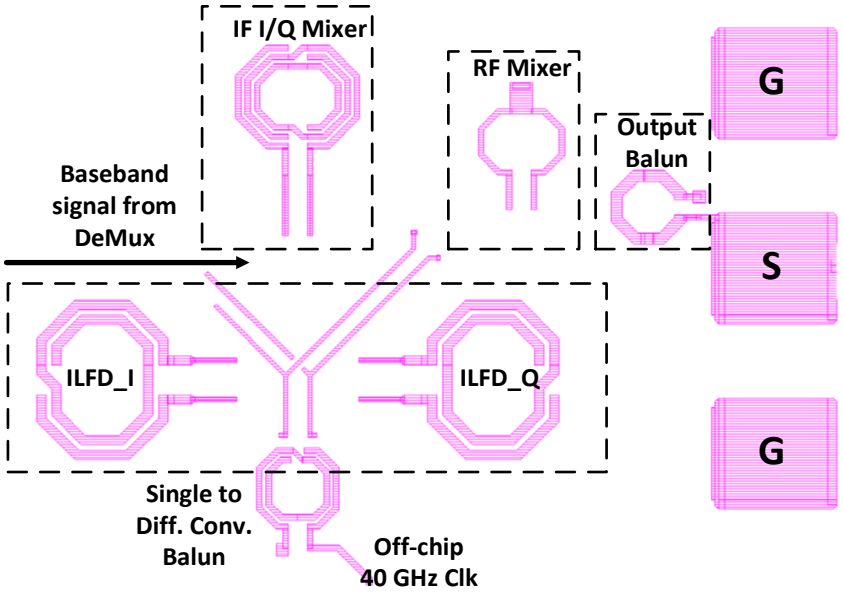
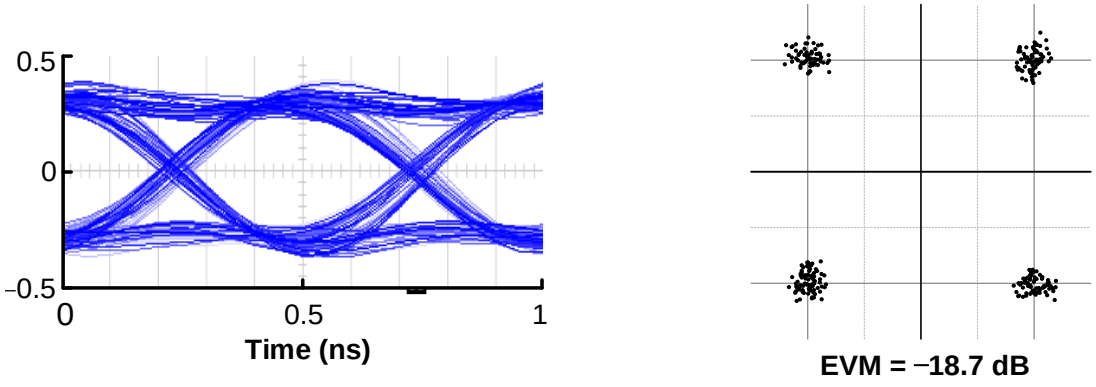


Fig. 3.15 RF link layout floorplan.

The physical design of the modulator is not trivial due to the severe crosstalk, attenuation and refection issues appeal at mmW band. Even worse, multiple high frequency I/Os must be handled to facilitate the test chip characterization. The RF link layout floorplan is depicted in Fig. 3.15 with the top metal layer shown only. The floorplan is designed with priority listed as follow: (1) high frequency RF modulated signals (2) NRZ baseband signal and (3) high frequency LOs. To facilitate delivering the 60-GHz modulated output signals, the output buffer and 60-GHz RF mixer are placed at the right hand side of the floorplan which is also the edge of the test chip. Then, the 20-GHz IF mixer is located next to the RF mixer to minimize the signal integrity issues arose form long routing trace. Next, the baseband signal from DeMux is fed to the RF up-conversion chain from the left hand side of the floor plan as the most natural way since the optical Rx is placed on the left half of the test chip. Finally, the ILFD is placed below the signal path with the LO signals go from bottom to top, which is perpendicular to the signal path direction to minimize crosstalk issues. The off-chip 40-GHz clock is fed into an on-chip balun for generating differential injection

sources from the bottom of the test chip. The divided 20-GHz outputs go through a ‘Y’ shape path to provide the LO signal for the QPSK modulator. The ‘Y’ shape path is carefully designed as part of the on-chip balun to minimize differential phase mismatch. And the left branch of the ‘Y’ shape path is only used as dummy for better layout symmetry.

The constellation and eye diagram from post-layout simulation is shown in Fig. 3.16 to verify the performance degradation due to layout mismatch and crosstalk. It can be seen that the layout introduced I/Q channel imbalance has little impact on the system performance.



(a) (b)

Fig. 3.16 (a) Simulated 4-Gb/s demodulated eye diagram and (b) constellation diagram.

3.5 Modulator System Experimental Results

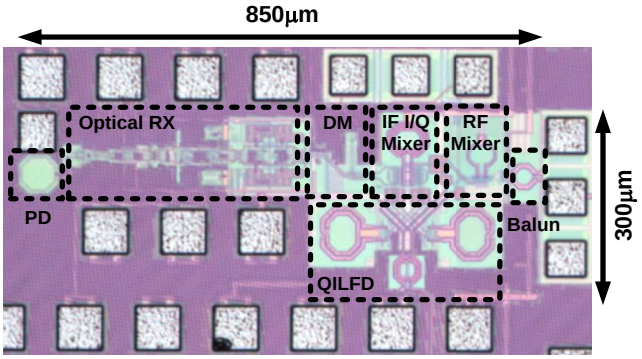


Fig. 3.17 Fiber-wireless modulator chip micrograph.

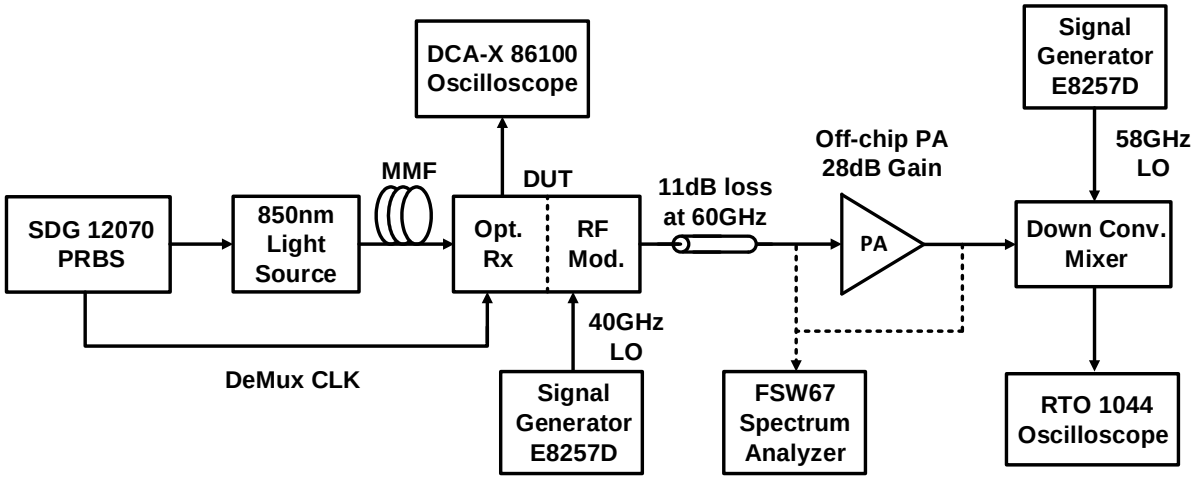


Fig. 3.18 Fiber-wireless modulator measurement setup.

Fig. 3.17 shows the micrograph of the SoC with an active area of 0.19 mm^2. The measurement setup is shown in Fig. 3.18. An 850-nm wavelength Mach-Zehnder Modulator generates the optical signal for the modulator. The optical input is top-illuminated on the on-chip PD through a multi-mode fiber. The half-rate 2-GHz synchronous clock for the DeMux is provided by the PRBS generator clock output. In a complete system, a CDR circuit would be required to extract the sampling clock signal from the incoming data. The design of such a CDR block will be described in the next chapter. The optical receiver is first characterized by direct RF probing at its output. A network analyzer is used to measure its frequency response while the eye diagram is captured by a

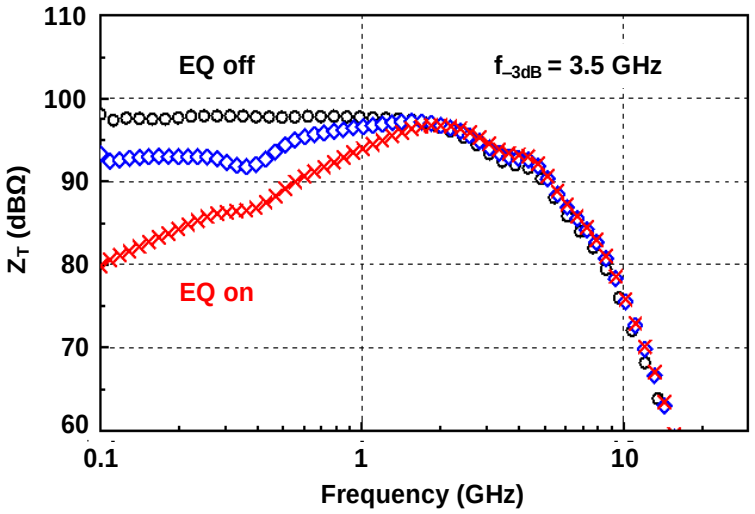
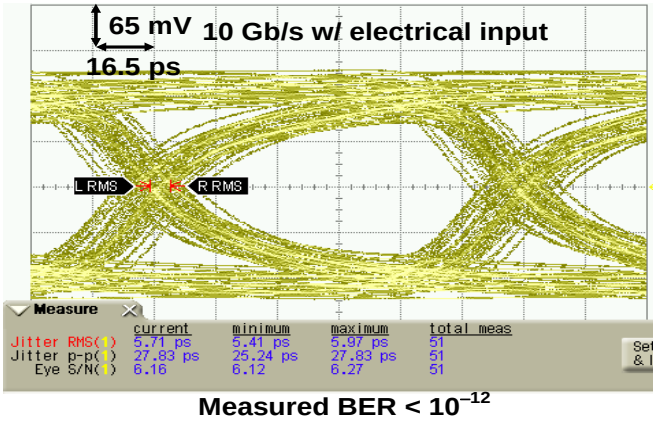


Fig. 3.19 Measured optical receiver frequency response

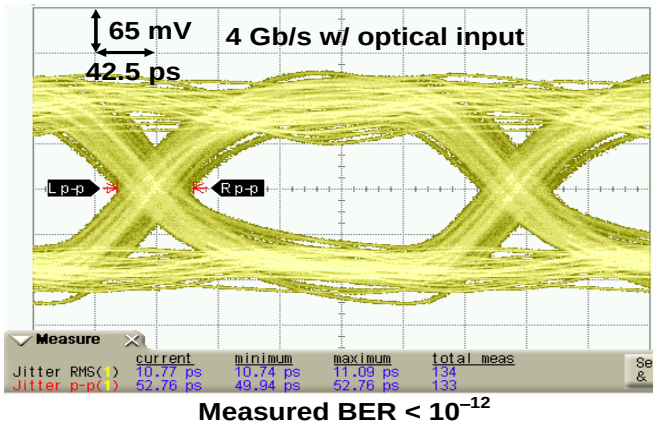
high-speed oscilloscope. Then the whole modulator is measured by a spectrum analyzer in the frequency domain. Limited by the testing equipment, the 60-GHz output is down-converted to a 2-GHz IF using an off-chip mixer and then sampled by a 20-GS/s, 4-GHz bandwidth real-time oscilloscope to examine the demodulated I/Q signals. A 28-dB gain off-chip power amplifier (PA) is used to compensate the cable and mixer loss during the down-conversion.

The frequency response of the optical Rx is shown in Fig. 3.19. A transimpedance gain of 98 dBΩ with a 18-dB equalizer tuning range is obtained. Fig. 3.20(a) depicts the 10-Gb/s Rx output eye diagram under 100-mA_{p-p} input. The Rx bandwidth is greatly extended due to the lack of on-chip PD capacitor loading in this case, which achieves 10 Gb/s operation when the equalizer is enabled. The RMS and P-P jitter are 5.7 ps and 27.8 ps, respectively. The optical Rx output eye diagram measured with an 850-nm light at the optical input sensitivity level of −3 dBm at 4 Gb/s is shown in Fig. 3.20(b). The RMS and P-P jitter are 10.8 ps and 52.8 ps, respectively.

The CW measurement without off-chip PA is conducted to evaluate the modulator output power. As shown in Fig. 3.21(a), a −18.2-dBm output power is measured including 11-dB cable loss, revealing that the modulator delivers −7.2-dBm output power. The modulated QPSK output



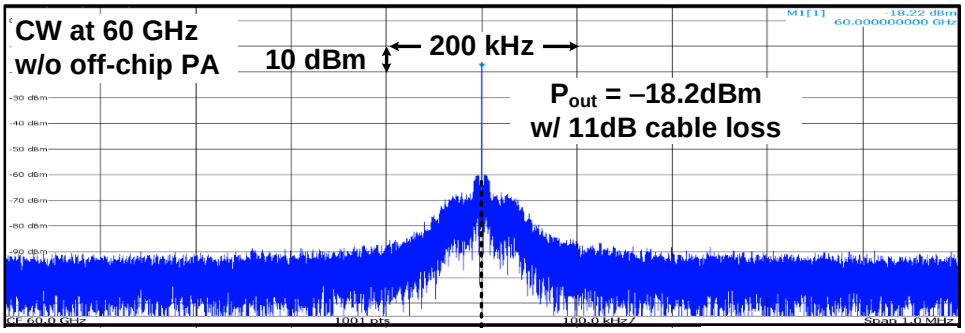
(a)



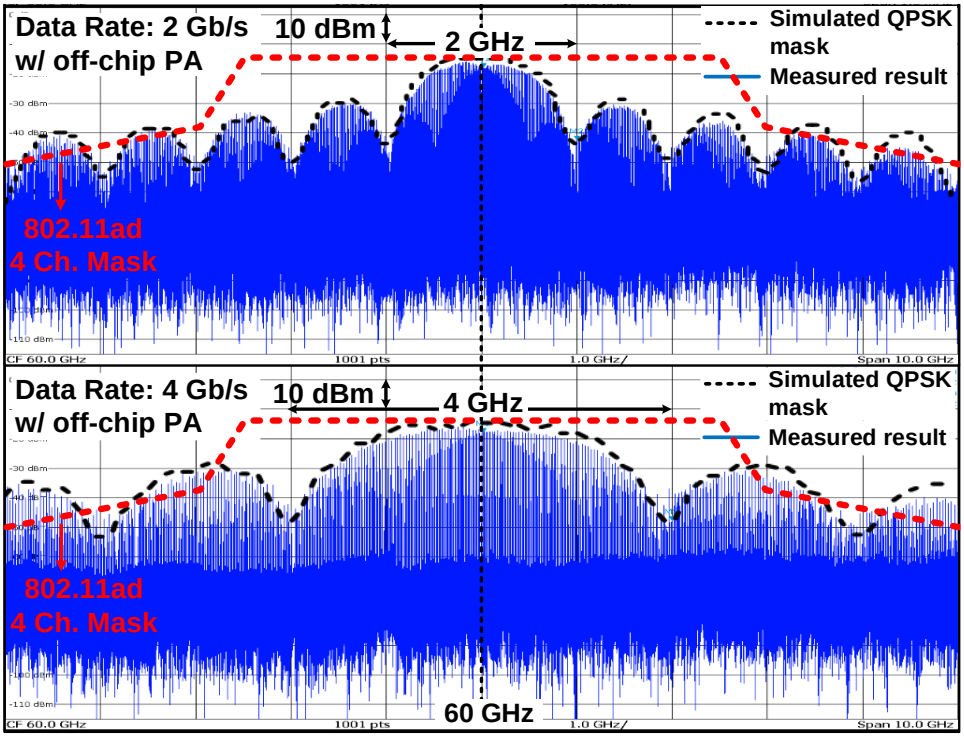
(b)

Fig. 3.20 (a) 10-Gb/s output eye diagram with electrical input and (b) 4-Gb/s output eye diagram under 850-nm optical input.

spectrum is measured with an off-chip PA. Fig. 3.21(b) shows the measured 2-Gb/s and 4-Gb/s QPSK output spectrum overlaid with a simulated mask at 60-GHz. In order to achieve high data rate, the modulator occupies all four channels of IEEE 802.11ad standard. The bandwidth of resonance tanks is intentionally designed to serve as a RF band-pass filter to reject the undesired sideband. The excessive side-band shown in Fig. 3.21(b) is mostly due to the deviation of LC-tank quality factor.



(a)



(b)

Fig. 3.21 Measured output spectrum at 60 GHz of (a) CW output and (b) modulated 4-Gb/s QPSK signal.

Fig. 3.22 shows the measured data eye and QPSK constellation diagram reconstructed using Matlab. The measured EVM and RMS jitter are –14 dB and 42 ps for 2 Gb/s and –12 dB and 24 ps for 4 Gb/s, respectively. The degradation of the demodulated eye and EVM at 4 Gb/s is partially due to the lack of RF filtering in the measurement setup, which results in spectrum contamination for a high data rate signals during down-conversion to 2 GHz.

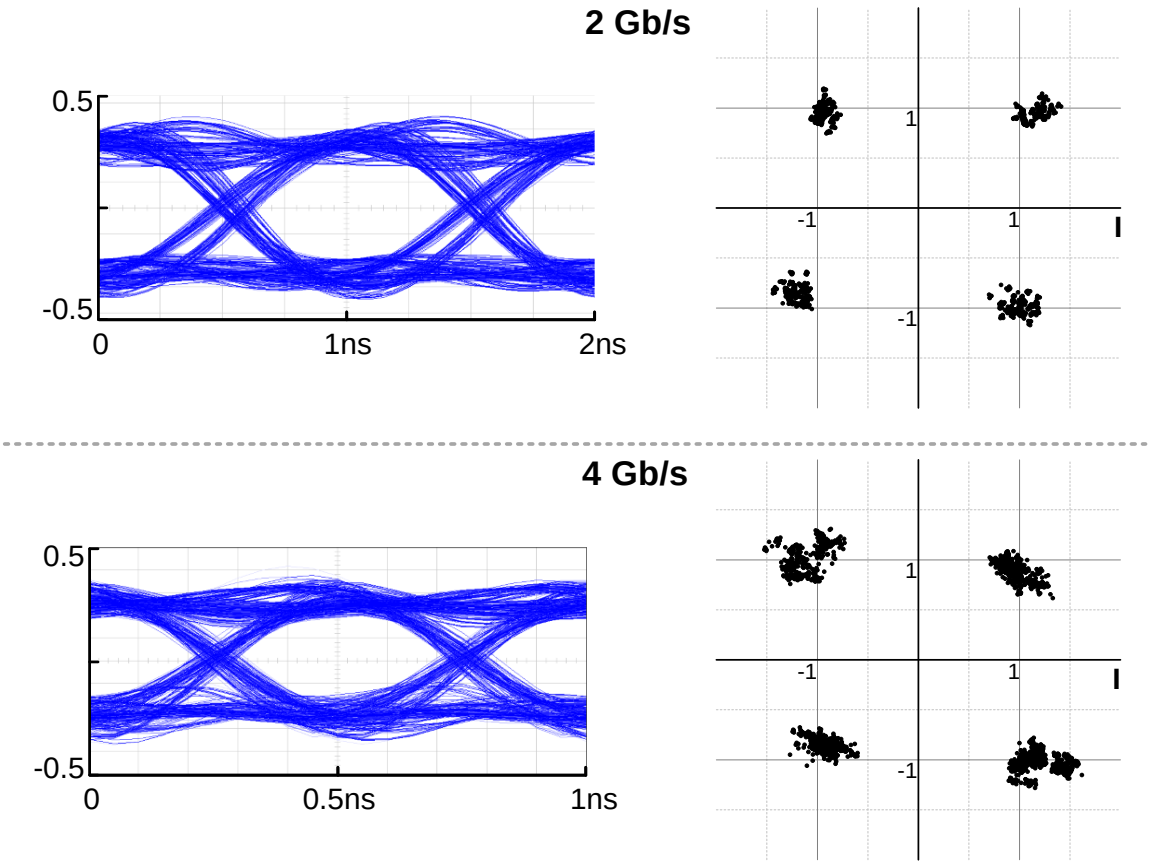


Fig. 3.22 Measured demodulated eye diagrams and constellation diagram.

The performance of the proposed SoC is summarized in Table VI. The optical Rx compensated by a two-stage EQ achieves 4-Gb/s O/E conversion with an on-chip PD having only 0.5-GHz bandwidth. The RF modulator up-converts the received 4 Gb/s baseband to 60 GHz in QPSK modulation scheme. The optical Rx and 60GHz modulator attain an efficiency of 8.8 pJ/b and 10.8 pJ/b while consuming 35 mW and 43 mW from a 1-V supply, respectively. Compared to fully-integrated optical Rx in [35], this work achieves better energy efficiency with much less chip area. The 60-GHz modulator is also optimized for power efficiency and small chip area.

Table VI: Fiber-Wireless Modulator Performance Comparison.

		[35]	[36]	[37]	**This Work**
Optical Receiver	Technology	65-nm CMOS	40-nm CMOS	65-nm CMOS	**65-nm CMOS**
	PD Bias (V)	0.3	-	-	**0.5**
	PD Resp. (mA/W)	360	-	-	**51**
	PD BW (GHz)	0.06	-	-	**0.5**
	Opt. Gain (dBΩ)	78.5	-	-	**98**
	Opt. DR (Gb/s)	3.125	-	-	**4**
	Opt. Sens. (dBm)	3.8	-	-	**–3**
	Area (mm^2)	0.27	-	-	**0.06**
	Eff. (pJ/b)	16	-	-	**8.8**
	Pwr (mW)	50	-	-	**35**
60GHz QPSK Modulator	Mod. Scheme	-	QPSK	QPSK	**QPSK**
	RF EVM (dB)	-	–13	–22	**–12**
	RF DR (Gb/s)	-	4.6	2.5	**4**
	Integrated PA	-	Yes	Yes	**No**
	Output Pwr (dBm)	-	–13	0	**–7.2**
	Area (mm^2)	-	N/A	0.8*	**0.13**
	Eff. (pJ/b)	-	Mod.: 20.1	Mod.+PA: 138.8	**Mod.: 10.8**
	Pwr (mW)	-	Mod.: 93	Mod.+PA: 347	**Mod.: 43**

* Estimated from die photo.

Chapter 4 Clock and Data Recovery with Embedded Equalization

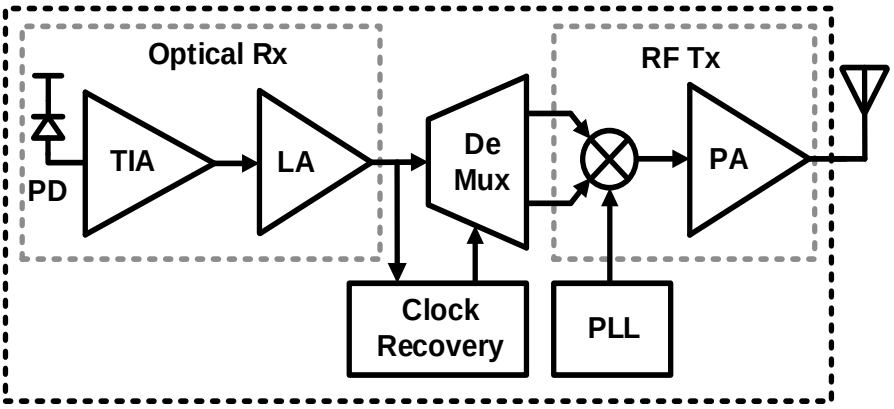


Fig. 4.1 CDR in a fiber-wireless communication system.

The function of a CDR is to extract the timing information and regenerate a clean output data from the jittery input. For a fiber-wireless communication system as shown in Fig. 4.1, a CDR senses the data at the output of the limiting amplifier and provides a phase adjusted clock for the de-multiplexer. This chapter discusses the design and experimental results of a 30-Gb/s CDR with embedded FFE and DFE equalization to compensate the insufficient optical front-end bandwidth or the potential channel loss. The proposed sub-sampling phase detection scheme allows a power-efficient linear operation at quarter-rate. The sampling phase detector is further extended to incorporate the build-in FEE and DFE with low hardware and power overhead. Measured with a low-loss input channel, the CDR achieves BER < 10^{-12} with an energy efficiency of 0.27 pJ/bit at 30 Gb/s. Measured with a high-loss input channel, the BER is improved from 10^{-3} to 10^{-12} at 26 Gb/s when the equalization is enabled.

4.1 Background of CDR

4.1.1 CDR Phase Detection

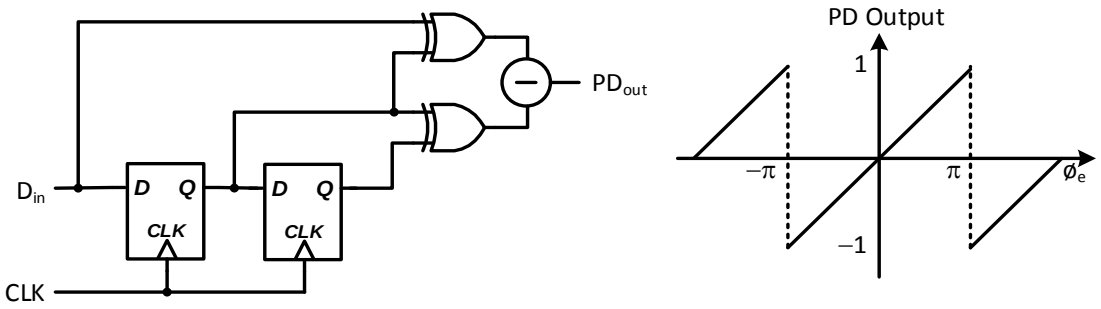


Fig. 4.2 Linear Hodge phase detector.

The CDR phase detector (PD) compares edge transitions of the incoming data with the recovered clock and generates an output indicating the phase difference between them. The PDs can be categorized as linear PD (e.g. Hodge PD [38]) or binary PD (e.g. Alexander or bang-bang PD [39]). As shown in Fig. 4.2, the output of a linear PD is linearly proportional to the phase difference between clock and data within $\pm\pi$ range. Due to its linear characteristic, the CDR loop with a linear PD can be analyzed and designed with the traditional linear feedback theory, which eases the design and makes it appealing to certain applications that is sensitive to jitter peaking like SONET [40]. However, several potential issues limit its usage in high-speed links: (1) The linear PD represents the phase difference by the output pulse width. However, it is difficult to accurately generate narrow pulses when the unit interval is already less than 40 ps in 100GbE systems. (2) The conventional Hodge PD is not compatible with quarter-rate operation, which further prohibits its usage in high-speed systems. Other issues like sampling clock delay and data pattern dependency further complicate the design. [41].

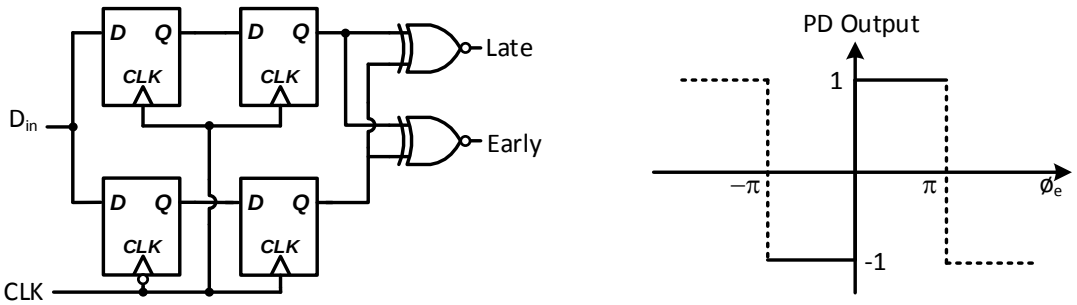


Fig. 4.3 Non-linear Alexander phase detector.

On the other hand, the binary PD is more suitable for high data rate applications since it simply produces a binary output to indicate the early or late phase relationship between the incoming data and the recovered clock as shown in Fig. 4.3. The long-term average of this binary output approaches zero mean when the loop is locked. A third state "idle" can be added to reduce the disturbance when no edge transition is detected. However, a large steady-state jitter is still expected because the PD output bounces between high and low states even in the locked state. Also, the input jitter dependency of the PD gain makes the loop design difficult [42]. Even with above mentioned drawbacks, the BBPD is getting more and more popular in modern high-speed data communication systems due to following advantages: (1) The binary operation of BBPD relaxes the requirement of latches since generating narrow pulses is not required as in the linear PD. (2) The BBPD can be easily modified to incorporate half and quarter-rate (or even more sub-rates) operations to extend its operation range [43], [44]. (3) The binary output makes a binary PD naturally suitable for digital loop filter [45], [46].

4.1.2 CDR Architectures

A. PLL-based CDR

Fig. 4.4 shows a PLL-based CDR with a reference clock. Similar to a conventional PLL, the PLL-based CDR adjusts the phase of the sampling clock by tuning its VCO frequency. Due to the limited locking range of the phase loop, an auxiliary frequency loop is usually required to course

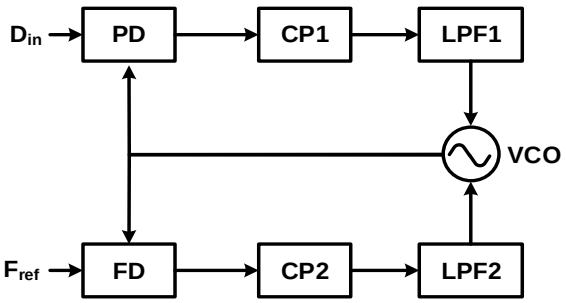


Fig. 4.4 Block diagram of PLL-based CDR.

tune the VCO and extend the locking range. A lock detector is usually used to switch the control voltage between the frequency and the phase lock loops to avoid pulling the VCO. Drawbacks of a PLL-based CDR shown in Fig. 4.4 are: (1) Dual loop filters and a specific VCO for each lane take large silicon area and power consumption and (2) Potential frequency pulling between the frequency and the phase loops [47].

B. DLL/PI-based CDR

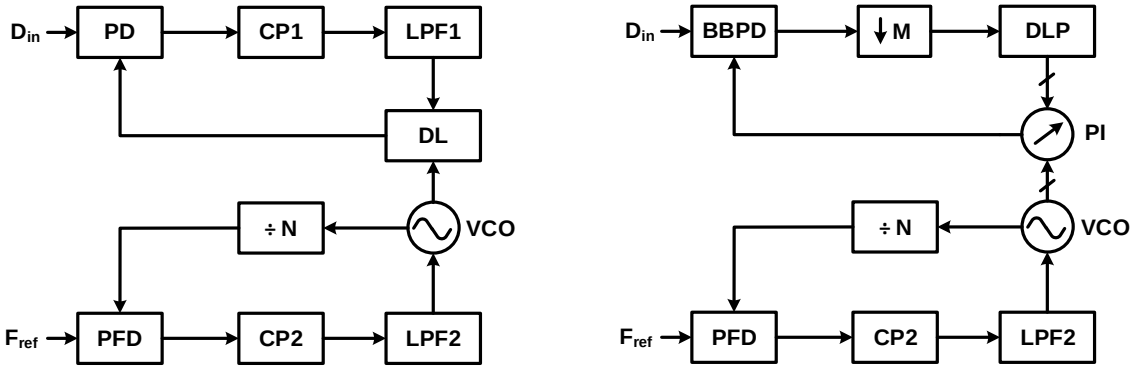


Fig. 4.5 Block diagram of DLL/PI-based CDR.

A DLL/PI-based CDR shown in Fig. 4.5 contains a stand-alone frequency loop to generate the sampling clock and a delay line or phase interpolator (PI) to finely adjust the clock phase. Compared to the PLL-based CDR, the frequency and the phase loops in the DLL/PI-based CDR are not correlated and thus can be optimized independently. Also, the frequency loop can be shared

by multiple lanes to save chip area and power. In addition, the first order phase loop in a DLL/PI-based CDR does not have jitter accumulation and jitter peaking issues as the PLL-based CDR.

The main challenge associated with a DLL-based CDR is its finite phase tuning range, which constrains its use in asynchronous clocking systems. To resolve this issue, a PI is proposed as the phase adjustment block in a PI-based CDR [48]. The PI can be considered as a special type of delay line that can achieve 360 °phase rotation by mixing quadrature input clocks. The PI output phase is given by:

$$Y_{out} = Asin(\omega t - \theta) = \cos(\theta)X_I + \sin(\theta)X_Q, \quad (4\text{-}1)$$

where $X_I = \sin(\omega t)\,,\ X_Q = \cos(\omega t).$

A 360 °phase rotated clock can be synthesized by controlling the θ in Eq. (4-1). Nevertheless, it is difficult to realize a PI with a high linearity because the cosine and sine terms in Eq. (4-1) are hard to generate in transistor level implementations. The resulted PI DNL deteriorates peak-to-peak jitter of the sampling clock and recovered data when tracking a frequency offset [48].

4.1.3 CDR Phase Domain Model

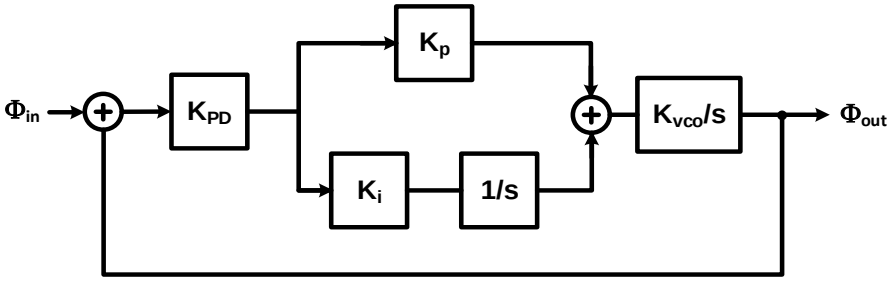


Fig. 4.6 CDR phase domain model.

Fig. 4.6 shows the phase domain linear model of a PLL-based CDR. The model of a PI-based CDR is similar to the PLL-based one except that the VCO gain (K_{vco}) is replaced by a PI gain (K_{PI}) and the phase integration feature of VCO is artificially implemented with an integrator. Compared

to a conventional PLL, the CDR has no feedback frequency divider in the loop, which makes the PD operates at high speed. Three most important loop properties are described below.

A. Jitter Transfer

The jitter transfer describes how much incoming data jitter (θ_{in}) is transferred to the retimed data (θ_{out}). It is derived as

$$\frac{\theta_{out}}{\theta_{in}} = \frac{sK_{PD}K_pK_{VCO} + K_{PD}K_iK_{VCO}}{s^2 + sK_{PD}K_pK_{VCO} + K_{PD}K_iK_{VCO}}, \quad (4\text{-}2)$$

where $K_p = I_{cp}R$ is the proportional gain and $K_i = \frac{I_{cp}}{C}$ is the integration gain determined by the capacitor and resistor in the loop filter. Due to the second order loop response, a peaking is inevitable in the jitter transfer, which could be a severe issue in the data repeater application where multiple CDRs are cascaded in series in a long transmission link. The jitter transfer has a low pass response to track the low frequency jitter while rejecting high frequency jitter.

B. Jitter Generation

The jitter generation characterizes the amount of jitter generated by the CDR itself when negligible jitter is present on the input data ($\theta_{in} = 0$). The CDR generated jitter is usually dominated by the noise of the VCO or PI. Therefore, the transfer function of the jitter generation can be simplified to the transfer function from the VCO/PI noise to the CDR output, which is a high pass response with its corner frequency governed by the CDR loop bandwidth. Therefore, we observe a trade-off between the jitter transfer and the jitter generation in a PLL-based CDR loop.

C. Jitter Tolerance

The jitter tolerance specifies the maximum peak-to-peak jitter amplitude that the CDR can tolerate while maintaining a certain BER. The jitter tolerance is usually regulated by

communication standards and described as a mask of the input jitter amplitude versus the jitter frequency as shown in Fig. 4.7. It consists of two regions: (1) Low frequency in-band jitter: The CDR is designed to track jitter components within this region without BER degradation. (2) High frequency out-of-band jitter: The jitter in this region is beyond the CDR loop bandwidth and thus unable to be tracked, resulting in a BER degradation.

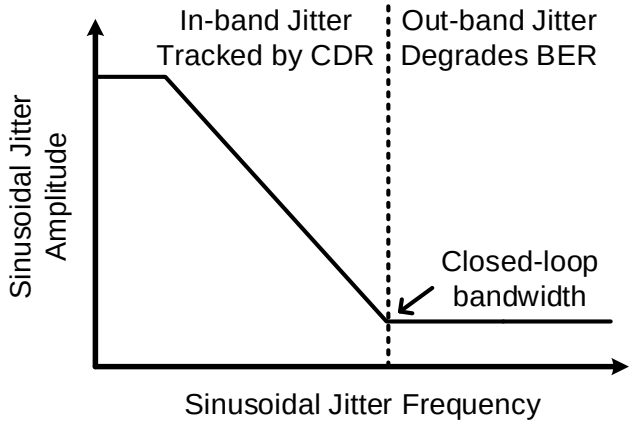
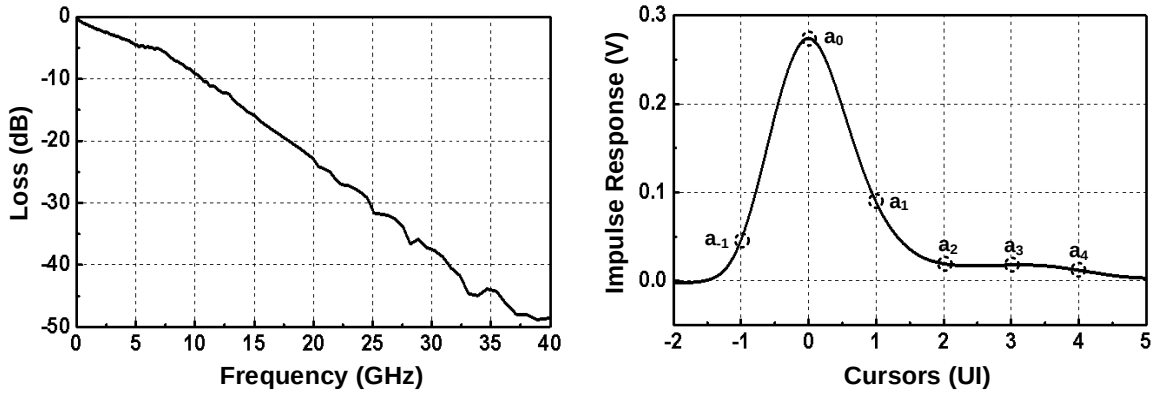


Fig. 4.7 CDR jitter tolerance mask.

4.2 Background of Discrete-Time Equalization



(a) (b)

Fig. 4.8 A lossy channel example: (a) measured channel insertion loss and (b) simulated impulse response based on the measured s-parameter.

The measured frequency response of a lossy channel is shown in Fig. 4.8(a). For a 25 Gb/s data input, this channel introduces 14-dB loss at Nyquist frequency (12.5 GHz), which results in severe amplitude and timing distortions. Fig. 4.8(b) presents the impulse response of the example channel. The pre-cursors and post-cursors of the impulse response equivalently represents the frequency domain loss in the time domain. The pre-cursors and post-cursors lead to significant ISI issue since the amplitude of the current bit is the accumulation of the main cursor of the current bit and all post-cursors of preceding bits and pre-cursors of succeeding bits.

To further boost transmission data rate and range, an equalizer is needed to compensate the channel loss in serial link communication systems. This section provides the background of two discrete-time equalizers as the foundation of the embedded equalization utilized in the proposed CDR.

4.2.2 Feed Forward Equalizer

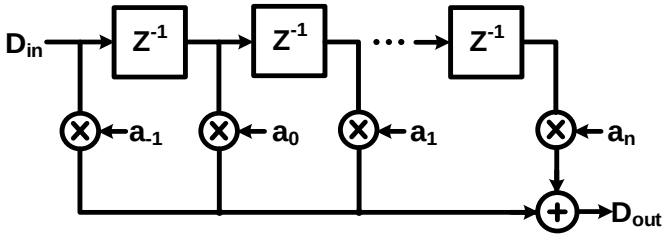


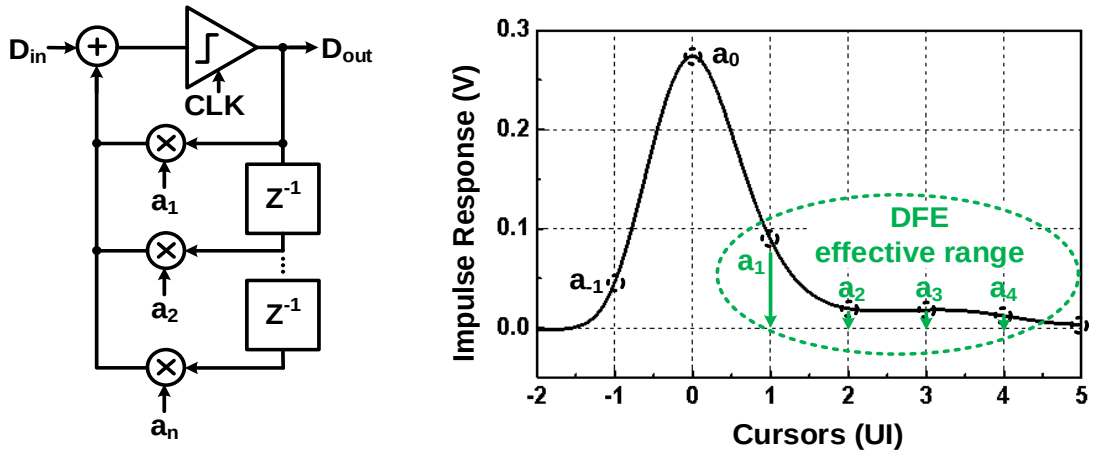
Fig. 4.9 Block diagram of feed forward equalizer.

The feed forward equalizer (FFE) as shown in Fig. 4.9 is a finite impulse response (FIR) linear filter used to flatten the channel response. In a FFE, the data propagates through delay stages, multiplies with tap coefficients and finally sums together to produce the equalized output. To reduce circuit implementation complexity, the delay in FFE is often chosen to be 1 or 0.5 UI [49]. Since the current and delayed input are linearly weighted by tap coefficients, the FFE is a linear equalizer like a CTLE. Therefore, it also amplifies high frequency noise. A FFE can be implemented at either transmitter (Tx) or receiver (Rx) side due to the LTI property of the system. However, it is much more widely adopted at Tx side because of the convenience of generating the delayed input. At the Tx side, the FFE input is well timed digital bits which can be simply delayed by flip-flops. On the other hand, the input of a FFE at the Rx side is a distorted analog signal. Implementing precise delay for an analog signal over a wide frequency range is not a trivial task [50], [51]. Therefore, FFE is more popular at the Tx side. However, it is difficult to implement adaptation at the Tx side since it cannot sense the channel information. A back channel is required to achieve adaptive equalization in this case.

A FFE often contains pre-cursor, main cursor and post-cursor taps. The negative tap (a_{-1}) shown in Fig. 4.9 is called pre-cursor tap while the a_0 is called main cursor tap and $a_1 \sim a_n$ are post-cursor taps. The pre-cursor tap compensates the phase variation induced pre-cursor as shown in the

impulse response in Fig. 4.8. The post-cursor tap compensates the long tail resulted from the channel magnitude loss at high frequencies. Limited by the maximum output swing, the summation of tap coefficients of a FFE at the Tx side needs to be unity.

4.2.3 Decision Feedback Equalizer



(a) (b)

Fig. 4.10 (a) Block diagram of decision feedback equalizer and (b) DFE post-cursor cancellation.

The major issue of linear equalizers like CTLE and FFE is the amplification of high frequency noise and cross-talk. This problem limits their maximum achievable equalization gain in a heavily loss channel condition and necessitates other type of equalization technique. The decision feedback equalizer (DFE) is a non-linear equalizer that can distinguish between signals and noise and achieve more flexible equalization for complicated channel condition. The block diagram of a typical DFE is shown in Fig. 4.10. It contains a slicer to sample and regenerate the input data to full logic level, multiple stages of delay cells to store the history of the input data, coefficient taps to control the feedback strength and a summer to perform arithmetic summation. For DFE, the feedback taps emulate the post-cursors of each preceding bit and eliminate the ISI by canceling their impacts on the current bit as shown in Fig. 4.10(b). Since the ISI compensation is conducted after the logic

decision of the incoming bit is made, the DFE is a nonlinear equalizer and thus avoids high frequency noise amplification and

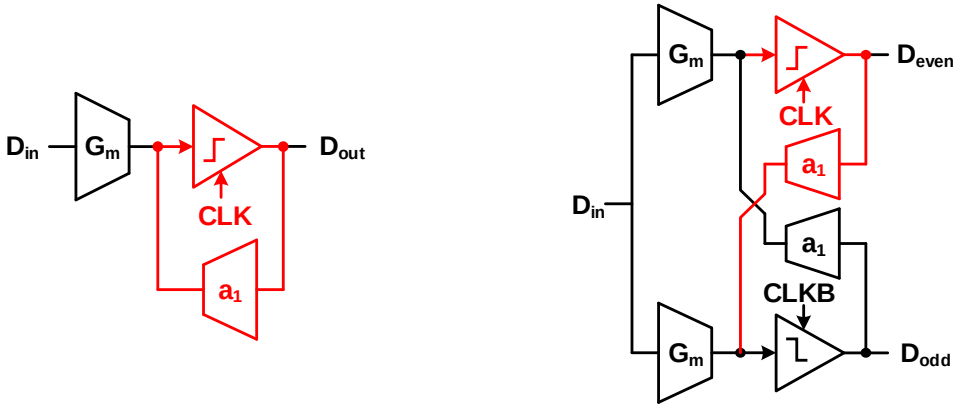


Fig. 4.11 1-tap full-rate and half-rate direct feedback DFE.

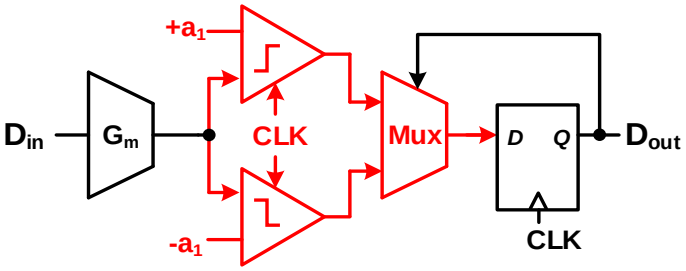


Fig. 4.12 1-tap loop-unrolling DFE.

cross-talk issues. One major limitation of DFE is that it can only compensate post-cursor ISI as shown in Fig. 4.10(b) since only the ISI information of current and past bits are known. Therefore, a transceiver dealing with severe channel loss usually requires both FFE, CTLE and DFE to achieve optimum equalization.

Moreover, the DFE feedback loop needs to settle before the sampling instant of the next bit. The most stringent timing requirement happens at the first tap feedback loop shown as the red path in Fig. 4.11 since the data detection, coefficient multiplication and summation have to be finished within 1 UI. The timing of the feedback loop is given by

$$T_{ckq} + T_{setup} + T_{settle} < 1UI \tag{4-3}$$

where T_{ckq} is the comparator clock to output delay, T_{setup} is the comparator setup time and T_{settle} is the feedback summing node settling time. For data rate over 25 Gb/s, closing the feedback loop within 40 ps becomes very expensive in terms of power consumption and chip area. Therefore, an advanced technique like loop-unrolling [52] as shown in Fig. 4.12 is widely adopted to relax the timing constrain. The timing of a loop-unrolling DFE first tap feedback loop is given by

$$T_{ckq} + T_{setup} + T_{mux} < 1UI \tag{4-4}$$

where T_{mux} is the multiplexer propagation delay. The loop-unrolled DFE pre-computes two feedback possibilities to relax feedback timing as long as $T_{mux} < T_{settle}$. However, the loop-unrolling is usually applied to the first tap only since the hardware overhead increases exponentially.

4.3 Proposed CDR with Embedded FFE and DFE

4.3.1 CDR System Overview

A. System Architecture

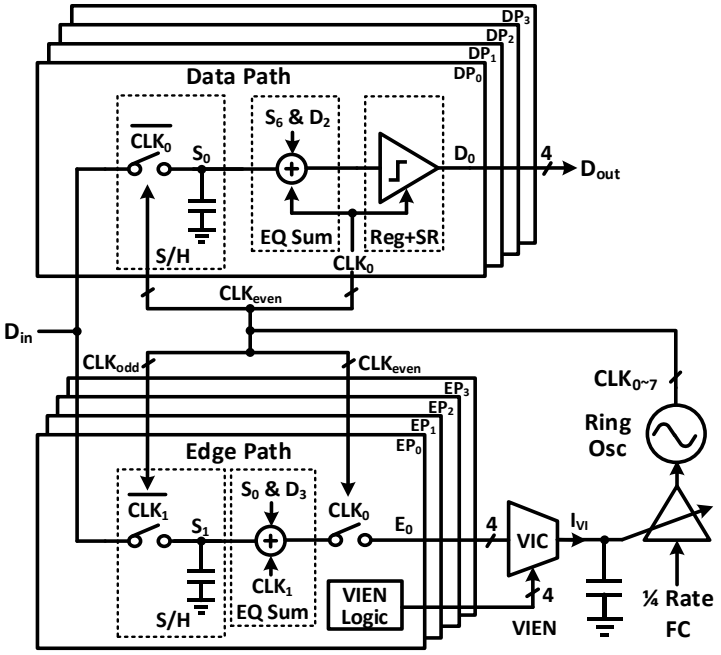


Fig. 4.13 CDR system block diagram.

Fig. 4.13 shows the block diagram of the proposed CDR architecture. The proposed CDR runs at quarter-rate to achieve high energy efficiency without using area consuming inductive peaking techniques. The incoming data is sampled and processed by four data paths and four edge paths to recover the amplitude and the timing information, respectively. The eight phases quarter-rate clock is generated by an injection-locked ring oscillator. A quarter-rate forwarded clock serves as the injection source for the ring oscillator. Under strong injection, the phase of the ring oscillator follows the phase of the injection source which is controlled by the edge paths and the delay line.

Each data path consists of a sample/hold (S/H) stage, a charge-steering EQ summer and a latch to regenerate the input data. The S/H samples and holds the input data for half clock period to allow stable EQ summation. As shown in Fig. 4.13, the FFE and DFE are performed by deducting the

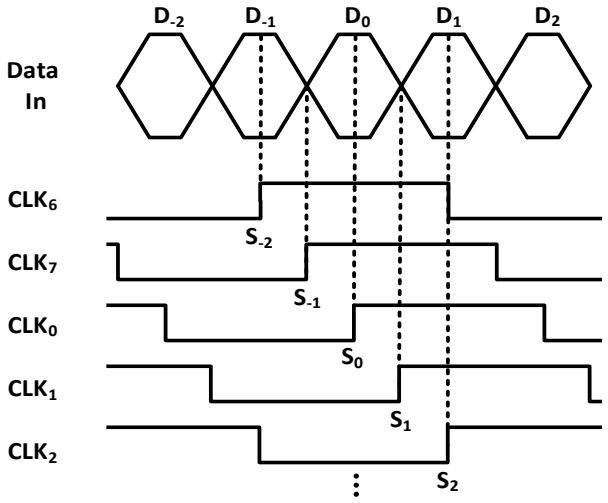


Fig. 4.14 CDR system timing diagram.

current sample (S_0) with the weighted preceding sample (S_{-1}) and the weighted digitized preceding bit (D_{-2}). The equalized data sample triggers the comparator regeneration pair to produce full swing output.

The edge path extracts timing information by detecting the crossing point of the input date as shown in Fig. 4.14. When the crossing point of the input data and the edge sampling clock phase are not aligned, the edge path senses a non-zero differential input voltage and produces a charge pump output current (I_{CP}) that is proportional to the phase deviation. The I_{CP} charges the capacitor in the loop filter and produces a control voltage to control the delay line.

B. Embedded Equalization

Fig. 4.15 shows a detail block diagram of the embedded FFE and DFE. The FFE is implemented by directly forwarding the previous analog sample to the summer of the current sample as indicated by the green path in Fig. 4.15. Meanwhile, the DFE is conducted by feeding back the regenerated preceding bit to cancel the second post-cursor at the decision instant of current bit as shown by the red path in Fig. 4.15. For example, the CKL_1 samples the input data and holds the sampled value S_1. The S_1 is forwarded to the next path to cancel the first post-cursor when the S_2 is sampled by

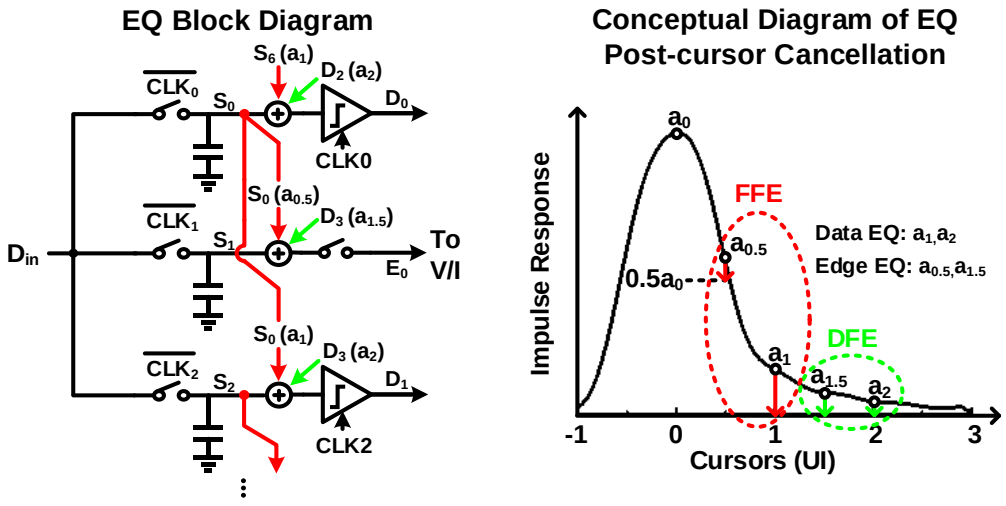
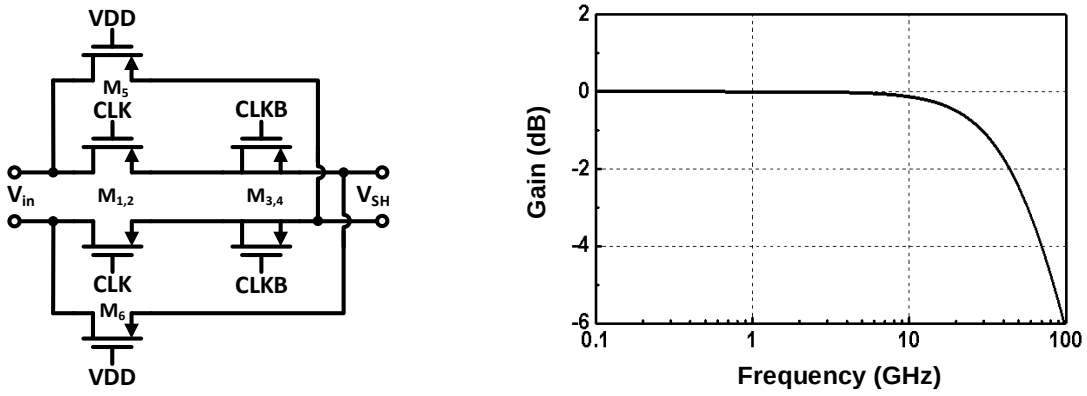


Fig. 4.15 Block diagram of the embedded FFE and DFE.

the *CLK*$_2$. Meanwhile, the regenerated data (*D*$_{-1}$) is fed back to the *CLK*$_2$ path to perform DFE for canceling the second post-cursor. In this way, the stringent feedback timing of the DFE first post-cursor feedback loop is avoided.

4.3.2 Data Path Implementation

A. Sampler



(a) (b)

Fig. 4.16 (a) Schematic of the sampler and (b) simulated frequency response.

Fig. 4.16 shows the schematic and the frequency response of the sampler. The sampler consists of a PMOS switch pair (*M*$_{1-2}$) and dummy transistors (*M*$_{3-6}$). Since the common-mode (CM) voltage

of the input data is set at 0.7 V, only PMOS transistors with size of 2μ/30n are adopted as sampler switches. The $M_{3\text{-}4}$ dummy transistors are sized to be half of the $M_{1\text{-}2}$ (1μ /30n) to compensate for the clock feedthrough. The dummy transistors $M_{5\text{-}6}$ are sized identical to the $M_{1\text{-}2}$ to eliminate the data feedthrough when the $M_{1\text{-}2}$ are off. The simulated post-layout frequency response of the sampler with a 5-fF loading capacitor is shown in Fig. 4.16(b). For a sub-rate system without non-overlapping clocking, multiple samplers would be switched on and load the input source at certain clock period. Therefore, the 3-dB bandwidth of each sampler is over-designed to be 58 GHz to ensure a short settling time and precise acquisition.

B. Charge Steering EQ Summer

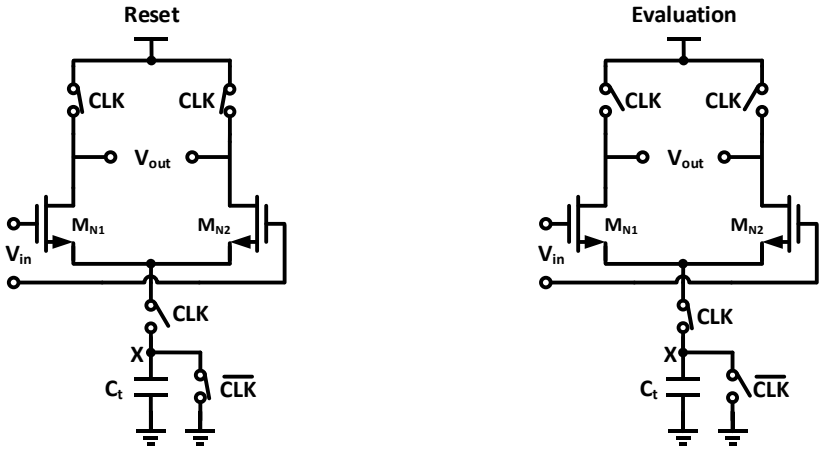


Fig. 4.17 Operation of the charge steering differential pair.

Fig. 4.17 shows the concept view of a charge-steering amplifier [53], [54] in reset and evaluation mode, respectively. The charge-steering amplifier is a dynamic circuit that requires a reset phase to pre-charge its output node to Vdd and an evaluation phase to generate a differential output. Compared to a conventional CML structure, the resistive load is replaced by a pair of PMOS switches. Also, the current tail in a conventional CML differential pair is replaced by a switched charge sink (C_t) to control the gain and the output CM level. The simulated transient waveforms of the charge-steering amplifier are shown in Fig. 4.18. In reset mode, the output is pre-charged to

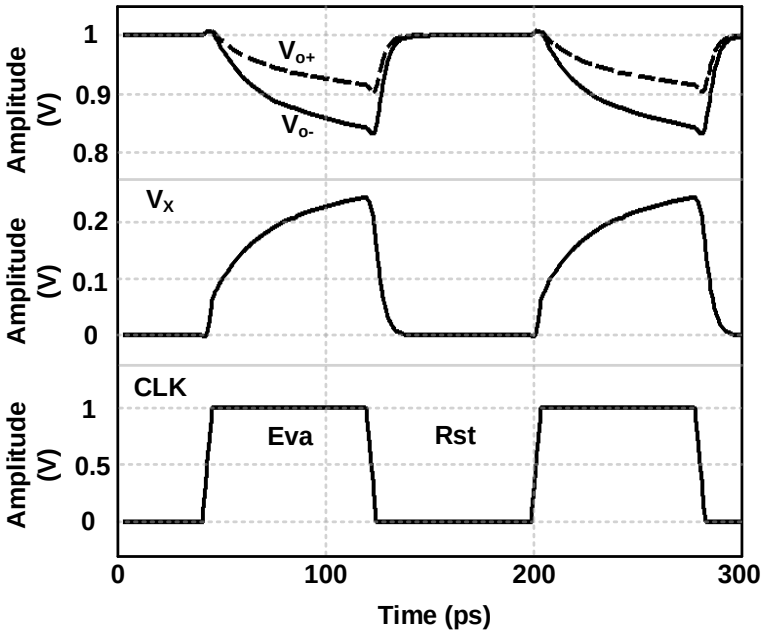


Fig. 4.18 Simulated transient waveforms of the charge steering amplifier.

Vdd and the C_t is discharged to ground. In evaluation mode, the charge at the output node is steered by the input differential pair to C_t, which builds up a non-zero voltage (V_x) at node X. The V_x eventually turns off the input differential pair and thus holds the output voltage. With a large C_t, V_x rises at a slower rate and gives output nodes more time to discharge and build up a larger voltage difference. However, an excessively large C_t may sink too much charge and collapse the output common-mode level, which demolishes the differential voltage gain. The first order approximation of the differential voltage gain with a small input signal and a properly designed capacitor ratio is given by [53]:

$$A_v \approx \frac{2C_t}{C_L}, \tag{4-5}$$

where C_L is the total capacitance at the output node and C_t is the total capacitance at the tail node.

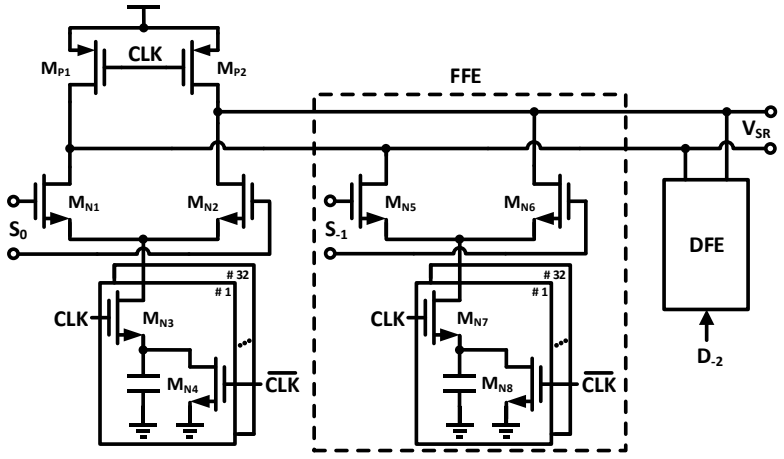


Fig. 4.19 Schematic of the charge-steering summer.

Compared to conventional CML differential pairs with resistive load, the charge-steering amplifier exhibits several advantages: (1) The bandwidth of output nodes is not limited by the RC time constant as in a conventional CML amplifier. (2) The charge-steering amplifier is more power efficient and scalable with the operation data rate since it only conducts dynamic power.

However, the dynamic operation brings several challenges to the design of charge-steering style circuits: (1) The gain and output CM level are sensitive to the ratio of the output parasitic capacitor to C_t. (2) It requires a full swing CMOS style clock to effectively control switches implemented by MOS transistors. (3) Charge-steering style circuits are sensitive to the CM noise and cross-talk from full swing clocks. The charge-steering differential pair is actually a pseudo differential circuit because the tail capacitor sink is a low impedance path for high frequency signals and has limited effect on degenerating CM noise. In addition, the output nodes are high impedance nodes which are not capable of regulating the output voltage under severe cross-talk or coupling. (4) The charge-steering amplifier produces a return-to-zero (RZ) output due to the need for resetting. This makes it difficult to cascade multiple charge-steering stages [55].

Even though the charge-steering architecture exhibits several design challenges as discussed above, it is adopted as the EQ summer in this design due to the unparalleled power efficiency. In

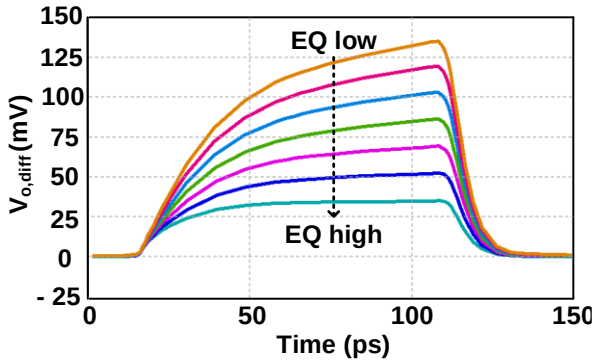


Fig. 4.20 Simulated transient waveforms of summer differential output under various EQ tap settings.

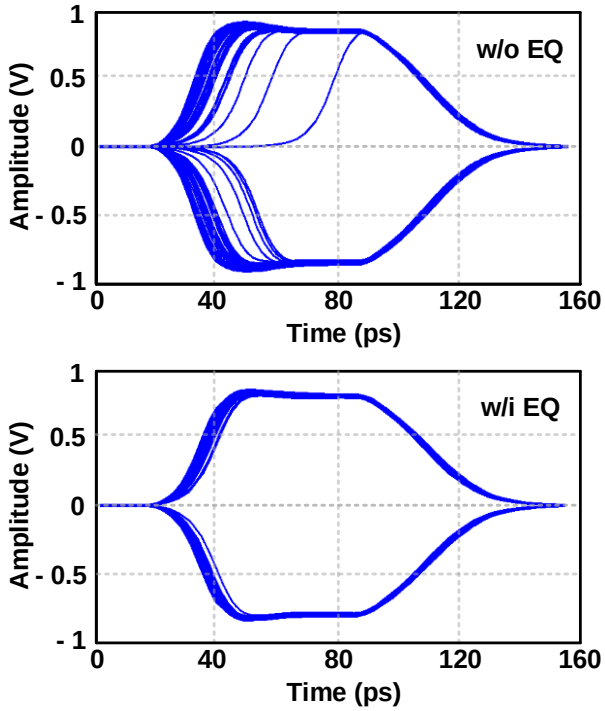


Fig. 4.21 Simulated NR eye diagrams at the summer output with EQ enabled and disabled.

the data path, a charge-steering differential pair with two feedback taps is utilized as the equalizer summer as shown in Fig. 4.19. The equalization feedback paths are implemented by auxiliary charge-steering differential pair branches with tunable tail capacitors. The feedback tap coefficients are adjusted by controlling the number of capacitor units connected to the tail node. The output of the charge-steering summer is directly connected to a CMOS regeneration cell which will be described in the next section. The drop of the summer output common-mode voltage is

compensated by the PMOS cross-coupled pair in the CMOS regeneration cell. Fig. 4.20 shows the summer differential output voltage under different EQ feedback tap settings. The differential output voltage linearly decreases with the increase of the EQ feedback strength, which verifies the function of charge-steering summer and the EQ feedback coefficient control.

Fig. 4.21 depicts simulated RZ eye diagrams at the summer output with severely distorted input. Due to the significant jitter and narrow eye opening of the input data, the summer output eye diagram suffers from considerable peak-to-peak jitter and metastability when the equalization is disabled. In contrast, the eye diagram with equalization enabled shows significant improvement on the horizontal eye opening.

C. Modified SR Latch

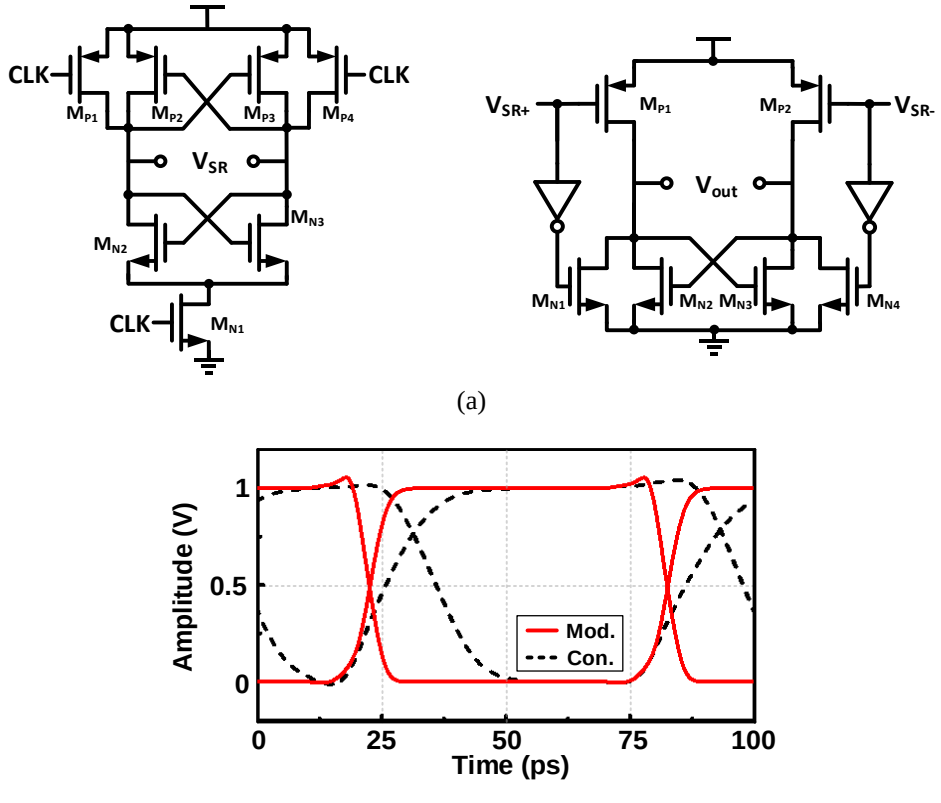


Fig. 4.22 (a) Schematic of the regeneration pair with SR latch and (b) comparison between a modified SR latch and a conventional SR latch.

The output of the EQ summer is directly connected to a clocked CMOS cross-coupled pair shown in Fig. 4.22(a) for the data regeneration. Similar to the strong-arm comparator, a SR latch is needed to keep the regenerated output when the cross-coupled pair is in reset mode. Conventional SR latches implemented by CMOS logics exhibits long propagation delay, asymmetric transition and heavy input loading. [56] presents a modified SR latch to correct the asymmetric transition. Nevertheless, the delay and loading issues remain considerable. In this design, a modified SR latch is proposed to achieve symmetric transition with low latency and moderate input loading. As shown in Fig. 4.22(a), the proposed solution consists of a pair of auxiliary inverters and a core latch amplifier. Its operation as a SR latch can be illustrated as below: (1) Sensing mode: In the sensing mode, the latch input (V_{SR}) and its inverted version (V'_{SR}) determine the output of the core latch amplifier. The auxiliary NMOS pair (M_{N1} and M_{N4}) accelerates and balances the output transition by discharging the output node before the NMOS cross-coupled pair ($M_{N2\text{-}3}$) is turned on. (2) Latching mode: The SR latch input is charged to high in the reset period, turning off the PMOS differential pair ($M_{P1\text{-}2}$). Meanwhile, the M_{N1} and M_{N4} are turned off by the inverted input (V'_{SR}). As a result, the SR latch output is disconnected from the input and kept by the NMOS cross-coupled pair ($M_{N2\text{-}3}$). To reduce the parasitic loading at the latch output, only the NMOS cross-coupled pair is adopted. The effect of the charge leakage due to the lack of PMOS cross-coupled pair is negligible at such high data rate. Fig. 4.22(b) compares the simulated transient waveform of a conventional and the proposed SR latch. A 2.8 times improvement in the propagation delay and the symmetrical transition are observed in the proposed SR latch.

4.3.3 Edge Path Implementation

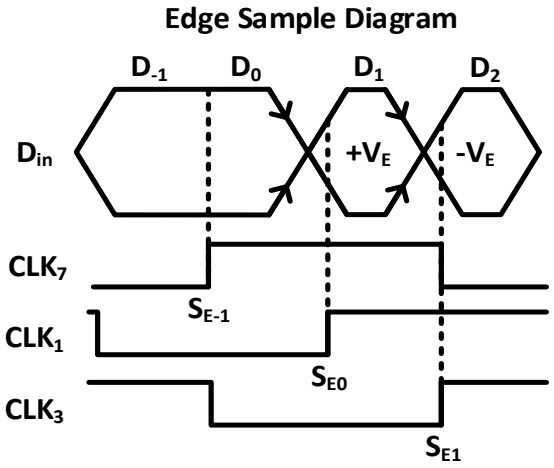


Fig. 4.23 Edge transition examples.

The edge path samples the input data transition and generates a current that is proportional to it. However, the input PRBS data may contain arbitrarily long consecutive "1" or "0" with a transition density of 50%. Invalid edge samples like S_{E-1} in Fig. 4.23 originating from consecutive bits must be discarded to avoid a large disturbance at the loop filter. The valid samples are simply identified by performing XOR logic for data bits before and after a certain edge sample (e.g., D_0 XOR D_1 for S_{E1}). Besides consecutive bits, an edge transition may come in two different directions. For example, the edge samples S_{E0} and S_{E1} in Fig. 4.23 exhibit same sampled amplitude with an opposite polarity, which actually indicates identical clock phase deviation. In this case, the sign of the S_{E1} requires an inversion operation before feeding to the loop filter. To simplify hardware implementation, the edge sample sign is defined as the sign of the data bit preceding to a certain edge sample.

Fig. 4.24 presents a conceptual timing diagram of the edge path. The CLK_0 and the CLK_2 trigger two data paths to regenerate input data and produce edge path enable signal. The data path takes roughly ¼ of each clock cycle ($t_1 - t_4$) to complete the evaluation and holds the valid output for the rest ¾ clock cycle ($t_3 - t_7$). Since the charge-steering EQ summer needs to be reset for half clock cycle, its output is sampled again and kept from t_4 to t_7 to ensure a stable input for the V/I converter.

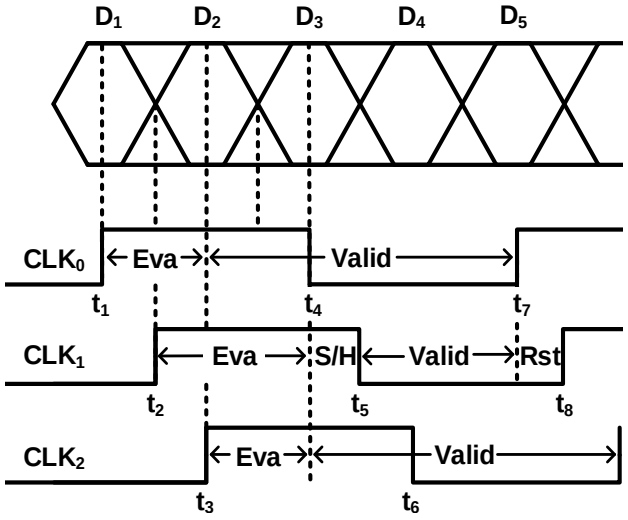


Fig. 4.24 Edge path timing diagram.

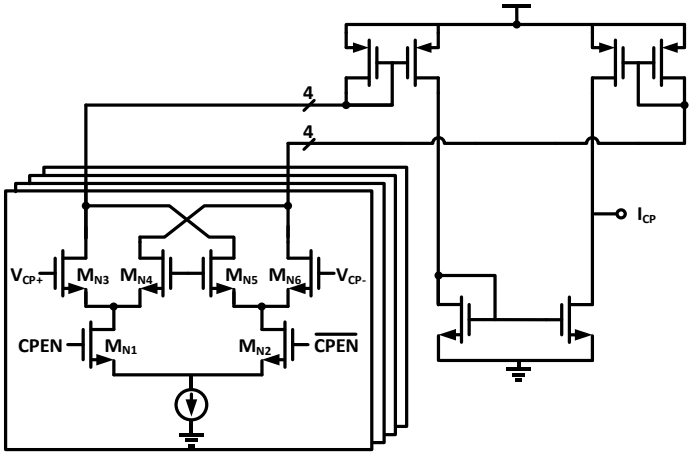


Fig. 4.25 Schematic of the charge pump.

The V/I converter would be enabled from t_5 to t_7 if the edge path senses a valid sample. Finally, the edge path is reset from t_7 to t_8.

The sampler and the equalizer summer in the edge path share the same implementation as in the data path. The schematic of the V/I converter is shown in Fig. 4.25. The V/I converter consists of four identical input slices for four edge paths and a set of P/NMOS current mirror to sink or source the current. Each input slice has two oppositely connected differential pairs ($M_{N3\text{-}6}$) and a pair of enable

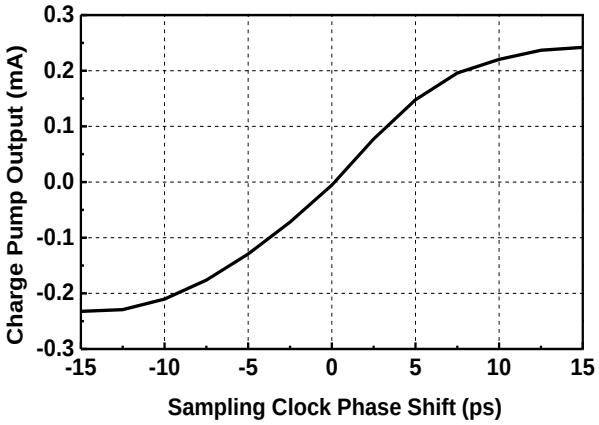


Fig. 4.26 Simulated edge path transfer curve.

switches ($M_{N1\text{-}2}$) to control the polarity. The enable signal is generated by the logic operation as discussed before to determine the polarity and validity of each edge sample. The transfer curve of four edge paths is simulated by manually tuning the sampling clock phase while measuring the averaged charge pump output current. As shown in Fig. 4.26, the transfer curve verifies the wide range linear operation of the proposed phase detector with a PD gain of 33 μA/ps.

4.3.4 Injection-Locked Oscillator and Delay Line

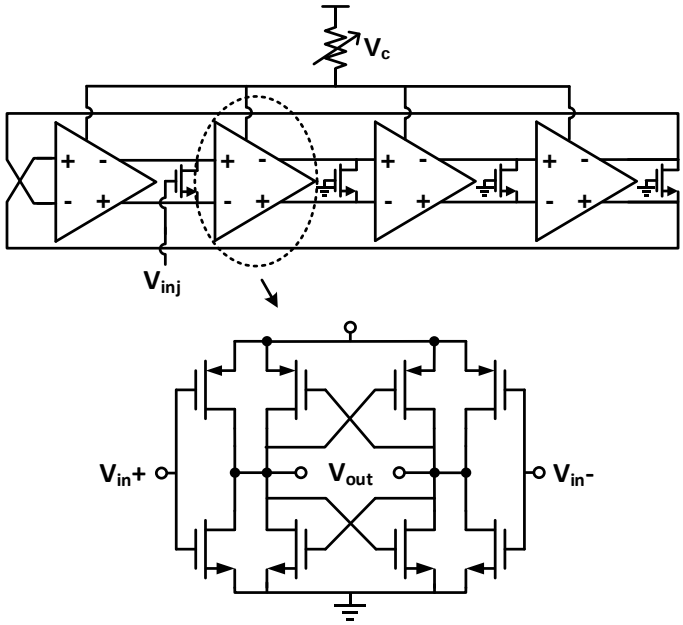
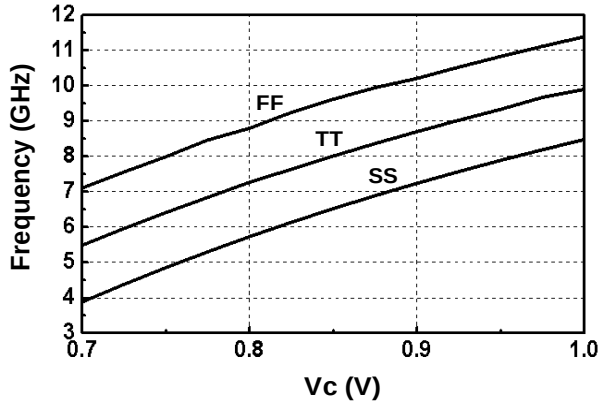
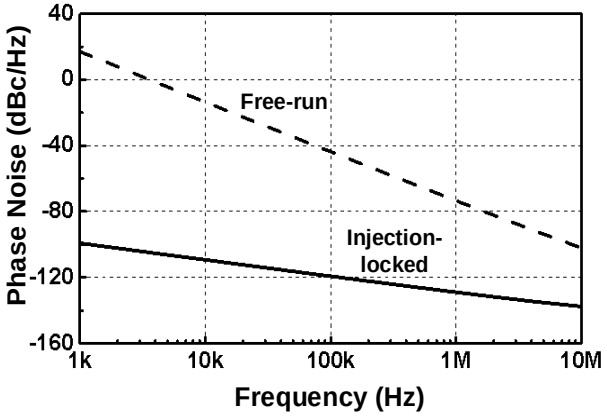


Fig. 4.27 Schematic of the ring oscillator.

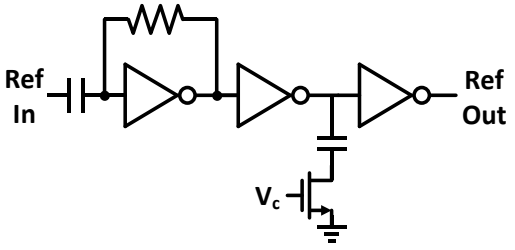


(a)

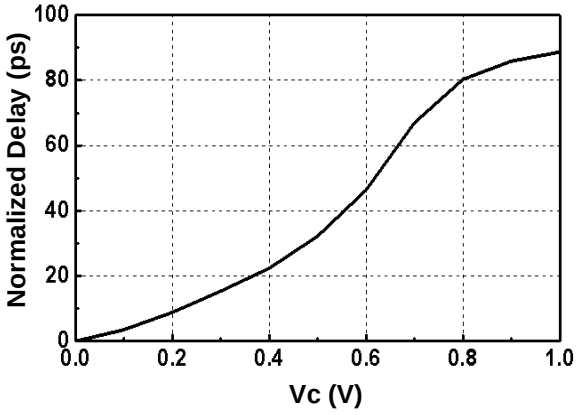


(b)

Fig. 4.28 (a) Simulated ring oscillator frequency tuning range and (b) phase noise.



(a)



(b)

Fig. 4.29 (a) Schematic of the reference clock delay line and (b) simulated delay range.

A CMOS ring oscillator is adopted in this design to produce the eight-phases clock for the quarter-rate CDR. A ring oscillator is more suitable for the injection-locked multi-phase clock generation because it has much wider tuning and locking range compared to a LC-VCO.

Meanwhile, its inferior phase noise could be corrected by injection locking as long as the a “clean” injection source is provided.

Fig. 4.27 shows the schematic of the four-stage ring oscillator. The pseudo differential delay cells in the ring oscillator consists of a pair of main inverter and a weak auxiliary cross-coupled inverter to enhance differential operation. The cross-coupled inverter pair is sized to be half of main inverters to reduce excessive capacitive loading and power consumption. A NMOS transistor and three dummy transistors are placed at the output of each delay cell to perform the direct injection [57]. Since the oscillator output amplitude varies with its output frequency, an AC coupled inverter buffer chain is used to restore the clock to full swing. The simulated frequency tuning range is shown in Fig. 4.28(a). The tuning range covers target operation rate under three extreme process corners. As shown in Fig. 4.28(b), the VCO phase noise at 1 MHz is improved by 40 dB after being injection-locked.

Fig. 4.29 shows the schematic of the delay line and the simulated tuning range. The delay tuning range is about 70 ps as the control voltage varies from 0.2 V to 0.8 V, which is sufficient to cover 1 UI delay range under process variation. The duty cycle distortion due to the extra loading capacitor to ground is not a problem since a pulse generator is followed to generate narrow pulse as the injection source.

4.4 Experimental Results

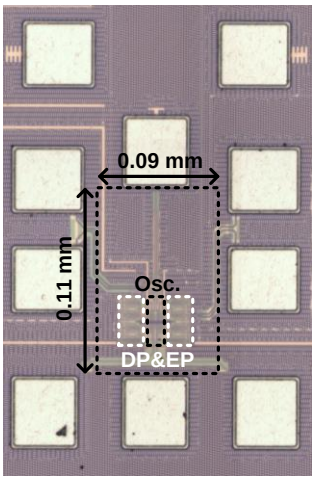


Fig. 4.30 CDR chip micrograph.

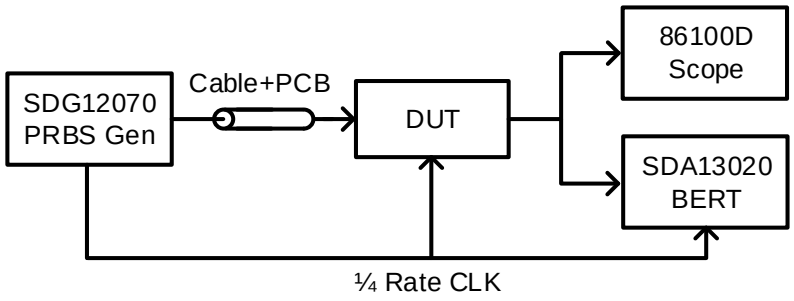


Fig. 4.31 CDR measurement setup.

The die photo of the CDR fabricated in 28-nm CMOS is shown in Fig. 4.30. The core circuit occupies only 0.01 mm^2. Fig. 4.31 depicts the measurement setup. The PRBS data generated by a Picoseconds SDG12070 PRBS generator is fed to the DUT with a 1.5-meter coaxial cable and pre-characterized PCB traces as the inserted lossy channels. The high-speed input and output signals are brought to PCB transmission lines through aluminum bonding wires fabricated with standard wedge-bonding process. The recovered clock and data signals are measured in the time domain by a Keysight 86100D wide-band scope. Besides, a Picoseconds SDA13020 error detector performs the BER measurement for the recovered data. The ¼ rate clock is provided by the PRBS generator as the injection reference clock as well as the trigger for the BERT. The maximum measurable data rate in this setup is limited to 30 Gb/s by the PRBS generator.

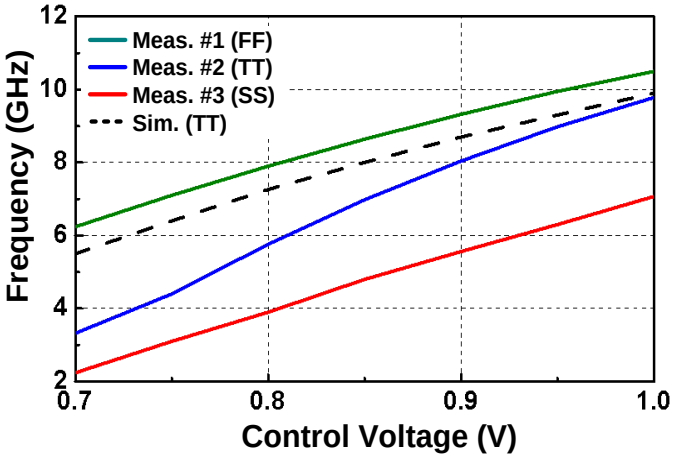


Fig. 4.32 Measured ring oscillator tuning curve.

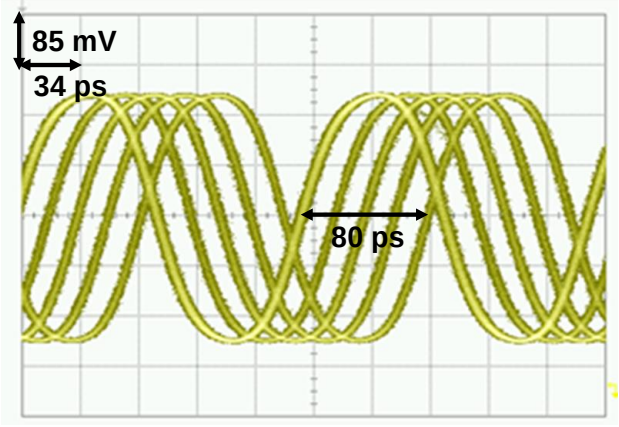


Fig. 4.33 Measured delay line phase tuning range.

Fig. 4.32 shows the measured tuning range of free-running ring oscillators in FF, TT and SS process corners. Compared to the simulation result shown as the dash line in Fig. 4.32, the measured tuning range in the TT corner is extended at the low frequency end. This measurement verifies prototypes in the TT and FF corners are able to cover the input data ranges from 25 Gb/s to 30 Gb/s in the quarter-rate operation.

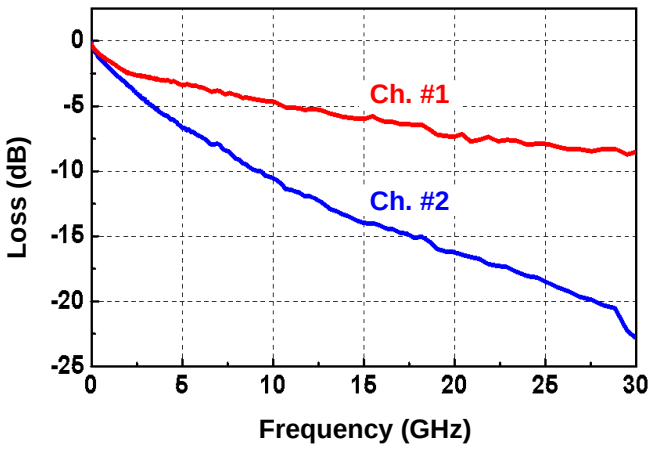


Fig. 4.34 Measured insertion loss of input channels.

The phase tuning range of the delay line is measured as shown in Fig. 4.33. The delay line is able to cover over 180 °tuning for a 6.25-GHz clock, which is equivalent to 80-ps phase adjustment range and is sufficient for 25-Gb/s data with a UI of 40 ps. The measured rms and peak-to-peak jitter of the clock after being injection-locked are 1 ps and 6.8 ps, respectively.

Fig. 4.34 presents the measured insertion loss of two channels used in the measurement setup. The channel #1 is a low loss channel consists of a 1.5-meter coaxial cable while the channel #2 is a high loss channel consists of a 1.5-meter coaxial cable and a 12-cm PCB trace. For 25 Gb/s PRBS data, the loss arose from the channel #1 and the channel #2 at Nyquist rate are 5.3 dB and 12.5 dB, respectively. Following measurements are first conducted with the channel #1 to verify the maximum operation speed and then with the channel #2 to demonstrate the equalization capability of the CDR.

Fig. 4.35 shows eye diagrams of PRBS data transmitted over the channel #1 and impulse responses of the channel #1. As shown in Fig. 4.35(a), the vertical eye opening ratio is about 60% and 45% at 25 Gb/s and 30 Gb/s, respectively. The degraded eye opening at 30 Gb/s is mostly due to the higher attenuation at the main-cursor (a_0) as shown in Fig. 4.35(b). In addition to the main-

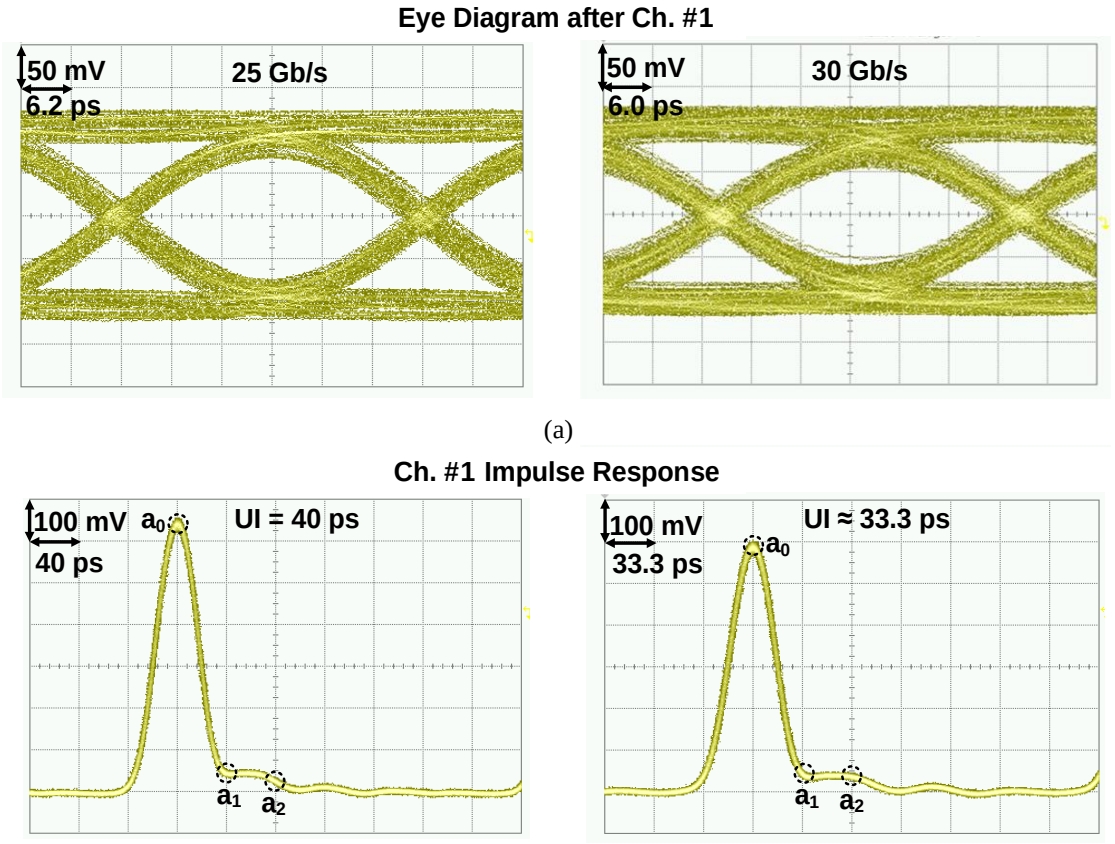


Fig. 4.35 (a) Eye diagrams of 25 Gb/s and 30 Gb/s data over the channel #1 and (b) channel #1 impulse responses.

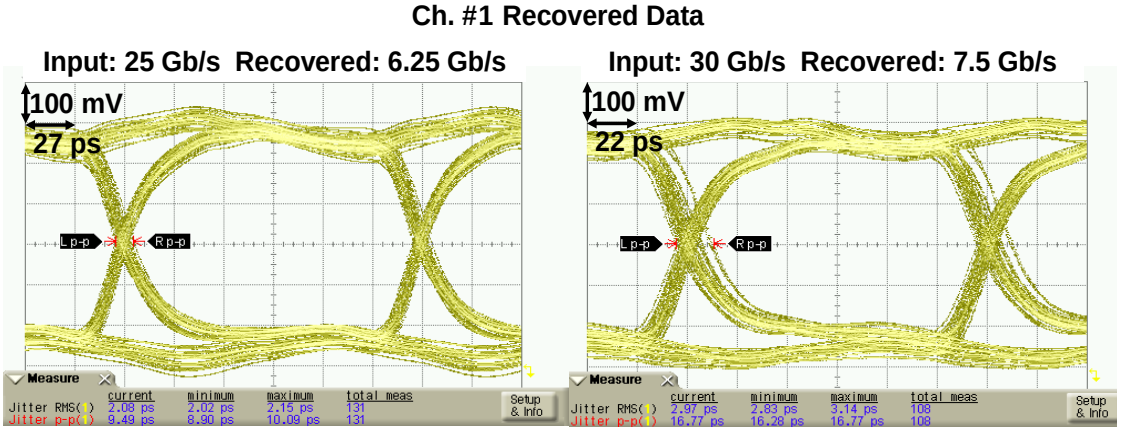


Fig. 4.36 Measured recovered data eye diagrams with 25 Gb/s and 30 Gb/s input data over the channel #1.

cursor attenuation, the non-zero first and second post-cursors (a_1 and a_2) resulted from channel reflections introduce larger timing jitter in the eye diagram.

Fig. 4.36 shows the recovered 6.25-Gb/s and 7.5-Gb/s data eye diagrams with 25-Gb/s and 30-Gb/s inputs shown in Fig. 4.35(a). The measured rms jitter and peak-to-peak jitter are 2.1 ps and 9.5 ps at 6.25 Gb/s and 3 ps and 16.8 ps at 7.5 Gb/s, respectively. Due to the single-ended operation of the 86100D scope, the measured jitter is partially contributed by the common-mode power supply noise and the series inductive peaking from the parasitic bondwire inductance between the CDR output buffer and the PCB trace. According to simulations, the large transient switching current of CMOS inverter output buffer leads to 80-mV_{p-p} ripple at the supply line. The measured BER bathtub curves of the recovered data are shown in Fig. 4.37. For both 25-Gb/s and 30-Gb/s inputs, the recovered data achieve error free operation (BER<10^{-12}) over 80% and 60% UI, respectively.

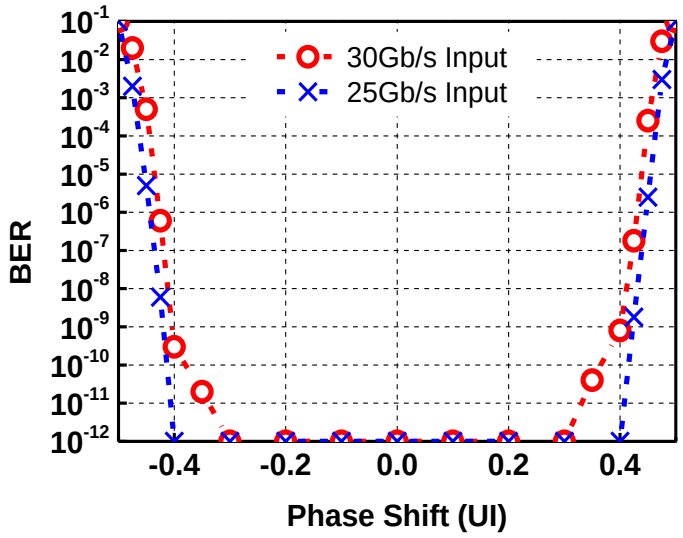
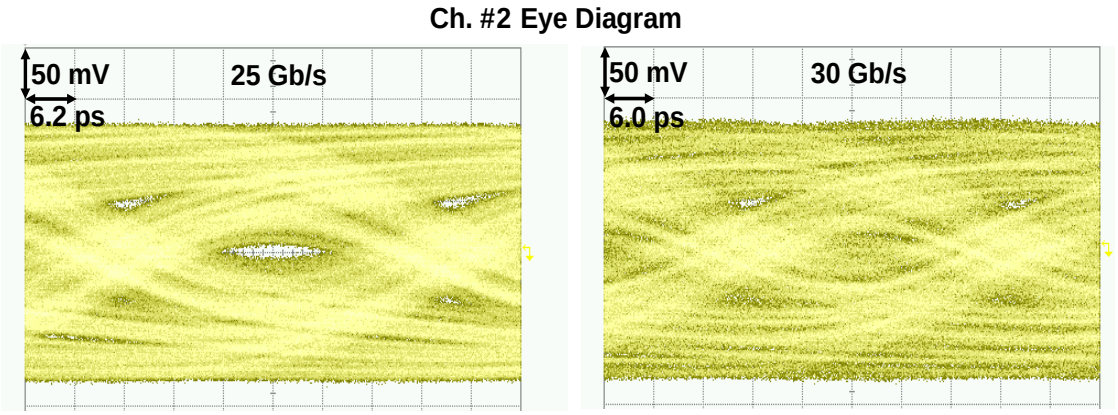
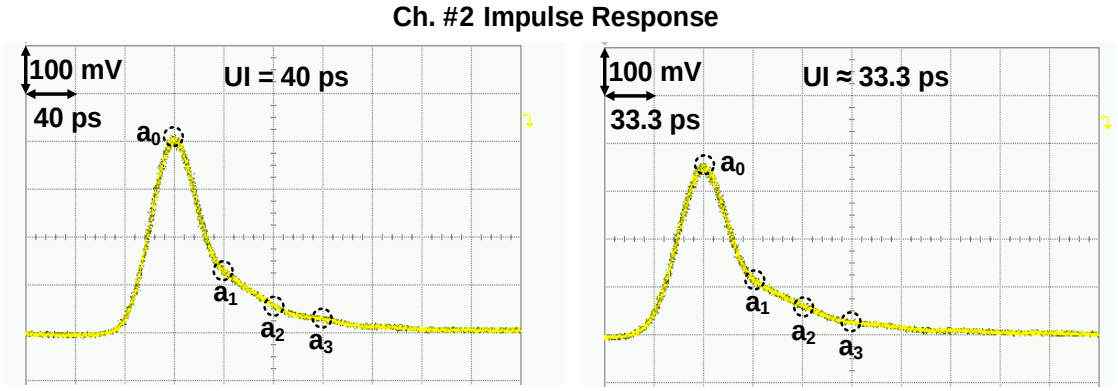


Fig. 4.37 Measured BER bathtub curves of the recovered data shown in Fig. 4.36.

Fig. 4.38(a) shows eye diagrams of data transmitted over the channel #2 and impulse responses of the channel #2. Due to the 12.3-dB and 14-dB insertion loss at Nyquist rate for 25-Gb/s and 30-Gb/s input date, the eye diagrams are severely distorted. The vertical eye-opening for the 25-Gb/s input is only 5 mV while the 30-Gb/s input eye is completely closed. Compared to the channel #1, the main-cursor (a_0) of channel #2 is further attenuated by 38% and 42% at 25 Gb/s and



(a)



(b)

Fig. 4.38 (a) Eye diagrams of 25 Gb/s and 30 Gb/s data over the channel #2 and (b) measured channel #2 impulse responses.

30 Gb/s as shown in Fig. 4.38(b). The severe channel loss of the channel #2 at high frequencies behave itself as the long post-curst tail in the time domain as depicted in Fig. 4.38(b). In addition, the ratio between the main-cursor and the first post-cursors is greatly reduced, which results in severe ISI in eye diagrams after the channel #2. Fig. 4.39 shows the measured BER bathtub curves versus input data rate for data transmitted over the channel #2. The high BER of data over 25 Gb/s demonstrates the poor input signal quality and the need for equalization to achieve error free transmission.

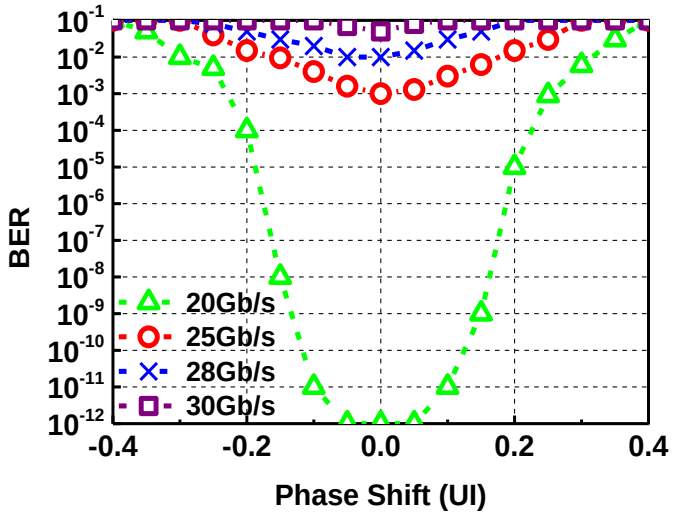


Fig. 4.39 Measured BER bathtub curves for CDR input data over the channel #2.

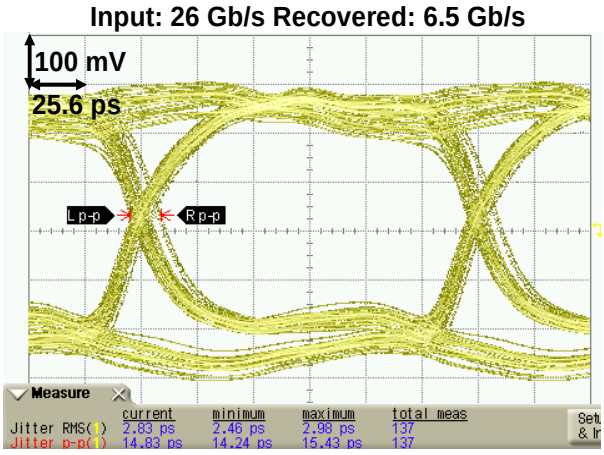


Fig. 4.40 Measured recovered data eye diagram with 26 Gb/s input over the channel #2.

Fig. 4.40 shows the recovered 6.5 Gb/s data eye diagram with 26 Gb/s input data transmitted through the channel #2. The CDR embedded equalization is enabled to compensate for the channel loss and recover the BER from 10^{-3} to 10^{-12}. The eye diagram of the recovered data depicts a rms jitter of 2.8 ps and a peak-to-peak jitter of 14.8 ps. Fig. 4.41 shows the measured bathtub curve of the recovered data shown in Fig. 4.40. The CDR successfully improves the BER from 3.6×10^{-3} to less than 10^{-12} within 46% UI.

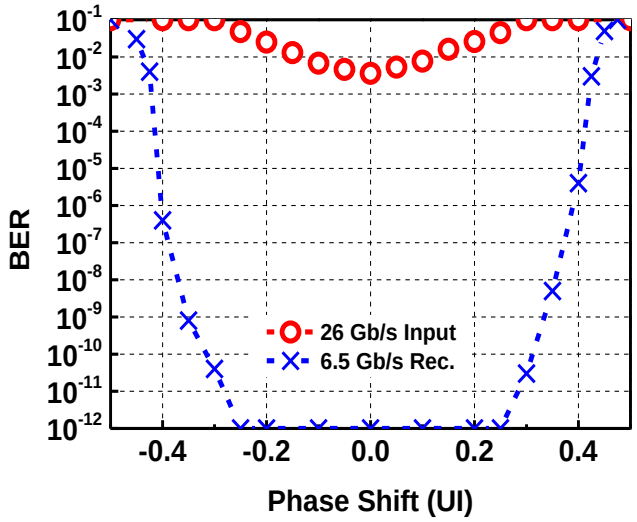


Fig. 4.41 Measured BER of the 26 Gb/s input data and the 6.5 Gb/s recovered data.

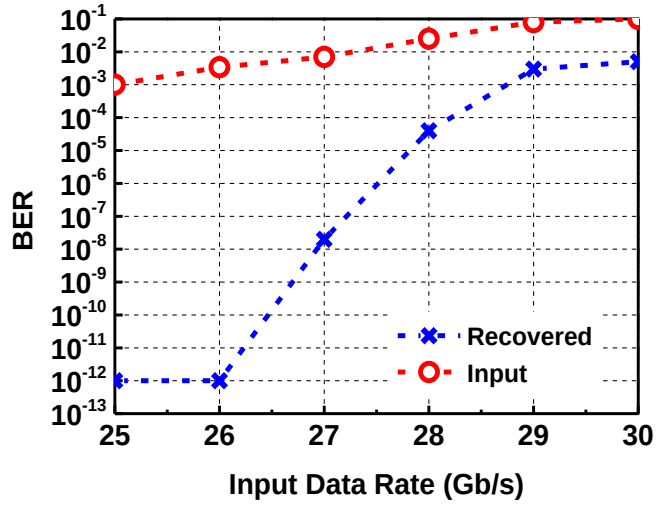


Fig. 4.42 Measured BER vs. input data rate for data over the channel #2.

Fig. 4.42 presents the measured BER curves of the input and the recovered data at various data rate. The CDR build-in equalization is able to achieve less than 10^{-12} BER for input data rate up to 26 Gb/s. According to Fig. 4.38(b), further increase of the input data rate results in an even severely attenuated main-cursor. Although the build-in FFE and DFE can improve eye-opening ratio, the significantly decreased eye-opening amplitude eventually falls below the sensitivity of the charge-steering based comparator and leads to high bit error rate.

Table VI shows the performance comparison of this design with other published works. Compared to prior arts, the proposed architecture achieves best power efficiency among designs with equalization and minimum active area. According to simulations, the equalization capability can be further improved by 7 dB an additional DFE tap and a CTLE with power consumption of 3 mW to cover even severer channel loss as in [60].

Table VII: CDR Performance Comparison.

	[58] Jung JSSC 13’	[59] Kim TCAS-I 15’	[60] Hong JSSC 16’	**This Work**
PD Arch.	½ Rate Linear	N/A	½ Rate BB	**¼ Rate Linear**
Clock Arch.	Embedded	Forwarded	Embedded	**Forwarded**
Equalization	No	CTLE	CTLE+DFE	**FFE+DFE**
Max. Ch. Loss (dB)*	N/A	N/A	20 @ 12.5 GHz	**13 @ 13 GHz**
DR (Gb/s)	25	9.6	27	**30/26**
Power (mW)	5	9.2	84.5	**8**
Eff. (pJ/bit)	0.2	0.96	3.12	**0.28**
Technology	65 nm	65 nm	40 nm	**28 nm**
Active Area (mm^2)	0.04	0.016	0.09	**0.01**

* For BER < 10^{-12}

Chapter 5 Conclusion and Future Work

This thesis investigates the design and implementation of power efficient, low-cost and high performance optical and fiber-wireless hybrid systems to facilitate the rapid increasing global data traffic demand. The main challenges of designing such systems in standard CMOS process are analyzed carefully. Novel topologies are proposed in both circuit and system level to achieve the targeted performance.

The first circuit block examined in this research is the TIA presented in Chapter 2. As the most critical block in an optical receiver chain, TIA generally determines the receiver performance. The key challenges of CMOS transimpedance amplifier are gain-bandwidth trade-off and noise optimization. A multiple-inductive peaking technique achieving 2.8x bandwidth extension ratio is proposed to alleviate the gain-bandwidth trade-off without power penalty. Meanwhile, the inverter based core amplifier is optimized for better power efficiency and reduced input referred noise.

In Chapter 3, a fiber-wireless modulator with fully integrated on-chip PD for short-range backhaul connectivity in emerging fiber-wireless mobile networks is presented for the first time. The optical receiver performs the O/E conversion with an on-chip PD to eliminate the need for a costly off-chip PD. The integrated 60-GHz QPSK modulator enables a power efficient, low cost and small form factor solution for the future fiber-wireless networks.

Chapter 4 presents a power-efficient 30-Gb/s CDR with an embedded equalization to compensate for a channel loss up to 13 dB. The quarter-rate linear phase detection is achieved by the proposed sub-sampling linear PD. Meanwhile, the sampling front-end enables an efficient implementation of DRE and FFE at the Rx side. In addition to the architecture level innovation, the power consumption is further reduced with circuit level design optimizations by utilizing the charge-steering style EQ summer and the proposed SR latch.

5.1 Summary of main contributions

The main contributions of this thesis is summarized as follow:

1. 25-GHz 0.12-pJ/bit CMOS Transimpedance Amplifier

- A multiple inductive peaking technique is proposed for broadband TIA design
- A detail analysis of the inverter based TIA for gain, noise and power consumption optimization is presented

2. Fully-Integrated Optical-to-mmW Modulator

- A fully-integrated optical-to-mmW modulator for the next generation communication system is presented for the first time

3. 30-Gb/s 0.28-pJ/bit CDR with Embedded Equalization

- A sampling phase detector is proposed to achieve the quarter-rate linear operation
- A modified SR latch is proposed to reduce propagation delay and transition asymmetry
- First to integrate a low-overhead FFE and DFE in a CDR for channel loss compensation

5.2 Future work

To realize a more complete and robust fiber-wireless system, several blocks need to be integrated or optimized.

First, frequency synthesizers (PLL) are required at both the Tx and the Rx sides to provide LOs for the mmW transceiver and multi-phases clocks for the CDR, respectively. The architecture of the PLL for mmW transceiver is likely to be a LC-VCO based due to its high operation frequency and stringent requirement for phase noise performance. In contrast, the architecture of the PLL generating sub-rate clocks for the CDR could be a ring oscillator based one to save silicon area and facilitate the multi-phase clock generation. Recent researches have shown a great potential of ring

oscillator based injection-locked PLLs for realizing phase noise performance that is comparable to LC-VCO based PLLs with much lower power and area consumption [61], [62].

Secondly, integrating an on-chip power amplifier (PA) would further reduce the fiber-wireless communication system implementation complexity and cost. However, a wideband PA is required to fully utilized the available bandwidth at the mmW band. Simply reducing the quality factor of the LC resonator to achieve the required bandwidth sacrifices the PA efficiency. Therefore, advanced wideband mmW circuits techniques [63], [64] should be further investigated.

Appendix: High-Speed PCB Design

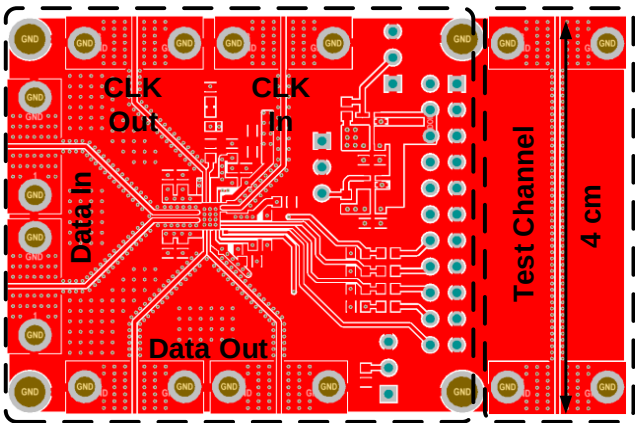


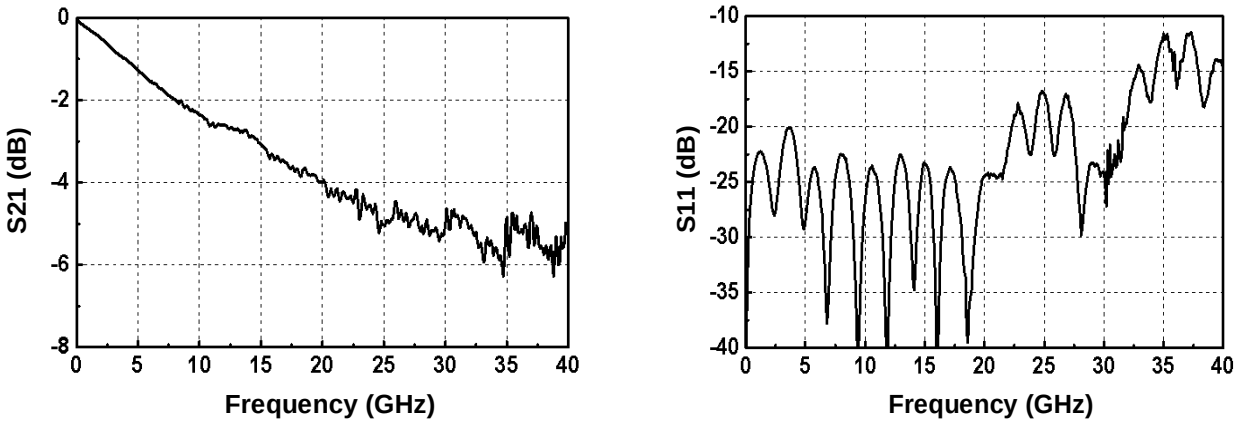
Fig. A-1 PCB top layer layout view

Table A-1 PCB Microstrip Design Parameter

Substrate Thickness	12 mils
Substrate Dielectric	3.55
Trace Width	14 mils
Trace Separation to Ground	5 mils
Trace Thickness	1 oz. (0.035 mm)

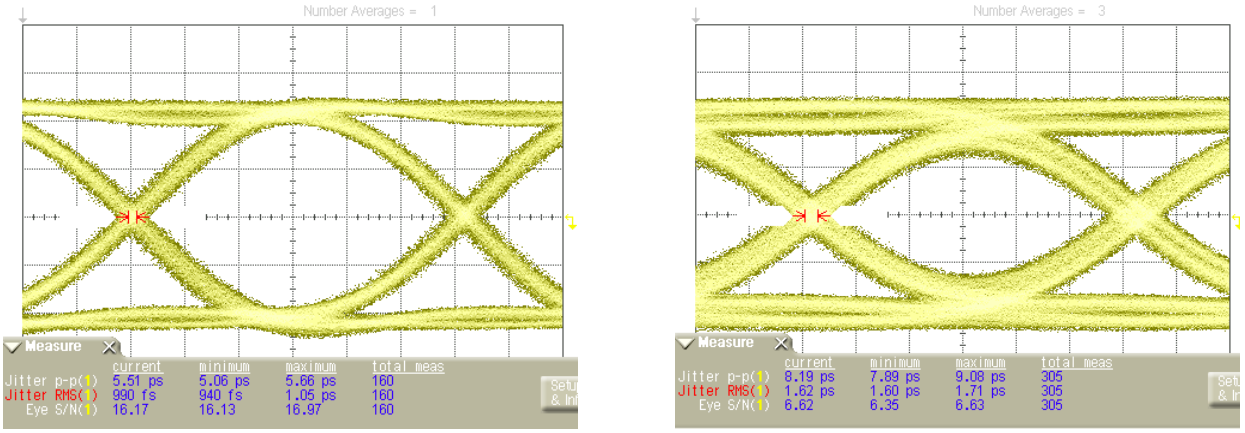
The top layer layout view of the PCB designed for CDR measurement is shown in Fig. A-1. In addition to the core area, a 4-cm test channel is fabricated to verified the high-frequency characteristics of the PCB. The PCB is a 4-layer design with top and bottom layers made with the Rogers 4003 high frequency circuit material to reduce the insertion loss. The trace is designed to be 50-Ω impedance matched by adjusting width and thickness of the trace according to the substrate dielectric constant and the Substrate thickness given in Table A-1. The measurement results of the test channel mounted with two Southwest 26-GHz end-launch connectors are shown in Fig. A-2 and Fig. A-3. The insertion loss at 12.5 GHz and 25 GHz are 3 dB and 5 dB respectively. The S11 is below –15 dB within 30 GHz. A time domain measurement shown in Fig. A-3 is also conducted to verified the signal integrity of the trace. The measured rms jitter is 1.6 ps with 1-m cable and the

channel. The channel and connectors degrade rms jitter by 0.6 ps compared to the case with 1-m cable only.



(a) (b)

Fig. A-2 Measurement of the 4cm test channel: (a) insertion loss (S21) and (b) reflection (S11).



(a) (b)

Fig. A-3 Measured eye diagrams at 25 Gb/s of (a) 1-m Gore cable and (b) 1-m Gore cable with test channel.

Bibliography

[1] Cisco Visual Networking Index (VNI) Forecast, Jun. 2015.

[2] C. Q. Wu, E. A. Sovero, B. Massey, "40-GHz transimpedance amplifier with differential outputs using InP-InGaAs heterojunction bipolar transistors," *IEEE Journal of Solid-State Circuits*, vol.38, no.9, pp.1518-1523, Sept. 2003.

[3] J. Mullrich *et al*, "High-gain transimpedance amplifier in InP-based HBT technology for the receiver in 40- Gb/s optical-fiber TDM links," *IEEE Journal of Solid-State Circuits*, vol.35, no.9, pp.1260-1265, Sept. 2000.

[4] J. G. Andrews, S. Buzzi, W. Choi, S. V. Hanly, A. Lozano, A. C. Soong, and J. C. Zhang, "What will 5G be?," *IEEE Journal on Selected Areas in Communications*, vol. 32, no. 6, pp. 1065–1082, 2014.

[5] J. G. Andrews, H. Claussen, M. Dohler, S. Rangan, and M. C. Reed, "Femtocells: Past, Present, and Future," *IEEE Journal on Selected Areas in Communications*, vol. 30, no. 3, pp. 497–508, Apr. 2012.

[6] Z. Pi, F. Khan, "An introduction to millimeter-wave mobile broadband systems," *IEEE Communications Magazine*, vol.49, no.6, pp.101-107, Jun. 2011.

[7] X. Zhang, B. Hraimel, K. Wu, "Breakthroughs in Optical Wireless Broadband Access Networks," *IEEE Photonics Journal*, vol.3, no.2, pp. 331-336, Apr. 2011.

[8] M. Sauer, A. Kobyakov, J. George, "Radio Over Fiber for Picocellular Network Architectures," *IEEE Journal of Lightwave Technology*, vol.25, no.11, pp.3301-3320, Nov. 2007.

[9] X. Zhang, B. Hraimel, K. Wu, "Breakthroughs in Optical Wireless Broadband Access Networks," *IEEE Photonics Journal*, vol.3, no.2, pp. 331-336, Apr. 2011.

[10] S. M. Park and H-J Yoo, "1.25-Gb/s regulated cascode CMOS transimpedance amplifier for Gigabit Ethernet applications," *IEEE Journal of Solid-State Circuits*, vol. 39, pp. 112-121, Jan. 2004.

[11] D. Lee, J. Han, G. Han and S. M. Park, "An 8.5-Gb/s Fully Integrated CMOS Optoelectronic Receiver Using Slope-Detection Adaptive Equalizer," *IEEE Journal of Solid-State Circuits*, vol. 45, pp. 2861-2873, Dec. 2010.

[12] S-H Huang, W-Z Chen, Y-W Chang and Y-T Huang, "A 10-Gb/s OEIC with Meshed Spatially-Modulated Photo Detector in 0.18-um CMOS Technology," *IEEE Journal of Solid-State Circuits*, vol. 46, pp. 1158-1169, May 2011.

[13] J-Y Jiang, P-C Chiang, H-W Hung, C-L Lin, T. Yoon and Jri Lee, "100 Gb/s Ethernet chipsets in 65nm CMOS technology," *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pp. 120-121, Feb. 2013.

[14] D. Li, G. Minoia, M. Repossi, D. Baldi, E. Temporiti, A. Mazzanti, and F. Svelto, "A Low-Noise Design Technique for High-Speed CMOS Optical Receivers," *IEEE Journal of Solid-State Circuits*, vol. 49, pp. 1437-1447, Jun. 2014.

[15] Q. Pan, Z. Hou, Y. Wang, Y. Lu, W.-H. Ki, K. C. Wang, and C. P. Yue, "A 48-mW 18-Gb/s fully integrated CMOS optical receiver with photodetector and adaptive equalizer," in *IEEE Symposium on VLSI Circuits Digest of Technical Papers*, pp. 1-2, Jun. 2014.

[16] J. Kim and J. F. Buckwalter, "Bandwidth Enhancement with Low Group-Delay Variation for a 40-Gb/s Transimpedance Amplifier," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 8, pp. 1964–1972, Aug. 2010.

[17] E. Säckinger, *Broadband circuits for optical fiber communication*, John Wiley & Sons, 2005.

[18] B. Razavi, *Design of integrated circuits for optical communications*, John Wiley & Sons, 2012.

[19] Y. Wang, Y. Lu, Q. Pan; Z. Hou, L. Wu, W-H Ki and C. P. Yue, “A 3-mW 25-Gb/s CMOS transimpedance amplifier with fully integrated low-dropout regulator for 100GbE systems,” *IEEE Radio Frequency Integrated Circuits Symposium*, pp. 275-278, Jun. 2014.

[20] Y. Lu, W-H Ki, and C. P. Yue, "A 0.65ns-response-time 3.01ps FOM fully-integrated low-dropout regulator with full-spectrum power-supply-rejection for wideband communication systems," *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pp. 306-307, Feb. 2014.

[21] S. Galal and B. Razavi, "40-Gb/s amplifier and ESD protection circuit in 0.18-μm CMOS technology," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 12, pp. 2389-2396, Dec. 2004.

[22] C-F Liao and S-I Liu, "40 Gb/s Transimpedance-AGC Amplifier and CDR Circuit for Broadband Data Receivers in 90 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 3, pp. 642-655, Mar. 2008.

[23] P. Staric and E. Margan, *Wideband Amplifiers*. Springer Science & Business Media, 2007.

[24] T. Y. Man, K. N. Leung, C. Y. Leung, P. K. T. Mok and M. Chan, "Development of Single-Transistor-Control LDO Based on Flipped Voltage Follower for SoC," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol.55, no.5, pp. 1392-1401, Jun. 2008.

[25] J. S. Youn, H. S. Kang, M. J. Lee, K. Y. Park, and W. Y. Choi, “High-speed CMOS integrated optical receiver with an avalanche photodetector,” *IEEE Photonics Technology Letters*, vol. 21, no. 20, pp. 1553–1555, Oct. 2009.

[26] C. Li and S. Palermo, "A Low-Power 26-GHz Transformer-Based Regulated Cascode SiGe BiCMOS Transimpedance Amplifier," *IEEE Journal of Solid-State Circuits*, vol.48, no.5, pp.1264-1275, May 2013.

[27] S. Hur, T. Kim, D. J. Love, J. V. Krogmeier, T. A. Thomas and A. Ghosh, "Millimeter Wave Beamforming for Wireless Backhaul and Access in Small Cell Networks," *IEEE Transactions on Communications*, vol. 61, no. 10, pp. 4391-4403, October 2013.

[28] K. Okada *et al.*, "Full Four-Channel 6.3-Gb/s 60-GHz CMOS Transceiver With Low-Power Analog and Digital Baseband Circuitry," *IEEE Journal of Solid-State Circuits*, vol.48, no.1, pp.46-65, Jan. 2013.

[29] Y. Wang *et al.*, "A 60GHz 4Gb/s fully integrated NRZ-to-QPSK modulator SoC for backhaul links in fiber-wireless networks," *European Solid-State Circuits Conference*, pp. 152-155, Sept. 2015.

[30] Q. Pan, Z. Hou, Y. Li, A. W. Poon, and C. P. Yue, "A 0.5-V P-Well/Deep N-Well photodetector in 65-nm CMOS for monolithic 850-nm optical receivers," *IEEE Photonics Technology Letters*, vol. 26, no. 12, pp. 1184−1187, Jun. 2014.

[31] B. Razavi, *Design of integrated circuits for optical communications*, John Wiley & Sons, 2nd Ed., pp. 24.

[32] D.Z. Turker et al., "A DCVSL Delay Cell for Fast Low Power Frequency Synthesis Applications," *IEEE Transactions on Circuits and Systems I: Regular Papers*, Jun. 2011.

[33] C. Yue, H.C. Luong, "Analysis and Design of a 2.9-mW 53.4–79.4-GHz Frequency-Tracking Injection-Locked Frequency Divider in 65-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol.48, no.10, pp.2403-2418, Oct. 2013.

[34] L. Jing; A. Li, D. Luo, C.R. Rowell, C.P. Yue, "Millimeter-wave 4:1 Transformer-based balun design for CMOS RF IC's," *IEEE International Wireless Symposium (IWS)*, pp. 1-4, Apr. 2015.

[35] Y. Dong, and K. Martin, "A monolithic 3.125 Gbps fiber optic receiver front-end for POF applications in 65 nm CMOS," in *IEEE Custom Integrated Circuits Conference*, pp. 1-4, Sep. 2011.

[36] V. Vidojkovic *et al.*, “A Low-Power Radio Chipset in 40nm LP CMOS with Beamforming for 60GHz High-Data-Rate Wireless Communication,” *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pp.236-237, Feb. 2013.

[37] T. Tsukizawa *et al*., “A Fully Integrated 60GHz CMOS Transceiver Chipset Based on WiGig/IEEE802.11ad with Built-In Self Calibration for Mobile Applications,” *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pp.230-231, 17-21 Feb. 2013.

[38] H. R. Charles, “A self correcting clock recovery curcuit,” *IEEE Journal of Lightwave Technology*, vol. 3, pp. 1312-1314, Dec. 1985.

[39] J. D. H. Alexander, "Clock Recovery from Random Binary Data," *IEEE Electronics Letters*, vol. 11, pp. 541-542, Oct. 1975.

[40] “SONET OC-192 Transport System Generic Criteria,” Telcordia, Piscataway, NJ, Tech. Rep. GR-1377-CORE, Mar. 1998.

[41] J. Cao, Sui Huang and M. M. Green, "Non-idealities in linear CDR phase detectors," *European Conference on Circuit Theory and Design*, pp. 158-161, 2011.

[42] J. Lee, K. S. Kundert, and B. Razavi, “Analysis and modeling of bang-bang clock and data recovery circuits,” *IEEE Journal of Solid-State Circuits*, vol. 39, no. 9, pp. 1571–1580, Sep. 2004.

[43] J. Lee and B. Razavi, "A 40-Gb/s clock and data recovery circuit in 0.18-µm CMOS technology," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 12, pp. 2181-2190, Dec. 2003.

[44] L. Rodoni *et al.*, “A 5.75 to 44 Gb/s Quarter Rate CDR With Data Rate Selection in 90 nm Bulk CMOS,” *IEEE Journal of Solid-State Circuits*, vol. 44, no. 7, pp. 1927–1941, Jul. 2009.

[45] J. L. Sonntag and J. Stonick, "A Digital Clock and Data Recovery Architecture for Multi-Gigabit/s Binary Links," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 8, pp. 1867–1875, Aug. 2006.

[46] P. K. Hanumolu, G.-Y. Wei, and U.-K. Moon, "A Wide-Tracking Range Clock and Data Recovery Circuit," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 2, pp. 425–439, Feb. 2008.

[47] M. T. Hsieh and G. E. Sobelman, "Architectures for multi-gigabit wire-linked clock and data recovery," *IEEE Circuits and Systems Magazine*, vol. 8, no. 4, pp. 45–57, Fourth 2008.

[48] N. Kalantari and J. F. Buckwalter, "A Multichannel Serial Link Receiver With Dual-Loop Clock-and-Data Recovery and Channel Equalization," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 11, pp. 2920–2931, Nov. 2013.

[49] J. F. Bulzacchelli, "Design techniques for CMOS backplane transceivers approaching 30-Gb/s data rates," *IEEE Custom Integrated Circuits Conference*, pp. 1–8, 2013.

[50] A. Momtaz and M. M. Green, "An 80 mW40 Gb/s 7-tap T/2-spaced feed-forward equalizer in 65 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 3, pp. 629–639, Mar. 2010.

[51] E. Mammei *et al.*, "Analysis and design of a power-scalable continuous-time FIR equalizer for 10 Gb/s to 25 Gb/s multi-mode fiber EDC in 28 nm LP CMOS," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 12, pp. 3130–3140, Dec. 2014.

[52] B. Zhang *et al.*, "A 28Gb/s multi-standard serial-link transceiver for backplane applications in 28nm CMOS," *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pp. 52–53, Feb. 2015.

[53] J. W. Jung and B. Razavi, "A 25-Gb/s 5-mW CMOS CDR/Deserializer," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 3, pp. 684–697, Mar. 2013.

[54] S.-H. W. Chiang, H. Sun, and B. Razavi, “A 10-Bit 800-MHz 19-mW CMOS ADC,” *IEEE Journal of Solid-State Circuits*, vol. 49, no. 4, pp. 935–949, Apr. 2014.

[55] J. W. Jung and B. Razavi, “A 25 Gb/s 5.8 mW CMOS Equalizer,” *IEEE Journal of Solid-State Circuits*, vol. 50, no. 2, pp. 515–526, Feb. 2015.

[56] B. Nikolic, *et al.,* "Improved Sense-Amplifier-Based Flip-Flop: Design and Measurements," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 6, pp. 876-884, June 2000.

[57] S. D. Toso, et al., “A 0.06 mm 11 mW Local Oscillator for the GSM Standard in 65 nm CMOS,” *IEEE Journal of Solid-State Circuits*, vol. 45, no. 7, pp. 1295–1304, Jul. 2010.

[58] J. W. Jung and B. Razavi, "A 25-Gb/s 5-mW CMOS CDR /Deserializer, " *IEEE Journal of Solid-State Circuits*, vol. 48, no. 3, pp. 684-697, March 2013.

[59] Y. J. Kim, S. H. Chung, K. S. Ha, S. J. Bae, and L. S. Kim, “A 9.6 Gb/s 0.96 mW/Gb/s Forwarded Clock Receiver With High Jitter Tolerance Using Mixing Cell Integrated Injection-Locked Oscillator,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 10, pp. 2495–2503, Oct. 2015.

[60] Z. H. Hong, Y. C. Liu, and W. Z. Chen, “A 3.12 pJ/bit, 19 #x2013;27 Gbps Receiver With 2-Tap DFE Embedded Clock and Data Recovery,” *IEEE Journal of Solid-State Circuits*, vol. 50, no. 11, pp. 2625–2634, Nov. 2015.

[61] S. Choi, S. Yoo and J. Choi, "10.7 A 185fs rms-integrated-jitter and -245dB FOM PVT-robust ring-VCO-based injection-locked clock multiplier with a continuous frequency-tracking loop using a replica-delay cell and a dual-edge phase detector," *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pp. 194-195, Feb. 2016.

[62] M. Kim, S. Choi and J. Choi, "A 450-fs jitter PVT-robust fractional-resolution injection-locked clock multiplier using a DLL-based calibrator with replica-delay-cells," *Symposium on VLSI Circuits (VLSI Circuits)*, pp. C142-C143, Jun. 2015.

[63] M. Bassi, et al., “A 40-67 GHz Power Amplifier With 13 dBm Psat and 16% PAE in 28nm CMOS LP,” *IEEE Journal of Solid-State Circuits*, vol. 50, no. 7, Jul. 2015.

[64] S.V. Thyagarajan, A. M. Niknejad, and C. D. Hull, “A 60 GHz Drain-Source Neutralized Wideband Linear Power Amplifier in 28nm CMOS,” *IEEE Trans. Circuits Syst. I. Reg. Papers*, vol. 61, no. 8, Aug. 2014