# Wireless Power Acquisition and Regulation: Power Management Integrated Circuits for Biomedical Implantable Devices

by

Yan Lu

A Thesis Submitted to
The Hong Kong University of Science and Technology
in Partial Fulfillment of the Requirements for
the Degree of Doctor of Philosophy
in the Department of Electronic and Computer Engineering

December 2013, Hong Kong

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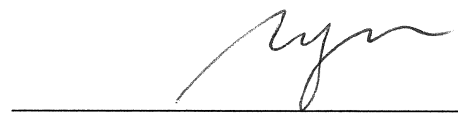

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and have found that it is complete and satisfactory in all respects,
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***To my parents***

# ACKNOWLEDGEMENTS

First of all, I would like to express my tremendous and sincere thanks to my supervisor, my mentor, Professor Ki. I benefit really a lot from his free supervisory style. He always encourages me to think big, and do the research that I am much interested in. During my four years of PhD study under his guidance, I developed quite a lot in many aspects including but not limited to technical skills, research methodology and my personality. And he is always generous and supportive to me (and his other students) for conference, internship, exchange and many other opportunities. He is sometimes like a friend, and sometimes like a father to me. Without him, it won't be possible for me to achieve what I have done today.

I am also very grateful to Professor Patrick Yue as well. He had led me into another interesting (high frequency) research area, and had provided me the opportunities of using the advance processes. He also introduced me to the exciting industrial world by sharing his previous start-up experiences and taking me to the company trips. He and Prof. Ki are like my complementary supervisors who had significantly improved my efficiencies.

I would also like to thank Professor C. Y. Tsui for including me in his neuron stimulation project, which is also a very interesting and promising research topic. I enjoyed the trips to the University of Hong Kong for the lab rat experiments, which are conducted together with Prof. Ki, Prof. Tsui and my partner Xing Li.

I am sincerely grateful to Professor Pingbo Huang, Professor Philip K. T. Mok, Prof. C. Y. Tsui, Prof. Brian K. W. Mak and Prof. Danny H. K. TSANG for serving as my thesis examination committee, and Professor Seng Pan U for serving as my thesis external examiner, spending their invaluable time to read my thesis in details, and giving insightful comments for me to improve my thesis.

I'd like to give special thanks to Prof. Bram Nauta and Prof. Anne-Johan Annema for their guidance during my visit in their group at University of Twente.

I would like to thank my labmates and fellow students, for the technical and non-technical discussions, on- and off-campus activities, who had made the life of my PhD study delightful

and memorable. They are Dr. Jun Yi, Dr. Patrick Wu, Dr. Chenchang Zhan, Dr. Xiaocheng Jing, Dr. Vincent Chan, Dr. Edward Ho, Cheng Huang, Patrick Kwan, Oliver Lee, Erick Lai, Yonggen Liu, Xiaohao Hu, YK Teh, Lin Cheng, Fan Yang, Min Tan, Xing Li, Xun Liu, Lisong Li, Yuan Gao, Jungmoon Kim, Jiawei Zheng and Junmin Jiang of the Integrated Power Electronics Laboratory (IPEL); and Prof. Liang Wu, Prof. Rongxiang Wu, Dr. Li Sun, Alex Quan Pan, Robin Zhengxiong Hou, Yipeng Wang, Salahuddin Raju, and George Fengyu Che of the High-Speed Silicon Lab (HS2L); Dr. Bing Liu, Dr. Ruoyu Xu and Jing Guo of the MIXIC Lab; Haifeng Ma, Dawei Ye, Dr. Milad Darvishi, Saifullah Amir, Erik Olieman, Johan Withagen and Claudia Palattella of the ICD Group of UT. Special thanks go to Xiaocheng for everything. Special thanks go to Cheng Huang for teaching me photography, playing badminton with me, encouraging me on research. I am also grateful to Vincent Chan for leading me into the Marathon run.

I would also like to thank all the senior PhDs of IPEL, who had significantly contributed to IPEL and had setup an excellent standard for the younger students like me. They are Prof. Dongsheng Ma, Prof. Alex Leung, Prof. Hoi Lee, Dr. Hylas Lam, Dr. Scottie Man, Dr. Feng Su, Dr. Patrick Wu, Dr. Jun Yi, Dr. Chenchang Zhan, Dr. Edward Ho, Dr. Henry Kwong, Dr. Xiaocheng Jing, and Dr. Vincent Chan.

I’d like to thank my badminton friends at HKUST for the fun we had. They are Yuxuan Zhang, Dr. Yue Jia, Yuanyuan Wang, Dr. Jing Tang, and Dr. Ping Chen. The wins and losses of the matches released me from stress and tension in the university.

Last but not least, I would like to thank my parents for their endless love and unconditional supports.

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## ABSTRACT

Implantable microelectronic devices (IMDs), specifically the retinal/cochlear prostheses and the brain-machine interfaces, have gained great breakthroughs in the past decade. Sensations are restored for vision/hearing-impaired or spinal-cord injured people by these IMDs accordingly. Such devices require miniaturized form factor, real-time and high-efficiency wireless power transfer in the range of 10 to 100 mW. In this thesis, power management integrated circuits (PMIC) designed for IMDs are introduced in two parts: (1) wireless power acquisition and (2) regulation.

Inductively coupled (near-field) wireless power transfer is commonly used to power up the IMDs, for the reasons of high efficiency and low human tissue specific absorption rate (SAR) comparing to far-field power transmission. Three high-efficiency active rectifiers (AC-to-DC power converters) are designed, fabricated with standard 0.35 μm CMOS process, and measured with inductively coupled PCB air coils. The four diodes of a conventional passive rectifier are replaced by two cross-coupled PMOS transistors and two comparator-controlled NMOS switches to eliminate diode voltage drops such that high voltage conversion ratio could be achieved even at low AC input amplitude $|V_{AC}|$. The comparators are implemented with switched-offset biasing to compensate for the delays of active diodes and to eliminate multiple pulsing and reverse current. The first rectifier uses a CMOS peaking current source

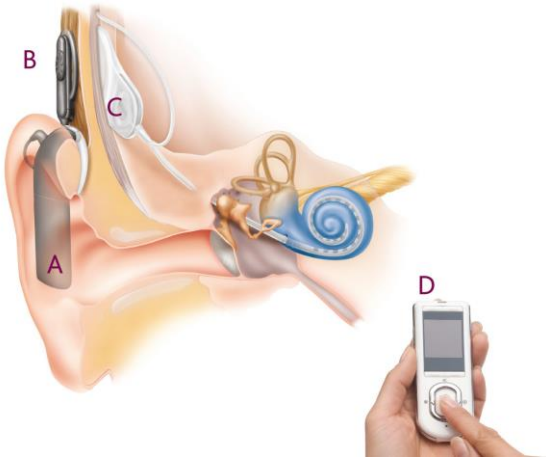
to obtain a bias current that is insensitive to the change in $|V_{AC}|$. The second and improved rectifier uses a modified CMOS peaking current source with bias current that is quasi-inversely proportional to the supply voltage (QIPV) to better control the reverse current over a wide AC input range (1.5 to 4 V). The third rectifier also employs the novel QIPV bias circuit, and is equipped with reconfigurable 1X or 2X modes for extended-range wireless power transmission. The active rectifiers process the converted magnetic power efficiently to DC electrical power, and constitute the input part of the PMICs for implants.

Since the coupled $|V_{AC}|$ may change by a couple of times due to relative movements (distance and/or orientation) between the primary and secondary coils, the rectifier DC output voltage would change substantially. Besides, different regulated supply voltages are needed for various functional blocks. For example, the microelectrode may need 2 to 10 V depending on the tissue impedance that is being stimulated; and 1 V is needed for digital and low-power circuits. To improve the overall efficiency, a novel dual-output charge pump (DOQP), consists of one step-down output and one step-up output with variable voltage conversion ratios, is inserted between the rectifier and the low-dropout (LDO) regulator. In addition to the charge pump, an ultra-fast response fully integrated LDO regulator with full spectrum power supply rejection is proposed to improve the performance of noise-sensitive building blocks, such as the RF receiver, the voltage and/or frequency references.

# Chapter 1 INTRODUCTION

## 1.1 Research Background

Implantable microelectronic devices (IMDs) have gained great breakthroughs in the past decade. Wirelessly powered cochlear implants have helped hearing-impaired people to restore hearing [1], [2], and retinal prostheses have also succeeded in clinical trials with partial vision restoration [3]-[7]. A successful product of the cochlear implant and a prototype of retinal prostheses are shown in Fig. 1.1. Moreover, there are increasing interests in brain-machine interfaces (BMIs), the diagrammatic sketch of which is shown in Fig. 1.2, due to the recent success in data acquisition from cortical microelectrodes, providing hope for patients with epilepsy, spinal-cord injuries, or Parkinson's disease [8], [9]. Implanted devices with functions such as neural recording and/or stimulation usually need power in the milli-Watt range or higher [1]-[9]. Therefore, biomedical implants with a highly-efficient wireless power transfer scheme that could deliver real-time power in the range of 10 to 100 mW with a small form factor are in great demand.



(a)

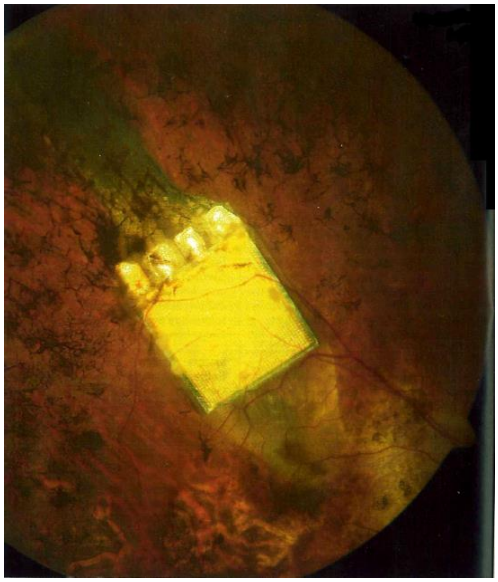

(b)

Fig. 1.1 (a) Cochlear implant [2] and (b) retinal prostheses [4].

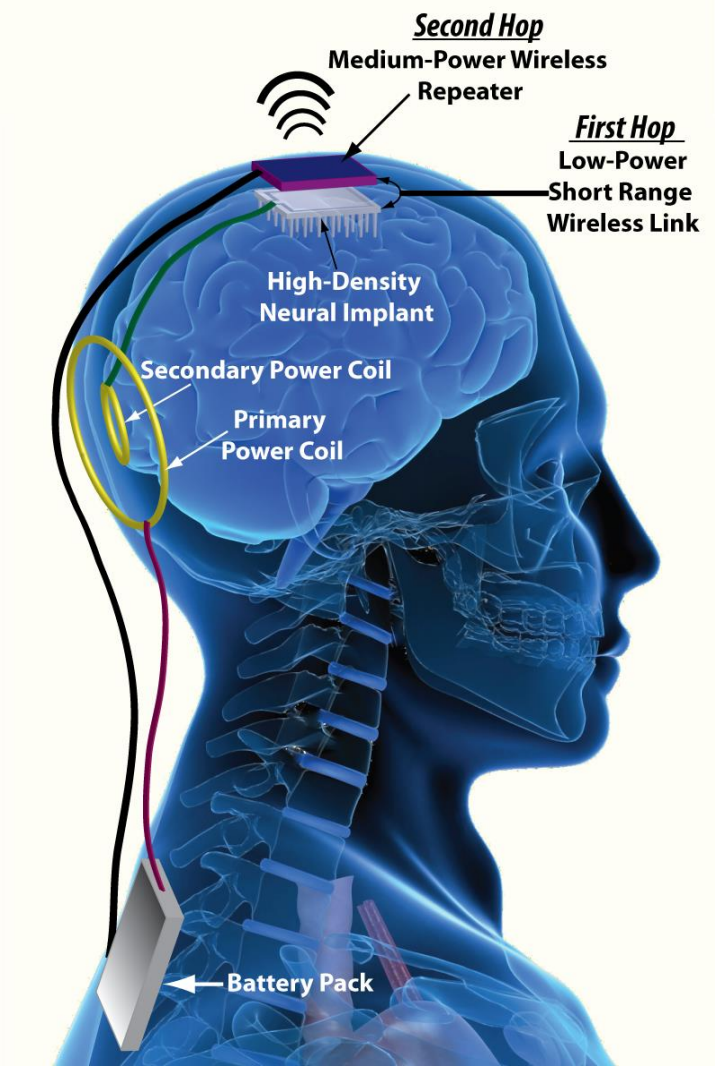



Fig. 1.2 Diagrammatic sketch of the BMI.

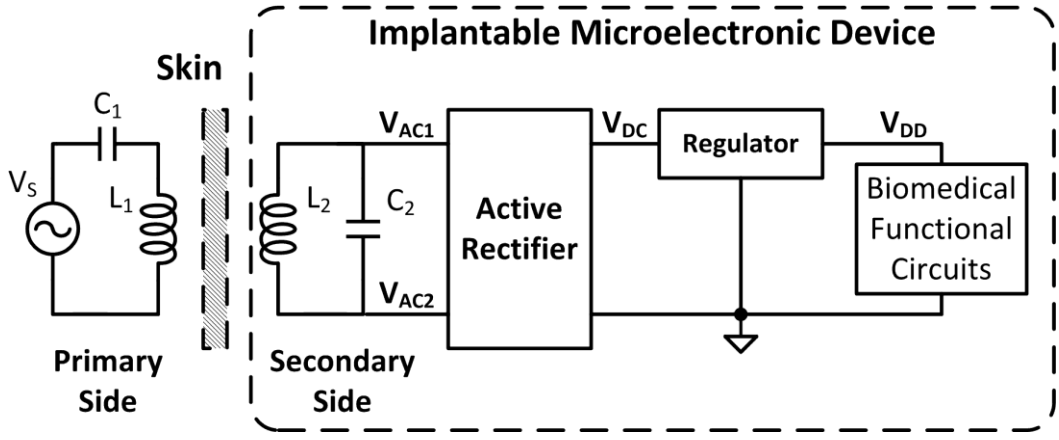



Fig. 1.3 A generic transcutaneous inductive power link for implantable devices.

Fig. 1.3 shows a generic transcutaneous inductively-coupled power transmission system for implants. Power is received from the secondary winding of the coupling coils, and the unregulated AC input voltage is converted by the rectifier to a DC voltage first, and then regulated to power up functional circuits such as neuron recording and/or stimulating channels as well as the RF transceiver. To achieve high overall system efficiency, every stage of the cascaded power management IC needs to be optimized, while the focus of this research is on the rectifier and the regulator.

## 1.2 System Requirements

The received power is dependent on the coupling coefficient *k* between the primary (external) coil and the secondary (internal) coil. Unfortunately, *k* varies significantly with the distance and orientation between these two coils. As a result, the active rectifier in Fig. 1.3 should be designed to accommodate a wide range of AC input amplitude [10], [20]-[23].

Besides, different regulated supply voltages are needed for various functional blocks. For example, the microelectrode may need 2 to 10 V depending on the tissue impedance that is being stimulated; and sub-1 V is needed for digital and low-power circuits. To realize these output voltages, switched-capacitor power converters (SCPC, a.k.a. charge pump, QP, Q stands for charge) with step-up and/or step-down capabilities are more commonly used in the IMDs than inductive switching converters, because on-chip capacitors can be more easily integrated that take full advantages of advanced processes when compared to (off-chip) inductors.

Since there are many noise-sensitive building blocks (such as the RF receiver, analog-to-digital converter, digital-to-analog converter, and voltage/frequency references) in an IMD, well regulated power supplies are needed, and traditionally linear regulators are used. However, the efficiency of a linear regulator is poor if there is a large difference between the supply voltage and the output voltage. To accomplish high overall power efficiency, the dropout voltage of the linear regulator should be kept low. Therefore, a low dropout (LDO) regulator should be used, and a fully-integrated LDO that can only have limited filtering capacitance should still provide good power supply rejection (PSR), as well as fast load and line transient responses.

From the system point of view, with these fully-integrated PMICs that require a few or no discrete components, the volume of the IMDs could be considerably shrunk, such that the IMDs could be more reliable and more easily implanted.

From the circuit perspective, state-of-the-art performances should be accomplished for each individual circuit: by operating at 13.56 MHz, both the input tuning capacitors and the output filtering capacitors are expected to be integrated on-chip; the dual-output charge pump is expected to effectively convert the rectified voltage into two or more supply voltages for different functional blocks in the IMDs; and the on-chip LDO should provide a well-regulated voltage with full-spectrum PSR to supply power to noise-sensitive blocks, and response fast to the load transient current with limited load capacitance.

In a nutshell, this research is targeted as designing, implementing and measuring innovative, area-efficient and high efficiency power management integrated circuits, including AC-to-DC converter, switched-capacitor power converter and low dropout regulators for biomedical implantable devices.

### 1.3 Operation Frequency

Wireless power transfer systems can be divided into two categories according to transmission modes of near-field and far-field operations. As shown in Fig. 1.4, the near-field operation assumes that the transmission distance is much smaller than the wavelength, that is, $d << \lambda$; while the far-field operation has the wavelength being much smaller than the transmission distance, that is, $\lambda << d$.

In selecting the frequency for the wireless power link operating in the near-field condition (also known as the inductively-coupled condition), that is, the distance between the coils is much smaller than the wavelength $\lambda$, suggestions of 1 to 3 MHz are common [3], [10] as power attenuation through human tissue increases at higher frequencies. However, switching at high frequency could reduce the volume of the resonance *LC* tank and the output filtering capacitor such that the whole implant could be integrated on-chip or on-package. Besides, smaller inductance with higher *Q* can be more easily achieved at higher frequencies within

limited space, and this is one of the key factors in improving the overall efficiency of the wireless power transfer system. An additional advantage is that the data coil could be eliminated by transmitting the uplink data through the power link using time interleaving if the wireless power transmission frequency is sufficiently high to achieve the required data rate. In this research, we choose 13.56 MHz in the readily available ISM band. Although 13.56 MHz is on the high side of the frequencies that have been conventionally adopted for inductively-coupled power transmission, the specific absorption rate (SAR) in the tissue is still quite low compared to the thermal power dissipation in the coils [11].

For far-field power transmission, the output power level is limited as the coil distance is larger (in other words, the coil diameter is smaller), making it more difficult for the EM wave to be focused and transmitted from the transmitting antenna to the receiving loop antenna efficiently. For example, the wireless power link in [12] uses 915 MHz that operates at the boundary of near-field and far-field transmission in delivering a few hundred micro-watt.

As a comparison, applications such as wireless mobile phone charger uses 6.78 MHz or 13.56 MHz for fast loop response to the load transient [13], [14]; and [15] operates at 6.78 and 13.56 MHz uses coils with magnetic core to increase the power transfer efficiency by 3 times; however, the magnetic core is heavy and not suitable for implantable devices; and ~150 kHz that is compliant with IEEE Qi standard [16] is used for higher power conversion efficiency [17]; and 900MHz is often used in long distance RFID applications [18].

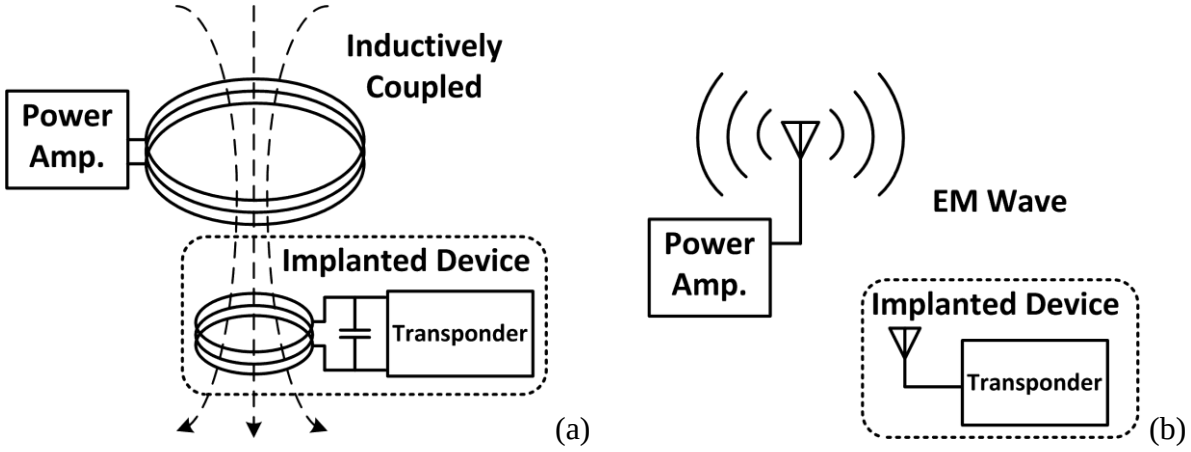



Fig. 1.4 Wireless power transfer systems with (a) near-field or (b) far-field operation, respectively.

The selection of the operation frequency is a tradeoff between efficiency, device volume and power level as shown in Fig. 1.5. Our target output power is in the tens of mW range with air coils, and taking the above factors into consideration, we decided to use 13.56 MHz with near-field coupling.

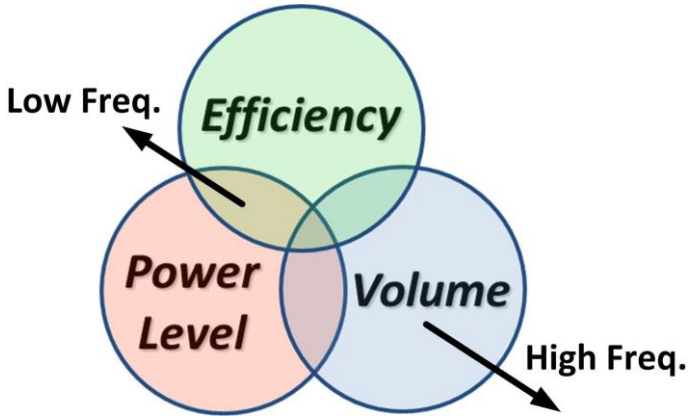



Fig. 1.5 Tradeoffs in selecting the operation frequency.

### 1.4 Conclusion

Wireless power transfer has many applications such as implantable medical devices (IMDs), RFIDs, and electric vehicle and mobile phone wireless chargers. In this research, wireless power transfer for the first application is investigated. This research faces many design challenges, especially a miniature size is required. The operation frequency is chosen to be 13.56 MHz with near-field operation for good tradeoffs among efficiency, device volume and power level in this specified case.

# Chapter 2 RECTIFIER: FROM PASSIVE TO ACTIVE

## 2.1 Passive Rectifier

Diode, the simplest semiconductor device, can be easily used to convert AC voltage into DC voltage as shown in Fig. 2.1. The half-wave rectifier delivers current from the sinusoidal AC source to the DC output when the positive amplitude is higher than the DC output voltage; while the full-wave rectifier delivers current to the output at both positive and negative peak points. That means the time interval for charge transfer of a half-wave rectifier is only half of that of a full-wave rectifier. Thus, in delivering the same load current with the same output capacitor, the output ripple of the half-wave rectifier is basically two times higher than that of the full-wave rectifier.

In standard CMOS processes, the diodes can be replaced by diode-connected MOS transistors. This is a cost-effective way to implement the passive rectifier [10]. However, the transconductance $g_m$ of the MOS transistors is smaller than the $g_m$ of a real PN junction diode [19]. This requires a large $V_{GS}$ for MOS transistors when driving a large current, which means that it is less efficient when compared to using diodes. If low-threshold voltage transistors are used to reduce the $V_{GS}$, reverse (sub-threshold) leakage current would increase accordingly.

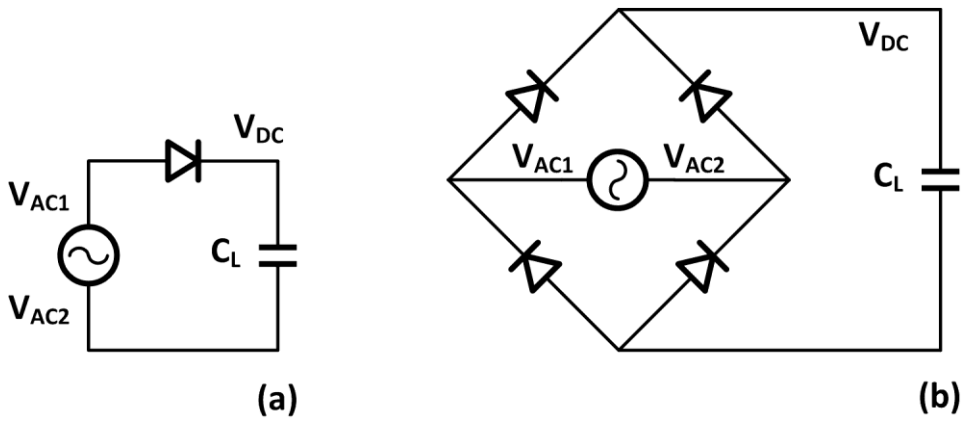



Fig. 2.1 (a) Half-wave rectifier, and (b) full-wave rectifier

## 2.2 Active Rectification for IMDs

The diode voltage drop ($V_{diode} \approx 0.7$ V) of a passive rectifier, as shown in Fig. 2.2(a), limits the voltage conversion ratio ($M$) and the power conversion efficiency (PCE). The full-wave active rectifier shown in Fig. 2.2(b), of which the upper diodes are replaced by two cross-coupled PMOS switches and the lower diodes by two comparator-controlled NMOS switches (active diodes), reduces the voltage drop from $2V_{diode}$ to $2V_{DS}$ ($V_{DS}$ is the turn-on voltage of the power switches). When operating at a high frequency such as 13.56 MHz, comparator delay and gate-drive buffer delay affect the efficiency of the rectifier, as reverse current will occur if large power switches are not turned off correctly. Many schemes were proposed to tackle the above problems [20]-[25].

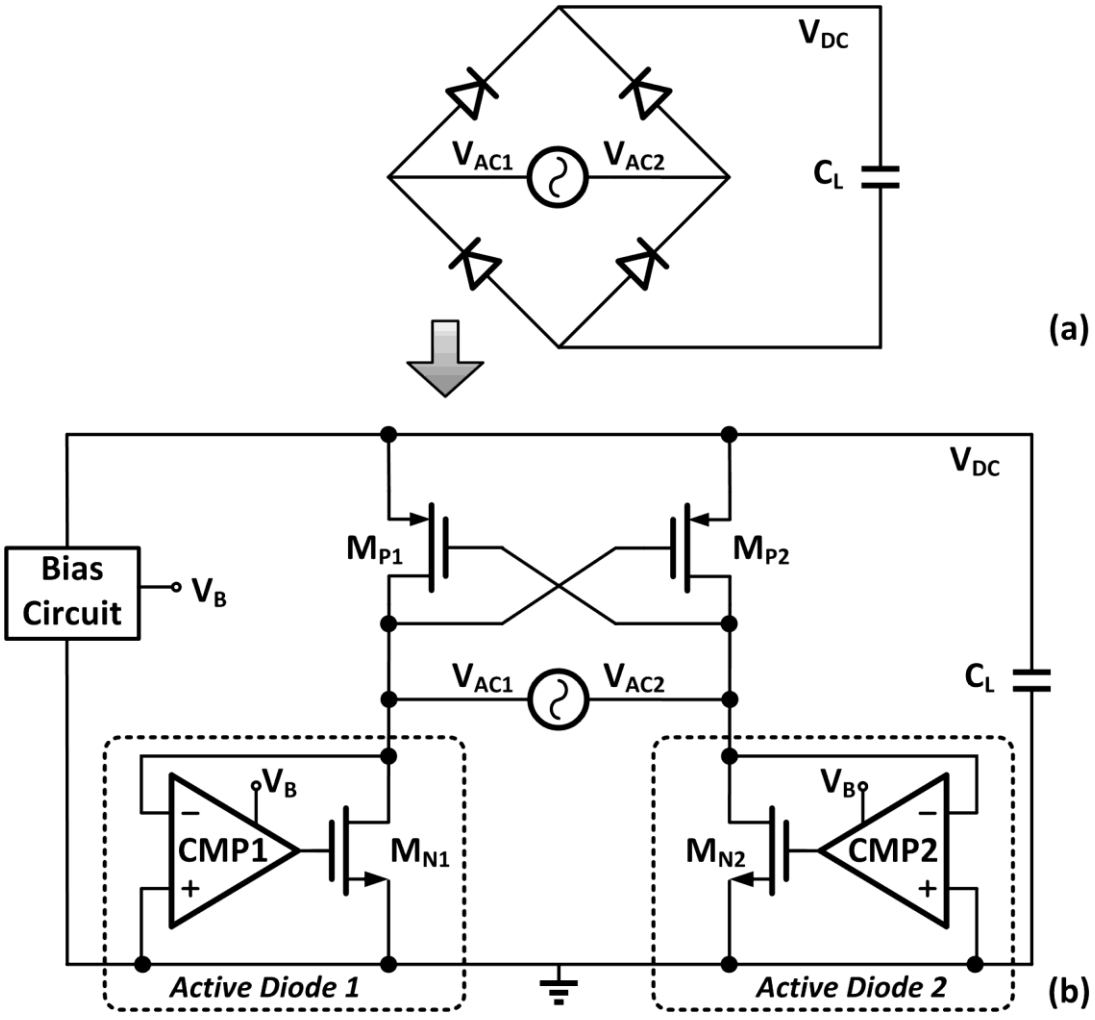



Fig. 2.2 (a) The passive full-wave rectifier, and (b) the active full-wave rectifier.

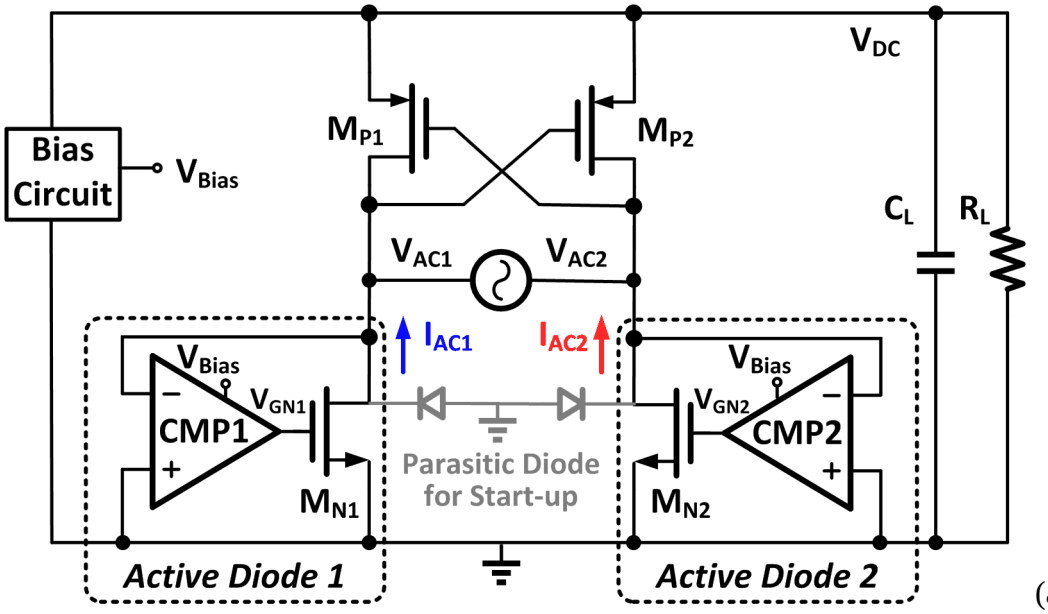
### 2.2.1 Operation Principle and Problems of Active Rectifiers

An important parameter in evaluating a full-wave rectifier is the voltage conversion ratio M, defined as

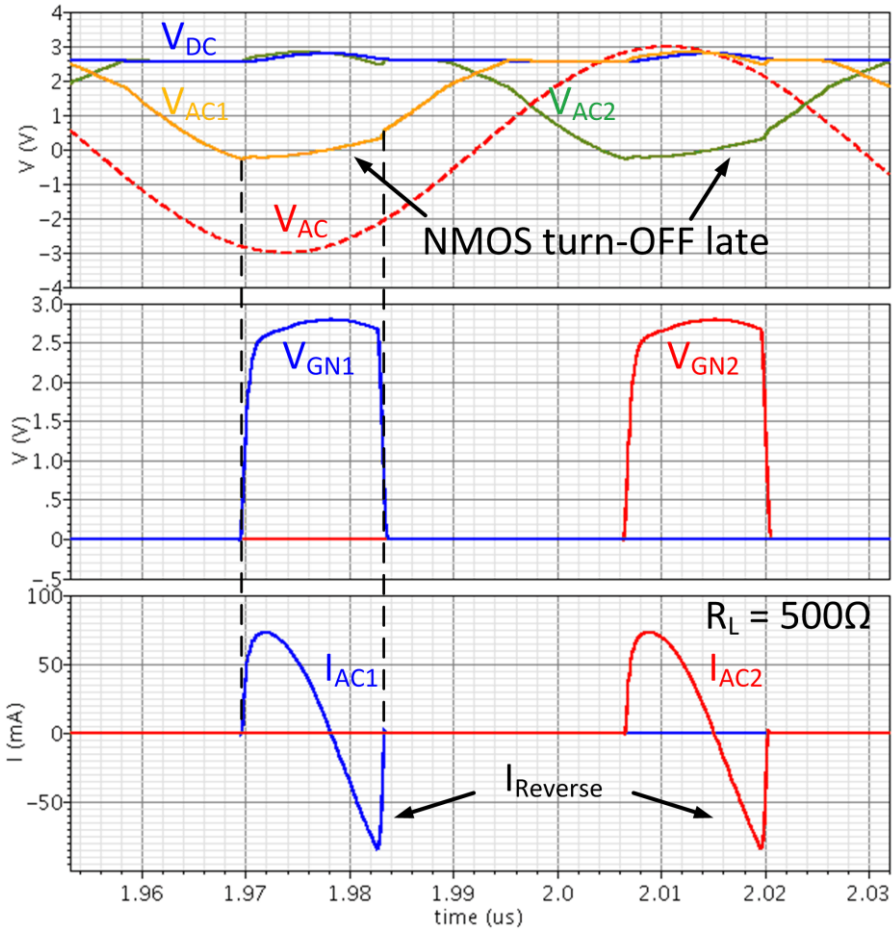
$$M = \frac{V_{DC}}{|V_{AC}|} \tag{2.1}$$

where $|V_{AC}|$ is the amplitude of the input AC signal to the rectifier, and $V_{DC}$ is the averaged rectified output DC voltage. By replacing the four diodes of a full-wave rectifier with power transistors, $M$ is significantly increased even when the input amplitude is low. The generic active rectifier, shown in Fig. 2.2(b), consists of an $LC$ tank, cross-coupled PMOS transistors, comparator controlled NMOS switches (active diodes), a bias current generator and an output filtering capacitor $C_L$. The operation principle is demonstrated by the simulated waveforms shown in Fig. 2.3, as follows. When $V_{AC2} - V_{AC1} > |V_{tP}|$ (threshold voltage of $M_{P1,2}$), $M_{P2}$ is turned on; and when $V_{AC1}$ swings below 0 V, the comparator CMP1 turns on the switch $M_{N1}$, charging up $V_{DC}$ by $V_{AC}$. After $V_{AC1}$ swings above zero, $M_{N1}$ is then turned off by CMP1. During the next half of the AC input cycle, the other half of the rectification circuit will conduct in a similar fashion as described above.

With proper control of the power switches, a high voltage conversion ratio could be obtained. However, in reality, the delay time $t_{delay}$ of the comparator and the gate drive buffer will limit the dynamic performance. The propagation delay of the rising edge of the comparator $t_{pLH}$ will shorten the current conduction time $\Delta t$, limiting the highest operation frequency of the active rectifier. On the other hand, $t_{pHL}$ of the output falling edge forces the power NMOS transistors $M_{N1,2}$ to turn off late, and charge of the output capacitor will flow back to ground through $M_{N1,2}$, resulting in reverse leakage current $I_{leak}$ as shown in Fig. 2.3. This is the main challenge of active rectifier designs [20], [21]. To eliminate $I_{leak}$, power transistors $M_{N1,2}$ have to be turned off immediately when $V_{AC}$ goes below $V_{DC}$. However, $M_{N1,2}$ have to be large to handle a large output current, increasing the response times of the active diodes. This problem is more pronounced when the operation frequency is required to be high and the input amplitude $|V_{AC}|$ is low (for example, below 1.5 V) because delay times of comparators and buffers are inversely proportional to the supply voltage.




(a)




(b)

Fig. 2.3 (a) The active full-wave rectifier, and (b) its simulated waveforms of reverse current problem in active rectifier.

### 2.2.2 Comparison of Comparator Delay Compensation Schemes

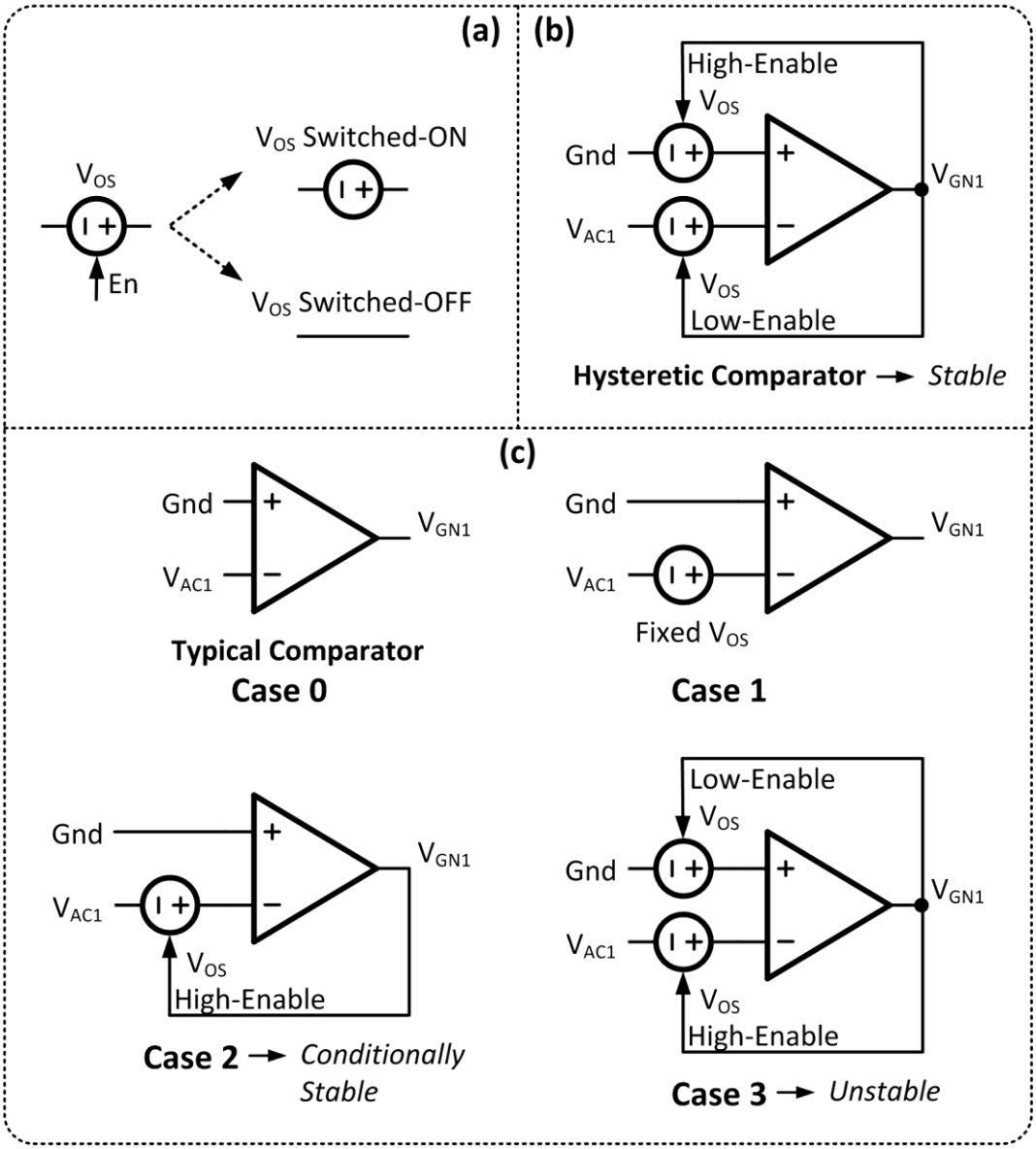



Fig. 2.4 (a) Symbol of artificial switched-offset; (b) hysteretic comparator; and (c) comparator schemes for reverse current control.

To achieve a higher voltage conversion ratio and PCE, the power transistors $M_{N1,2}$ should be turned off right before reverse current occurs [20]-[26]. Comparators with unbalanced bias currents or asymmetric differential input are used to set an artificial input offset voltage to compensate for the delay and to turn the power switches on and off properly. The symbol of artificial input offset with an enable pin is shown in Fig. 2.4(a). When the enable bit is high, a non-zero offset voltage is introduced to the comparator; and when the enable bit is low, the

offset voltage is zero (a wire). Prior reverse current control schemes fall into one of the cases sketched in Fig. 2.4(b). Case 0: the comparators have no artificial offset (reverse current occurs due to delays). Case 1: The comparators have fixed artificial offset such that the power switches are turned off earlier, but turned on later. Case 2: The comparators have dynamic artificial offset such that the power switches are only turned off earlier. Case 3: The comparators have dynamic artificial offset at both edges such that the power switches are turned on and off earlier.

To compare the performance of the above comparator schemes on especially low-voltage active rectifiers, the quantity Crest Factor (CF) used in evaluating electrical appliances is employed. CF is the ratio between the peak current delivered to the load and the corresponding RMS current

$$\mathrm{CF} = \frac{I_{\mathrm{p}}}{I_{\mathrm{RMS}}}. \tag{2.2}$$

A higher CF means a higher peak current for the same load condition, and larger power transistors are thus needed to reduce the $V_{\mathrm{DS}}$ for achieving high voltage conversion ratios. Routing metal needs to be wider for a higher CF as well.

The scenarios of current conduction of Case 0 to Case 3 are sketched in Fig. 2.5 and discussed as follows. Case 1 is implemented in [21] and [25], with constant offset introduced to the comparators using unbalanced bias currents [21] or asymmetrical differential input transistors [25]. The power NMOS switches are turned off earlier by $t_{\mathrm{delay}}$ to eliminate the reverse current; however, they are turned on later by $2t_{\mathrm{delay}}$ than the ideal case, and the conduction time $\Delta t_1$ is $2t_{\mathrm{delay}}$ shorter. For the same load current, the peak current $I_{\mathrm{p1}}$ has to be higher, limiting its operation at a higher frequency. The delays get worse when $|V_{AC}|$ is low. Moreover, the simple bias circuit that determines $t_{\mathrm{delay}}$ is strongly affected by $|V_{\mathrm{AC}}|$.

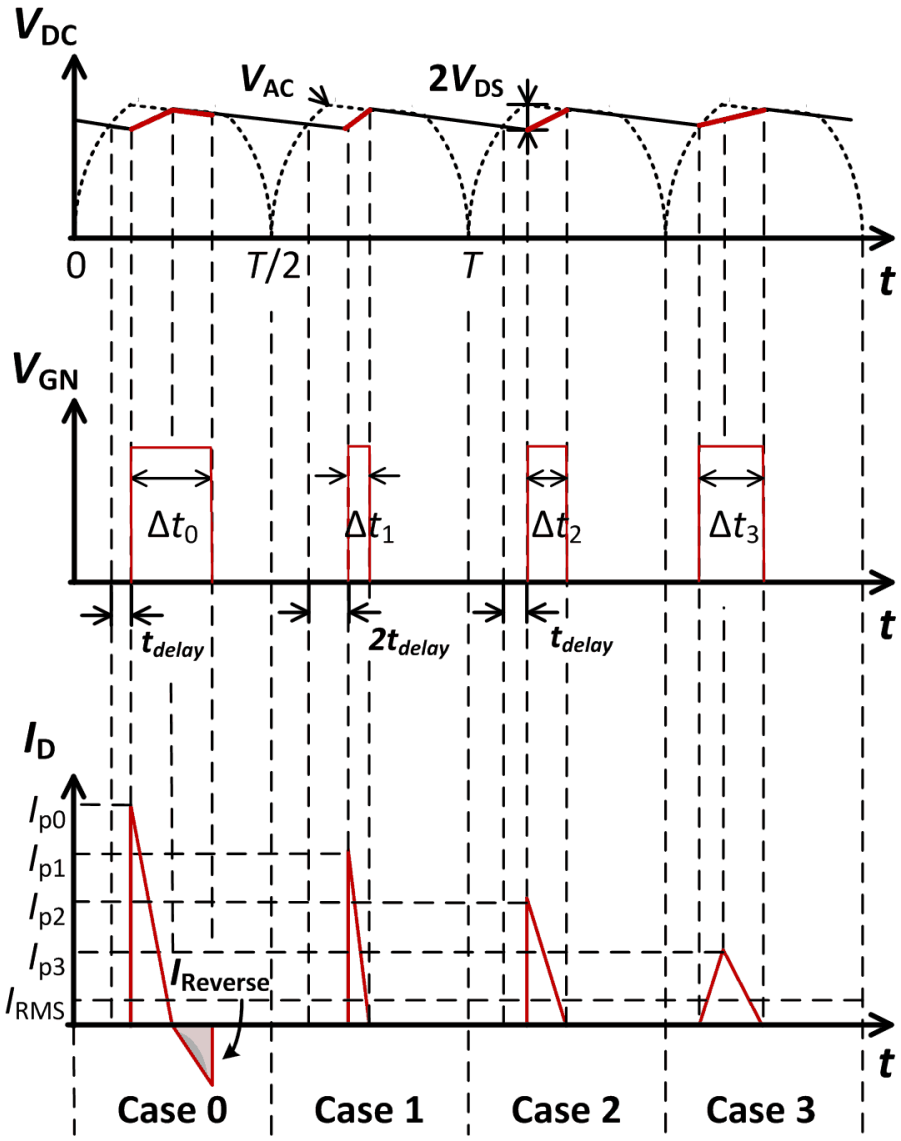



Fig. 2.5 Conceptual waveforms of the input/output voltages, power NMOS gate voltage and conducted currents for active rectifiers with different comparators.

In [20], self-biased active diodes are employed, and to reduce or eliminate $t_{delay}$, a reverse current control (RCC) scheme (Case 2) is introduced. However, both the bias current and the operation of the RCC transistor are highly affected by $|V_{AC}|$ and process variations, making the rectifier hard to be optimized over a wide input range. Moreover, as the reverse current control is realized by a time-varying offset, the artificial offset would disappear right after the power NMOS transistor is turned off. If the RCC transistor turns on prematurely (for example, due to process variations) and turns off the active diode while $|V_{AC}|$ is still higher than $V_{DC}$, the comparator will go high again in the same cycle. Simulation waveforms of the described

scenario are shown in Fig. 2.6. The efficiency would deteriorate with this multiple pulsing problem, especially in light load condition when switching loss dominates.

Case 3 is realized in [23] and [24], where it uses self-biased active diodes similar to [20], with an offset-control function for the comparators to compensate for both turn-on and turn-off delays such that $\Delta t_3$ could be maximized (lowest CF). It suffers from the same and even worse multiple-pulsing problem as [20], as the dynamic offset (+/– offset voltages) transition of the offset-control circuit is unstable: when the comparator outputs a 1(0), the dynamic offset flips the output to 0(1), and this positive feedback makes the comparator undergoes self-oscillation. This phenomenon is what a Schmitt trigger designed to avoid. To make the scheme work, [23] adds a delay cell in the offset-control path in addition to its calibration bits. If the delay time $t_{dp}$ is large enough (comparable to half period), the comparator could be stable, but then the power switch would be turned on for at least the duration of $t_{dp}$ that limits the minimum conduction time ($\Delta t_{min} > t_{dp}$). This property makes its operation more like a constant-on time control at light load condition. As a result, its light load efficiency is degraded.

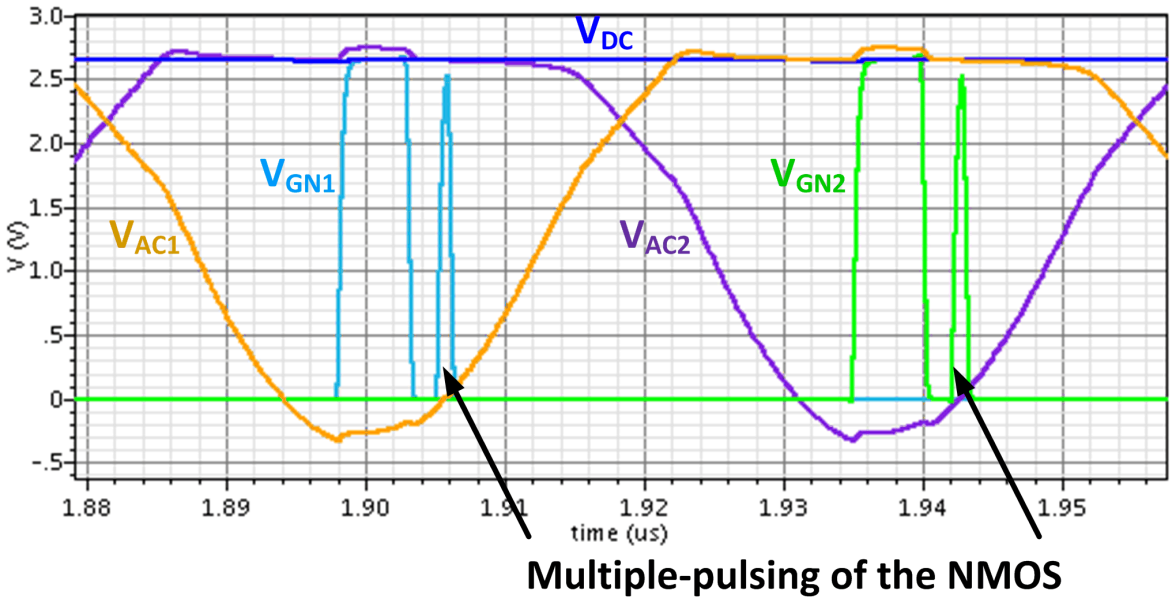



Fig. 2.6 Simulated waveforms of multiple-pulsing problem associated with dynamic offset schemes.

To summarize, Case 2 has larger $\Delta t$ than Case 1, and in the ideal situation, Case 3 has the largest $\Delta t$. However, a comparator with both compensated turn-on and turn-off delays is

logically unstable: the hysteresis goes the opposite direction as a normal Schmitt trigger goes, and the robustness of the rectifier is degraded. In our proposed works ([22] and [26]), Case 2 is employed. It has a longer $\Delta t$ compared to Case 1, and is more robust compared to Case 3.

### 2.2.3 Delay Time of Active Diodes

Before discussing the current source to be used to bias CMP1 and CMP2, the delay time of the active diode $t_{d,AD}$ should be investigated first. The parameter $t_{d,AD}$ consists of the comparator delay $t_{d,C}$ and the gate drive buffer delay $t_{d,B}$. To simplify the calculation, as shown in Fig. 2.7, the supply voltage of a typical comparator and buffer is connected to $V_{DC}$ that is AC input dependent, and the input signal is assumed to be sinusoidal, that is, $V_{in}(t) = \alpha|V_{AC}|\times\sin(2\pi t/T)$, where $\alpha$ is a scaling factor. Let the trigger point of the inverter buffer be the 50% point of $V_{DC}$, that is, $M|V_{AC}|/2$ ($M$ = 0.9). Using the small-signal model, the output current $I_{CD}(t)$ that charge/discharge the output capacitor $C_{OUT}$ is

$$I_{CD}(t) = g_m V_{in}(t) = g_m \alpha |V_{AC}| \sin(2\pi t/T) \tag{2.3}$$

where $g_m$ is the transconductance of the comparator input stage. The comparator delay $t_{d,C}$ is the time that $I_{CD}(t)$ charges the capacitor $C_{OUT}$ by $V_{DC}/2$:

$$\begin{aligned} \int_0^{t_{d,c}} I_{CD}(t)\,dt &= \int_0^{t_{d,c}} g_m \alpha |V_{AC}| \sin(2\pi t/T)\,dt \\ &= C_{OUT} V_{DC}/2 = C_{OUT} M |V_{AC}|/2 \end{aligned} \tag{2.4}$$

For $t << T$, $\sin(2\pi t/T) \approx 2\pi t/T$, and we have

$$\tfrac{1}{2} g_m \alpha |V_{AC}| 2\pi t_{d,C}^2 / T = C_{OUT} M |V_{AC}|/2 . \tag{2.5}$$

Therefore,

$$t_{d,C} = \sqrt{\frac{MC_{OUT}T}{2\pi\alpha g_m}} = \sqrt{\frac{MC_{OUT}T}{2\pi\alpha\sqrt{2I_B k_n (W/L)}}} . \tag{2.6}$$

From (2.6) we have $t_{d,c} \propto \sqrt[4]{1/I_B}$ . If $I_B$ is independent of $V_{DC}$, then so does $t_{d,C}$. The simulated $t_{d,C}$ of Fig. 2.7 is plotted in Fig. 2.8, which verified the above calculations that $t_{d,C}$ has a very weak relation with $I_B$. However, all the previous bias current generation circuits would provide an $I_B$ that is more or less proportional to $V_{DC}$, in such a case

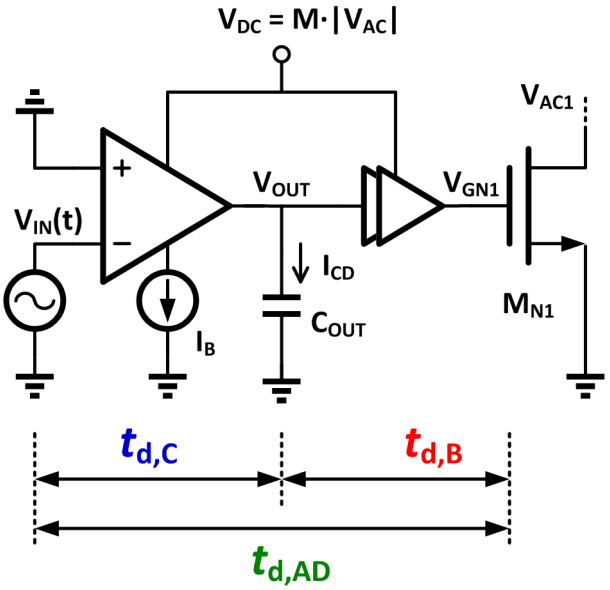



Fig. 2.7 Simplified schematic of active diode 1 with emphasis on supply voltage, input signal and load capacitor for delay calculations.

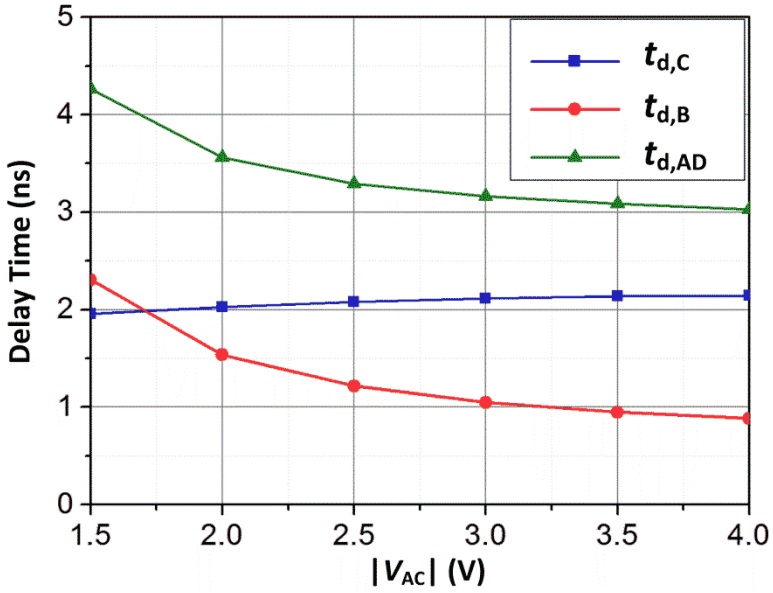



Fig. 2.8 Simulated active diode delay $t_{d,AD}$, comparator delay $t_{d,C}$ and gate drive buffer delay $t_{d,B}$ with respect to $|V_{AC}|$.

$$t_{d,C} \propto \sqrt[4]{1/I_B} \propto \sqrt[4]{1/|V_{AC}|}\,. \qquad (2.7)$$

On the other hand, the buffer delay $t_{d,B}$ would change inversely proportional to the supply voltage, according to the calculated propagation delay (the time to reach the 50% point) of an inverter [27]:

$$t_P = 0.69\frac{3}{4}\frac{C_L V_{DC}}{I_{DS}}\left(1-\frac{7}{9}\lambda V_{DC}\right)$$
$$= 0.52\frac{C_L V_{DC}(1-\frac{7}{9}\lambda V_{DC})}{k'(W/L)V_{DSsat}(V_{DC}-V_t-V_{DSsat}/2)} \quad (2.8)$$

where $I_{DS}$ is the drain current, $k' = \mu C_{ox}$, and $\lambda$ is the channel-length modulation factor. Assuming that $V_{DC} - V_t >> V_{DSsat}/2$ and $\lambda = 0$, (2.8) can be written as

$$t_P = t_{d,B} = 0.52\frac{C_L}{k'(W/L)(V_{DC}-V_t)}. \quad (2.9)$$

From the above first-order approximation, we learn that $t_{d,B}$ is approximately inversely proportional to the supply voltage. Consequently, to keep $t_{d,B}$ approximately constant we need an adaptive current source that is approximately inversely proportional to $V_{DC}$.

### 2.3 Conclusion

Active rectifiers are widely used in low-voltage AC-to-DC power conversion to achieve higher voltage conversion ratio and power conversion efficiency. However, active rectifiers also suffer from active-diode delay problem that would introduce reverse current and consequently degrade the efficiency. Delay times of active diodes are calculated and simulated in this research, and the total delay time shows an inverse relationship with the power supply. Different comparator delay compensation schemes were proposed to solve this problem, but each scheme has their pros and cons as discussed in this section. Circuit implementations of the comparator and the bias current designed to fix the above problems will be given in the following chapter.

# Chapter 3 ACTIVE RECTIFIER IMPLEMENTATIONS

Two full-wave active rectifiers (labeled as Rec1 and Rec2, respectively) are proposed, implemented and measured in a 0.35 μm CMOS N-well process in this research. Both of them are using delay time compensated comparators with the proposed switched-offset scheme. The two designs used different bias current sources, with the second being an improved version over the first. The first one (Rec1) [22] used a peaking current source, while the second one (Rec2) [26] used a proposed quasi-inversely proportional to $V_{DC}$ (QIPV) current source. Detailed analysis, optimization and measurement results will be presented in this chapter.

## 3.1 Comparator with Switched-Offset

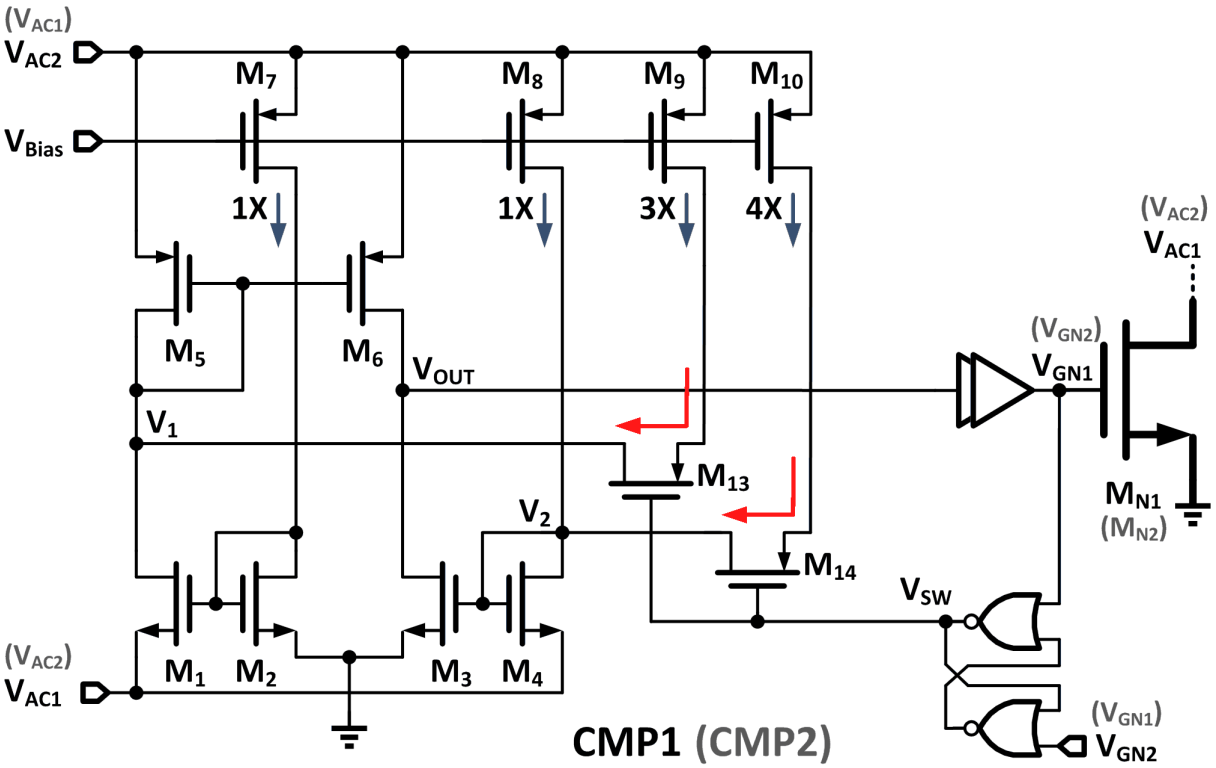



Fig. 3.1 The proposed delay time compensated comparator with switched-offset scheme (Active Diode 1(2) in Fig. 2.3).

In our proposed switched-offset scheme, delay time compensation is realized by comparators with time-varying offset voltages associated with a specially designed current source, as shown in Fig. 3.1. The two comparators CMP1 and CMP2 are push-pull differential common-gate comparators, and the dynamic switched currents are also implemented in a push-pull fashion, for minimizing power consumption and also for reducing the comparator response time [21]. When $V_{AC2} - V_{AC1} > |V_{tP}|$, $M_{P2}$ is turned on. When $V_{AC1}$ swings below 0 V, $M_1$ of CMP1 sinks a larger current than $M_2$, causing $M_6$ to source a larger current than $M_3$ can sink, thus driving $V_{OUT}$ as well as $V_{GN1}$ high and turns on the active diode switch $M_{N1}$. As a result, the rectifier filtering capacitor $C_L$ is charged up by $V_{AC}$. Note that in the previous phase, $V_{GN2}$ has been high, causing $V_{SW}$ of CMP1 to be high, and the switches $M_{11}$ and $M_{12}$ are turned off. In the present phase, $V_{GN1}$ drives $V_{SW}$ low and turns on $M_{11}$ and $M_{12}$, allowing auxiliary bias currents from $M_9$ and $M_{10}$ to introduce the designed DC offset. This offset voltage of the differential pairs with unbalanced bias currents is

$$V_{OS} = \sqrt{\frac{2I_+}{k_n (W/L)}} - \sqrt{\frac{2I_-}{k_n (W/L)}}$$

$$= \left(\sqrt{n} - 1\right) \sqrt{\frac{2I_-}{k_n (W/L)}} = \left(\sqrt{n} - 1\right) V_{OV-}, \qquad (3.1)$$

where $k_n = \mu_n C_{ox}$, $I_+$ and $I_-$ are the unbalanced bias currents, n is the ratio of $I_+$ and $I_-$, and $V_{OV-}$ is the gate overdrive voltage of $M_1$ through $M_4$ when they are operating with balanced bias current (1X). The sizes of the common-gate input pairs $M_1$ through $M_4$ are the same, with $V_{OV-}$ lower than 100 mV. The bodies of $M_1$ through $M_4$ are all connected to the on-chip ground, such that the threshold voltage $V_{tN}$ of $M_1$ and $M_4$ would be smaller than $V_{tN}$ of $M_2$ and $M_3$ when $V_{AC1} < 0$ due to the body effect. The bias currents of $M_7$ through $M_{10}$ are 1X, 1X, 3X and 4X respectively. The current of $M_{10}$ should be 3X (same as $M_9$); however, taking the body effect of $M_4$ into consideration, it is set as 4X instead to make $V_2$ even higher. The current ratio n is equal to four in our case, and the value of the dynamic artificial offset (around 100 mV) is set by the current ratios of $M_7$ through $M_{10}$. The auxiliary bias currents also serve as slew-rate enhancement currents that charge up $V_1$ and $V_2$, starving $M_6$ and feeding $M_1$. Hence, $V_{OUT}$ is pulled low, turning off the power switch $M_{N1}$ right before $V_{AC1} > 0$ to prevent the occurrence of reverse current. A NOR SR-latch is added at each output of the

comparators to avoid the aforementioned multiple-pulsing problem that is caused by the dynamic offset scheme. Due to the NOR implementation of the SR-latch, $V_{SW}$ stays low even when $V_{GN1}$ goes low, such that $M_1$ and $M_4$ are saturated by the auxiliary bias currents, and prevent $M_{N1}$ from turning on again in the same phase even if $V_{AC1}$ is still lower than 0 V, thus eliminating multiple-pulsing.

To save static power, the power supplies of the comparators CMP1 and CMP2 are connected to (the distorted sinusoidal waveforms) $V_{AC2}$ and $V_{AC1}$, respectively, such that only one comparator is biased to work in every phase [20]. In addition, the $V_{OUT}$ node of the comparators is coupled to ground in the layout, to make sure that this high-impedance node would not jump when the supply ($V_{AC2}$ or $V_{AC1}$) is low. However, to eliminate multiple pulsing, the power supply of the gate drive buffers and the latches should be connected to the DC output $V_{DC}$. All N-wells are connected to $V_{DC}$. Some PN junctions (P+ active area to N-well) are slightly forward biased by $V_{AC2} - V_{DC}$ (or $V_{AC1} - V_{DC}$, equal to $V_{DS}$ of the power PMOS that is approximately 70 mV), the associated leakage current is negligible. When $V_{AC2}$ or $V_{AC1}$ is slightly higher than $V_{DC}$ during the conduction time, the matched currents of $M_7$ through $M_{10}$ would be larger than the designed bias current with larger $V_{GS}$. This arrangement is good for the comparators to have more instantaneous current and faster response.

### 3.2 Current Source Design

For a robust design, the bias circuit of the active rectifier should not require a startup circuit, as this is the frond-end of the wireless power receiver. As shown in Fig. 3.2, in [21], [24], a simple current source with a diode-connected MOS transistor driving a resistor is used; and in [20], [23] and [25], self-biased current sources are used. The above schemes give the bias current approximately proportional to the input voltage amplitude $|V_{AC}|$. In [22], a peaking current source (PCS) with all transistors operating in the saturation region [28] is used to bias the comparators so that the bias current would stay approximately constant when $|V_{AC}|$ changes. However, for a constant $t_{d,AD}$, the bias current should be approximately inversely proportional to $|V_{AC}|$. In the proposed design [26], to further improve the performance at low $|V_{AC}|$, the bias current is set quasi-inversely proportional to $|V_{AC}|$ ($\approx V_{DC}$), labeled as QIPV biasing and shown in Fig. 3.3(b), such that the comparator offset could be well controlled over the whole AC input range.

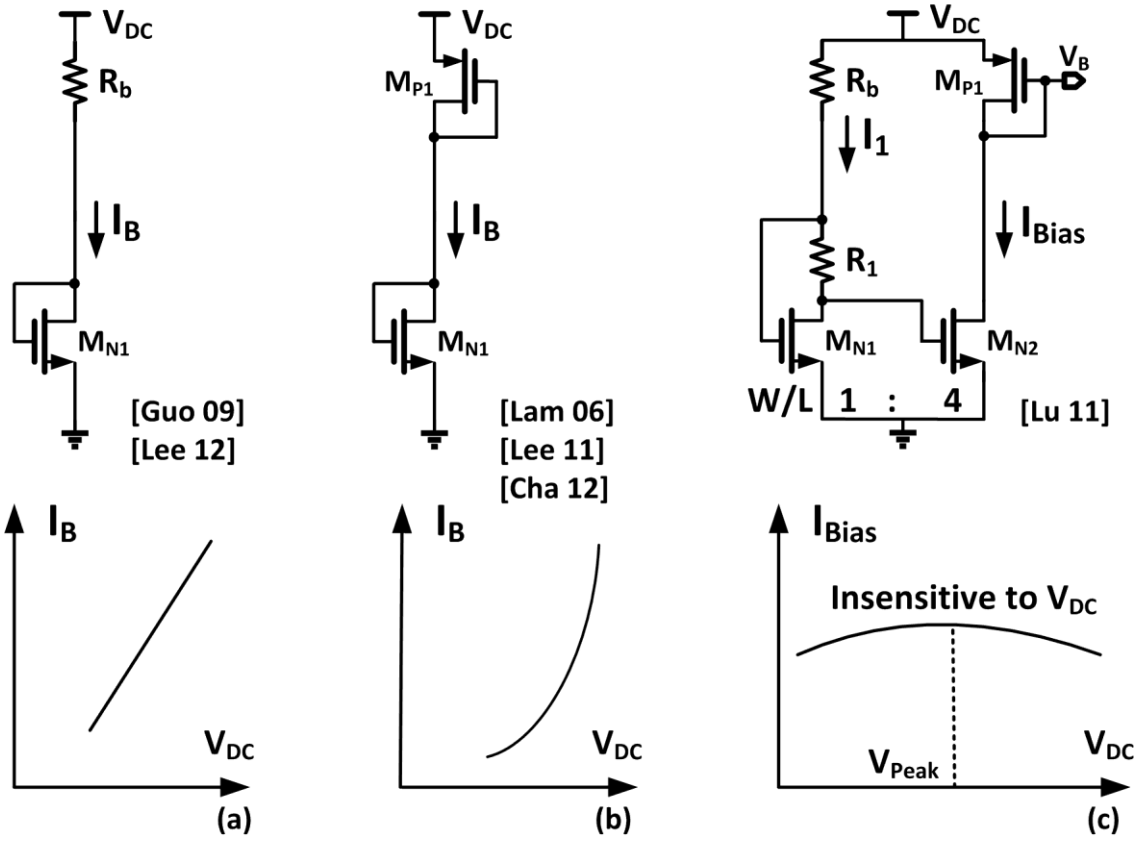



Fig. 3.2 Bias circuits without start-up requirement.

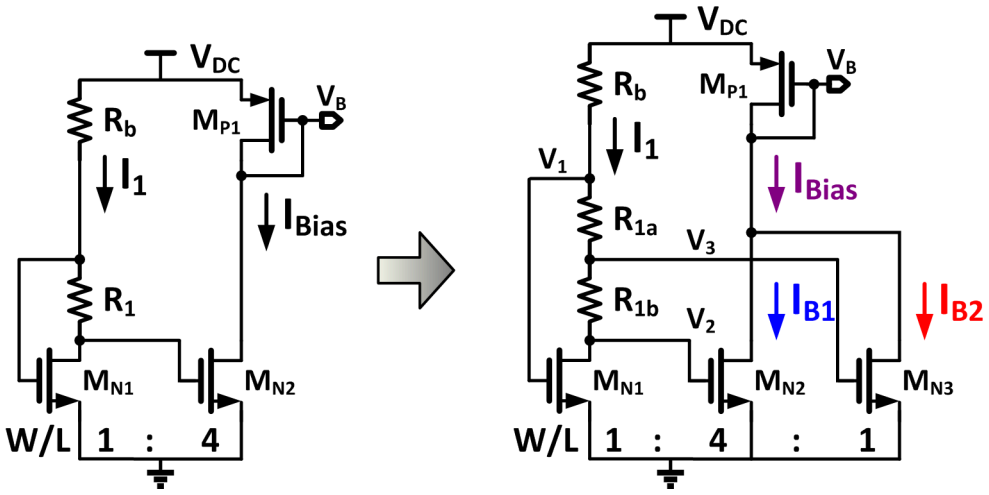
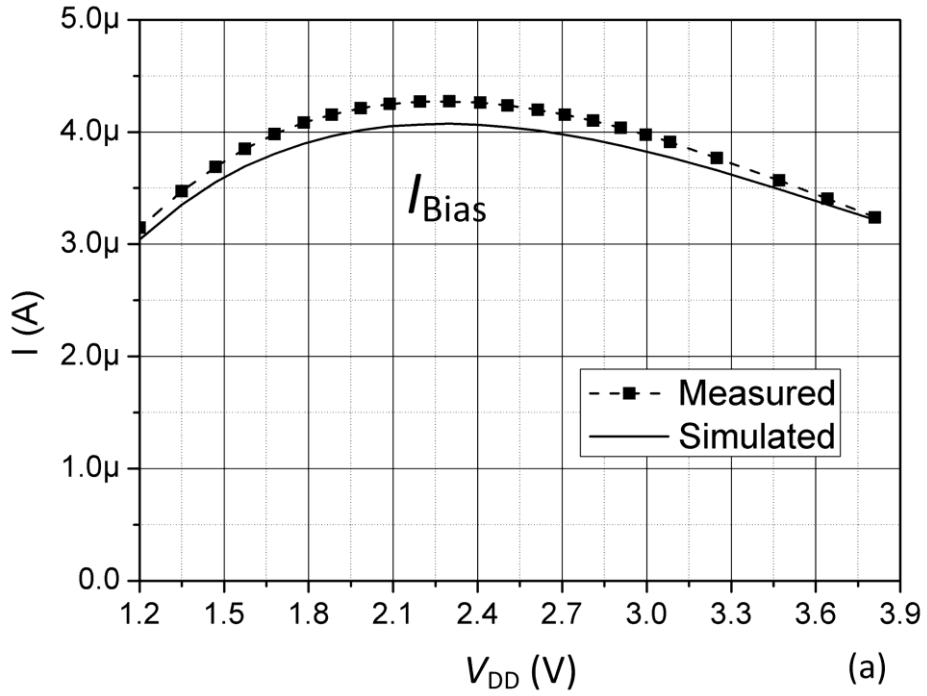



Fig. 3.3 Schematic of (a) peaking current source for Rec1 and (b) the proposed QIPV biasing circuit for Rec2.



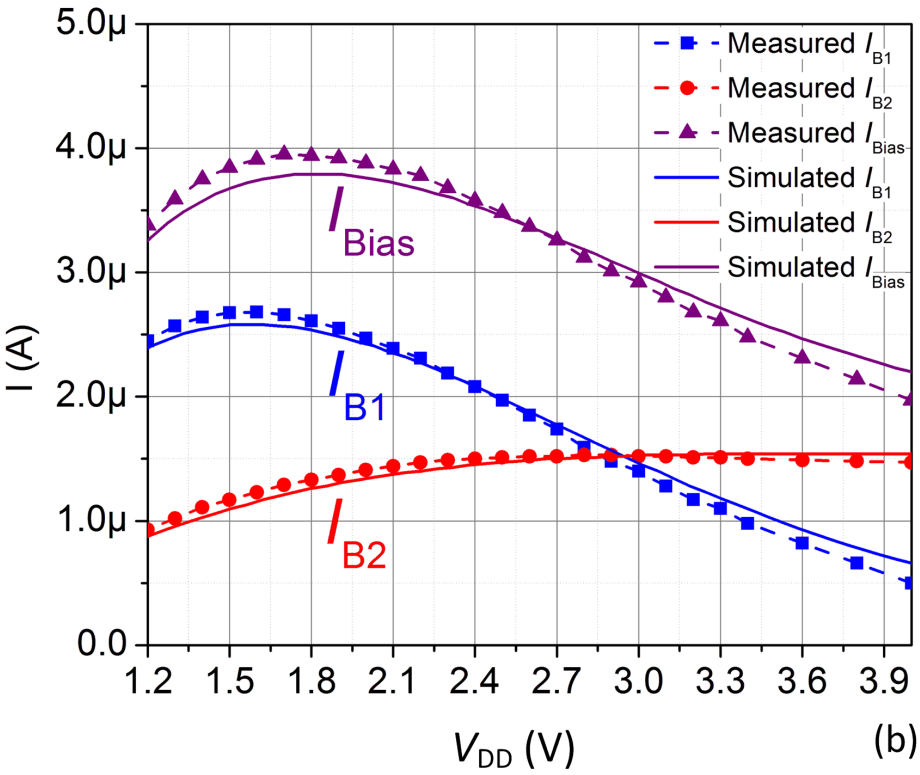




Fig. 3.4 Simulated and measured output current versus supply voltage of (a) peaking current source for Rec1 and (b) the proposed QIPV biasing circuit for Rec2.

The bipolar peaking current source was discussed in [29], and CMOS peaking current source was discussed in [30] and studied in [28]. With reference to Fig. 3.3(a), the relationship of $I_1$ and $I_{\text{Bias}}$ are given by

$$I_1 = \frac{V_{\text{DD}} - V_{\text{GS1}}}{R_{\text{b}}} = \frac{1}{2} k_{\text{n}} \left( \frac{W}{L} \right)_1 \left( V_{\text{GS1}} - V_{\text{tN}} \right)^2 \tag{3.2}$$

$$I_{\text{Bias}} = \frac{1}{2} k_{\text{n}} \left( \frac{W}{L} \right)_2 \left( V_{\text{GS1}} - V_{\text{tN}} - I_1 R_1 \right)^2 . \tag{3.3}$$

For $I_{\text{Bias}}$ to be insensitive to the change of $I_1$, we set $\text{d}I_{\text{Bias}}/\text{d}I_1$ to zero, and using (3.2) and (3.3), the condition for locating the maxima is

$$I_1 R_1 = \frac{1}{2} \left( V_{\text{GS1}} - V_{\text{tN}} \right), \tag{3.4}$$

and the bias current peaks at the nominal $V_{\text{DC}}$ that we use to calculate $I_1$, that is, $I_1 = (V_{\text{DC,nom}} - V_{\text{GS1}})/R_{\text{b}}$.

A simple assignment is to set $(W/L)_2 = 4(W/L)_1$ to give $I_{\text{Bias}} = I_1$. As shown in Fig. 3.4(a), measurement results match well with simulation results [22]. The peak current is designed to be around 4.1 μA when the supply voltage is 2.3 V, and the minimum bias current is 3.2 μA when $V_{\text{DC}} = 3.8$ V. Note that when $V_{\text{DC}}$ changes from 1.2 to 3.8 V, $I_1$ changes by over ±50%, but the bias current changes by only ±12.3%.

To realize a bias current that is inversely proportional to $V_{\text{DC}}$, one may set the peak current point to be the lowest $V_{\text{DC}}$ in the application (1.2 V in our case). However, due to the quadratic relation, the bias current will drop too much at the highest $V_{\text{DC}}$ (3.8 V). Our proposed QIPV biasing circuit is shown in Fig. 3.3(b). The resistor $R_1$ in Fig. 3.3(a) is split into two, and no additional current branch is needed. Two output currents ($I_{\text{B1}}$ and $I_{\text{B2}}$) can then be obtained with different peak current points. The peak current point of $I_{\text{B1}}$ ($V_{\text{DC,P1}}$) is set to be near the lowest $V_{\text{DC}}$, while the peak current point of $I_{\text{B2}}$ ($V_{\text{DC,P2}}$) is set to be near the higher end of the $V_{\text{DC}}$ range. $I_{\text{B2}}$ is used to compensate $I_{\text{B1}}$ at the high end of the $V_{\text{DC}}$ range when it drops significantly. The peak currents of $I_{\text{B1}}$ and $I_{\text{B2}}$ are

$$I_{\mathrm{B1,peak}} = \frac{1}{2} k_{\mathrm{n}} \left( \frac{W}{L} \right)_2 \left[ \sqrt{\frac{2I_{11}}{k_{\mathrm{n}} \left( W/L \right)_1}} - I_{11}(R_{\mathrm{1a}} + R_{\mathrm{1b}}) \right]^2 \tag{3.5}$$

$$I_{\mathrm{B2,peak}} = \frac{1}{2} k_{\mathrm{n}} \left( \frac{W}{L} \right)_3 \left[ \sqrt{\frac{2I_{12}}{k_{\mathrm{n}} \left( W/L \right)_1}} - I_{12} R_{\mathrm{1a}} \right]^2 . \tag{3.6}$$

where $I_{11}$ is the value of $I_1$ at $V_{\mathrm{DC,P1}}$, and $I_{12}$ is the value of $I_1$ at $V_{\mathrm{DC,P2}}$. Note that the size of $\mathrm{M_{N3}}$ is the same as $\mathrm{M_{N1}}$, while $(W/L)_2$ is still four times of $(W/L)_1$, because $I_1$ at $V_{\mathrm{DC,P2}}$ is roughly two times higher than $I_1$ at $V_{\mathrm{DC,P1}}$. With this assignment, $I_{\mathrm{B2,peak}}$ is about half of $I_{\mathrm{B1,peak}}$. The combined bias current $I_{\mathrm{Bias}} = I_{\mathrm{B1}} + I_{\mathrm{B2}}$ then resembles a QIPV output current.

Simulated and measured results of the proposed QIPV biasing circuit are shown in Fig. 3.4(b). The measured $I_{\mathrm{B1}}$ peaks at around 1.6 V with a current of 2.68 μA, and drops to 0.5 μA at $V_{\mathrm{DC}}$ = 4 V. The measured $I_{\mathrm{B2}}$ peaks at around 2.9 V with a current of 1.53 μA. Meanwhile, $I_{\mathrm{Bias}}$ peaks at around 1.7 V with 3.95 μA, and drops to 1.97 μA at $V_{\mathrm{DC}}$ = 4 V. The proposed QIPV circuit can be easily modified to bias an amplifier designed to have a constant (or adaptive) bandwidth, for example, to compensate for the negative effects with decreasing supply voltage.

### 3.3 Power Transistor Sizing Optimization

NMOS transistors are chosen to implement the active diodes and PMOS transistors the cross-coupled pair for two reasons. First, by using PMOS transistors for the cross-coupled pair, they are driven by the AC input, not the comparator, and their parasitic gate capacitors do not affect the speed and the switching loss of the rectifier, as they are part of the *LC* resonant tuning capacitor $C_2$ that do not dissipate power, and the energy is just transferred between the resonant capacitors and the secondary coil $L_2$.

Second, the mobility of NMOS transistors is higher, and results in smaller *W*/*L* ratios that reduce switching loss. For the trade-off between switching loss and conduction loss, $W_{\mathrm{N}}$ is set to be 600 μm with minimum channel length; on the other hand, *W*/*L* of the power PMOS could be large to achieve a small turn-on voltage drop ($W_{\mathrm{P}}$ = 4000 μm). In this design, the turn-on voltage drop of power NMOS $V_{\mathrm{DSN}}$ and PMOS $|V_{\mathrm{DSP}}|$ are set to be ~250 mV and ~70

mV respectively at $|V_{AC}|$ = 1.5 V and $R_L$ = 500 Ω. The total voltage drop is only ~320 mV in the worst case, which is much smaller than using passive diodes.

### 3.4 Minimum Operating Voltage

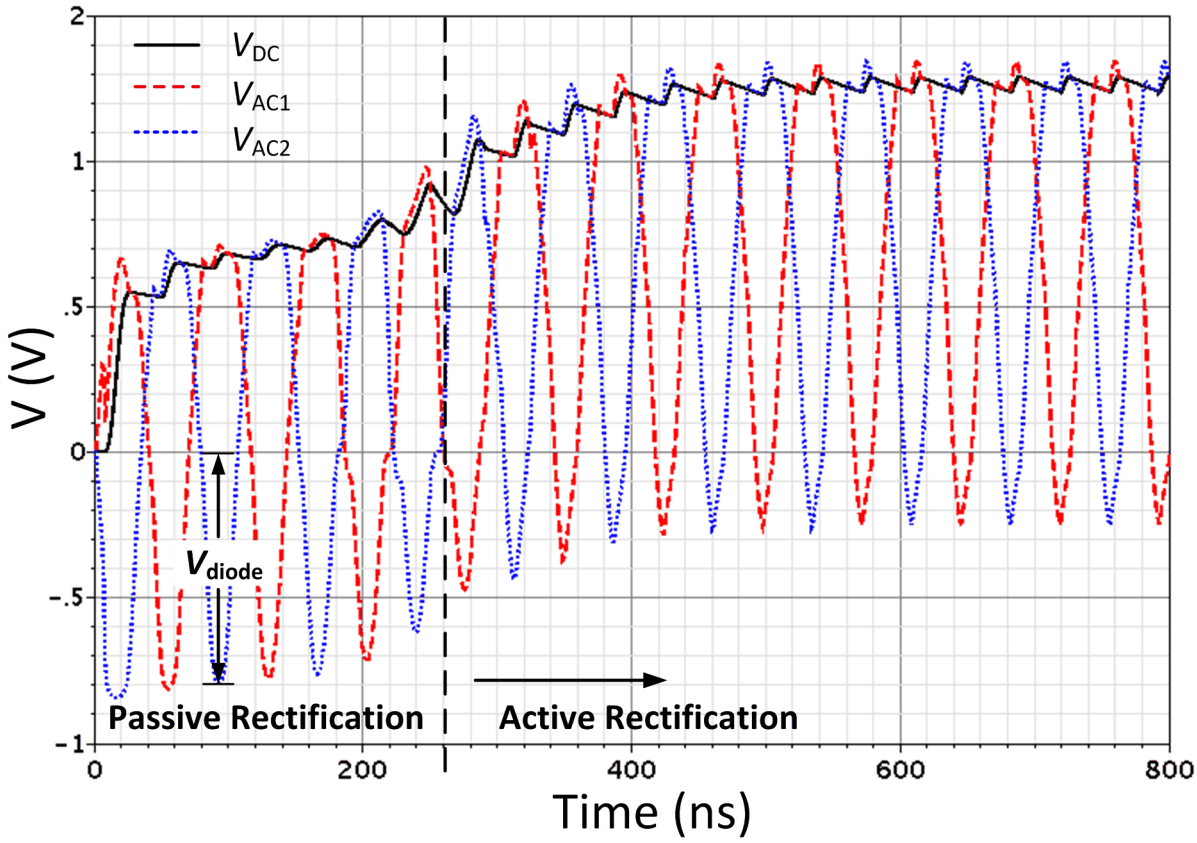



Fig. 3.5 Simulated start-up process of the proposed active rectifier (Rec2).

The lowest input amplitude $V_{AC,min}$ for our proposed rectifiers to work is determined by the minimum supply voltage of the comparators. The rectified DC voltage should be higher than $V_{GS}$ + $V_{DSsat}$ for the comparators to work, so $V_{AC,min}$ is given by

$$V_{AC,min} = V_{DC,min} + V_{Drop} = V_{GS} + V_{DSsat} + V_{DSN} + |V_{DSP}|, \quad (3.7)$$

where $V_{DSN}$ and $|V_{DSP}|$ are the drain-to-source voltages of the power transistors. However, the lowest input amplitude for start-up is the same as that of using passive diodes, because when the active rectifier is relaxed, the DC output voltage $V_{DC}$ is 0 and is unable to turn on the power NMOS switches. Instead, as illustrated in Fig. 3.5, parasitic diodes of the power

NMOS switches will be forward-biased when $V_{AC} > V_{DC}$ during start-up. After the output capacitor is charged up to higher than the minimum supply voltage required by the comparators that are biased by the QIPV current source, the power NMOS switches are then activated, and the active rectifier could then function as designed. Latch-up problem could be avoided by careful layout.

### 3.5 Simulation and Measurement Results

The proposed active rectifiers were designed and fabricated in a 0.35 μm CMOS N-well process. Micrographs of the rectifiers are shown in Fig. 3.6. The sizes of these two rectifiers, including the pads, are 0.12 $mm^2$ and 0.19 $mm^2$, respectively; and the active areas are 0.041 $mm^2$ and 0.065 $mm^2$, respectively. The measurement setup is shown in Fig. 3.7, including the identical coupling coils that are etched on single-side printed circuit boards (PCBs). The primary and secondary coils each have 3 turns with inner and outer radii of 0.75 cm and 1 cm respectively, and were separated by 1 cm during measurements. The measured inductance of the coils is 310.4 nH, and the series resistance is 480 mΩ at 13.56 MHz and 190 mΩ at DC. The DC output of the rectifier drives a 1.5 nF off-chip filtering capacitor.

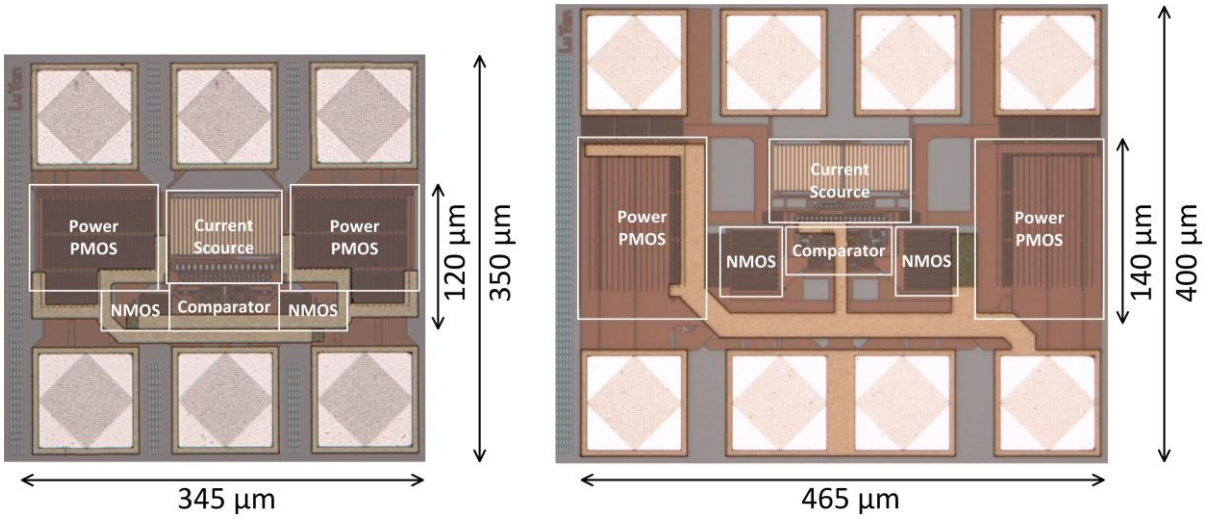



Fig. 3.6 Micrographs of Rec1 and Rec2.

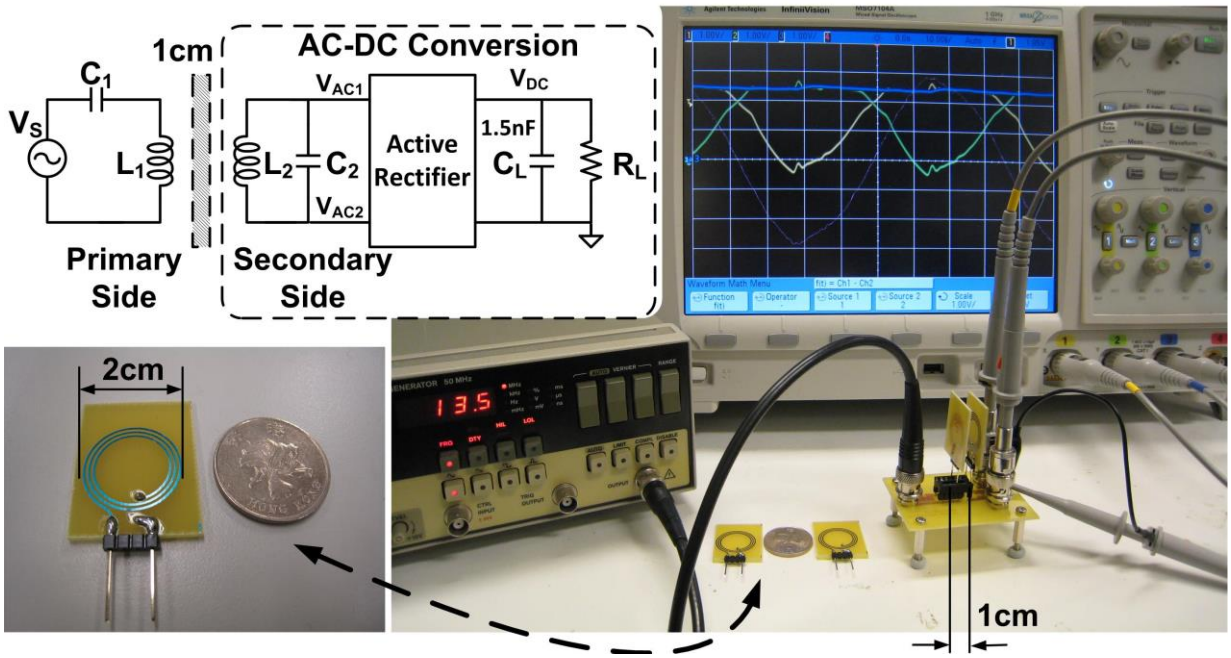



Fig. 3.7 Measurement setup for the proposed 13.56 MHz active rectifiers.

Since the peripheral circuits for measuring the voltage conversion ratio $M$ and the power conversion efficiency PCE are different, two separate PCBs are made and measured accordingly. Fig. 3.8 shows the measured AC input and DC output waveforms of the proposed active rectifiers Rec1 and Rec2, respectively. The peak of $I_{B1}$ is eventually designed to locate at 1.6 V instead of 1.2 V to reserve adequate margin for keeping the PCE high in the middle and higher range of $V_{AC}$. The optimized case is when the input amplitude $V_{AC}$ is 3 V and $R_L$ is 500 Ω. The input voltage ripples across $V_{AC1}$ and $V_{AC2}$ are due to large change in load current when turning on and off the power NMOS switches. As can be observed from Fig. 3.8(a) and Fig. 3.8(b), reverse current is well eliminated, which means that the NMOS switch is turned off when its drain voltage is higher than the ground voltage. The worst operating condition for the rectifier is at heavy load and low input amplitude, as shown in Fig. 3.8(c) and Fig. 3.8(d). In this case, a small amount of reverse current is observed due to slower response time of the rectifier at lower supply voltages. Conduction loss of the power transistors increases at heavy load and when the gate overdrive voltage is small at low $V_{AC}$. The performance could further be improved if the bias current of the comparator is slightly increased to have a larger offset for faster response.

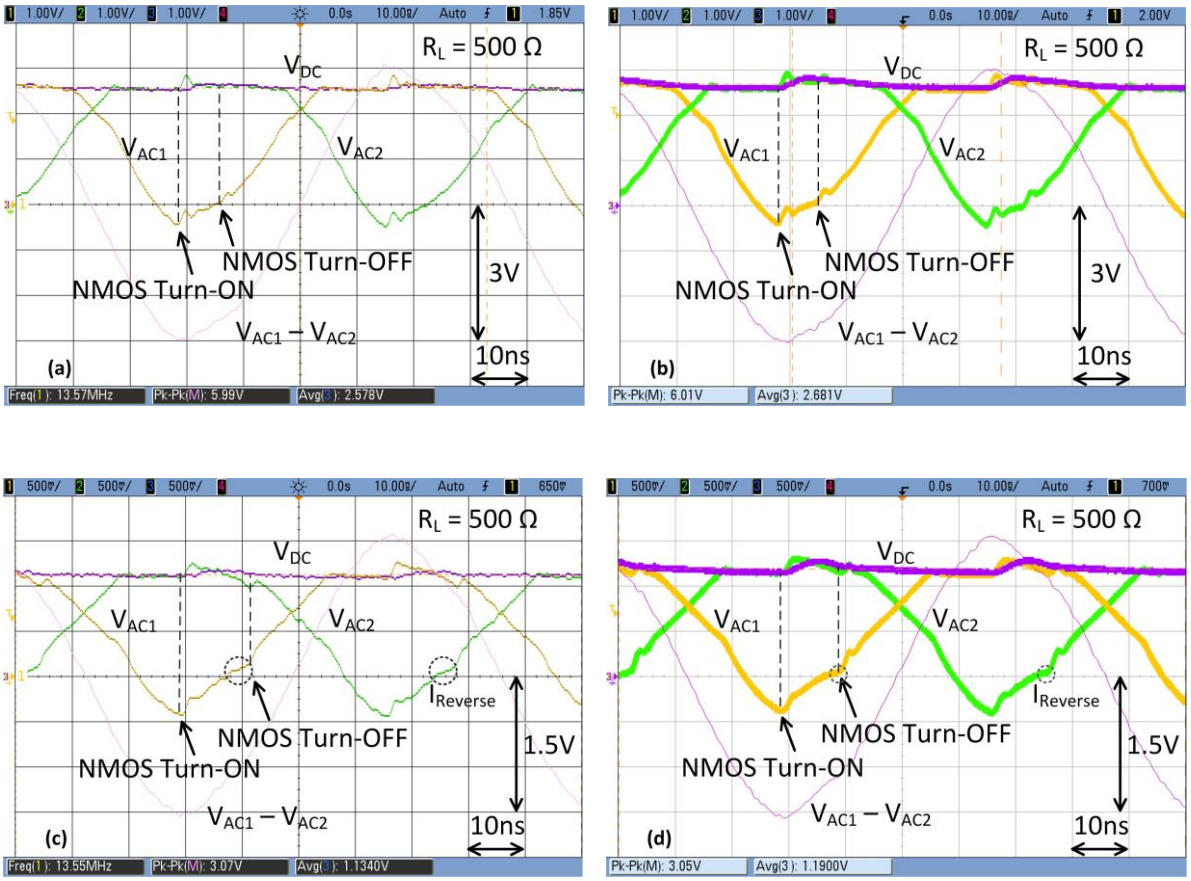



Fig. 3.8 Measured waveforms of AC inputs and DC output at $R_L$ = 500Ω and $V_{AC}$ = 3 V of (a) Rec1 and (b) Rec2; at $R_L$ = 500Ω and $V_{AC}$ = 1.5 V of (c) Rec1 and (d) Rec2.

Fig. 3.9 summarized the measured voltage conversion ratios of the rectifiers versus $V_{AC}$ under different loading conditions ($R_L$ = 500 Ω, and 5 kΩ). The peak voltage conversion ratios of Rec1 and Rec2 are 92.3% and 93.1%, respectively, when $R_L$ = 5 kΩ. The minimum $M$ of Rec1 and Rec2 are 74% and 79%, respectively, when $R_L$ = 500 Ω.

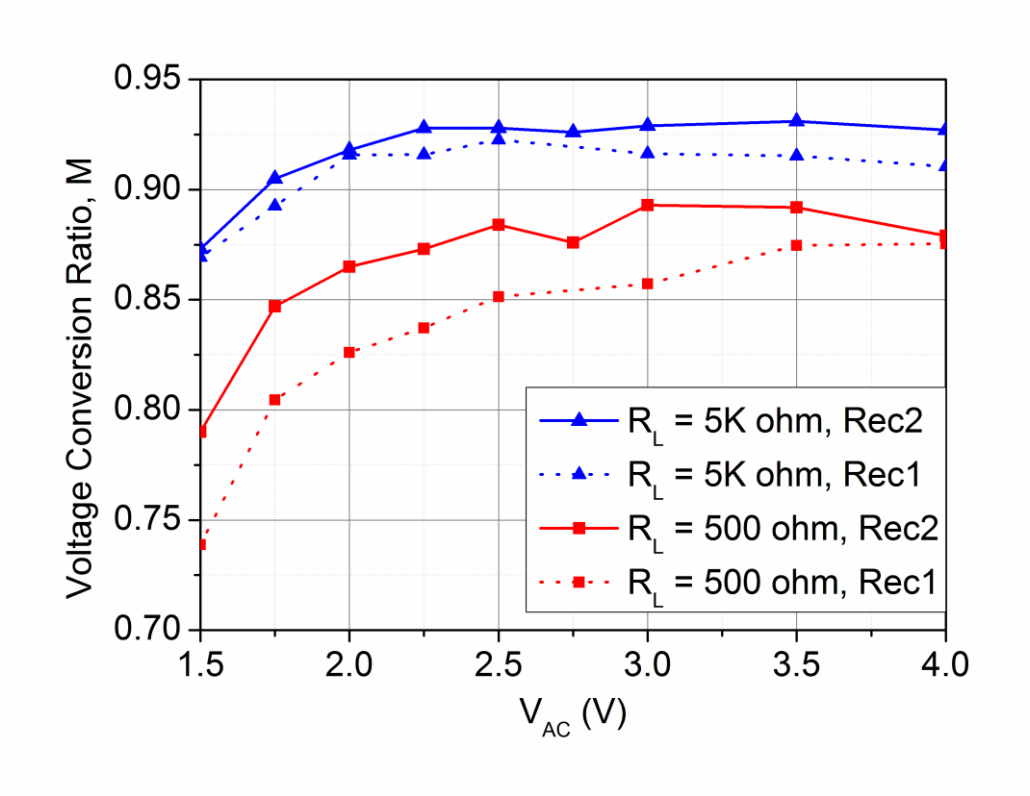



Fig. 3.9 Measured voltage conversion ratios of Rec1 and Rec2 with different loadings.

The power conversion efficiency PCE of an AC to DC converter is defined as

$$\mathrm{PCE} = \frac{P_{\mathrm{OUT}}}{P_{\mathrm{IN}}} = \frac{V_{\mathrm{DD}}^2 / R_{\mathrm{L}}}{\frac{1}{\mathrm{N}\cdot\mathrm{T}}\int_{t_0}^{t_0+\mathrm{N}\cdot\mathrm{T}} V_{\mathrm{AC}}(t)\cdot I_{\mathrm{AC}}(t)\,\mathrm{d}t}, \tag{3.8}$$

where T is the period of the input sinusoidal wave, and N is the number of cycles that are integrated for $P_{\mathrm{IN}}$ calculation. The main losses are conduction loss, switching loss and comparator static power. For PCE measurement, as shown in Fig. 3.10, a 10 Ω resistor is inserted in the input path to measure the AC input current $I_{\mathrm{AC}}$. $C_{2\mathrm{B}}$ is used to filter the distorted $V_{\mathrm{AC}}$ waveforms caused by the 10 Ω resistor during large $\Delta I/\Delta t$ transients. The data of $V_{\mathrm{AC}}$ and $I_{\mathrm{AC}}$ can be collected by two identical differential probes with the setup shown in Fig. 3.10(a); or by two identical single-ended probes as shown in Fig. 3.10(b). In addition, a voltage meter with floating terminals not connected to the ground is needed for the measurement with single-ended probes. Note that according to (3.8), the PCE is not necessarily lower than the voltage conversion ratio at the same loading condition [31], as the highest PCE usually is designed to be at heavy load, while the highest $M$ is always obtained at light load.

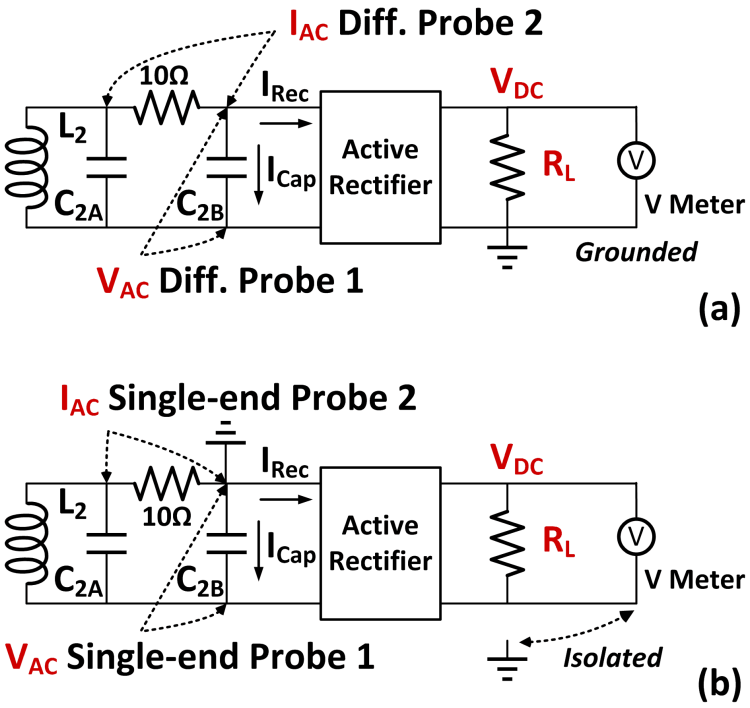



Fig. 3.10 The PCB schematics for PCE measurements with (a) differential voltage probes or (b) single-end probes.

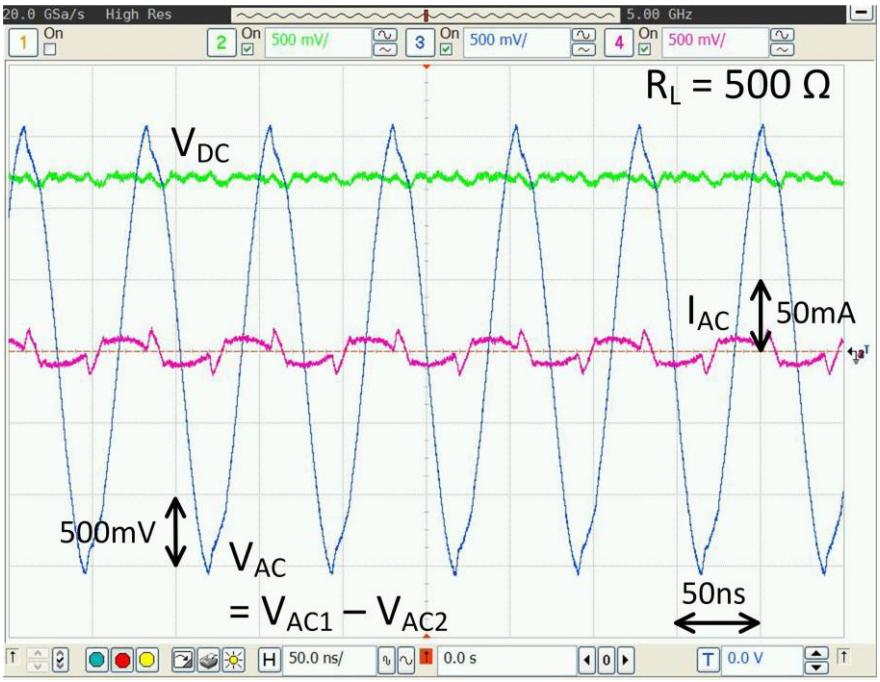
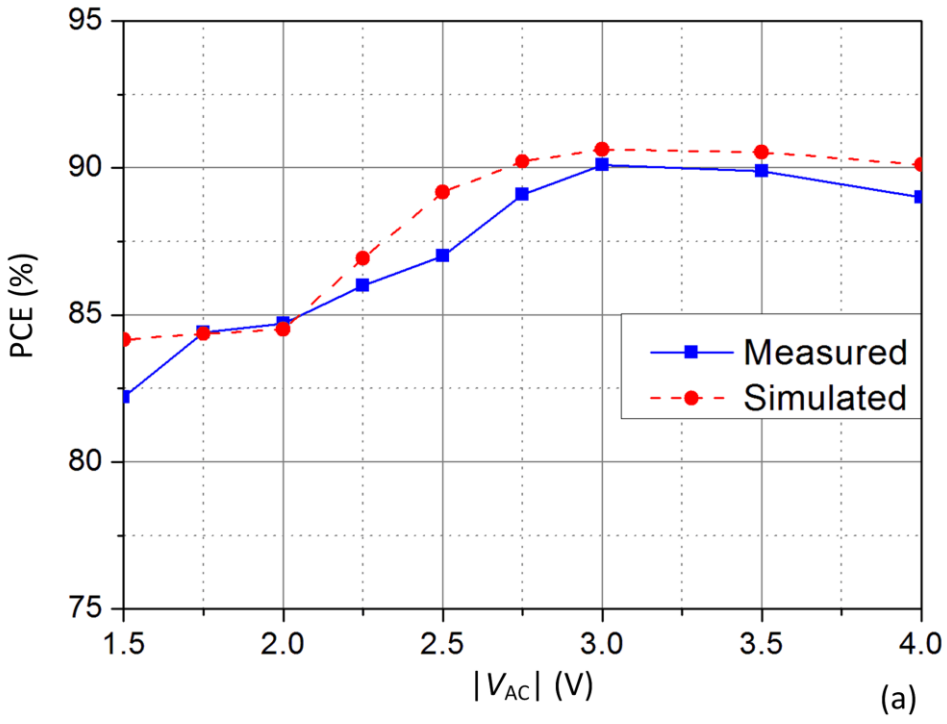



Fig. 3.11 Measured waveforms of $V_{AC}$, $I_{AC}$ and $V_{DC}$ for PCE calculation.

In our experiments, two identical probes with >1 GHz bandwidth are used to measure $V_{AC}$ and $I_{AC}$. About 10,000 points of $V_{AC}$ and $I_{AC}$ (6 cycles) were integrated and averaged for $P_{IN}$ in each PCE calculation. The secondary coil $L_2$ resonates with $C_{2A}$ + $C_{2B}$ at 13.56 MHz, with $C_{2B}/C_{2A}$ = 0.15. As shown in Fig. 3.11, the measured $I_{AC}$ is the sum of $I_{Cap}$ that goes through $C_{2B}$ and $I_{Rec}$ that goes into the rectifier. To obtain accurate PCE results, $C_{2B}/C_{2A}$ cannot be large, otherwise, the large $I_{Cap}$ of $C_{2B}$ that does not dissipate power will affect the accuracy of the relatively small rectifier input current $I_{Rec}$ that dissipates power. Note also that the scales of the two identical probes should be kept the same to guarantee accuracy. As summarized in Fig. 3.12(a), with $R_L$ = 500 Ω, the PCEs of Rec2 were measured to be 82.2% to 90.1% with $|V_{AC}|$ that varied from 1.5 to 4 V; while in Fig. 3.12(b) the PCEs of 82.3% and 71.2% were measured at $|V_{AC}|$ = 3 V with $R_L$ = 100 Ω and 5 kΩ, respectively. Simulated PCEs are also included for reference: 84.2% to 90.7% were obtained with a load resistor of 500 Ω, and 82.9% to 81.3% were obtained at $|V_{AC}|$ = 3 V with $R_L$ = 100 Ω and 5 kΩ, respectively. All the above results were measured and simulated at an input frequency of 13.56 MHz. In Fig. 3.12(c), measured and simulated PCEs of Rec2 that operated at the transmission frequencies from 10 to 20 MHz are shown, with $R_L$ = 500 Ω and $|V_{AC}|$ = 3 V. The measured PCEs matched quite well with the simulated PCEs at heavy load, and started to deviate from the simulated PCEs at light load of 1 kΩ since $I_{Rec}$ became too low to be measured accurately.



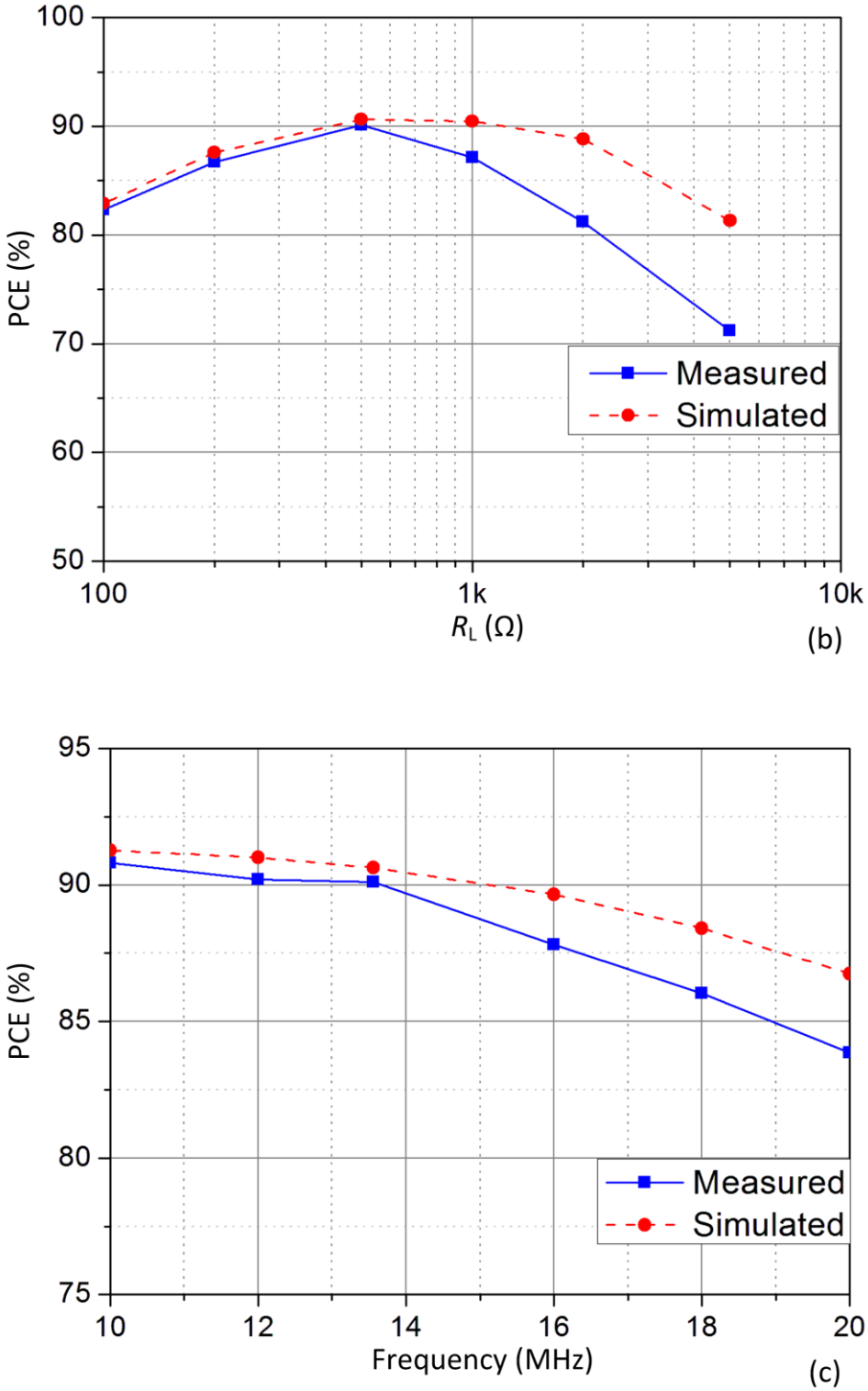



Fig. 3.12 Measured and simulated PCEs of the proposed Rec2 operating at 13.56 MHz with (a) $R_L$ = 500 Ω and (b) $|V_{AC}|$ = 3 V; and its frequency response with condition of $R_L$ = 500 Ω and $|V_{AC}|$ = 3 V.

Table 3.1 COMPARISON TO THE STATE-OF-THE-ART RECTIFIERS

| | TCAS-II 06 [20] | JSSC 09 [21] | TCAS-I 11 [23] | TCAS-II 12 [25] | TBCAS 12 [31] | JSSC 12 [15] | **This Work Rec1 [22]** | **This Work Rec2 [26]** |
|---|---|---|---|---|---|---|---|---|
| Technology | 0.35 μm | 0.35 μm | 0.5 μm | 0.18 μm | 0.18 μm | 0.18 μm | **0.35 μm** | **0.35 μm** |
| Chip Area | 0.107 $mm^2$ | 1.03 $mm^2$ | 0.263 $mm^2$ | 0.009 $mm^2$ | 0.608 $mm^2$ | 0.34 $mm^2$ | **0.12 $mm^2$** | **0.19 $mm^2$** |
| Frequency | 13.56 MHz | 1.5 MHz | 13.56 MHz | 13.56 MHz | 10 MHz | 13.56 MHz | **13.56 MHz** | **13.56 MHz** |
| Input Amp. | 1.5 ~ 3.5 V | 1.2 ~ 2.4 V | 3.3 ~ 5 V | 0.9 ~ 2 V | 0.8 ~ 2.7 V | N/A | **1.5 ~ 4 V** | **1.5 ~ 4 V** |
| Load Cap. | 200 pF | 1 μF | 10 μF | 10 μF | 200 pF | 5.8 μF | **1.5 nF** | **1.5 nF** |
| Output Voltage | 1.2 ~ 3.22 V ($R_L$ = 1.8 kΩ) | 1.13 ~ 2.28 V ($R_L$ = 2 kΩ) 0.98 ~ 2.08 V ($R_L$ = 100 Ω) | 2.5 ~ 3.9 V ($R_L$ = 500 Ω) | 0.45 ~ 1.78 V ($R_L$ = 1 kΩ) | 0.3 ~ 2.0 V ($R_L$ = 2 kΩ) | 1.2 V (w/ load chip) | **1.28V ~ 3.65V ($R_L$ = 1.8 kΩ) 1.13V ~3.50V ($R_L$ = 500 Ω)** | **1.28V ~ 3.56V ($R_L$ = 1.8 kΩ) 1.19V ~3.52V ($R_L$ = 500 Ω)** |
| Coil Diam. | 6.0 cm | N/A | 3.0 cm | N/A | N/A | 7 mm | **2.0 cm** | **2.0 cm** |
| $P_{OUT}$ (Max.) | 5.76 mW | 43.3 mW | 30.42 mW | 3.2 mW | 2 mW | 112.5 mW | **24.5 mW** | **24.8 mW** |
| Voltage Conversion Ratio, M | 0.78 ~ 0.92 ($R_L$ = 1.8 kΩ) | 0.94 ~ 0.95 ($R_L$ = 2 kΩ) 0.82 ~ 0.84 ($R_L$ = 100 Ω) | 0.76 ~ 0.81 ($R_L$ = 500 Ω) | 0.82 ~ 0.89 ($R_L$ = 1 kΩ) | 0.6 ~ 0.89 ($R_L$ = 2 kΩ) | N/A | **0.85 ~ 0.9 ($R_L$ = 1.8 kΩ) 0.74 ~ 0.88 ($R_L$ = 500 Ω)** | **0.873 ~ 0.93 ($R_L$ = 1.8 kΩ) 0.79 ~ 0.89 ($R_L$ = 500 Ω)** |
| PCE (Simulated) | 65% ~ 89% ($R_L$ = 1.8 kΩ) | 82% ~ 87% ($R_L$ = 100 Ω) | 71% ~ 84.5% ($R_L$ = 500 Ω) | N/A | 60% ~ 86% ($R_L$ = 2 kΩ) | 93% (w/ load chip) | **82.5% ~ 89.6% ($R_L$ = 500 Ω)** | **84% ~ 90.7% ($R_L$ = 500 Ω)** |
| PCE (Measured) | N/A | N/A | 68% ~ 80.2% ($R_L$ = 500 Ω) | 60% ~ 81.9% ($R_L$ = 1 kΩ) | 37% ~ 80% ($R_L$ = 2 kΩ) | N/A | **N/A** | **82% ~ 90.1% ($R_L$ = 500 Ω)** |

Table 3.1 summarized and compared the performances of our works with state-of-the-art designs. With inductively coupled air coils our proposed rectifier, operating at 13.56 MHz in the ISM frequency band, achieved good voltage conversion ratio and power conversion efficiency over a wide input range and loads.

## 3.6 Conclusions

In this chapter, a switched-offset scheme for high-speed high-current active rectifiers for biomedical implants is proposed. Longer conduction time is achieved without sacrificing robustness, and the multiple-pulsing problem related to dynamic offset is eliminated through careful design of the digital logic. Two rectifiers with peaking current source or QIPV biasing circuit were implemented and measured, verifying that they could operate efficiently over wide input amplitude and load current range. The comparators of the second active rectifier were biased with novel QIPV biasing circuit, and reverse current was much reduced at low $|V_{AC}|$, and was eliminated at high $|V_{AC}|$. Compared to previous 13.56 MHz designs, both the voltage conversion ratio and PCE at low $|V_{AC}|$ and at heavy loading are improved. To conclude, the proposed rectifiers that operate at 13.56 MHz make it possible to use one secondary coil for both wireless power link and uplink data transmission; to minimize the volume of biomedical implants by switching at high frequency; and to deliver an output power of tens of milli-Watt for neuron recorders and/or stimulators.

# Chapter 4 RECONFIGURABLE ACTIVE RECTIFIER

As discussed in Chapter 1, for cochlear implants and retinal prostheses, having a miniaturized form factor and being battery-less are highly desirable. Such devices require real-time power transfer in the range of 10 to 100 mW, and as human tissue specific absorption rate (SAR) increases with frequency, inductively-coupled power links that operate at 13.56 MHz or lower in ISM bands are commonly used. However, lower transmission frequency means larger matching and filtering capacitors that are bulky. In addition, the received AC input amplitude $|V_{AC}|$ would fluctuate due to changes in distance and orientation between the coupling coils.

As discussed in Chapter 2, active rectification suffers from reverse current caused by the comparators that turn off the power switches with delay. To achieve a high voltage conversion ratio (VCR) and power conversion efficiency (PCE), conduction time $\Delta t$ of the active diodes should be maximized, and the power switches should be turned off right before reverse current sets in. Hence, comparators with unbalanced bias currents and asymmetric differential inputs are also used to set an artificial input offset voltage to compensate for the delay and to turn the power switches on and off properly. Again, in this design, only the turn-off edges of the power switches are compensated by comparator offset to maximize $\Delta t$ without sacrificing robustness.

In this chapter, a fully integrated reconfigurable active rectifier (labeled as Rec3) [26] that can be switched between the full-wave rectifier (1X) mode and the voltage doubler (2X) mode in the 30 mW range with all capacitors fabricated on-chip will be presented, as shown in Fig. 4.1. The effectiveness of utilizing on-chip capacitors is significantly improved by a switching arrangement that avoids connecting the output capacitors in series in the 2X mode. Reverse current is reduced for $|V_{AC}|$ that ranges from 1.25 V to 4 V by the bias current that is quasi-inversely proportional to the output DC voltage $V_{DC}$ (QIPV).

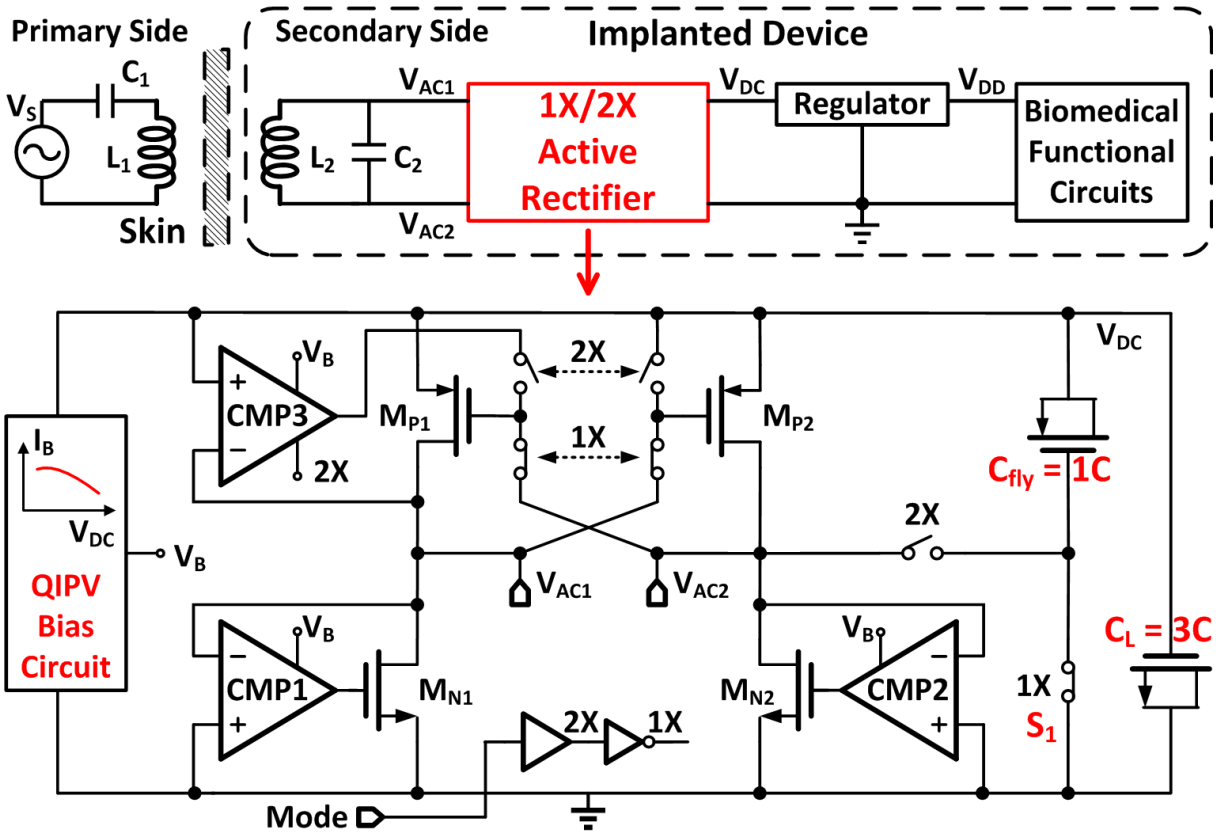



Fig. 4.1 Block diagram of an inductively powered biomedical implantable system-on-a-chip alongside the proposed fully integrated 1X/2X active rectifier with QIPV bias current.

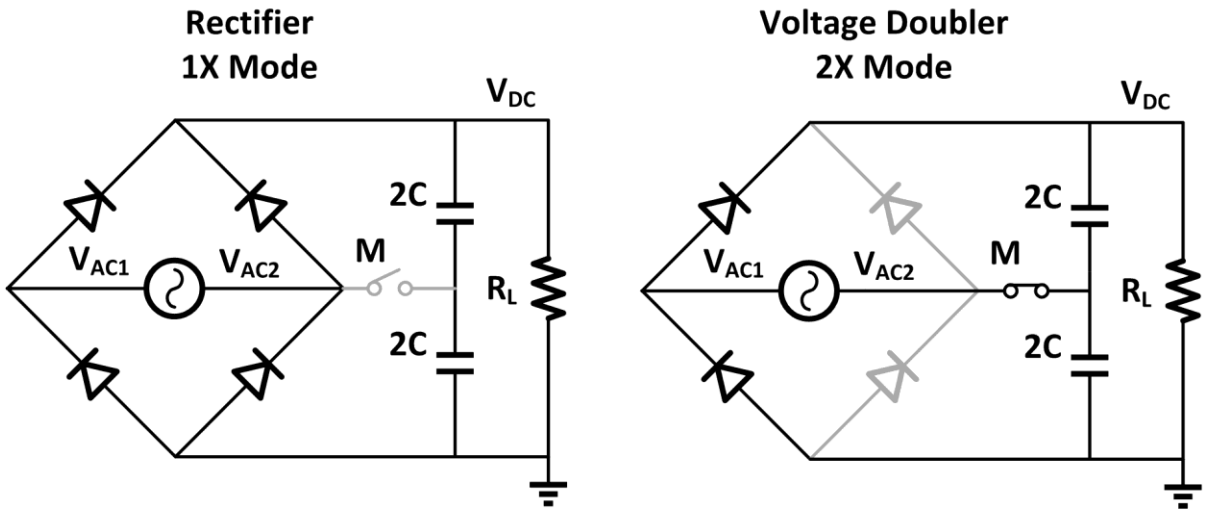



Fig. 4.2 Schematic of the passive reconfigurable rectifier (universal rectifier) with 1X (rectifier) mode and 2X (voltage doubler) mode.

### 4.1 Voltage Doubler

For domestic electrical appliances that can use an AC supply voltage of 220/110 $V_{RMS}$, a passive reconfigurable rectifier (universal rectifier) with 1X (rectifier) mode and 2X (voltage doubler) mode is commonly used as shown in Fig. 4.2.

To cater for coupling coefficient $k$ variations with distance and/or orientation, a reconfigurable rectifier may be able to increase $V_{DC}$ without increasing the transmitted power. The same idea is employed in the loosely coupled inductive link in [24] to extend the coupling range. However, in the design of [24], the two load capacitors are not utilized effectively. Those two 1 µF capacitors are connected in series and resulted in an equivalent load capacitor $C_{L,eq}$ of 0.5 µF, and both cannot be integrated on-chip.

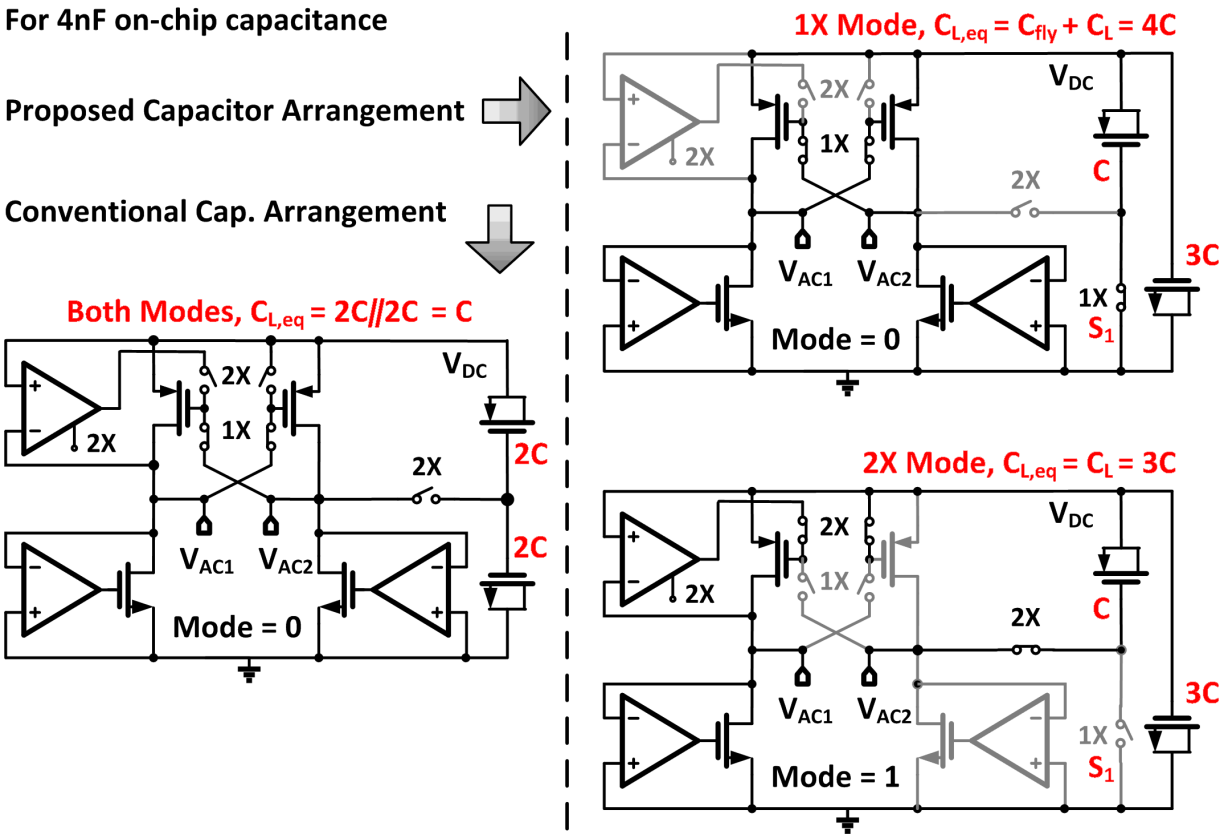



Fig. 4.3 The conventional and the proposed arrangement of $C_L$, assuming that the total capacitance available is 4C for implementing $C_L$.

Fig. 4.3 shows the conventional and the proposed arrangement of $C_L$. Assume that the total capacitance available is 4C for implementing $C_L$, in the conventional topology, two 2C capacitors are connected in series that results in $C_{L,eq}$ equal to C in both the 1X and the 2X mode. In the proposed topology, $C_{fly}$ = C and $C_L$ = 3C are connected through switches $S_1$ and $S_2$. In the 1X mode, $S_1$ is turned on, the two capacitors are in parallel, and $C_{L,eq}$ is 4C; and in the 2X mode, $S_1$ is opened, $C_{fly}$ acts as a flying capacitor to charge up $C_L$, and $C_{L,eq}$ is 3C. As a result, the proposed topology increases $C_{L,eq}$ by 4 and 3 times compared to the universal rectifier in the 1X and the 2X mode, making it possible to integrate the capacitors on-chip. In our case, $C_{fly}$ and $C_L$ are equal to 1 and 3 nF respectively. Based on the considerations of voltage conversion ratio at the maximum loading condition in the 2X mode, $C_{fly}$ is set to be 1 nF. Because $C_{fly}$ served as a pumping capacitor for voltage doubling in a charge pump, small $C_{fly}$ will decrease the VCR and consequently the PCE.

### 4.2 Bias Current

As discussed in Section 3.2, for a robust design, the bias circuit of the active rectifier should not require a startup circuit. In [20], [23] and [25], self-biased currents that are quadratic with respect to the supply voltage were used; and in [21] and [24], a simple bias current that is proportional to the supply voltage was used; in Rec1 [22] a peaking current source (PCS) is used to bias the comparators so that the bias current would stay approximately constant when $|V_{AC}|$ changes; and in Rec2 [26], to further improve the performance at low $|V_{AC}|$, the QIPV bias current is used, because for a constant active diode delay $t_{d,AD}$, the bias current should be approximately inversely proportional to $|V_{AC}|$.

In Rec3 [32], the QIPV bias current is also used, but with a different $I_{B1}$ and $I_{B2}$ ratio as shown in Fig. 4.4. For Rec3, the ratios of $M_{N1}$ : $M_{N2}$ : $M_{N3}$ are 2 : 8 : 1. The peak current point of $I_{B1}$ is set close to the lowest $V_{DC}$, while the peak current point of $I_{B2}$ is set close to the higher end of $V_{DC}$, and $I_{B2}$ is used to compensate $I_{B1}$ at high $V_{DC}$ when $I_{B1}$ drops significantly. Therefore, as $V_{DC}$ decreases the unbalanced bias current increases and a larger offset is obtained.

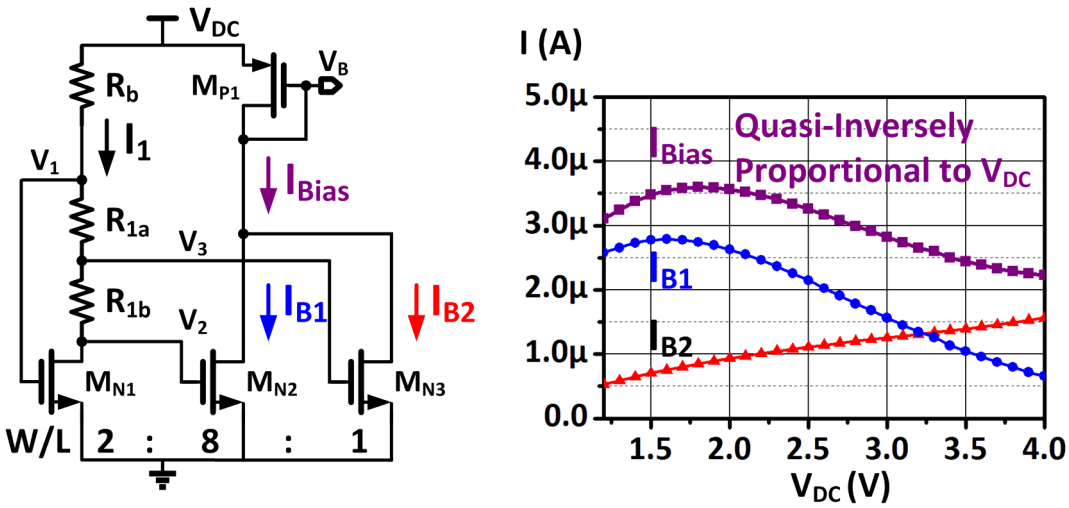



Fig. 4.4 QIPV biasing with aspect ratios $M_{N1}$ : $M_{N2}$ : $M_{N3}$ = 2 : 8 : 1.

### 4.3 NMOS and PMOS Active Diodes

The schematics of the comparators CMP1 (CMP2) with $M_{N1}$ ($M_{N2}$), and the comparator CMP3 with $M_{P1}$, are shown in Fig. 4.5. The "Mode" signal also changes the value of the unbalanced currents in CMP1 and CMP2, such that the offsets of CMP1 and CMP2 are set to different values in the two modes, because the input sinusoidal wave have different slew rates in the 1X and the 2X mode. Note that for Rec3 the minimum value of $V_{DC}$ is 1.6 V as the rectifier would operate in the 2X mode in low voltage conditions. Thus, the proposed QIPV $I_{Bias}$ helps the rectifier to reduce the reverse current for $V_{DC}$ from 1.6 to 4 V.

The CMP3 is disabled in the 1X mode by cutting off its bias current with an "En" signal, because the power PMOS transistors are cross-coupled in the 1X mode. In the 2X mode, CMP2 is not disabled even it does not need to work in this mode, because its input terminal $V_{AC2}$ is always equal to roughly half of $V_{DC}$ (always above Ground voltage) in the 2X mode. It means that the CMP2 output would not fluctuate in the 2X mode, and no extra switching loss will be induced by CMP2 and $M_{N2}$.

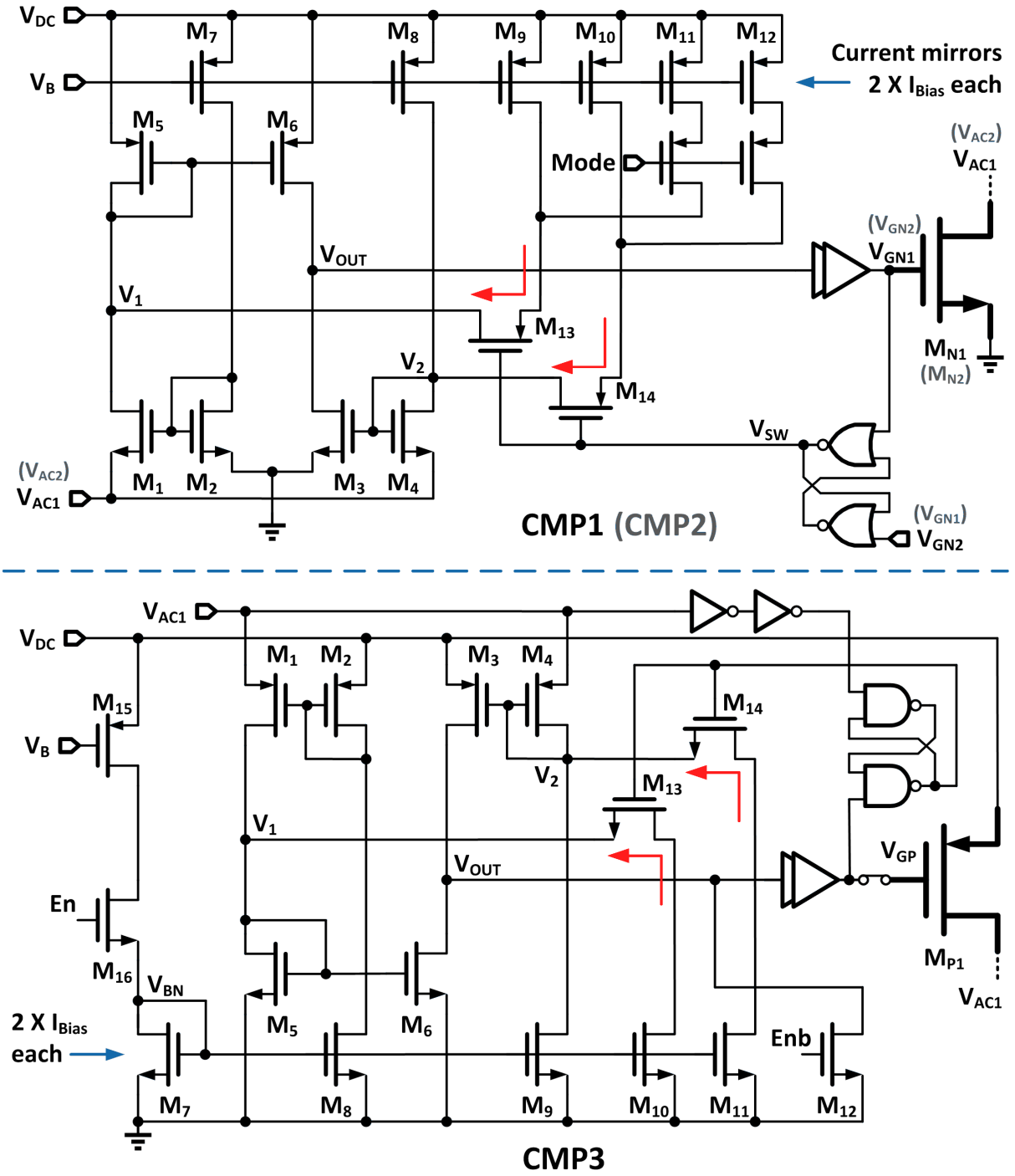



Fig. 4.5 Schematics of the CMP1 (CMP2) with $M_{N1}$ ($M_{N2}$), and the CMP3 with $M_{P1}$.

Transistor sizes of the power MOS need to tradeoff for peak VCRs and PCEs between the 1X mode and the 2X mode. Because the output voltage $V_{DC}$ in the 2X mode is double of the $|V_{AC}|$ input, the input current of the converter should be double of the output current. Thus, for the same loading, more current needs to be conducted in the 2X mode, and consequently larger

transistors are needs for the 2X mode. Another point is that, as mentioned in Section 3.3, when the PMOS transistors are configured as cross-coupled pair, they are driven by the AC input, not the comparator, and their parasitic gate capacitors do not affect the speed and the switching loss of the rectifier, as they are part of the *LC* resonant tuning capacitor $C_2$ that do not dissipate power. However, this feature is no longer true in this reconfigurable case, as the power PMOS $M_{P1}$ also needs to be driven in the 2X mode that prevents using large power PMOS as were done for the active rectifiers Rec1 and Rec2.

The simulated waveforms of the reconfigurable rectifier in the 1X mode with $R_L$ = 500 Ω and $|V_{AC}|$ = 1.5 and 3 V, respectively, are given in Fig. 4.6. Also, the simulated waveforms of the reconfigurable rectifier in the 2X mode with $R_L$ = 500 Ω and $|V_{AC}|$ = 1.25 and 1.8 V, respectively, are given in Fig. 4.7. From the current waveforms of $I_{AC}$, we can easily tell that reverse currents are well eliminated in all cases.

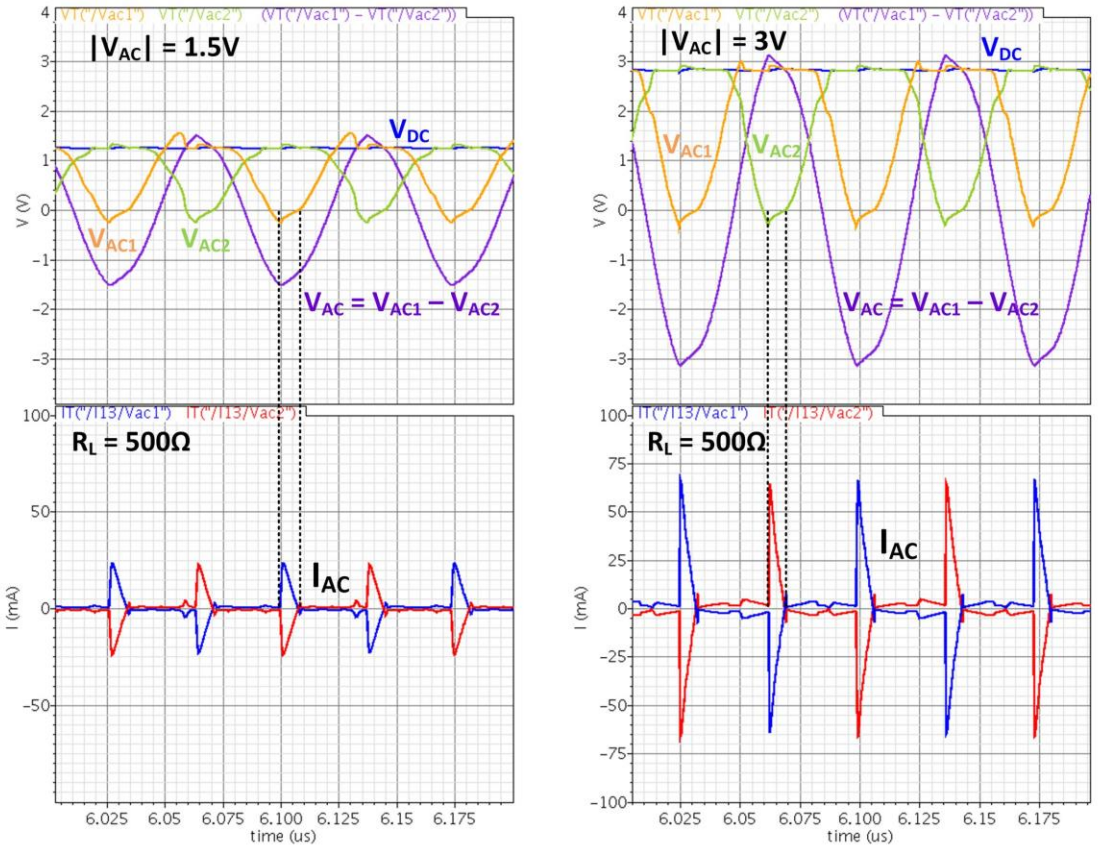



Fig. 4.6 Simulated waveforms of the reconfigurable rectifier in 1X mode with $R_L$ = 500 Ω, and $|V_{AC}|$ = 1.5 and 3 V, respectively.

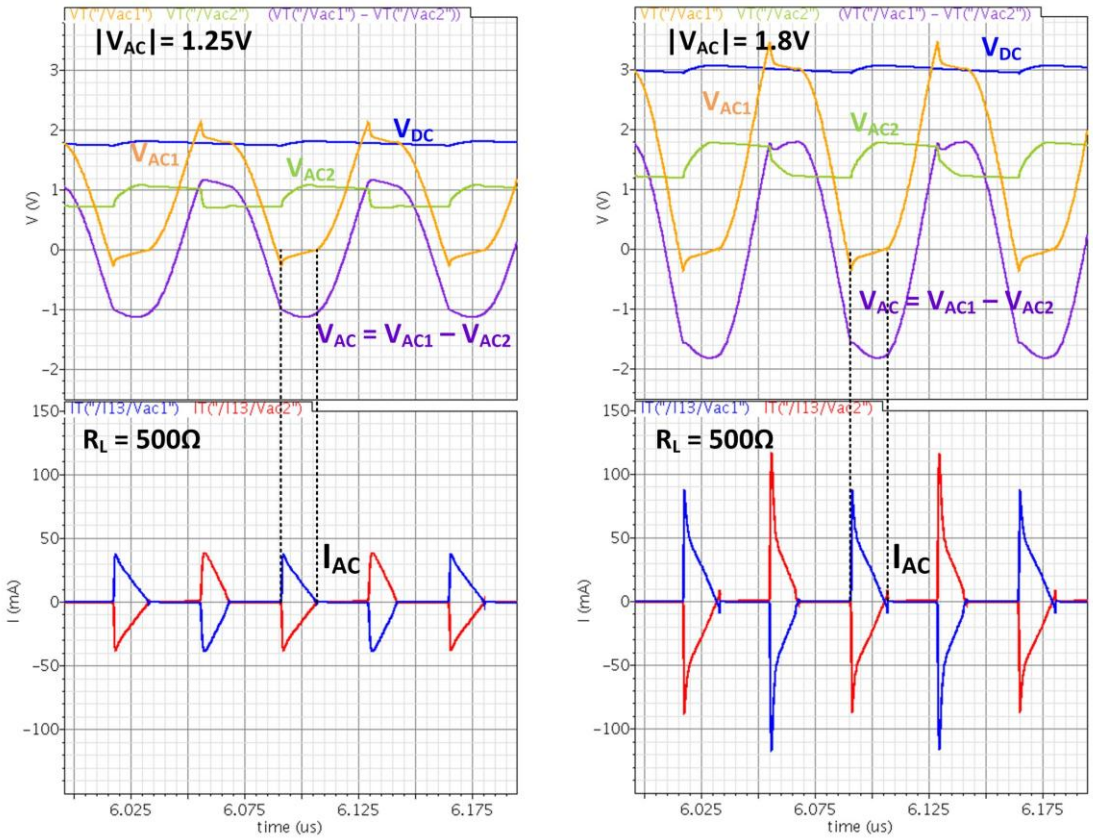



Fig. 4.7 Simulated waveforms of the reconfigurable rectifier in 2X mode with $R_L$ = 500 Ω, and $|V_{AC}|$ = 1.25 and 1.8 V, respectively.

### 4.4 Start-Up of Reconfigurable Rectifier

The start-up process of the reconfigurable rectifier is shown in Fig. 4.8. At the beginning, the active diodes are off, $V_{DC}$ is 0 V, and the Mode pin is M = 0. The output capacitor $C_L$ is charged up by $V_{AC}$ the same way as a passive rectifier does. After $V_{DC}$ is charged up to a specified voltage to activate the bias circuit and the comparators, the rectifier will automatically change to active rectification with M = 1, and the rectifier then operates in the 2X mode and fast charge up $V_{DC}$. When $V_{DC}$ is charged to a sufficiently high level (~3.7 V), a hysteretic comparator commands M = 0 and the rectifier enters the 1X mode. During the mode change when M changes from "1" to "0", the $V_{AC}$ input would fluctuate for a while (~5 μs) as shown in the simulation waveforms in Fig. 4.8. This is due to the change in the equivalent load impedance seen from the primary side during this transition, and the coupled

$V_{AC}$ would consequently change. Eventually, $V_{DC}$ settles to a steady value around 2.8 V in this case. Latch-up problem could be avoided by careful layout.

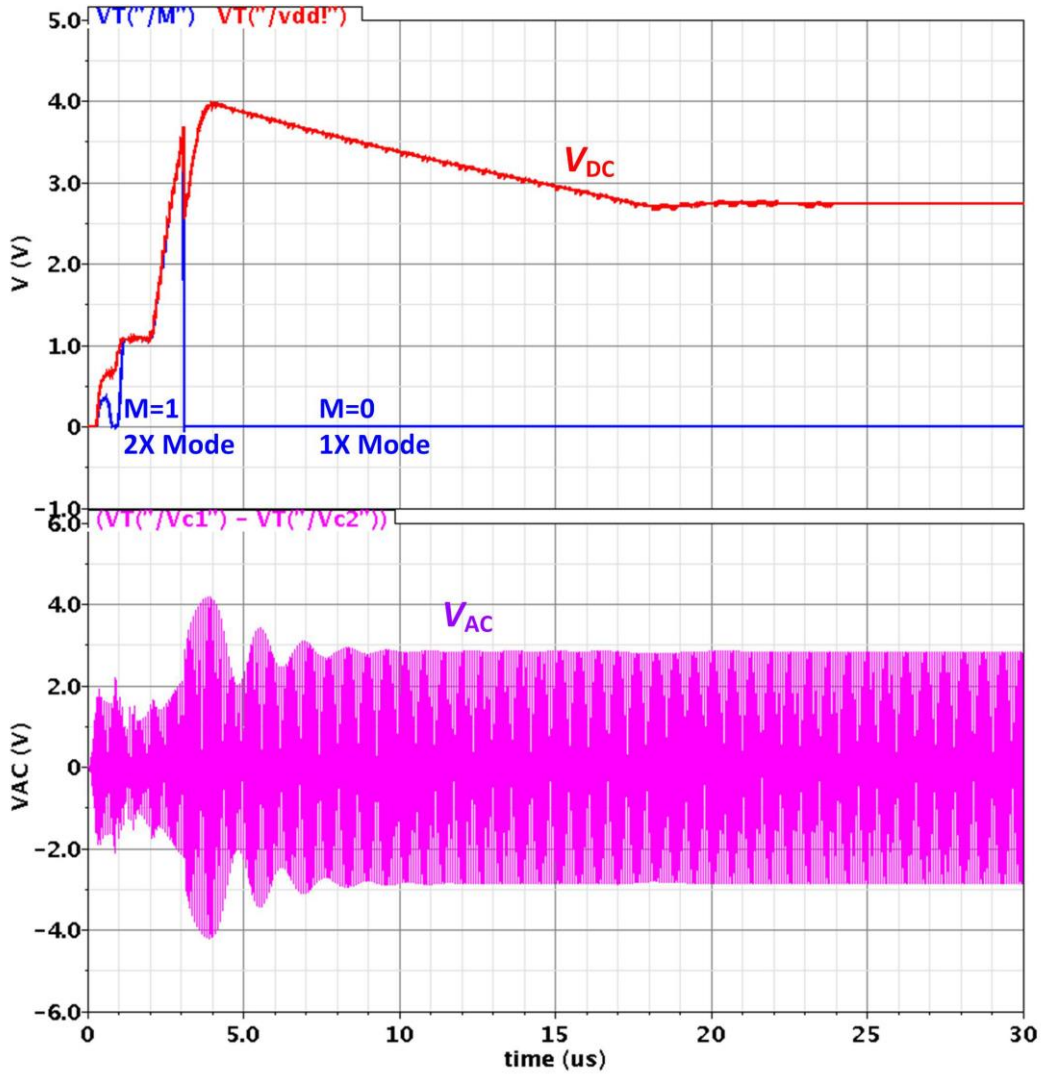



Fig. 4.8 Simulated start-up waveforms of the reconfigurable rectifier with mode selection pin "M" controlled by a hysteretic comparator.

### 4.5 Measurement and Comparison

The proposed 1X/2X rectifier was fabricated in a 0.35 μm CMOS process. The chip micrograph and measurement setup are shown in Fig. 4.9. The active area is 0.1 $mm^2$, and the capacitor area is 1.3 $mm^2$. The flying and output capacitors $C_{fly}$ and $C_L$ are MOS capacitors with a capacitance density of 3.2 $fF/\mu m^2$ that could be much higher for an advanced process

with stacked metal capacitors. The coupling coils $L_1$ and $L_2$ for measurements are 2 cm and 1.8 cm in diameter, respectively. The secondary inductor $L_2$ is 268 nH and resonates with the tuning capacitor $C_2 = C_{2A} + C_{2B}$ of 514 pF at 13.56 MHz.

For verification and characterization, $C_2$ is off-chip for this prototype. Ultimately, $C_2$ should be fabricated on-chip, and $L_2$ could be embedded on substrate or in package. The measured AC input and DC output voltage waveforms in both modes with $R_L$ = 500 Ω and $C_L$ = 4 nF (on-chip) are shown in Fig. 4.10. The worst voltage conversion efficiency occurs at the lowest $|V_{AC}|$ points. The measured voltage waveforms are consistent with the simulated waveforms.

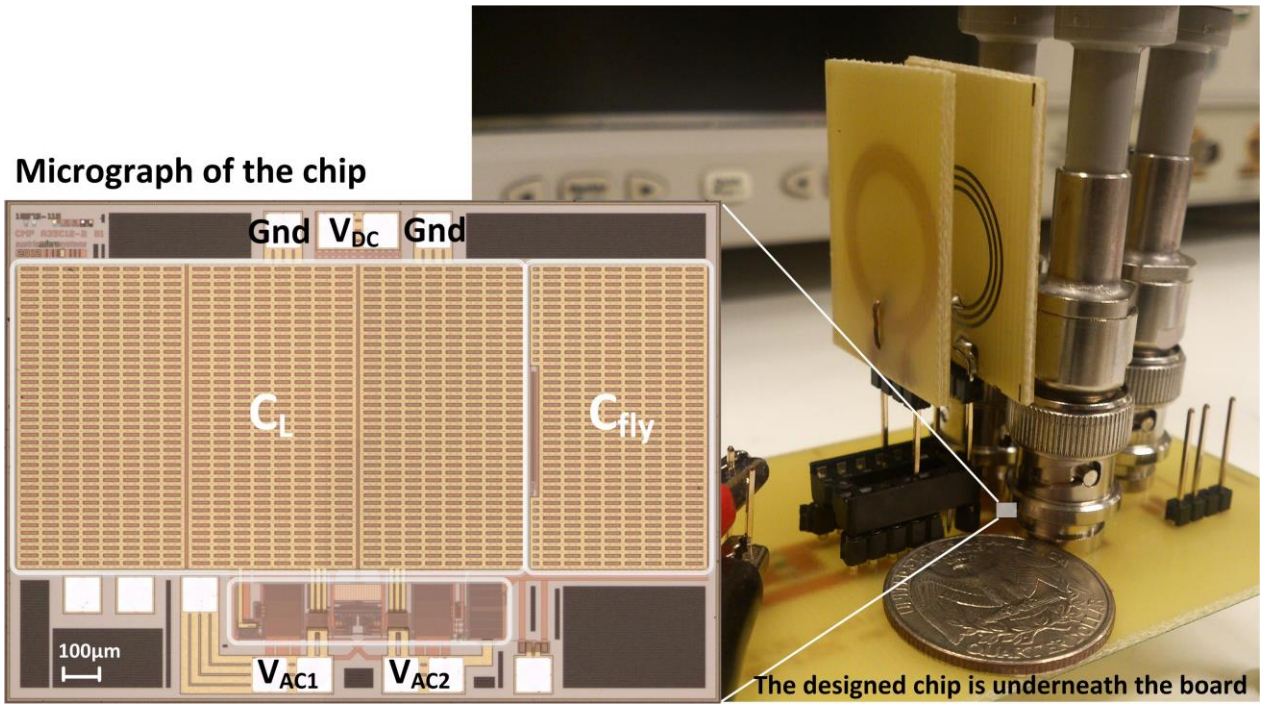



Fig. 4.9 Chip micrograph and measurement setup of Rec3.

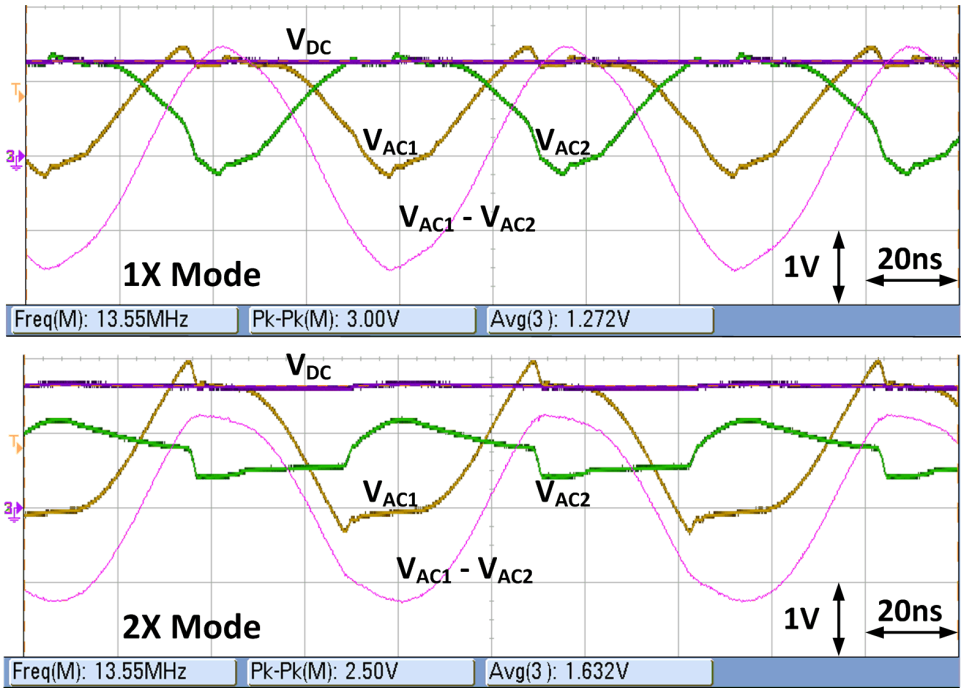



Fig. 4.10 Measured AC input and DC output voltage waveforms in both modes with $R_L$ = 500 Ω and $C_L$ = 4 nF (on-chip) at their lowest $|V_{AC}|$ points.

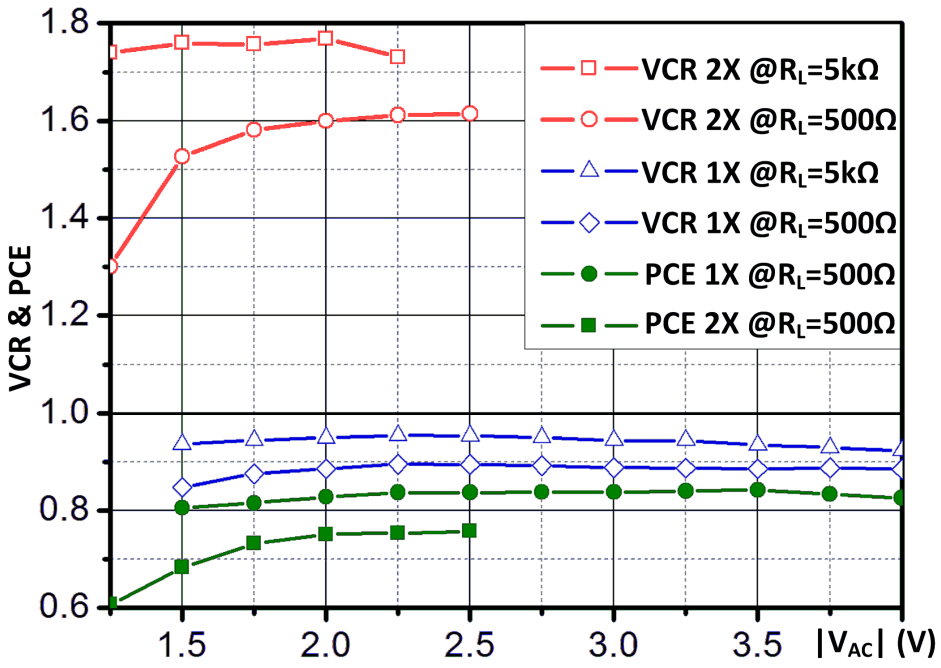



Fig. 4.11 Measured voltage conversion ratios and power conversion efficiencies of the 1X/2X rectifier in both modes.

VCRs and PCEs under different conditions are plotted in Fig. 4.11. With $R_L$ = 500 Ω, the VCR is 0.85 ~ 0.9 in the 1X mode with the QIPV bias current optimized for this case, and is 1.3 ~ 1.61 in the 2X mode. With $R_L$ = 5 kΩ, the VCR is 0.92 ~ 0.95 in the 1X mode, and is 1.73 ~ 1.77 in the 2X mode. For PCE measurements, as discussed in Section 3.5, a 10 Ω resistor is inserted in the input path to measure the AC input current $I_{AC}$. $C_{2B}$ is used to filter the distorted $V_{AC}$ waveforms caused by the 10 Ω resistor during large d$I$/d$t$ (VCR and PCE were measured with different boards). Two identical differential probes with >1 GHz bandwidth are used to measure $V_{AC}$ and $I_{AC}$. The secondary coil $L_2$ resonates with $C_{2A}$ + $C_{2B}$ at 13.56 MHz, with $C_{2B}/C_{2A}$ = 0.15. With $R_L$ = 500 Ω, the PCEs of the 1X and the 2X mode are measured to be 81% ~ 84.2% and 61% ~ 76%, respectively. Table 4.1 summarizes the performance of Rec1, Rec2 and Rec3 with the state-of-the-art designs.

Table 4.1 COMPARISON WITH STATE-OF-THE-ART RECTIFIERS

| | Lam TCAS-II 06 | Cha TCAS-II 12 | Lee ISSCC 12 | **This Work Rec1** | **This Work Rec2** | **This Work Rec3** |
|---|---|---|---|---|---|---|
| Tech. (μm) | 0.35 | 0.18 | 0.5 | **0.35** | | |
| Area ($mm^2$) | 0.107 | 0.009 | 0.585 | **0.04** | **0.065** | **0.1 (w/o $C_L$)** |
| Freq. (MHz) | **13.56** | | | | | |
| $\|V_{AC}\|$ (V) | 1.5- 3.5 | 0.9- 2 | 3.2- 5 (1X)<br>1.7- 2.5 (2X) | **1.5 - 4** | **1.5 – 4** | **1.5 - 4 (1X)**<br>**1.25 - 2.5 (2X)** |
| $C_L$ (nF) | 0.2 | 10,000 | 2,000 | **1.5** | **1.5** | **4** |
| $R_L$ (Ω) | 1.8k | 1k | 500 | **500** | **500** | **500** |
| $V_{DC}$ (V) | 1.2 - 3.2 | 0.45 - 1.78 | 2.5 - 4.3 | **1.13 - 3.5** | **1.2 - 3.5** | **1.27 - 4** |
| Coil (cm) | 6.0 | N/A | 3.0 | **2.0** | **2.0** | **1.8** |
| $P_{OUT,MAX}$ (mW) | 5.76 | 3.2 | 37 | **24.5** | **24.8** | **32** |
| VCR 1X | 0.78 - 0.92 | 0.82 - 0.89 | ~0.84 | **0.74 - 0.88** | **0.79 - 0.89** | **0.85 - 0.9** |
| VCR 2X | N/A | N/A | ~1.41 | **N/A** | **N/A** | **1.3 - 1.61** |
| PCE 1X | 65% - 89% | 60% - 81.9% | 73% - 77% | **82.5% - 90%** | **82% - 90%** | **81% - 84.2%** |
| PCE 2X | N/A | N/A | 64% - 70% | **N/A** | **N/A** | **61% - 76%** |

## 4.6 Conclusion

In this chapter, an area-efficient reconfigurable 1X/2X active rectifier is introduced. The output capacitor $C_L$ was integrated on-chip with a switching arrangement that avoid connecting the output capacitors in series in the 2X mode. The lowest input $|V_{AC}|$ was extended from 1.5 V to 1.25 V in Rec3 by using the reconfigurable architecture, and VCRs and PCEs were improved with proper design of the bias current for reverse current control.

# Chapter 5 SWITCHED-CAPACITOR POWER CONVERTER FOR IMDS

The primary consideration of designing the power management unit (PMU) for implantable medical devices (IMDs) is the integration level. For implanted devices any off-chip components are undesirable. As capacitors and switches can be built fully on-chip, switched-capacitor power converters (commonly known as charge pumps) are more favorably used in IMDs than inductors. As there are many noise-sensitive building blocks (such as the RF receiver, digital-to-analog converter and voltage/frequency references) in the IMDs, well regulated power supplies are needed.

An input-adaptive dual-output charge pump (DOQP) with variable fractional conversion ratio *M* and low dropout regulators (commonly known as LDOs) in cascade is implemented for the PMU of implantable energy harvesting devices [33]. The charge pump has one step-down and one step-up output adaptively converted from a 1.8 to 4.0 V harvested energy source, and the outputs of the LDOs are set at 1 V and 3 V respectively. To improve the overall efficiency, conversion ratios of k/6 (k=2, …, 12) are realized by 1/2- and 1/3-capacitors using an interleaving scheme. The PMU is designed with a 0.13 μm 3.3 V CMOS process, and attains the peak efficiency of 81.3% and a flat efficiency curve over a wide input range.

## 5.1 Input Adaptive Dual-Output Charge Pump with Fractional-*M*

Fig. 5.1(a) shows the conventional implementation of the power management unit in an implanted system. It consists of a resonating secondary *LC* tank, a rectifier, and several LDO regulators for different functional blocks, including neuron recording or stimulating channels, DSP, RF and mixed-signal circuits. A step-up QP is needed when the input voltage is not high enough to support RF transmission or neuron stimulation functions [34]. For wirelessly powered devices, the coupled $|V_{AC}|$ may change by a couple of times due to changes in distance and/or orientation between the primary and secondary coils, and the rectifier DC output voltage $V_{DC}$ would change substantially. The system efficiency is given by

$$\eta_S = \eta_{Link} \times \eta_{Rec} \times \eta_{QP} \times \eta_{LDO}. \quad (5.1)$$

When $V_{DC}$ is high the pass transistors of the LDOs have to sustain large voltage drops, and the efficiencies could be quite low [35]. As a result, the conversion ratio of the QP should be adaptive to the input voltage $V_{DC}$.

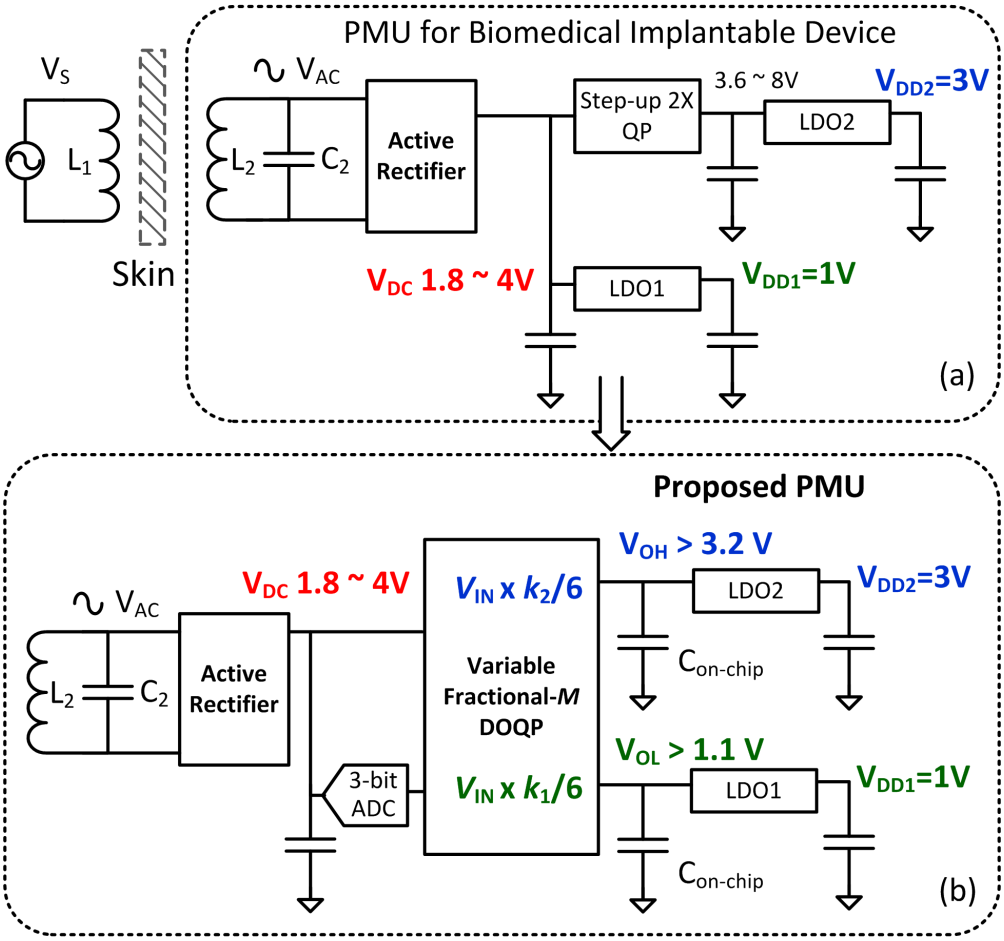



Fig. 5.1 A PMU for biomedical implantable devices: (a) conventional implementation; and (b) proposed implementation.

The proposed PMU, shown in Fig. 5.1(b), provides two voltages $V_{DD1}$ = 1 V and $V_{DD2}$ = 3 V that serve as power supply voltages of downstream functional blocks. A novel dual-output charge pump (DOQP) with variable fractional voltage conversion ratios $M$ is inserted between the rectifier and the LDOs. The DOQP has one step-down output ($V_{OL}$) and one step-up output ($V_{OH}$). The AC input $V_{AC}$ is first converted by the rectifier into the DC voltage $V_{DC}$, which is digitized by a 3-bit analog-to-digital converter (ADC). $V_{DC}$ is between 1.8 V to 4 V under normal conditions, and the logic instructs the DOQP to adaptively change its conversion ratios to give $V_{OL}$ higher than 1.1 V and $V_{OH}$ higher than 3.2 V. The dropout

voltages of the respective LDOs are 100 mV and 200 mV at full loads. This architecture attains higher power conversion efficiency as the LDOs that provide $V_{DD1}$ and $V_{DD2}$, respectively, do not have a large voltage drop, which means that $\eta_{LDO}$ is high. With careful design of the DOQP with variable conversion ratios and $\eta_{QP}$, then $\eta_S$ could be significantly improved within the input range.

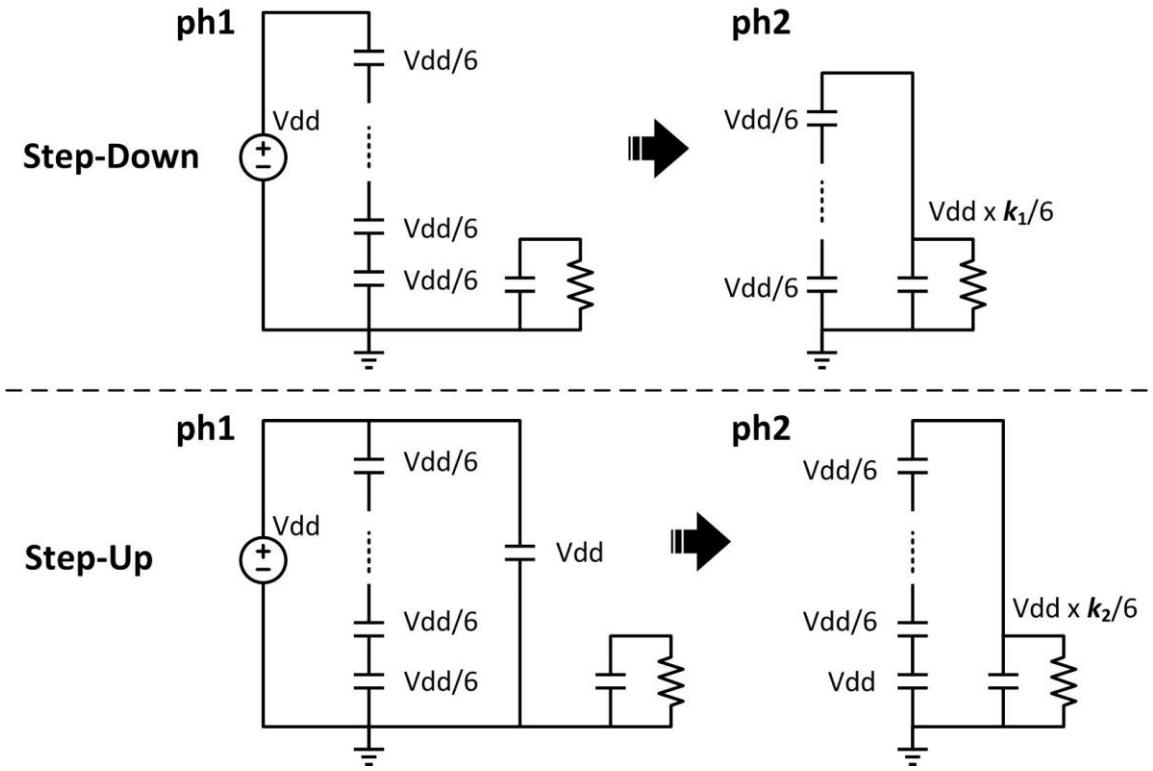



Fig. 5.2 Conventional methods of generating fractional-M step-down or step-up charge pump.

The conversion ratios $M_1$ and $M_2$ of the proposed DOQP adaptively changes with the DC voltage $V_{DC}$. LDO1 is capable of dealing with $V_{OL} = V_{DC} \times k_1/6$ ($k_1$ = 2, 3, 4, 5), and LDO2 is capable of dealing with $V_{OH} = V_{DC} \times k_2/6$ ($k_2$ = 6, 7, ..., 12). As shown in Fig. 5.2, to realize the step-down ratio $M_1 = k_1/6$, six capacitors are needed in conventional implementations for the step-down function only. Another six capacitors are needed to realize the step-up ratio $M_2 = k_2/6$. When n (relaxed) capacitors are connected in series and charged up by $V_{DC}$, the capacitor voltages are $V_{DC}$/n and the conversion ratio is $M$ = 1/n. We label these capacitors as 1/n caps. Note that simply connecting 1/3 and 1/2 caps in series to realize $M$ = 5/6 is not sustainable, because after the two capacitors are discharged as a 5/6 cap in the very first cycle, the voltage on the discharged 1/3 (or 1/2) cap will not be equal to the other un-discharged 1/3

(or 1/2) caps. Governed by the charge balance law [36], [37], after the next charging phase with 1/3 (or 1/2) caps in series, the voltages of each cap will no longer be $V_{DC}/3$ (or $V_{DC}/2$) anymore. Sustainable operation requires all fractional caps be discharged to the same voltage before the next charging cycle. As a result, an interleaving scheme has to be used to evenly discharge each capacitor.

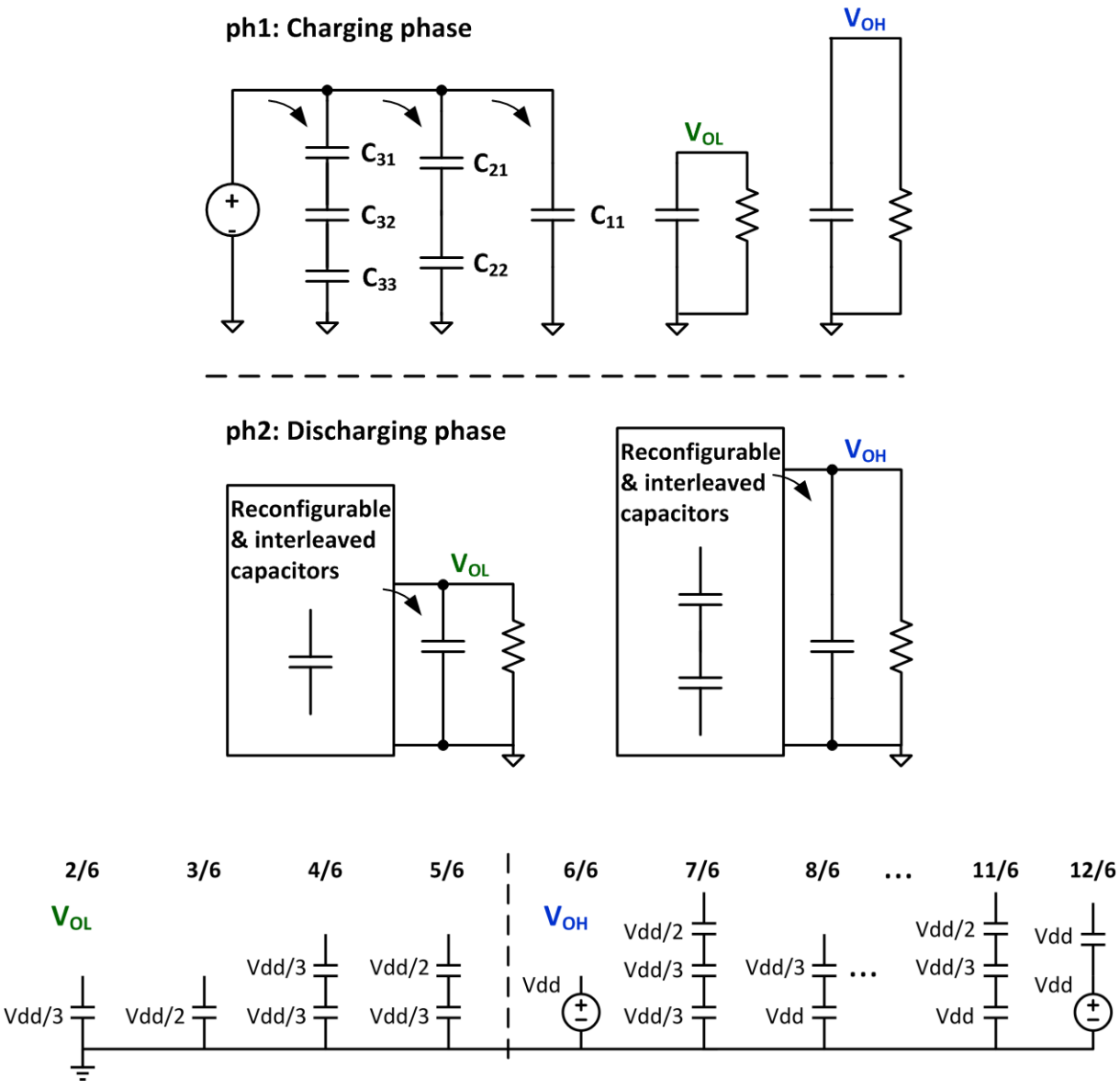



Fig. 5.3 Charging and discharging phases of proposed conversion scheme.

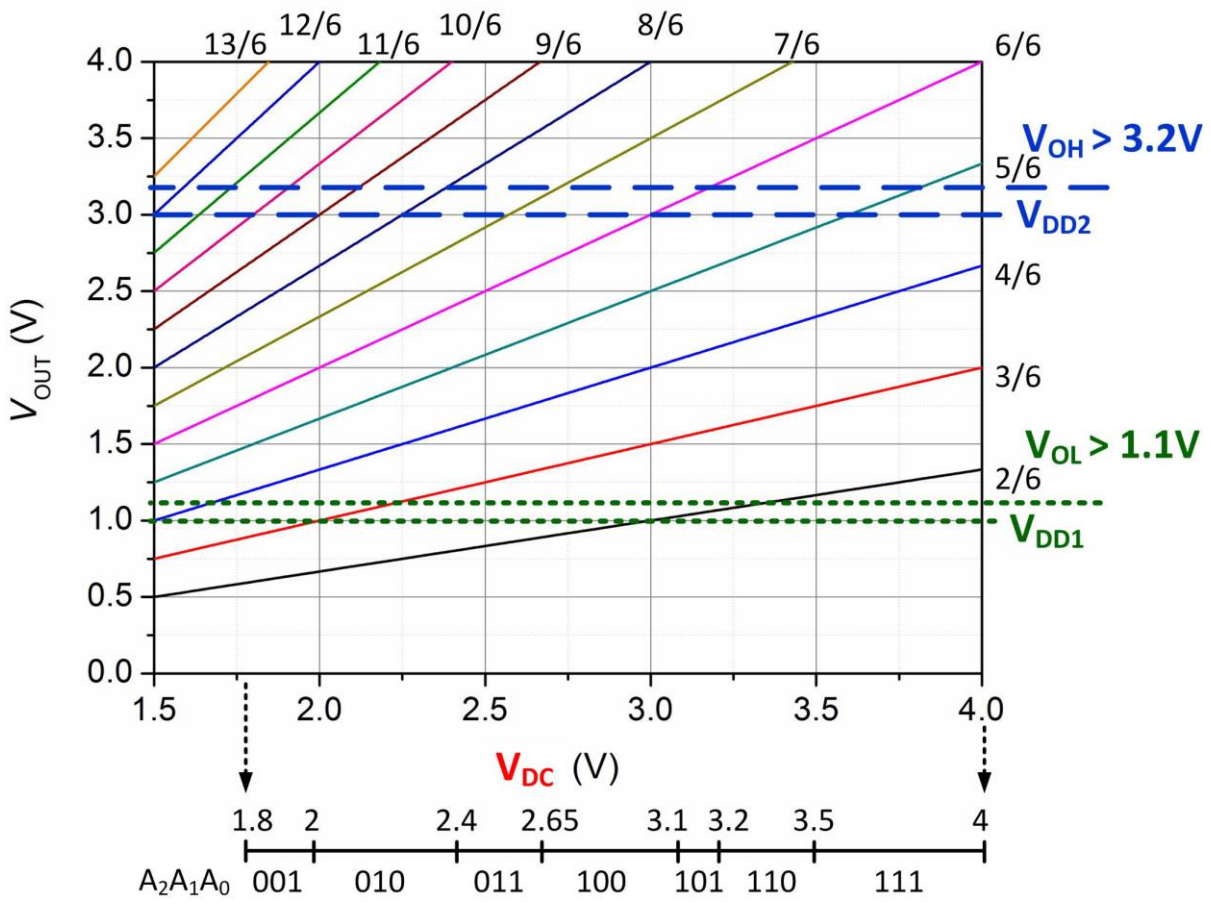



Fig. 5.4 Possible conversion ratio combinations of the proposed DOQP scheme, and the 7 segments of $V_{DC}$ defined for ADC.

Table 5.1 REALIZATION OF EACH *M*

| **$V_{OL}$ Step-down (*ADC Code* )** | 2/6 (*111*) | 3/6 (*110, 101, 100, 011*) | 4/6 (*010*) | 5/6 (*001*) |
|---|---|---|---|---|
| **Caps used** | **1/3** | **1/2** | **1/3+1/3** | **1/2+1/3** |

| **$V_{OH}$ Step-up (*ADC Code*)** | 6/6 (*111, 110*) | 7/6 (*101*) | 8/6 (*100*) | 9/6 (*011*) | 10/6 (*N/A*) | 11/6 (*010*) | 12/6 (*001*) |
|---|---|---|---|---|---|---|---|
| **Caps used** | **1** | **1/2+1/3+1/3** | **1+1/3** | **1+1/2** | **1+ 1/3+ 1/3** | **1+1/2+1/3** | **1** |

As shown in Fig. 5.3, we have three 1/3 flying caps ($C_{31}$, $C_{32}$, $C_{33}$), two 1/2 flying caps ($C_{21}$, $C_{22}$) and one step-up flying cap $C_{11}$, and their conversion ratios are listed in Table. 5.1. The

1.8 to 4.0 V $V_{DC}$ is quantized by a 3-bit ADC into 7 segments ($A_2A_1A_0$ = 001 ~ 111): [1.8 ~ 2 V], [2 ~ 2.4 V], [2.4 ~ 2.65 V], [2.65 ~ 3.1 V], [3.1 ~ 3.2 V], [3.2 ~ 3.5 V] and [3.5 ~ 4 V]. The conversion rate of the ADC is quite low as $V_{DC}$ would only vary slowly. Note that $M$ = 1/3 + 1/3, 1/2 + 1/3 + 1/3 and 1 + 1/3 + 1/3 cannot be realized simultaneously, because four 1/3 caps are needed and there are only three of them. Fortunately, as shown in Fig. 5.4 and Table 5.1, the above mentioned ratios are not necessarily needed, as the existing ratios can already cover the whole input range of $V_{DC}$. In our proposed PMU circuit, the first output voltage ($V_{DD1}$) is selected to be 1 V for the digital circuits, and the second output voltage ($V_{DD2}$) is selected to be 3 V for the analog, RF and stimulation circuits.

## 5.2 Circuit Implementation

The top level schematic of the DOQP with variable fractional conversion ratio is shown in Fig. 5.5. Six flying caps ($C_{31}$, $C_{32}$, $C_{33}$, $C_{21}$, $C_{22}$ and $C_{11}$) are connected with reconfigurable switches. Each of the 1/3 caps is associated with seven switches, while each 1/2 caps is associated with six switches. These switches connect each of the plates of the capacitors to GND, $V_{DC}$, $V_{OL}$, $V_{OH}$ or other capacitors. When the conversion ratio $M$ = 1 is needed, the switches $S_1$ or $S_2$ is turned on by the controller to connect $V_{DC}$ to either $V_{OL}$ or $V_{OH}$. Also, $S_1$ and $S_2$ help with the startup of the circuit, as the input will be directly connected to the outputs when they are low.

To implement $M$ = 1 + 1/3, for example, the 1/3 caps could be connected to either the top or the bottom plate of $C_{11}$. Parasitic capacitors connected to the flying capacitors will be charged and discharged that degrade the efficiency significantly. Therefore, in this design, 1/3 caps are connected to the bottom plates as there are fewer switches and hence smaller associated parasitic capacitance.

There are interleaving flying capacitors connected to both outputs, and the load at one output will discharge them and eventually affect the other output. In the proposed PMU, each output of the DOQP is followed by an LDO, so the cross-regulation between these two outputs can be minimized.

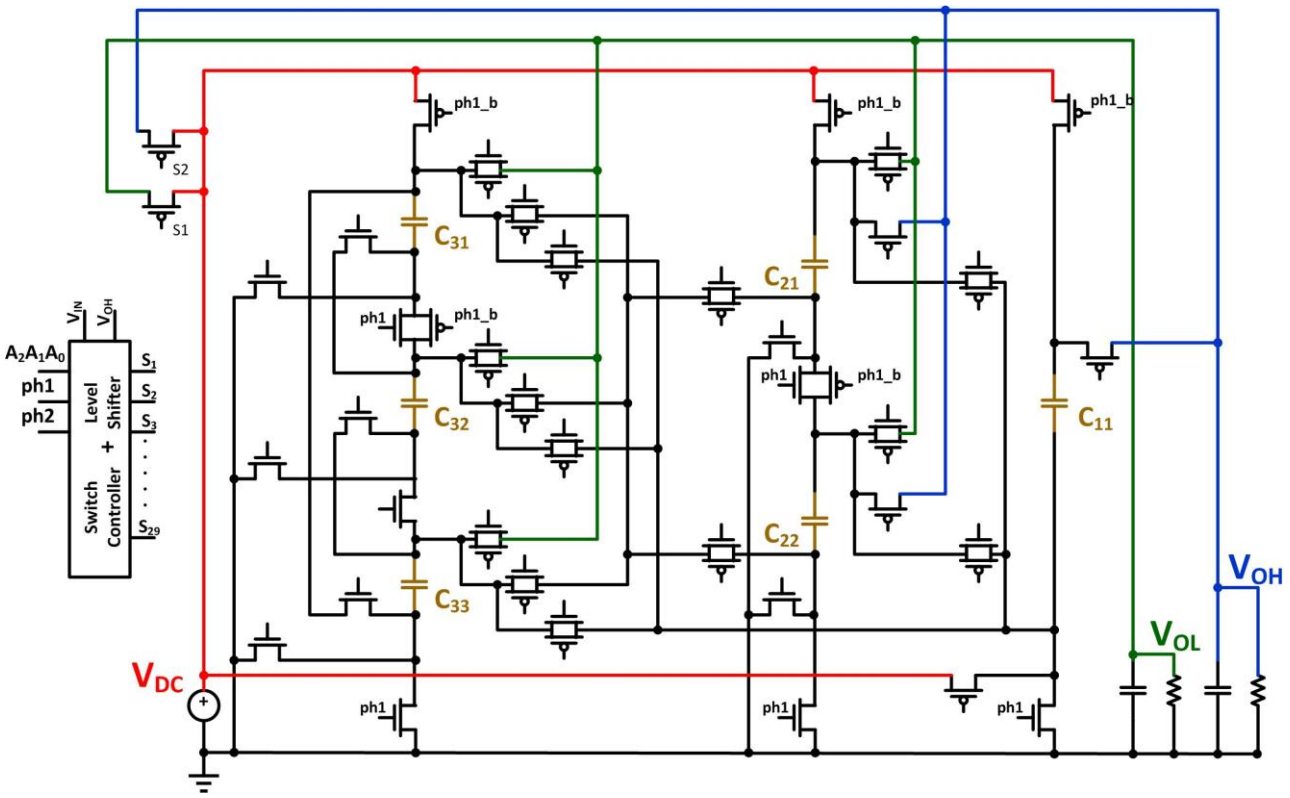



Fig. 5.5 Top level schematic of the variable fractional-*M* DOQP.

The clock generation circuit is shown in Fig. 5.6(a). It has to be reset before the circuit is powered on, and the duration of the reset signal has to be longer than 3 clock periods. The major phase $\phi_1$ is the discharging phase and $\phi_2$ is the charging phase. The charging phase $\phi_2$ is further divided into $\phi_{2\text{-}31}$, $\phi_{2\text{-}32}$ and $\phi_{2\text{-}33}$ for controlling the 1/3 interleaving capacitors; and $\phi_{2\text{-}21}$ and $\phi_{2\text{-}22}$ are used to enable 1/2 caps in charging up the output capacitors. In some input voltage scenarios such as $A_2A_1A_0$ = 010, all three 1/3 caps will be used. The waveforms are shown in Fig. 5.6(b). After the reset signal of all D flip-flops (DFFs) goes to "0", the clock starts ticking, and so does the DOQP.

NMOS switches are used to connect bottom plates to Ground, and PMOS switches are used to connect top plates to $V_{DC}$ and $V_{OH}$. Level shifters are added in the gate drive buffers to control switches that are connected to $V_{OH}$. The n-wells of the PMOS transistors are connected to $V_{DC}$ if the corresponding nodes are never connected to $V_{OH}$; otherwise, they are connected to $V_{OH}$. For connecting internal nodes and $V_{OL}$, CMOS pass gates are used.

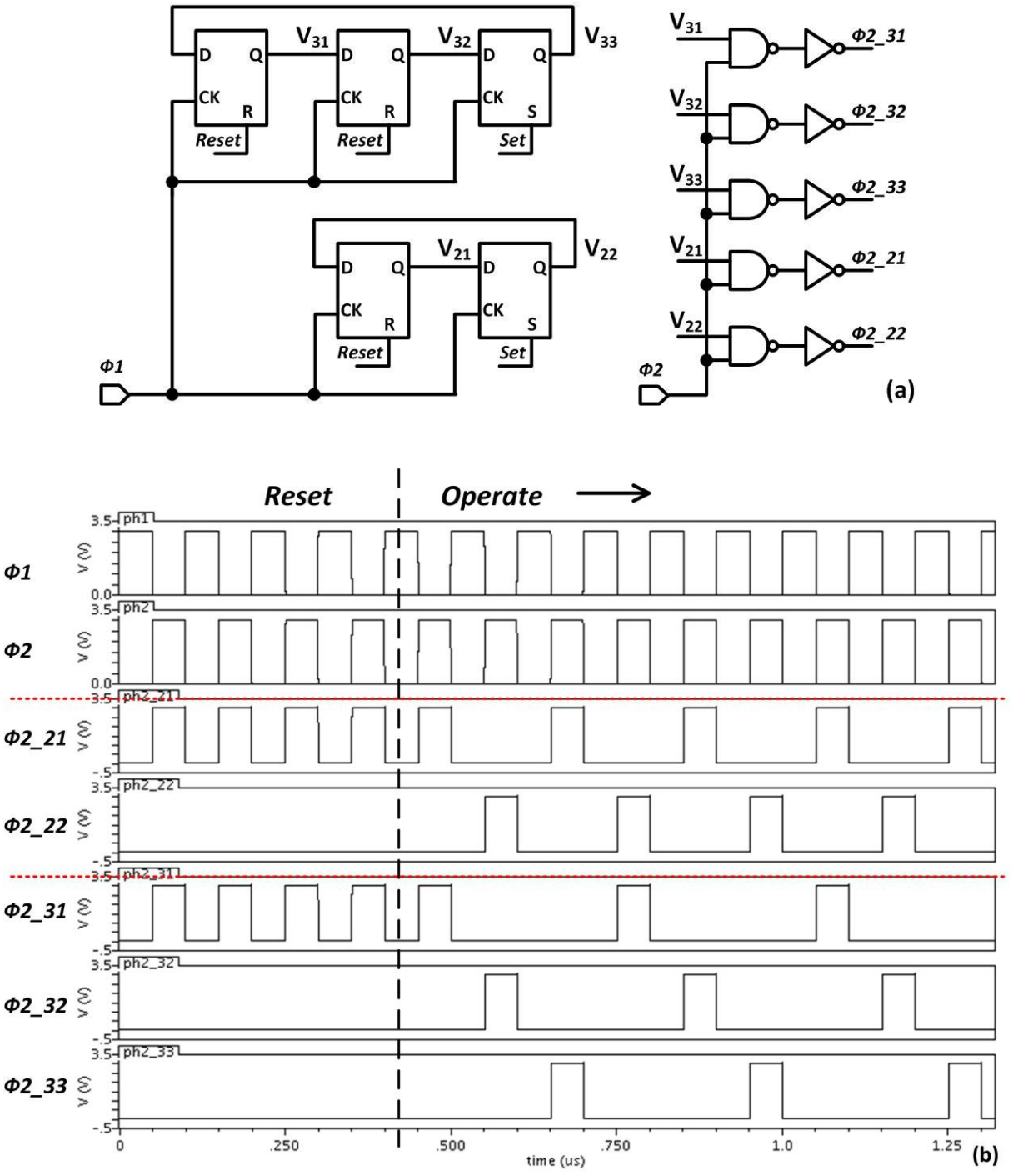



Fig. 5.6 Phase generation circuit for the interleaving scheme (a), and its output waveforms (b).

Passive components, especially capacitors, are very area consuming. The unit capacitance of an MIM capacitor is around 1 fF/μm$^2$, and that of a MOM capacitor (also known as finger capacitor) is around 2 fF/μm$^2$ by using several metal layers simultaneously, for example, Metal 2 to Metal 6 for the technology nodes below 130 nm. To save area, these two types of

capacitors can be stacked together to get a unit capacitance of over 3 fF/μm$^2$. With this assumption, a chip area of 1.2 × 1.2 mm$^2$ can accommodate over 3 nF of capacitance (if 15% of the area is used for peripheral components such as switches, clock and routing). The output filtering capacitors are implemented by MOS capacitors that have much higher unit capacitance. In our design, $C_{31} = C_{32} = C_{33} = 800$ pF, $C_{21} = C_{22} = C_{11} = 400$ pF, and the output capacitors are 500 pF.

### 5.3 Simulation Results

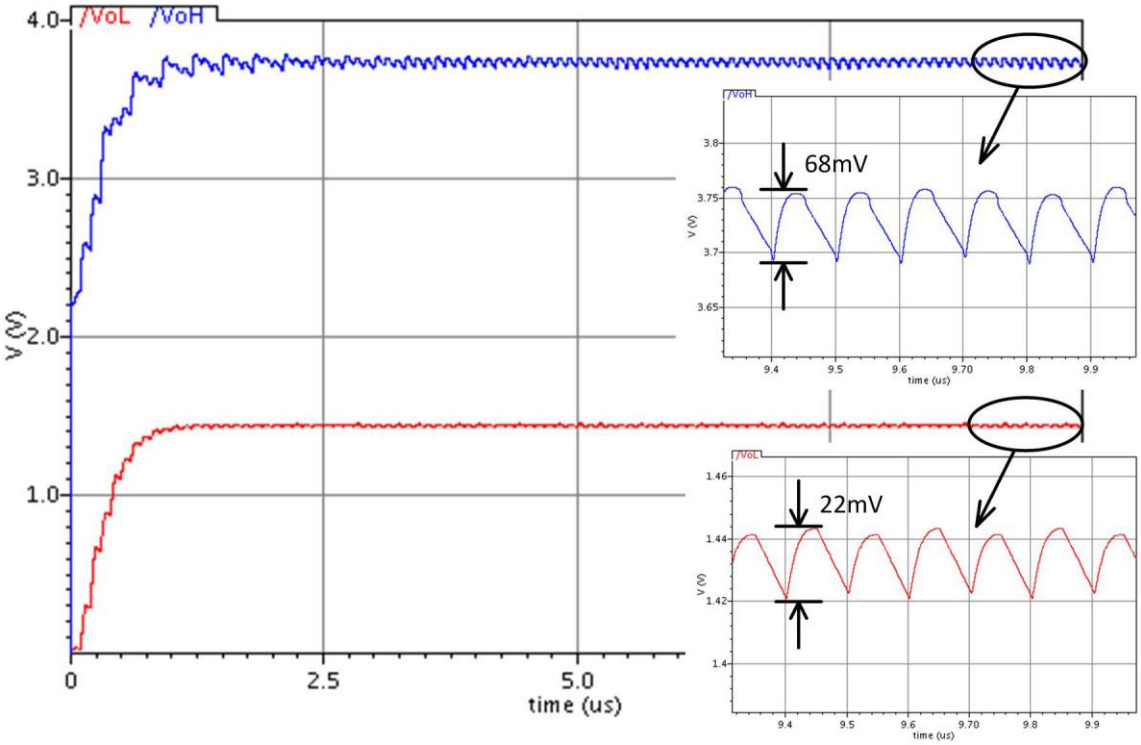



Fig. 5.7 Output waveforms of the DOQP when $V_{DC}$ is 3 V, $I_{OH}$ = 500 μA and $I_{OL}$ = 200 μA respectively.

To verify the functionality of the DOQP with variable fractional conversion ratio, the circuit was simulated with 3.3 V I/O devices in standard 0.13 μm CMOS n-well process. The switching frequency was 10 MHz and the optimum load current was 500 μA for $V_{OH}$, and 200 μA for $V_{OL}$. The chip area was estimated to be 1.2×1.2 mm$^2$ by assuming MIM and MOM capacitors were stacked together as discussed above. Switches were designed to have minimum sizes that guaranteed near-complete charge transfer in every half cycle when

operating at 10 MHz clock frequency. Minimizing the switch sizes would increase the conversion efficiency by reducing the parasitic capacitance [37].

Fig. 5.7 shows the output waveforms of the DOQP when $V_{DC}$ is 3V, $M_1$ = 1 + 1/3 for $V_{OH}$ and $M_2$ = 1/2 for $V_{OL}$ ($A_2A_1A_0$ = 100). The output voltage ripples are 68 mV and 22 mV respectively. Fig. 5.8 shows the efficiency of the DOQP as well as the PMU efficiency versus the input voltage $V_{DC}$. When calculating the PMU efficiency for the plot, ideal LDOs were cascaded with the DOQP. Also, comparison between proposed PMU and the conventional PMU (with ideal QP and LDOs) is shown in Fig. 5.8. Good conversion efficiencies were achieved in this design over a wide input range, and the peak efficiency of 81.3% was obtained at $V_{DC}$ = 3.2 V.

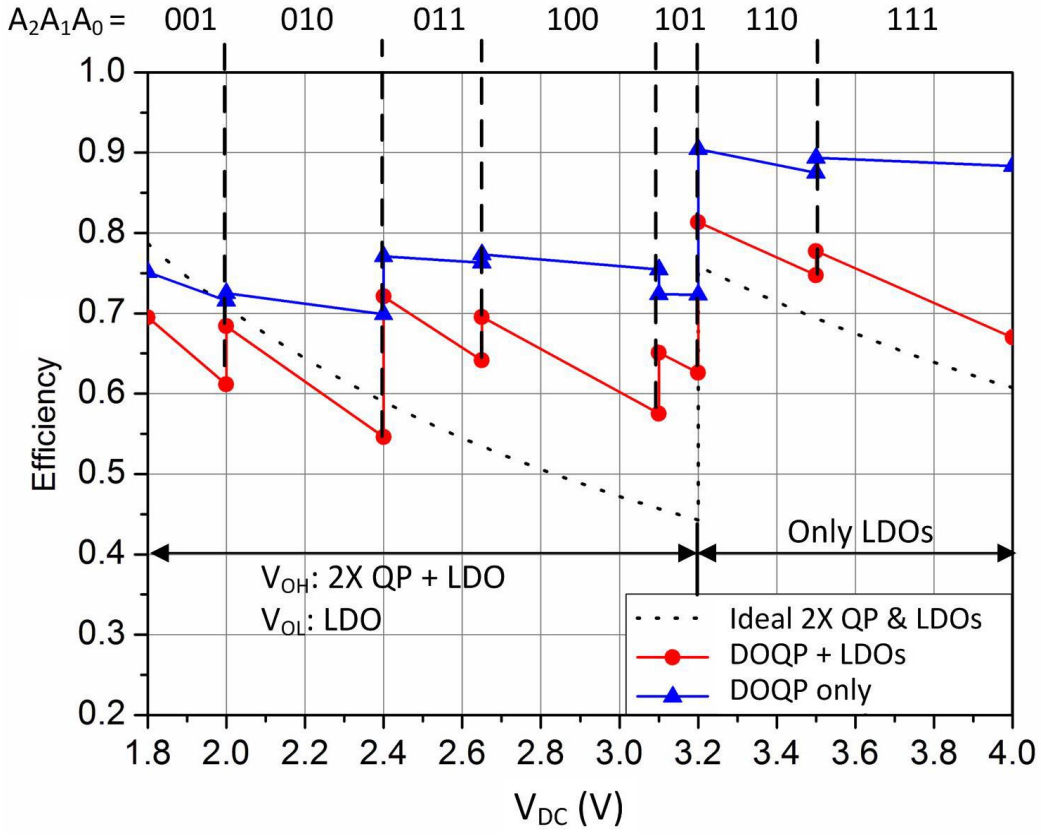



Fig. 5.8 Efficiencies of the proposed PMU and the ideal conventional PMU.

Note that, for a charge pump, the ideal unity efficiency with $V_{OUT} = M_{ideal} \times V_{IN}$ of a QP only occurs under the no load condition [38]. When the load current $I_O$ is $0^+$, the efficiency drops to zero because the output power is zero but $V_{OUT}$ is still equal to $M_{ideal} \times V_{IN}$. The efficiency

then increases as $I_O$ increases until reaching the optimum loading, but $V_{OUT}$ keeps dropping monotonously. Thus, to optimize the power conversion efficiency, the relationship between the input voltage and *M* needs to be defined carefully.

### 5.4 Conclusion

In this chapter, a dual-output charge pump with variable fractional-*M* is proposed. It is inserted between the rectifier and the LDOs in the PMU for inductively coupled wireless power transfer. Interleaving scheme is used to control the fractional capacitors such that the conversion ratio can assume many values according to change in the input voltage. Simulation results show that the efficiency of the PMU is improved over a wide input range.

# Chapter 6 FULLY-INTEGRATED LDO WITH DC-TO-20GHZ POWER-SUPPLY-REJECTION

Low-dropout regulators (LDOs) are indispensable building blocks in system-on-chips (SoCs) due to its low noise, small quiescent current, fast response and good power-supply-rejection (PSR) characteristics. In general, analog circuit loads require the LDO to have high PSR, while digital circuit loads require the LDO to response with fast load transient current. Low-dropout regulators that are fully-integrated and area-efficient are highly desirable for point-of-load power delivery. In addition, supplying power to individual noise-sensitive and/or noise-generating building blocks with separate LDOs can improve the system performance significantly. In particular, on-chip LDOs with PSR up to the GHz range are in high demand for wideband communication systems [39].

## 6.1 Fully Integration of LDO

Off-chip capacitors are conventionally connected to the power supply outputs for filtering purposes. Recently published LDOs that require off-chip capacitors (that is, not fully-integrated) are summarized and compared in Table 6.1. With a large capacitor, say 1 μF, small load transient ripples can be achieved using bandwidth extension techniques such as load-current dependent boost current [40], dynamically-biased buffer impedance attenuation [41], adaptively-biased super current mirror [42], and multiple small-gain stages with nanometer process [43]; while high PSR can be achieved with feed-forward ripple cancellation technique [44]. However, for fully-integrated LDOs, large load capacitors are no longer available, and performance of both transient response and PSR will degrade significantly, as discussed below.

Many fully-integrated LDOs with limited on-chip capacitance (a.k.a. output capacitor-less) have been proposed in the past decade [45]-[54]. To make a comparison, a figure-of-merit (FOM) of LDO is defined in [24], and widely adopted by other researchers, that is

$$\text{FOM} = T_R \frac{I_Q}{I_{MAX}} = \frac{C \times \Delta V_{OUT}}{I_{MAX}} \times \frac{I_Q}{I_{MAX}}, \quad (6.1)$$

Table 6.1 COMPARISON OF LDOS WITH OUTPUT CAPACITOR

| Author | Al-Shyoukh | Lam | El-Nozahi | Ho | Harwood |
|---|---|---|---|---|---|
| **Publication** | JSSC 2007 | ISSCC 2008 | JSSC 2009 | JSSC 2010 | ISSCC 2012 |
| **Technology** | 0.35µm | 0.35µm | 0.13µm | 90nm | 40nm |
| $V_{OUT}$ | 1.8V | 0.9V | 1V | 0.9V | N/A |
| **Dropout Voltage** | 200mV | 150mV | 150mV | 100mV | 150mV |
| $I_Q$ | 20µA | 4 to 164µA | 50µA | 9.3µA | N/A |
| $I_{O,MAX}$ | 200mA | 50mA | 25mA | 50mA | N/A |
| $C_L$ | 1µF* | 1µF | 4µF | 1µF | N/A |
| **PSR** | N/A | -50dB @1MHz | -56dB* @10MHz | -35dB @10MHz | -30dB @1.5GHz |
| $\Delta V_{OUT}$ @ $T_{Edge}$ | 54mV @100ns | 6.6mV @10ns | 10mV @10ns | 10mV @10ns | N/A |
| **Load Regulation** | 34mV | 3mV | N/A | 4.1mV | N/A |
| $T_R$ | 270ns | 132ns | 1600ns | 200ns | N/A |
| **FOM** | 27ps | 10.6ps | 3200ps | 37.2ps | N/A |

*The advantages are highlighted with GREEN color, while the disadvantages are in RED.

where $I_Q$ is the quiescent current, and the response time $T_R$ is a function of total on-chip capacitance $C$, load-transient undershoot of the output voltage $\Delta V_{OUT}$ and maximum load current $I_{MAX}$. State-of-the-art fully-integrated LDOs are listed and compared in Table 6.2. To achieve full integration, some specifications have to be sacrificed. A considerably large current (6%) was used to drive the non-dominant poles to high frequencies in [46], resulted in 94% current efficiency. A cascaded structure with 600 mV dropout voltage was employed in [47] that significantly improved the PSR performance, but also considerably degraded the transient response. A single-transistor-control LDO based on the flipped voltage follower (FVF) topology provided stable voltage regulation at various output capacitor conditions including the output capacitor-less condition in [48], but it was sensitive to process, voltage and temperature (PVT) variations, and was not fast enough with 160 mV load-transient undershoots observed. The flipped voltage follower was also employed in [49] with slew-rate

enhancement circuit that responded to 100 ns load transient edges; however, its PSR degraded to 0 dB before 1 MHz. An ultra-fast response comparator-based regulator in 45 nm SOI process was proposed in [50] that consumed 12 mA of quiescent current and required an on-chip deep-trench capacitor of 1.46 nF, but its intrinsic 10 mV ripple is not suitable for supplying RF/analog front-end systems.

Table 6.2 COMPARISON OF FULLY-INTEGRATED LDOS

| Author | Leung | Hazucha | Gupta | Man | Guo | Bulzacchelli |
|---|---|---|---|---|---|---|
| **Publication** | JSSC 2003 | JSSC 2005 | ISSCC 2007 | TCAS1 2008 | JSSC 2010 | JSSC 2012 |
| **Technology** | 0.6µm | 90nm | 0.6µm | 0.35µm | 90nm | 45nm SOI |
| $V_{OUT}$ | 1.3V | 0.9V | 1.2V | 1V | 0.5 to 1V | 0.9 to 1.1V |
| $V_{DO}$ | 200mV | 300mV | 600mV | 200mV | 200mV | 85mV |
| $I_Q$ | 38µA | 6mA | 50µA | 95µA | 8µA | 12mA |
| $I_{O,MAX}$ | 100mA | 100mA | 5mA | 50mA | 100mA | 42mA |
| $C_L$ | 12pF | 600pF | 60pF | 20pF** | 50pF | 1.46nF |
| **PSR** | -30dB @1MHz | N/A | -27dB @50MHz | N/A | 0dB @1MHz | N/A |
| $\Delta V_{OUT}@T_{Edge}$ | 180mV @500ns | 90mV @100ps | 937mV | 160mV @200ns | 114mV @100ns | N/A |
| **Load Reg.** | ±0.25% | 90mV | N/A | 14mV | 10mV | 3.5mV |
| $T_R$ | 2000ns | 0.54ns | N/A | ~300ns | N/A | 0.288ns* |
| **FOM** | 760ps | 32ps | N/A | N/A | N/A | 62.4ps* |

* Simulated result

** Parasitic capacitance of the voltage probe

From the literature review above, we conclude that there is a gap between the performances of fully-integrated and non-fully-integrated LDOs. An area-efficient ultra-fast response LDO with full spectrum power supply rejection is highly demanded. In this chapter, a tri-loop LDO is proposed that achieves an FOM of 3.01 ps and PSR of lower than -12 dB over the whole spectrum (DC to 20GHz). The basic idea of this design is to take advantage of the advanced 65 nm process by keeping most of the limited available capacitance at the output node for better PSR and transient response, and pushing the internal poles to frequencies higher than the unity-gain frequency by using buffer impedance attenuation (BIA) and flipped voltage follower (FVF) techniques. Consequently, the performance is improved with process scaling.

In the proposed tri-loop architecture, the BIA technique is integrated into the FVF structure with the output node being the dominant pole, and a tri-input error amplifier (EA) is proposed to improve the DC accuracy.

### 6.2 Dominant Pole Considerations

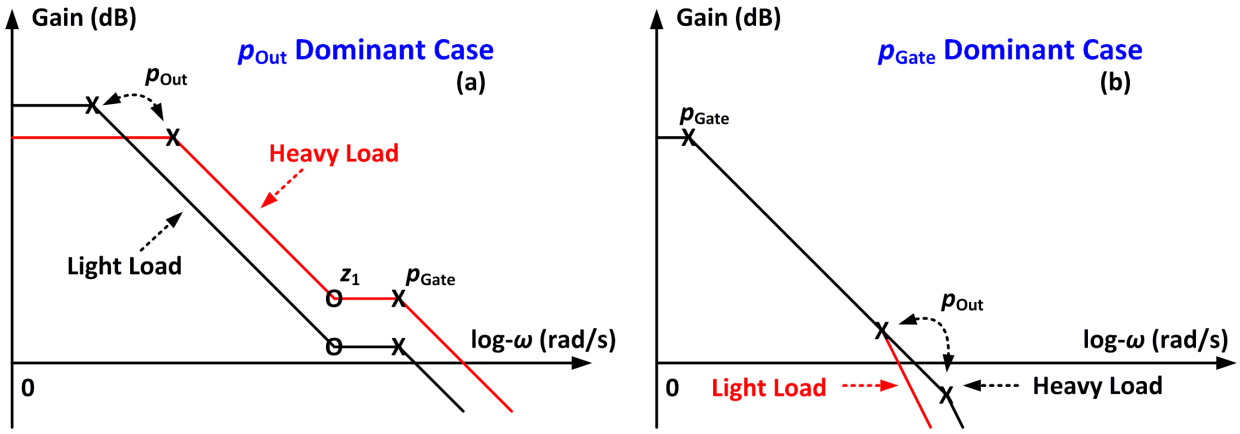



Fig. 6.1 Magnitude plot of a generic LDO with two low frequency poles: (a) with $p_{Out}$ being its dominant pole; and (b) with $p_{Gate}$ being its dominant pole.

Table 6.3 LDO CATEGORIZATION BY INTEGRATION LEVEL AND DOMINANT POLE LOCATION

| **Integration** | **with Off-Chip Capacitor** | | **Fully-on-Chip** | |
|---|---|---|---|---|
| **Dominant pole** | Internal node | Output node | Internal node | Output node |
| **Transient $\Delta V_{OUT}$** | Small | Small | large | Med. |
| **PSR** | Med. | High | Low | Med. |
| **UGF** | Low | Med. | Med. | High |
| **$I_Q$** | Low | Med. | Med. | High |
| **Limit on $I_{O,MIN}$** | Yes | No | Yes | No |
| **Process Scaling** | No | Yes | No | Yes |

For an LDO, the largest capacitors are the output filtering capacitor $C_L$ and the parasitic gate capacitor $C_{Gate}$ of the power MOS transistor. Hence, there are at least two low-frequency (LF) poles: the output pole $p_{Out}$, and the pole at the gate of the power MOS $p_{Gate}$, as sketched in Fig. 6.1 with either $p_{Out}$ or $p_{Gate}$ being the dominant pole. The pole frequency $p_{Out}$ would shift to a

lower frequency when the load resistance increases and vice versa. Basically, LDOs with an off-chip filtering capacitor are designed to be $p_{Out}$ dominant, while all fully-integrated analog "capacitor-less" LDOs have an internal dominant pole $p_{Gate}$. Thus, LDOs can be classified by the need for an off-chip capacitor or not, or they can be classified by being output-pole dominant or internal-pole dominant. Therefore, there are 4 combinations of which the pros and cons are summarized in Table 6.3 and discussed as follows.

There are many benefits in designing $p_{Out}$ as the dominant pole by using most of the available capacitance at the output node. First of all, a larger output capacitor filters out power supply noise and glitches and serves as a buffer for load-transient current changes, resulting in a smaller $\Delta V_{OUT}$. Second, as argued in [55], because the output voltage is well regulated by the control loop at low frequency, and the noise is bypassed to ground by $C_L$ at high frequency, the worst case PSR would occur at medium frequency. Thus, increasing both the output capacitance and the loop bandwidth (that is, the unity gain frequency UGF) would improve the PSR. Third, $p_{Out}$ moves to lower and lower frequency as the load current decreases, reducing the loop bandwidth significantly. In fact, the zero-load condition is not even discussed in many output-capacitor-less designs, and instead, a minimum load current ($I_{O,MIN}$) is needed to satisfy stability requirements. If $C_L$ is reduced to satisfy stability requirements, the high frequency PSR performance will be degraded, and is not acceptable in our application.

For the $p_{Out}$ dominant case, pole-zero cancellation is usually used to extend the loop bandwidth and to enhance the stability. The zero $z_1$ may be generated by the equivalent series resistance (ESR) of $C_L$ or by a high-pass feedback network as proposed in [45]. Alternatively, the non-dominant pole $p_{Gate}$ may be pushed to frequencies higher than the UGF by circuit techniques mentioned in [40]-[43]. The only drawback with $p_{Out}$-dominant is that a relatively high quiescent current is needed to push the internal poles to higher frequencies. This requirement can be relaxed by using advanced processes that have lower parasitic capacitance. The transistors will have smaller feature sizes, and the internal poles could be moved to higher frequencies with the same bias current. At the same time, smaller $C_L$ can be used and results in smaller chip area and higher UGF. To summarize, designing the dominant pole at the output node of an LDO enjoys process scaling that is one of the most desirable characteristics in integrated-circuit design.

## 6.3 Circuit Topologies

### 6.3.1 Flipped Voltage Follower

The replica biasing technique is widely used in source-follower based or flipped-voltage-follower (FVF) based LDOs for supplying power to digital ICs with ultra-fast load-transient responses [56], [46]. The schematic of a single-transistor-control LDO based on FVF in [48] is shown in Fig. 6.2 as an example. This circuit can be divided into three parts: the error amplifier (EA), the $V_{SET}$ generation and the flipped voltage follower. For simplicity, we assume $I_1 = I_2$ and $(W/L)_7 = (W/L)_8$. The mirrored voltage $V_{MIR}$ is controlled to be equal to $V_{REF}$ by the EA, and $V_{SET}$ is generated from $V_{MIR}$ by the diode-connected $M_7$. Followed by a FVF, $V_{OUT}$ is set by $V_{SET}$ through $M_8$, and it is a mirrored voltage of $V_{MIR}$. In the FVF, $M_8$ act as a common-gate amplifying stage from $V_{OUT}$ to $V_G$.

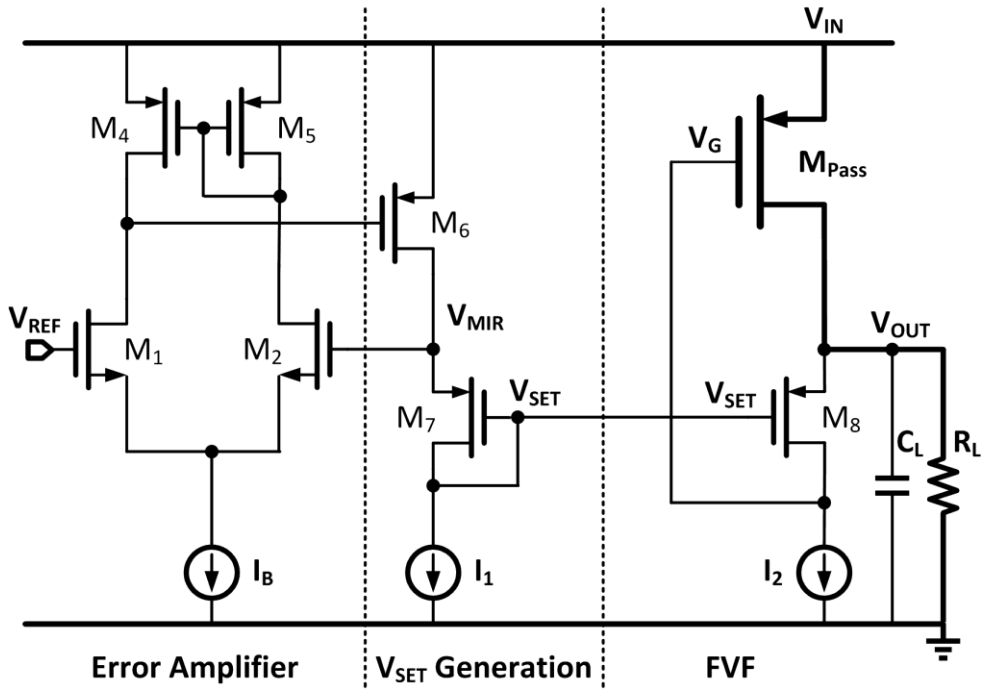



Fig. 6.2 The single-transistor-control LDO regulator based on the FVF topology.

Obviously, there are two low-frequency poles ($p_{Gate}$ and $p_{Out}$) in the FVF when a relatively large on-chip $C_L$ (ranging from 100 pF to 1 nF) is used to handle the load current that ranges

from 0 to 10 mA. This topology is very difficult (if not impossible) to be stable if $p_{Out}$ is the dominant pole. In [48], $p_{Gate}$ dominant is adopted using a small $C_L$ (or even no $C_L$). In [46], $p_{Gate}$ dominant is also adopted with an ESR zero. Adaptive voltage positioning by intentionally setting $V_{OUT}$ to a lower value at heavy load has been used. However, lower $V_{OUT}$ is undesirable for analog loads.

Another issue associated with this structure is the DC accuracy of $V_{OUT}$. The offset voltage between $V_{REF}$ and $V_{OUT}$ can be divided into two parts. First, there is an offset between $V_{REF}$ and $V_{MIR}$ that consists of systematic and random offsets of the EA. Second, the mismatches between the voltage mirror ($M_7$ and $M_8$) and the bias currents ($I_1$ and $I_2$) will generate an offset between $V_{MIR}$ and $V_{OUT}$. Hence, the FVF-based topology has low immunity to PVT. Moreover, the loop gain of the FVF is low, which results in poor load regulation. Nevertheless, due to its fast transient response, the FVF structure is used as the starting point, and improvements will be discussed in Section 6.4.

### 6.3.2 Buffer Impedance Attenuation

To realize the LDO with $p_{Out}$ dominant, $p_{Gate}$ in Fig. 6.2 should be pushed to high frequency not only by using large bias current $I_2$ but also with additional circuitry. A buffer can be inserted between the gain stage with high output impedance and the power stage with large input capacitance [41], as shown in Fig. 6.3. The buffer presents low input capacitance to $V_A$ and low output impedance to $V_G$, pushing the two poles at $p_A$ and $p_{Gate}$ to very high frequencies. In this design, the output capacitor $C_L$ is 130 pF, the bias current $I_2$ is 20 μA, and the buffer consumes another 20 μA, and all the above help pushing $p_{Gate}$ to the GHz range. The remaining problem is the low DC accuracy of $V_{OUT}$ as the buffer has unity gain or slightly lower than unity gain that would worsen the problem.

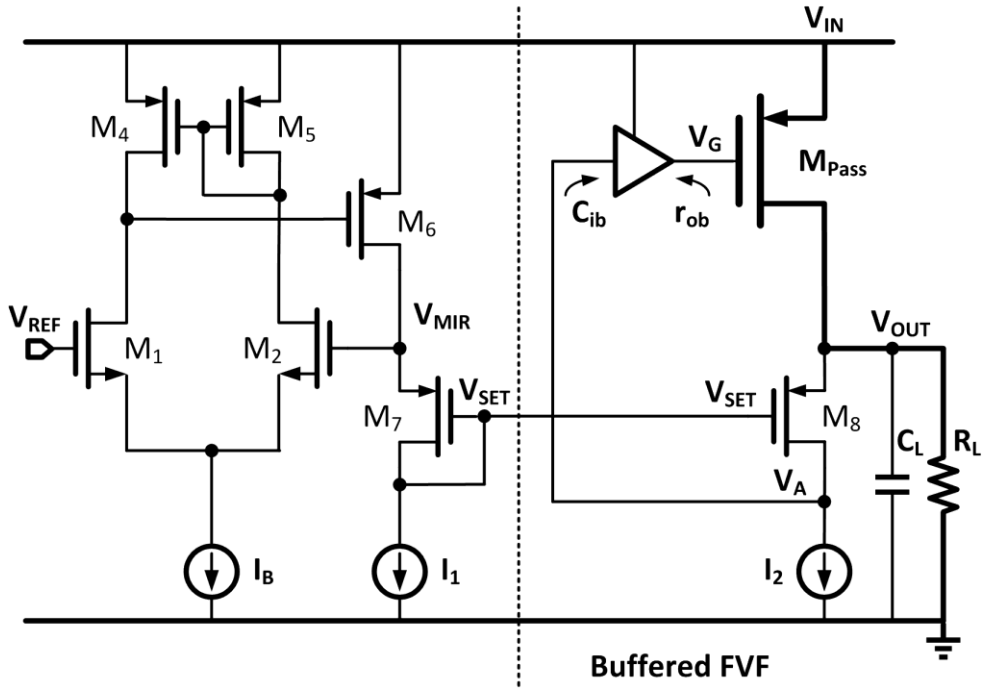



Fig. 6.3 The FVF based LDO regulator with inserted buffer.

### 6.4 Circuit Implementation and Analysis

Based on the previous introduced circuit topologies, in this research, a fully-integrated tri-loop low-dropout regulator designed in a 65 nm CMOS general purpose (GP) process is proposed that achieves ultra-fast transient response and full spectrum (DC to 20GHz tested) power supply rejection with limited chip area, current budget and voltage headroom [57]. The transistor-level schematic is shown in Fig. 6.4.

#### 6.4.1 Tri-Loop Architecture

To increase the DC accuracy of the FVF-based LDO, a third loop is introduced through using a tri-input EA. In previous architectures, only $V_{MIR}$ is fed forward to generate $V_{OUT}$, and $V_{OUT}$ is not fed back to the EA. Now, the EA compares $V_{REF}$ with both $V_{MIR}$ and $V_{OUT}$, and the $W/L$ ratios of the three input transistors $M_1$, $M_2$ and $M_3$ are $(W/L)_1 : (W/L)_2 : (W/L)_3 = 4 : 1 : 3$ such that $V_{OUT}$ is computed to be

$$\left( V_{REF} - \frac{1}{4} V_{MIR} - \frac{3}{4} V_{OUT} \right) \times A_{EA} = V_{OUT} \tag{6.2}$$

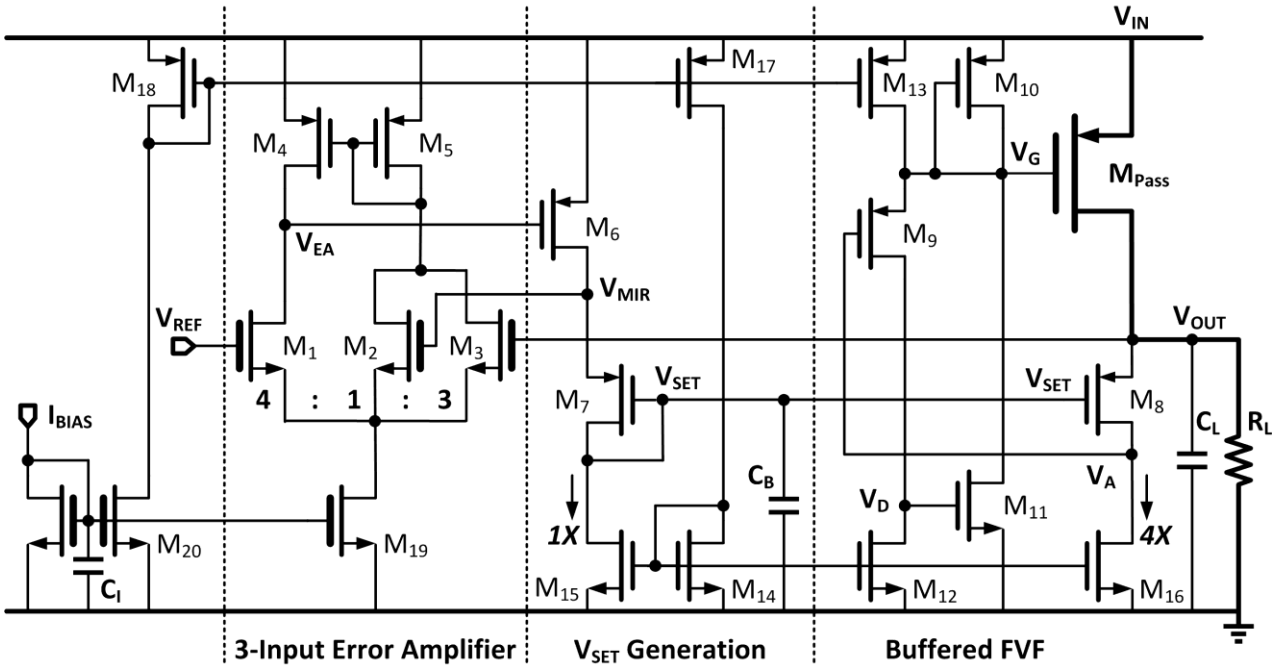



Fig. 6.4 Transistor level schematic of the proposed fully integrated tri-loop LDO.

$$V_{\mathrm{MIR}} = V_{\mathrm{OUT}} + \Delta \mathrm{V}\,, \tag{6.3}$$

where $\mathrm{A_{EA}}$ is the gain of the EA (including the $V_{\mathrm{SET}}$ generation stage), and $\Delta$V is the voltage difference between $V_{\mathrm{MIR}}$ and $V_{\mathrm{OUT}}$ due to PVT and load variations. By substituting (6.3) into (6.2), and assuming $\mathrm{A_{EA}} >> 1$, we have

$$V_{\mathrm{OUT}} = \frac{\mathrm{A_{EA}}}{1+\mathrm{A_{EA}}} V_{\mathrm{REF}} - \frac{\Delta \mathrm{V} \cdot \mathrm{A_{EA}}/4}{1+\mathrm{A_{EA}}} \approx V_{\mathrm{REF}} - \frac{\Delta \mathrm{V}}{4} \tag{6.4}$$

$$V_{\mathrm{MIR}} = \frac{\mathrm{A_{EA}}}{1+\mathrm{A_{EA}}} V_{\mathrm{REF}} + \frac{3\Delta \mathrm{V} \cdot \mathrm{A_{EA}}/4}{1+\mathrm{A_{EA}}} + \frac{\Delta \mathrm{V}}{1+\mathrm{A_{EA}}} \approx V_{\mathrm{REF}} + \frac{3\Delta \mathrm{V}}{4}\,. \tag{6.5}$$

Therefore, $V_{\mathrm{OUT}}$ is closer to $V_{\mathrm{REF}}$ than $V_{\mathrm{MIR}}$ by setting the size ratio of $\mathrm{M_2}$ and $\mathrm{M_3}$ to be 1 : 3.

Since the EA is not in the high-speed path, the input transistors of the EA and its tail current mirror are implemented with 2.5 V I/O devices for DC gain and ESD considerations. Different symbols are used to distinguish the I/O devices from the 1-V core devices in Fig. 6.4. All on-chip MOS capacitors are I/O devices to avoid gate leakage current if thin-oxide

(1.0 V) devices are used. The remaining transistors are thin-oxide devices for fast response. To suppress off-chip noise, a 2 pF $C_{\mathrm{I}}$ is added at the bias input node $I_{\mathrm{Bias}}$, and may not be needed if $I_{\mathrm{Bias}}$ is generated on-chip. To save static current, the ratio of $\mathrm{M}_7$ and $\mathrm{M}_8$, and that of their bias currents, is set to be 1 : 4, as $V_{\mathrm{SET}}$ is in the low-speed path that does not need much current, but $V_{\mathrm{A}}$ is in the high-speed path and needs a larger current.

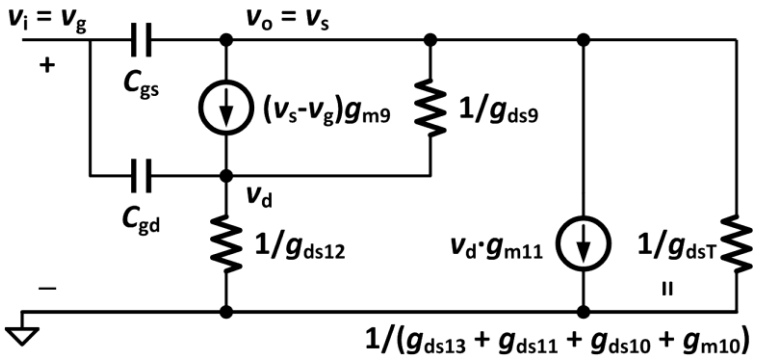



Fig. 6.5 Small-signal model of the buffer for input/output impedance and gain calculation.

The buffer used for impedance attenuation consists of $\mathrm{M}_9$ through $\mathrm{M}_{13}$, and three parameters are of concern: the input capacitance $C_{\mathrm{iB}}$, the output resistance $r_{\mathrm{oB}}$, and the DC gain $\mathrm{A}_{\mathrm{B}}$. The small-signal model of the buffer is shown in Fig. 6.5. The input capacitance of the circuit can be computed by noting that

$$C_{iB}\Delta \mathrm{V}_g = C_{gs}\Delta \mathrm{V}_{gs} + C_{gd}\Delta \mathrm{V}_{gd}\,, \tag{6.6}$$

and in the small-signal limit, (6.6) can be rewritten as

$$C_{\mathrm{iB}} = \left(1 - v_{\mathrm{s}}/v_g\right)\cdot C_{\mathrm{gs}} + \left(1 - v_{\mathrm{d}}/v_g\right)\cdot C_{\mathrm{gd}}\,, \tag{6.7}$$

where $C_{\mathrm{gs}}$ and $C_{\mathrm{gd}}$ are the gate-to-source and gate-to-drain capacitances of $\mathrm{M}_9$. The voltage gains are calculated as

$$\mathrm{A}_{\mathrm{B}} = \frac{v_{\mathrm{s}}}{v_{\mathrm{g}}} = 1 \Big/ \left(1 + \frac{1}{\mathrm{A}_1} + \frac{2}{\mathrm{A}_1\mathrm{A}_2}\right) \tag{6.8}$$

with

$$\mathrm{A}_1 = g_{\mathrm{m9}}/g_{\mathrm{ds9}} \tag{6.9}$$

$$A_2 = \left(g_{m11} + g_{ds12}\right) / g_{dsT} \tag{6.10}$$

and

$$\frac{v_d}{v_g} = \frac{v_d}{v_s}\frac{v_s}{v_g} = -\frac{1}{A_2}\frac{v_s}{v_g} = -\frac{A_1}{A_1A_2 + A_2 + 2} \tag{6.11}$$

$$g_{dsT} = g_{m10} + g_{ds10} + g_{ds11} + g_{ds13}\,. \tag{6.12}$$

Here, $A_1$ is the intrinsic gain of $M_9$, and $-A_2$ is the gain from the drain to the source of $M_9$. Assume $A_1$ and $A_2$ to be much larger than 1, then $A_B \approx 1$. Combining (6.7), (6.8) and (6.11), we have

$$C_{iB} = \frac{A_2 + 2}{A_1A_2 + A_2 + 2} C_{gs} + \left(1 + \frac{A_1}{A_1A_2 + A_2 + 2}\right) C_{gd}$$

$$\approx \frac{1}{A_1} C_{gs} + \left(1 + \frac{1}{A_2}\right) C_{gd} \approx C_{gd}\,. \tag{6.13}$$

Since $M_9$ operates in the saturation region, most of the channel charge is associated with the source, which means that $C_{gs}$ is much larger than $C_{gd}$, and hence, $C_{iB}$ is small. The output resistance of the buffer $r_{oB}$ is given by

$$r_{oB} = \frac{1}{A_3\left(g_{m9} + g_{ds9}\right) + g_{dsT}}, \tag{6.14}$$

where $A_3 = (g_{m11}+g_{ds12})/(g_{ds12}+g_{ds9})$. It needs to be increased to further attenuate $r_{oB}$. Note that $g_{dsT}$ includes the term $g_{m10}$ from $M_{10}$, and lowering $r_{oB}$ by increasing $g_{m10}$ also increases the pull-up capability of the buffer.

A fundamental design trade-off is identified between the DC gain and the frequency response: to satisfy the assumption that $A_1$, $A_2$ >> 1, the channel length $L$ of $M_9$ should be long; to reduce $C_{gs}$ and $C_{gd}$, $L$ of $M_9$ should be short. In this design, the minimum $L$ is used for $M_9$ for speed consideration, and $M_{11}$ operates in the sub-threshold region to give a larger $g_{m11}$ to increase $A_2$ and $A_3$. The gate capacitance of $M_{11}$, which would generate an additional pole $p_D$ at node $V_D$, is neglected in the analyses above. This non-dominant pole $p_D$ is located in the GHz range as verified in the following AC simulations and transient measurements.

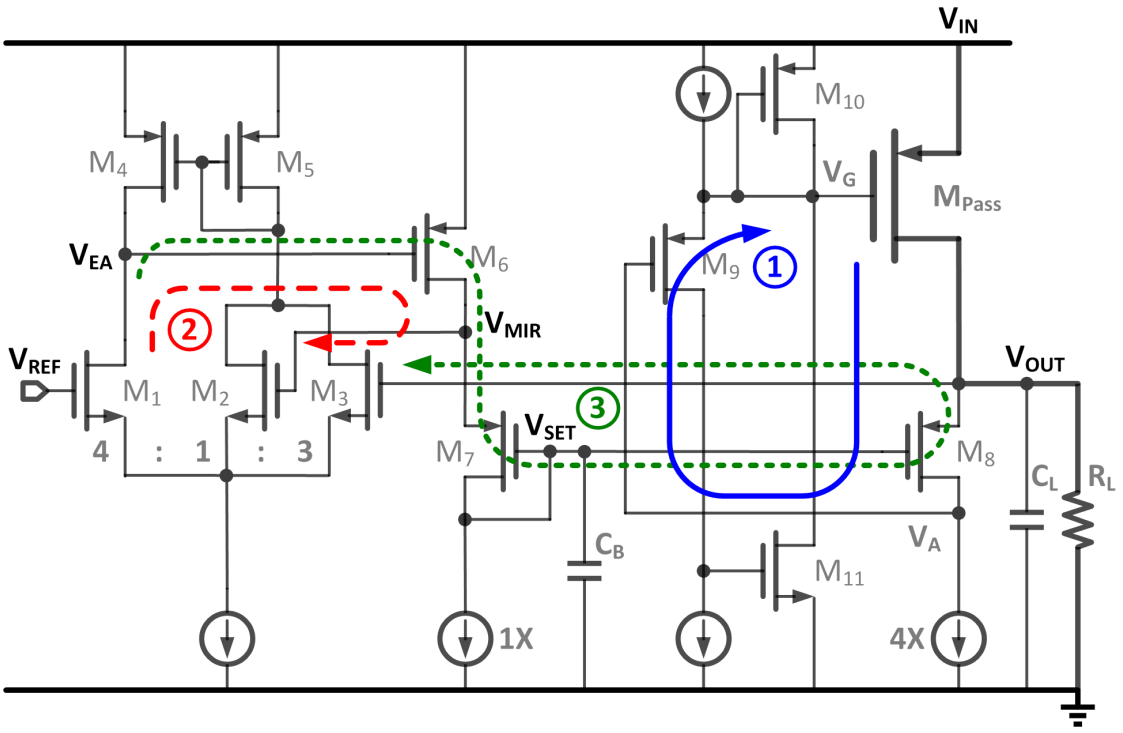



Fig. 6.6 The simplified diagram of the three loops in the proposed LDO regulator.

### 6.4.2 Stability Analyses

The signal paths of each loop are superimposed on the schematic shown in Fig. 6.6. Each loop has a different function: loop-1 is an ultra-fast low-gain loop with $p_{Out}$ being its dominant pole, and non-dominant poles $p_{Gate}$ and $p_A$ are pushed to the GHz range by the buffer impedance attenuation technique; loop-2 is composed of the EA and the diode-connected $M_7$ and is a slow loop that generates the voltages of $V_{MIR}$ and $V_{SET}$; loop-3 has $V_{OUT}$ fed back to the EA such that the DC accuracy is improved. In other words, loop-1 is used to deal with the fast load-transient current, while loop-3 is used to enhance the $V_{OUT}$ DC accuracy. To simulate the loop response of each loop, two simulation setups are configured and described as follows.

*Setup 1*: As shown in Fig. 6.7, the signal path of loop-1 is broken between $V_A$ and the buffer input. The AC small signal is injected to the buffer input and the output is observed at $V_A$. To isolate the influence from loop-2 and loop-3, the path from $M_7$ to $M_8$ is also broken. To maintain the DC bias, a DC voltage $V_{SET}$ is applied to the gate of $M_8$, and to account for the loading effect, a replica buffer stage is added to $V_A$ to mimic $C_{iB}$.

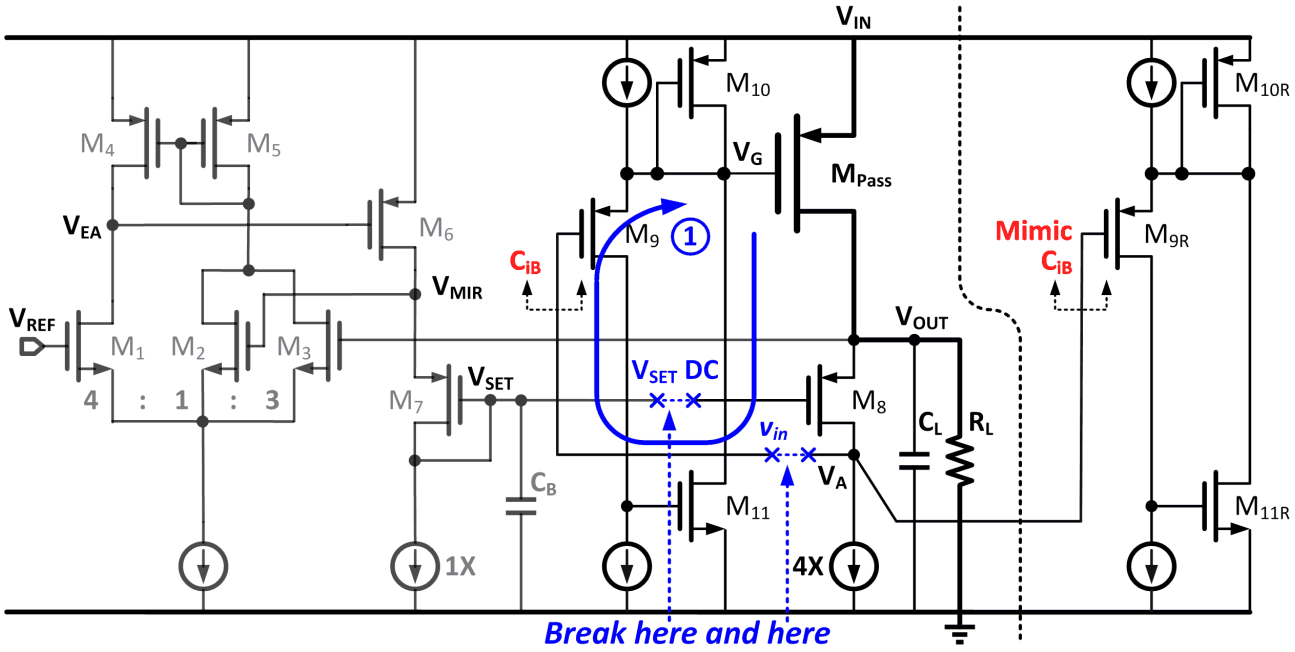



Fig. 6.7 Break the loop-1 with replica buffer to mimic its input capacitance.

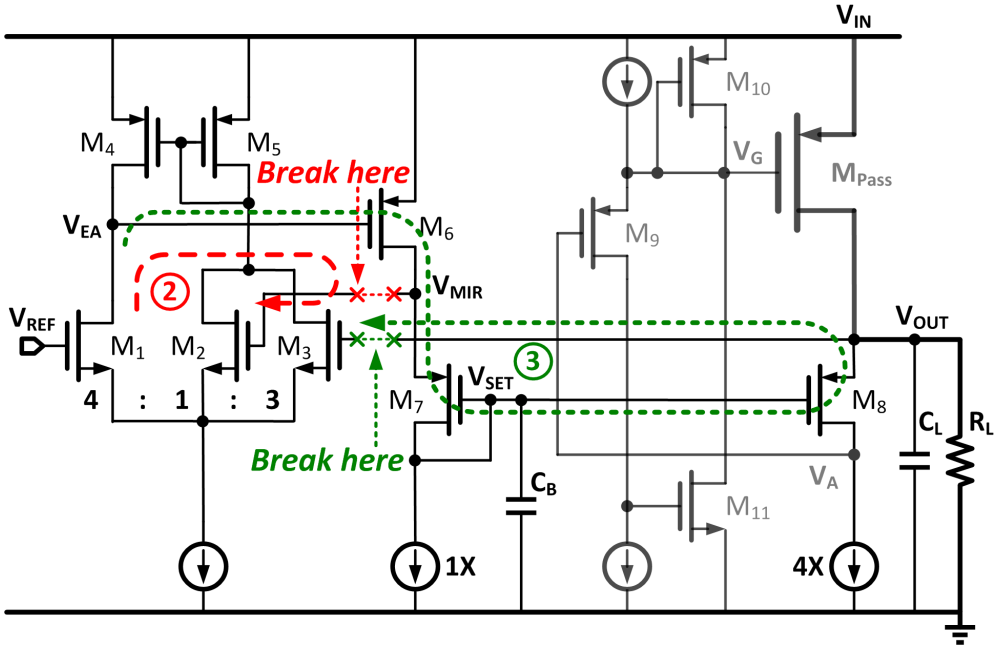



Fig. 6.8 Break the loop-2 and -3 simultaneously for stability analysis.

*Setup 2*: Loop-2 and loop-3 are broken from $V_{MIR}$ to $M_2$ and from $V_{OUT}$ to $M_3$, respectively, as shown in Fig. 6.8. The AC small signal is injected into the EA through $M_2$ only. Now, the AC

response of loop-2 can be obtained at $V_{MIR}$, and the response of loop-3 can be obtained at $V_{OUT}$, simultaneously. Loop-2 and loop-3 can be considered together because they both contain the error amplifier in their respective loop.

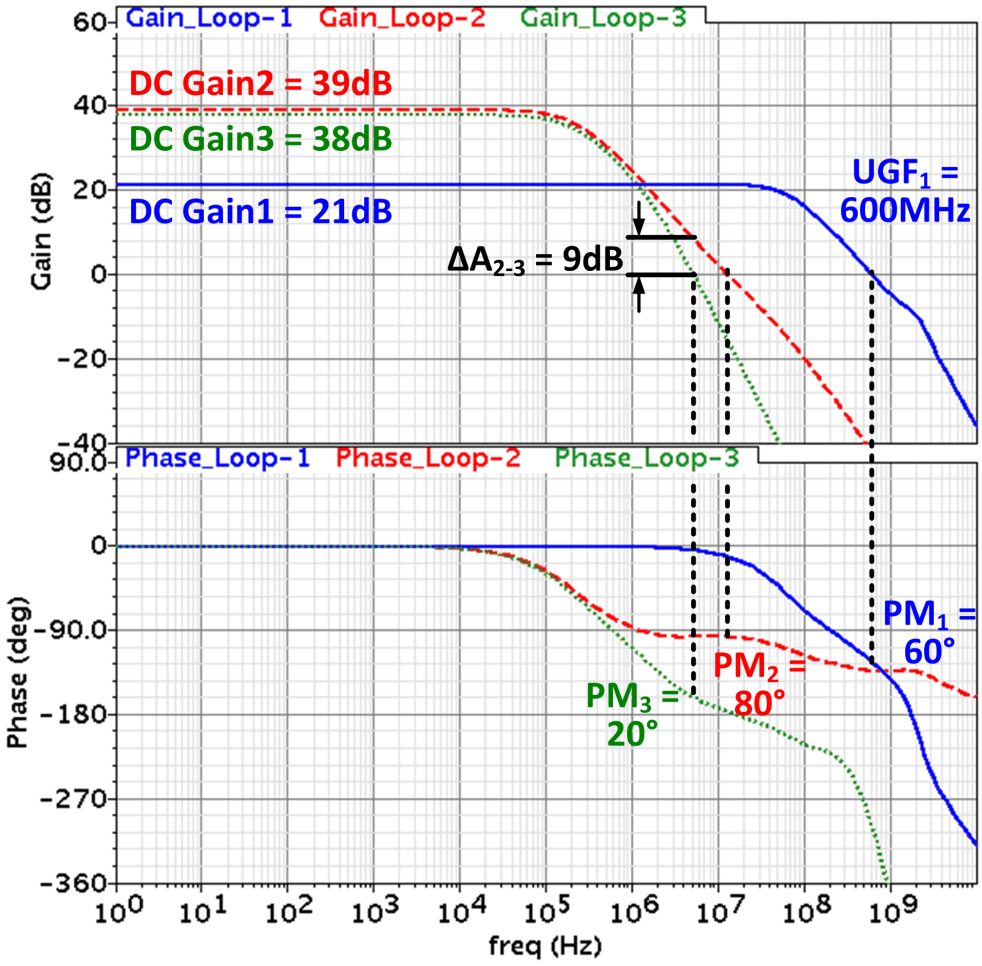



Fig. 6.9 Simulated frequency response of the three loops of the proposed LDO regulator with $V_{IN}$ = 1.2 V, $V_{OUT}$ = 1.0 V and $R_L$ = 100 Ω.

Simulation results of these two setups are combined in Fig. 6.9, which shows the Bode plots of the three loops at the worst case (at heavy load condition with $I_O$ = 10 mA). When $V_{OUT}$ is 1.0 V, loop-1 has a DC gain of 21 dB and its $UGF_1$ is 600 MHz, with a phase margin ($PM_1$) of 60 °. Loop-2 has one dominant pole located at $V_{SET}$ and a non-dominant pole located at $V_{EA}$, and $PM_2$ = 80 °. Loop-3 has two non-dominant poles located at $V_{EA}$ and $V_{OUT}$, respectively, and $PM_3$ is only 20 °. Nevertheless, the stability of the circuit is determined by the system loop

gain, not individual loop gains. A third loop breaking setup for stability analysis is shown in Fig. 6.10 and described as follows.

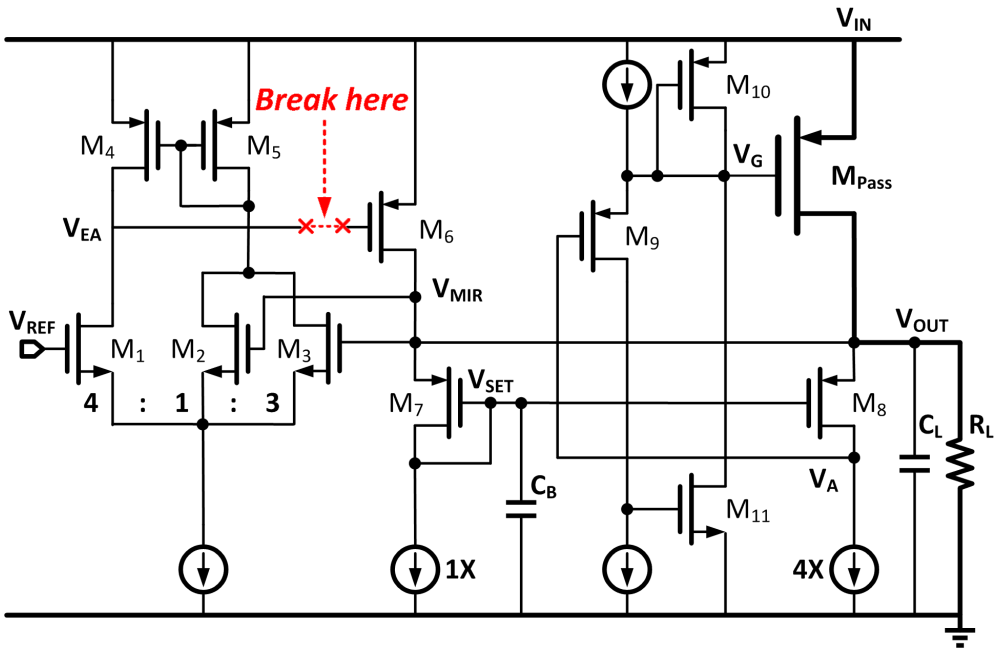



Fig. 6.10 Break the loop at the EA output.

*Setup 3*: Loop-2 and loop-3 contain the error amplifier, and by breaking the loops between $V_{EA}$ and the gate of $M_6$ we have

$$v_{EA} = \frac{-g_{m2}\left(r_{o1} \| r_{o4}\right)}{1+sC_{EA}\left(r_{o1} \| r_{o4}\right)}\left(v_{mir} + 3v_{out}\right). \tag{6.15}$$

The loop-gain transfer function of loop-2 plus loop-3 is given as

$$\begin{aligned} T(s) = \frac{v_{EA}}{v_{in}} &= \frac{-g_{m2}\left(r_{o1} \| r_{o4}\right) g_{m6}\left(r_{o6} \| r_{o15}\right)}{\left(1+sC_B\left(r_{o6} \| r_{o15}\right)\right)\left(1+sC_{EA}\left(r_{o1} \| r_{o4}\right)\right)} \\ &+ \frac{-3g_{m2}\left(r_{o1} \| r_{o4}\right) g_{m6}\left(r_{o6} \| r_{o15}\right) g_{m8}\left(r_{op} \| R_L\right)}{\left(1+sC_B\left(r_{o6} \| r_{o15}\right)\right)\left(1+sC_{EA}\left(r_{o1} \| r_{o4}\right)\right)\left(1+sC_L\left(r_{op} \| R_L\right)\right)} \\ &= \frac{-g_{m2}\left(r_{o1} \| r_{o4}\right) g_{m6}\left(r_{o6} \| r_{o15}\right)\left(1+sC_L\left(r_{op} \| R_L\right)+3g_{m8}\left(r_{op} \| R_L\right)\right)}{\left(1+sC_B\left(r_{o6} \| r_{o15}\right)\right)\left(1+sC_{EA}\left(r_{o1} \| r_{o4}\right)\right)\left(1+sC_L\left(r_{op} \| R_L\right)\right)}, \end{aligned} \tag{6.16}$$

where $v_{in}$ is the AC signal injected at the gate of $M_6$, $C_{EA}$ is the parasitic capacitance at the $V_{EA}$ node, and $r_{op}$ is the output resistance of $M_{Pass}$. There are three poles and one zero in the transfer function, while the dominant pole is generated by $C_B$. The zero is generated by Loop-2, which is a shorter signal path compare to Loop-3. It is the pole-zero tracking pair that makes the entire LDO stable in all loading conditions. The simulated bode plot of *Setup 3* is given in Fig. 6.11. The phase margins are 68 ° at 10mA loading and 40 ° at no load condition, respectively.

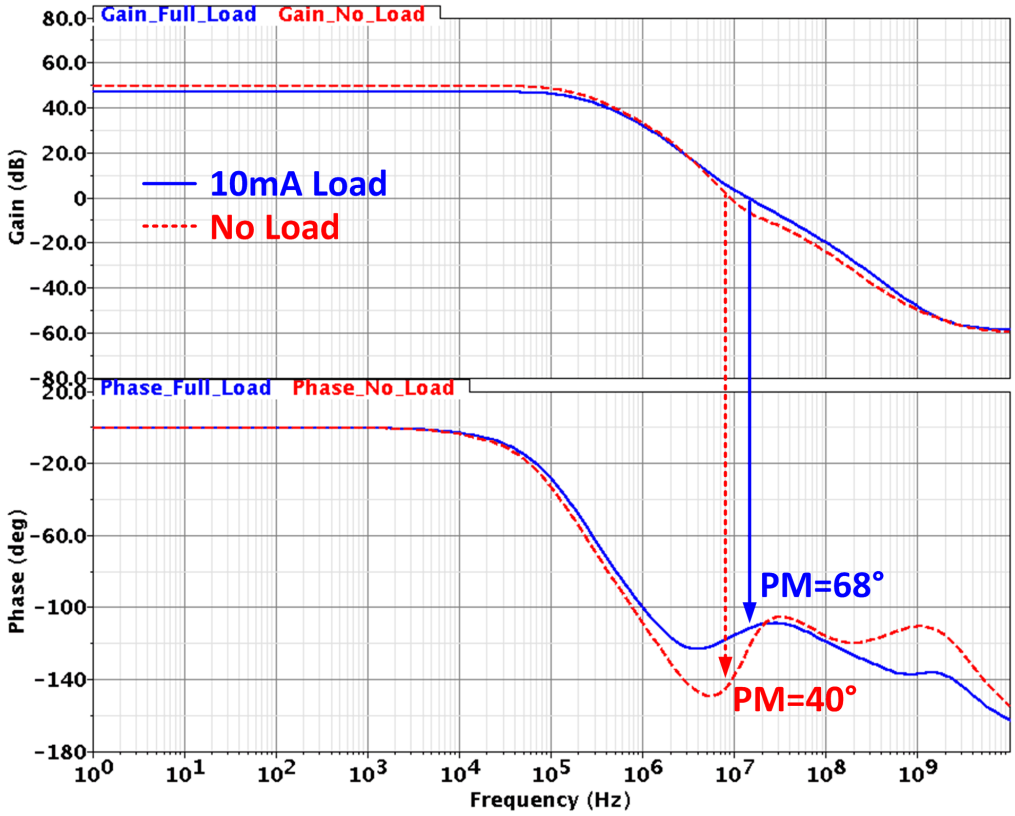



Fig. 6.11 Simulated bode plot of the LDO with $V_{IN}$ = 1.2 V, $V_{OUT}$ = 1.0 V and $R_L$ = 100 Ω.

In this research, the ($W/L$) ratio of $M_2$ and $M_3$ is aggressively set to be 1 : 3. This setting is to trade stability margin for better $V_{OUT}$ DC accuracy. To gain more design margin for stability, the weighting of $M_2$ and $M_3$ could be set to 2 : 2 by scarifying DC accuracy. Alternatively, in another extreme case, with $M_2$ (loop-2) being removed and $M_3$ having the same size as $M_1$, the DC accuracy is maximized. However, the dominant pole of loop-3 at $V_{SET}$ has to be much lower than before, and the settling time of $V_{OUT}$ will be much longer due to the slow loop-3.

### 6.4.3 Load Regulation

Curves of load regulation are shown in Fig. 6.12, with $(W/L)_2$ : $(W/L)_3$ being set to 1 : 3, 2 : 2 and 1 : 0 (no loop-3) respectively. In the case of no loop-3, $V_{OUT}$ changed by 34 mV when the load current is changed from 10 µA to 10 mA. For our proposed case of 1 : 3, $V_{OUT}$ changed by only 11 mV with the same change in load current. DC accuracy is improved by about 3 times by adding loop-3 without degradation in stability and speed performance. If the ratio between $M_2$ and $M_3$ is 2 : 2, $V_{OUT}$ would change by 20 mV.

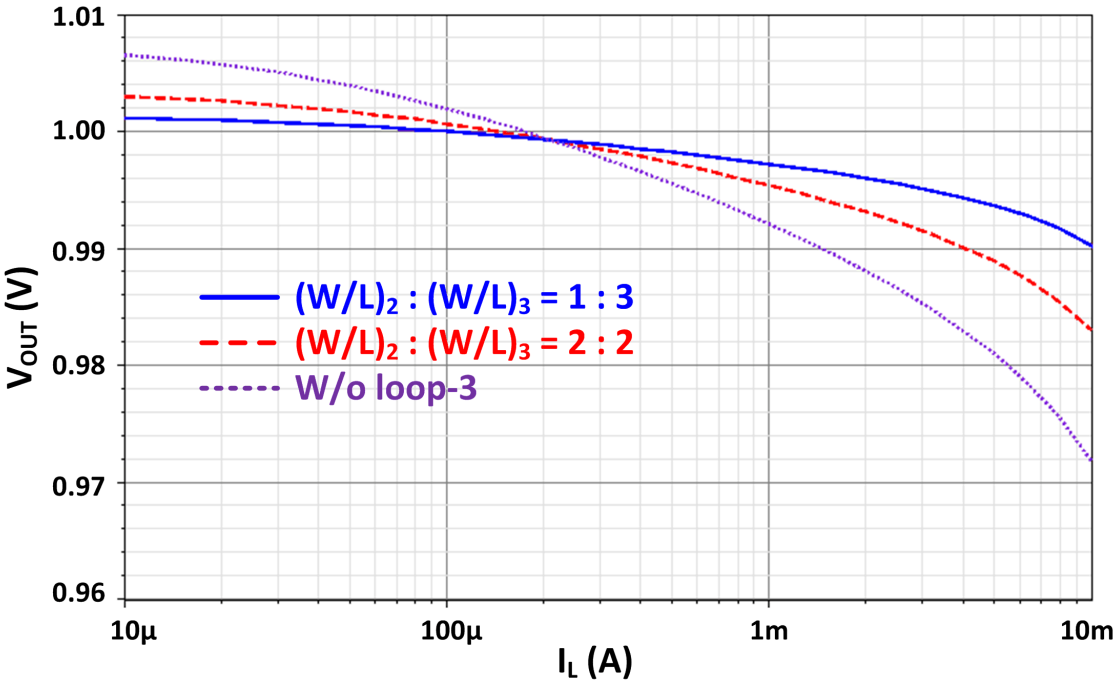



Fig. 6.12 Simulated $V_{OUT}$ load regulation with $(W/L)_2$ : $(W/L)_3$ being set to 1 : 3 and 2 : 2, respectively; plus the case without loop-3.

### 6.4.4 Power Supply Rejection

For many published works on fully-integrated LDOs with fast transient responses, performance on power supply rejection is usually not discussed. However, PSR is the most important specification for an LDO designed for noise-sensitive load. Supply ripples are mainly due to the output voltage ripples from the pre-stage DC-DC converter, and on-chip

noise generated by the digital/driver circuits. Ripples generated by DC-DC converters could be higher than 100 MHz [58], while noise generated by digital circuits is in the GHz range.

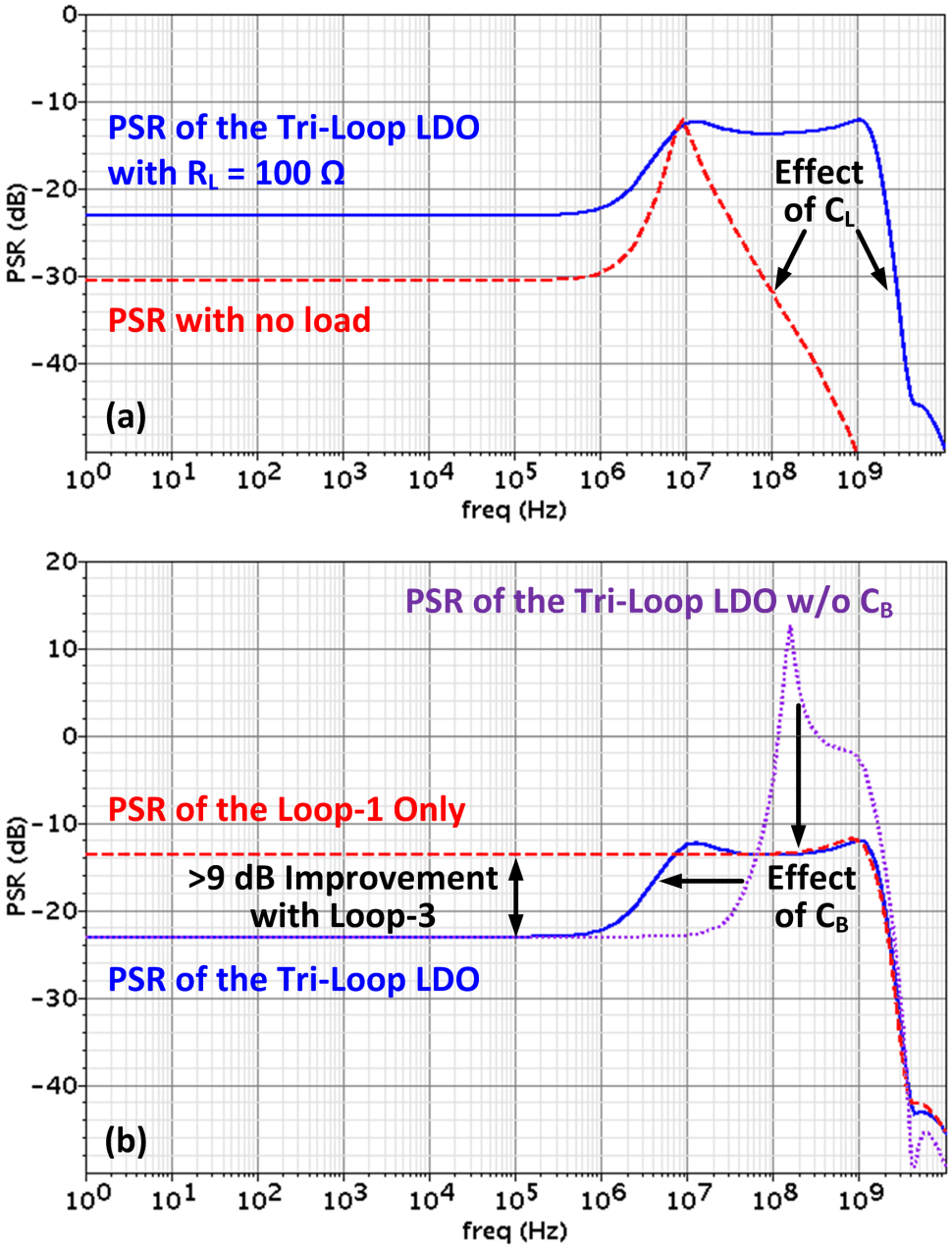



Fig. 6.13 (a) Simulated PSR of the proposed LDO with or without $R_L$ = 100 Ω, respectively; and (b) PSR of loop-1 only and the tri-loop regulator with or without $C_B$, with $V_{IN}$ = 1.2 V, $V_{OUT}$ = 1.0 V and $R_L$ = 100 Ω.

By setting $p_{Out}$ as the dominant pole, most of the silicon area (capacitance) can be effectively used to stabilize $V_{OUT}$ and reject noise from $V_{IN}$. The simulated PSR curves of the proposed

LDO with and without a 100 Ω $R_L$ are shown in Fig. 6.13(a); and the PSR of the tri-loop regulator with and without $C_B$, and the PSR of the regulator with only loop-1 and $C_B$, are plotted in Fig. 13(b), respectively. At medium and high frequencies, the light-load PSR is better than the full-load PSR, as $C_L$ can more effectively bypass the ripple to ground when it is in parallel with a larger $R_L$. The ultra-fast loop-1 could response to the input ripple in the VHF (very high frequency, 30 MHz – 300 MHz) range with the assistance of $C_L$, but with only loop-1, the LDO will have poor PSR at low frequencies. For the proposed tri-loop LDO, PSR with 9 dB improvement is achieved at frequencies lower than 1 MHz. In FVF-based structures, $V_{OUT}$ is mainly determined by $V_{SET}$. Therefore, adding a bypass capacitor $C_B$ (about 7 pF in this design) at the $V_{SET}$ node could improve the PSR by filtering out the ripple that comes from $V_{MIR}$ to $V_{OUT}$. Adding $C_B$ is effective in the medium frequency range (around 100 MHz to 1 GHz). The total on-chip capacitance is less than 140 pF.

### 6.5 Measurement Results

The measurement setup of the LDO with on-chip load for load transient measurement is shown in Fig. 6.14. The on-chip $R_L$ is connected in series with the switch $S_1$ implemented by a 1.0 V device driven by an on-chip inverter buffer, and the rising and falling edges $T_{Edge}$ of the load current are less than 200 ps (in simulations they are only 120 ps). The static currents of the chip with $S_1$ ON and with $S_1$ OFF are measured as $I_{MAX}$ and $I_Q$, respectively. The dropout voltage is about 150 mV at $I_{MAX}$ (the worst case). With chip-on-board setup, all the transient waveforms are collected by a pair of 7 GHz differential probes with input impedance of 50 kΩ || 0.32 pF connected to a 4 GHz oscilloscope. Single bonding wire is bonded to each input/output terminal of the prototype. The parasitic *RLC* low-pass filter consists of the 2 nH bonding wire inductance and the input impedance of the probe, and the cutoff frequency is over 6 GHz. With the above setup, ultra-fast transient currents and voltages are generated and measured.

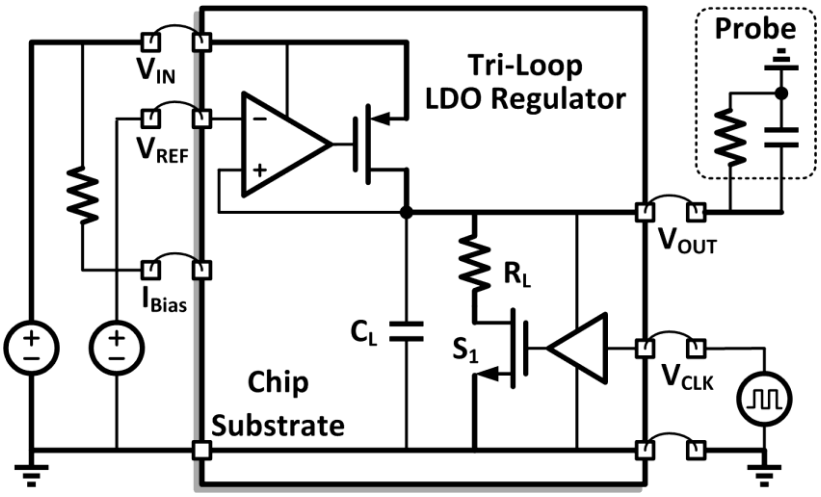



Fig. 6.14 Testing setup of the regulator with on-chip load for measurement.

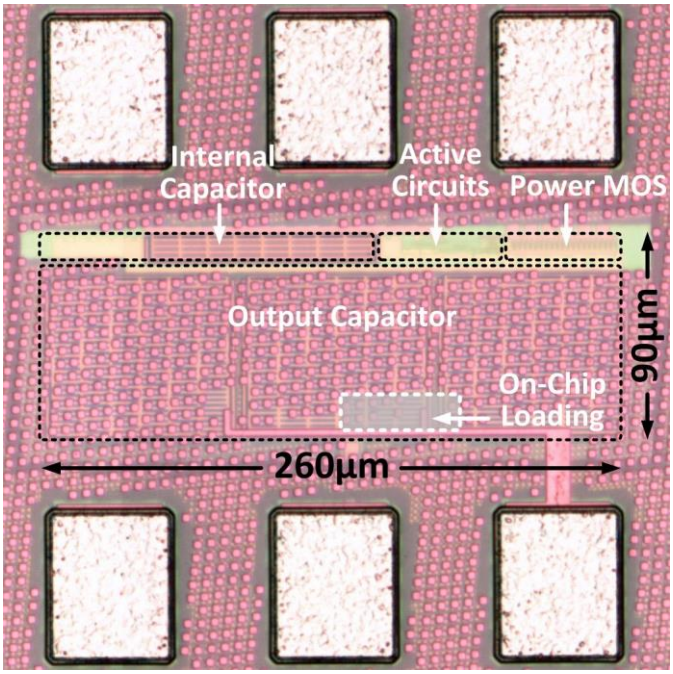



Fig. 6.15 Micrograph of the proposed LDO with on-chip loading for characterization

The prototype chip of the proposed LDO was fabricated using 65 nm CMOS GP process. The micrograph of the proposed LDO with on-chip loading for characterization is shown in Fig. 6.15. The chip area is $260 \times 90$ µm$^2$, including 140 pF of on-chip capacitors and the circuit for generating load current transients. Stacked MOS and MIM capacitors are used to reduce the silicon area.

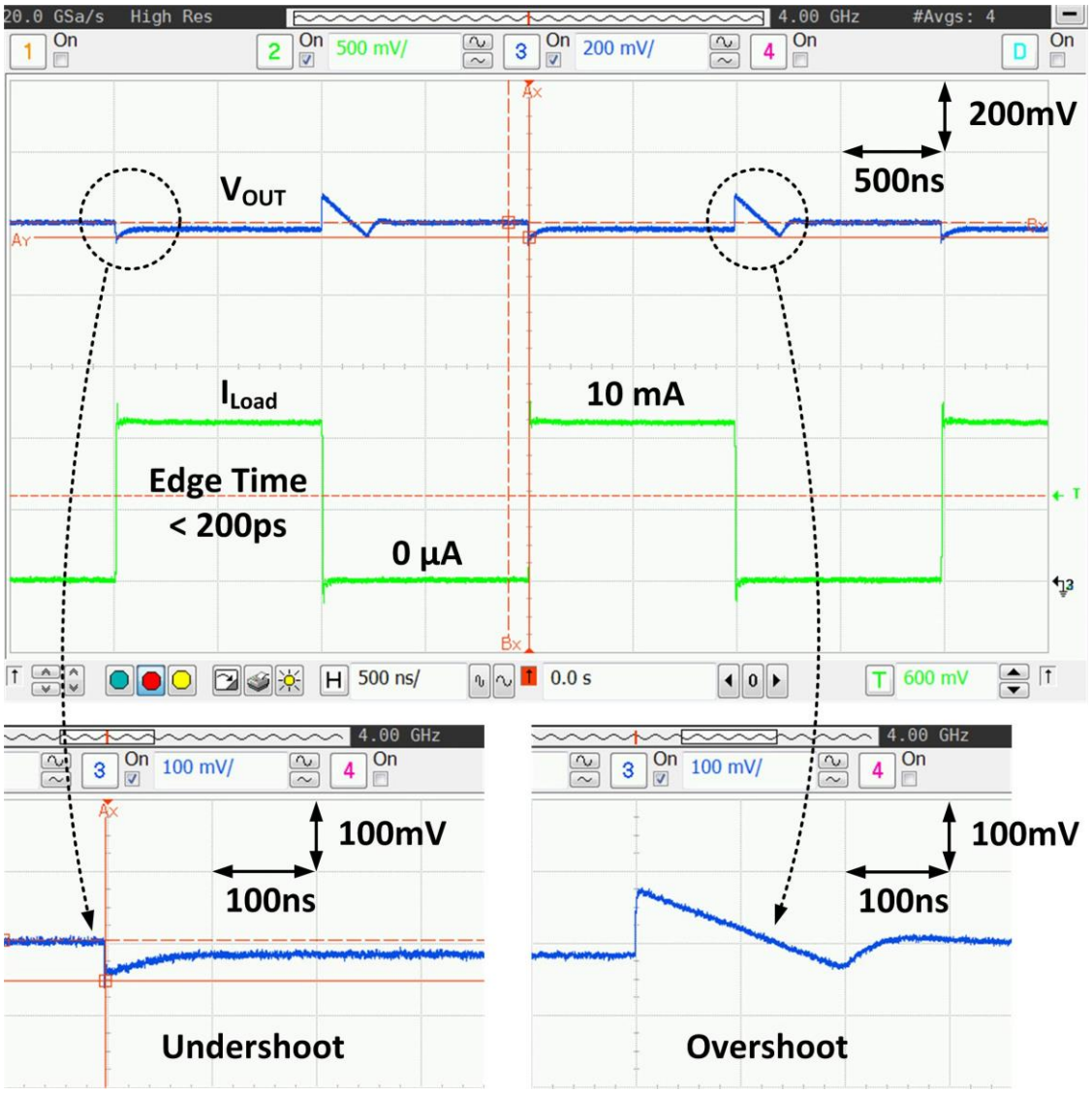



Fig. 6.16 Measured transient response with $V_{IN}$ = 1.2 V, $V_{OUT}$ = 1.0 V, and on-chip load current change from 0 µA to 10 mA within edge times of 200 ps.

Fig. 6.16 shows the measured transient response of the output voltage $V_{OUT}$ with on-chip load current change from 0 µA to 10 mA within 200 ps, with zoom-in details of the undershoot and overshoot voltages. With a quiescent current of only 50 µA, the measured undershoot voltage was 43 mV, and $V_{OUT}$ recovered to its steady state value in 100 ns with the help of loop-3 regulation. When the load current stepped from 10 mA to 0 µA, the measured overshoot voltage was 82 mV, and $V_{OUT}$ was gradually discharged by the bias current of $M_8$, and then regulated by loop-3 to its steady state value. The well-behaved transient waveforms of $V_{OUT}$ confirmed the stability of the proposed tri-loop LDO. The FOM calculated according to (1) of [46] is 5.74 ps, and the response time is only 1.15 ns. FOM is expected to be improved further

with process scaling. Note that FOM improvement is not necessarily true for internal pole dominant cases, because low loop bandwidth is required by limiting $I_{O,MIN}$ for stability considerations, as mentioned in Section 6.2.

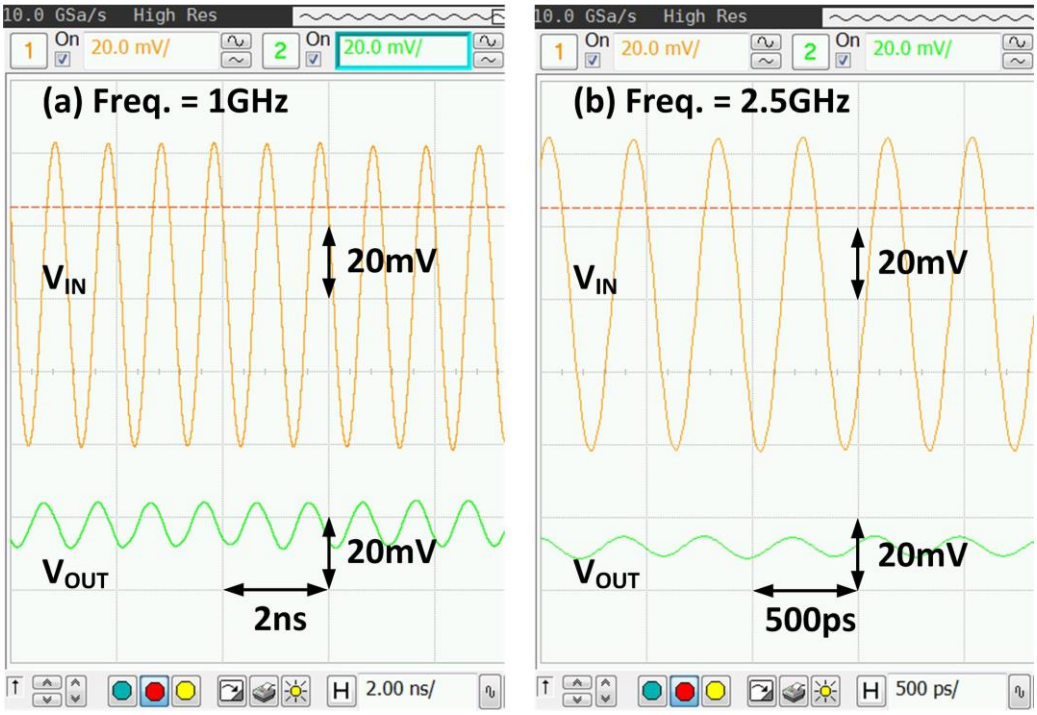



Fig. 6.17 Measured transient waveforms for PSR calculation, with $V_{IN}$ = 1.2 V and 80 mV $V_{PP}$ input ripple at (a) 1 GHz and (b) 2.5 GHz, respectively.

The measured transient waveforms for evaluating PSR are shown in Fig. 6.17, and the peak-to-peak ripple of the ac component of the supply voltage at 1 GHz and 2.5 GHz is 80 m*V*. The PSR data at frequencies ≥ 2.5 GHz is measured by a spectrum analyzer, and they are consistent with the data measured by transient waveforms at 2.5 GHz. The power supply rejection is better than -12 dB up to 20 GHz, and is suitable for ultra-high data rate wideband communication systems with digital buffers generating high frequency glitches on-chip.

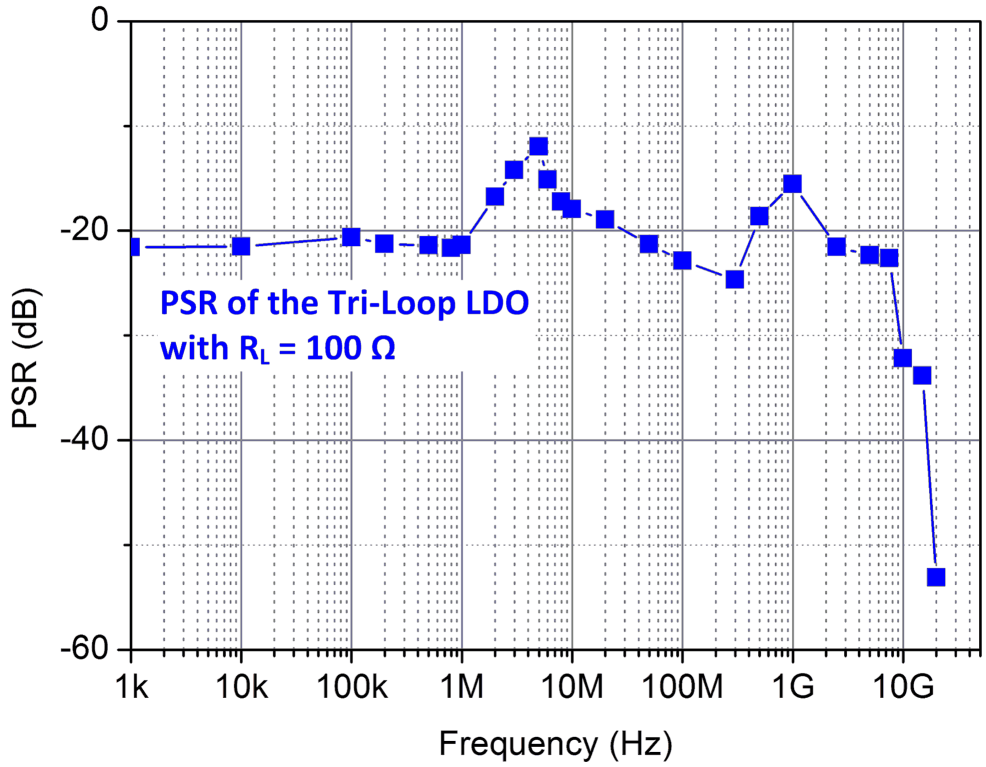



Fig. 6.18 Measured PSR up to 20 GHz with $R_L$ = 100 Ω.

Fig. 6.18 shows the summary of the measured PSR of the proposed LDO up to 20 GHz. For low frequencies (< 1 MHz), PSR is better than -21 dB; and the worst case occurs at 5 MHz with -12 dB rejection. PSR at 1 GHz is -15 dB. For frequencies higher than 2.5 GHz, PSR would be dominated by the ESR of the filtering capacitors ($C_L$ and $C_B$) [55]. Since the ESR zero is not needed in our proposed architecture, ESR of the on-chip capacitors is minimized in the layout design for good PSR.

Performance comparison with state-of-the-art LDOs is summarized in Table 6.4. Compared to previous ultra-fast transient response designs [46] and [50], response time on the order of nanosecond is achieved by the proposed architecture with much smaller $I_Q$ and $C_L$, and hence resulting in the best FOM. Furthermore, full spectrum PSR characterization is presented, while other fully-integrated LDO regulators only present PSR at specific frequencies.

Table 6.4 COMPARISON OF STATE-OF-THE-ART LDOS

| **Publication** | **[8] ISSCC 2008** | **[9] JSSC 2010** | **[12] JSSC 2005** | **[15] JSSC 2010** | **[16] JSSC 2012** | **This Work** |
|---|---|---|---|---|---|---|
| $C_L$ | Off-Chip | | **On-chip** | | | |
| **Technology** | 0.35 µm | 90nm | 90nm | 90nm | 45nm SOI | **65nm** |
| $V_{OUT}$ | 0.9V | 0.9V | 0.9V | 0.5 to 1V | 0.9 to 1.1V | **1V** |
| $V_{DO}$ | 150mV | 100mV | 300mV | 200mV | 85mV | **150mV** |
| $I_Q$ | 4 to 164 µA | 9.3 µA | 6mA | 8 µA | 12mA | **50 µA** |
| $I_{MAX}$ | 50mA | 50mA | 100mA | 100mA | 42mA | **10mA** |
| $C_{Total}$ | 1 µF | 1 µF | 600pF | 50pF | 1.46nF | **140pF** |
| **PSR** | -50dB @1MHz | -35dB @10MHz | N/A | 0dB @1MHz | N/A | **-15.5dB @1GHz** |
| $\Delta V_{OUT}$ $@T_{Edge}$ | 6.6mV @10ns | 10mV @10ns | 90mV @100ps | 114mV @100ns | N/A | **82mV @200ps** |
| **Load Reg.** | 3.05mV | 4.1mV | 90mV | 10mV | 3.5mV | **11mV** |
| $T_R$ | 132ns | 200ns | 0.54ns | N/A | 0.288ns* | **1.15ns** |
| **FOM** | 10.6ps | 37.2ps | 32ps | N/A | 62.4ps* | **5.74ps** |

*Simulated results.

## 6.6 Conclusions

In this research, a fully-integrated low-dropout regulator with ultra-fast transient response and full spectrum PSR characterization is presented. A tri-loop architecture based on the buffered flipped voltage follower is proposed and verified in 65 nm CMOS process. By comparing the design methodologies of previous non-fully-integrated and fully-integrated LDO designs, a gap in transient and PSR performances is identified, investigated and filled in this research.

The FVF structure with output-pole dominant is employed for its fast transient response and good medium- and high-frequency PSR. With the combined effects of the high-bandwidth loop-1, $C_L$ and $C_B$, good full spectrum PSR is achieved. With the additional loop-3, $V_{OUT}$ DC accuracy is improved by 3 times compared to the conventional FVF-based LDO. As FOM scales with process, the proposed architecture would perform even better using more advanced processes.

# Chapter 7 VOLTAGE REFERENCE AND REGULATORS FOR IMDS

In this chapter, a voltage reference and two LDO regulators designed for a retina micro-current electrical neuromuscular stimulation (MENS) implant device are introduced. The MENS device is supplied wirelessly with a power link frequency of 40 MHz. The transmission frequency is chosen for smaller passive components value in the IMD. A full wave rectifier at the power receiver front-end would charge up the energy storage capacitor twice per cycle (that is, every 12.5ns), and would result in supply voltage ripples at the frequency of 80 MHz. Thus, in this chapter, functional blocks of a power management unit with power-supply-rejection (PSR) optimized up to 80 MHz will be discussed.

## 7.1 Symmetrically Matched Bandgap Reference

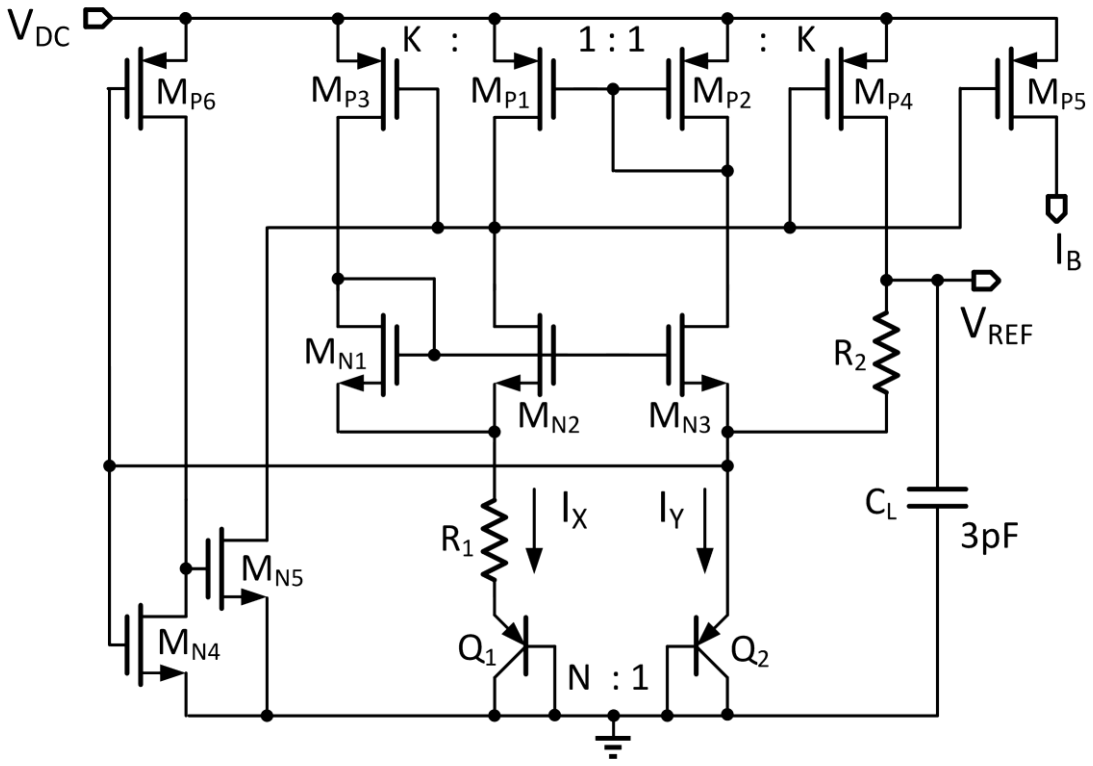



Fig. 7.1 The two-branch self-biased symmetrically matched bandgap reference used in this design.

To save static current, a two-branch self-biased symmetrically matched bandgap reference, as shown in Fig. 7.1, is used in this design [59]. In this topology, only two branches are needed to generate a bandgap voltage $V_{REF}$ (around 1.2 V). The currents $I_X$ and $I_Y$ are well-matched with symmetrically matched transistors $M_{P1}$ through $M_{P4}$, and $M_{N1}$ through $M_{N3}$, which means not only that they have the same $V_{GS}$ but also the same $V_{DS}$. Hence, channel length modulation of the mismatch current is eliminated. The start-up circuit consists of $M_{N4}$, $M_{N5}$ and $M_{P6}$. The reference voltage is given by

$$V_{ref} = V_{EB2} + \frac{R_2}{R_1}\frac{K}{K+1}\ln(N)\times V_T \qquad (7.1)$$

where $N$ and $K$ are the size ratios of $Q_1 : Q_2$ and $M_{P3} : M_{P1}$ respectively. In this design, $K = 3$, and $N = 8$ for matching considerations.

The total current of the reference is less than 2 μA, excluding the bias currents provided to other circuit blocks. A 3 pF NMOS load capacitor $C_L$ is connected to $V_{REF}$ to improve its PSR at wireless power transfer frequencies (around 80 MHz).

### 7.2 Voltage Regulators

The wirelessly transferred power is not steady. The generated DC supply voltage $V_{DC}$ not only contains ripples at 80 MHz, but also fluctuates with the movement between the coupling coils. Thus, a linear voltage regulator is needed to regulate the rectified voltage to a predefined fixed DC supply voltage. The regulator should also suppress the high frequency noise, and provide a clean supply to power up the electrical stimulation (ES) generator in the MENS implant. The implant is designed to have power link feedback such that the transmitted power will be adjusted to keep $V_{DC}$ in the range of 3.3 V to 4.0 V.

Two fully-integrated regulators are implemented in this IMD, one regulator has an output voltage of 3 V for the ES generator, and the second regulator has an output voltage of 1.2 V for the digital blocks. Schematics of the regulators are shown in Fig. 7.2.

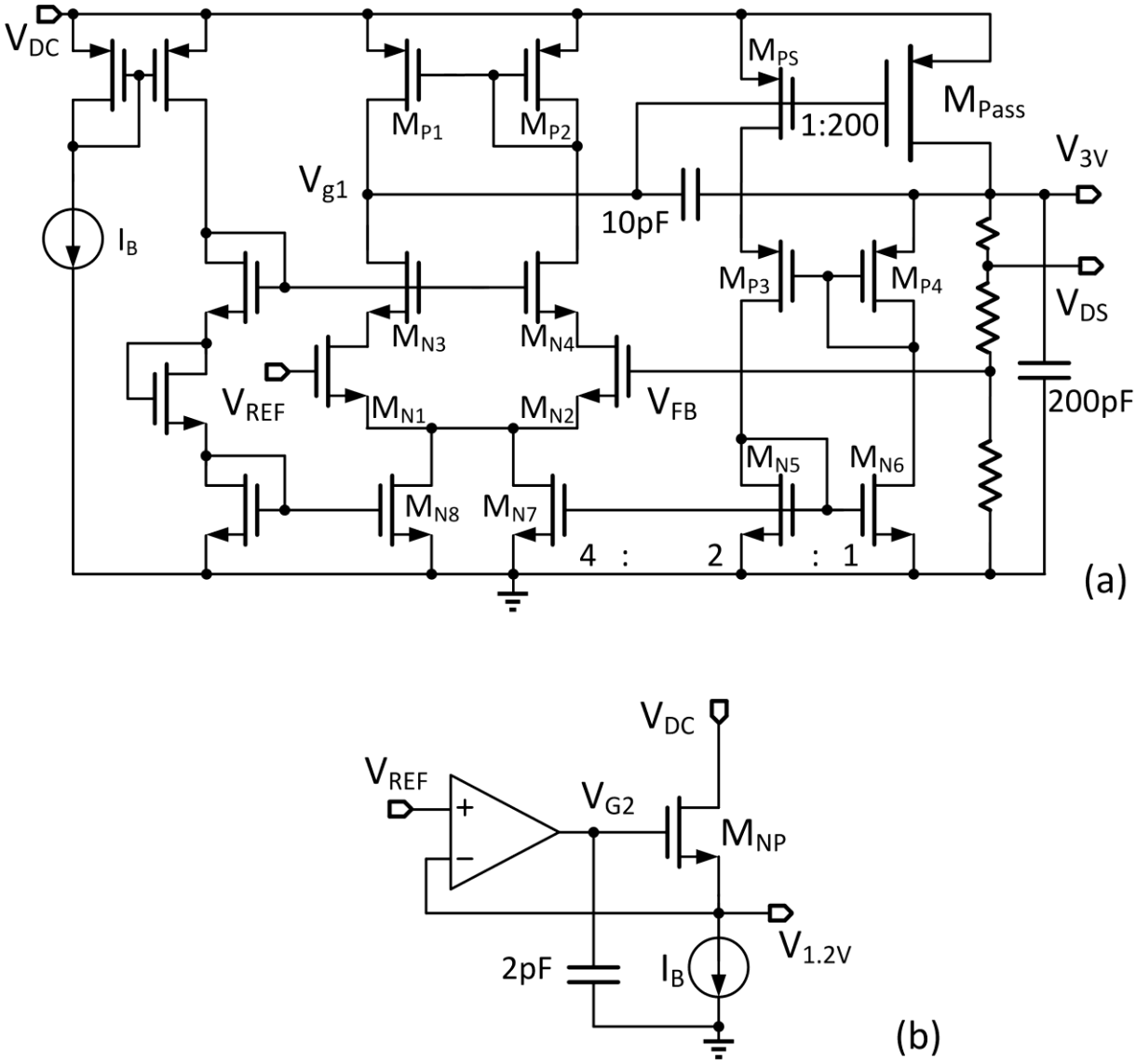



Fig. 7.2 (a) The LDO that generates 3 V for ES generator; and (b) the linear regulator that generates 1.2 V for digital blocks.

For the 3 V regulator, the loop is stabilized by Miller compensation with a 10 pF MIM capacitor, which means that this LDO falls into the internal pole dominant category discussed in Section 6.2. Thus, the PSR of the LDO will degrade to 0 dB at a certain frequency. Since the ripple frequency is known to be at 80 MHz, the LDOs have been designed to avoid the worst case PSR that occurs at around 80 MHz. A sensing MOSFET $M_{PS}$ is used to sense the output current. In this way, the bias current of the error amplifier is adaptive to the output current with the additional bias current provided by $M_{N7}$ [60]. Quiescent current of the 3 V

regulator is < 3 μA at light load, and is 21 μA when the load current is 1 mA. A 200 pF NMOS capacitor is connected to the output for PSR improvement.

For the 1.2 V regulator, as the input is high (> 3.3 V) and the output is low (1.2 V), it is implemented using a conventional linear regulator with an NMOS power transistor $M_{NP}$, as shown in Fig. 7.2(b). The power stage is a source follower that has low output impedance and intrinsically fast response: when the voltage of $V_{1.2V}$ drops due to load transient, $V_{GS}$ of $M_{NP}$ will automatically be increased to provide more current to the load. Thus, this regulator only consumes a quiescent current of 2 μA. A 2 pF de-coupling capacitor referenced to ground is connected to $V_{G2}$ to improve its PSR performance.

### 7.3 Simulation and Measurement Results

The simulated PSR curves of the voltage reference and the regulators are shown in Fig. 7.3. By design, $V_{REF}$ of the regulators was generated by the bandgap voltage reference that shared the same supply voltage $V_{DC}$. A 6 kΩ and 120 kΩ load resistors were connected to $V_{3V}$ and $V_{1.2V}$, respectively, corresponding to load currents of 500 μA and 10 μA, respectively. For the three circuits with nodes of $V_{REF}$, $V_{3V}$ and $V_{1.2V}$, the power supply rejections at frequencies below 1 kHz were 48 dB, 40 dB, respectively; and those at 80 MHz were 56 dB, 30 dB and 38 dB, respectively.

The MENS implant was fabricated using a 0.13 μm CMOS process. The overall chip size is 2.25 $mm^2$ including pads. The die photo is shown in Fig. 7.4. The silicon area of the voltage reference, the 3-V LDO and the 1.2-V LDO are 0.018 $mm^2$, 0.063 $mm^2$ and 0.0012 $mm^2$, respectively. The measured voltage waveforms of $V_{DC}$, $V_{3V}$ and $V_{1.2V}$ are shown in Fig. 7.5. For the implant device, there is an ENABLE signal for stimulation that is controlled by and transmitted from the primary side of the system (outside the implant). To reduce the device size, only one pair of coils was used for both the data link and the power link. Thus, the rectifier output $V_{DC}$ would experience fluctuation during data transmission, as can be observed in Fig. 7.5. Nevertheless, the voltage regulator could significantly reduce the supply ripple on $V_{DC}$, and provide stable supplies $V_{3V}$ and $V_{1.2V}$ for the functional circuits.

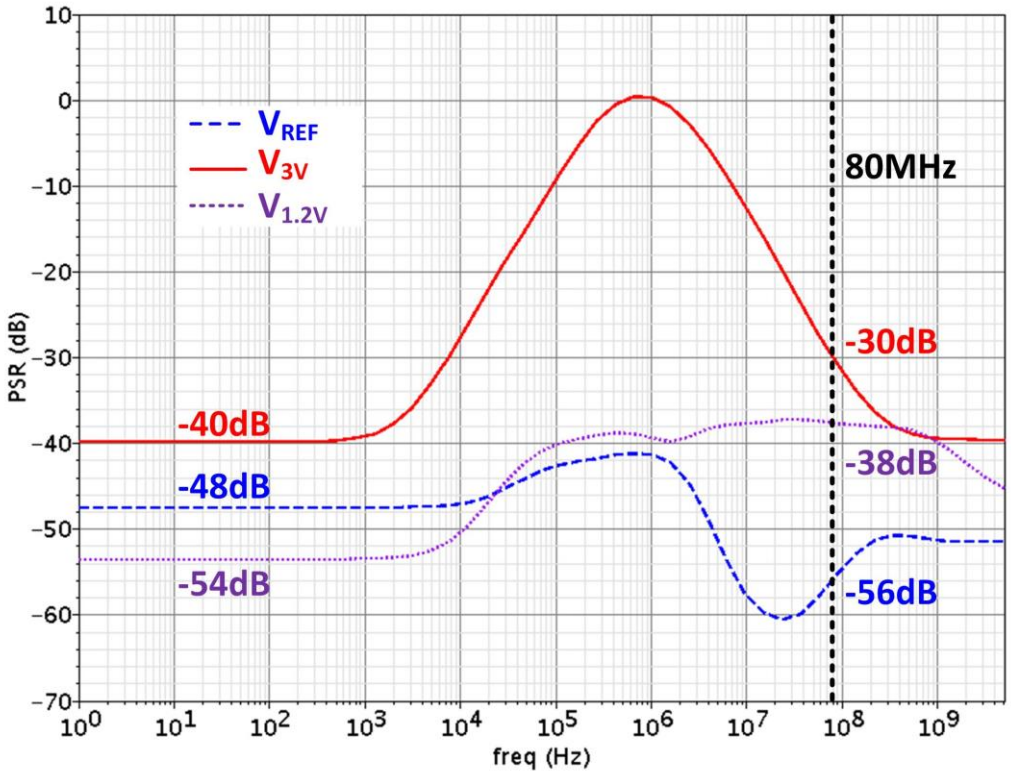



Fig. 7.3 Simulated PSR of the bandgap reference and the voltage regulators at $V_{DC}$ = 3.2 V.

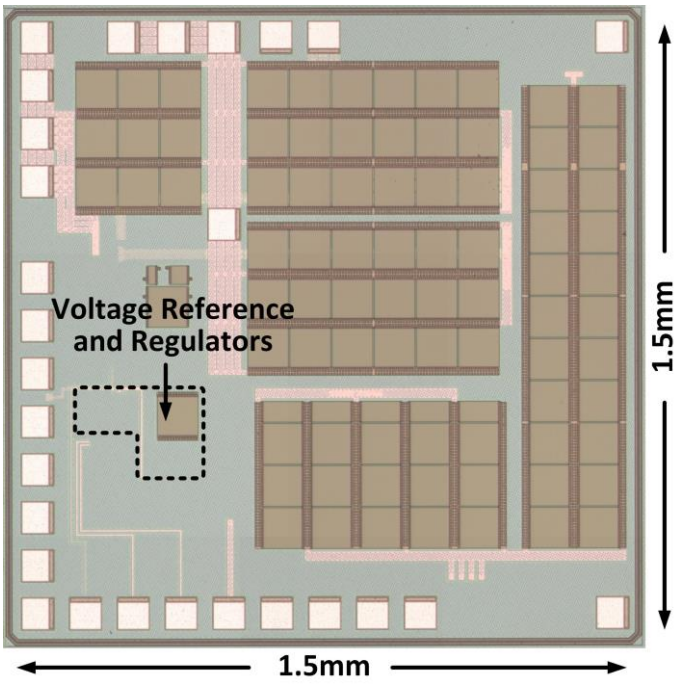



Fig. 7.4 Chip Micrograph of the MENS implant.

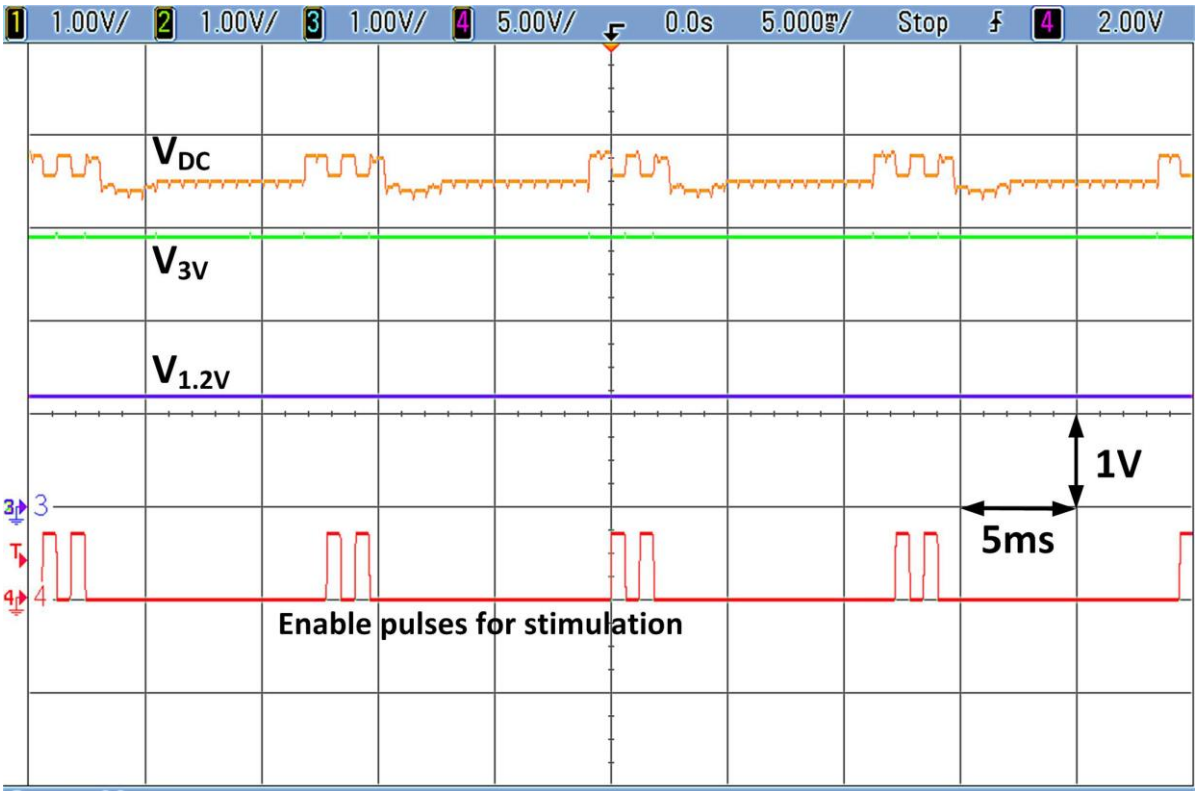



Fig. 7.5 Measured voltage waveforms of the $V_{DC}$, $V_{3V}$ and $V_{1.2V}$.

### 7.4 Conclusion

In this chapter, functional blocks of a PMU as a design example for the retina micro-current electrical neuromuscular stimulation (MENS) implant device are introduced. With the good PSR at the wireless power transmission frequency, clean and stable supplies are obtained for the functional circuits in the implantable medical device.

# Chapter 8 AN NMOS-LDO REGULATED SWITCHED-CAPACITOR POWER CONVERTER

As discussed in previous chapters, fully-integrated and high-efficiency power converters with fast response and small output ripple are needed for implantable medical devices. In this chapter, a fully-integrated NMOS source-follower low-dropout regulated step-down switched-capacitor DC-DC converter with fast-response adaptive-phase (Fast-RAP) control giving an output voltage ripple lower than 2 mV is demonstrated in 65 nm CMOS process.

## 8.1 DC-DC Converter and LDO in Cascade

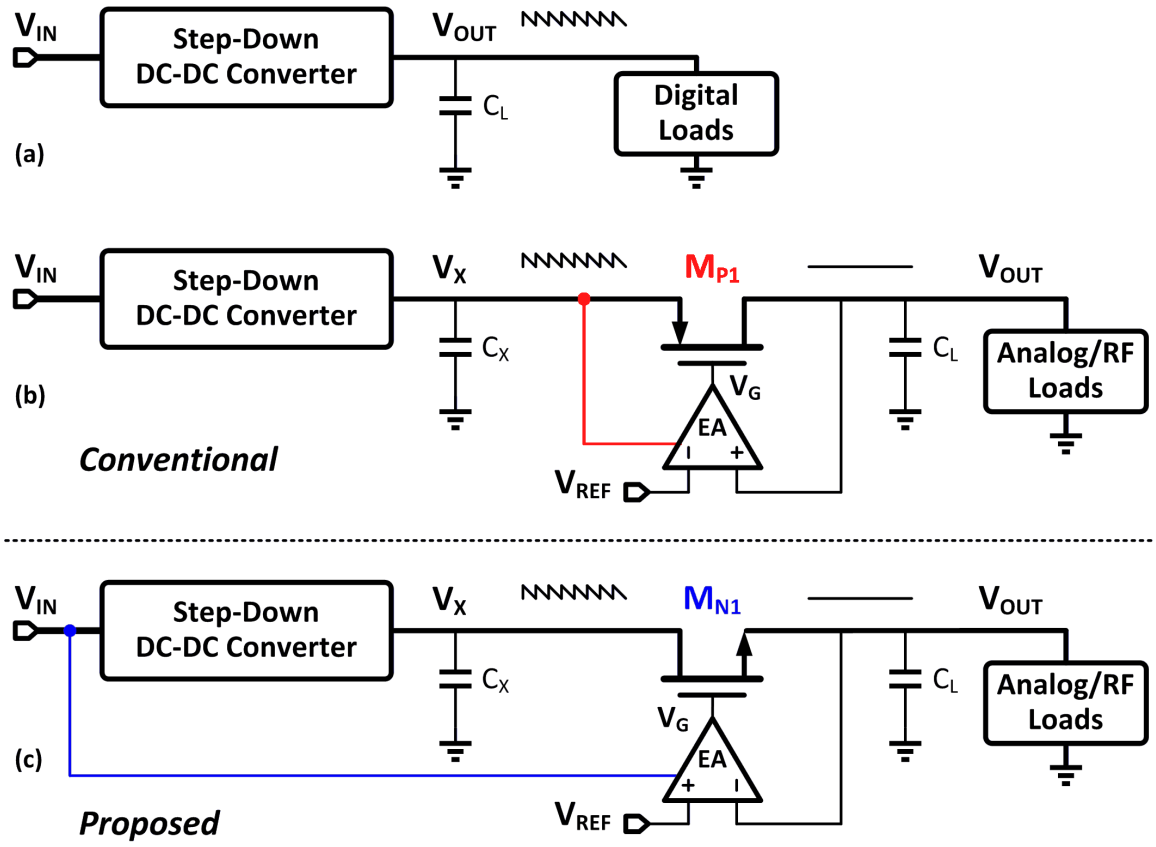



Fig. 8.1 Conventional PMOS-LDO regulated and proposed NMOS-LDO regulated architecture for connecting DC-DC converter and LDO in cascade.

As shown in Fig. 8.1, digital loads can be directly supplied by a DC-DC converter, while the analog/RF loads should be supplied by an LDO in suppressing switching noise of the supply. The power transistor of an LDO is commonly a PMOS transistor as the gate voltage $V_G$ can easily be driven by low voltage. However, the output impedance $r_o$ of a common-source PMOS power stage is high, and gives a low-frequency pole at $V_{OUT}$ that limits the loop bandwidth. Despite a high driving voltage is needed, the NMOS source-follower power stage is at times preferred because it has low $r_o$ that gives an output pole with higher frequency and faster transient responses.

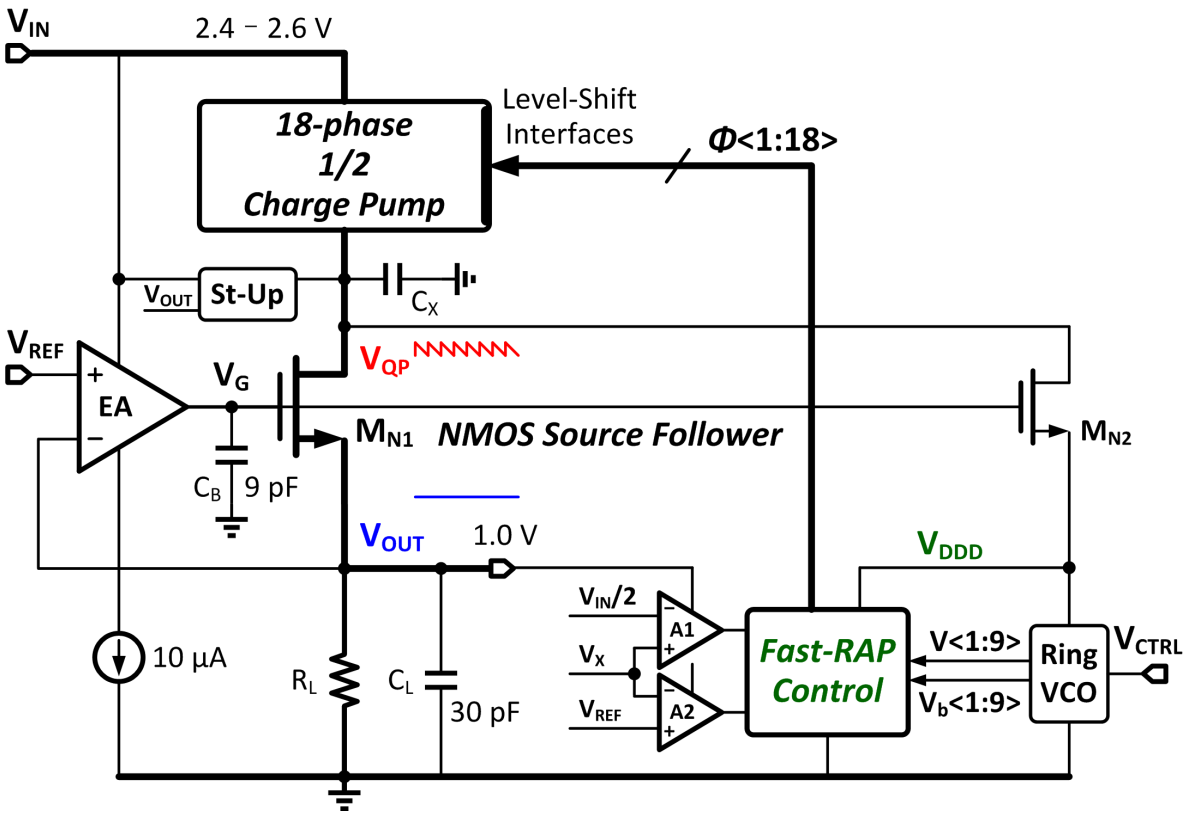



Fig. 8.2 Block diagram of the fully-integrated NMOS-LDO regulated switched-capacitor DC-DC converter with fast-response adaptive-phase control.

As shown in Fig. 8.2, this work presents a fully-integrated NMOS source-follower based low-dropout regulator (NMOS-LDO) in cascade with a step-down switched-capacitor DC-DC converter (or charge pump) with fast-response adaptive-phase (Fast-RAP) control and less than 2mV output ripple in 65 nm GP CMOS. The switching frequency of the charge pump

(QP) is 90 MHz, and the maximum efficiency of the QP is 80.3%. To achieve high efficiency at light load, the Fast-RAP controller uses fewer phases, and it commands to use more phases (1/3/9/18) as the load increases. Even at full load, the output ripple of the QP at $V_{QP}$ is very small, and is further attenuated by a 50 mV NMOS-LDO with only 4.1% efficiency overhead.

For the proposed QP+LDO combo, the input voltage is 2.4 V to 2.6 V, the output voltage is 1.0 V, and the power supply of the cascode error amplifier (EA) is tied to $V_{IN}$ to drive the gate of $M_{N1}$. Schematic of the EA and the start-up circuit is shown in Fig. 8.3. The start-up circuit consumes less than 1 μA quiescent current.

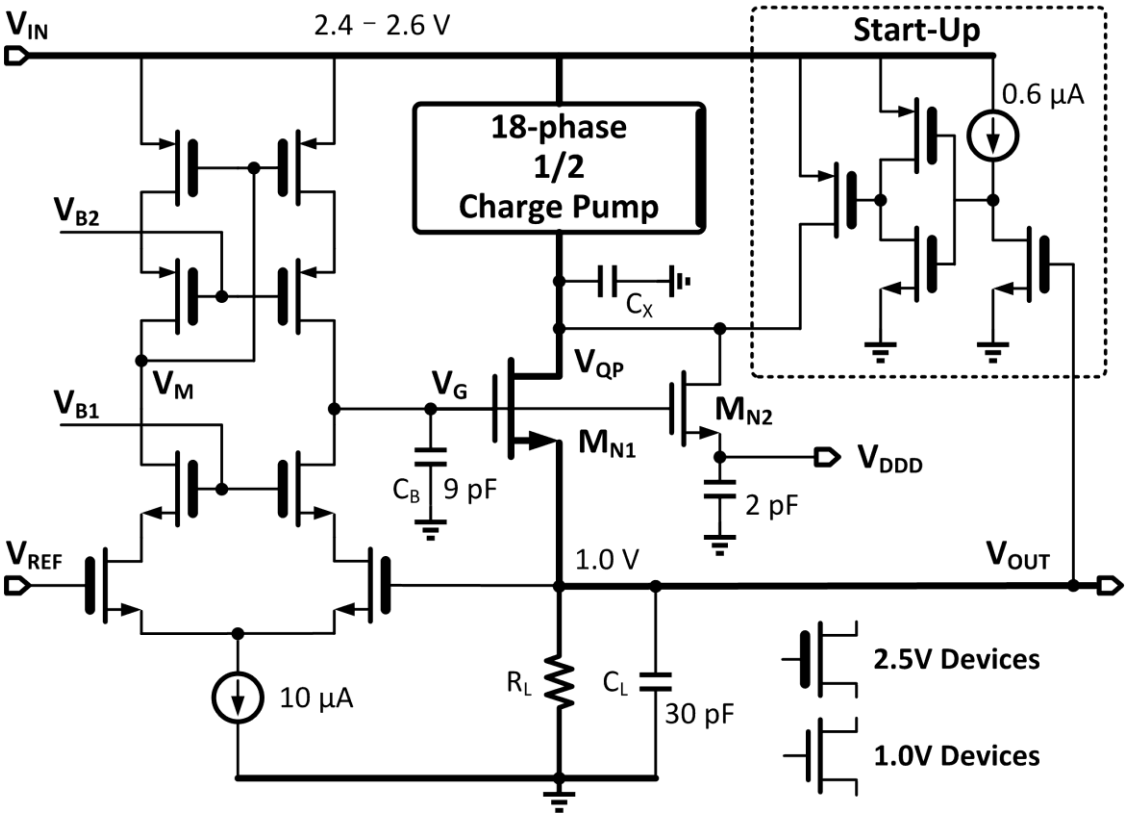



Fig. 8.3 Schematic of the cascode error amplifier and the start-up circuit.

The voltage drop across the QP output $V_{QP}$ and the LDO output $V_{OUT}$ can be <50 mV. A by-pass capacitor $C_B$ = 9 pF is added to suppress noise at $V_G$ and consequently $V_{OUT}$ has very low voltage ripples. Another power MOS $M_{N2}$ shares $V_G$ with $M_{N1}$ and generates an auxiliary $V_{DDD}$ to drive the digital controller and the current-starved 9-inverter ring oscillator (VCO), isolating digital circuit noise from affecting $V_{OUT}$. By using NMOS as the pass transistor, the

LDO output pole becomes a non-dominant pole, while the dominant pole is set by $C_B$ and is located at $V_G$.

### 8.2 Control Loop for Fast Response

Hysteretic control, with single- or multi-boundary, is popular due to its fast response and good stability [61]. However, hysteretic or any other ripple-based control methods cannot achieve small output ripple as they need a relatively large output ripple to define the trip points unambiguously [62]. Pulse frequency modulation (PFM) with a load-dependent switching frequency is another popular control method with the advantage of high efficiency over a wide load range, but suffers from slow responses and a load-dependent noise spectrum [63]. To achieve fast load response, Ref. [64] proposed a fast loop triggered by an additional 3.3 GHz clock that bypasses the main integrator loop when the output voltage is lower than its low limit, but such a high frequency clock may not be available in many low-power applications such as implantable medical devices.

Our Fast-RAP control scheme is sketched in Fig. 8.4. Instead of using a separate clock for fast response, a frequency tripler (3xClk) that makes the controller to response three times faster is implemented by interleaving phases of the VCO. The 3xClk is generated by V<1> XOR V<4> XOR V<7> that are VCO phases. Similarly, a 9xClk could be generated with the 9-inverter VCO, but to achieve a lower quiescent current, the 3xClk is adopted.

One period of the 9-inverter VCO is T, and one period of the 3xClk is T/3. To avoid phase-number oscillation (to be discussed shortly), a much lower frequency clock Clk/4 is generated by dividers, logics and VCO phases, and the period is 4T. The Fast-RAP controller reads its inputs at the falling edge of every 3xClk, so the pulse width of one “Down” signal should be shorter than T/3 to avoid false multiple-reading. The rising edge of Clk/4 is designed to be leading the falling edge of 3xClk to satisfy the setup time requirement.

The Fast-RAP controller controls the number of phases of the QP to be used, and tries to keep the output voltage $V_{QP}$ within the upper boundary $V_{IN}/2 - V_{OS1}$ and the lower boundary $V_{REF} + V_{OS2}$. The phase number does not change in the steady state. When the load current $I_{Load}$ suddenly increases and drives $V_{QP}$ down to be lower than $V_{REF} + V_{OS2}$, "Up" is set to 1, and the

Fast-RAP controller will enable all 18 phases within half of 3xClk period (T/6) to drive $V_{QP}$ up fast. However, if $V_{QP}$ is higher than $V_{IN}/2 - V_{OS1}$ (due to over-charging or decreasing in load current), "Down" is set to 1, and the phase number will be reduced by only one step (from 18→9, or 9→3, or 3→1) within 4T initiated by Clk/4. Hence, the phase number goes up fast to accommodate for a large $I_{Load}$; and goes down slowly and step by step when $I_{Load}$ decreases, to avoid phase-number oscillations. The offset voltages $V_{OS1}$ and $V_{OS2}$ are generated by unbalanced input transistor sizes of the amplifiers A1 and A2, and are designed to be 30 mV and 80 mV, respectively. In the typical case with $V_{IN}$ = 2.5 V, for example, the hysteresis window for phase-number control is from 1.08 V to 1.22 V that is large enough to avoid phase number oscillation at any fixed $I_{Load}$.

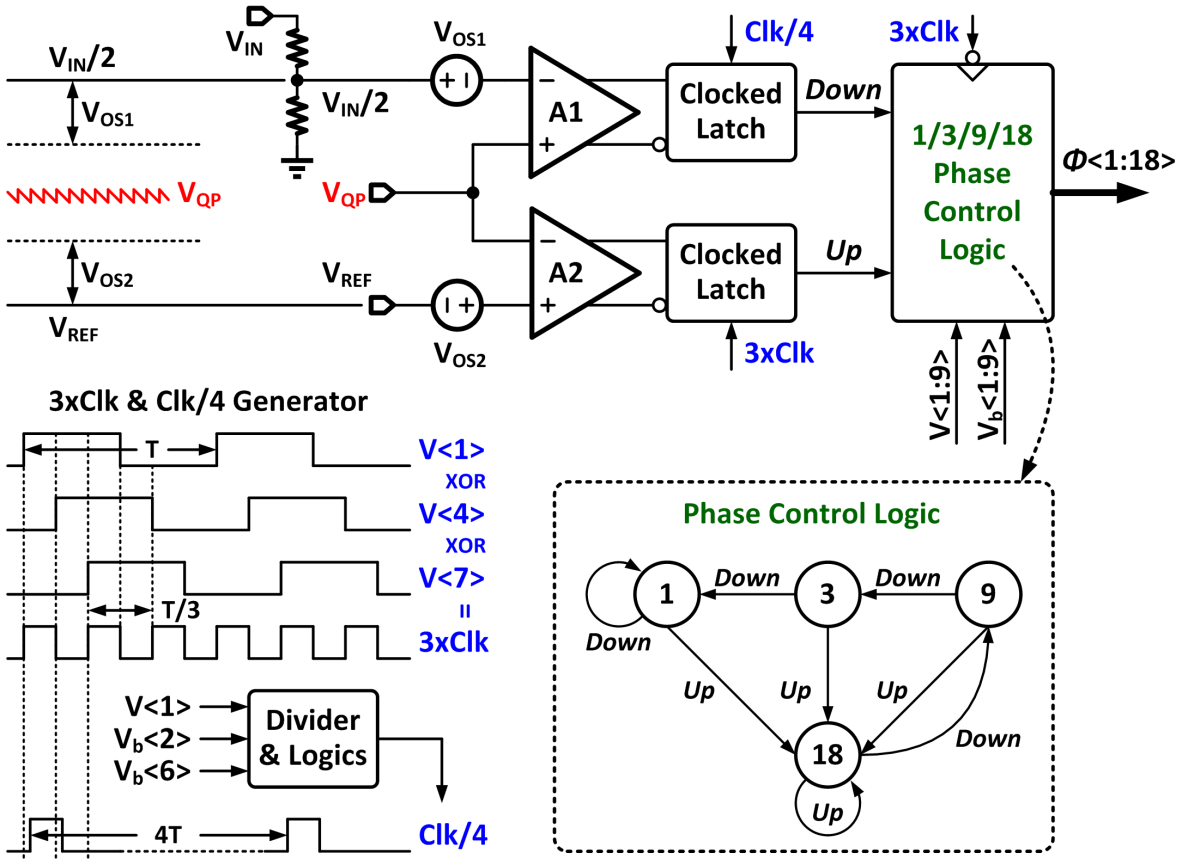
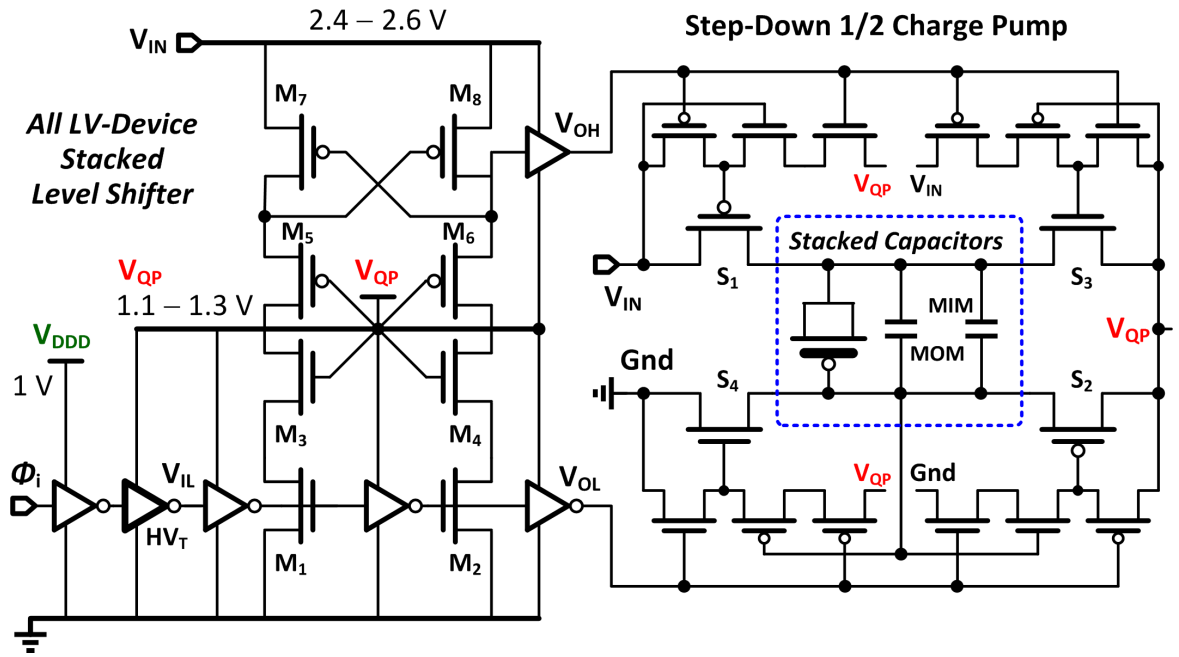



Fig. 8.4 The Fast-RAP control logic with clock frequency tripler (3xClk) and pulse divider (Clk/4) and Up/Down signal generated by comparing $V_{QP}$ with $V_{REF}$ and $V_{IN}/2$.

### 8.3 Unit Cell of the QP

Fig. 8.5 shows the unit cell of the 18-phase QP implemented with only low-voltage (LV) transistors. The clock phases have to be passed from the Fast-RAP controller with a supply voltage $V_{DDD}$ (= 1 V) to the unit cell with a supply voltage $V_{QP}$ (1.1 to 1.3 V), and a level shifter (an inverter) between $V_{DDD}$ and $V_{QP}$ is needed. As $V_{DDD}$ is lower than $V_{QP}$, the PMOS of this inverter cannot be completely turned off when the inverter input is "1", and high-$V_T$ transistors are used to reduce sub-$V_T$ leakage current in this state. A stacked level shifter (LS) is employed to further convert the phase signal from the ($V_{QP}$, Gnd) domain to the ($V_{IN}$, $V_{QP}$) domain [6]. The improvements of the stacked LS over the conventional high-voltage (HV) device LS is listed in the table. The delay time and the power consumption are reduced by 3 and 2 times, respectively. To realize non-overlap timing and consequently eliminate the reverse current, 3-transistor based inverters are utilized to drive the power switches $S_1$ through $S_4$. The flying capacitor $C_{FLY}$ (30 pF for each phase) is realized by connecting HV PMOS, MOM and MIM capacitors in parallel to reduce gate-leakage current and increase capacitance as well as power density.




| LS $V_{IL}$ to $V_{OH}$ | Conventional | Stacked | Improvement | Conditions |
|---|---|---|---|---|
| $T_{D,Rise}$ (ps) | 120.7 | 40.2 | 300.3% | $V_{IN}$ = 2.5 V |
| $T_{D,Fall}$ (ps) | 305.0 | 93.0 | 328.0% | $V_{QP}$ = 1.1 V |
| Power (µW) | 13.7 | 6.05 | 226.4% | F = 100 MHz |

Fig. 8.5 Unit cell of the 18-phase charge pump with all low-voltage (LV) device stacked level shifter (LS) and a high-$V_T$ inverter at $V_{DDD}$ to $V_{QP}$ interface.

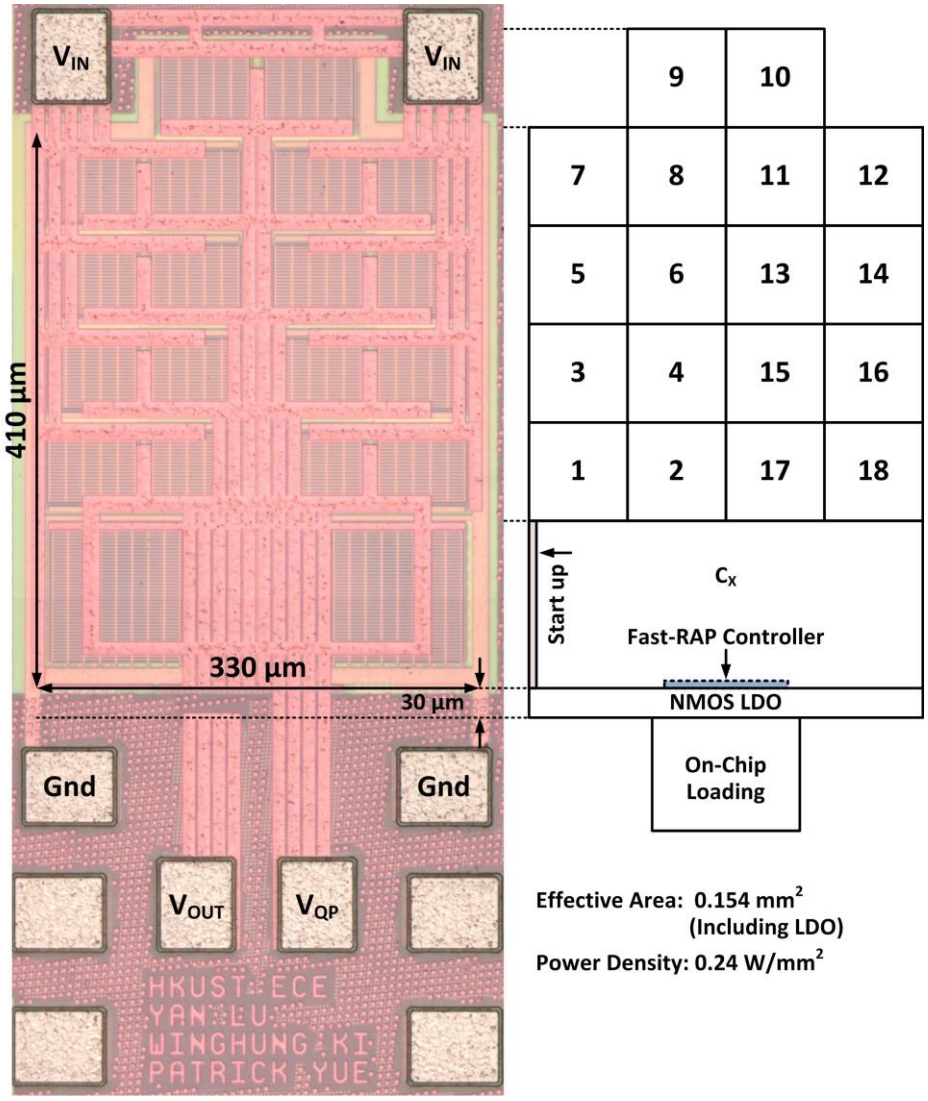



Fig. 8.6 Chip micrograph of the NMOS-LDO regulated QP.

### 8.4 Measurement Results

The chip micrograph is shown in Fig. 8.6. The effective area is 0.154 $mm^2$, including the fully-integrated NMOS-LDO that occupies only 0.01 $mm^2$. Fig. 8.7 shows the measured output spectrums of $V_{QP}$ and $V_{OUT}$ with $V_{IN}$ = 2.5 V, $V_{OUT}$ = 1 V and $f_{SW}$ = 90 MHz. With an on-chip load current $I_{Load}$ = 10 mA, the maximum noise power at $V_{QP}$ (due to the output ripple at $V_{QP}$) is –49.1 dBm, corresponding to 2.2 $mV_{P-P}$ on a 50 Ω resistor, while the noise power at $V_{OUT}$ is –64.1 dBm (0.39 $mV_{P-P}$), an attenuation of 15 dB. With $I_{Load}$ = 20 mA, the maximum noise power at $V_{QP}$ is –40.9 dBm (5.7 $mV_{P-P}$), while the noise power at $V_{OUT}$ is –54.3 dBm

(1.22 $mV_{P-P}$), an attenuation of 13.4 dB. Therefore, output ripples are well-attenuated by the merged LDO.

Fig. 8.8 shows the measured overall efficiency $\eta_{QP+LDO}$ and derived QP efficiency $\eta_{QP}$ at $f_{SW}$ = 90 MHz. The peak $\eta_{QP+LDO}$ is 76.2% when the peak $\eta_{QP}$ is 80.3%, achieving a power density of 0.24 W/mm$^2$. Light-load efficiencies are significantly improved by the adaptive-phase scheme.

Fig. 8.9 shows the measured load transient waveforms of $V_{QP}$ and $V_{OUT}$ with 200 ps rise/fall time of load current changes. By installing the 3xClk for the controller, the phase number can quickly be changed from 1/3/9 at light load to 18 at heavy load. Consequently, the voltage droop at $V_{QP}$ is reduced. The undershoot voltage of $V_{OUT}$ is 83 mV for a 20 mA current step.

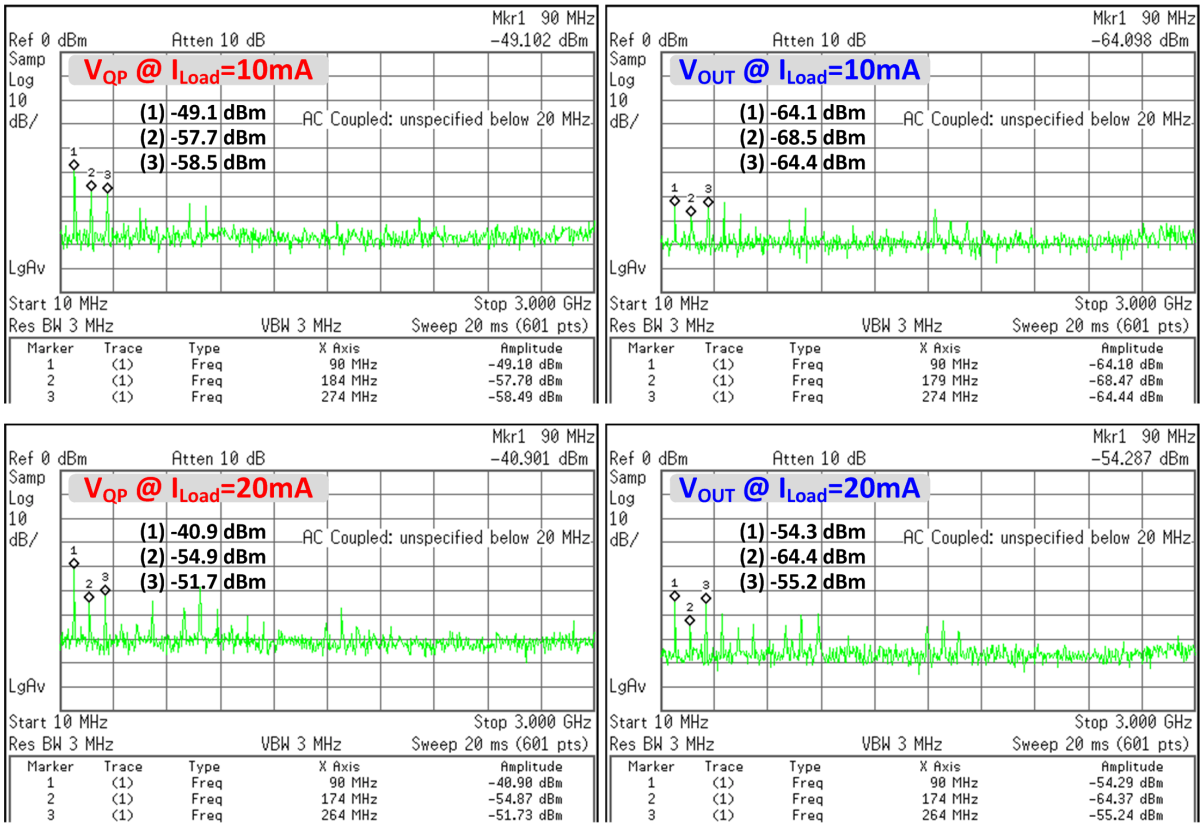



Fig. 8.7 Measured output spectrums of $V_{QP}$ and $V_{OUT}$ with $I_{Load}$ = 10 mA and 20 mA, respectively, at $V_{IN}$ = 2.5 V.

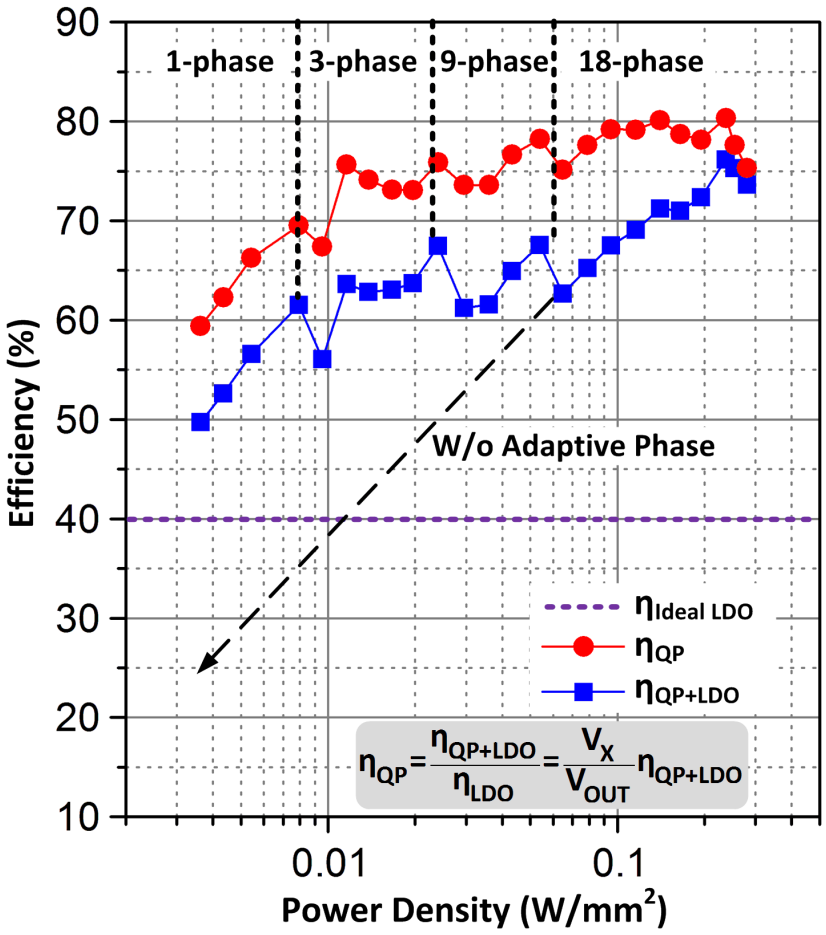



Fig. 8.8 Measured total efficiency $\eta_{QP+LDO}$ and derived $\eta_{QP}$ at $f_{SW}$ = 90 MHz.

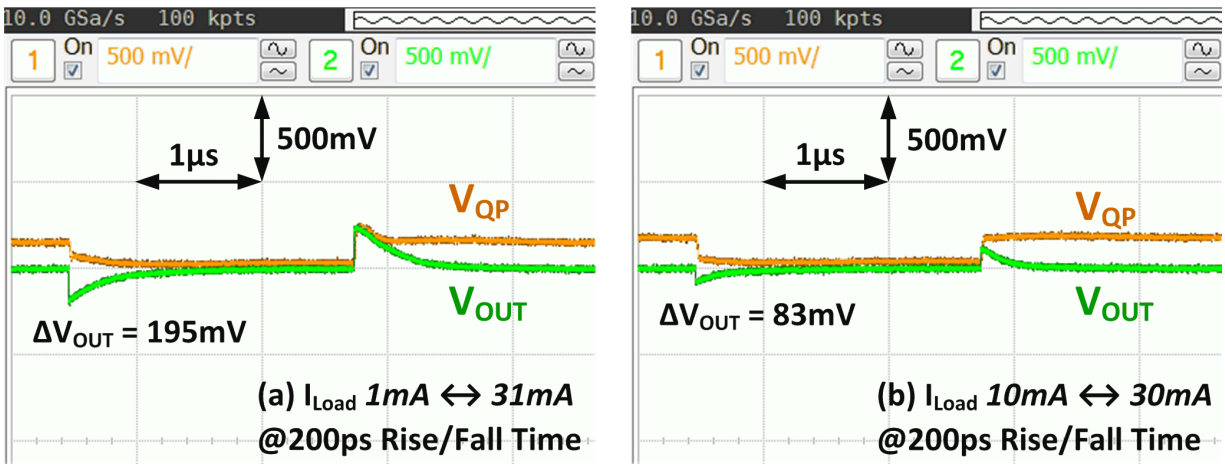



Fig. 8.9 Measured transient response with on-chip loading.

Table 8.1 summarizes the performance comparison of the proposed QP+LDO combo with state-of-the-art QP designs. Our design achieves the smallest output voltage ripple at higher power density. The performance summary of the LDO is also listed, and the figure-of-merit (FOM) defined in [46] is adopted. The calculated response time $T_R$ and FOM are 0.254 ns and 0.085 ps, respectively, and both are ultra-small.

Table 8.1 COMPARISON WITH PRIOR QP WORKS AND SUMMARY OF THE NMOS-LDO

| QP Work | [3] 2011 | [4] 2012 | [2]2013 | **This Work** |
|---|---|---|---|---|
| Technology | 90nm | 90nm | 65nm | **65nm** |
| Topology | 1/2 | 1/2, 2/3 | 1/3, 2/5 | **1/2 + LDO** |
| # Phases | 10 | 41 | 18 | **18** |
| $V_{OUT}$ | 1.3-1.5V | 0.7V | 1V | **1V** |
| $C_{FLY}$ | 2nF | 1.148nF | 3.88nF | **0.54nF** |
| $C_L$ | 3.2nF | 84pF | 0 | **0.26nF($C_X$)** |
| Power Density ($W/mm^2$)@$\eta_{Peak}$ | 0.05 | 0.039 | 0.19 | **0.24** |
| $f_{SW}$ @$\eta_{Peak}$ | 70MHz | 50MHz | N/A | **90MHz** |
| $I_{IN,\ noload}$ | 85µA | N/A | N/A | **161µA** |
| $\eta_{QP,Peak}$ | 77% | 81% | 74.3% | **80.3%** |
| $\eta_{QP+LDO,Peak}$ | N/A | N/A | N/A | **76.2%** |
| $V_{OUT}$ Ripple | N/A | 3.8mV | N/A | **2mV** |

| **LDO in This Work** | |
|---|---|
| $V_{IN}$ | **2.4-2.6V** |
| $V_{OUT}$ | **1V** |
| Dropout | **50mV** |
| C ($C_B$+$C_L$) | **39pF** |
| $I_Q$ | **10µA** |
| $I_{MAX}$ | **30mA** |
| $\Delta V_{OUT}$ | **83mV @ 10mA↔30mA 195mV @ 1mA↔31mA** |
| DC Reg. | **0.2mV/mA** |
| $T_R$* | **0.254ns** |
| FOM* | **0.085ps** |

$$* \mathbf{FOM} = T_R \frac{I_Q}{I_{MAX}} = \frac{C \times \Delta V_{OUT}}{I_{MAX}} \times \frac{I_Q}{I_{MAX}}$$

## 8.5 Conclusions

In this chapter, a fully-integrated NMOS source-follower low-dropout regulated step-down switched-capacitor DC-DC converter with fast-response adaptive-phase control and < 2 mV output voltage ripple is demonstrated in 65 nm CMOS process. Operating at 90 MHz with the 18-phase interleaving scheme, the output voltage ripples at the QP output are small. The maximum QP efficiency is 80.3%, and is only slightly attenuated at $V_{OUT}$ by a 50mV dropout regulator with an efficiency overhead of only 4.1%, and an area overhead of only 6.5%.

Light-load efficiency is improved by the adaptive-phase control, and the smallest output ripple is achieved in this work with the 18-phase QP. In fact, this chip is the first switched-capacitor DC-DC converter that implements adaptive phase for efficiency optimization without sacrificing the transient response.

# Chapter 9 CONCLUSIONS AND FUTURE WORKS

## 9.1 Thesis Conclusions

Wireless power transfer has numerous applications that include implantable medical devices (IMDs), RFIDs, electric vehicle and mobile phone wireless chargers. In this research, power management related to wireless power transfer for IMDs is investigated. There are many design challenges and among which is miniaturized size. The transmission frequency of 13.56 MHz in the ISM band with near-field operation was chosen to give a good tradeoff among efficiency, device volume and power level.

There are many sources of power loss that result in efficiency degradation: from the transmitter circuits there are the power amplifier and its supply modulator; from the receiver circuits there are AC-to-DC power conversion, DC-to-DC power conversion, and voltage regulation; and there are the resonant tanks of both the primary and the secondary sides. The efficiency of the receiver circuit is of critical importance as it is related to thermal dissipation of the implanted devices into the tissue of the living subject. Thus, the AC-to-DC power conversion on the receiver side is chosen to be the starting point of this research.

Active rectifiers are widely used in low-voltage AC-to-DC power conversion, to achieve higher voltage conversion ratio and power conversion efficiency (PCE). However, active rectifiers also suffer from active diode delay problem which would introduce reverse current and consequently degrade the efficiency. Delay time of the active diode was calculated and simulated in this research, and it was shown to be inversely proportional to the voltage of the power supply. Different comparator delay compensation schemes were proposed to solve this problem, but each scheme has its pros and cons as discussed in this thesis. A switched-offset scheme for high-speed high-current active rectifier for biomedical implants was proposed. Longer conduction time was achieved without sacrificing robustness, and the multiple-pulsing problem related to dynamic offset was eliminated through careful design of the digital logic. Two rectifiers (Rec1 and Rec2) with peaking current source and QIPV biasing circuit

respectively were implemented and measured, verifying that they could operate efficiently over wide input amplitude and wide load current range. The comparators of the second active rectifier were biased with a novel QIPV biasing circuit, and reverse current was much reduced at low $|V_{AC}|$, and was eliminated at high $|V_{AC}|$. Compared to previous 13.56 MHz designs, both the voltage conversion ratio (VCR) and PCE at low $|V_{AC}|$ and at heavy loading have been improved. An area-efficient reconfigurable 1X/2X active rectifier (Rec3) was further introduced. The filtering capacitor $C_L$ was integrated on-chip with a switching arrangement that avoid connecting the output capacitors in series in the 2X mode. The lowest input $|V_{AC}|$ was extended from 1.5 V down to 1.25 V in Rec3 by using the proposed reconfigurable architecture, and the VCRs and PCEs were improved with proper design of the bias current for reverse current control.

For DC-to-DC power conversion, a dual-output charge pump with variable fractional-*M* conversion ratio was proposed. It was inserted between the rectifier and the LDOs in the PMU for inductively coupled wireless power transfer. Interleaving scheme was used to control the fractional capacitors such that the conversion ratio could assume many values according to change in the input voltage. Simulation results showed that the efficiency of the PMU was improved over a wide input range.

For voltage regulation, a fully-integrated low-dropout regulator with ultra-fast transient response and full spectrum power supply rejection (PSR) characterization was presented. A tri-loop architecture based on the buffered flipped voltage follower (FVF) was proposed and verified in 65 nm CMOS process. By comparing the design methodologies of previous non-fully-integrated and fully-integrated LDO regulator designs, a gap between transient responses and PSR performance was identified, investigated and filled in this research. The output-pole dominant FVF structure was employed for its fast transient response and good medium- and high-frequency PSR. With the combined effects of the high-bandwidth loop-1 (dealing with the low-frequency range), $C_L$ (dealing with the high-frequency range) and $C_B$ (dealing with the medium-frequency range), good full spectrum PSR was achieved. With the additional loop-3, $V_{OUT}$ DC accuracy was improved by 3 times compared to the conventional FVF-based LDO. As FOM scales with process, the proposed architecture would perform even better using more advanced processes. In Chapter 7, a PMU design example for the retina micro-current electrical neuromuscular stimulation (MENS) implant device was introduced.

With good PSR at the wireless power transmission frequency, clean and stable supplies were obtained for the functional circuits in the implantable medical device.
Last, but not the least, a charge pump + LDO combo was proposed. Small output ripple, fast transient response and flat power efficiency were achieved simultaneously by combining the advantages of charge pump and LDO.

### 9.2 Future Works

All my previous wireless power link designs were designed to operate at 13.56 MHz [22], [26], [32]. However, other ISM frequencies such as 6.78 MHz, 40.68 MHz, 434 MHz and 869 MHz could also be considered. One question I would like to answer is this: what is the optimum frequency of the wireless power link in the 0.5 cm to 2 cm range for cochlear/retinal prosthesis and deep-brain stimulators?

To answer this question, higher frequency bands certainly need to be investigated. Also, RF-to-DC converters which usually achieve only a peak efficiency of 30% should be improved. As the input voltage is close to the MOSFET threshold voltage, a rectifier with multi-stages is required [18]. The optimized solution for different applications should depend on combinations of different rectifier topologies with different number of stages. In addition, optimization in the system level should be made: good transient response is needed when subject to load changes and coil movements. A power-efficient and robust wireless power transmission system remains my future research goal.

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# BIOGRAPHY AND PUBLICATIONS

## Biography

**Yan Lu** (路延) received the B. Eng. degree and the M. Sc. degree in microelectronic engineering from South China University of Technology, Guangzhou, China, in 2006 and 2009, respectively. He joined the Hong Kong University of Science and Technology as a PhD student in 2009 Fall.

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Lu was the recipient of the following awards: the Outstanding Postgraduate Student Award of Guangdong (Canton) Province in 2008, the PhD Student Overseas Research Award 2012-13, the School of Engineering PhD Fellowship of HKUST in 2013, and the IEEE Solid-State Circuits Society Predoctoral Achievement Award 2013-2014.

# Publications

**Book Chapter**

[1] Wing-Hung Ki, **Yan Lu**, Feng Su, and Chi-Ying Tsui, "Analysis and Design Strategy of On-Chip Charge Pumps for Micro-Power Energy Harvesting Applications," *VLSI-SoC: The Advanced Research for Systems on Chip*, Springer, pp. 158-186, Aug. 2012.

**Journal Papers**

[2] **Yan Lu**, Wing-Hung Ki, "A 13.56MHz CMOS Active Rectifier with Switched-Offset and Compensated Biasing for Biomedical Wireless Power Transfer Systems," *IEEE Trans. on Biomedical Circuits and Systems*, to appear.

[3] **Yan Lu**, Gang Yuan, Lawrence Der, Wing-Hung Ki, and C. Patrick Yue, "A ±0.5% Precision On-Chip Frequency Reference with Programmable Switch Array for Crystal-Less Applications," *IEEE Trans. on Circuits and Systems-II: Express Briefs*, vol. 60, pp. 642-646, Oct. 2013.

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**Conference Papers**

[5] **Yan Lu**, Wing-Hung Ki, and C. Patrick Yue, "A 0.65ns-Response-Time 3.01ps FOM Fully-Integrated Low-Dropout Regulator with Full-Spectrum Power-Supply-Rejection for Wideband Communication Systems," *IEEE International Solid-State Circuits Conference (ISSCC)*, 2014, to appear.

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