Device Technology and Integration for GaN-based Sensors and High-frequency Power Electronics

by

Xing LU

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January 2015

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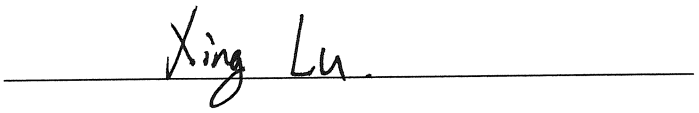

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Abstract

Wide bandgap gallium nitride (GaN) and related compounds possess superior material properties, including high electron saturation velocity, large breakdown electric field, and sustainability at high operating temperatures. Because of strong spontaneous and piezoelectric polarization effects, GaN-based heterostructures forming a two-dimensional electron gas (2DEG) channel with large sheet carrier concentration and high electron mobility are ideal for high-frequency power electronics. In addition to other characteristics such as high acoustic velocity, high mechanical and thermal stability and inherent chemical inertness, GaN has also been considered as an attractive thin film piezoelectric material for fabrication of on-chip acoustic wave devices. This dissertation aims at the exploration of GaN-based device technologies and their integration for applications in novel sensors and high-frequency power electronics.

In this thesis, monolithic integration technology of acoustic wave devices with high electron mobility transistors (HEMTs) on AlGaN/GaN heterostructures has been demonstrated. High performance Lamb-wave sensors were designed and fabricated using a GaN-on-Si platform. Then two on-chip oscillators were implemented by monolithically integrating a Lamb-wave or a surface acoustic wave (SAW) delay line device with AlGaN/GaN HEMT circuitries. The monolithic oscillators in this work, which are suitable for sensor systems operating at high ambient temperature, could potentially be extended to high-frequency power applications.

A scalable gate-last self-aligned technology was developed for fabrication of GaN-based metal-insulator-semiconductor high electron mobility transistors (MISHEMTs). Source/drain (S/D) regrowth and low-k benzocyclobutene (BCB) planarization techniques were employed to reduce the access resistance and parasitic capacitance, minimizing the RC-related delay. Thin AlN barriers and *in-situ* grown SiN_x gate dielectrics by metal-organic chemical vapor deposition (MOCVD) were incorporated to facilitate the device scaling, with increased gate control capabilities, maintaining high channel conductivity and suppressing the gate leakage. The fabricated gate-last self-aligned *in-situ* SiN_x/AlN/GaN MISHEMTs exhibited high performance, demonstrating great potential for the next-generation RF/microwave power applications.

CHAPTER 1 INTRODUCTION

1.1 Background of GaN Technology

Gallium Nitride (GaN) and its alloy compounds have been considered as a promising material system for semiconductor device applications since the 1960s, from the initial breakthroughs with blue/ultraviolet (UV) light emitting diodes (LEDs) to laser diodes (LDs), UV detectors to radio frequency (RF)/microwave power electronics and then to sensors [1]. Fig 1.1.1 illustrates the wide scope of applications where GaN-based technology can be applied.

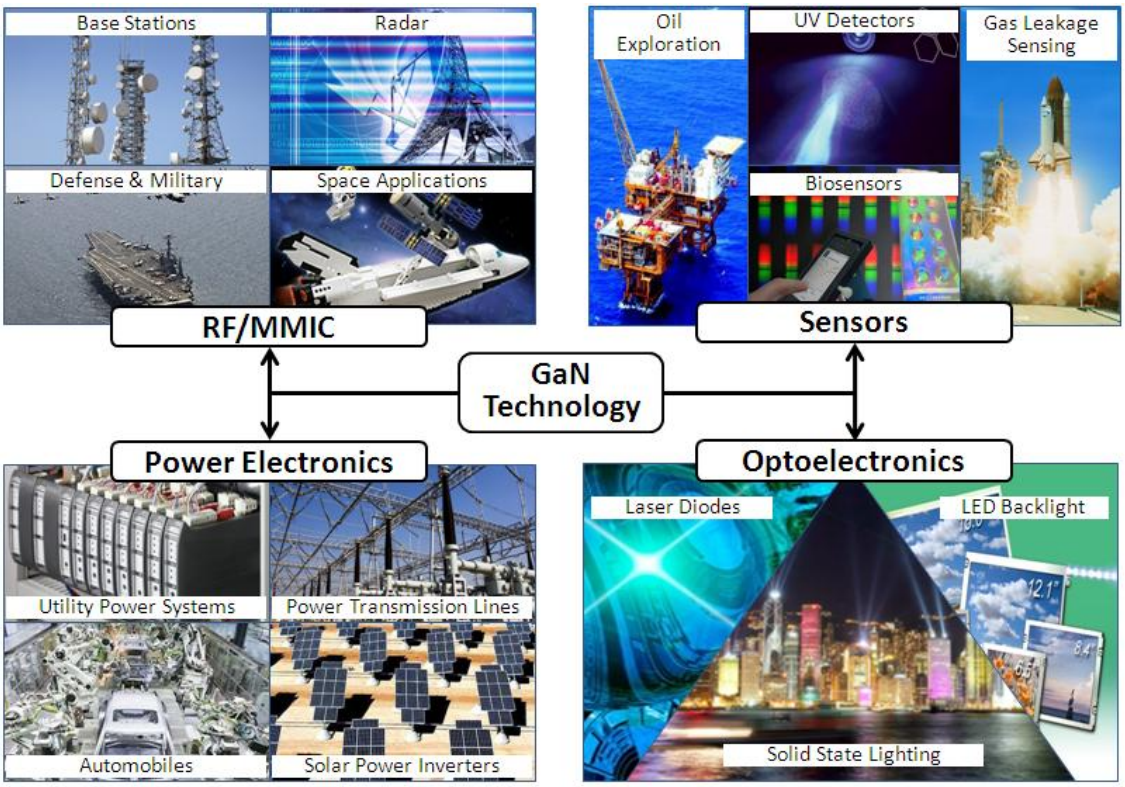

Figure 1.1.1 The applications of GaN-based technology

GaN-based LEDs and LDs have already been commercialized for a variety of lighting, display and data storage applications, which benefit from the direct and wide bandgap nature of III-nitrides, as well as the achievement of p-type conduction in GaN [2]. Featuring superior material properties, such as wide bandgap, high electron saturation velocity, and high critical

breakdown field, GaN attracts lots of attention in high speed and high power electronics intended for radar, satellite, wireless base stations, automobiles and utility grid applications. In addition, GaN-based semiconductors offer other advantageous properties, including high mechanical and thermal stability, inherent chemical inertness, strong piezoelectric effect and high acoustic velocity, making them good candidates for acoustoelectronic devices, especially sensors operating in harsh environments such as for gas leakage detection at high ambient temperature.

Table 1-1 lists the material properties of GaN and other competing materials [3-9]. Compared to conventional compounds and silicon semiconductors, GaN exhibits much better figures for most of the specifications, including a wide bandgap of 3.4 eV, a large critical breakdown field of 3.3 MV/cm, a high electron saturation velocity of 2.5×10^7 cm/s, a good thermal conductivity up to 1.5 W/ cm K and a relatively strong piezoelectric property. All these excellent and unique properties enable GaN-based devices to be a potential game changer for many key applications, especially high frequency, high power and high temperature electronics.

Table 1-1 Properties of four competing materials in semiconductor platforms.

Properties	Si	GaAs	SiC	GaN
Bandgap (eV)	1.1	1.4	3.2	**3.4**
Electron Mobility (cm^2/V s)	1350	8500	700	**1200 (bulk) 2000 (2DEG)**
Saturation Velocity (10^7cm/s)	1.0	1.3	2.0	**2.5**
Breakdown Field (MV/cm)	0.3	0.4	3.0	**3.3**
Thermal Conductivity (W/cm K)	1.5	0.5	4.5	**1.5**
Piezoelectric Property	--	Weak	Weak	**Strong**

High-quality single crystalline GaN-based heterostructures have been successfully grown on sapphire, SiC and Si substrates to fabricate high electron mobility transistors (HEMTs)

since 1993, when the first AlGaN/GaN HEMT was demonstrated [10]. During the past two decades, intensive research has been done and significant progress has been made to boost GaN HEMTs' performance, in terms of the device operation speed and the current and voltage drive capabilities [11, 12]. Fig 1.1.2 compares the material limitations on the Johnson Figure of Merit (*JFoM*) for Si, InP and GaN [13]. The *JFoM*, a common benchmarking for high-frequency high-power transistors, is determined by the product of the cut-off frequency (f_T) and off-state breakdown voltage (BV_{off}). With much higher electron saturation velocity and a larger breakdown field, GaN produces about a 4 times and 20 times higher *JFoM* than InP and Si, respectively, indicating the great potential of GaN-based HEMTs for RF/microwave power applications. High temperature operation is also important for electronics because it can reduce the burden of thermal management. Fig 1.1.3 compares the intrinsic carrier density as a function of temperature between Si, GaAs, SiC and GaN [14]. GaN-based devices, inherently featuring smaller intrinsic carrier concentration, can deliver the excellent capability of operating at high temperatures at which mainstream Si and GaAs-based devices stop functioning.

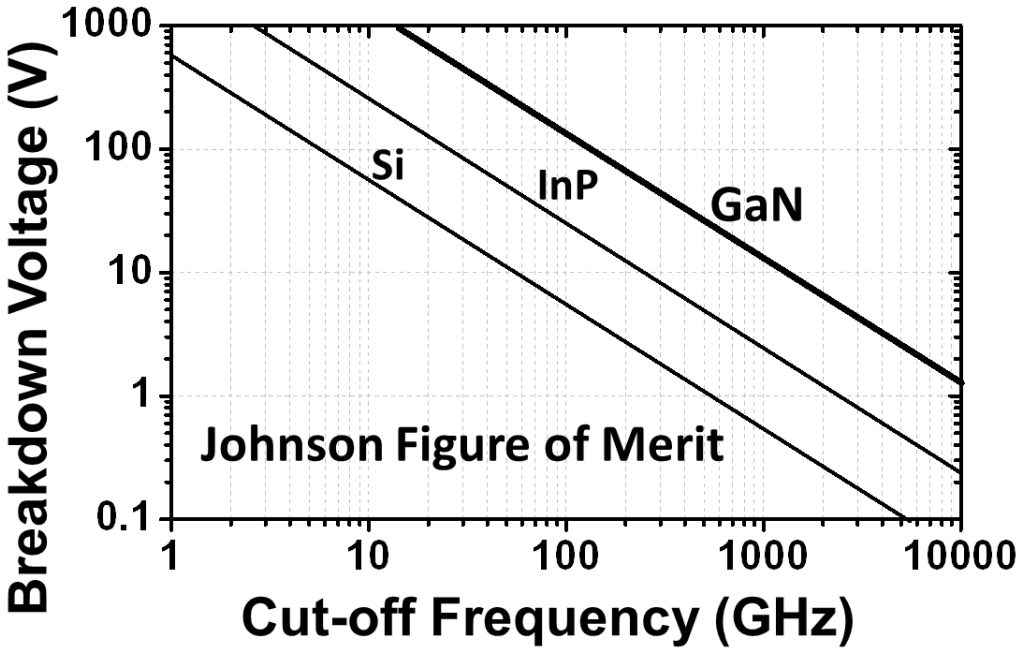

Figure 1.1.2 The material limitations on the *JFoM* for GaN, InP and Si.

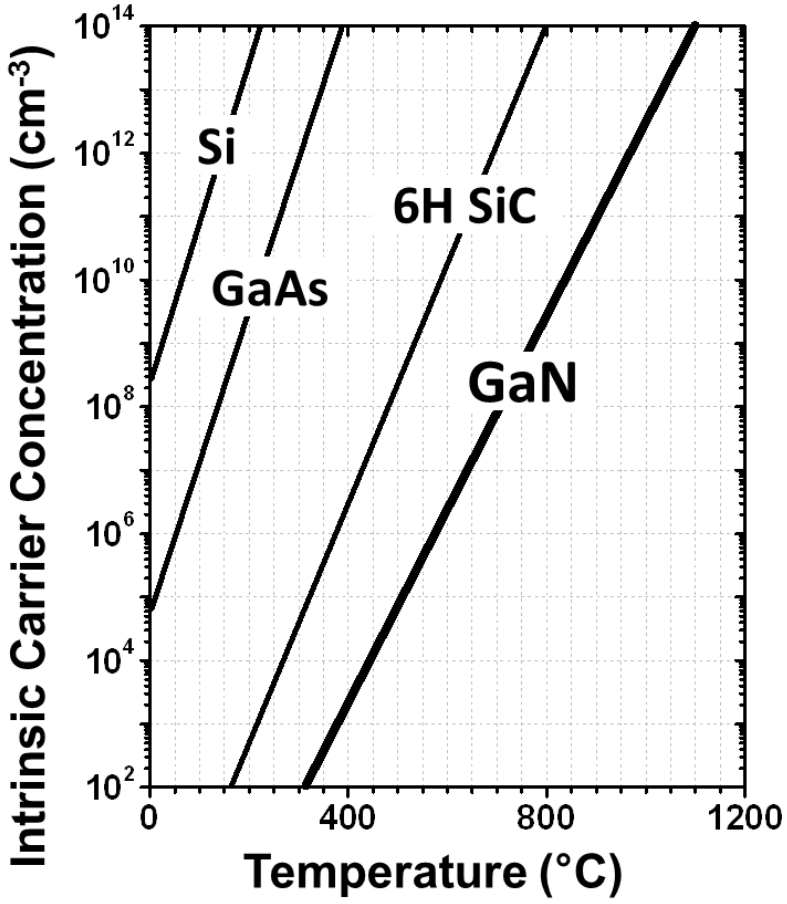

Figure 1.1.3 The temperature dependence of intrinsic carrier concentration profiles for GaN, 6H SiC, GaAs and Si.

1.2 Fundamentals of GaN-based Acoustic Wave Devices and $Al_xGa_{1-x}N$/GaN HEMTs

1.2.1 Piezoelectric effects and spontaneous polarization of III-nitrides

The crystal structure of III-nitride epitaxial layers is wurtzite, where the most common growth direction is normal to the (0001) basal plan and the bilayers consist of two closely spaced hexagonal layers [1, 15]. One of the layers is formed by cations and the other by anions, leading to polar faces. In the case of GaN, a basal surface should be either a Ga- or N-face, as shown in Fig 1.2.1. Almost all metal-organic chemical vapor deposition (MOCVD) grown nitrides are Ga-faced, while those grown in a molecular beam epitaxial (MBE) system are usually N-faced.

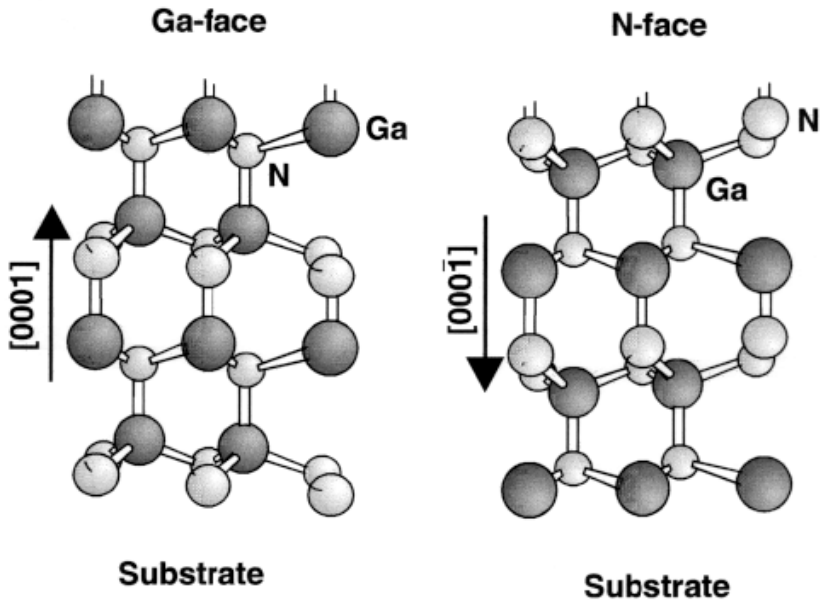

Figure 1.2.1 Crystal structures of Ga-faced and N-faced wurtzite GaN. [1]

The noncentrosymmetric III-nitride crystals lead to a strong ionicity and a residual electrical polarity of the semiconductors along the (0001) axis; therefore, both strong piezoelectric effects and spontaneous polarizations can be observed [9, 16]. The piezoelectric properties of GaN and AlN are much larger than those in conventional III-V compounds and SiC. In addition, the spontaneous polarization of III-nitrides along the (0001) axis is also very large and leads to strong electric fields up to 3 MV/cm. In this case, the piezoelectric and spontaneous polarization can have a significant influence on the electrical and optical properties of devices. This is because the induced electric fields can influence the shape of the band edges and the carrier distribution inside III-nitride heterostructures, and consequently influence the radiative recombination in light-emitting devices as well as the electrical properties of transistor structures [1, 15-18].

1.2.2 GaN-based acoustic wave devices

Acoustic wave devices based on piezoelectric materials, which allow transduction of electric and acoustic energies, have been constructed in a number of configurations for sensing and communication applications [19, 20]. The medium used to generate acoustic waves in the acoustic wave devices is generally a sputtered polycrystalline material with a

piezoelectric property, mainly AlN, ZnO, and lead zirconate titanate (PZT) [21-29]. We believe the choice of material can be extended to crystalline GaN, a wide bandgap semiconductor currently being exploited in the fabrication of LEDs and HEMTs. The piezoelectric property of GaN is modest when compared to standard piezoelectric ceramics such as PZT that possess hundreds of times higher piezoelectric constants. However, single crystalline GaN can be epitaxially grown, thus giving a very smooth surface and excellent control of layer quality, properties and thickness across the wafer. In addition, GaN offers the benefits of high acoustic velocity, high chemical, mechanical, and thermal stability, as well as monolithic integration with microelectronic systems on the basis of the same material. Hence, GaN has been considered as an attractive thin film piezoelectric material for fabrication of on-chip acoustic wave devices [6, 30, 31]. A distinction can be made depending on how the acoustic wave propagates through the piezoelectric GaN layers: Film Bulk Acoustic-wave Resonators (FBARs) [32-34], Surface Acoustic Wave (SAW) devices [35-37] and Lamb-wave, also known as Flexural Plate Wave (FPW), devices [38, 39], as shown in Fig 1.2.2.

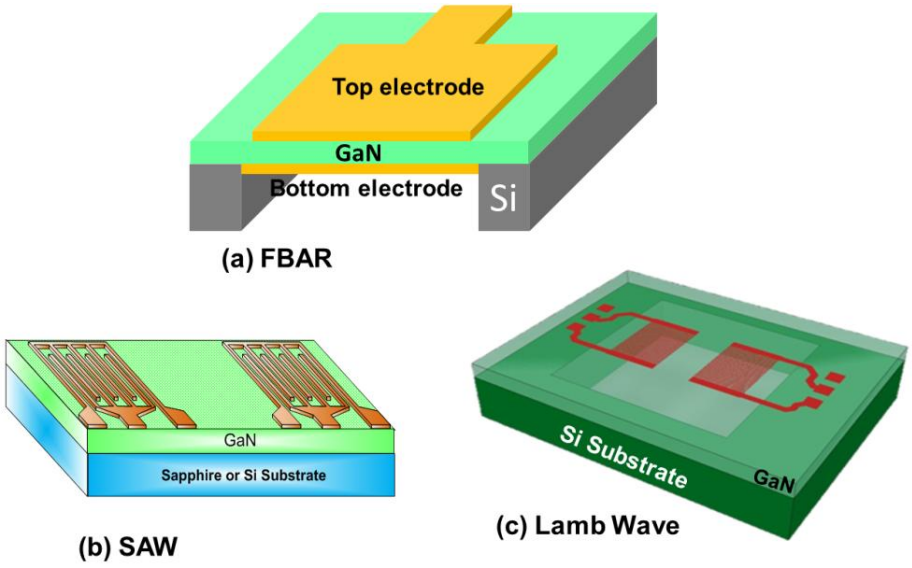

Figure 1.2.2 GaN-based acoustic wave devices: FBAR (a), SAW (b), FPW (c).

The waves that can propagate in a solid depends upon both the properties of the solid and its boundaries [19]. Fig 1.2.3 shows schematically the waves that propagate in a semi-infinite solid having a single plane boundary and in a solid plate that has two plane boundaries. The

SAW is an elastic wave traveling along the surface of a solid, with an amplitude that typically decays exponentially with depth into the substrate, as shown in Fig 1.2.3 (a). The Lamb waves propagate in a solid plate, whose particle motion lies in the plane that contains the direction of wave propagation and the direction perpendicular to the plate, as shown in Fig 1.2.3 (b). Both SAW and Lamb waves are constrained by the elastic properties of the material surfaces that guide them.

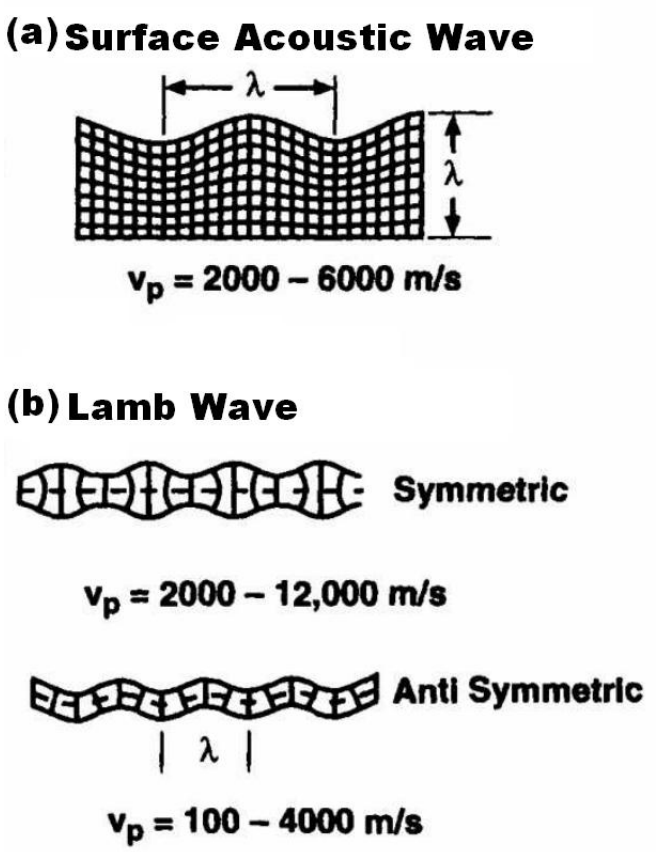

Figure 1.2.3 Pictoral representations of elastic waves in solids. Motions of groups of atoms are depicted in these cross-sectional views of plane elastic waves propagating to the right. Vertical and horizontal displacements are exaggerated for clarity. Typical wave speeds, v_p, are shown below each sketch. (a) SAW. (b) Lamb waves [19].

An interdigitated transducer (IDT) is the most convenient configuration to generate or detect SAW and Lamb waves in the settings of an acoustic wave delay line device. A delay line device consists of two IDTs on two ends of a piezoelectric substrate or membrane, serving as a transmitter or receiver. Each IDT has an array of periodic interlocking comb-shaped finger electrodes, as shown in Fig 1.2.4. [5, 19, 40, 41].

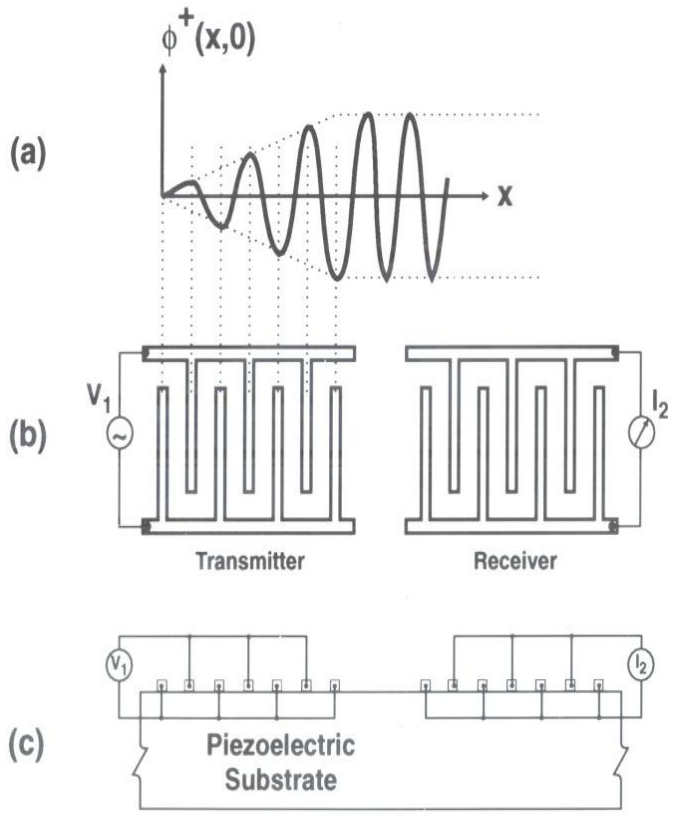

Figure 1.2.4 IDTs, formed by patterning electrodes on the surface of a piezoelectric substrate or membrane for exciting acoustic waves: (a) wave electrical potential, (b) top view, (c) side view [41].

When an alternating voltage is applied to the transmitter IDT, a periodic strain field is generated in the piezoelectric material because of the piezoelectric effect, and standing acoustic waves are produced. These standing waves will result in the propagation of waves launched away from the transmitter to the receiver. Propagation of a mechanical wave in a piezoelectric medium is accompanied by an associated wave potential (∅). When the wave is incident on a receiving IDT, the piezoelectric effect generates an electrical response that can be detected. For typical delay line acoustic wave devices, the transmitter IDT is the same as the receiver IDT so that a reciprocity relation holds. A network analyzer can be used to measure the transfer function of this set-up.

The acoustoelectric conversion is the most efficient when the acoustic wave wavelength (λ) matches the IDT periodicity, where the coherent waves contributed by each electrode pair superimpose and reinforce, and constructive interference occurs. The effect of reinforcement

increases with the number of pairs of finger electrodes. The frequency of maximum wave excitation, i.e. peak amplitude of the transfer function, is given by

$$f_{peak} = v/\lambda \tag{1.1}$$

where the acoustic velocity v is a characteristic property of the material. Fig 1.2.5 shows the typical transfer function S_{12}-Parameter of SAW devices using $Al_xGa_{1-x}N$ on sapphire substrates (x = 0, x = 0.53 and x = 1) [1]. The SAW velocity of epitaxial GaN film on sapphire substrates is around 4000 m/s.

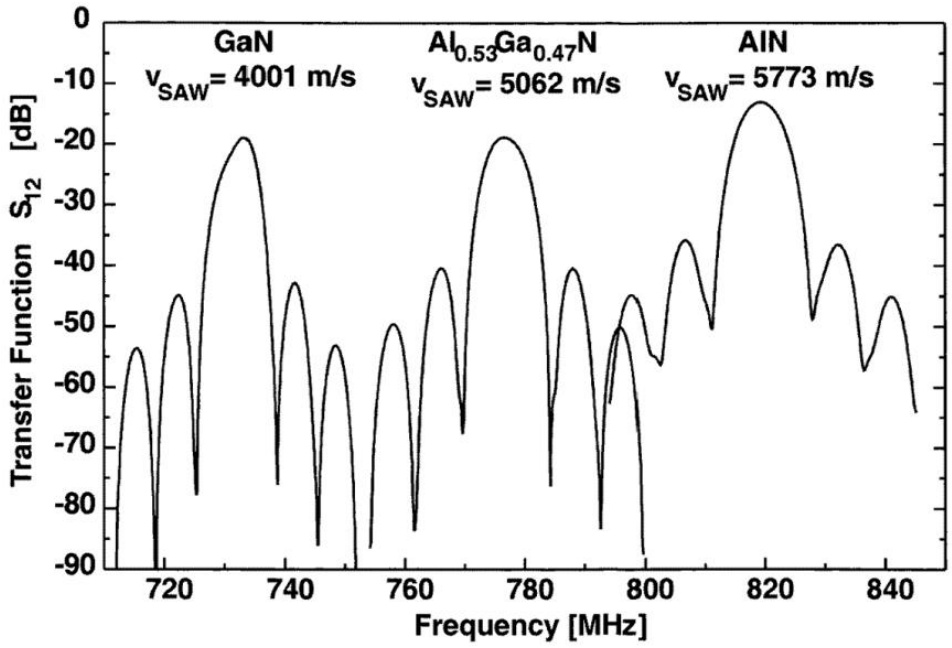

Figure 1.2.5 The typical transfer function S_{12}-Parameter of SAW devices using $Al_xGa_{1-x}N$ on sapphire substrates (x = 0, x = 0.53 and x = 1). [1]

1.2.3 $Al_xGa_{1-x}N$/GaN-based HEMTs

With a direct bandgap ranging from 3.4 to 6.2 eV for GaN and AlN, respectively, a III-nitride alloy system offers unique opportunities in heterojunction design. GaN processes a high electron saturation velocity, a large breakdown field and excellent thermal stability, making it very suitable for use as a channel material in RF power transistors [3, 4, 11-13, 42]. The AlGaN/GaN-based HEMT is the most widely investigated and mature one. Fig. 1.2.6 shows the cross-sectional schematic and the energy-band profile of a typical $Al_xGa_{1-x}N$/GaN

HEMT. Because of the conduction band offsets, an electron potential well is formed at the hetero-interface between the AlGaN and GaN. The electrons are confined in this potential well to form a two-dimensional electron gas (2DEG) [1, 15]. As the electrons transport in a two-dimensional way, bulk scattering effects such as ionized impurity scattering are reduced, resulting in greatly improved electron mobility.

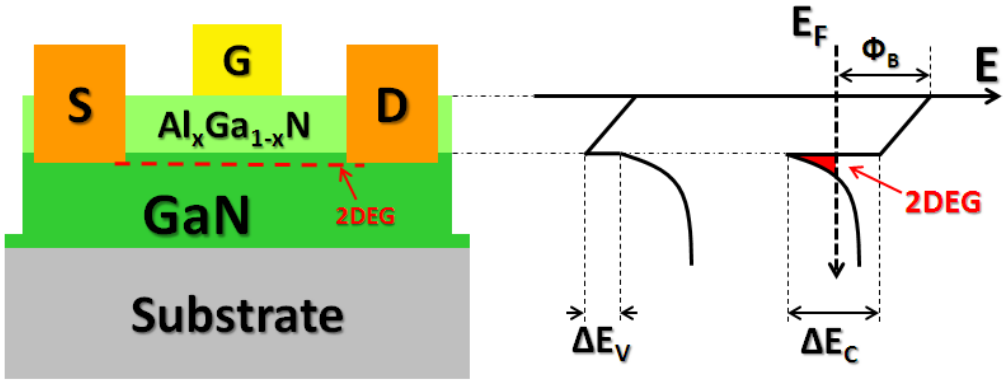

Figure 1.2.6 The cross-sectional schematic and the energy-band profile of a typical $Al_xGa_{1-x}N$/GaN HEMT.

Further contributing to the outstanding performance of AlGaN/GaN HEMTs is their ability to achieve a 2DEG with sheet carrier concentration of 10^{13} cm^{-2} or even higher without any intentional doping, well in excess of that achievable in the conventional III-V material systems. It has been proved that the formation of the high density 2DEG in AlGaN/GaN structures relies on strong spontaneous and piezoelectric polarization [18]. For the Ga-face AlGaN/GaN heterostructure grown by MOCVD, a thin AlGaN barrier layer on the GaN buffer layer experiences tensile strain caused by lattice mismatch. In the absence of external electric fields, the total macroscopic polarization (P) is the sum of the spontaneous polarization (P_{SP}) in the equilibrium lattice and the strain-induced or piezoelectric polarization (P_{PE}). The directions of the spontaneous and piezoelectric polarizations are both pointing towards the substrate, leading to a positive polarization induced charge density (+σ).

$$|\sigma(x)| = |P_{PE}(Al_XGa_{1-x}N) + P_{SP}(Al_XGa_{1-x}N) - P_{SP}(GaN)| \qquad (1.2)$$

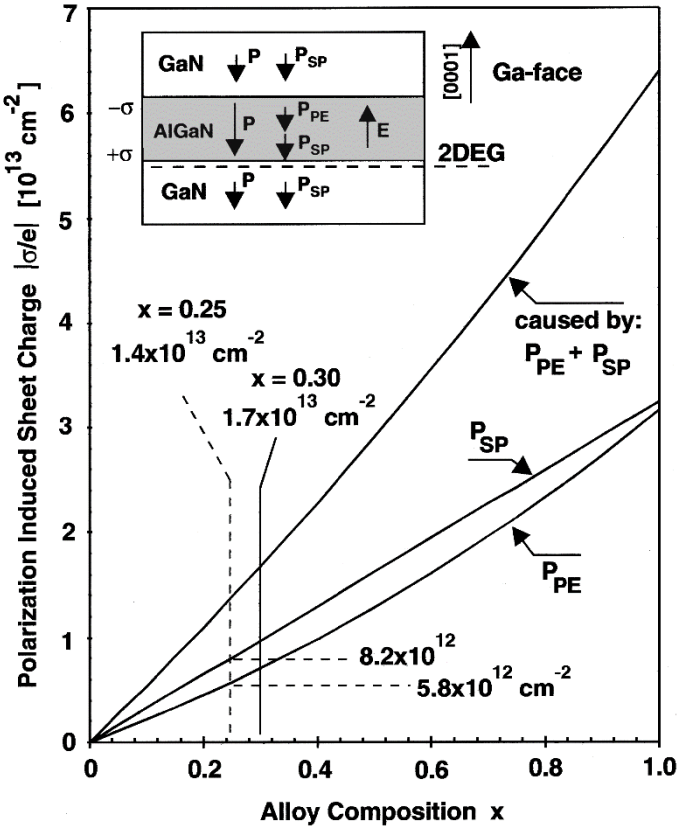

Figure 1.2.7 The calculated charge density at the $Al_xGa_{1-x}N$/GaN interface plotted versus the alloy composition [15].

Free electrons tend to compensate the positive polarization induced charge and form a 2DEG with a sheet carrier concentration (n_s), which is bound at the lower AlGaN/GaN interface for the Ga-face structures, as shown in the inset of Fig 1.2.7 [15].

$$n_s(x) = \frac{+\sigma}{e} - \left(\frac{\varepsilon_0 \varepsilon_r(x)}{de^2}\right)[e\emptyset_b(x) + E_F(x) - \Delta E_C(x)] \qquad (1.3)$$

where e is the electron charge, ε_0 is the vacuum permittivity, ε_r is the relative dielectric constant of the $Al_xGa_{1-x}N$ layer, d is the thickness of the barrier layer, $\emptyset_b$ is the Schottky barrier height, E_F is the Fermi level with respect to the GaN conduction-band-edge energy, and ΔE_C is the conduction band offset at the AlGaN/GaN interface where a 2DEG forms.

By increasing the Al composition of the barrier, the piezoelectric and spontaneous polarizations are increasing, and likewise the polarization induced charge ($+\sigma$) and the sheet carrier concentration (n_s). In Fig 1.2.7, the charge density (σ/e) at the $Al_xGa_{1-x}N$/GaN interface caused by the spontaneous and piezoelectric polarizations is plotted versus the alloy

composition.

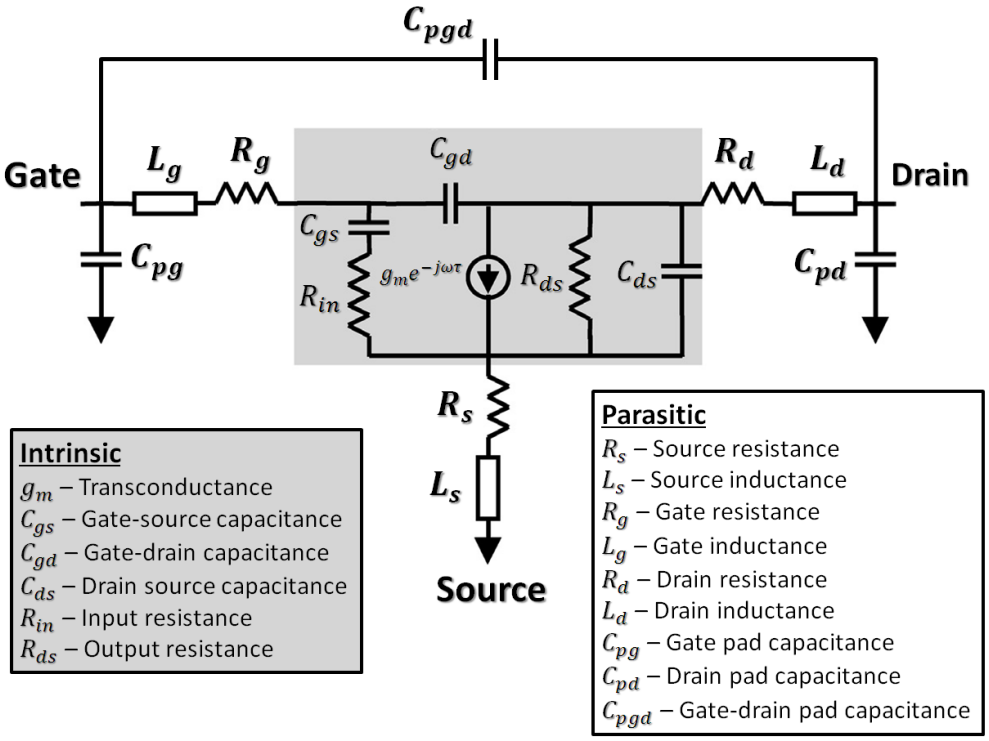

Figure 1.2.8 The 15-element small signal equivalent circuit model for a HEMT [43].

As shown in Fig. 1.2.6, a HEMT is formed by placing one Schottky contact as the gate electrode and two Ohmic contacts as the source/drain (S/D) electrodes on top of an AlGaN/GaN heterostructure. The 2DEG sheet carrier concentration within the heterojunction channel and therefore the drain current of the HEMT can be controlled or modulated by applying an appropriate bias voltage on the Schottky barrier gate. In order to design an RF or microwave HEMT device, it is crucial to understand the principles of device operation and to take into consideration the effect of parasitic components. Fig. 1.2.8 shows the most popular 15-element small signal equivalent circuit model for a HEMT [43]. The grey box highlights the intrinsic device elements, which include the intrinsic transconductance (g_m), the gate-source and gate-drain capacitance (C_{gs} and C_{gd}), the drain-source coupling capacitance (C_{ds}), the charging resistance (R_{in}) and the output resistance (R_{ds}). The τ, in the expression of $g_m(\omega) = g_m \cdot e^{-j\omega\tau}$, is the time delay it takes for the channel depletion region to respond to the gate signal. The parasitic elements include the pad capacitances C_{pg}, C_{pd} and C_{pgd},

the pad inductances L_g, L_d, and L_s, and the gate and series S/D resistances R_g, R_s, and R_d. The physical origins of these equivalent circuit elements are illustrated in Fig. 1.2.9 [44]. The intrinsic elements are a function of the direct current (DC) bias, while the parasitic ones are bias independent. The equivalent circuit elements, which are usually extracted from the devices' microwave S-parameter measurements, can be used to analyze and predict the RF performance of a HEMT.

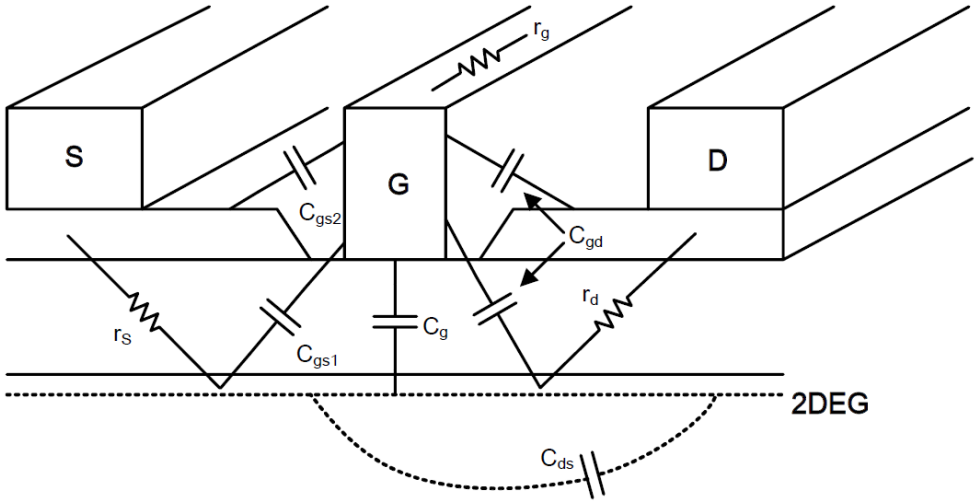

Figure 1.2.9 The physical origins of the elements in an equivalent circuit model [44].

The g_m is the measure of the devices' intrinsic gain, representing the effectiveness of the gate in modulating the drain current. When taking into account the parasitic components, such as R_s, the extrinsic transconductance (G_m) can be described as

$$G_m = \frac{g_m}{1+g_m \cdot R_s} \tag{1.4}$$

The current gain cut-off frequency (f_T) and the maximum oscillation frequency (f_{max}) are two figures of merit (*FoM*s) for the high frequency performance of a HEMT. The f_T is the frequency at which the short circuit current gain ($|h_{21}|^2$) of the device falls to unity. In the first order approximation, the equation below gives the definition of f_T:

$$f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})} \tag{1.5}$$

In general, a device with a high f_T value will function usefully at a higher frequency than a

device with a lower f_T value. A high f_T can be achieved by increasing g_m and reducing C_{gs} and C_{gd} of the HEMT. Considering the physical mechanism of a HEMT operation, f_T can also be represented by the channel electron drift velocity through the following equation:

$$f_T = \frac{v_{sat}}{2\pi L_G} \tag{1.6}$$

where v_{sat} is the saturation electron drift velocity and L_G is the gate (channel) length (L_G). It is apparent that a higher electron saturation velocity and smaller L_G in higher f_T.

The f_{max} is the highest frequency at which power gain can be obtained from a device. This may be used as an indicator of the ultimate frequency limits of a device. For most RF/microwave applications, the f_{max} appears to be more useful than the f_T because microwave designers are typically concerned with power gain at matched conditions. The f_{max} is defined as the frequency at which the power gain of a device reaches unity, which can be expressed as:

$$f_{max} = \frac{f_T}{\sqrt{\frac{4}{R_{ds}}\left(R_{in}+\frac{R_S+R_g}{1+g_m R_S}\right)+\frac{4C_{gd}}{5C_{gs}}\left(1+\frac{2.5C_{gd}}{C_{gs}}\right)(1+g_m R_S)^2}} \tag{1.7}$$

A simple form of the equitation can be written as:

$$f_{max} = \frac{f_T}{2}\sqrt{\frac{R_{ds}}{R_g+R_{in}}} \tag{1.8}$$

Apparently, to maximize the f_{max}, the f_T and the resistance ratio $\frac{R_{ds}}{R_g+R_{in}}$ of the HEMT have to be optimized.

1.3 Contributions and Organization of Thesis

Electronic sensing and RF-communication systems have dramatically changed our daily lives since 1947, when the first transistor was invented. Advanced semiconductor devices are the key components within these systems and ultimately determine their performances. In this never ending challenge, GaN-based semiconductors and heterostructure devices are unique

contenders for future leading-edge electronic systems due to their outstanding material properties with respect to speed, power, efficiency, linearity, and robustness. Therefore, it is essential and meaningful to develop novel GaN-based devices and circuits for next-generation sensing and RF-communication applications.

This thesis aims at the exploration and design of such devices and monolithic integration technologies for GaN-based sensors and RF/microwave power electronics. The work can be divided into sensors and high-frequency power devices.

For the sensors, Lamb-wave and SAW delay line devices and their monolithically integrated oscillators were designed and fabricated with MOCVD-grown GaN-based thin films on silicon substrates. The Lamb-wave sensors were firstly improved by optimizing the device geometries. Then the Lamb-wave and SAW delay line devices were integrated with AlGaN/GaN HEMT circuits to form monolithic oscillators. After that, the temperature effects and power handling capabilities were investigated for the discrete and integrated devices. These integrated oscillators are reported up-to-date.

For the high frequency power devices, innovative device scaling technologies were implemented to boost the device performance of the GaN-based HEMTs. A gate-last self-aligned process was first developed by employing S/D regrowth and low-k benzocyclobutene (BCB) planarization techniques, which enabled the reduction of access resistance and parasitic capacitance, minimizing the RC-related delay. A thin AlN barrier was then used to facilitate the device scaling, with increased gate control capabilities and maintaining high channel conductivity. *In-situ* SiN_x grown by MOCVD was investigated as gate dielectric for the AlN/GaN MISHEMTs. The advantages of the *in-situ* SiN_x over other *ex-situ* deposited insulators includes better surface passivation effects, suppression of gate leakage current and the elimination of process- and growth- related defects.

Finally, high performance i*n-situ* SiN_x/AlN/GaN MISHEMTs were fabricated using the abovementioned techniques. The device with a L_G of 0.23 μm exhibited a maximum drain current density (I_{DS}) exceeding 1600 mA/mm, with a high on/off ratio (I_{on}/I_{off}) of over 10^7. The f_T and f_{max} were 55 and 86 GHz, respectively. Additionally, the effect of temperature on

both the DC and RF performances of the gate-last self-aligned MISHEMTs was studied from room temperature (RT) up to 550 K. The small signal equivalent circuit model of the fabricated MISHEMTs was also analyzed to provide insights into the role of various parameters in the device performance.

The rest of this dissertation is organized as follows:

Chapter 2 presents the design and fabrication of Lamb-wave and SAW delay line devices and their monolithic integrated oscillators using GaN-on-Si technology. After a review of prior works, Lamb-wave sensors with improved performance are demonstrated. The development of the monolithic acoustic wave oscillators is also discussed in detail.

Chapter 3 describes the development of a gate-last self-aligned technology for fabrication of AlGaN/GaN HEMTs. Regrown S/D Ohmic contactS, low-k BCB planarization and precisely defined gate-to-regrown-S/D distances (L_{GS}/L_{GD}) by the SiN_x sidewall spacers are key elements of the devices. The details of the fabrication processes and device characterizations are provided in this chapter.

Chapter 4 reports the investigation of an *in-situ* SiN_x gate dielectric grown on AlN/GaN heterostructures by MOCVD. Both material structural and electrical characterizations are performed to evaluate the performance of the *in-situ* SiN_x film as a gate insulator. The benefits of using *in-situ* SiN_x as gate dielectric, such as suppressed leakage current and a low interface trap state density, are presented.

In Chapter 5, high performance *in-situ* SiN_x/AlN/GaN MISHEMTs are demonstrated using the techniques and material structures developed in Chapter 3 and Chapter 4. The thermal evolution of the DC and RF performances of the fabricated devices and their small signal equivalent circuit modeling are discussed.

Chapter 6 summarizes the dissertation and suggests future research work.

CHAPTER 2 LAMB-WAVE SENSORS AND MONOLITHIC INTEGRATED ACOUSTIC WAVE OSCILLATORS USING GAN-ON-SI

2.1 Introduction

Acoustic wave technology has been used extensively in commercial applications such as telecommunications, automotives and environmental sensing, for several decades. Monolithic integration of acoustic wave devices with on-chip electronics yields a compact system-on-chip (SoC) solution, which has advantages in both detection and communication applications. The advantages include improved performance, increased yield, reduced packaging volume and lower overall cost.

With high acoustic wave velocity and a strong piezoelectric effect, GaN has been exploited for the fabrication of acoustoelectric devices such as filters and UV sensors [30-37]. Their inherent chemical inertness and bio-compatibility also make them attractive for biosensors [5, 38, 39]. Furthermore, GaN-based acoustic wave devices can be potentially integrated with a wide range of other well-developed GaN devices, such as HEMTs, LEDs, and power switches. The first demonstration of a monolithic integrated SAW oscillator on a GaAs substrate can be traced back to 1999 [45]. However, the integration of GaN-based electronics with acoustic functions is still limited and mostly at device level without proper circuit functions [46, 47], for example the integration of one acoustic wave filter with one HEMT for signal amplification.

Compared to their conventional counterparts, such as those based on silicon and GaAs technologies, circuits based on wide bandgap materials (GaN and SiC) offer superior performance under high-temperature environments. Smart sensors with integrated electronics that can operate at high ambient temperatures without external cooling can greatly benefit a variety of industrial applications, especially in automotive, aerospace and deep-well drilling systems [48]. For example, automobile engines and brake sensors are required to operate reliably at ambient temperatures above 150 ℃, telemetry during underground mining and oil

drilling requires sensors and electronics to handle up to 225 ℃, and aircraft engine intelligent control and structural health monitoring systems with various sensors need to function up to 500 ℃ and higher [49, 50]. In such applications, monolithic integration of the sensor circuits with wireless transceivers would greatly reduce the system form factor, weight, and complexity. An essential component in these wireless sensor systems with high-temperature tolerance is an RF local oscillator possessing low-temperate dependence and coefficients. The RF carrier signal will be modulated by the sensor signal and transmitted to the cooler part of the system.

Recently, there have been several reported results of hybrid oscillators based on SiC operating at high temperatures ranging from 200 ℃ to 475 ℃ [51-53]. These oscillators used Cree's SiC MESFETs mounted onto a substrate carrier. In addition, an NMOS SiC ring oscillator operating at 625 kHz under 300 ℃ [54] and a 66 MHz, 375 ℃ ring oscillator based on AlGaN/GaN HEMTs on a sapphire substrate [55] have been demonstrated. However, these oscillators suffered from a relatively large temperature drift with large temperature coefficient of frequency (TCF) in the order of 10^3 ppm/℃.

In this work, GaN-based Lamb-wave sensors were firstly improved by modifying the device geometries [56]. Then, monolithic integrated SAW and Lamb-wave oscillators [57, 58], which are suitable for sensing applications at high ambient temperature and can potentially be extended to high power RF systems, were developed.

2.2 Two generations of GaN-based Lamb-wave sensors

Nowadays, MOCVD technology is mature enough to allow versatile sensors to be fabricated with high-quality epitaxial GaN on silicon substrates, instead of on traditional sapphire or SiC substrates, whilst conventional Si-based semiconductor processing techniques can still be adopted. Recently, high performance Lamb-wave sensors have been developed using GaN-on-Si structures by both our group [39] and others [38] independently, with the former showing good mass sensitivity and the latter demonstrated for chemical and biological sensing.

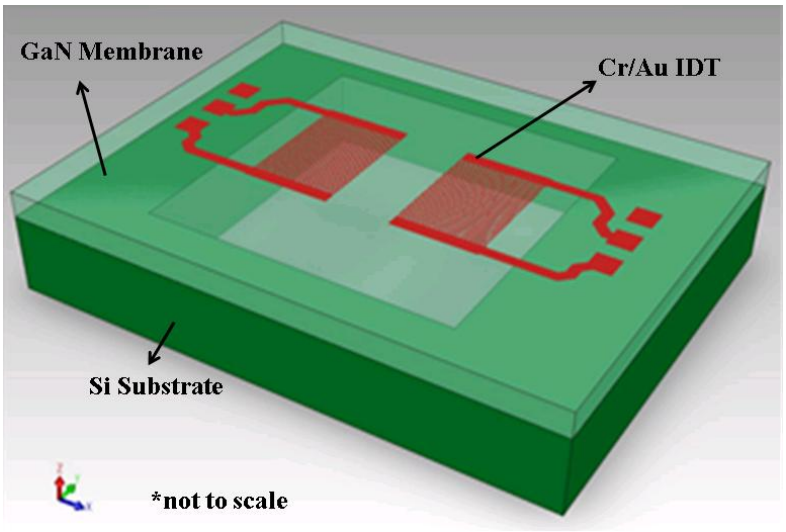

Figure 2.2.1 The schematic of the Lamb-wave sensor using a GaN-on-Si structure.

Fig. 2.2.1 shows a schematic of the sensor structure previously developed by our group, referred as first generation sensors (*G-I*) in this dissertation. The Lamb-wave sensors are of two-port delay line configurations formed by a 1-μm thick suspending GaN membrane with two Cr/Au top IDTs located near the edges of the back side cavity formed by local excavation of the silicon substrate.

Table 2-1 The design parameters of *G-I* and *G-II* sensors.

Design Parameters	*G-I*	*G-II*
IDT Period (λ)	16 μm	16 μm
Width of IDT Fingers	4 μm	4 μm
Number of Pairs in each IDT	15	20
IDT Aperture	400 μm	400 μm
Side to Side IDT Separation	240 μm (15 λ)	1440 μm (90 λ)
Thickness of the Membrane	1.085 μm	1.085 μm
Dimension of the Si Excavation	1.2 mm×1.2 mm	0.6 mm×2.2 mm

In this work, second generation sensors (*G-II*) with similar configurations to *G-I*, but different geometries, were designed. The design parameters of the *G-I* and *G-II* sensors are compared in Table 2-1. Optical micrographs of the fabricated sensors are shown in Fig. 2.2.2. The IDT electrodes that appear suspended in air are, in fact, mechanically supported by the transparent GaN membrane.

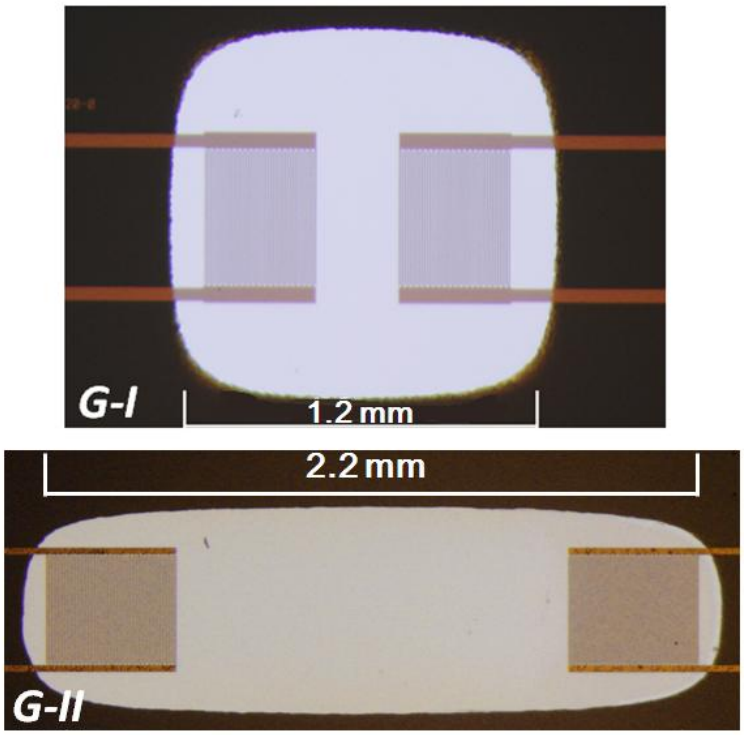

Figure 2.2.2 The optical micrographs of the fabricated *G-I* and *G-II* sensors.

There were four main processing steps in the fabrication of Lamb-wave sensors, as illustrated in Fig. 2.2.3. Firstly, a stack of GaN-based epitaxial layers was grown on a high-resistivity Si (111) substrate using an AIXTRON2000HT MOCVD system, as shown in Fig. 2.2.3(a). High-resistivity substrates were used to minimize electromagnetic feedthrough. The full epitaxial stack consisted of a 40 nm buffer layer and a 900 nm GaN layer. A 20 nm interlayer and a 125 nm AlGaN layer were inserted in the GaN layer to counter-balance the tensile strain produced by the mismatch of the thermal expansion between the substrate and the epi-layers and to prevent cracks on the surface. Secondly, the IDT electrodes were formed on top of the epi-layers by e-beam evaporation of Cr/Au (3 nm / 30 nm) and a liftoff process, as shown in Fig. 2.2.3(b). Thirdly, similar techniques to those in the second step were performed on the back side of the wafer to pattern a 300 nm thick Al etch mask for silicon substrate removal, as shown in Fig. 2.2.3(c). Finally, the silicon substrate was selectively removed by an SF_6-based inductively coupled plasma (ICP) etching process for releasing the membrane. The fabrication was completed by stripping away the Al mask with a hot H_3PO_4 solution. Fig. 2.2.3(d) is a cross-sectional view of the finished device.

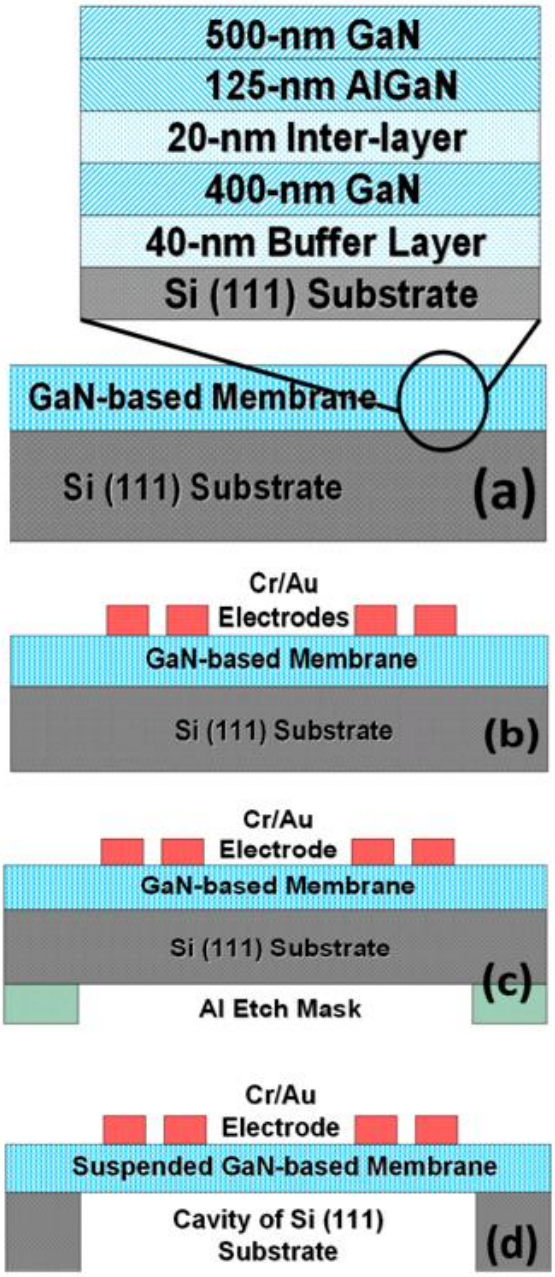

Figure 2.2.3 The fabrication process of the Lamb-wave sensors.

The fabricated sensors were characterized using an RF-probe station, a pair of RF-probes, and an Agilent Vector Network Analyzer. Short-Open-Load-Through (SOLT) calibration was performed prior to taking measurements, and no de-embedding was carried out. All the measurements were conducted with 50-Ω termination impedance. The magnitude of the S_{21} Parameters from 300 kHz to 600 MHz of the unloaded *G-I* and *G-II* sensors are shown in Fig. 2.2.4. The peak is observed at around 473 MHz, which indicates the propagation of the lowest order symmetric mode (S_0) wave. The corresponding phase velocity is ~7580m/s for the 16

μm wavelength and the 1.085 μm thick GaN-based membrane. This is in agreement with the reported value in the literature [38]. The lowest order anti-symmetric mode (A_0) wave, appearing at around 50 MHz, is much weaker than the S_0 wave. This suggests a weak electroacoustic coupling and a high noise level near the lower frequency A_0 peak.

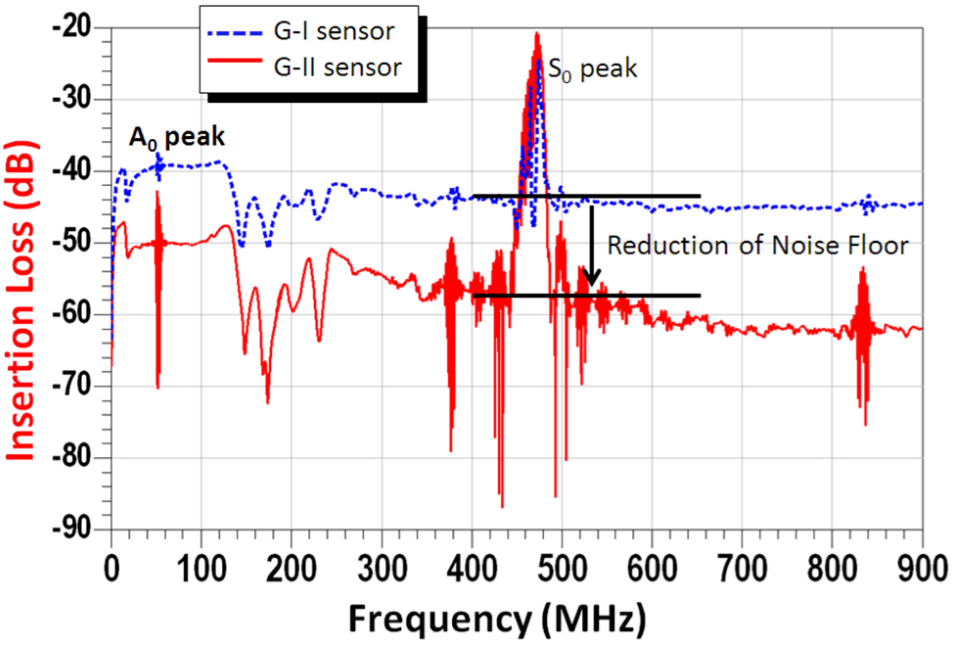

Figure 2.2.4 The magnitude of the S_{21} Parameter of the unloaded *G-I* and *G-II* sensors.

There are three different design parameters between the two generations of sensors: the number of pairs in each IDT, the separation between two IDTs, and the dimension of the silicon excavation, as listed in Table 2.2.1.

Firstly, the signal strength of the S_0 wave in the *G-II* sensors is -20 dB, approximately 4 dB higher than that of the *G-I* sensors. This can be explained by the increased number of IDT pairs (from 15 to 20), which results in a stronger electroacoustic coupling in the *G-II* sensors, that is more than needed for compensating for the attenuation induced by a longer acoustic path length.

Secondly, the noise floor around the S_0 peak is considerably lower, by more than 10 dB in the *G-II* sensors, compared with that of the *G-I* sensors. Other weak acoustic modes, such as the shear horizontal acoustic plate mode (SH-APM), can also be observed in Fig. 2.2.4, but they are out of the scope of this dissertation. The lower noise floor in the *G-II* sensors is a

result of the significantly increased IDT separation from 15 λ to 90 λ.

Thirdly, the *G-II* sensors have a smaller area of silicon excavation (1.32 mm^2) than that of the *G-I* sensors (1.44 mm^2). This indicates that the performance improvements do not come at the expense of device size. As well, an improvement of fabrication yield and mechanical robustness in wafer handling was realized due to the reduction of the suspended membrane width from 1.2 mm down to 0.6 mm.

The mass sensitivities of the sensors were evaluated by loading or depositing different thicknesses of SiO_2 on the back side of the membranes using plasma-enhanced chemical vapor deposition (PECVD). The shift of resonant frequency, due to the mass-loading effect in the acoustic wave propagation path, was recorded by measuring the S_{21} Parameters after each successive deposition. The linear relationships of the resonant frequency versus the thicknesses of deposited SiO_2 for the *G-I* and *G-II* sensors are derived in Fig 2.2.5, with the correlation coefficients (R^2) of 0.95834 and 0.99812, respectively. The absolute mass sensitivity in terms of frequency shift (S_{mf}) is defined as

$$S_{mf} = \frac{\Delta f}{\Delta m} \tag{2.1}$$

where Δf is the shifts of the resonant frequency produced by mass loading on the sensor surface. Δm is the loaded mass per unit area. Since

$$\Delta \mathrm{m} = \rho \times \Delta \mathrm{d} \tag{2.2}$$

where ρ and $\Delta \mathrm{d}$ are the density of the loaded material (2.3 g/cm^3 for PECVD SiO_2 [59]) and the change of thickness, respectively,

$$S_{mf} = \frac{\Delta f}{\Delta d} \cdot \frac{1}{\rho} \tag{2.3}$$

where $\frac{\Delta f}{\Delta d}$ is the gradient of the linear fit in the graph. The normalized mass sensitivity in terms of frequency shift is defined as the absolute mass sensitivity divided by unloaded resonant frequency, which is 473 MHz in this case. The *G-II* sensors exhibit 1.6 times higher sensitivity (272 cm^2/g vs.174 cm^2/g) and better linearity than the *G-I* sensors. This can be

explained by the improved signal strength and the lower noise level in the *G-II* sensors, as shown in Fig. 2.2.4. The larger signal to noise ratio (SNR) results in a smaller minimum distinguishable frequency shift and a more accurate measurement, i.e., a higher sensitivity.

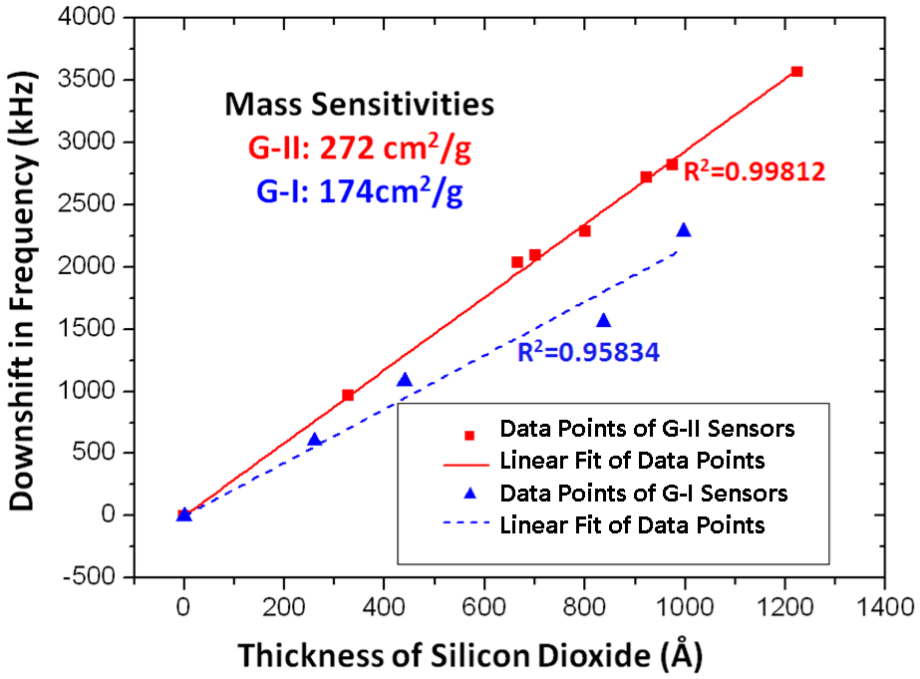

Figure 2.2.5 The linear relationships of the frequency versus the thicknesses of deposited SiO_2 for the *G-I* and *G-II* sensors.

2.3 Monolithic integrated acoustic wave oscillators

2.3.1 Integration consideration

In this work, fully integrated acoustic wave oscillators were developed using an AlGaN/GaN-on-Si platform for the first time. The oscillator prototype was implemented by monolithically integrating a SAW or a Lamb-wave two-port delay line device with electronics using AlGaN/GaN HEMTs.

The piezoelectric material that couples between the strain and electric fields provides a convenient medium to launch acoustic waves using IDTs, as described previously. To launch acoustic waves, an RF electrical signal is applied on an IDT to create elastic deformation in a piezoelectric material. However, the presence of a 2DEG in the AlGaN/GaN heterojunction channel screens the applied electric field and prohibits the acoustoelectric transductions in the

IDTs [35, 46]. Our solution to this problem is to locally dry-etch away the top AlGaN barrier layer and fabricate the acoustic wave devices on the exposed GaN surface, while the active HEMTs are fabricated on the mesa where the AlGaN barrier layer remains.

2.3.2 Delay line oscillator design and fabrication

An acoustic wave oscillator consists of an amplifier configured in a feedback loop with an acoustic wave delay line device. The amplifier must provide sufficient gain at a desired oscillation frequency to compensate for the insertion loss of the acoustic wave device. In this work, a five-stage HEMT amplifier was designed with a gain of over 40 dB and each stage was an active-load common-source amplifier, as shown in Fig. 2.3.1. All HEMTs in the circuit are in depletion-mode (D-mode). Active load is formed by connecting the gate and source of a D-mode transistor together so that the transistor is biased at the on-state all the time. A total of 12 HEMTs are used in this design, including two source-follower buffers. The L_G of all the HEMTs is 1.5 μm and the gate-to-source distance (L_{GS}) and gate-to-drain distance (L_{GD}) are both 1 μm. Passive elements, including metal-insulator-metal (MIM) capacitors and mesa resistors, are fabricated on the same chip. On-chip bypass capacitors are also included for the gate (V_g) and drain (V_d) supplies, which are not shown in the schematic.

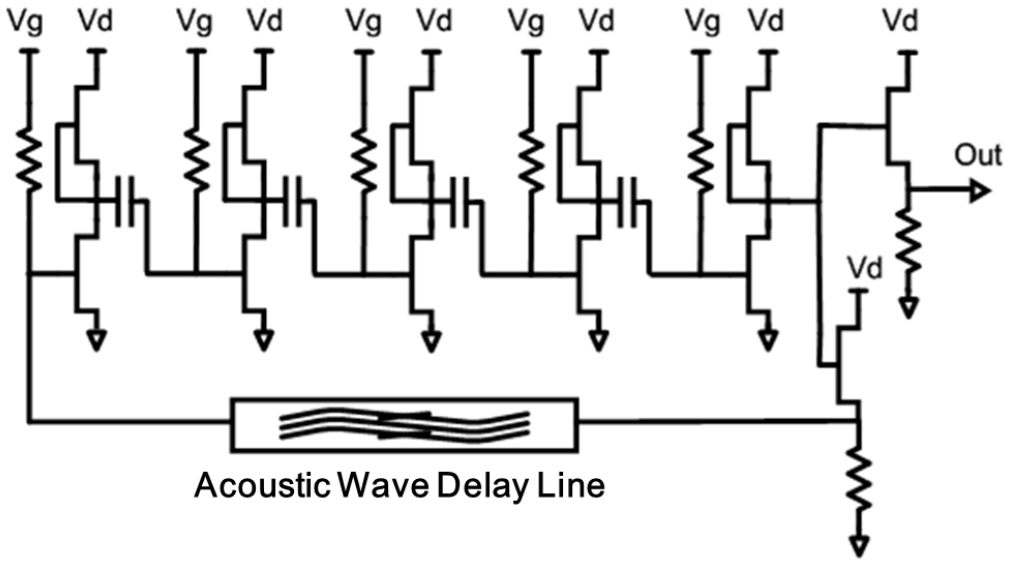

Figure 2.3.1 The schematic of the integrated oscillator circuit.

The operation frequency of an acoustic wave delay line oscillator is determined by the acoustic velocity, the wavelength (λ) and the path length between the two IDTs. In this study, the IDT finger width and the spacing between two adjacent IDT fingers are both 4 μm, resulting in a λ of 16 μm. Both the input and output IDTs have 50 pairs of fingers. The electrode separation of the two IDTs is 480 μm, 30 times longer than the wavelength, and the IDT aperture is 300 μm.

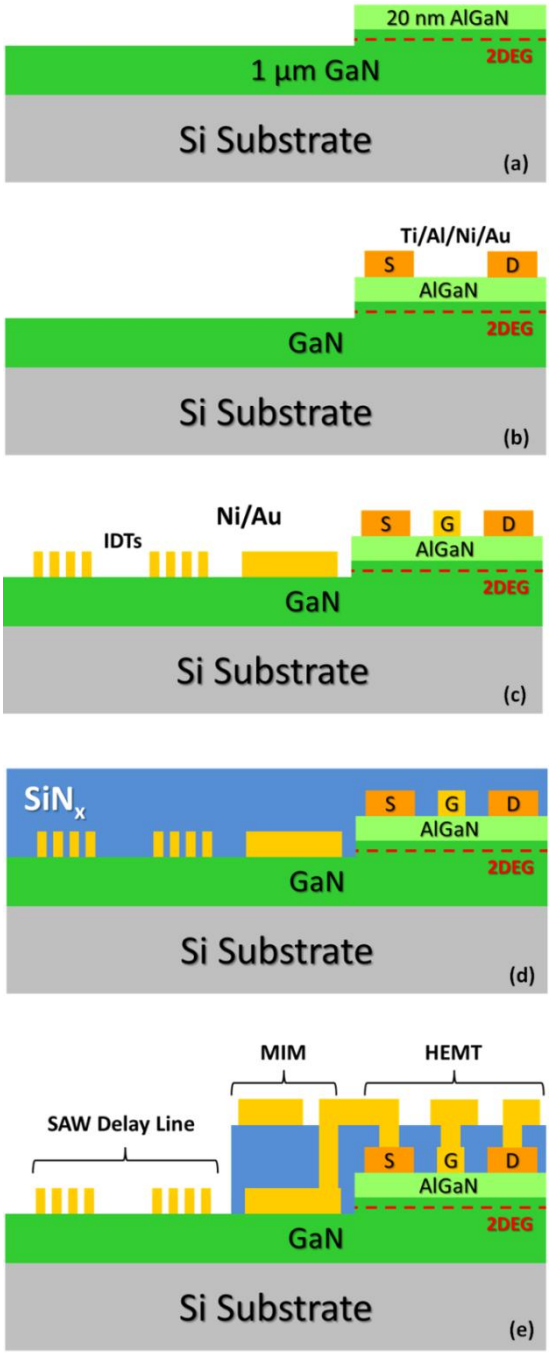

Figure 2.3.2 The fabrication process of the integrated SAW oscillator.

The AlGaN/GaN heterostructures used in this work were grown on a silicon substrate using an AIXTRON2000HT MOCVD system. The structure consisted of a high temperature AlN seed layer, a SiN_x mask layer, a 1 μm thick GaN buffer layer and a 20 nm thick AlGaN barrier layer. The fabrication process was modified from a conventional AlGaN/GaN HEMT process flow [4] [55], as illustrated in Fig. 2.3.2. Firstly, the top AlGaN barrier layer was selectively etched away by Cl_2-based ICP etching for not only isolating the active devices, but also removing the 2DEG within the heterojunction channel for acoustoelectric transduction in the IDTs, as shown in Fig. 2.3.2(a). Secondly, the S/D Ohmic contacts of the HEMTs were formed by e-beam evaporation of Ti/Al/Ni/Au and a liftoff process, followed by rapid thermal annealing (RTA) at 850 ℃ for 30 seconds, as shown in Fig. 2.3.2(b). Thirdly, the Schottky metal for forming the IDTs of the acoustic wave device, gate electrodes of the HEMTs and the bottom metal plates of the MIM capacitors was patterned by e-beam evaporation of Ni/Au and a liftoff process, as shown in Fig. 2.3.2(c). Then, a 2000 Å silicon nitride layer was deposited by PECVD, serving as both the interlevel dielectric and MIM capacitor dielectric, as shown in Fig. 2.3.2 (d). After that, reactive ion etching (RIE) was used for via opening, and the whole processing for an SAW oscillator was completed with the formation of interconnection, as shown in Fig. 2.3.2(e). An optical micrograph of the fabricated circuit is given in Fig. 2.3.3 and a one-stage active-load amplifier is shown in detail. The oscillator circuit size is approximately $2 \times 1.2\ mm^2$.

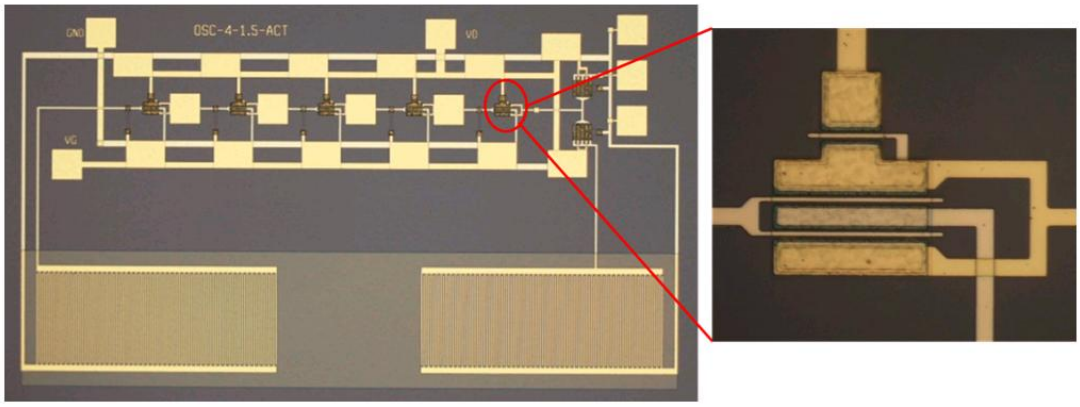

Figure 2.3.3 The optical micrograph of a fabricated SAW oscillator.

For the Lamb-wave oscillator, similar techniques as described previously for the

Lamb-wave sensor fabrication were added to selectively remove the Si substrate from the back side and release the Lamb-wave device membrane. Firstly, a 300 nm thick Al etch mask was patterned on the back side of the wafer. Then the Si substrate was selectively removed by an SF_6-based ICP etching process. The fabrication was completed by stripping away the Al mask with a hot H_3PO_4 solution. Fig. 2.3.4(a) shows a cross-sectional schematic of the Lamb-wave oscillator. An optical micrograph of a fabricated circuit is given in Fig. 2.3.4(b).

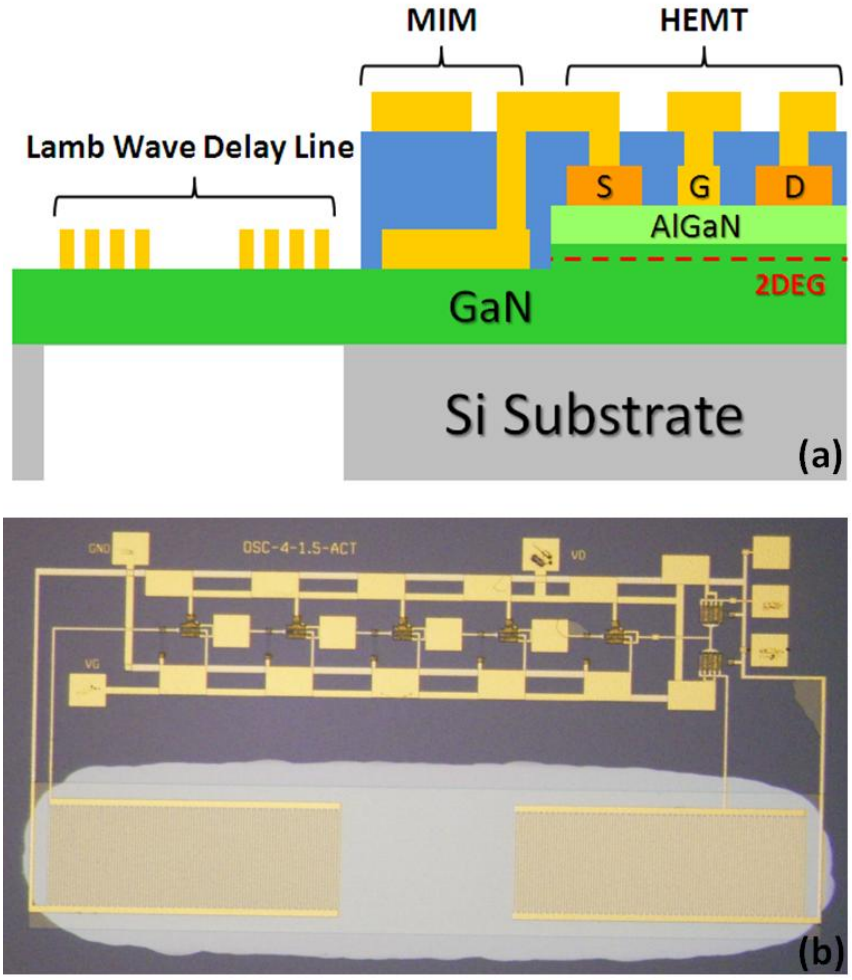

Figure 2.3.4 The cross-sectional schematic (a) and the optical micrograph (b) of the Lamb-wave oscillator.

2.3.3 Device characterization and discussion

On-wafer characterization of the devices and circuits was performed from RT to 250 ℃. A high-temperature probe station with a thermal controller to adjust and keep the temperature

constant was used. The measurements were carried out in air ambient. Before each measurement, the temperature was held constant for 5 minutes to assure thermal equilibrium was reached.

A. SAW Delay Line Characterization

The S_{21} Parameter between 100 and 600 MHz of the SAW device at RT was measured. The magnitude of S_{21} Parameter of the SAW delay line is shown in Fig. 2.3.5. A sharp peak is clearly observed at 252.3 MHz, which indicates the propagation of the Rayleigh waves. The SAW velocity was calculated to be 4037 m/s, in agreement with the values in the literature [1]. The measured insertion loss at the operation frequency is 28.2 dB, and the quality factor (*Q*) is approximately 1000. Low insertion loss and high-*Q* are both desirable for frequency-selective components in high performance oscillator systems. Another peak with lower *Q* at around 500 MHz is believed to be another mode of acoustic waves propagating through the multilayers structure.

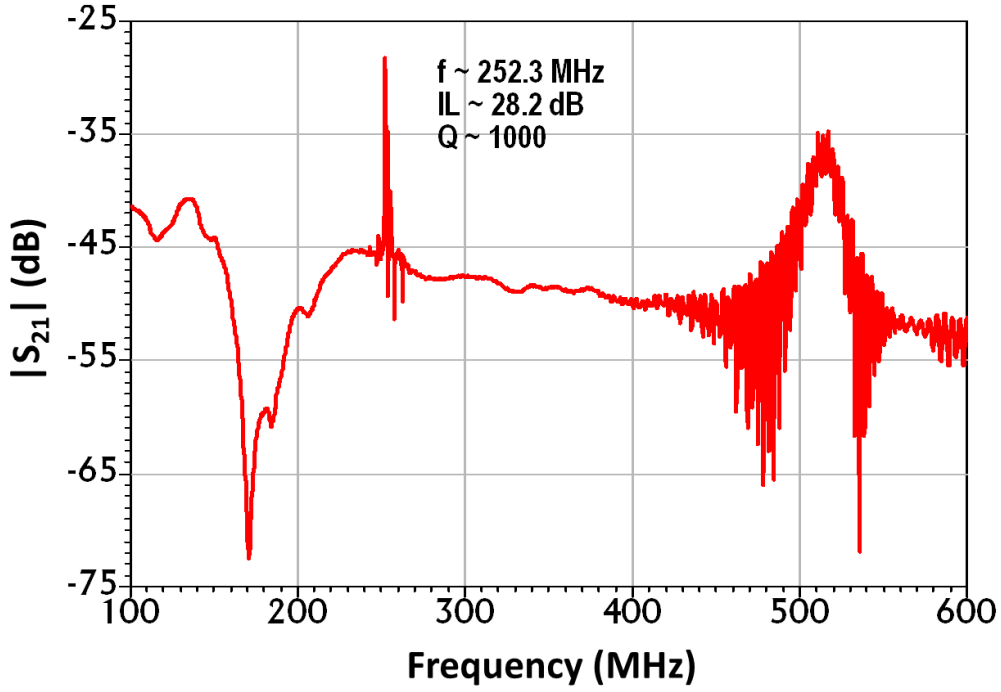

Figure 2.3.5 The magnitude of the S_{21} Parameter of the SAW delay line device.

The power handling capability of the SAW device was also assessed by configuring a discrete sustaining power amplifier along with the SAW device into an oscillator loop and

measuring its incident power level [60], as shown in Fig. 2.3.6. The SAW device was kept running at an input power level of 28 dBm (630 mW). No measurable performance degradation was observed after the power handling test, indicating that the SAW device is able to tolerate even greater input power levels. The excellent power handling capability highlights the potential of the GaN-based SAW oscillators for RF/microwave power applications.

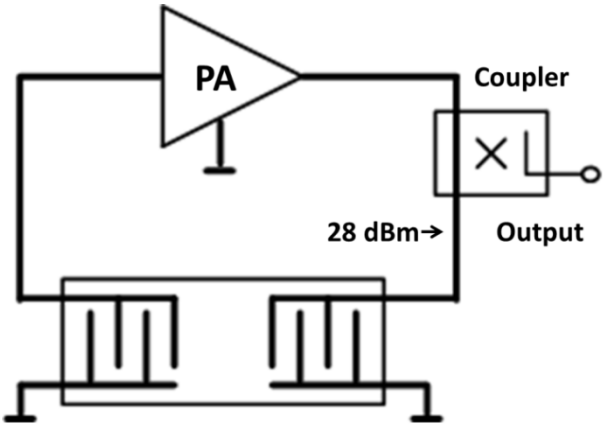

Figure 2.3.6 The schematic showing the power handling test setup.

B. Lamb-wave Delay Line Characterization

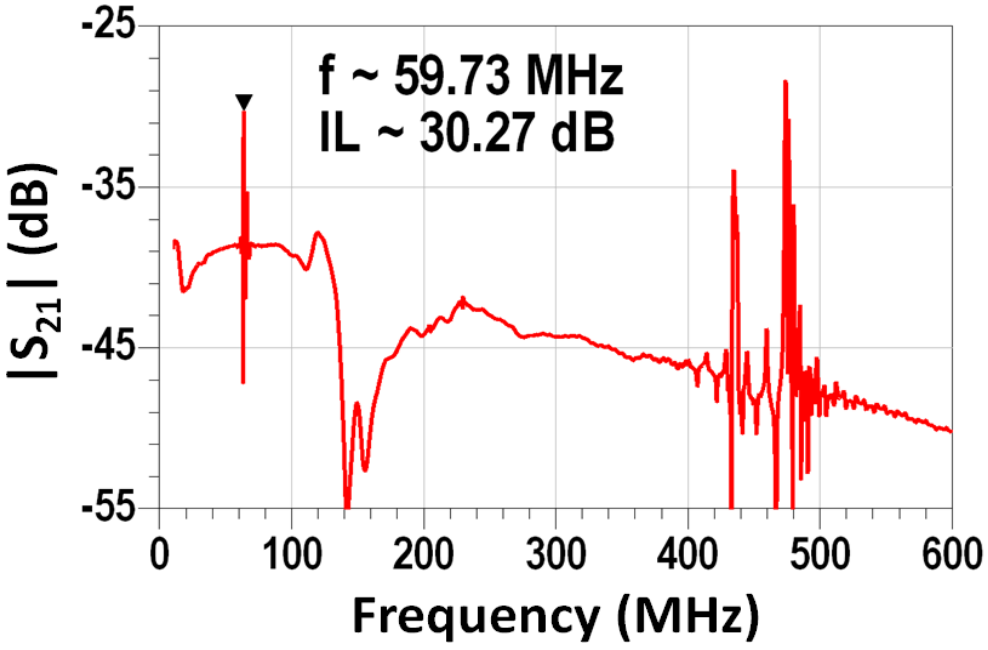

Figure 2.3.7 The magnitude of the S_{21} Parameter of a Lamb-wave delay line device.

The magnitude of S_{21} Parameter from 10 to 600 MHz for a Lamb-wave delay line in RT is plotted in Fig. 2.3.7. A sharp peak is clearly observed at 59.73 MHz with an insertion loss of 30.27 dB, which indicates the propagation of the A_0 mode wave. The corresponding phase velocity is ~956 m/s for the 16 μm wavelength and the 1 μm thick GaN-based membrane. This is in agreement with results using the numerical calculation suggested in [61]. The two other peaks, at 435 and 474 MHz, are believed to be the shear horizontal acoustic plate mode (SH-APM) and S_0 mode waves, respectively.

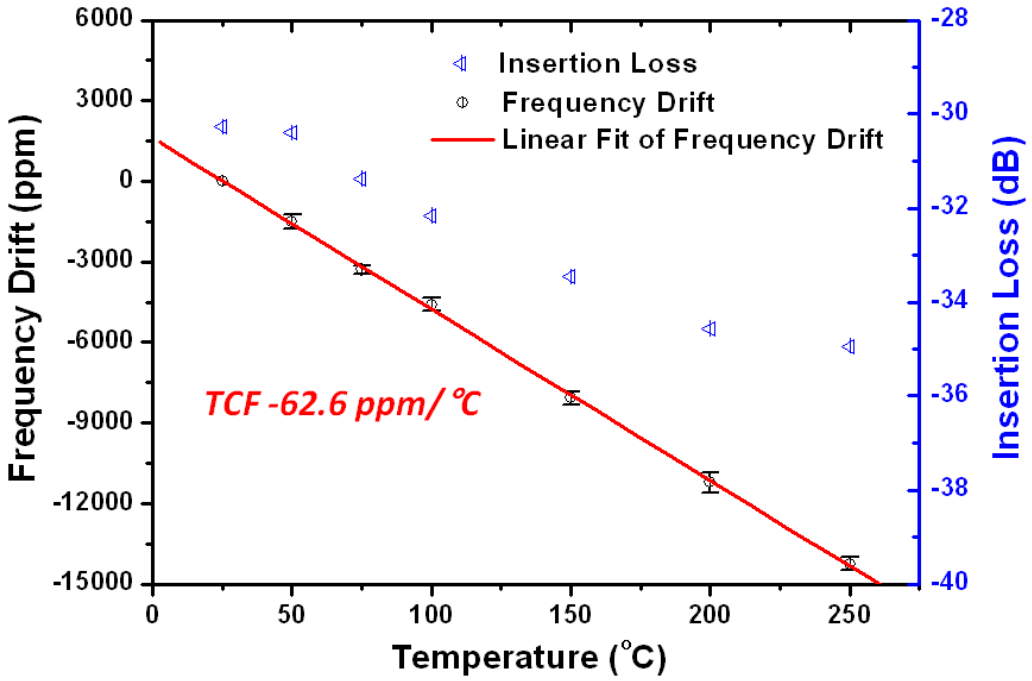

Figure 2.3.8 The temperature dependence of the A_0 wave peak frequency and insertion loss at the peak frequency.

The peak frequency drift and insertion loss of the A_0 wave are plotted as a function of temperature in Fig. 2.3.8. The peak frequency moves linearly with the temperature at a rate of 62.6 ppm/℃ and the insertion loss drops to 34.94 dB at 250 ℃. Three devices in the same wafer were measured and the fluctuations of the frequency drift were very small, within 380 ppm, as shown by the I-shaped error bars in Fig. 2.3.8. Given the different device configurations, the TCF of this GaN delay line device was somewhat larger than the reported value (~-28 ppm/℃) of one-port AlN Lamb-wave resonators [62, 63]. However, a similar temperature-compensation technique, i.e., using SiO_2, can be implemented in this GaN

Lamb-wave device as well to further improve the thermal stability. To our knowledge, this is the first reported high-temperature characterization for a GaN-based Lamb-wave device.

C. AlGaN/GaN HEMT DC Performance

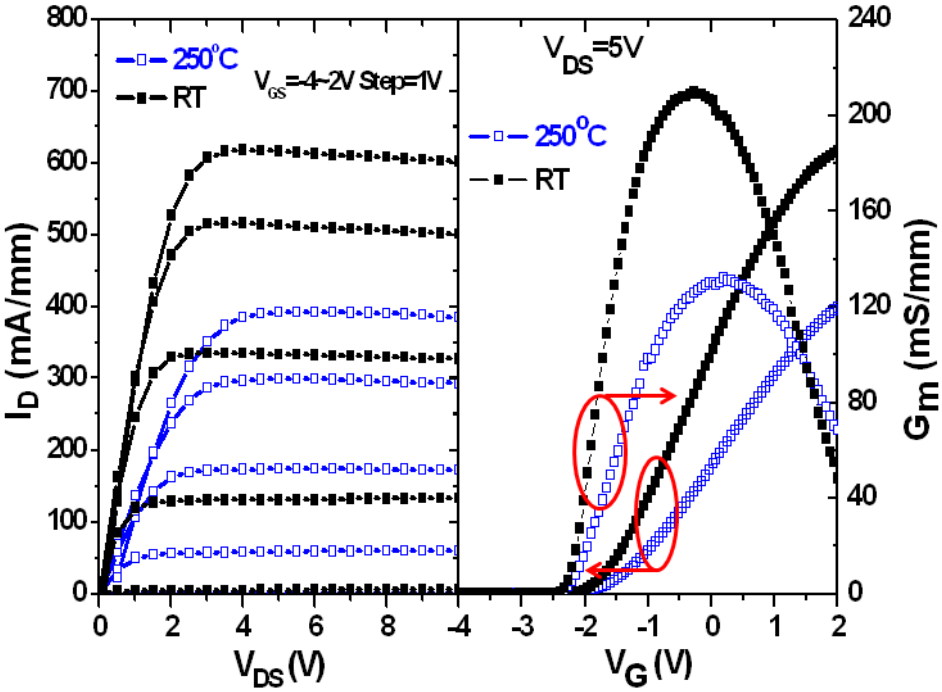

Figure 2.3.9 The DC characteristics of a fabricated AlGaN/GaN HEMT.

The measured typical DC characteristics of a fabricated D-mode HEMT are shown in Fig. 2.3.9. The device features a low DC output conductance and a peak G_m of 210 mS/mm with a threshold voltage (V_{th}) of 2.1 V at RT. The maximum drain current density (I_D) is 620 mA/mm. Good uniformity of HEMT performance over the whole wafer is achieved. The devices in the amplifier path were sized to provide sufficient gain to satisfy the requirement for starting up the oscillation, even at high temperature. At 250 ℃, the peak G_m and I_D decrease to 132 mS/mm and 400 mA/mm, respectively, which sets the required device width to be 100 μm.

D. Measured Oscillators Performances

The integrated SAW oscillator was tested on-wafer using a spectrum analyzer, with a V_d of approximately 10 V and a V_g of approximately 1.4 V. The oscillator operates at 252.7 MHz, which matches well with the SAW device characteristics, as shown in Fig. 2.3.10.

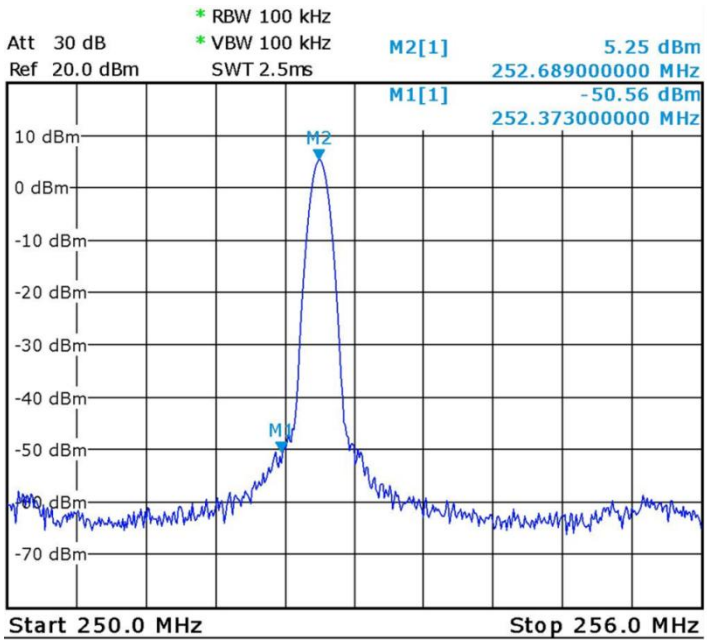

Figure 2.3.10 The measured frequency spectrum of the integrated SAW oscillator operating at RT.

The SAW oscillator phase noise was estimated from the measured frequency spectrum. At 300-kHz offset frequency, the phase noise was approximately 105 dBc/Hz. In theory, the phase noise performance should be much better with such a high-*Q* SAW device as the frequency selective feedback path. Thus, it is reasonable to believe that the HEMT electronics are the dominating noise source. Furthermore, the impedances between the SAW device and the electronic circuits were not well matched, which results in high insertion loss. Since this was the first demonstration, we believe the compromised phase noise performance was mainly caused by the high insertion loss as well as the yet to be perfected material and device fabrication techniques. The phase noise performance could be significantly improved if the SAW delay line device was properly impedance matched with the electronic circuits and by further optimizing the material quality, the process as well as the circuit configuration. In addition, this oscillator design was chosen mainly for its simplicity to demonstrate the feasibility of monolithic integration and is not an optimized circuit for phase-noise performance. To further improve the phase noise, the amplifier configuration needs to be modified to a more complex topology.

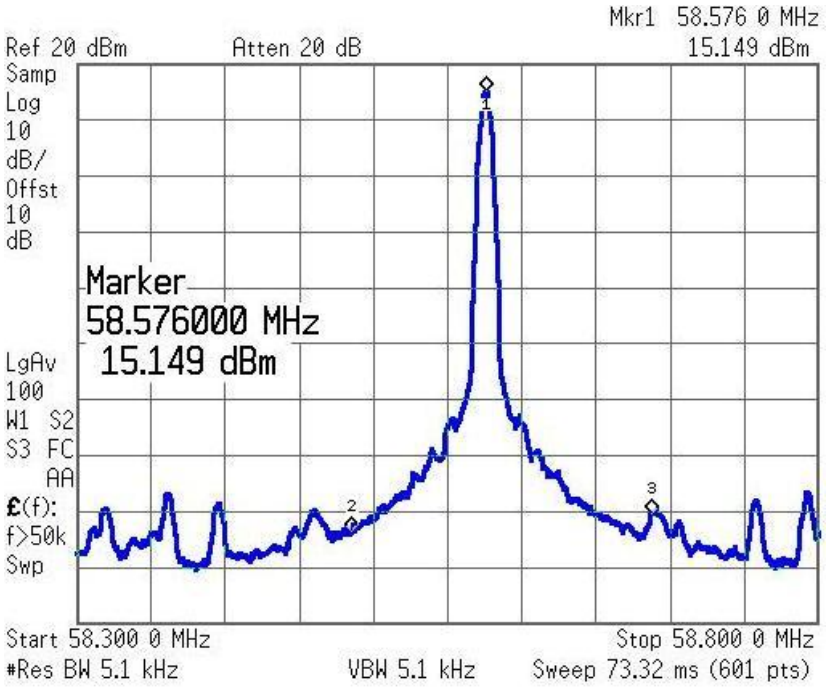

Figure 2.3.11 The measured frequency spectrum of the integrated Lamb-wave oscillator operating at RT.

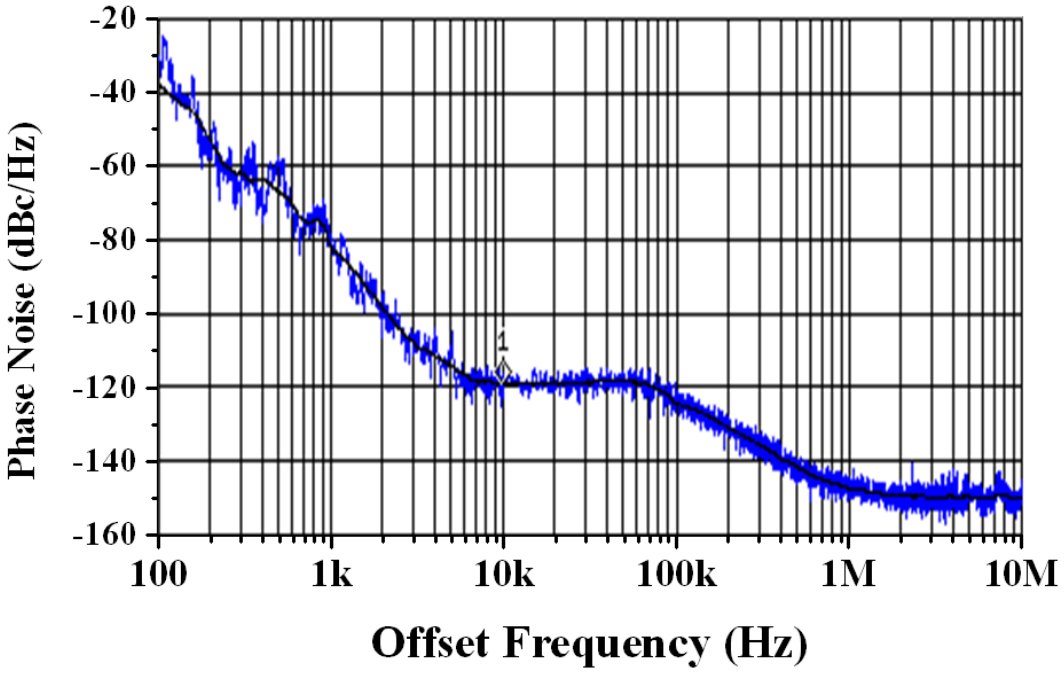

Figure 2.3.12 The measured phase noise of the integrated Lamb-wave oscillator operating at RT.

The integrated Lamb-wave oscillator oscillates at 58.58 MHz and produces an output power of 15.15 dBm at RT, as shown in Fig. 2.3.11, which matches well with the Lamb-wave

delay line device characteristic. As shown in Fig. 2.3.12, the measured phase noise of this 58-MHz oscillator at RT is -83 dBc/Hz at 1-kHz offset frequency and the phase noise floor is as low as -148 dBc/Hz.

Figure 2.3.13 illustrates the dependence of the Lamb-wave oscillation frequency and the output power on temperature. Over the temperature range from RT to 230 ℃ and with a fixed bias condition, the oscillation frequency decreases linearly from 58.576 to 58.0 MHz, which is less than 1%. The TCF of the Lamb-wave oscillator is 47.5 ppm/℃, which is lower than the temperature dependence for the stand alone Lamb-wave delay line. This enhancement in TCF can be attributed to the feedback mechanism and the temperature dependence of the amplifier. By adjusting the gate bias, oscillation up to 250 ℃ (our measurement limit) was observable, with an output power of 11.3 dBm.

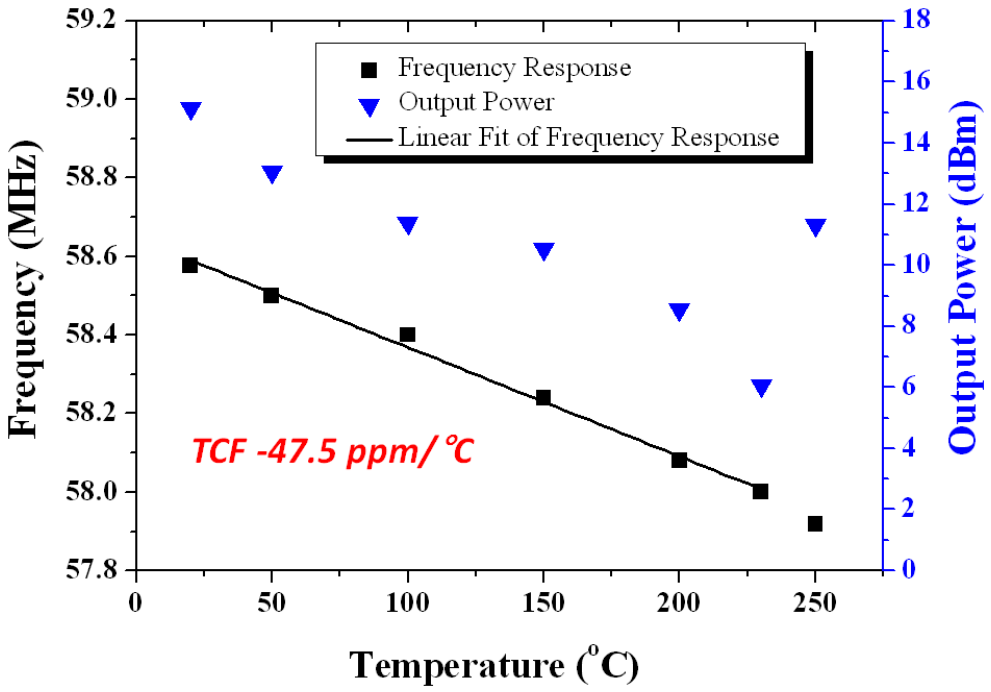

Figure 2.3.13 The temperature dependence of the oscillation frequency and output power of the Lamb-wave oscillator.

The performance of this Lamb-wave oscillator is limited by both the increasing loss in the lamb-wave device and the decreasing gain in the HEMT amplifier at high temperatures. By optimizing the Lamb-wave device and designing a higher gain amplifier, or with better heat dissipation, the temperature performance could be further improved.

The results in this study demonstrate, for the first time, the viability of integrated acoustic wave oscillators on a GaN-on-Si platform. AlGaN/GaN HEMTs are inherently suitable for high frequency operation. In this design, the oscillation frequency can be proportionally increased by down scaling the IDT features of the acoustic wave devices. Higher frequency leads to wider-bandwidth higher-speed communication applications and greater-sensitivity detection applications.

2.4 Summary

In this study, GaN-based Lamb-wave sensors were improved by modifying the device geometries. The improved sensors exhibit a 1.6 times higher sensitivity and better linearity.

For the first time, monolithically integrated SAW and Lamb-wave oscillators have been realized experimentally using AlGaN/GaN directly grown on Si substrates. The SAW delay line device exhibits a high *Q* of up to 1000 and an excellent power handling capability. It was also shown that the Lamb-wave oscillator is able to deliver high output power (>11 dBm) up to 250 ℃. Over a wide temperature range from RT to 230 ℃, the oscillation frequency exhibits a linear dependence on temperature with a small TCF of -47.5 ppm/ ℃. The frequency drift is less than 1%.

This work represents a major step toward the integration of GaN-based electronics with acoustic functions for sensing and high frequency power applications.

CHAPTER 3 GATE-LAST SELF-ALIGNED TECHNOLOGY FOR ALGAN/GAN HEMTS

3.1 Introduction

GaN-based HEMTs have great potential for RF and microwave wave power applications due to their unique combination of high electron velocity, large sheet carrier density and high breakdown field. Since the first demonstration of AlGaN/GaN HEMTs in 1993 [10], remarkable progress has been made to improve the transistor performance and reliability, leading to state-of-the-art results in terms of device operation speed and output power density. For example, f_T and f_{max} exceeding 300 GHz [64-66] and an output power density of 1.7W/mm at 95GHz [67] and 2.5 W at 40 GHz [68] have been successfully demonstrated in the literature. Such results were accomplished through process maturity in material growth and device fabrication, and innovative device scaling technologies. These technologies include heavily doped S/D Ohmic contact regrowth [64-67, 69-75], a thin AlN or InAlN top barrier [64, 65, 68-73, 75-80], an AlGaN or InGaN back barrier [64, 66, 70, 72-74, 76], the advanced T-gate fabrication process [64, 65, 70-72, 74] , or a gate-first self-aligned approach [66, 69, 70].

To facilitate a transistor operating at high speed with large output power and high efficiency, small on-state resistance (R_{on}) is always highly required to reduce the delay time and the dynamic power loss. As the channel dimensions are scaled down, the R_{on} becomes limited by the external resistance, such as the S/D Ohmic contact resistance and the access resistance. The formation of low Ohmic contacts resistance on the wide bandgap barrier layer of a GaN-based HEMT is difficult as compared to that in traditional Si CMOS technology. The reason is that the doping level in GaN by ion implantation is much lower than that in Si CMOS, and the activation efficiency is also very poor in GaN. On the other hand, multi-layer metals (Ti/Al/Ni/Au) and annealing at high temperature, typically around 850 ℃ [55], have always been adopted to form alloyed Ohmic contacts for conventional AlGaN/GaN HEMTs.

This is realized by the diffusion of Ti into AlGaN or GaN to cause n-type doping. The annealing process results in poor surface morphology and a rough metal boundary, limiting the minimum feature sizes that can be controlled during the fabrication. Thus, this alloyed Ohmic contact process prohibits the employment of advanced technologies for device scaling, such as gate self-alignment. In addition, some spikes formed under the alloyed Ohmic contact may cause a high electric field and consequently reduce the breakdown voltage.

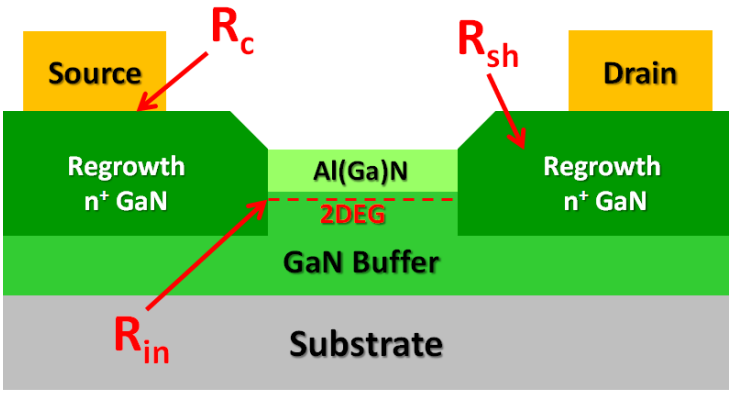

Figure 3.1.1 The cross-sectional schematic of the S/D regrowth structure.

One emerging alternative approach is incorporating regrown heavily doped GaN or InGaN S/D for Ohmic contact formation. Both MOCVD and MBE have been used for S/D regrowth [64-67, 69-75, 81]. After patterning the dummy gate regrowth mask and recessing the device S/D region, the sample is loaded back into the MOCVD or MBE chamber to regrow n^+-GaN or InGaN in the S/D region, as shown in Fig. 3.1.1. The contact between the electrode and regrown S/D (R_c) and the sheet resistance of the regrown S/D (R_{sh}), determined by the regrowth doping level, should be small enough to reduce the device access resistance. In addition, the regrowth interface resistance (R_{in}) associated with the 3D n^+-GaN/InGaN to 2DEG transition region also contributes to the total device on-resistance (R_{on}). Moreover, the surface morphology of the regrown S/D also plays an important role. Since the gate metal in very short gate length HEMTs needs to be precisely positioned, a high step and rough surface will interfere with the alignment accuracy.

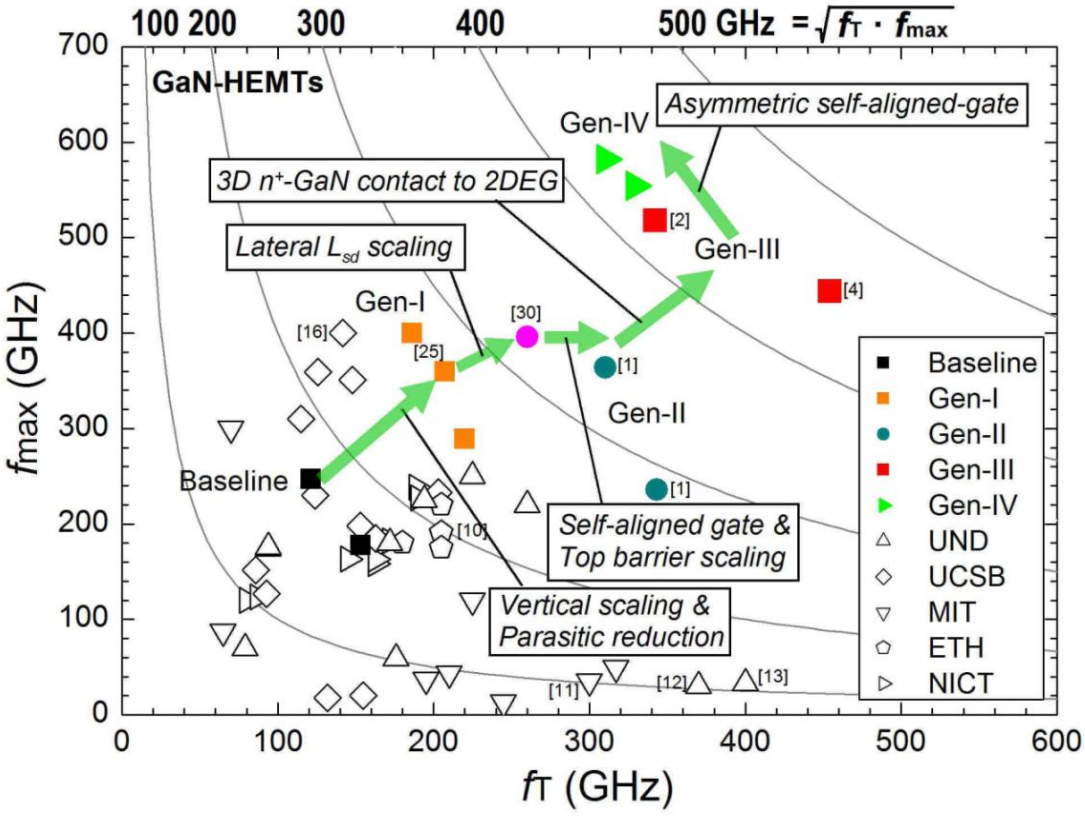

Figure 3.1.2 Summary of the RF performances for stat-of-the-art GaN HEMTs in the literature [64].

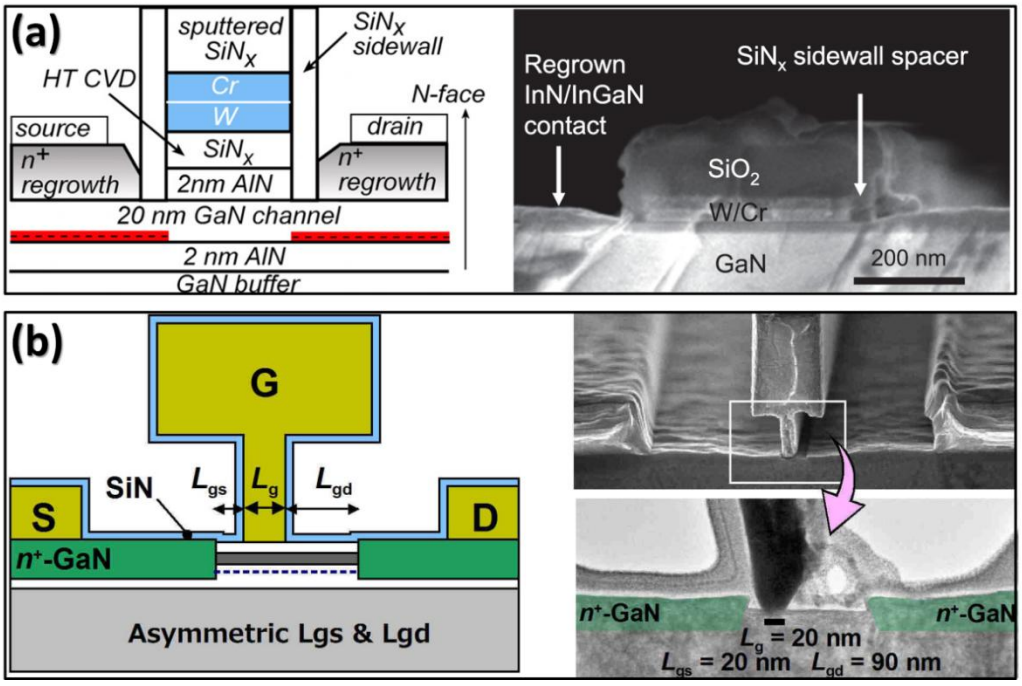

Figure 3.1.3 The cross-sectional schematics and SEM images of the device structures in the literature: gate-first self-aligned process (a) [70] and T-gate process (b) [64].

For high-frequency power applications, f_T, f_{max}, I_{DS} and BV_{off} are the key device performance parameters. In addition to the superior material properties, a proper design of the gate configuration and aggressive device scaling are desirable for high frequency GaN HEMTs. As summarized in Fig. 3.1.2, advanced gate scaling technologies, such as a gate-first self-aligned structure or a T-gate fabrication process, for the reduction of intrinsic and parasitic delay components in GaN HEMTs significantly enhance both f_T and f_{max} up to the 450 and 600 GHz range, respectively. Cross-sectional schematics and scanning electron microscopy (SEM) images of reported devices fabricated using a gate-first self-aligned (a) [70] or a T-gate process (b) [64] in the literature are illustrated in Fig. 3.1.3.

In this work, a gate-last self-aligned process was developed for fabrication of AlGaN/GaN HEMTs. Regrown S/D Ohmic contacts and low-κ BCB (κ=2.65) planarization technologies were implemented to reduce the access resistance and parasitic capacitance, minimizing the RC-related delay. Compared with the gate-first self-aligned process, the T-shaped gate formed in this gate-last approach enables high f_T and f_{max} simultaneously. In addition, this demonstrated gate-last self-aligned process is less demanding in gate lithography than the conventional T-gate process, which can potentially reduce the process complexity and improve the yield[82].

3.2 Device structure and fabrication process

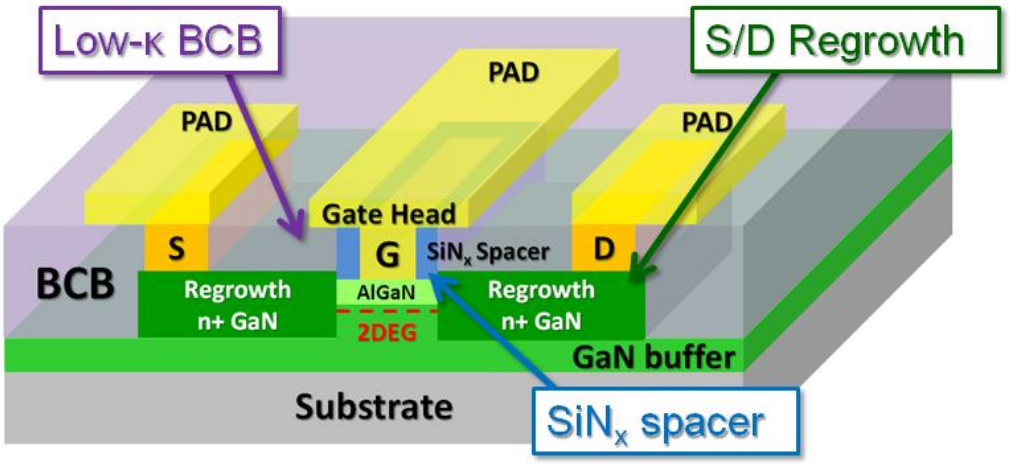

Figure 3.2.1 The self-aligned gate-last AlGaN/GaN HEMT architecture.

The self-aligned gate-last AlGaN/GaN HEMT architecture is shown in Fig.3.2.1. The regrown n^+-GaN S/D for minimizing contact resistance was incorporated and a low-κ BCB polymer supporting layer was employed under the gate head to minimize the parasitic capacitance. The devices also feature precisely defined L_{GS} and L_{GD} by the SiN_x sidewall spacers.

The AlGaN/GaN heterostructures were grown on a 2-inch sapphire substrate in an AIXTRON2000HT MOCVD system. The epi-layers consist of, from bottom to top, a 35 nm low-temperature AlN nucleation layer, a 300 nm high-temperature AlN buffer layer, a 2.7 μm undoped GaN layer, a 1 nm AlN spacer layer and, finally, a 25 nm $Al_{0.3}Ga_{0.7}N$ barrier layer, as shown in Fig.3.2.2(a). Room temperature Hall measurements showed a 2DEG density of 1.01 $\times 10^{13}/cm^2$ with a mobility of 1950 cm^2/V s, leading to a sheet resistance of 315 Ω/□. The gate-last self-aligned process was realized by means of a dummy gate [69], which was eventually removed after BCB planarization and replaced with a metal gate. Fig. 3.2.2 illustrates the detailed process flow. Firstly, 300-nm-thick SiO_2 was deposited by PECVD. The initial 1 μm SiO_2 dummy gate was defined by photolithography and patterned using a RIE process. Subsequently, wet lateral etching was performed in a buffered oxide etchant (BOE) solution to further shrink the SiO_2 gate length down to < 500nm [Fig. 3.2.2(b)]. A layer of PECVD SiN_x was then blanket deposited and followed by an anisotropic RIE process to form sidewall spacers. Before regrowth, the S/D regions were exposed by ICP etching down to the GaN buffer. The etch depth into the MISHEMT structure was 90 nm [Fig. 3.2.2(c) & (d)]. After that, 150 nm n^+-GaN with a two-step doping profile (Si doping level: ~2×10^{19} cm^{-3} for the first 30 nm and up to 6×10^{19} cm^{-3} for the remaining 120 nm) was grown in the exposed S/D regions by MOCVD [Fig. 3.2.2(e)]. The light doping used at the beginning of the regrowth ensures that the regrown layer is of good crystalline quality and smooth for the subsequent growth of heavily doped top layer. After mesa isolation etching by ICP, S/D electrodes were formed on the n^+-GaN layer using a nonalloyed Cr/Au contact. The distance between the S/D metal electrodes (L_{SD}) was 4 μm [Fig. 3.2.2(f)]. Then, the sample was spin-coated with a layer of BCB and cured in a vacuum oven at 250 ℃. The curing time was two hours including thirty minutes for

temperature ramping. The cured BCB film was able to provide sufficient mechanical support for the following T-shaped metal gate [Fig. 3.2.2(g)]. After curing, the BCB was etched back using an RIE process to expose the SiO_2 dummy gate [Fig. 3.2.2(h)]. Finally, the dummy gate was removed by BOE and replaced with a Ni/Au metal gate [Fig. 3.2.2(j)].

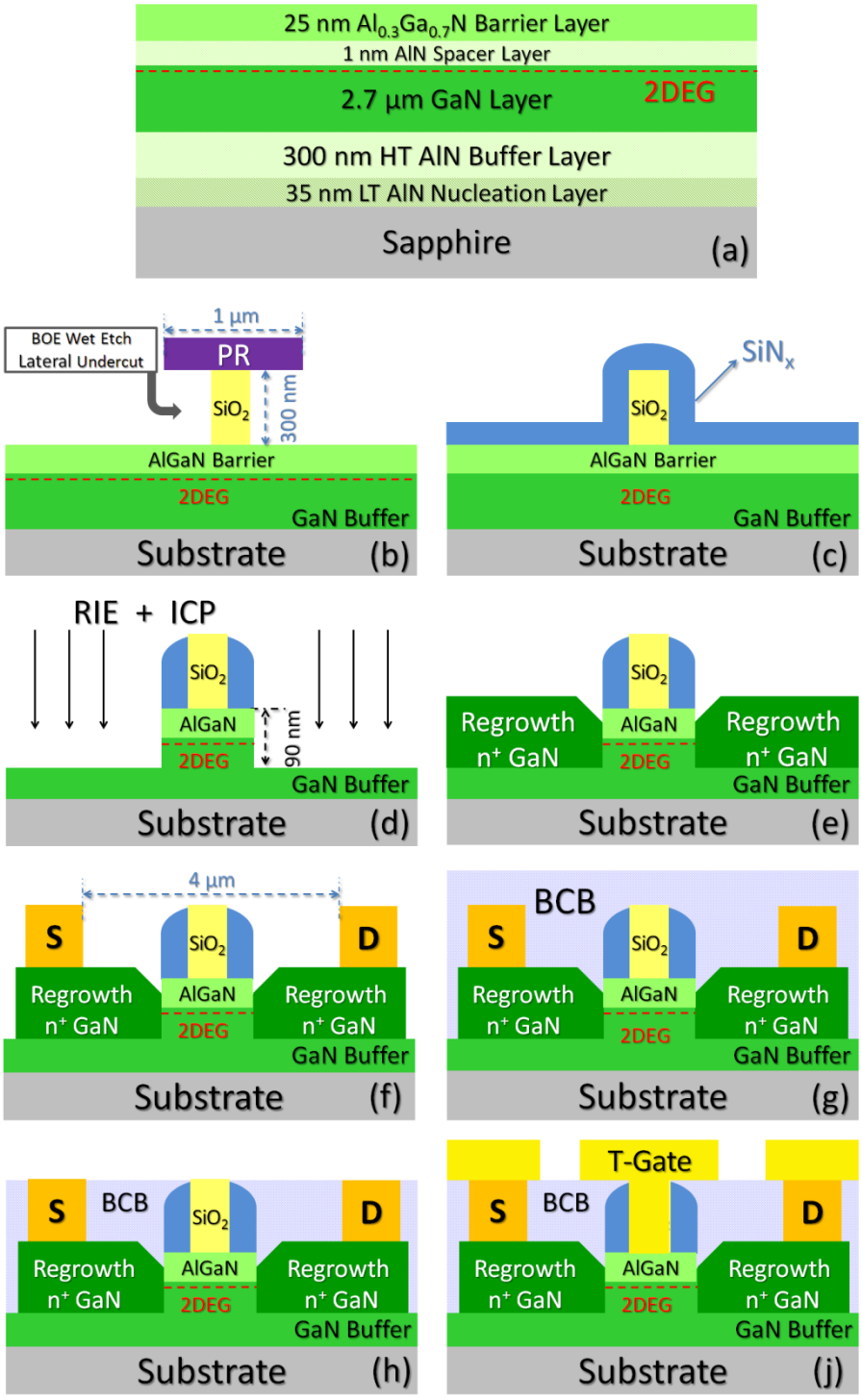

Figure 3.2.2 The fabrication process of the gate-last self-aligned AlGaN/GaN HEMTs.

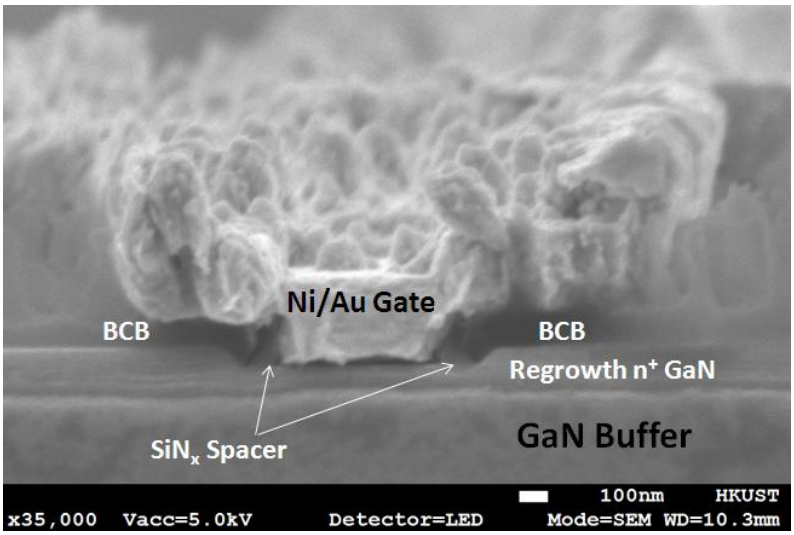

Figure 3.2.3 The cross-sectional SEM image of a fabricated device.

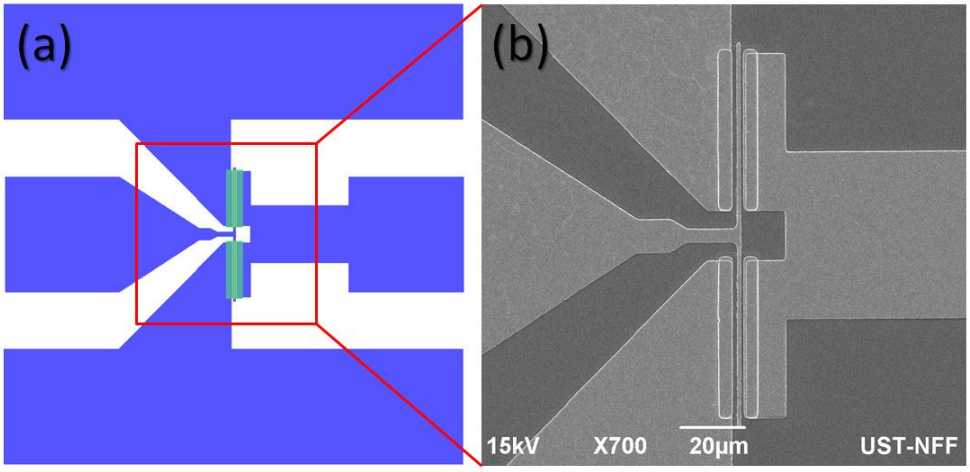

Figure 3.2.4 The device layout (a) and a top-view SEM image of the gate region (b)

A cross-sectional SEM image of the gate region for a fabricated HEMT is shown in Fig. 3.2.3. The gate head of the T-shaped gate is 1.5 μm, defined by photolithography. The thickness of the BCB supporting layer is about 100 nm and the L_{GS} and L_{GD} are 90nm, which is defined by the SiN_x sidewall spacers. The PECVD SiN_x sidewall spacers, grown at a relatively low temperature (300 ℃), could be densified during the high temperature S/D regrowth process. Therefore, they could withstand the BOE wet etching during the SiO_2 dummy gate removal. Fig.3.2.4 shows the device layout (a) and a top-view SEM image of the gate region (b). The pad configuration is specially designed for RF characterization using GSG probes. As shown

in Fig. 3.2.5, conventional HEMTs with 1 μm gate length fabricated on a similar AlGaN/GaN heterostructure were used as a reference for comparison in this work.

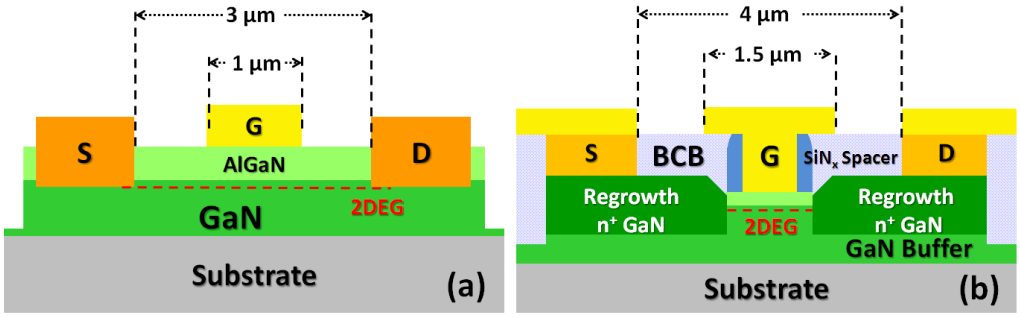

Figure 3.2.5 The cross-sectional schematics of the conventional HEMT (a) and gate-last self-aligned HEMT (b).

3.3 Device characterization and discussion

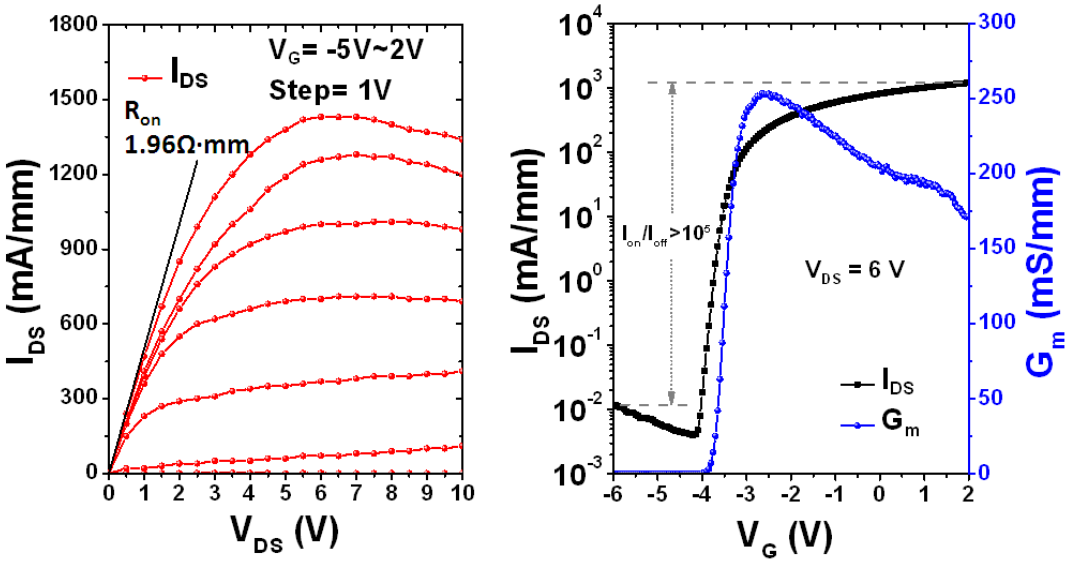

Figure 3.3.1 The DC output and transfer characteristics of the gate-last self-aligned HEMT with L_G = 0.35 μm and W_G = 2 × 50 μm.

The DC characteristics of the fabricated AlGaN/GaN HEMTs were measured on-wafer using an HP4156A precision semiconductor parameter analyzer. Fig. 3.3.1 shows the DC performance of the 0.35 μm gated self-aligned AlGaN/GaN HEMT with a gate width (W_G) of 2 × 50 μm. The device exhibits a high maximum I_{DS} of 1400 mA/mm at V_{DS} = 6 V and V_{GS} =

2 V, and the R_{on} is as low as 1.96 Ω mm. The peak G_m is 262 mS/mm at V_{DS} = 6 V and V_{GS} = -2.8 V. Moreover, the device presents both gate leakage and off-state drain leakage below 10^{-2} mA/mm at V_{GS} = -6 V and V_{DS} = 6 V, resulting in a large I_{on}/I_{off} of over 10^5. The typical DC characteristics of the reference conventional HEMT are shown in Fig. 3.3.2. Compared with the gate-last self-aligned one, the HEMT fabricated using the conventional technology shows a relatively low maximum I_{DS} of 800 mA/mm, a low peak G_m of 230 mS/mm, and a much larger R_{on} of 3.31Ω mm.

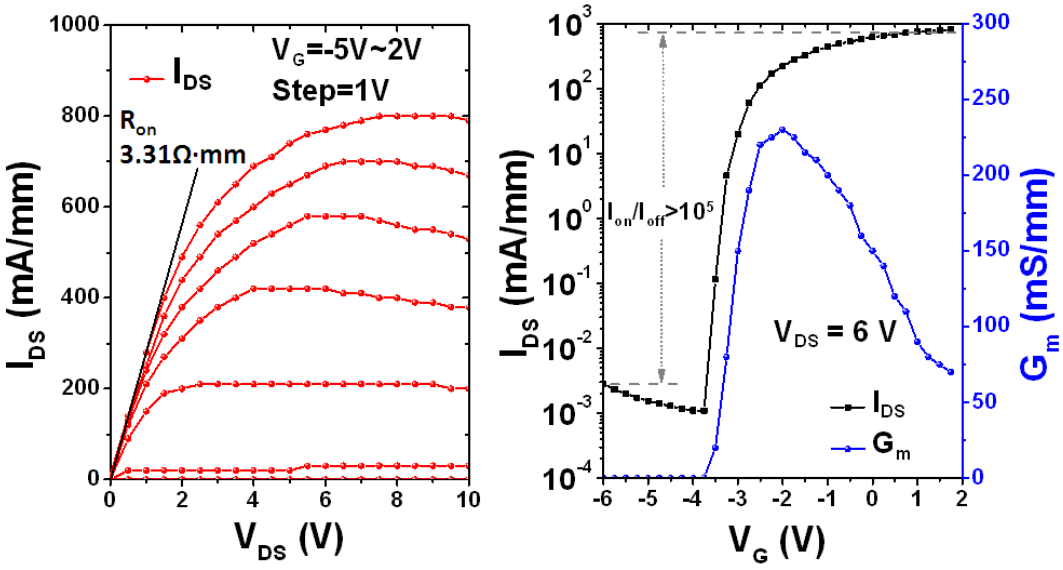

Figure 3.3.2 The DC output and transfer characteristics of the conventional HEMT with L_G = 1 μm and W_G = 2 × 50 μm.

On-wafer S-parameter measurements were carried out in the frequency range of 0.1 - 39 GHz using an HP 4142B modular DC source/monitor and an Agilent PNA network analyzer 8722ES with Cascade microwave GSG probes. The system was calibrated with an off-wafer short-open-load-through (SPLT) calibration standard. On-wafer open and short pads were used to de-embed the parasitic pad capacitances from the measured S-parameters.

Fig. 3.3.3 shows the RF characteristics of the 0.35 μm gated device measured at the maximum f_T bias condition (V_{DS} = 9 V, V_{GS} = -2 V). A simultaneously high f_T and f_{max} of 34 and 37 GHz are obtained, respectively, and the $f_T \times L_G$ product is 11.9 GHz μm. At a drain bias of 9 V and a gate bias of -1.5 V, the best f_T of 12 GHz and f_{max} of 31 GHz are obtained for the

1 µm gated device fabricated using the conventional technology, as shown in Fig 3.3.4.

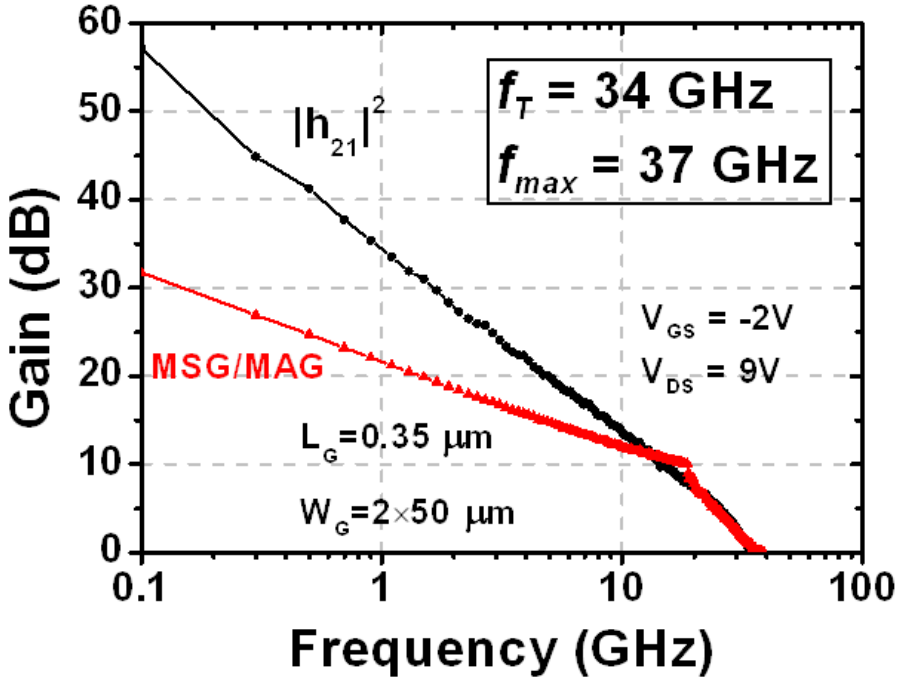

Figure 3.3.3 The Small signal RF characteristics of the gate-last self-aligned HEMT with L_G = 0.35 µm and W_G = 2 ×50 µm showing peak f_T and f_{max} of 34 and 37 GHz, respectively.

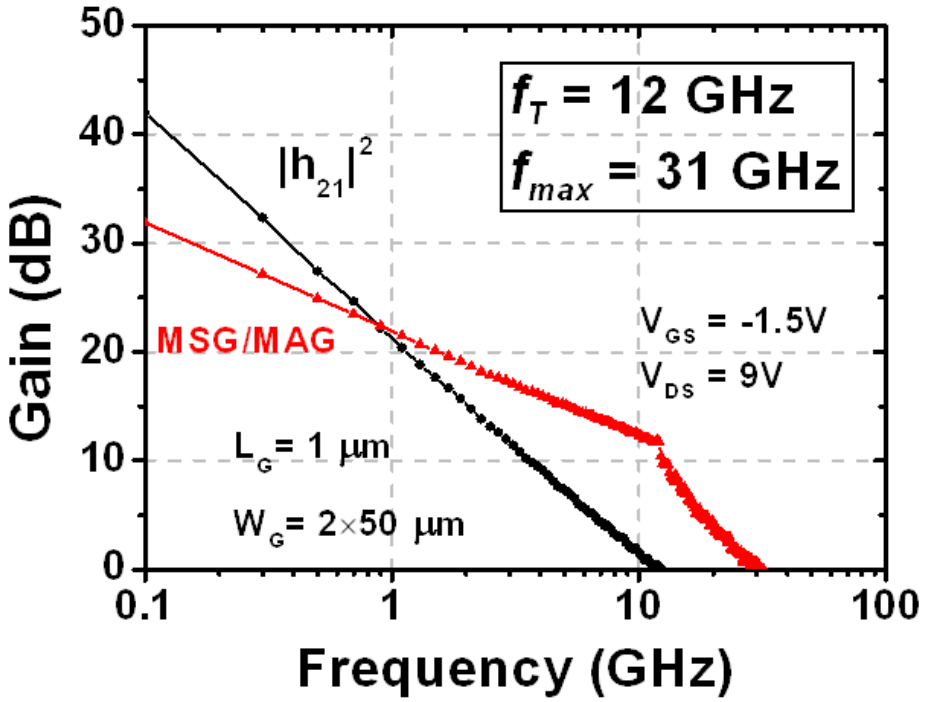

Figure 3.3.4 The Small signal RF characteristics of the conventional HEMT with L_G = 1 µm and W_G = 2 ×50 µm showing peak f_T and f_{max} of 12 and 31 GHz, respectively.

The achieved better performances in the gate-last self-aligned device are mainly attributed to the scaled self-aligned architecture as well as the reduction of access resistance by the heavily doped S/D regrowth. However, the S/D regrowth conditions in the abovementioned experiment are not optimum. Transmission line method (TLM) measurements were used to investigate the electrical properties of the regrown n^+-GaN on the sample. Fig. 3.3.5 shows the results of the two TLM patterns, whose schematics are shown in the insets (*TLM-1* and *TLM-2*). The metal/n^+-GaN contact resistance and the sheet resistance of the n^+-GaN are 0.319 Ω mm and 282 Ω/□, respectively, as determined by *TLM-1*. These values are much higher than, almost double, the best results achieved previously by our group [81], suggesting a much lower doping concentration in the regrown S/D in this experiment. Moreover, no reliable linear fitting can be obtained for *TLM-2*, indicating the very large and non-uniform interface resistances between the 3D n^+-GaN and the 2DEG channel.

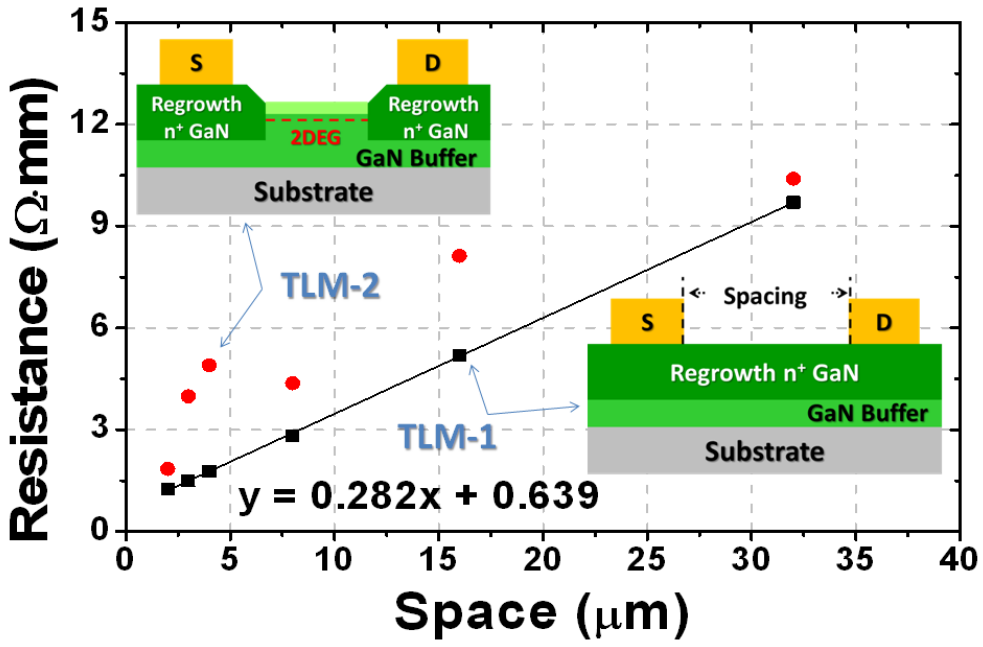

Figure 3.3.5 The results of the two TLM patterns.

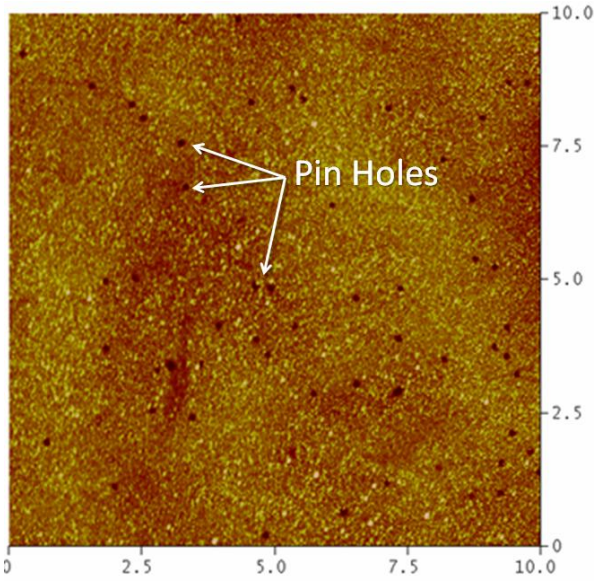

Figure 3.3.6 AFM image of the regrown n^+-GaN across a scanned area of 10 μm × 10 μm.

Figure 3.3.6 shows an atomic force microscopy (AFM) image of the regrown n^+-GaN across a scanned area of 10 μm × 10 μm. Obviously, there are lots of pin holes on the surface and they become much denser in the region near the regrowth boundary than in other regions. The pin holes at the regrowth interface may result in poor connection between the regrown n^+-GaN and the 2DEG channel, leading to larger interface resistance and non-uniformity. The poor regrowth conditions may introduce high parasitic resistance and hinder the device performances. As a result, the device could be further improved by optimizing the regrowth conditions, such as by eliminating the pin holes, and increasing the doping concentration and the thickness of the regrown layer.

3.4 Summary

This chapter presents novel AlGaN/GaN HEMTs fabricated using a gate-last self-aligned process. Regrown n^+-GaN S/D by MOCVD was adopted to reduce the contact resistance. The sub-micron gated device featuring scaled self-aligned L_{GS}/L_{GD} and a low-κ BCB supporting layer under the gate head, exhibited improved DC and RF performances when compared with the device fabricated using a conventional process. The device with an L_G of 0.35 μm showed a maximum I_{DS} exceeding 1200 mA/mm with a low R_{on} of 1.96 Ω mm and an I_{on}/I_{off} of over

10^5. The f_T and f_{max} were 34 and 37 GHz, respectively, resulting in a $f_T \times L_G$ product of 11.9 GHz μm. However, the S/D regrowth conditions were yet-to-be perfected in this work.

Nevertheless, the demonstrated gate-last self-aligned technology can potentially reduce the process complexity and improve the yield for the fabrication of GaN-based HEMTs, by easing the alignment difficulty for the gate lithography in the conventional T-gate process. Further improvements can be achieved by optimizing the S/D regrowth conditions and shrinking the gate footprint and the gate head, and scaling the barrier thickness.

CHAPTER 4 MOCVD-GROWN *IN-SITU* SiN_x GATE DIELECTRIC FOR ALN/GAN MISHEMTS

4.1 Introduction

AlGaN/GaN HEMTs have been established as excellent candidates for microwave power applications due to their capability of higher power densities at higher frequencies as compared to Si and GaAs-based devices. The ever increasing demand for high-speed high-power devices has prompted much research recently into device scaling [64].

The frequency at which a HEMT operates is limited by the electron transit time from the source to the drain. Therefore, to reduce the gate or channel length is desirable and effective for boosting device operation speed. However, as the gate length scales, it is necessary to minimize the other parasitic delays in the device and take into account short channel effects to facilitate the high frequency performance of a HEMT. Aspect ratio (the ratio between the gate length and the gate-to-channel separation) is a critical factor affecting the operation of the field effect transistor and should be maintained sufficiently high to mitigate the short channel effects [43]. However, maintaining the aspect ratio alone does not guarantee performance improvement in GaN-based HEMTs. It is clear that the reduction of the barrier thickness for a conventional AlGaN/GaN HEMT will result in a significant drop of the carrier concentration in the 2DEG channel and a high gate leakage current. To overcome these problems, alternative thin barriers, such as lattice matched InAlN or all binary AlN, have been used recently [64, 65, 68-73, 75-80]. Among these III-Nitride heterostructures, AlN/GaN offers the highest theoretical 2DEG sheet charge density from a combination of the large bandgap of AlN and the maximum spontaneous and piezoelectric polarizations. As shown in Fig. 4.1.1, the conventional $Al_{0.3}Ga_{0.7}N$/GaN heterostructures show a 2DEG density below 10^{13} cm^{-2} with a barrier thickness lower than 15 nm, while AlN/GaN heterostructrues offer a significant carrier concentration, even when using barrier thicknesses below 6 nm [83]. Recently, high-quality AlN/GaN epitaxial growth has been reported with a large 2DEG concentration (>

2×10^{13} cm^{-2}) and high mobility (> 1200 cm^2/V s) for extremely thin AlN barriers [77, 83, 84]. The use of an ultra-thin AlN barrier layer can increase the intrinsic transconductance and decreases the short channel effects by placing the gate much closer to the 2DEG channel. In addition, the AlN barrier, with its high dielectric constant (8.5) and wide bandgap (6.2 eV), provides better carrier confinement and a larger breakdown field.

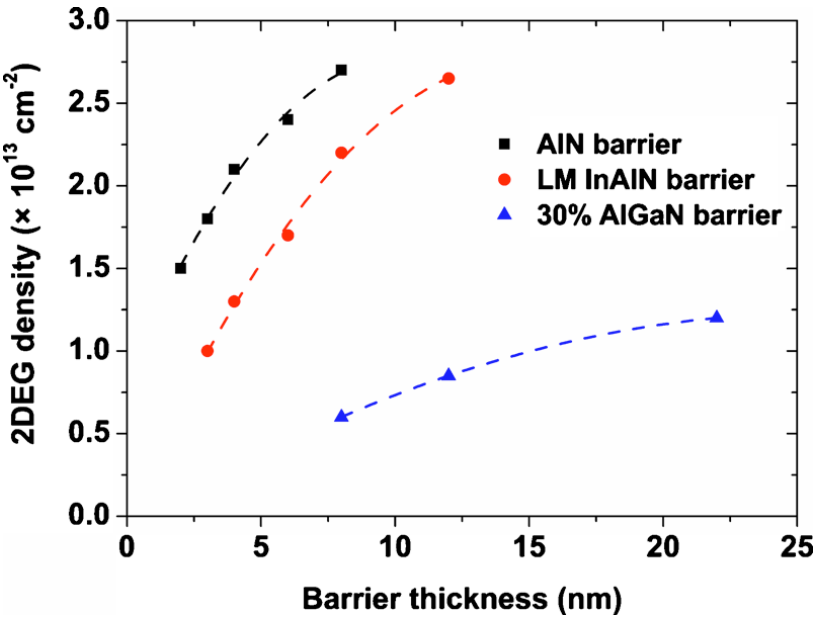

Figure 4.1.1 The 2DEG carrier densities of SiN_x/AlN/GaN, lattice matched $In_{0.17}Al_{0.83}N$/GaN, and $Al_{0.3}Ga_{0.7}N$/GaN heterostructures as a function of the barrier layer thickness [83].

Despite the excellent progress in AlN/GaN devices to date, there are still significant challenges to be overcome before they can be fully commercialized. Having a very thin AlN barrier layer, of only a few nm, the devices may suffer from surface sensitivity and large gate leakage currents unless the epilayers are well passivated [78]. The drain current degradation phenomenon of an unpassivated AlN/GaN HEMT, as shown in Fig 4.1.2, has been reported previously [85]. When sweeping of the transfer characteristics was continuously repeated for the unpassivated AlN/GaN HEMT, the values of both the drain current and the transconductance decreased gradually to unmeasurable levels. This phenomenon is caused by the surface trap centers, which trap electrons from the channel or gate current during measurement with a very long time constant. When the sweeping measurement was continuously repeated, the trapped electrons did not have enough time to be released. As a

result, more and more trapped electrons accumulated in the AlN surface, and thus increased the surface potential. The 2DEG underneath the AlN barrier layer was gradually depleted by the increased surface potential, and thus the drain current decreased. Besides this, the gate leakage current was significant, as large as 1 mA/mm, for the AlN/GaN HEMT with a 3 nm thick barrier, as shown in Fig 4.1.3 [85]. High gate leakage current leads to a large noise figure, high power consumption and reliability issues for the devices.

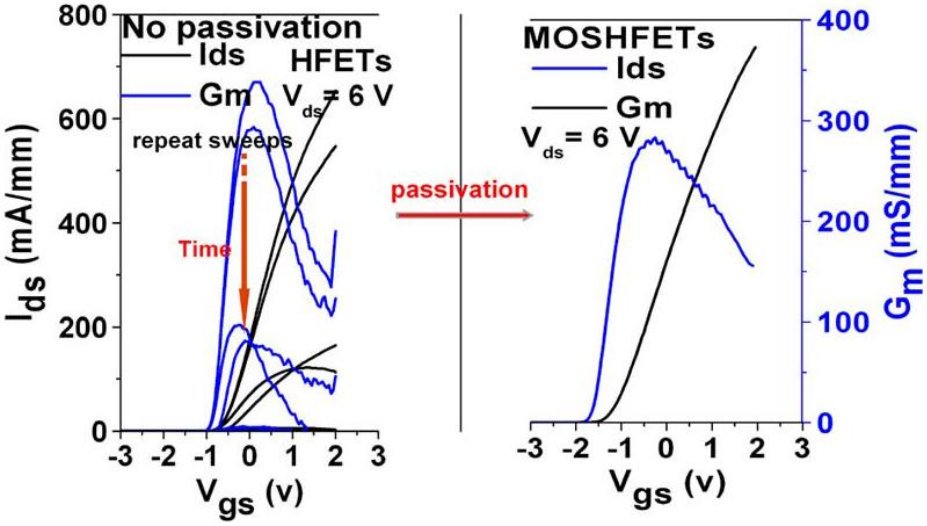

Figure 4.1.2 The drain current degradation phenomenon of an unpassivated AlN/GaN HEMTs [85].

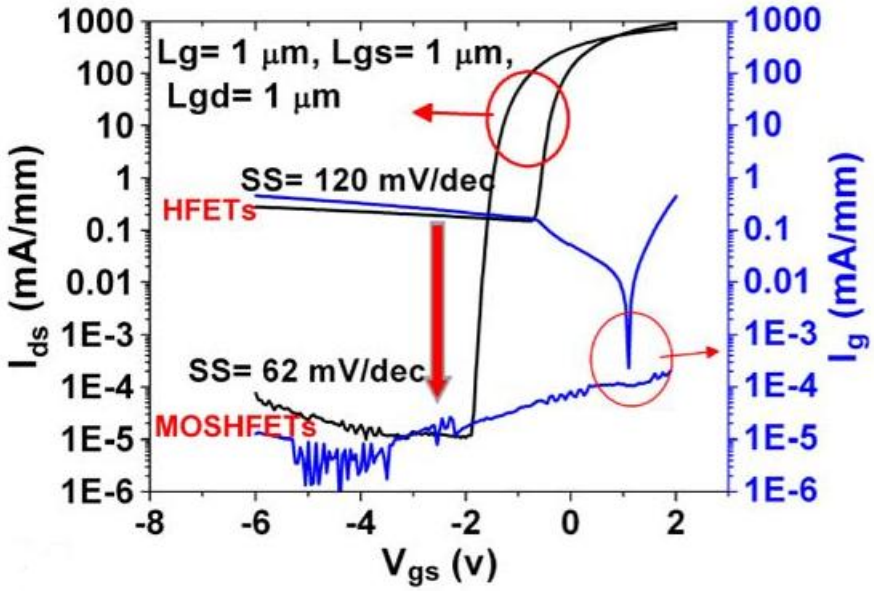

Figure 4.1.3 The gate leakage currents of the AlN/GaN HEMT and MOSHEMT with a barrier thickness of 3 nm [85].

To overcome these problems, several *ex-situ* deposited dielectrics, such as Al_2O_3 [69, 77, 78, 85, 86], SiN_x [87, 88], HfO_2 [89, 90] and Ta_2O_5 [89], have been explored as gate insulators for AlN/GaN MISHEMTs. MIS structures are highly preferred over Schottky-gate HEMTs due to the suppressed gate leakage current and enlarged gate swing. However, the insertion of a gate dielectric creates an additional dielectric/III-nitride interface with high-density traps. These trap states can substantially deteriorate the device performances [91-97]. Studies have shown that the interface trap states between the gate dielectric and III-nitride semiconductors are usually induced by exposure to air and damage in the subsequent fabrication processes. These trap states are extremely sensitive to certain specific processing steps such as surface cleaning, dielectric deposition and pre-/post-deposition treatments [91, 92]. It was also found that the trap state density increases in general with Al composition in the barrier layer, probably due to native oxidation, higher surface sensitivity or oxygen incorporation associated with high Al composition [95, 96]. In particular, the trap state density of a dielectric/AlN interface can reach over 4×10^{13} $cm^{-2}eV^{-1}$ in dielectric/AlN/GaN MIS devices grown by MBE [89, 98]. The situation can become even more complicated in AlN barriers grown by MOCVD since significant strain relaxation can occur in the AlN layer during temperature ramp-down. This undesirable relaxation can be minimized by adding a thin GaN cap layer on the AlN barrier [85, 87]. However, an extra GaN layer between the gate dielectric and AlN barrier is not preferable for a MIS device because of the introduced additional GaN/AlN interface, the increased gate-to-channel distance and the relatively narrow band gap of GaN.

Recently, an MOCVD *in-situ* grown SiN_x layer immediately after the transistor structure has been reported to be advantageous over existing *ex-situ* deposited insulators, for better surface passivation effects of AlN/GaN HEMTs [83, 99-101]. The fact that the SiN_x is grown *in-situ* means that the AlN surface is never exposed to air. The main benefit is the prevention of oxidation/contamination of the AlN surface from air exposure or damage during the device fabrication process. Thus, the formation of interface states would be suppressed or reduced. Moreover, high temperature growth by MOCVD can facilitate the formation of high quality *in-situ* SiN_x films. However, limited work has been reported with successful use of *in-situ*

SiN_x as gate dielectric for AlN/GaN MISHEMTs. It was even found that *in-situ* SiN_x gate dielectrics can lead to larger gate leakage when compared with *ex-situ* deposited ones [102]. On the other hand, high performance AlN/GaN HEMTs have been reported with an *in-situ* SiN_x cap layer for surface passivation rather than a gate dielectric. The SiN_x in the gate region was selectively removed during the device fabrication [68, 83].

In this work, *in-situ* SiN_x grown by MOCVD was employed as the gate dielectric for thin-barrier AlN/GaN MISHEMTs. Both material structural and electrical characterizations were performed to evaluate the performance of the *in-situ* SiN_x film as a gate insulator [103, 104]. Finally, a thorough study of interfacial trapping effects in the SiN_x/AlN/GaN MIS structures was conducted and two kinds of trap states with different time constants were identified and characterized [105]. In particular, the SiN_x/AlN interface exhibits remarkably low trap state densities in the range of 10^{11} to 10^{12} $cm^{-2}eV^{-1}$. These results imply the great potential of *in situ* SiN_x as an effective gate dielectric for AlN/GaN MIS devices.

4.2 Growth and characterization of *in-situ* SiN_x thin film grown on AlN/GaN heterostructures

The *in-situ* SiN_x/AlN/GaN heterostructures were grown on a 2-inch Si (111) substrate in an AIXTRON2000HT MOCVD system. The epi-layers consist of, from bottom to top, a 45 nm AlN nucleation layer, 1.3 μm strain/resistivity-engineering buffer layers, a 1 μm GaN layer, followed by a 1.5 nm AlN barrier layer and finally an *in-situ* SiN_x cap layer, as shown in Fig 4.2.1(a). The *in-situ* SiN_x was deposited immediately following AlN/GaN heterostructure growth in the MOCVD chamber, using silane and ammonia as precursors. The chamber pressure and substrate temperature were 100 mbar and 1145 ℃, respectively. For the characterization of the electrical properties, MISHEMTs and circular-shaped MIS diodes were fabricated. Firstly, mesa etching for device isolation was performed using a CF_4/O_2-based reactive ion etch (RIE) process followed by a Cl_2-based inductively coupled plasma (ICP) etch process, as shown in Fig 4.2.1(b). After selective removal of the SiN_x cap layer in the Ohmic contact region by RIE, Ti/Al/Ni/Au (20/150/50/80 nm) was deposited by e-beam

evaporation and annealed at 850 ℃ in N_2 ambient for 30 s, as shown in Fig 4.2.1(c). Finally, the Ni/Au (20/200 nm) gate metal was deposited on the *in-situ* SiN_x by e-beam evaporation, as shown in Fig 4.2.1(d). The gate length (L_G) and gate-to-source/gate-to-drain distances (L_{GS}/L_{GD}) of the fabricated MISHEMTs are 1 μm. The diameter of the circular metal gate of the MIS diodes is 200μm.

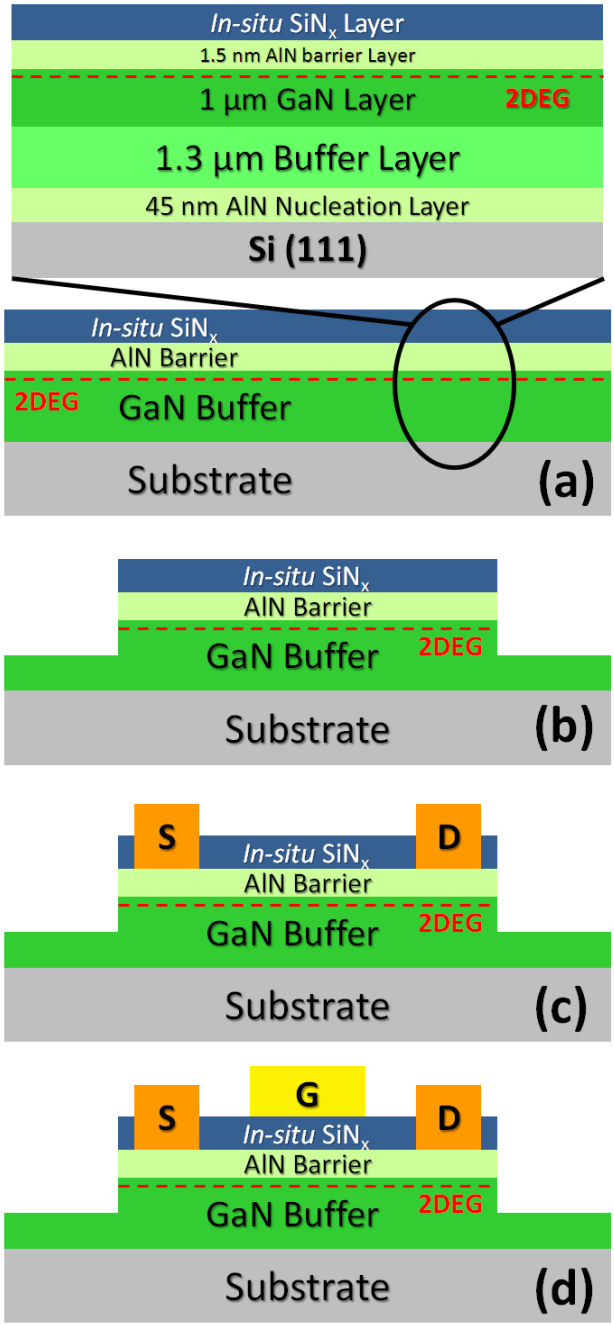

Figure 4.2.1 The fabrication process of the *in-situ* SiN_x/AlN/GaN MISHEMTs.

Similar GaN(1 nm)/AlN(3 nm)/GaN schottky diodes and Al_2O_3(7 nm)/GaN(1 nm)/AlN (3 nm)/GaN metal-oxide-semiconductor (MOS) diodes were fabricated and characterized as references for comparison in this work [85], as shown in Fig 4.2.2. The *in situ* SiN_x cap layer effectively alleviated the relaxation of AlN barrier during the post-growth cooling process, so the previously used 1 nm GaN surface protection layer for the GaN/AlN/GaN HEMT samples was omitted.

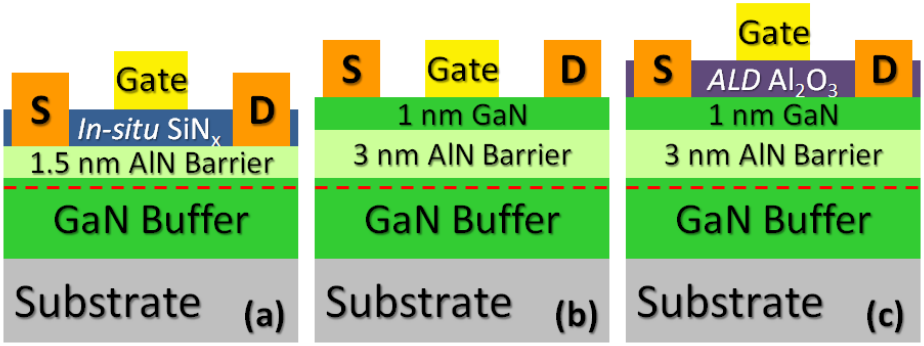

Figure 4.2.2 The cross-sectional schematics of the *in-situ* SiN_x/AlN/GaN MISHEMT (a), the GaN/AlN/GaN HEMT (b), and the Al_2O_3/GaN/AlN/GaN MOSHEMT (c).

The AFM and transmission electron microscopy (TEM) images in Fig 4.2.3 show good surface morphology and uniform coverage of the thin SiN_x film. The root mean square (RMS) roughness across a 5 μm × 5 μm scanned area is 2.15 nm. The thickness of the *in-situ* SiN_x film is 7 nm. The growth time was 28 minutes, and thus the growth rate is determined to be 2.5 Å/min.

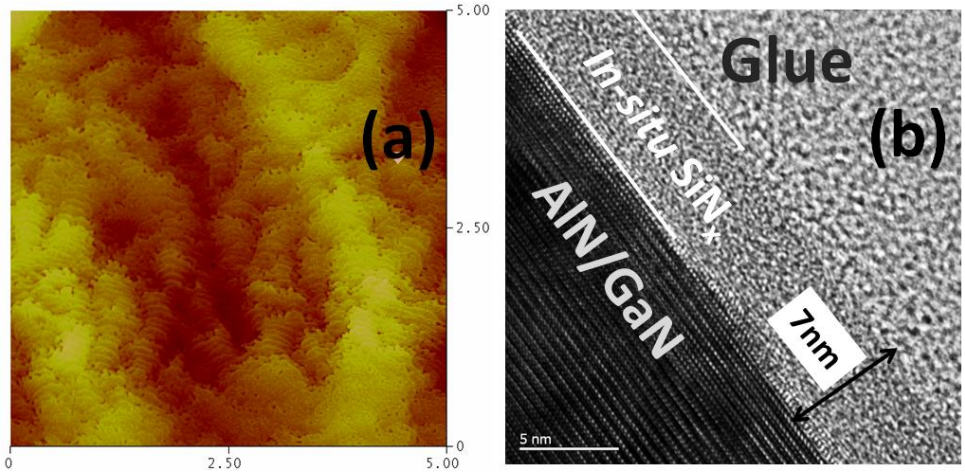

Figure 4.2.3 The AFM (a) and TEM (b) images of the 7 nm *in-situ* SiN_x film deposited on an AlN/GaN heterostructure by MOCVD.

To quantify the nitrogen composition in the SiN_x film, x-ray photoelectron spectroscopy (XPS) measurements were carried out. The XPS spectra were acquired after sputter removal of about 2 nm of material from the surface by argon. The binding energy measurement was calibrated by correcting the adventitious C1s peak to be 285 eV. Fig 4.2.4 shows the results of the peak fitting performed on the Si2p core-level XPS spectrum of the 7 nm *in-situ* SiN_x. Two components corresponding to Si-N bonds (101.5 eV) and a mixing of Si-N and Si-Si or Si-H bonds (100.6 eV) were extracted from the spectrum [106, 107]. It was found that the *in-situ* SiN_x in this study is Si-rich with a N/Si ratio of 1.21, similar to the reported results [108].

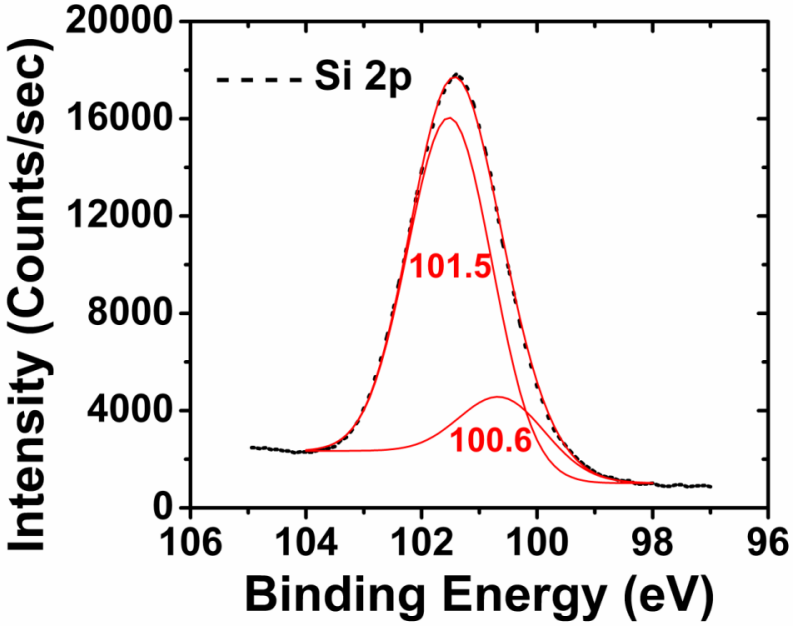

Figure 4.2.4 The XPS results of Si2p core-level spectra of the *in situ* SiN_x thin film deposited by MOCVD.

Leakage current measurements of the MIS diodes with 3 nm and 7 nm *in-situ* SiN_x were carried out. As compared with the reference GaN/AlN/GaN Schottky diode in Fig 4.2.5, at a negative bias of -5 V, the reverse leakage currents of the MIS diodes with 7 nm and 3 nm *in-situ* SiN_x were about 7 and 4 orders of magnitude lower, respectively. The leakage current density of the MIS diode with 7 nm *in-situ* SiN_x was in the order of 10^{-7} A/cm^2, remarkably lower than that of similar structures using other dielectrics [78, 85, 87-90]. Fig 4.2.6 shows the current density (J_L) versus electric field (E_F) plots, along with the data of MOS diodes

made with various thicknesses of Al_2O_3. Direct tunneling current was observed for the 3 nm *in-situ* SiN_x film, while the film with a thickness of 7 nm showed no significant direct tunneling. On the other hand, the reference sample with 7 nm Al_2O_3 showed the direct tunneling phenomenon. Leakage current plots for the thicker Al_2O_3 on conventional AlGaN/GaN heterostructures in the literature [93, 95] are also included for comparison. At low field, the leakage current of the 7 nm *in-situ* SiN_x diode is comparable with that of much thicker Al_2O_3 MOS diodes. The breakdown field (E_{BD}) for the 7 nm *in-situ* SiN_x on AlN/GaN heterostructures is around 5.7 MV/cm, as shown in the inset of Fig 4.2.6.

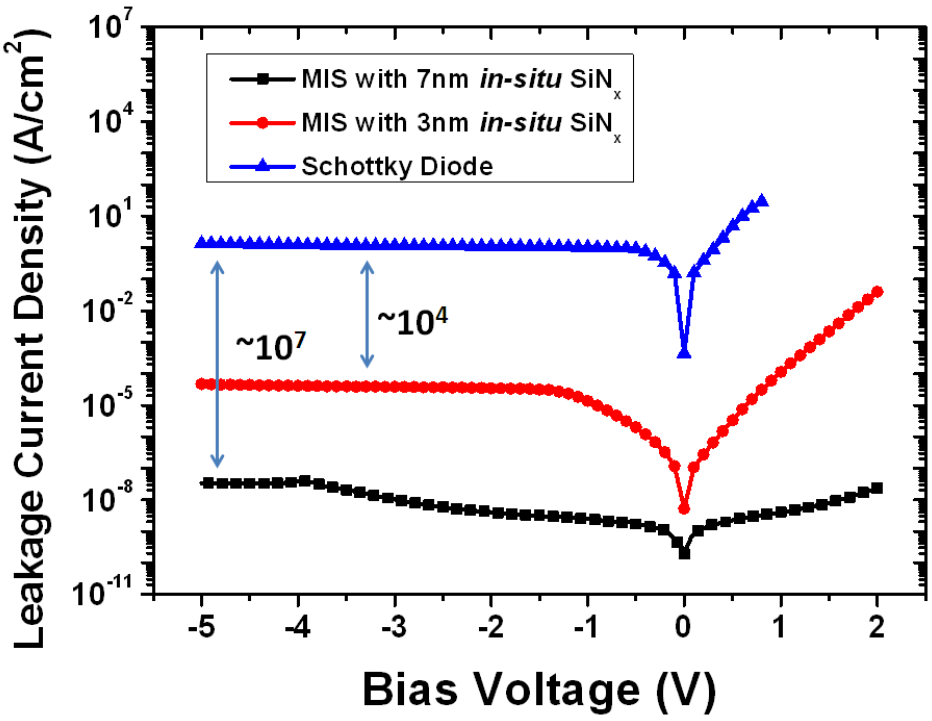

Figure 4.2.5 The leakage currents of a GaN/AlN/GaN Schottky diode with a 3 nm AlN barrier and two 1.5-nm-barrier MIS diodes with 3 nm and 7 nm *in-situ* SiN_x.

To determine precisely the nature of conduction in the *in-situ* SiN_x film, $\log(J_L/E_F)$ vs $E_F^{1/2}$ of the 7 nm *in-situ* SiN_x sample for E_F up to its breakdown limit is plotted in Fig 4.2.7. It is revealed that the *in-situ* SiN_x exhibits a typical silicon nitride behavior [109-111]. The curve can be fitted accurately by the combination of an Ohmic conduction mechanism and a Frenkel-Poole emission mechanism, described by

$$J_L = \frac{E_F}{\rho_{ohm}} \tag{4.1}$$

and

$$J_L = C \times E_F \times exp\left\{-\frac{q}{kT}\left[\emptyset_D - \left(\frac{q}{\pi\varepsilon_0\varepsilon_{dyn}}E_F\right)^{1/2}\right]\right\} \quad (4.2)$$

respectively, where C is a constant, $\emptyset_D$ is the Frenkel-Poole barrier height and ε_{dyn} is the dynamic dielectric constant of the SiN_x films. A high resistivity (ρ_{ohm}) of $>10^{14}$ Ω cm was obtained at a field lower than 1.3 MV/cm for the 7 nm *in-situ* SiN_x film. The Si-rich *in-situ* SiN_x in this study contains relatively high concentrations of Si dangling bonds and distorted excess Si-Si bonds, which may result in midgap defect states or bulk traps inducing more electrical conduction by Frenkel–Poole emission [109, 110]. Thus, the resistivity and breakdown field can be further improved by optimizing the *in-situ* SiN_x growth conditions by MOCVD, such as temperature, pressure and the gas flow of silane and ammonia, by adjusting the N/Si ratio.

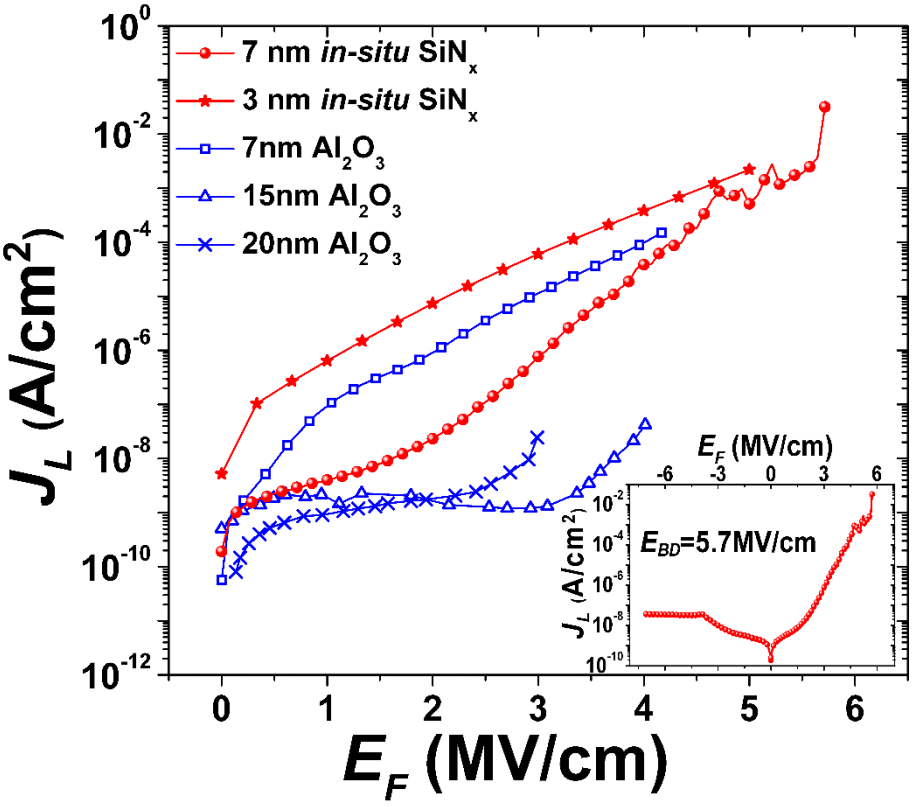

Figure 4.2.6 The leakage current density (J_L) versus electric field (E_F) plots for the *in-situ* SiN_x MIS diodes and the Al_2O_3 MOS diodes biased in the accumulation region. The inset shows the breakdown field (E_{BD}) of 7 nm *in-situ* SiN_x.

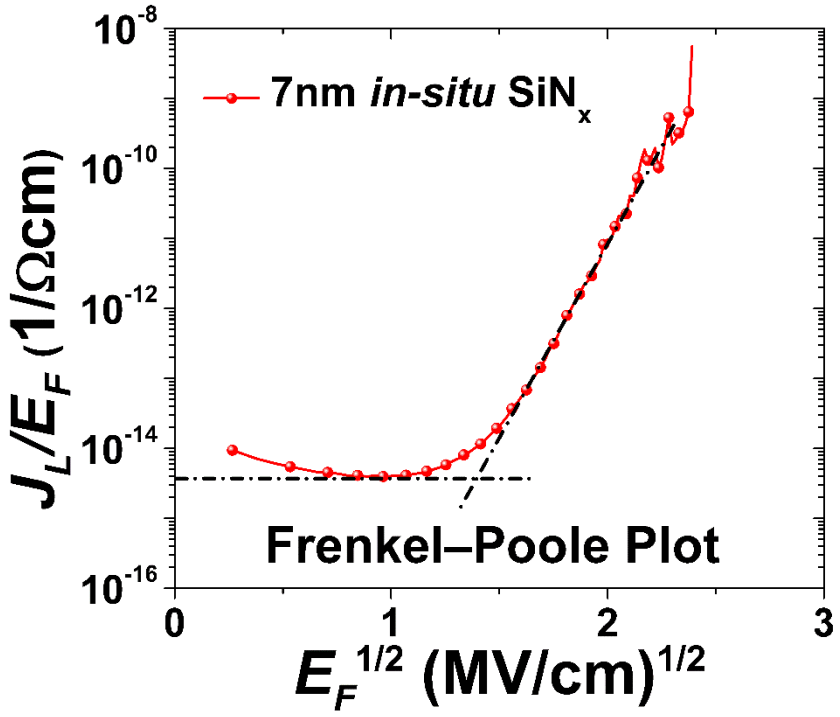

Figure 4.2.7 The Frenkel-Poole plot for the MIS diodes with 7 nm *in-situ* SiN_x.

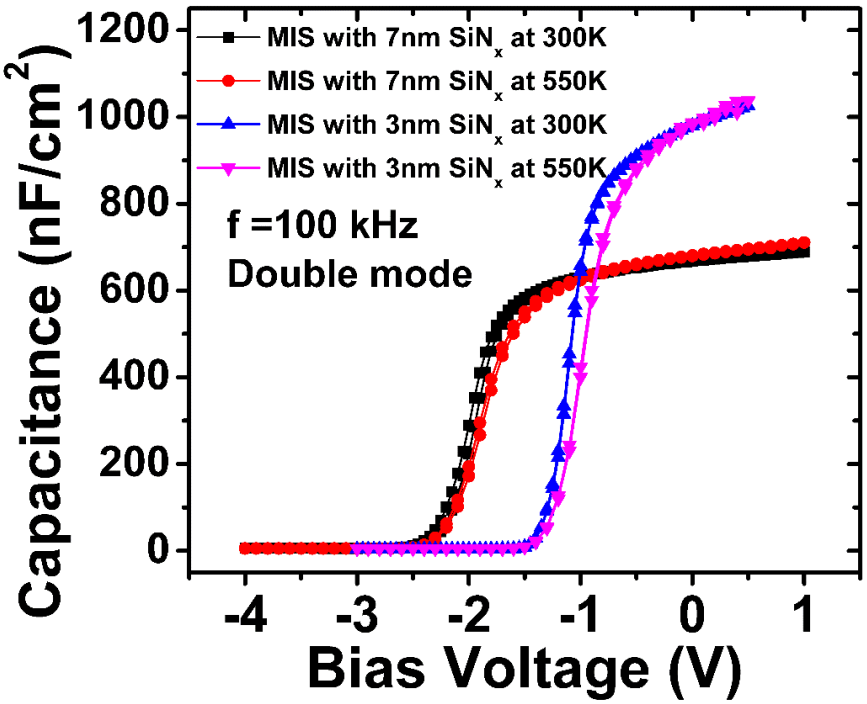

Figure 4.2.8 The double mode *C-V* characteristics of the *in-situ* SiN_x/AlN/GaN MIS diodes at two different temperatures.

Fig 4.2.8 illustrates the typical double mode capacitance-voltage (*C-V*) characteristics of *in-situ* SiN_x/AlN/GaN MIS diodes at two different temperatures, 300 K and 550 K. The measurements were set up with an up-and-down sweep rate of 0.05 V/s and a voltage variation of 50 mV at 100 KHz. A sharp transition from depletion mode to accumulation mode, with very small hysteresis for both diodes, was observed. The slight temperature shift from 300K to 550K suggests the presence of a high quality interface between the *in-situ* SiN_x layer and the AlN/GaN heterostructure [95, 112]. Using the measured capacitances of the MIS diodes with 3 nm and 7 nm *in-situ* SiN_x, 1037 nF/cm^2 and 661 nF/cm^2, respectively, and series capacitance combination with the 2DEG accumulation region $1/C_{MIS} = 1/C_{SiN_x} + 1/C_{AlN}$, the capacitance of the 7 nm *in-situ* SiN_x was determined to be 1042 nF/cm^2. The effective dielectric constant of the *in-situ* SiN_x in this work was deduced to be ~ 8.3, higher than the typical value of 7.5 for stoichiometric Si_3N_4. The higher value could be due to the higher silicon content in the film [110, 111], as determined by the XPS composition analysis.

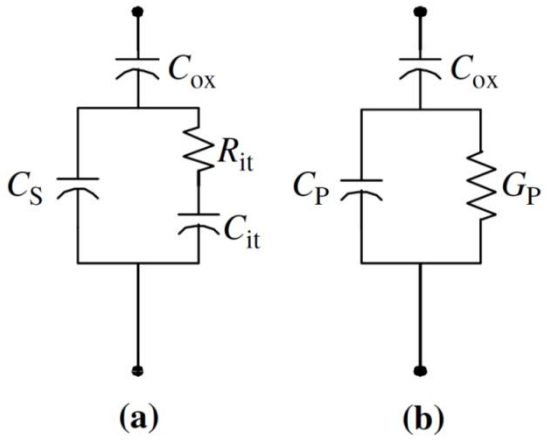

Figure 4.2.9 Equivalent circuits for conductance measurements: (a) MIS capacitor with an interface trap time constant $\tau_T = C_{it} \cdot R_{it}$, (b) simplified circuit of (a) [113].

A frequency dependent conductance analysis was performed in the frequency range of 1 kHz to 1 MHz to evaluate the trapping effects in the *in-situ* SiN_x/AlN/GaN MIS diodes. The conductance technique for determination of the trap states in a MIS capacitor is generally accepted as the most sensitive method [97, 113, 114]. The technique is based on measuring

the equivalent parallel conductance (G_p) of a MIS capacitor as a function of bias voltage and frequency. The conductance, representing the loss mechanism due to interface trap capture and emission of carriers, is a measure of the interface trap state density. A simplified equivalent circuit of a MIS capacitor appropriate for the conductance method is shown in Fig. 4.2.9(a). It consists of the gate dielectric capacitance (C_{ox}), the semiconductor capacitance (C_s), and the interface trap capacitance (C_{it}). The capture-emission of carriers by the trap states is a lossy process, represented by the resistance (R_{it}). It is convenient to replace the circuit in Fig. 6.24(a) with that in Fig. 4.2.9(b), where (C_p) and (G_p) are given by

$$C_p = C_s + \frac{C_{it}}{1+(\omega\tau_T)^2} \tag{4.3}$$

$$\frac{G_p}{\omega} = \frac{q\omega\tau_T D_T}{1+(\omega\tau_T)^2} \tag{4.4}$$

where $C_{it} = q^2 D_T$ (D_T is the trap state density), $\omega = 2\pi f$ (f is the measurement frequency) and the interface trap time constant $\tau_T = R_{it}C_{it}$. Equations (6.3) and (6.4) are for interface traps with a single energy level in the band gap. Interface traps at the dielectric/semiconductor interface, however, are continuously distributed in energy throughout the semiconductor bandgap. Capture and emission occurs primarily by traps located within a few kT/q above and below the Fermi level, leading to a time constant dispersion and giving the normalized conductance as

$$\frac{G_p}{\omega} = \frac{qD_T}{2\omega\tau_T}\ln[1 + (\omega\tau_T)^2] \tag{4.5}$$

Therefore, D_T and τ_T can be extracted by fitting the experimental G_p data using equation 4.5.

Fig 4.2.9 shows the plot of the parallel conductance (G_P/ω) as a function of the radial frequency (ω) for selected gate voltages near the threshold voltage (V_{th}) of the MIS diodes with 7 nm and 3 nm *in-situ* SiN_x. A good fitting was obtained, as demonstrated by the continuous curves in Fig 4.2.10, indicating a good quality of the *in-situ* SiN_x gate dielectric [97, 115].

The trap energy level below the conduction band, designated as the interfacial states (E_T),

can be deduced from τ_T by Shockley–Read–Hall statistics:

$$\tau_T = \frac{1}{v_{th}\sigma_n N_c}\exp(\frac{E_T}{kT}) \tag{4.6}$$

where $N_c = 4.3\times10^{14}\times T^{3/2}$ cm^{-3} is the effective density of states in the conduction band in GaN, $v_{th} = 2 \times 10^7$ cm s^{-1} is the average thermal velocity of electrons and $\sigma_n = 1\times10^{-14}$ cm^2 is the captured cross section of the trap states [95, 115].

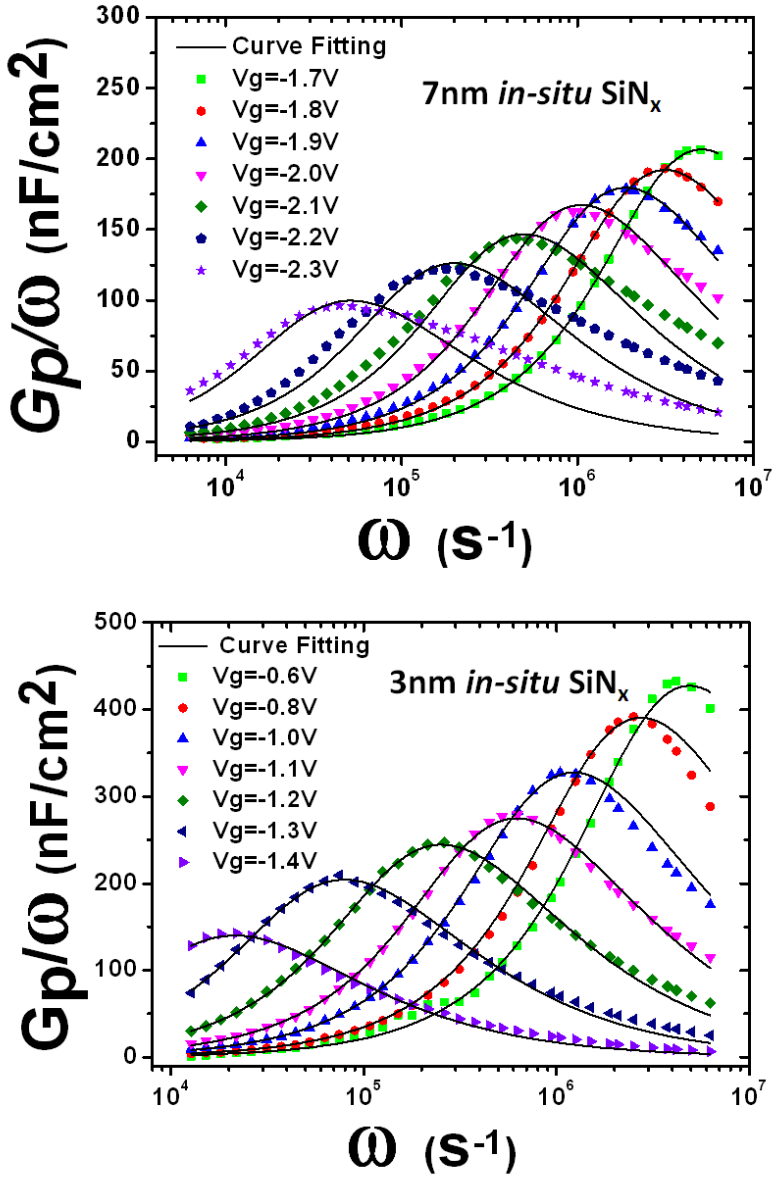

Figure 4.2.10 The frequency dependent parallel conductance as a function of radial frequency for the MIS diodes with 7 nm and 3 nm *in situ* SiN$_x$ biased with selected gate voltages near V_{th}.

The density of the trap states (D_T) as a function of their energy (E_T) for the MIS and MOS

diodes is shown in Fig 4.2.11. The trap states density for the MIS diodes with 7 nm *in-situ* SiN_x decreases from about 7×10^{12} $cm^{-2}eV^{-1}$ at an energy level of 0.31 eV to about 1.2×10^{12} $cm^{-2}eV^{-1}$ at E_T = 0.43 eV. The value is similar to the trap state density of the reference MOS diodes with 7 nm Al_2O_3, but slightly higher than the reported data on conventional Al_2O_3/AlGaN/GaN structures [97]. The relatively high trap states density is believed to stem from the low quality thin barrier layer of the AlN/GaN heterostructures grown on a Si substrate. On the other hand, the trap states density for the MIS diodes with 3 nm *in-situ* SiN_x is about two times higher than that of the MIS diodes with 7 nm *in-situ* SiN_x. This phenomenon has also been observed on Al_2O_3/AlGaN/GaN structures [97] and could be explained by the different surface passivation effects of the SiN_x layers with different thicknesses [116].

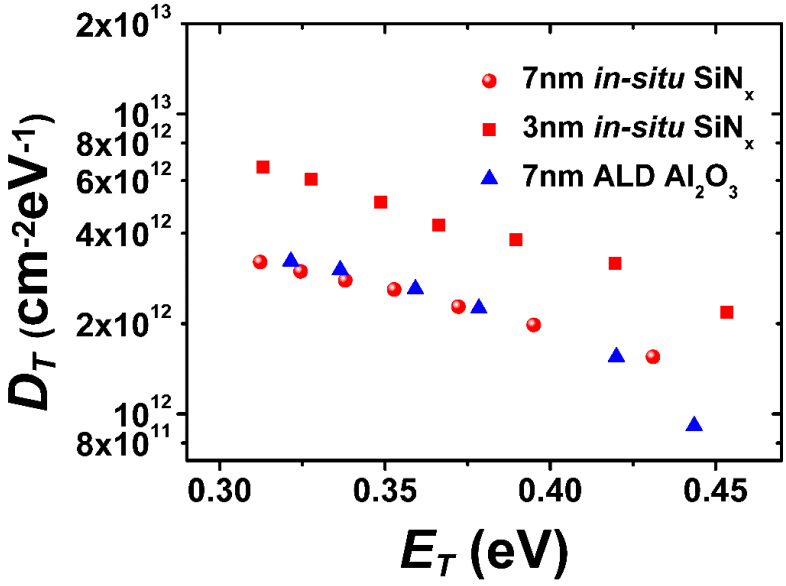

Figure 4.2.11 The trap state density as a function of their energy level depth below the conduction band for the MIS and MOS diodes.

According to TLM measurements, the sheet resistances of the two MISHEMT samples were around 1300 Ω/□ (with 7 nm *in-situ* SiN_x) and 4200 Ω/□ (with 3 nm *in-situ* SiN_x), respectively, which is about one order of magnitude lower than that of the 1.5-nm-barrier GaN/AlN/GaN HEMT sample without surface passivation [81]. To further evaluate the effectiveness of the *in-situ* SiN_x thin film as a passivation layer, the current-voltage (*I-V*)

characterization between the source and drain terminals for all four samples was performed, as shown in Fig 4.2.12. The source-drain spacing was 3 μm. The current density was greatly enhanced by both the *in-situ* SiN_x and Al_2O_3 passivation. The improvement is due to the reduced AlN relaxation, increased carrier concentration and surface protection effects [85]. The different slopes of the saturated current in the cases of the *in-situ* SiN_x and Al_2O_3 passivation can be explained by the different AlN barrier thicknesses and different surface scattering effects, as well as the different surface potential induced by the GaN surface protection layer in the Al_2O_3 MOSHEMT sample, because the current is a strong function of 2DEG density and electron mobility. When comparing the two MISHEMT samples, thicker *in-situ* SiN_x layer led to a higher current density, suggesting better surface passivation effects. A similar phenomenon has also been observed with other dielectrics [85, 116].

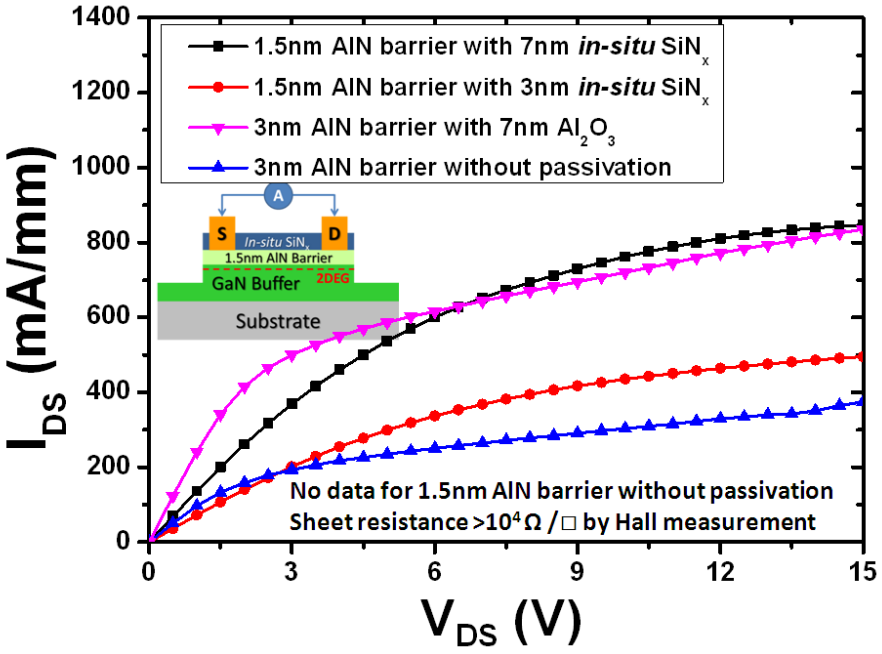

Figure 4.2.12 The *I–V* characteristics between the source and drain terminals. The inset shows the measured schematic with 3 μm source-drain spacing.

The fabricated 1 μm gated MISHEMT with 7 nm *in-situ* SiN_x gate dielectric and 1.5 nm AlN barrier exhibited a peak G_m of 248 mS/mm and a maximum I_{DS} of 730 mA/mm, as shown in Fig 4.2.13. DC-RF dispersion of this MISHEMT was also characterized to verify the effectiveness of the *in-situ* SiN_x passivation. A 500 μs pulsed voltage was applied to the gate,

with the base voltage at −4 V (quiescent bias at pinch-off condition). Negligible current degradation, as shown in the output curve of Fig 4.2.13, confirms the good surface passivation effect of the *in-situ* SiN_x layer. The output characteristics of a 1 μm gated Al_2O_3(7 nm)/GaN(1 nm)/AlN (3 nm)/GaN MOSHEMT are included in Fig 4.2.14 for comparison [85]. The *in-situ* SiN_x/AlN/GaN MISHEMT with thinner barrier (1.5 nm) exhibits a comparable high maximum I_{DS} and smaller current degradation during the gate-pulsed measurement.

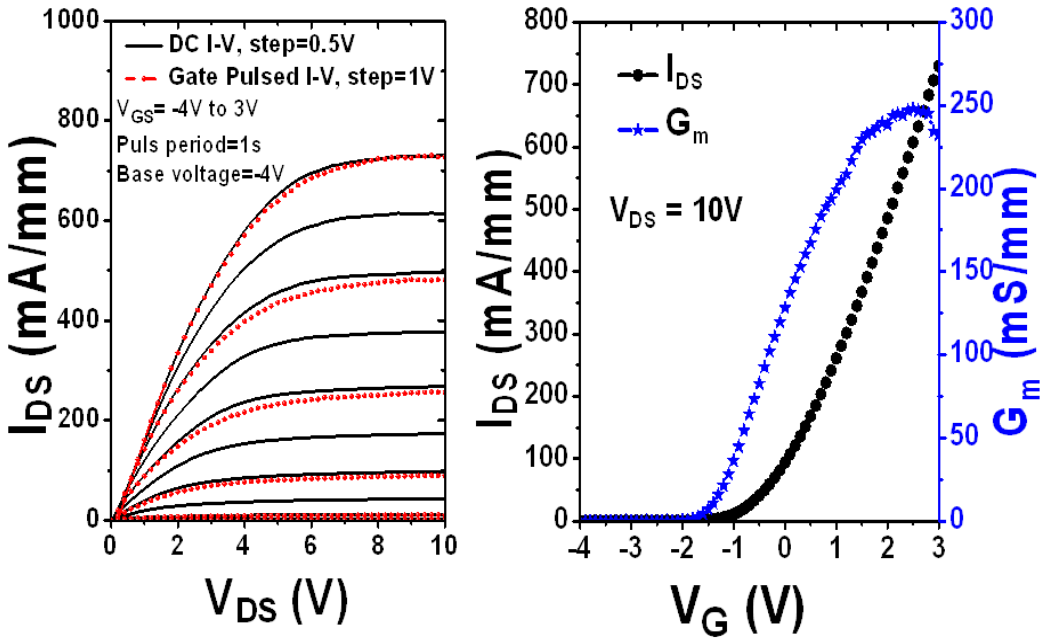

Figure 4.2.13 The gate-pulsed/DC output (left) and transfer (right) characteristics of a 7 nm *in-situ* SiN_x/AlN/GaN MISHEMT with L_G = L_{GS} = L_{GD} =1 μm.

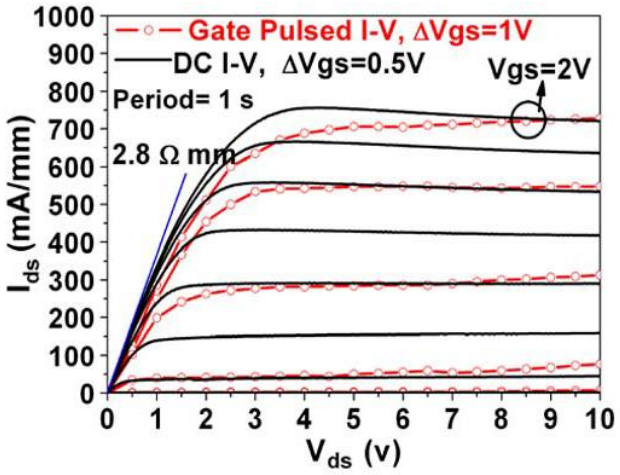

Figure 4.2.14 The gate-pulsed/DC output characteristics of a Al_2O_3(7 nm)/GaN(1 nm)/AlN (3 nm)/GaN MOSHEMT with L_G = L_{GS} = L_{GD} =1 μm [85].

4.3 Investigation of the interfacial trapping effects in *in-situ* SiN_x/AlN/GaN MIS structures grown on sapphire substrates

To achieve a high quality interface for III-nitride MISHEMTs has always been a great challenge, especially for devices with a thin AlN barrier. *In situ* SiN_x has been claimed to be the optimum passivation layer and gate dielectric for III-nitride HEMTs by a number of research groups. However, the investigation of interface trapping effects for *in situ* SiN_x MIS structures is still limited. In our work, the trap state density data for the MIS structures in section 4.2 is not optimum and we believe that the high value stems from the low quality thin barrier layer (only 1.5 nm) of the AlN/GaN heterostructures grown on a Si substrate. This means that the results do not accurately reflect the high quality interface through using an *in situ* SiN_x gate dielectric. Therefore, further work was conducted using sapphire substrates, with increased barrier thickness and optimized growth conditions, to improve the heterostructure quality and minimize the influence of the AlN barrier quality. A thorough study of the interface trapping effects was performed.

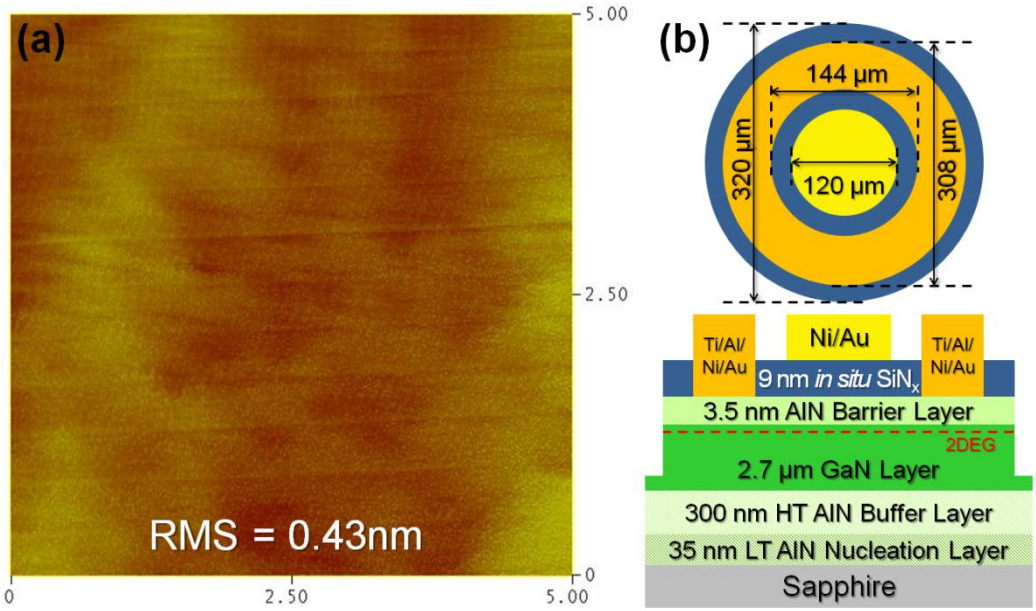

Figure 4.3.1 (a) The AFM image of the as-grown *in-situ* SiN_x/AlN/GaN MISHEMT sample. (b) The architecture of the MIS diode.

The *in-situ* SiN_x/AlN/GaN heterostructures were grown on a 2-inch sapphire substrate in an

AIXTRON2000HT MOCVD system. The epi-layers consist of, from bottom to top, a 35 nm low-temperature AlN nucleation layer, a 300 nm high-temperature AlN buffer layer, a 2.7 μm undoped GaN layer, followed by a 3.5 nm AlN barrier layer and, finally, a 9 nm *in-situ* SiN_x cap layer. An AFM image of the as-grown sample in Fig. 4.3.1(a) shows a smooth surface morphology and the RMS roughness across a 5 μm × 5 μm scanned area is 0.43 nm. Room temperature Hall measurements showed a 2DEG density of 1.41 $\times 10^{13}/cm^2$ with a mobility of 1010 $cm^2/V\,s$, corresponding to a sheet resistance of 438 Ω/□. The smooth surface morphology and high 2DEG mobility demonstrate the high quality of the *in-situ* SiN_x/AlN/GaN heterostructures in this work. Fig. 4.3.1(b) schematically shows the architecture of the MIS diode used for electrical characterization.

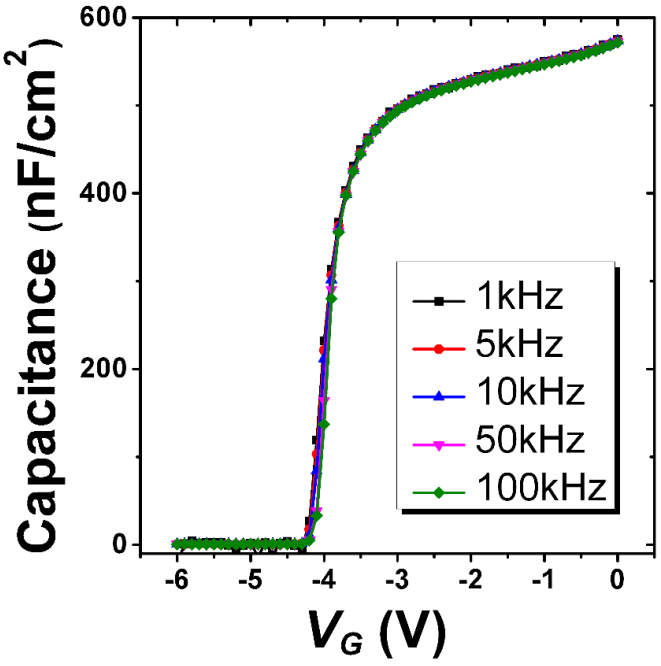

Figure 4.3.2 The multiple frequency *C–V* characteristics of the *in-situ* SiN_x/AlN/GaN MIS diode.

Fig. 4.3.2 shows the multiple frequency *C–V* characteristics of the *in-situ* SiN_x/AlN/GaN MIS diode. Sharp rising slopes with small frequency dispersion between 1 and 100 kHz can be observed, suggesting a high quality interface between the *in-situ* SiN_x gate dielectric and the AlN barrier. The *C-V* curves in Fig. 4.3.2 shows less saturation in the accumulation region. This is an indication of barrier accumulation, where the electrons start to transfer into the

barrier of the heterostructure [95, 117].

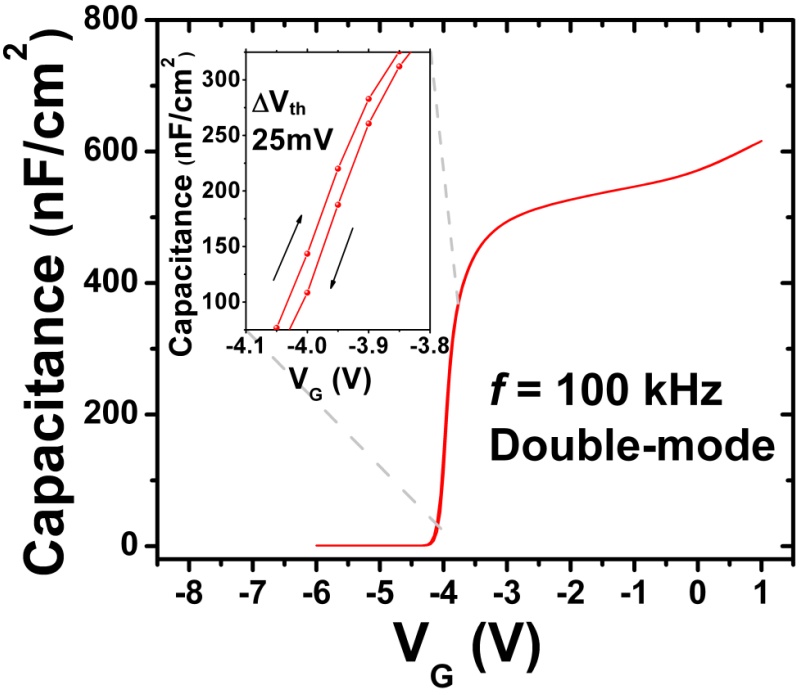

Figure 4.3.3 Double mode *C-V* characteristics of the *in-situ* SiN_x/AlN/GaN MIS diode. The inset gives the enlarged plot showing the hysteresis.

The double-mode *C-V* curves of the *in-situ* SiN_x/AlN/GaN MIS diode are plotted in Fig. 4.3.3. The measurements were set up with an up-and-down sweep rate of 0.05 V/s and a voltage variation of 50 mV at 100 KHz. As shown in the inset of Fig. 4.3.3, the clockwise hysteresis (ΔV_{th}) is as small as 25 mV when the maximum forward voltage in the sweep is at +1V. Such hysteresis can be attributed to the acceptor-like states in the dielectrics or at the dielectric/barrier interfaces with a relatively long emission time constant [93, 95, 117]. Using

$$D_T = C_{MIS} \cdot \Delta V_{th}/e \tag{4.7}$$

we estimate the density of "slow" trap states in the MIS diode to be as low as 1×10^{11} $cm^{-2}eV^{-1}$. This value is significantly lower than the reported results on Al_2O_3/(GaN)/AlGaN/GaN MIS devices [93-95]. The time constant of this "slow" trap state is larger than 100 s.

Fig. 4.3.4 shows the plot of the parallel conductance (G_P/ω) as a function of the radial frequency (ω) for selected gate voltages near the V_{th} of the MIS diode. The trap states

exhibited short time constants in the range between 0.5 μs and 60 μs and were designated as "fast" trap states. The density of the "fast" trap states (D_T) as a function of their energies (E_T) for the *in-situ* SiN_x/AlN/GaN MIS diode is shown in Fig 4.3.5. The density drops sharply from about $1.85\times10^{12}cm^{-2}eV^{-1}$ at an energy of 0.32 eV to about $1.32\times10^{11}cm^{-2}eV^{-1}$ at E_T = 0.44 eV. These values are significantly lower, by over one order of magnitude, than the trap state densities reported on similar (GaN)/AlN/GaN MIS structures using other *ex situ* deposited gate dielectrics in the literature [89, 98, 103]. Trap state density plots for the conventional (GaN)/AlGaN/GaN architecture capped with Al_2O_3 [96] are also included in Fig. 4.3.5 for comparison. Even with a barrier composed of pure AlN, the *in-situ* SiN_x-passivated MIS structure in this work exhibits a low trap state density comparable to the much more mature AlGaN/GaN MIS structures using an Al_2O_3 gate dielectric. It should be noted that the previous high trap state density values for the *in situ* SiN_x/AlN/GaN MIS structure in section 4.2 might have stemmed from the lower quality thin barrier layer of the AlN/GaN heterostructures grown on a Si substrate. In this work, the influence of the AlN barrier quality was minimized by using sapphire substrates, with increased barrier thickness and optimized growth conditions for the heterostructure. Therefore, a fairly high quality interface was achieved.

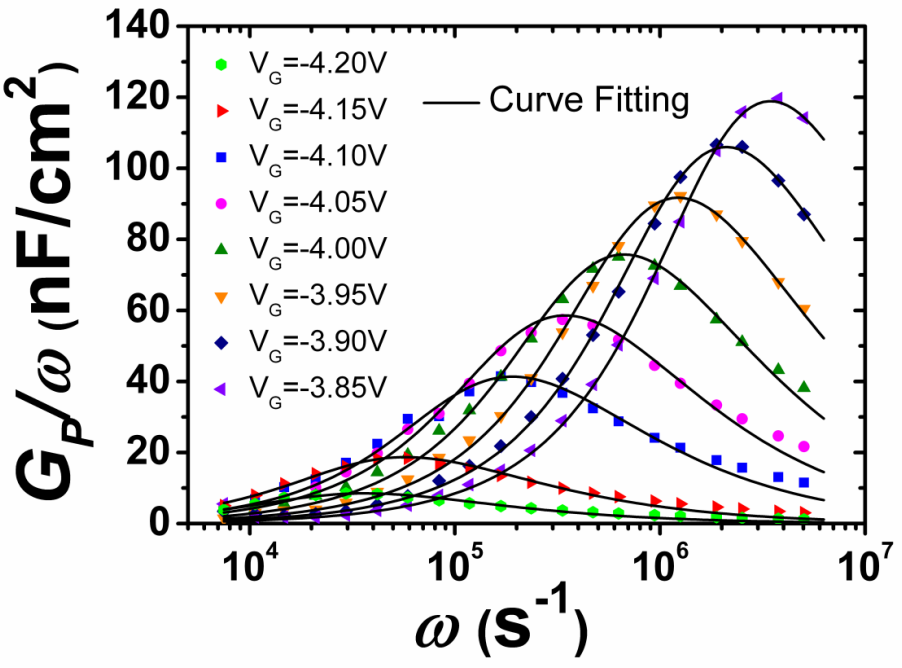

Figure 4.3.4 Frequency dependent parallel conductance as a function of radial frequency for the MIS diode biased at selected gate voltages near V_{th}.

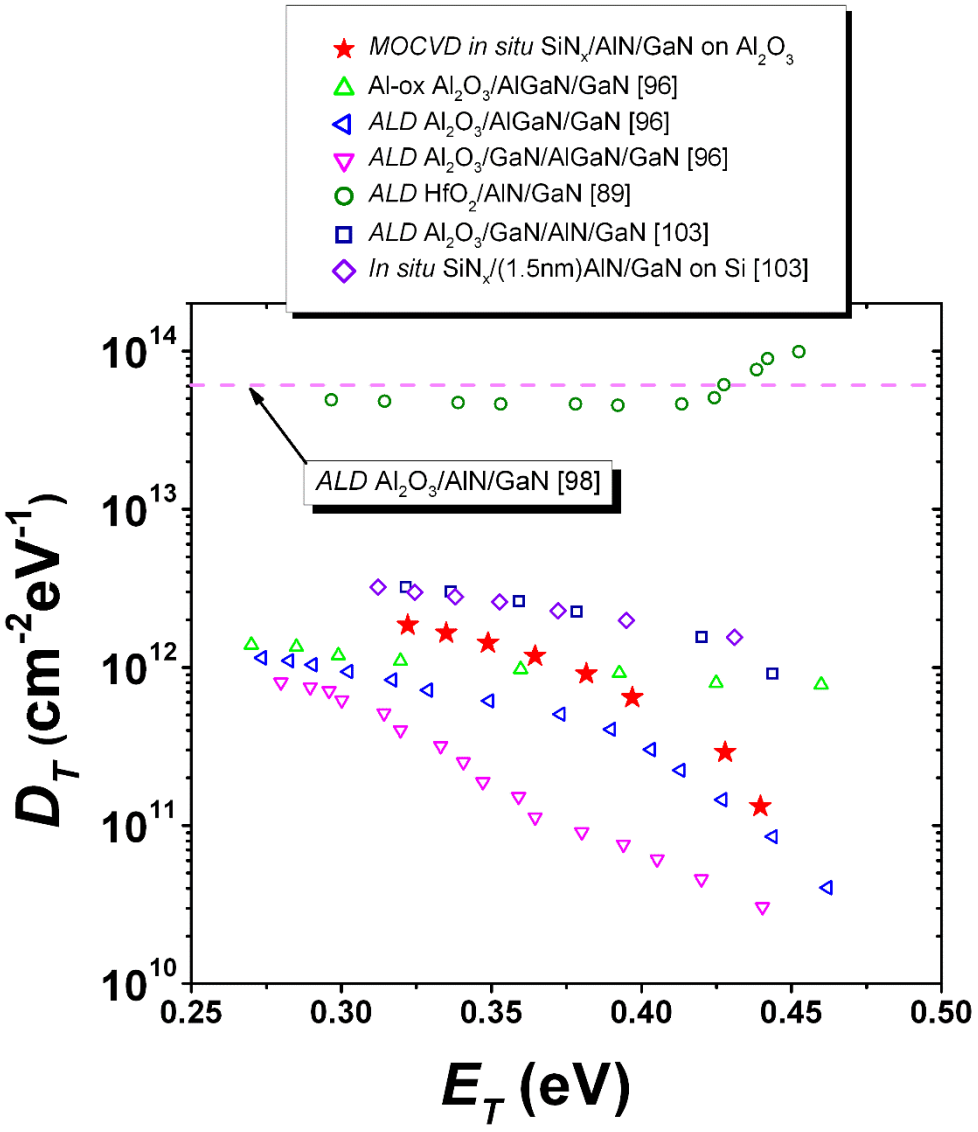

Figure 4.3.5 Trap state densities of the MIS diodes as a function of the energy level depth below the conduction band.

The abruptness of the dielectric/semiconductor interface has a profound impact on the trapping effects in MIS devices. Fig. 4.3.6 shows cross-sectional TEM images of the gate stack of the *in-situ* SiN_x/AlN/GaN MIS sample. The images were taken near the GaN [$1\bar{1}00$] zone axis. A 9-nm-thick *in situ* SiN_x layer was observed to grow uniformly on top of the AlN, as shown in Fig. 4.3.6 (a). Under high magnification, one could observe that the SiN_x/AlN interface exhibits excellent abruptness without any extra interfacial layers in between (see Fig. 4.3.6 (b)). This is in sharp contrast to other III-N MIS devices, which usually possess a rough interface or an irregular interfacial layer [94, 118]. The high-quality SiN_x/AlN interface in this

work can be attributed to the *in situ* high-temperature growth of the SiN_x layer. While the *in-situ* process prevents the direct exposure of the AlN surface to air, the high-temperature growth reduces the density of the unpassivated dangling bonds on the AlN surface through enhanced surface migration of SiN_x adatoms. The smooth and abrupt interface indicates that the *in-situ* SiN_x can effectively protect the AlN barrier from strain relaxation, surface oxidation and damage during the subsequent device fabrication process.

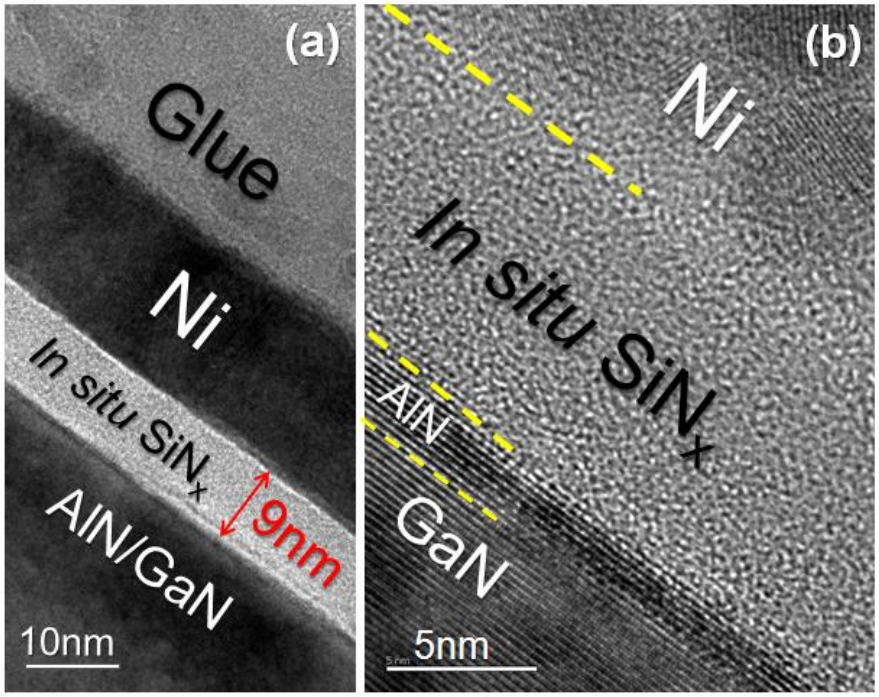

Figure 4.3.6 Cross-sectional TEM images of the gate stack showing the *in-situ* SiN_x/AlN/GaN architecture.

To examine the chemical composition profiles at the SiN_x/AlN interface, a 300-nm AlN on sapphire sample capped with 9 nm *in-situ* SiN_x was grown and probed by XPS. By sputter removal of materials from the surface with argon, we obtained a series of depth-resolved XPS spectra. Figure 4.3.7 (a), (b) and (c) reveal the spectra at depths of around 5 nm, 8 nm and 12 nm, respectively. The binding energy measurement at the sample surface was calibrated by correcting the adventitious C 1s peak to 285 eV. To study the bonding states of N and Al across the interface, we performed peak fitting on the N 1s and Al 2p core-level spectra. It was found that the peak distances between the Al 2p (Al-N, Al-O) and N 1s (Si-N, Al-N) remain the same

for different depths, and the peak positions agree well with the reported results for SiN_x and AlN in the literature. In the N 1s spectrum taken at the SiN_x/AlN interface (i.e. ~ 5 and 8 nm below the surface), two components corresponding to the Si-N bond and Al-N bond were identified. The Si-N peak drops significantly across the interface and finally disappears completely in the bulk AlN layer (i.e., ~ 12 nm below the surface). The Al 2p spectra, on the other hand, are composed of two components arising from the Al-N bond and Al-O bond at all three depths. In particular, the intensities of the strong Al-N peak and weak Al-O peak remain constant at all depths. The oxygen concentrations at different depths of the *in situ* SiN_x/AlN sample are all less than 4%, while the oxygen concentration at the exposed AlN surface is as high as 15.14% for an AlN sample without any surface passivation. Therefore, the oxide-related peaks in Fig. 4.3.6 are believed to stem from the oxygen incorporation in the AlN bulk during growth rather than post-growth oxidation of the AlN surface. These results show that the *in-situ* growth of SiN_x brought no obvious effects on the chemical bonding states of the AlN barrier layer. This is distinctly different from *ex-situ* deposition of gate dielectrics during which exposure to air and/or plasma can induce chemical degradations including composition change, binding energy drift and formation of native oxides in the semiconductor [94, 108]. Thus, the *in-situ* grown SiN_x layer can indeed effectively passivate the AlN surface from oxidation and damage, leading to a high quality *in-situ* SiN_x/AlN interface.

The XPS analysis also revealed that the *in-situ* SiN_x in this study exhibits a N/Si ratio (1.29) closer to the ideal value of 1.33 compared with the previously reported values (1.21 and 1.25) [100, 108]. This can be attributed to the high temperature and NH_3 vapor pressure which promote the incorporation of N into the amorphous film. The higher N content can effectively suppress the formation of Si dangling bonds and distorted excess Si-Si bonds, leading to fewer midgap defect states or bulk traps. This improved stoichiometry is a key factor for the significantly reduced hysteresis in the double-mode *C-V* measurement and hence the remarkably low “slow” trap states density [93, 104, 117, 118].

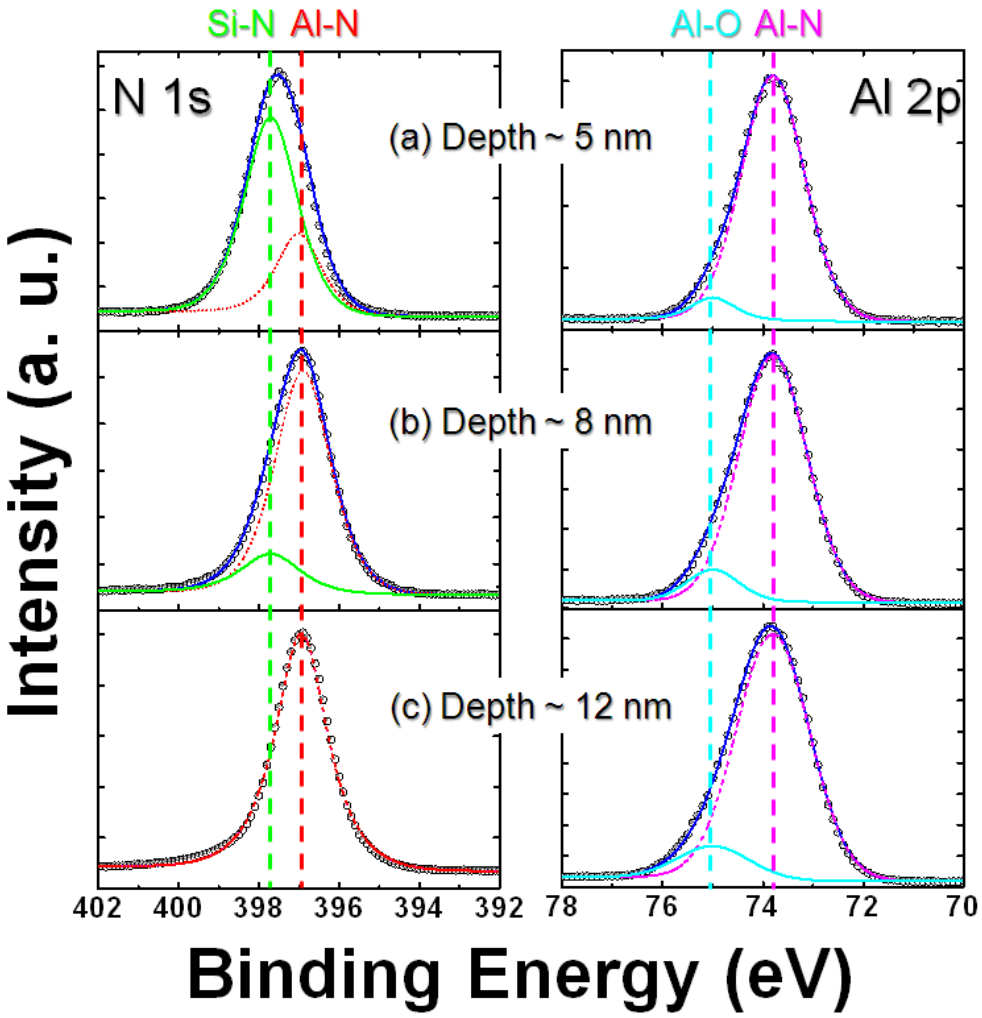

Figure 4.3.7 The N 1s and Al 2p core-level XPS spectra at three different depths from the surface.

4.4 Summary

In this study, *in-situ* SiN_x by MOCVD was employed as the gate dielectric for thin-barrier AlN/GaN MISHEMTs. The MOCVD grown *in-situ* SiN_x on AlN/GaN heterostructures was investigated by AFM, TEM, XPS and electrical characterization of MIS diodes. The *I-V* and *C-V* characteristics of the *in-situ* SiN_x/AlN/GaN MIS diodes exhibited a high resistivity of > 10^{14} Ω cm and a breakdown field of 5.7 MV/cm for the 7 nm *in-situ* SiN_x film and revealed a high effective dielectric constant of ~8.3. Two dominant types of trap states, designated as "slow" and "fast", were identified and characterized using double-mode *C-V* measurement and

frequency dependent conductance analysis, respectively. Remarkably low densities of trap states have been obtained for the *in situ* SiN_x/AlN/GaN MIS structures grown on sapphire substrates. The density of the "slow" trap states (τ_T > 100 s) was as low as 1×10^{11} $cm^{-2}eV^{-1}$, and the density of the "fast" trap states (0.5 μs < τ_T < 60 μs) decreased sharply from about $1.85\times10^{12}cm^{-2}eV^{-1}$ at an energy of 0.32 eV to about $1.32\times10^{11}cm^{-2}eV^{-1}$ at E_T = 0.44 eV.

The achieved results demonstrate the feasibility of *in-situ* SiN_x as a gate dielectric for high performance AlN/GaN MIS devices.

CHAPTER 5 FABRICATION AND CHARACTERIZATION OF GATE-LAST SELF-ALIGNED *IN-SITU* SiN_x/ALN/GAN MISHEMTS

5.1 Introduction

Progress in the gate-last self-aligned device fabrication process and the material growth of *in-situ* SiN_x/AlN/GaN heterostrcture has been demonstrated in Chapter 3 and Chapter 4. These technologies enabled the fabrication of high performance *in-situ* SiN_x/AlN/GaN MISHEMTs, as promising candidates for the next-generation RF and microwave wave power applications [82]. The competitive advantages of the developed MISHEMTs are as follows:

1. Advanced gate-last self-aligned architecture: Regrown n^+-GaN S/D was incorporated to minimize contact resistance. The gate-to-regrown-S/D distances were precisely self-defined by the SiN_x sidewall spacers, leading to reduced access resistance, and a low-κ BCB supporting layer was employed under the gate head to minimize the parasitic capacitance for high frequency operation.
2. High quality gate dielectric and good interface: The *in-situ* SiN_x gate dielectric was grown at high temperature (1145℃) immediately following the AlN/GaN heterostructure growth in the same MOCVD chamber. The AlN barrier was never exposed; thus oxidation/contamination of the AlN surface from air exposure or damage during the device fabrication process was avoided. In addition, the *in-situ* SiN_x gate dielectric was of high quality because of the sufficiently high growth temperature and the low growth rate.

In real applications, the small signal equivalent circuit model for a transistor is essential for reliable circuit design. Moreover, the accurate device modeling and parameter extraction can provide insights into the role of various parameters in the RF performance of a device. For further development of the gate-last self-aligned MISHEMTs technology, it is crucial to analyze their small signal equivalent circuit model and obtain valuable feedback in order to facilitate the device structure and process optimization [43, 119-121].

GaN-based electronic devices, inherently featuring a wide bandgap and smaller intrinsic carrier concentration, can deliver the excellent capability of operating at high temperatures [122]. In order to fully explore the potential of a device operating at high temperature, it is important to evaluate its high temperature behavior [123-126].

This chapter describes the processing and characteristics of the gate-last self-aligned *in-situ* SiN_x/AlN/GaN MISHEMTs. Small signal equivalent circuit modeling for the fabricated MISHEMTs was performed, and excellent agreement between the simulation and measurement was achieved. Additionally, the effect of temperature on the DC and RF performances of the gate-last self-aligned MISHEMTs was studied from RT up to 550 K. The thermal evolution of the main device parameters, such as I_{DS}, G_m, C_{gs}, C_{gd} and R_{ds}, was also investigated and discussed in this chapter.

5.2 Fabrication of the gate-last self-aligned *in-situ* SiN_x/AlN/GaN MISHEMTs

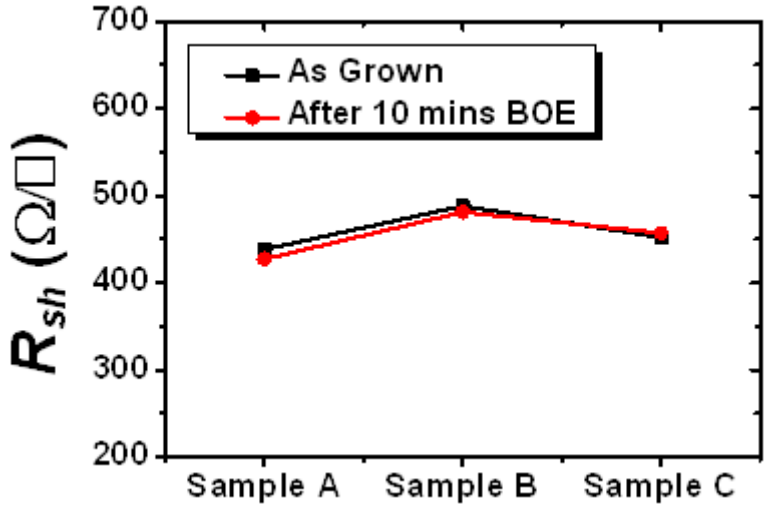

Figure 5.2.1 The R_{sh} of three *in-situ* SiN_x/AlN/GaN MISHEMT samples before and after 10 minutes BOE immersion.

The *in-situ* SiN_x/AlN/GaN heterostructures were grown on a 2-inch sapphire substrate, with an AlN barrier and *in-situ* SiN_x gate dielectric of 3 nm and 7 nm, respectively. The sustainability of the *in-situ* SiN_x gate dielectric with BOE is of great importance for this gate-last self-aligned process since the SiO_2 dummy gate has to be completely removed using

BOE. The etch rate of *in-situ* SiN_x by BOE was found to be extremely slow [99], which is attributed to the high growth temperature of 1145 ℃ in our experiment. No obvious degradation occurred for the *in-situ* SiN_x surface even after 10 minutes BOE immersion of the sample. In addition, RT Hall measurements for three samples before and after the BOE immersion were performed. As shown in Fig. 5.2.1, the sheet resistance (R_{sh}) remained the same for all three samples, indicating a high sustainability of the *in-situ* SiN_x gate dielectric with BOE.

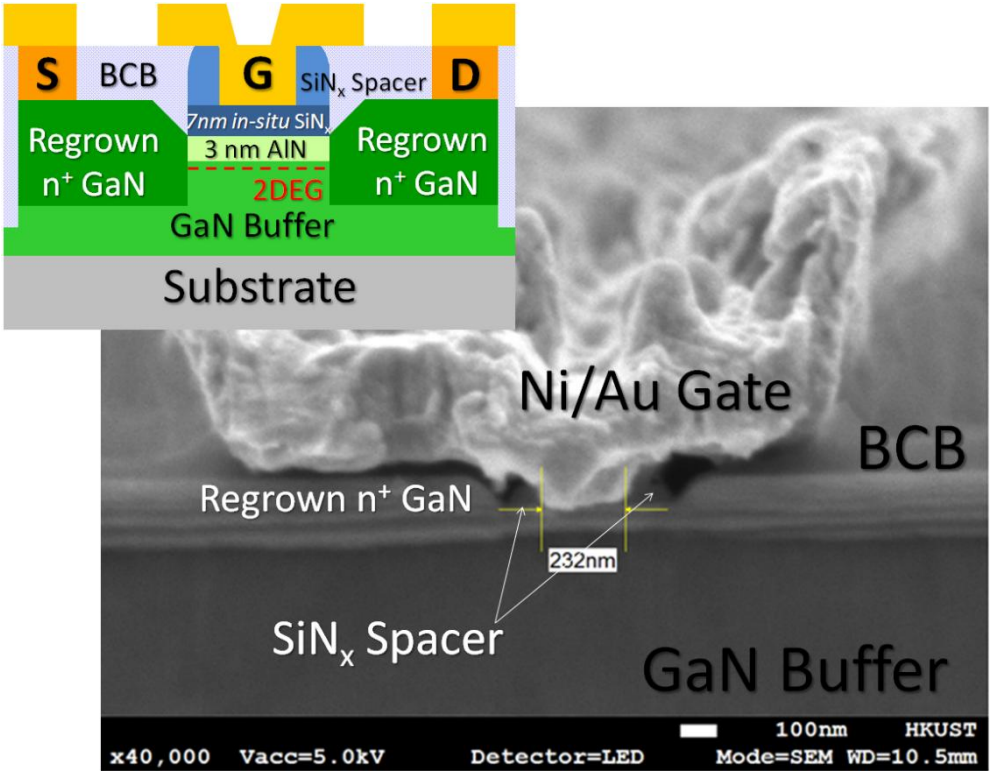

Figure 5.2.2 The cross-sectional SEM image of the gate region for a 0.23 μm gated MISHEMT. The inset shows the device architecture.

A cross-sectional SEM image of the gate region for a 0.23 μm gated device is shown in Fig. 5.2.2. The inset shows the architecture of the gate-last self-aligned *in-situ* SiN_x/AlN/GaN MISHEMT. The thickness of the S/D regrown n^+-GaN is 180 nm. Fig. 5.2.3(a) shows an AFM image of the regrown n^+-GaN across a scanned area of 5 μm × 5 μm. The RMS roughness value is 0.375 nm, and there are no pin holes on the surface. The metal/n^+-GaN contact resistance (R_c), the sheet resistance of the n^+-GaN (R_{sh1}), the regrowth interface resistance

(R_{in}) and the sheet resistance of the 2DEG channel (R_{sh2}) are 0.313 Ω mm, 157 Ω/□, 0.102Ω mm and 662 Ω/□, respectively, as determined by the TLM measurements in Fig. 5.2.3 (b) [81]. A high Si doping level of about 6×10^{19} cm^{-3} was deduced for the regrown n^+-GaN layer, which is desirable for reduction of the access resistance in high speed devices.

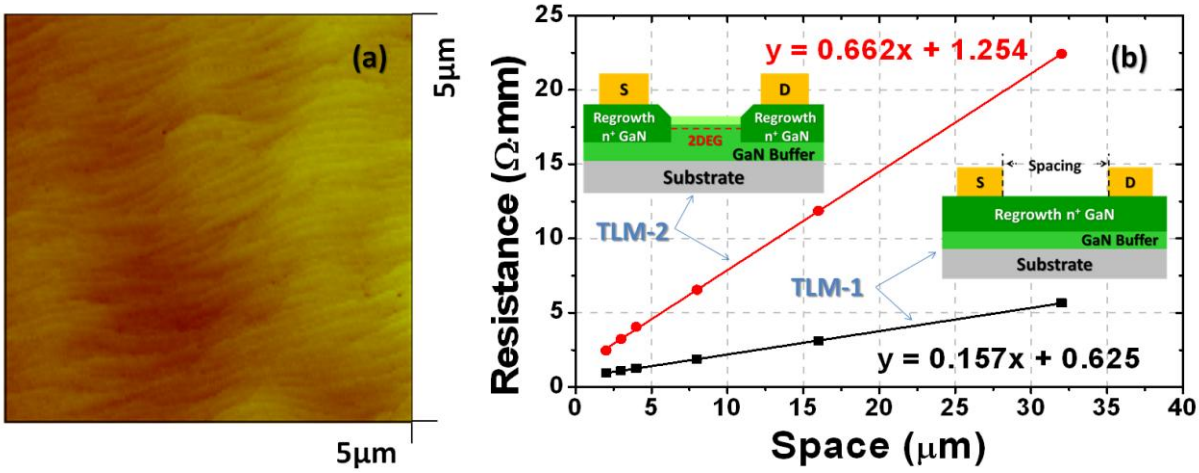

Figure 5.2.3 The AFM image (a) and TLM results (b) of the regrown n^+-GaN S/D.

5.3 DC and RF characterization at RT

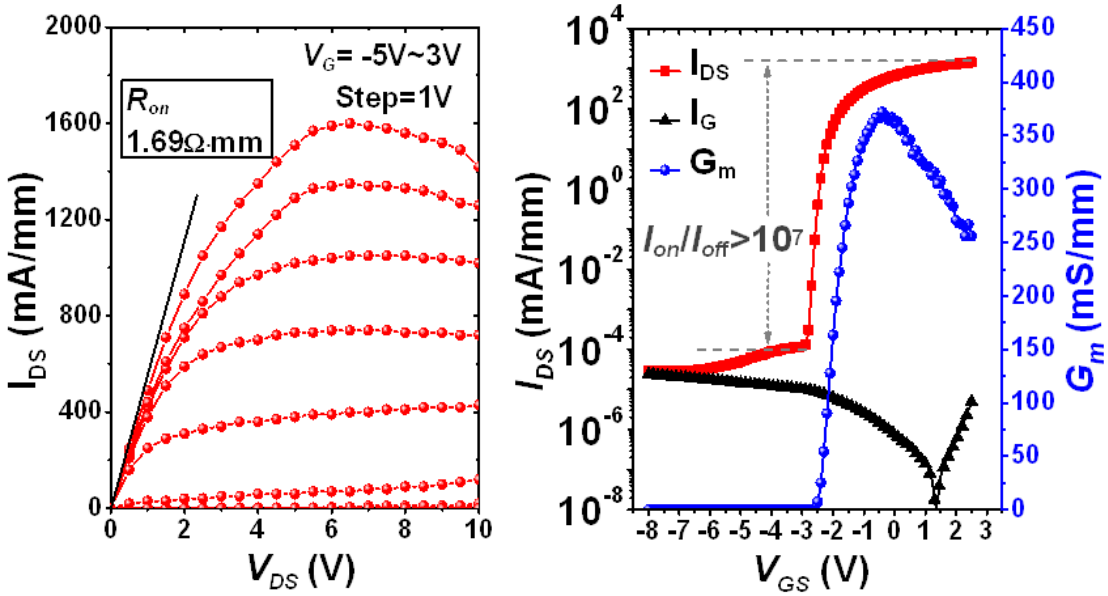

Figure 5.3.1 DC output and transfer characteristics of the MISHEMT with L_G = 0.23 μm and W_G = 2 × 50 μm.

Fig. 5.3.1 shows the RT DC characteristics of the 0.23 μm gated MISHEMT with a gate width (W_G) of 2 ×50 μm. The device exhibites a high maximum I_{DS} of 1600 mA/mm at V_{DS} = 6 V and V_{GS} = 3 V, and the R_{on} is as low as 1.69 Ω mm. The peak G_m is 372 mS/mm at V_{DS} = 6 V and V_{GS} = -0.5 V. The achieved results are mainly attributed to the reduction of access resistance by the heavily doped S/D regrowth as well as the scaled self-aligned L_{GS}/L_{GD}. Moreover, the device presents both gate leakage and off-state drain leakage below 10^{-4} mA/mm at V_{GS} = -8 V and V_{DS} = 6 V, resulting in a large I_{on}/I_{off} of over 10^7. This indicates that the high quality *in-situ* SiN_x was very effective in suppressing the leakage current and protecting the AlN surface.

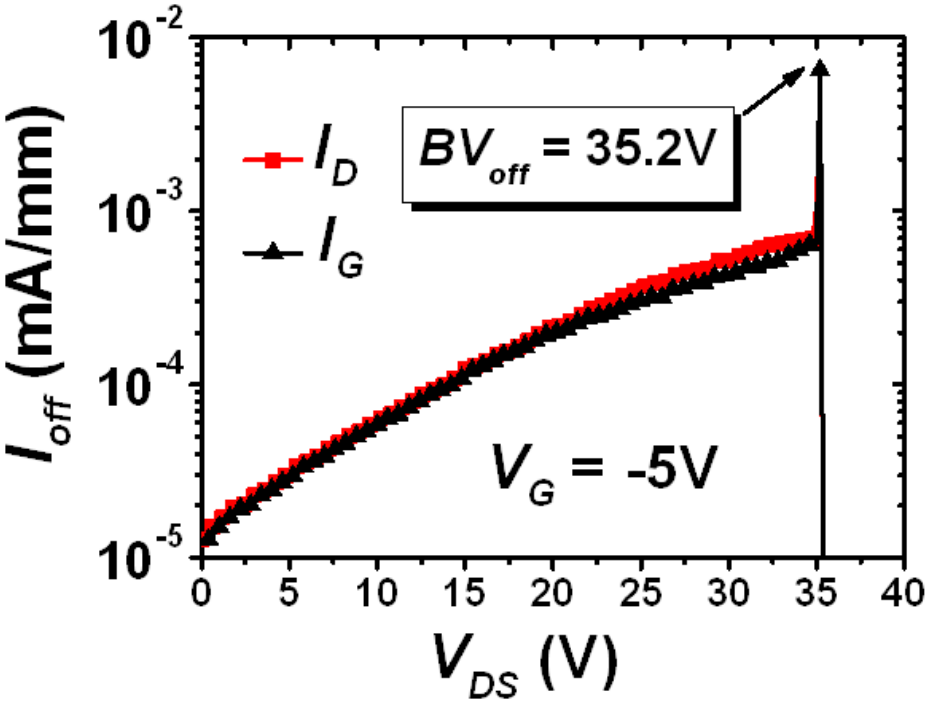

Figure 5.3.2 The three-terminal off-state breakdown characteristics of a gate-last self-aligned MISHEMT at V_{GS} = -5 V

The three-terminal off-state breakdown characteristics of the gate-last self-aligned MISHEMTs at V_{GS} = -5 V are plotted in Fig. 5.3.2. The device with L_{GD} = 90 nm features a BV_{off} in excess of 35 V. The BV_{off} is limited by catastrophic gate-drain breakdown and a breakdown field of 4.46 MV/cm can be deduced, which is well above the critical breakdown field of GaN. This is attributed to the high quality *in-situ* SiN_x gate dielectric used in the devices.

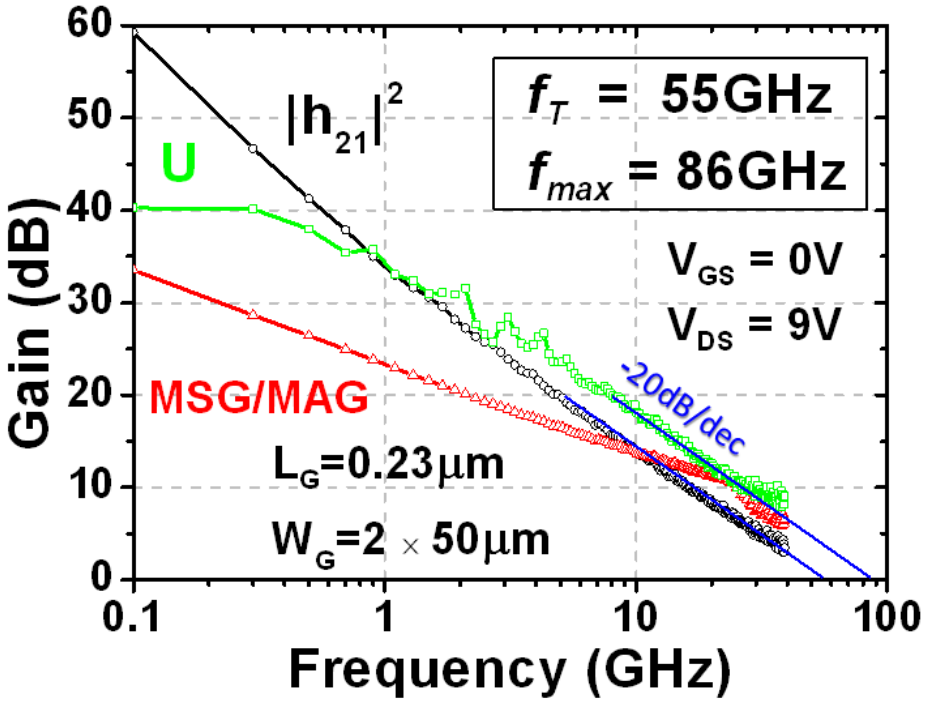

Figure 5.3.3 Small signal RF characteristics of the MISHEMT with L_G = 0.23 μm and W_G = 2 × 50 μm showing peak f_T and f_{max} of 55 and 86 GHz, respectively.

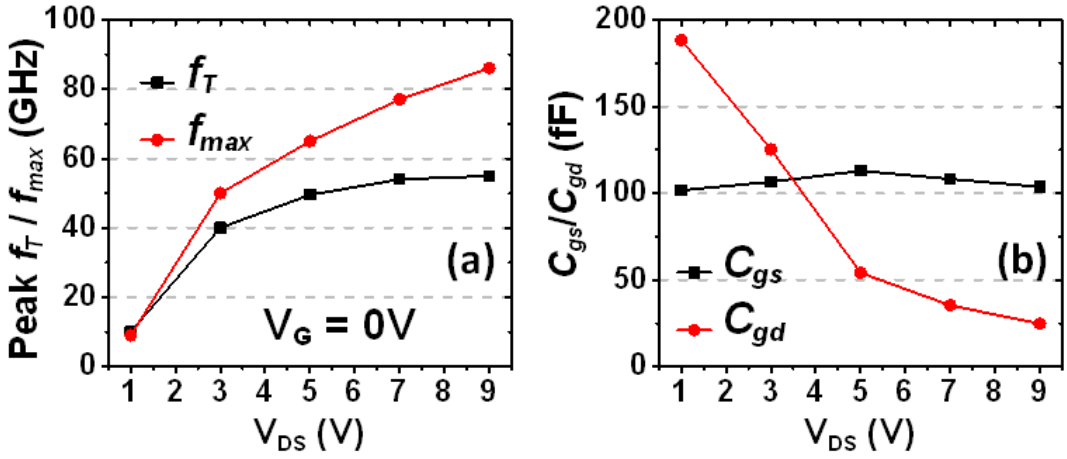

Figure 5.3.4 The peak f_T, f_{max} (a) and C_{gs}, C_{gd} (b) as a function of V_{DS} for the MISHEMT with L_G = 0.23 μm and W_G = 2 × 50 μm.

Fig. 5.3.3 shows the RF characteristics of the 0.23 μm gated device measured at the maximum f_T bias conditions (V_{DS} = 9 V, V_{GS} = 0 V) and at RT. A simultaneously high f_T and f_{max} of 55 and 86 GHz, respectively, was obtained by extrapolating the current gain ($|h_{21}|^2$) and unilateral power gain (U) using a −20 dB/dec slope. The peak f_T, f_{max} and gate capacitances (C_{gs} and C_{gd}) as a function of V_{DS} for the measured 0.23 μm device are plotted in Fig. 5.3.4.

The f_T continuously increases with V_{DS} until approaching the maximum value at V_{DS} = 7 V. This suggests that the drain depletion length and therefore the drain delay, which typically increase with V_{DS}, were suppressed in this self-aligned architecture [64, 69, 72].

To further understand the effects of various delay components on the device RF performance, delay time analysis was conducted for the 0.23 μm gated MISHEMT [69, 72, 127]. The total delay time in the device is defined as:

$$\tau_{total} = \frac{1}{2\pi f_T} \tag{5.1}$$

The total delay time consists of the parasitic delay time ($\tau_{parastic}$), the channel charging time ($\tau_{channel}$) and the electron transit time ($\tau_{transit}$), classified on the different sources of the delays through the device:

$$\tau_{total} = \tau_{parasitic} + \tau_{channel} + \tau_{transit} \tag{5.2}$$

The parasitic delay time was estimated to be ~0.4 ps, using

$$\tau_{parasitic} = C_{gd} \cdot (R_s + R_s) \tag{5.3}$$

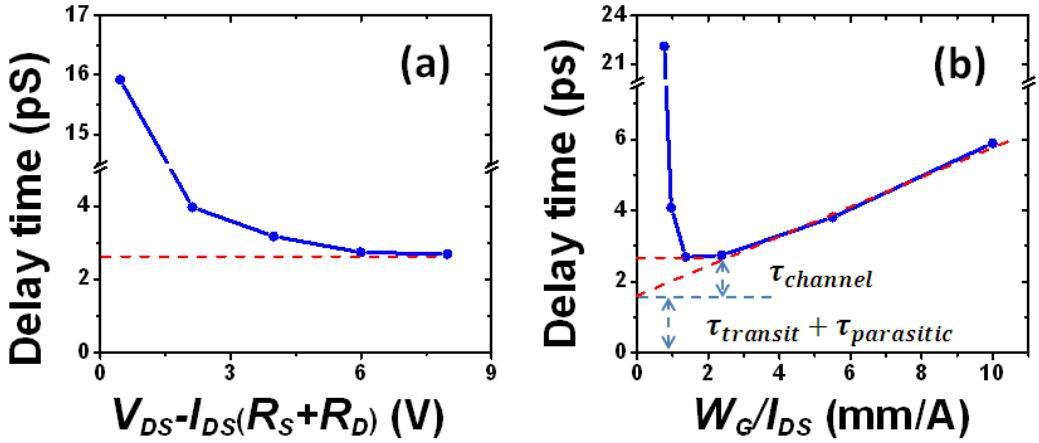

Figure 5.3.5 The delay time as a function of voltage across the channel (a) and the delay time as a function of reciprocal drain current density (b).

The electron transit time is the sum of the gate transit time and drain delay time, which is mainly determined by the electron velocity, the gate length and the drain depletion width. In

Fig 5.3.5(a), the total delay time is plotted as a function of voltage across the channel [$= V_{DS} - I_{DS}(R_s + R_d)$] for the 0.23 μm gated device. The delay time is nearly constant with increasing V_{DS}, suggesting that the drain depletion length and therefore the drain delay were suppressed in this self-aligned architecture. Thus, it is difficult to independently extract gate transit time and drain delay time from Fig 5.3.5(a) [72]. Fig 5.3.5(b) shows the dependence of the total delay time on the normalized gate width to drain current (W_G/I_{DS}). The linearly extrapolated delay time at zero is a combination of the parasitic delay time and the electron transit time. Thus the channel charging time was extracted to be ~1 ps and the electron transit time was ~1.3 ps.

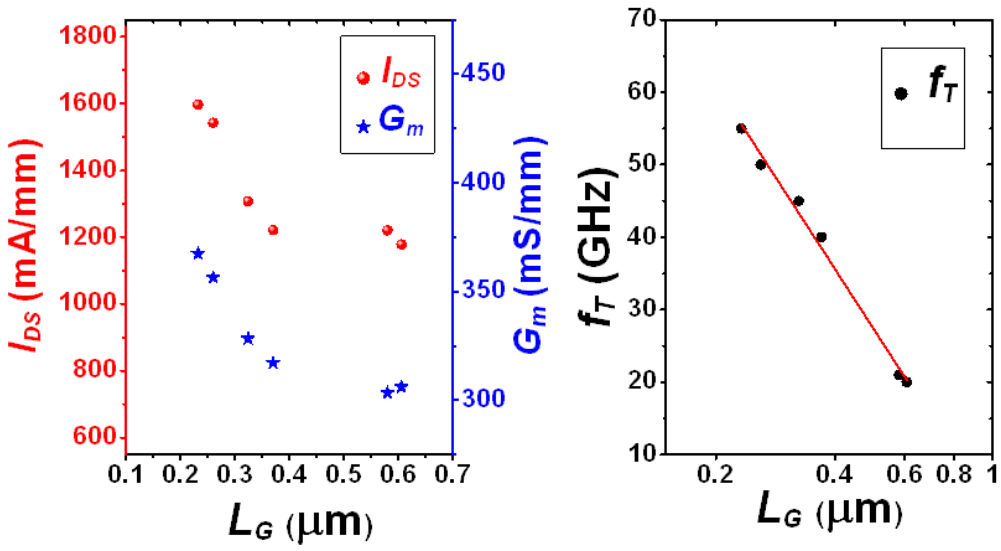

Figure 5.3.6 Scaling behavior of I_{DS}, G_m and f_T with respect to L_G for the gate-last self-aligned MISHEMTs.

Fig. 5.3.6 plots the typical scaling behavior of the maximum I_{DS}, peak G_m and f_T with respect to L_G for the gate-last self-aligned MISHEMTs. The best $f_T \times L_G$ product obtained on a 0.32 μm gated device was 14.6 GHz·μm, among the reported values for state-of-the-art GaN HEMTs in the literature [64-66, 79, 80, 86, 128]. The f_T scales as $1/L_G$, demonstrating the advantages of this gate-last self-aligned architecture in reducing the parasitic effects. However, the gate-last self-aligned MISHEMTs in this first demonstration are less than fully scaled, limited by the currently used photolithography technique. There are significant gate transit delay and large parasitic components in the devices, due to the relatively large L_G, L_{SD}, and the big gate head. To

further scale down the device dimensions, an e-beam lithography technique and a single step dry etch process will be required to define and pattern the SiO_2 dummy gate.

The T-gate geometry requires careful optimization for a deeply scaled device, since the gate capacitance has a great impact on the device RF performance [64, 74]. Due to the relatively high permittivity surrounding the gate, a device fabricated using a self-aligned approach will unfortunately have larger parasitic gate fringing capacitance than the conventional T-gate structure, whose gate is surrounded by air. However, a surface passivation layer and a supporting layer under the gate head are desirable when taking into consideration the reliability issues and interconnection requirements. In fact, even when L_G scales down to 30 nm, the extra gate fringing capacitance induced by the dielectrics surrounding the gate will still not dominate the device performance. It has been reported that the f_T for devices with a relatively high-κ SiN_x or SiON gate surrounding was only ~ 23% lower when compared with that of the devices after removing the gate surrounding dielectrics [66, 71]. One can expect that using low-κ dielectrics under the gate head could further reduce the parasitic gate fringing capacitance. Moreover, the gate region of the MISHEMT in this work is covered and protected by a SiO_2 dummy gate throughout the whole process until the final metal gate deposition. Therefore, the use of organic BCB at front end of line will not introduce much contamination to the device. Therefore, the proposed gate-last self-aligned technology using low-κ BCB in this work would be an alternative technology, balancing the device performance, reliability, and process complexity.

5.4 Small signal equivalent circuit modeling

To further investigate the device characteristics, small signal equivalent circuit model elements were extracted for the 0.23 μm gated *in-situ* SiN_x/AlN/GaN MISHEMT. The 15-element small signal equivalent circuit model described in Chapter 1 was implemented, as shown in Fig. 5.4.1.

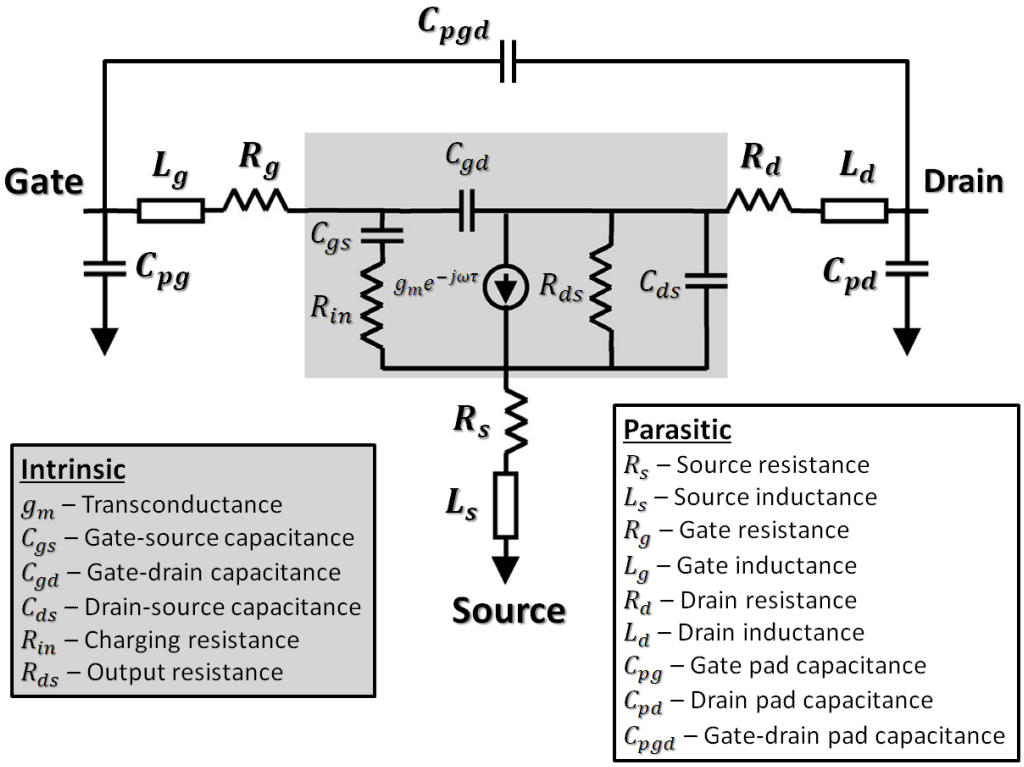

Figure 5.4.1 The 15-element small signal equivalent circuit model.

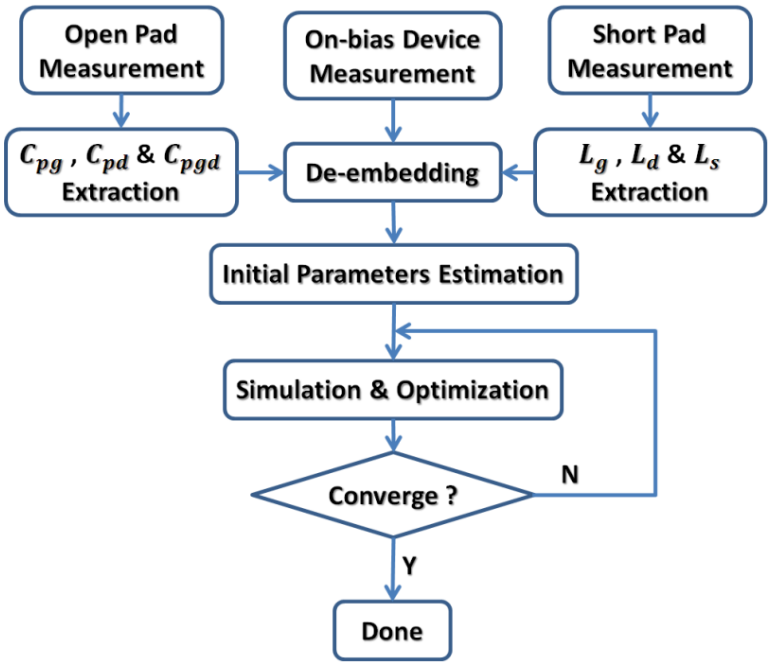

Figure 5.4.2 The flowchart shows the approach of small signal equivalent circuit modeling.

The extraction approach relies on intimate knowledge of the device architecture and the fabrication process. Firstly, the pad capacitances and inductances were extracted from the

measured S-parameters of the open and short pad structures. Secondly, the source and drain access resistances were estimated using the TLM test structures, while the gate resistance was estimated from the gate geometry. Then, on-bias device S-parameter measurement was conducted. After de-embedding, the intrinsic elements were estimated analytically [129]. Finally, the whole estimated equivalent circuit model was simulated and optimized in the Advanced Design System (ADS) software to fit the measured S-parameter. The flowchart in Fig. 5.4.2 depicts the parameter extraction approach.

5.4.1 Extrinsic Parameters Extraction

The parasitic pad capacitances were extracted from the measurement of an open pad structure, as shown in Fig. 5.4.3(a). Fig. 5.4.3(b) shows its π-network equivalent circuit. The Y-parameter of this equivalent circuit can be written as

$$Y_{11} = j\omega(C_{pg} + C_{pgd}) \tag{5.4}$$

$$Y_{12} = y_{21} = -j\omega(C_{pgd}) \tag{5.5}$$

$$Y_{22} = j\omega(C_{pd} + C_{pgd}) \tag{5.6}$$

Fig. 5.4.4 shows the imaginary part of the Y-parameter data of the open pad structure, converted from the measured S-parameter. It clearly shows a capacitive behavior. The linear fitting of the curves gives C_{pg} = 32.2 fF, C_{pd} = 31.6 fF, and C_{pgd} = 5.2 fF.

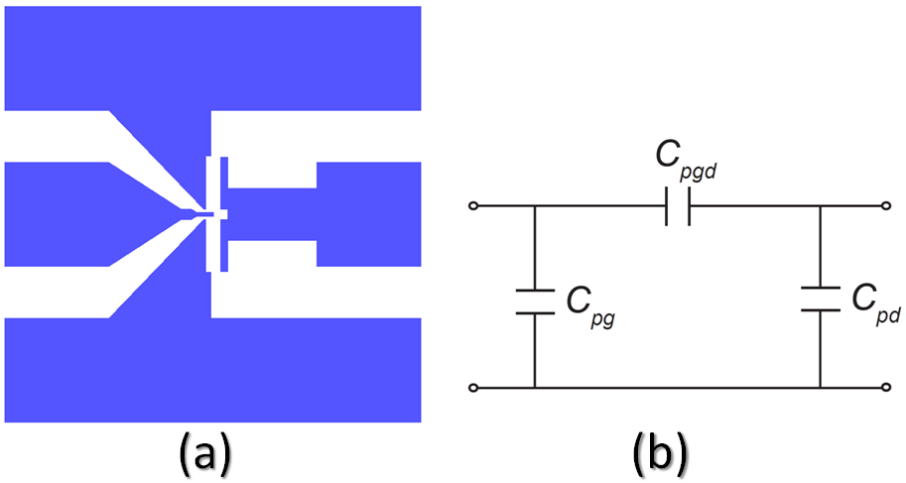

Figure 5.4.3 (a) Open pad structure and (b) its π-network equivalent circuit.

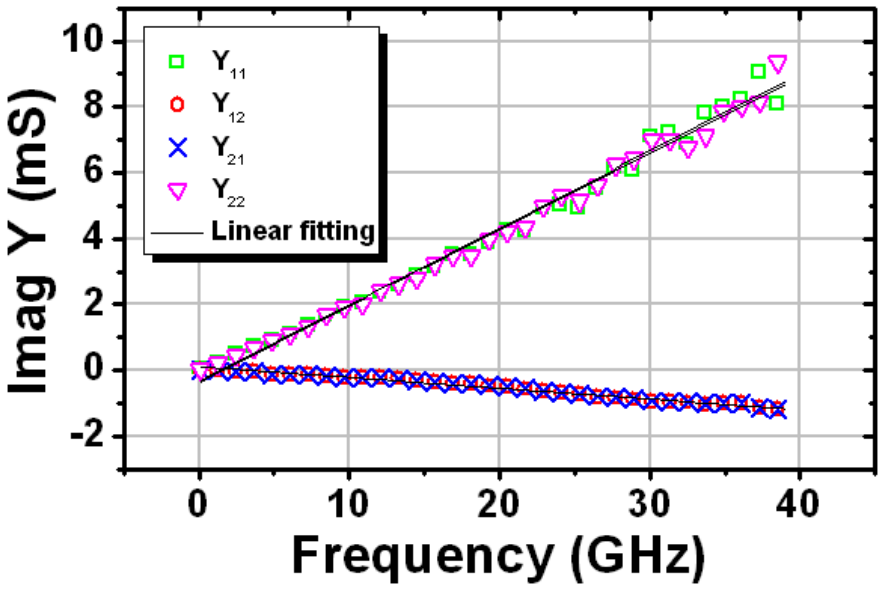

Figure 5.4.4 Imaginary part of the measured Y-parameter data of the open pad structure.

Similarly, the parasitic pad inductances were extracted from the measurement of an short pad structure, as shown in Fig. 5.4.5(a). Fig. 5.4.5(b) shows its T-network equivalent circuit. The Z-parameter of this equivalent circuit can be written as

$$Z_{11} = j\omega(L_g + L_S) \tag{5.7}$$

$$Z_{12} = j\omega(L_S) \tag{5.8}$$

$$Z_{22} = j\omega(L_d + L_S) \tag{5.9}$$

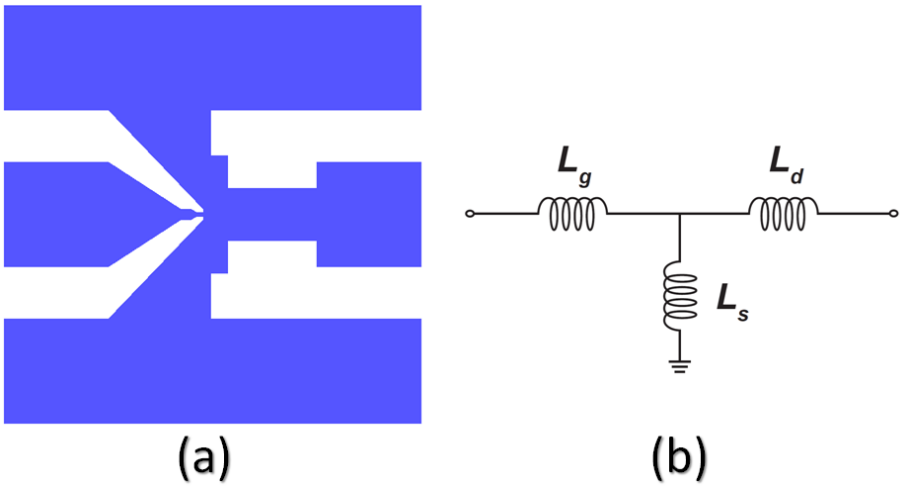

Figure 5.4.5 Short pad structure and (b) its T-network equivalent circuit.

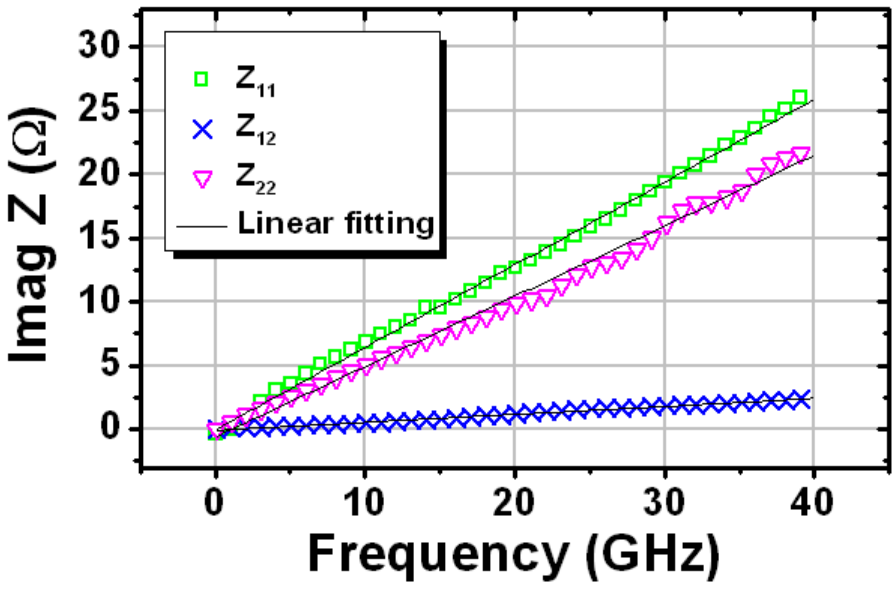

Figure 5.4.6 Imaginary part of the measured Z-parameter data of the short pad structure.

Fig. 5.4.6 shows the imaginary part of the Z-parameter data of the short pad structure, converted from the measured S-parameter. It clearly shows an inductive behavior. The linear fitting of the curves gives L_g = 93.3 pH, L_d = 77.9 pH, and L_s = 9.9 pH.

The total series S/D resistances (R_s and R_d) consist of three parts: the metal/n^+-GaN contact resistance (R_c), the sheet resistance of the n^+-GaN (R_{sh}) and the regrowth interface resistance (R_{in}), as expressed by

$$R_s = R_d = \frac{R_c}{W_G} + R_{sh}\frac{L_{GS}}{W_G} + \frac{R_{in}}{W_G} \tag{5.10}$$

where R_c, R_{sh} and R_{in} were determined by the TLM measurements previously and were 0.313 Ω mm, 157 Ω/□ and 0.102Ω mm, respectively. The gate-to-regrown S/D distance (L_{GS}) and the gate width (W_G) were 1.9 μm and 100 μm, respectively. Therefore, the R_s and R_d were estimated to be around 7.1Ω.

The MISHEMT gate resistance was estimated by applying the following expression

$$R_g = \frac{1}{3}\cdot\frac{W_G}{nL_G h}\cdot\rho \tag{5.11}$$

where W_G is the gate width , n is the number of gate fingers, L_G is the gate length, h is the thickness of the gate metal, ρ is the resistivity of the gate metals and the factor $\frac{1}{3}$ is introduced to account for the distributed RC effects at high frequency [130]. Thus, the R_g

was approximately 1.2Ω. There will be some error associated with this calculation due to the uncertainties in the fabrication process, such as the line width, spacing and the material thickness.

5.4.2 Intrinsic Parameters Estimation

The parasitic capacitances and inductances were then de-embedded from the measured S-parameter of the MISHEMT. The impedances of L_g, L_d and L_s were subtracted from the Z-parameter of the device, while the admittances of C_{pg}, C_{pgd} and C_{pd} were deducted from the resultant Y-parameter after conversion [131]. The resulting Y-parameter is uniquely related to the intrinsic elements, which can then be calculated analytically [129], as follows

$$C_{gd} = -\frac{-Im\,(Y_{12})}{\omega} \tag{5.12}$$

$$C_{gs} = \frac{Im\,(Y_{11})-\omega C_{gd}}{\omega}\left\{1 + \frac{[Re\,(Y_{11})]^2}{\left[Im(Y_{11})-\omega C_{gd}\right]^2}\right\} \tag{5.13}$$

$$C_{ds} = -\frac{Im\,(Y_{22})-\omega C_{gd}}{\omega} \tag{5.14}$$

$$R_{in} = \frac{Re\,(Y_{11})}{\left[Im(Y_{11})-\omega C_{gd}\right]^2+[Re\,(Y_{11})]^2} \tag{5.15}$$

$$g_m = \sqrt{\left\{[Re\,(Y_{21})]^2 + \left[Im(Y_{21}) + \omega C_{gd}\right]^2\right\}\left(1 + \omega^2 {C_{gs}}^2 {R_{in}}^2\right)} \tag{5.16}$$

$$\tau = \frac{1}{\omega}\cdot arcsin\left(\frac{-\omega C_{gd}-Im(Y_{21})-\omega C_{gs}R_{in}Re(Y_{21})}{g_m}\right) \tag{5.17}$$

$$R_{ds} = \frac{1}{Re(Y_{22})} \tag{5.18}$$

Once the intrinsic elements were determined, the whole estimated model was simulated in ADS and optimized to fit the measured S-parameter. A good agreement between the simulated and measured S-parameters from 0.1 to 39 GHz was achieved, as shown in the Smith chart in Fig. 5.4.7, suggesting the high reliability of the model topology and approach used in this work for determining the element values. Table 5-1 lists the optimum values of the extracted model elements for the gate-last self-aligned *in-situ* SiN_x/AlN/GaN MISHEMT.

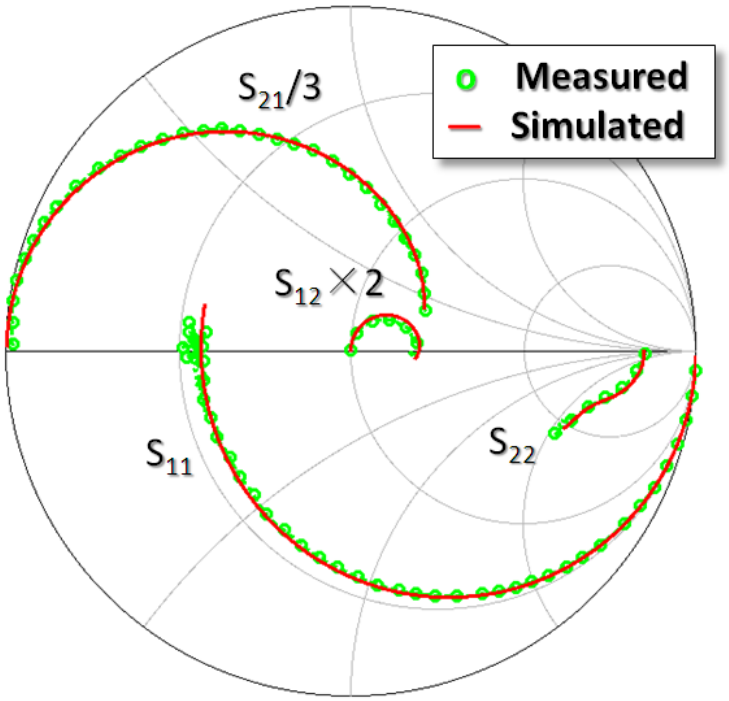

Figure 5.4.7 Smith chart shows the simulated and measured S-parameters of the 0.23 μm gated *in-situ* SiN_x/AlN/GaN MISHEMT.

Table 5-1 The small signal equivalent circuit model elements of the *in-situ* SiN_x/AlN/GaN MISHEMT (L_G = 0.23 μm and W_G = 2×50 μm) at V_{GS} = 0 V and V_{DS} = 9 V.

Intrinsic Parameters		Extrinsic Parameters	
g_m (mS/mm)	417	C_{pg} (fF)	28.1
C_{gs} (fF/mm)	1011	C_{pd} (fF)	35.7
C_{ds} (fF/mm)	117	C_{pgd} (fF)	6.3
C_{gd} (fF/mm)	161	L_g (pH)	78
R_{in} (Ω mm)	0.21	L_d (pH)	103
R_{ds} (Ω mm)	39.7	L_s (pH)	22.5
τ (ps)	0.5	R_g (Ω mm)	0.51
		R_d (Ω mm)	0.65
		R_s (Ω mm)	0.38
$f_{T,model}$ (GHz)	**54.1**	$f_{max,model}$ (GHz)	**87.3**

5.5 Thermal evolution of the device DC and RF performance

To investigate the influence of temperature on the device performance for the gate-last self-aligned MISHEMTs, high temperature (up to 550 K) DC and RF characterizations were performed for a 0.58 μm gated MISHEMT with a W_G of 2 × 50 μm.

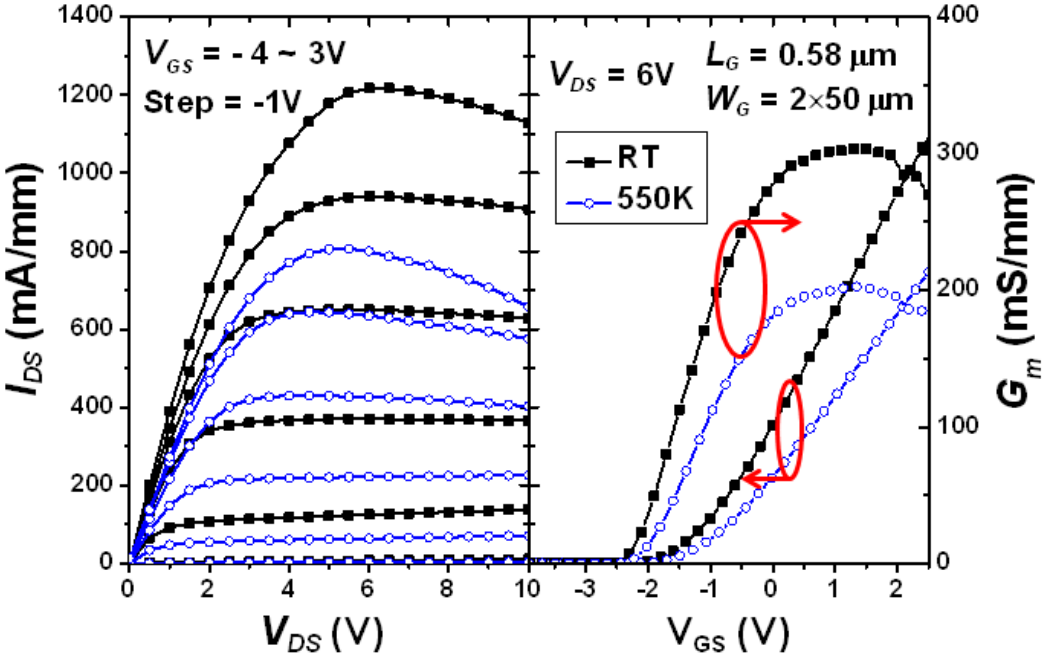

Figure 5.5.1 DC output and transfer characteristics of the MISHEMT with L_G = 0.58 μm and W_G = 2 × 50 μm at RT and 550 K

Fig. 5.5.1 shows the measured DC output and transfer characteristics at RT and 550 K. The maximum I_{DS} and peak G_m values are reduced by ~ 33 % between RT (I_{DS} = 1220 mA/mm and G_m = 303 mS/mm) and 550 K (I_{DS} = 810 mA/mm and G_m = 202 mS/mm), mainly due to the decrease in the electron mobility and drift velocity [123-125].

The thermal evolution of f_T and f_{max} as a function of V_{GS} at V_{DS} = 7 V is shown in Fig. 5.5.2(a). From RT to 550 K, the maximum of f_T (at V_{GS} = 1 V at V_{DS} = 7 V) moves linearly with temperature from 21.1 to 12.7 GHz, leading to a temperature dependent rate (α) of -33.3 MHz/K, as shown in Fig. 5.5.2(b). This value is lower than the results previously reported (~ -46 MHz/K) for the conventional T-gate AlGaN/GaN HEMTs on SiC [123], indicating good thermal stability of the gate-last self-aligned *in-situ* SiN_x/AlN/GaN MISHEMTs in this work. A

similar phenomenon has been also observed for f_{max}, which drops from 44.8 GHz at RT to 19.3 GHz at 550 K with $\alpha \approx$ - 102.6 MHz/K. On the other hand, the BCB can only handle up to 350 ℃, which is far below the limitation of GaN-based devices. To further develop its potential, other low-k thermal stable materials, such as porous SiO_2, could be employed as a supporting layer for GaN-based MISHEMTs.

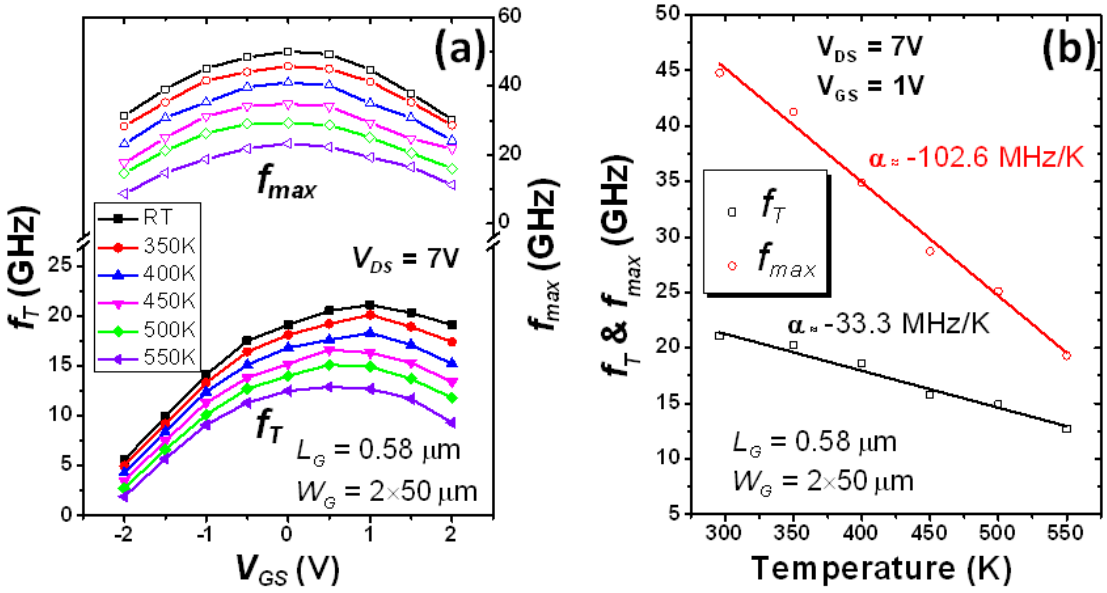

Figure 5.5.2 (a) The thermal evolution of f_T and f_{max} as a function of V_{GS} at V_{DS} = 7 V. (b) The dependence of f_T and f_{max} on the ambient temperature at V_{GS} = 1 V at V_{DS} = 7 V.

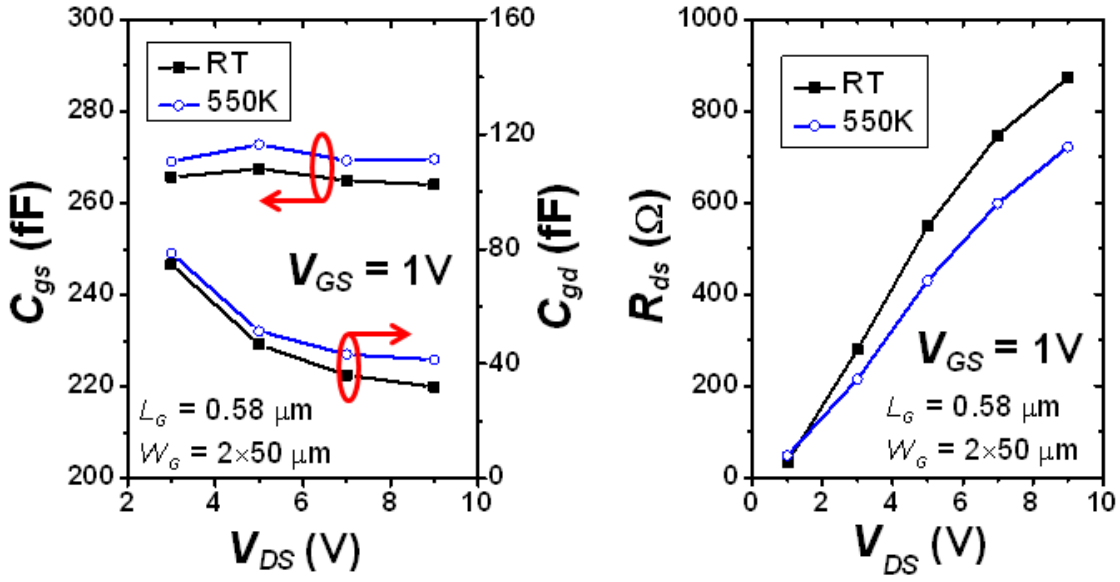

Figure 5.5.3 The thermal dependence of C_{gs}, C_{gd} and R_{ds} as a function of V_{DS}.

It was found that both f_T and f_{max} showed higher relative reduction between RT and 550 K (~ 40 % and ~ 57 %, respectively) when compared with the I_{DS} and G_m (~ 33 %), which is probably related to the change of intrinsic capacitances (C_{gs} and C_{gd}) and resistance (R_{ds}) with temperature. The C_{gs}, C_{gd} and R_{ds} directly affect the device RF performances, according to Equation 1.5 and 1.8. As shown in Fig. 5.5.3(a), both C_{gs} and C_{gd} show a slight increase with temperature. This may be explained by the changes of material permittivity and the structure deformations induced in the passivation and channel layers at high temperature [132, 133]. On the other hand, the dependency of R_{ds} on temperature is opposite [see Fig. 5.5.3(b)], which may be related to a lower 2DEG confinement at high temperature. Therefore, the relatively high reduction of f_T and f_{max} at high temperature can be clearly explained.

5.6 Summary

In this work, *in-situ* SiN_x/AlN/GaN MISHEMTs were fabricated using a scalable gate-last self-aligned technology. The device with a L_G of 0.23 μm exhibited a maximum I_{DS} exceeding 1600 mA/mm with a high I_{on}/I_{off} of over 10^7. The f_T and f_{max} were 55 and 86 GHz, respectively. The small signal equivalent circuit model was explored for the fabricated devices and excellent agreement between simulation and measurement was achieved. In addition, the effects of temperature on the DC and RF performances were studied for the MISHEMTs.

The achieved results suggest the potential of the gate-last self-aligned *in-situ* SiN_x/AlN/GaN MISHEMTs for the next-generation high-frequency power applications.

CHAPTER 6 SUMMARY AND SUGGESTED FUTURE WORK

6.1 Summary of the dissertation

Featuring superior material properties, GaN and its alloy compounds have attracted lots of attention for semiconductor device applications, especially in electronic sensing and RF-communication systems. This thesis focuses on the development of novel device and integration technologies for exploration of GaN-based sensors and high-frequency power electronics.

First, high performance Lamb-wave and SAW delay line devices and their monolithically integrated oscillators were designed and fabricated with an MOCVD-grown GaN-on-Si platform. By modifying the device geometries, the second generation Lamb-wave sensors exhibited enlarged signal-to-noise ratio, increased mass sensitivity and improved reliability and fabrication yield. Both of the Lamb-wave and SAW delay line devices were integrated with AlGaN/GaN HEMT circuits to form monolithic oscillators. The discrete SAW delay line device exhibited a high quality factor (Q) of up to 1000 and an excellent power handling capability. The integrated Lamb-wave oscillator was able to deliver high output power (>11 dBm) up to 250 ℃. In addition, the oscillation frequency exhibited a linear dependence on temperature with a small TCF of -47.5 ppm/ ℃ and the frequency drift was less than 1% over a wide temperature range from RT to 230 ℃.

For GaN-based HEMTs, innovative device scaling technologies were explored to improve the device performance. A scalable gate-last self-aligned process was developed by employing S/D regrowth and low-k BCB planarization techniques, which enabled the reduction of access resistance and parasitic capacitance. In contrast to the gate-first self-aligned process, the T-shaped gate formed in this gate-last approach enables high f_T and f_{max} simultaneously. When compared with the conventional T-gate process, this gate-last self-aligned process is less demanding in gate lithography, which can potentially reduce the process complexity and improve the yield.

To further facilitate the device scaling, a thin AlN barrier was preferred, with increased gate control capabilities and maintaining high channel conductivity. *In-situ* SiN_x grown by MOCVD was explored as the gate dielectric for the AlN/GaN MISHEMTs. The *in-situ* SiN_x gate dielectric demonstrated many advantages over other *ex-situ* deposited insulators, including better surface passivation effects, suppression of gate leakage current and the elimination of process- and growth- related defects on the AlN barrier. A high interface quality was achieved for the *in situ* SiN_x/AlN/GaN MIS structure.

Finally, high performance MISHEMTs were fabricated by combining the gate-last self-aligned process and the *in-situ* SiN_x/AlN/GaN heterostrcture. The sub-micron gated device exhibited high level DC and RF performance, such as a maximum I_{DS} exceeding 1600 mA/mm, a high I_{on}/I_{off} of over 10^7 and high f_T and f_{max} of 55 and 86 GHz, respectively. Small signal equivalent circuit modeling for the MISHEMTs was developed and a good agreement between the modeled and measured data was achieved. In addition, the thermal stability of the fabricated MISHEMTs was also studied up to 550 K.

To summarize, novel GaN-based device structures and integration technologies have been demonstrated in this dissertation, for applications in sensors and high-frequency power electronics.

6.2 Suggestions for future work

Although several device structures and integration technologies are proposed and discussed in this thesis, further improvements and investigations can still be made. Tremendous work is needed for further deployment of GaN-based electronics in next-generation sensing and RF-communication systems. The suggestions for future work are summarized as follows:

1. In order to pursue higher f_T and f_{max}, further scaling of the device geometry is desirable. For gate-last self-aligned MISHEMTs, the advanced e-beam lithography technique is needed to pattern a sub-100 nm SiO_2 dummy gate and sub-micron gate head. The short channel effects have to be taken into consideration when a device is highly scaled. Therefore, vertical scaling of the MISHEMTs and inserting back barriers should also be

conducted.

2. Enhancement-mode operation is always preferred for a GaN transistor, because it can simplify the circuits with a single-polarity voltage supply and improve the reliability of the power switches. Reliable techniques for fabrication of E-mode GaN MISHEMTs, such as a fluorine-based plasma treatment or a post-gate annealing, can be studied in the future.
3. Based on the small signal equivalent circuit model, a full device model of the MISHEMTs can be developed for circuit design simulation.
4. More GaN-based functional blocks and integrated circuits, with or without acoustic functions, such as power amplifiers, mixers or even transceivers, can be built.

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Appendix

A. Process flow of Gate-last Slef-aligned *in-situ* SiN_x/AlN/GaN MISHEMTs

Step 0: Starting Sample

In-situ SiN_x/AlN/GaN MISHEMT

Step 1: Wafer Cleaning

Acetone and IPA ultrasonic clean: 5 minutes each

DI water rinse: 4 cycles

Blow dry with N_2 gun

Dehydration bake: 120 ℃ oven, 10 minutes

Step 2: SiO_2 Dummy Gate Formation

2.1 SiO_2 Deposition

STS 310PC PECVD system

Temperature: 300 ℃

Thickness: 3000 Å (Deposition Rate 550 Å /min)

2.2 Photoresist Coating

Photoresist: AZ 703: Ethyl Lactate = 2:1, positive

Spin-coat: 1000 rpm/5 seconds, 4000 rpm/30 seconds

Soft bake: 90 ℃ hotplate, 1 minute

PR Thickness: ~0.6 μm

2.3 Photoresist Exposure and Development

Contact Aligner: Karl Suss MA6

Contact mode: Low vacuum

Exposure time: 2.0 seconds

Post-exposure bake: 110 ℃ hotplate, 1 minute

Developer: FHD-5, 1 minute

DI water rinse: 4 cycles

Blow dry with N_2 gun

2.4 Oxygen Plasma Descum

Chamber O_2 Pressure: 300 mTorr

Temperature: 70 ℃

Duration: 0.7 minute

2.5 SiO_2 Dummy Gate Patterning

Oxford Plasmalab 80 Plus Reactive Ion Etcher

Gas: CHF_3/O_2

Etch rate: 550 Å /min

Hard bake: 120 ℃ oven, 10 minutes

SiO_2 was patterned by BOE dip for 125s at room temperature (Etch rate: 3000 Å /min)

2.6 Photoresist Strip

MS2001, 70 ℃, 5 minute

DI water rinse: 4 cycles

Blow dry with N_2 gun

Step 3: SiN_x Sidewall Spacer Formation

3.1 SiN_x Deposition

STS 310PC PECVD system

Temperature: 300 ℃

Thickness: 900 Å (Deposition Rate 100 Å /min)

3.2 SiN_x Anisotropic Etching

Oxford Plasmalab 80 Plus Reactive Ion Etcher

Gas: CHF_3/O_2

Etch rate: 850 Å /min

Step 4: Source/Drain Regrowth

4.1 S/D Region Recess Etching

STS ICP-Etcher

Gas: BCl_3/Cl_2

Etch depth: 900 Å (Etch Rate 5000 Å/min)

4.2 S/D Regrowth

AIXTRON2000HT MOCVD

Temperature: 1090 ℃

Precursors: TMGA, Amonnia, SiH_4

Regrow thickness: 180 nm

Step 5: Device Isolation

5.1 Photoresist Coating

Photoresist: AZ 703, positive

Spin-coat: 1000 rpm/5 seconds, 4000 rpm/30 seconds

Soft bake: 90 ℃ hotplate, 1 minute

PR Thickness: ~0.9 μm

5.2 Photoresist Exposure and Development

Contact Aligner: Karl Suss MA6

Contact mode: Low vacuum

Exposure time: 4.0 seconds

Post-exposure bake: 110 ℃ hotplate, 1 minute

Developer: FHD-5, 1 minute

DI water rinse: 4 cycles

Blow dry with N_2 gun

5.3 Oxygen Plasma Descum

Chamber O_2 Pressure: 300 mTorr

Temperature: 70 ℃

Duration: 0.7 minute

5.4 Mesa Etching

STS ICP-Etcher

Gas: BCl_3/Cl_2

Etch depth: 2500 Å (Etch Rate 5000 Å/min)

5.5 Photoresist Strip

MS2001, 70 ℃, 5 minute

DI water rinse: 4 cycles

Blow dry with N_2 gun

Step 6: Source/Drain Electrodes Formation

6.1 Photoresist Coating

Photoresist: AZ 703, positive

Spin-coat: 1000 rpm/5 seconds, 4000 rpm/30 seconds

Soft bake: 90 ℃ hotplate, 1 minute

PR Thickness: ~1 μm

6.2 Photoresist Exposure and Development

Contact Aligner: Karl Suss MA6

Contact mode: Low vacuum

Exposure time: 4.0 seconds

Post-exposure bake: 110 ℃ hotplate, 1 minute

Developer: FHD-5, 1 minute

DI water rinse: 4 cycles

Blow dry with N_2 gun

6.3 Oxygen Plasma Descum

Chamber O_2 Pressure: 300 mTorr

Temperature: 70 ℃

Duration: 0.7 minute

6.4 Surface Preparation

HCl : H_2O = 1 : 10, 30 seconds

DI water rinse: 4 cycles

Blow dry with N_2 gun

6.5 Metal Deposition

Peva-600EI evaporation system

Chamber pressure: < 10^{-6} Torr

Metal: Cr/Au (200 Å/2000 Å)

6.6 Lift Off

Soak in Acetone: 10 hours

Acetone spray on surface to remove unwanted metal

Rinse in IPA

DI water rinse: 4 cycles

Blow dry with N_2 gun

Step 7: BCB Planarization

7.1 BCB Coating

CYCLOTENE 3022-35

Adhesion Promoter: AP3000

Spin-coat: 1000 rpm/5 seconds, 4000 rpm/30 seconds

Hard baking: 250 ℃, Vacuum oven, 2.5 hours

Thickness: 1.2 μm

7.1 BCB Etch Back

Oxford Plasmalab 80 Plus Reactive Ion Etcher

Gas: CF_4/O_2

Etch rate: 6000 Å /min

Etch to expose the SiO_2 dummy gate

Step 8: SiO_2 Dummy Gate Removal

Soak in BOE: 10 minutes

DI water rinse: 4 cycles

Blow dry with N_2 gun

Step 9: Gate Metallization

9.1 Photoresist Coating

Photoresist: AZ 703, positive

Spin-coat: 1000 rpm/5 seconds, 4000 rpm/30 seconds

Soft bake: 90 ℃ hotplate, 1 minute

PR Thickness: ~1 μm

9.2 Photoresist Exposure and Development

Contact Aligner: Karl Suss MA6

Contact mode: Low vacuum

Exposure time: 4.0 seconds

Post-exposure bake: 110 ℃ hotplate, 1 minute

Developer: FHD-5, 1 minute

DI water rinse: 4 cycles

Blow dry with N_2 gun

9.3 Oxygen Plasma Descum

Chamber O_2 Pressure: 300 mTorr

Temperature: 70 ℃

Duration: 0.7 minute

9.4 Metal Deposition

Peva-600EI evaporation system

Chamber pressure: < 10^{-6} Torr

Metal: Ni/Au (500 Å/2500 Å)

9.5 Lift Off

Soak in Acetone: 10 hours

Acetone spray on surface to remove unwanted metal

Rinse in IPA

DI water rinse: 4 cycles

Blow dry with N_2 gun

B. Publication list

Journal publications

1. **X. Lu**, J. Ma, H. Jiang, C. Liu, P. Xu and K. M. Lau, “Fabrication and Characterization of Gate-last Self-aligned AlN/GaN MISHEMTs with *in-situ* SiN_x Gate Dielectric”, ***Electron Devices, IEEE Transactions on.*** (Under Review)

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4. **X. Lu**, J. Ma, H. Jiang, and K. M. Lau, "Characterization of *in situ* SiN_x thin film grown on AlN/GaN heterostructure by metal-organic chemical vapor deposition," ***Applied Physics Letters***, 104, 032903, Jan 2014.

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11. T. Huang, Z. Liu, X. Zhu, J. Ma, **X. Lu**, and K. M. Lau, "DC and RF Performance of Gate-Last AlN/GaN MOSHEMTs on Si With Regrown Source/Drain", ***Electron Devices, IEEE Transactions on***, vol.60, Issue 10, August 2013.

12. A. M. H. Kwan, S. Song, **X. Lu**, et al. "Improved Designs for an Electrothermal In-Plane Microactuator," ***Microelectromechanical Systems, Journal of***, ***IEEE***, vol. 21, Issue 3, pp. 586-595, June 2012.

Conference publications

1. **X. Lu**, J. Ma, P. Xu, H. Jiang and K. M. Lau, “High Performance Self-aligned AlN/GaN MISHEMT with In-situ SiNx Gate Dielectric and Regrown Source/Drain,” in ***2014 The International Conference on Compound Semiconductor Manufacturing Technology***, May 2014, Denver, USA.

2. **X. Lu**, J. Ma, Z. Liu, T. Huang, and K. M. Lau, "*In-situ* SiN_x gate insulator by MOCVD for low-leakage-current ultra-thin-barrier AlN/GaN MISHMETs on Si," in ***10th international conference on nitride semiconductors (ICNS-10)***, Aug. 2013, Washington DC, USA.

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