Integration of Low Loss Interconnects in CMOS

by

Salahuddin Raju

A Thesis Submitted to

The Hong Kong University of Science and Technology

in Partial Fulfillment of the Requirements for

the Degree of Doctor of Philosophy

in the Department of Electronic and Computer Engineering

August 2016, Hong Kong

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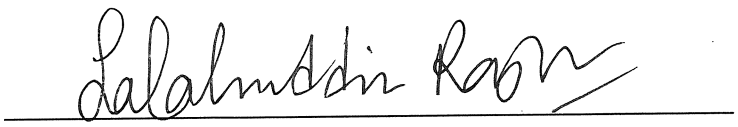

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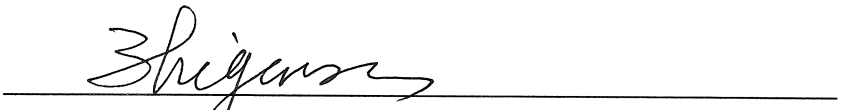

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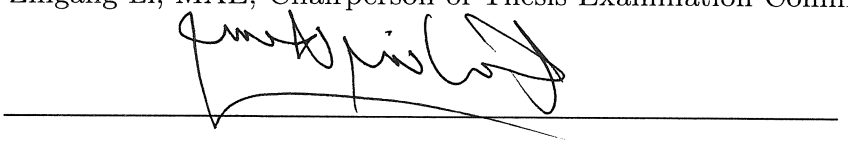

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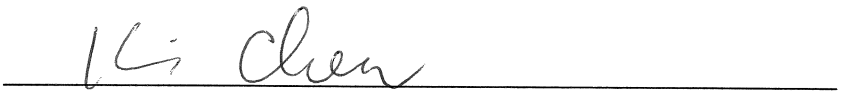

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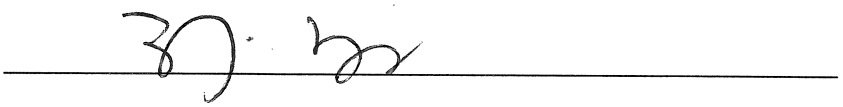

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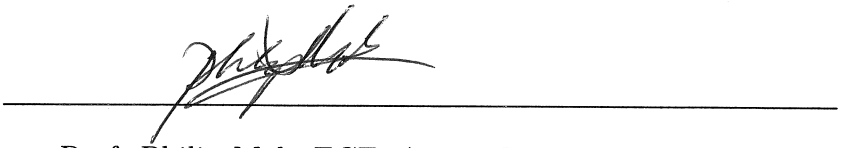

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Many people have contributed to this work. I would like to express my heartfelt gratitude each one of my colleagues and friends for their support. In early stage of my research, I had many discussion and brainstorming with Dr. Changjian Zhou. The work on low dielectric material was initiated after one of such brainstorming sessions. Since then, we had numerous collaborations, certainly a significant portion of the credit goes to him. I would also like to thank Suwen Li for helping me to grow CNTs for low dielectric materials. I had a great pleasure and fun working with the wonderful friends in the Device Characterization Lab (DCL). It was always enjoyable to discuss research topics in the meeting. The feedback from my friends in DCL was very useful. Since, a part of my research is related to the circuit-device interaction, I had always interaction with the members of High Speed Silicon Lab (HS2L). I would like to thank all my friends in HS2L. In particular, I would like to thank Yipeng Wang for helping with circuit simulation. It was my privilege to work with Dr. Haikun Jia in HS2L. Dr. Jia helped me with CMOS integration of antenna and measurements. I am extremely thankful to him in this regard.

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Integration of Low Loss Interconnects in CMOS

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Abstract

In this work, an interlayer dielectric with an extremely low dielectric constant of 1.96 is achieved using SiO_2 with vertically aligned cylindrical pores. Vertically grown carbon nanotubes are used as templates to form cylindrical pores to achieve high porosity while maintaining structural stability. Measurements show that an elastic modulus of 17.5 GPa can be maintained, even at 65% porosity, to provide sufficient mechanical strength for most back end of line (BEOL) processes. The tradeoff between the dielectric constant and elastic modulus for different porous structures has also been studied to project the ultimate achievable k-value.

A BEOL compatible thick dielectric and metal based interconnect, which eliminates the resistive and substrate eddy current loss from on-chip magnetics, is also proposed. Fully integrated on-chip inductors with up to 200 nH/mm^2 inductance density and a peak quality factor of 25, were implemented based on the proposed interconnect technology, and a complete system for on-chip wireless power supply was implemented to demonstrate the integration capability. The 2.5×2.5 mm^2 wireless power receiver chip can harvest 27 mW power from a 250 mW transmitting power source at a distance of 5.3 mm, which is the best power harvesting capability compared to other reported technologies.

The thick dielectric interconnect technology is also proved to be useful to minimize the radiation loss of on-chip antennas. Several millimeter-wave antenna topologies are demonstrated utilizing this technology. An on-chip triangular sleeve monopole, which

has a wide bandwidth from 23 GHz to 63 GHz, with 3.5 dB gain and efficiency of 98%, has been implemented. The antenna is integrated with a foundry fabricated wideband power amplifier IC. This demonstrates the efficacy of the proposed interconnect technology, which has applications ranging from power management to high-speed wireless data communication.

Chapter 1

Interconnect Challenges and Technology Requirements

The task of interconnects is to connect active devices in a certain configuration to achieve a collective functionality. The interconnects consist of metal lines and contact plugs to route the electrical signal to its destination, as shown in Figure 1.1. The metal lines are arranged layer by layer buried inside dielectrics, and different layers of metal lines are connected via contact plugs. When signal travels through the metal lines, it encounters metal resistance, R, and capacitance from the dielectric, C, and signal become delayed. In advanced technologies, this RC delay became comparable to the delay from the active devices [1], [2]. Also there is certain amount of power is consumed during the process. In practice, it is desirable to make the interconnect with highest conductive metal buried inside a low dielectric, k, constant material. One of the best conducting metal, Copper, has already been adopted to the interconnects, but there is still room for improvement to achieve low-k.

Since, the advance interconnects are mainly optimized for digital electronics, it became inefficient for analog and RF applications, especially for integrated magnetics applications and on-chip radiation structures. This work is mainly focused on the strategies to achieve low-k, and efficient implantation of interconnects for magnetics and

radiating structures.

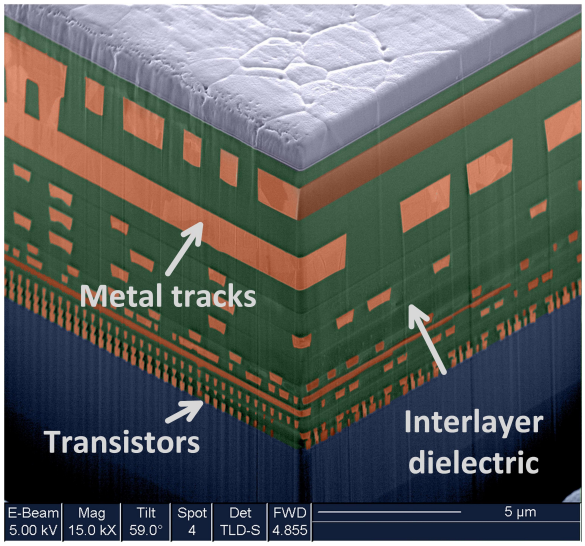

Figure 1.1: Cross-section of an interconnect structure (Courtesy of IBM).

1.1 Low-k Material Integration Challenges in BEOL

The international technology roadmap for semiconductors (ITRS) states that the effective k-value of 1.8–2.2 [2] will be required beyond 2024, but the manufacturable solution for such low-k ILDs are not known [3]–[5]. There is no solid material in nature exhibit such stringent k-value requirements. Most promising way of decreasing the k-value of a material is by introducing porosity. A typical way of porous dielectric implementation is described in Figure 1.2. To achieve such a low-k, more than 50% porosity will is required. However, there is an inverse relationship in between mechanical strength of the dielectric and the k-value, as described in Figure 1.3. The low-k material should satisfy some key requirements upon integration.

- Electrical: High breakdown strength, low loss tangent and low leakage.
- Mechanical: High elastic modulus, good adhesion between metal and other substrate.
- Chemical: Low moisture uptake.

- Thermal: Good thermal conductivity and high thermal stability.

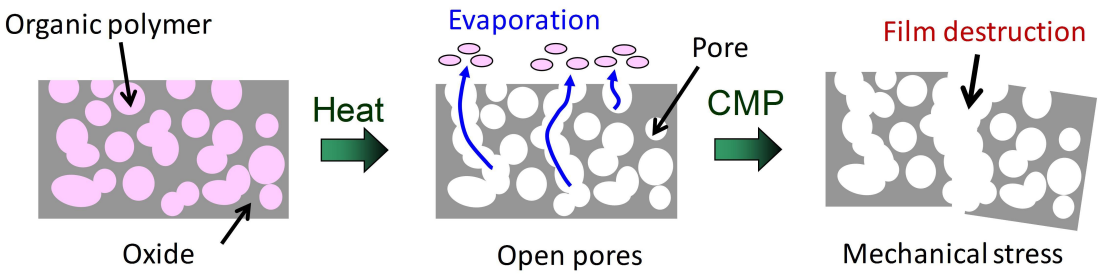

Figure 1.2: Implementation of porous dielectric with spherical pores.

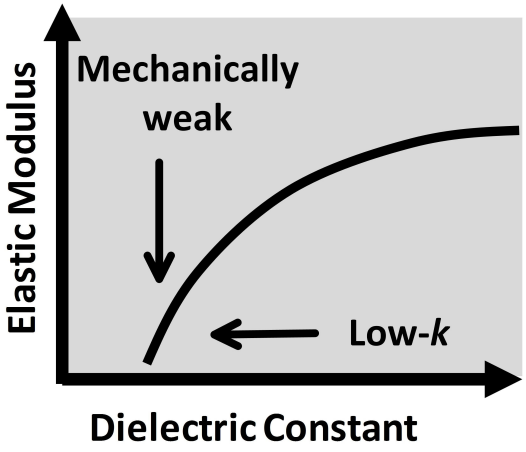

Figure 1.3: Inverse relationship between k-value and the elastic modulus of the porous dielectrics.

There is a complex interaction between pore morphology, porosity and the mechanical strength of the material. Conventionally, the porosity is introduced by using spherical pores (SP). The porous structure with SP reach its percolation threshold beyond 50% porosity, i.e. pores become interconnected. If any external force applied at this state, the material immediately collapses on itself; as a result the Young modulus (E) goes near zero as compared to the bulk. To overcome this barrier, this work presents a dielectric structure with vertically aligned cylindrical pores (VACP) is imprinted inside the bulk. Extremely low dielectric constant was achieved while surviving the stress during the chemical mechanical polishing (CMP). The reliability analysis upon electrical, thermal and mechanical stress was carried out, and the implication of such an ultralow-k

dielectric technology was investigated for high speed signal transmission.

1.2 Benchmarking Interconnects for On-Chip Magnetics

Efficient magnetic components are required for analog and RF applications. In some applications, passive discrete components take more space than the CMOS control IC itself. Integration of these passives into the control IC could reduce the overall size, and most importantly it would reduce the total solution cost. A theoretical benchmarking test was performed to evaluate the capability of magnetic integration, mainly inductor, in a particular foundry technology. To perform this test all interconnect layer information, including dielectric thickness, k-value and metal thickness were required. A typical cross-section of a on-chip inductor is shown in Figure 1.4. The main concern is to reduce the loss in the inductor. If the impedance of the inductance is defined as, $Z_S = R_S + j\omega L$, where R_S is the loss component and L is the value of inductance, the relative loss component can be quantified as $Q = \omega L/R_S$. Large quality factor, Q, indicates low loss in the inductor. A simulaiton platform, in Figure 1.5, was implemented for this benchmark. The TSMC 65 nm technology was used for this benchmark. All dielectric and metal layer information were inserted as fixed parameters. The outer diameter, metal width, metal spacing and operation frequency were the input variables of the benchmark. All fixed and input variables were inserted to an algorithm to create all possible inductor structures. The full 3D EM [6] simulation were performed to find out loss basic circuit parameters of those inductors. At a particular frequency, there was a best achievable inductor with highest Q value. At each operating frequency, extending from 10 MHz to 100 GHz, the highest Q-value inductors were extracted. The summary of the shown in

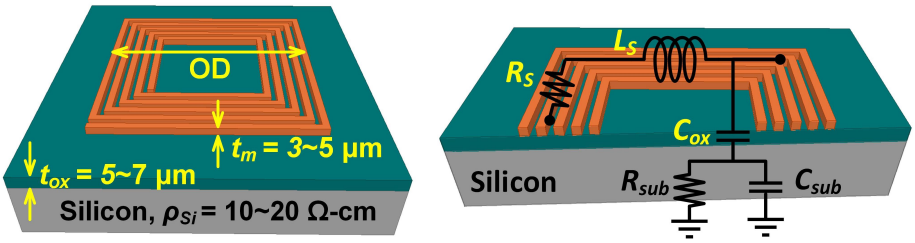

Figure 1.4: Cross-section of an inductor and its basic circuit parameters.

Figure 1.6. The highest possible Q-value and its corresponding inductance is shown in Figure 1.6. The results indicate that magnetic on TSMC 65 nm technolgy prove to be efficient in 1 GHz to 60 GHz. In low frequency range, the inductor becomes lossy even though large inductance value can be achieved. There is an interest of efficient inductors in such low frequencies, less than 1 GHz, especially in power management applications. It is evident that this is not possible in conventional CMOS interconnects. The conventional interconnects mainly consist of thin dialectic and metal (typically about several μm) on a low resistive (10–30 Ω–cm) silicon substrate. Due to small metal thickness, inductors suffer severe resistive loss. And for the thin dielectric, inductors suffer from substrate loss and low-self resonance frequency [7], [8]. In this work, an interconnect technology was proposed to eliminate such losses, and efficient on-chip magnetics were implemented in MHz frequency range.

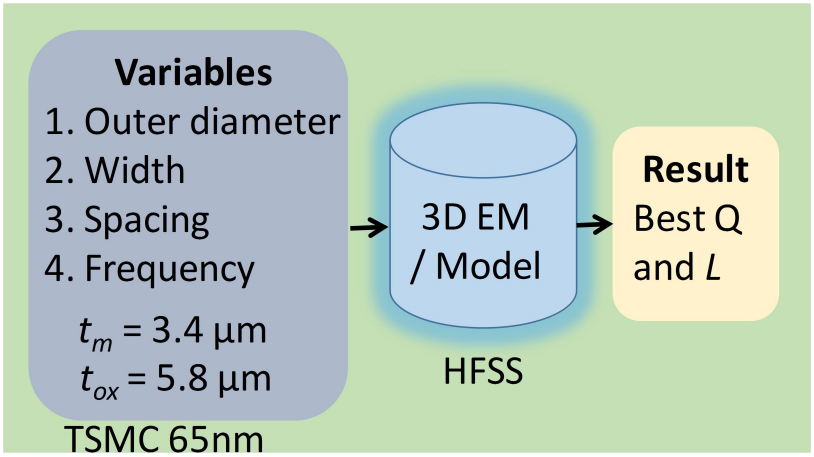

Figure 1.5: Simulation platform of the benchmark test.

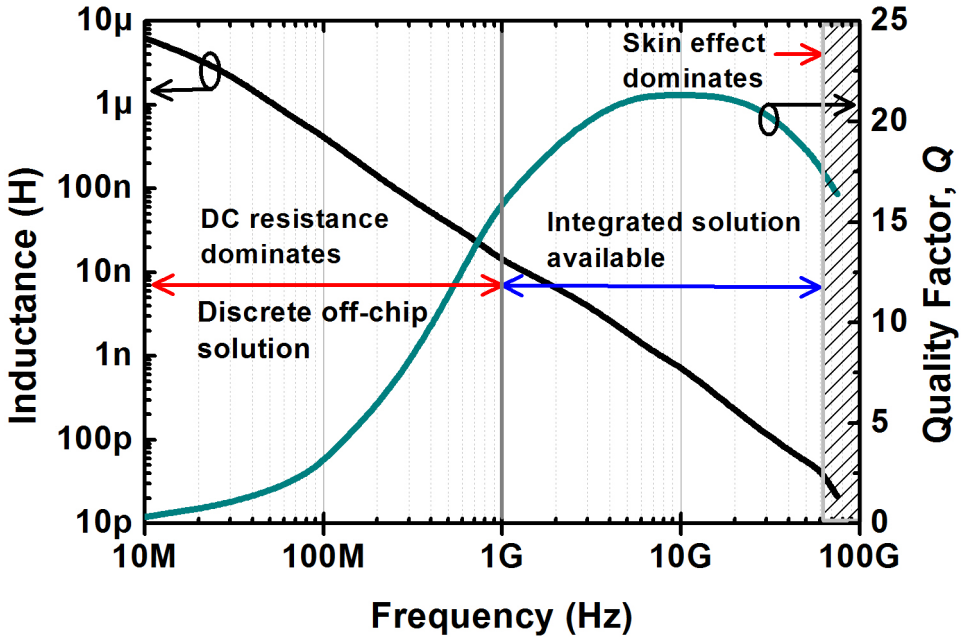

Figure 1.6: Highest possible Q-value at different frequency and its corresponding inductance.

1.3 Interconnect Non-Idealities for Electromagnetic Applications

The electromagnetic radiation from CMOS interconnect is most inefficient. In terms of cost and system integration, it is preferable to have radiating antenna on silicon. Low silicon resistivity is one of the major prohibiting factor of such applications. Since the dielectric constant of the silicon is large, when an antenna radiates close to the silicon, the EM wave sucked inside the silicon and certain amount of power was dissipated inside the silicon due to its lossy nature, especially in millimeter-wave frequency range. This loss may have been eliminated by using high resistive SOI substrate. Secondly, due to its high permittivity the silicon substrate, there is a surface wave created inside the silicon, as shown in Figure 1.7. This has severe detrimental effect of the antenna radiation patterns. As shown in Figure 1.8, radiation is uniformly spread out to the space from an isolated dipole. But when the diople implemented on silicon, it creates an undesirable radiation pattern, also its efficiency reduces.

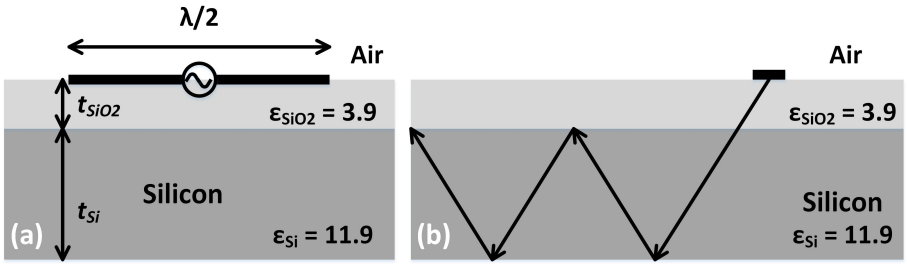

Figure 1.7: Antenna radiation (a) and surface wave mode (b) in silicon.

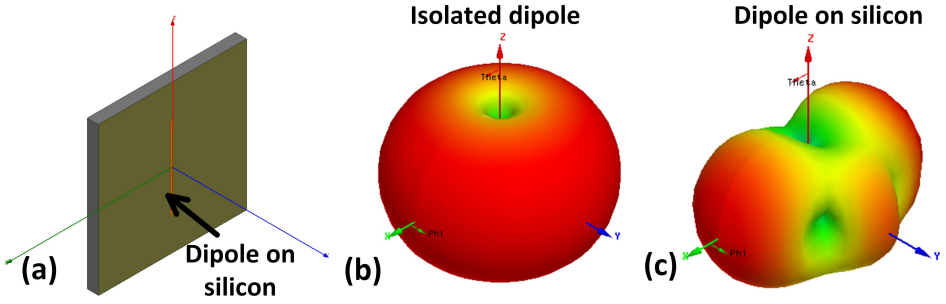

Figure 1.8: The radiation pattern of a dipole on silicon at 60 GHz.

This work proposed a interconnect technology to eliminate such radiation losses. Several antenna topologies were implemented. Effectiveness of the technology was also demonstrate by imlementing a broadband wireless data communication system.

1.4 References

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Chapter 2

Nanotube Assisted Ultralow-k Dielectrics

As the feature size in integrated circuits continues to scale down according to Moores law, reducing the dielectric constant (or k-value) of interlayer dielectric (ILD) becomes important [1] for minimizing propagation delay and dynamic power consumption in the back-end-of-line (BEOL). The international technology roadmap for semiconductors (ITRS) states that the effective k-value of 1.8–2.2 [2] will be required beyond 2024, but the manufacturable solution for such low-k ILDs are not known [3]–[5]. There is no solid material in nature exhibit such stringent k-value requirements. Most promising way of decreasing the k-value of a material is by introducing porosity. According to Maxwell-Garnett effective medium approximation, more than 50% porosity is required to achieve k-value less than 2.2 using typical silicon dioxide dielectric [6]–[9]. At this porosity, the pores become entirely interconnected, and such porous material does not survive upon integration due to its weak mechanical strength [10], [11]. To satisfy the manufacturing requirements of BEOL, relatively hard dielectric is required with an elastic modulus larger than 3 GPa.

In this chapter, a dielectric structure with vertically aligned cylindrical pores (VACP) is proposed to achieve high porosity while maintaining high mechanical strength.

The fabrication process, experimental characterization and effectiveness of cylindrical pore morphology will be described.

2.1 Formation of Nanotube Assisted Vertically Aligned Cylindrical Pores

The mechanical structure has a strong impact on the achievable porosity. As shown in Figure 2.1(a), the most common spherical porous (SP) structure reaches its percolation threshold beyond 50% porosity. After the percolation threshold, multiple pores become interconnected to form voids. Such a structure is mechanically unstable and will collapse with the application of small external force. It is due to the significant reduction of the elastic modulus (E). For VACP, even though the pores reach the percolation threshold as shown in Figure 2.1(b), there is always some fraction of the solid material directly opposing the stress of the applied force. Therefore, the displacement upon the external force is less, leading to a high E of the structured material.

The formation process of the VACP structure is illustrated in Figure 2.2. The process starts with a supporting substrate, it can be semiconductor, dielectric or metal. Then, nanotubes were grown on top of the supporting substrate, as shown in Figure

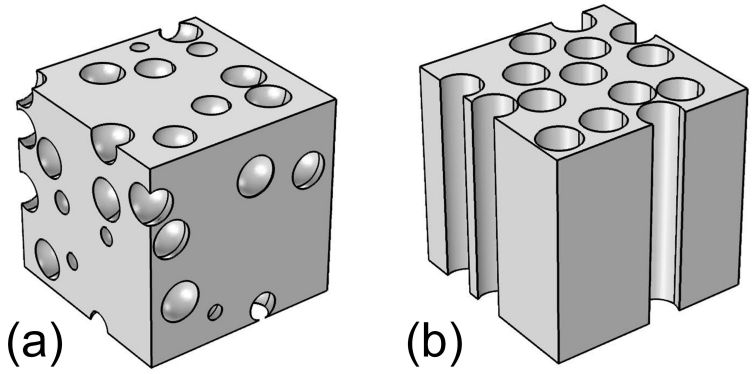

Figure 2.1: Dielectric films with spherical (a) and vertically aligned cylindrical pores (b) geometries with $\approx$ 50% porosity.

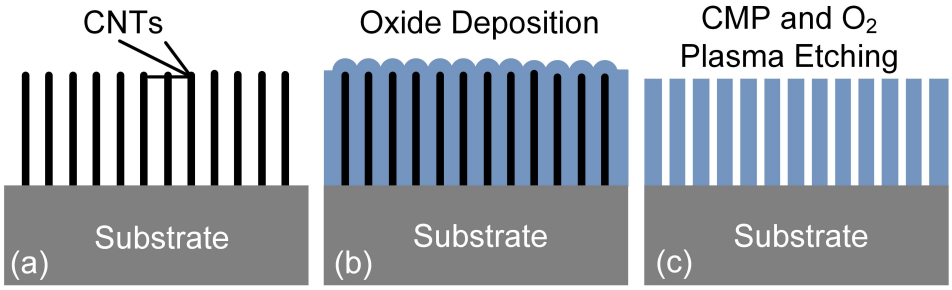

Figure 2.2: Formation process of vertically aligned cylindrical pores in dielectric assisted by vertically aligned nanotubes. (a) CNT growth on a substrate, (b) Desired oxide deposition, and (c) Chemical mechanical polishing (CMP) and CNT removal by O_2 plasma.

2.2(a). These nanotubes serve as templates of the cylindrical pores, and the diameter of the nanotubes are directly translated into the pore diameter. The empty space among nanotubes are filled with dielectric, as shown in Figure 2.2(b). In the following step, chemical mechanical polishing (CMP) is being done to planarize the surface. The top tip of the nanotubes would be exposed after CMP. The polishing time may need to be extended to expose all nanotube tips. The nanotubes are removed depending on their conductivity. If the insulating nanotubes are used, such as boron nitride (BN) nanotubes, it can be left inside the dielectrics. On the other hand, if the nanotubes are semiconducting or metallic, such as carbon nanotubes (CNT), it should be removed to obtain VACP dielectric, as shown in Figure 2.2(c).

The porosity in the material defined by the fraction of voids over the total volume. In VACP structure, the porosity, P, depends on the nanotube density (N_D) and the diameter of the tubes (d_{avg}), and the relationship can be described as,

$$P = \pi \left(\frac{d_{avg}}{2} \right)^2 N_D. \tag{2.1}$$

The void fraction in VACP structure is determined by the volume occupied by the nanotubes. A high density of nanotubes would be desirable to have highly porous dielectric.

For demonstration of VACP dielectrics, CNTs were used as templates, since it can be grown vertically aligned, density can be more than 10^{11} tubes/cm^2 [12], and most importantly, it can be synthesized at low temperature ($\leq 450^\circ$ C) [13]. Starting with the first metal layer for which Ti had been chosen in our process, vertically aligned CNTs were grown using Nickel catalyst. About 2 nm Nickel was deposited using evaporation method. The whole wafer was then loaded inside the plasma enhanced chemical vapor deposition (PECVD) chamber, and kept in vacuum for 10 min to eliminate any ambient gas. To form the nanoparticles, the catalyst film was annealed at 450° C with $H_2 : N_2 = 3 : 1$ at 2.8 Torr for 10 min. Then, 200 W RF plasma was introduced along with 35 sscm CH_4 to grow vertically aligned CNTs. The length of the CNT was controlled by the CH_4 plasma exposure time. The CNT height was about 1 μm. The temperature ramp up and ramp down were 100° C/min and 22° C/min, respectively. This operating condition is compatible to CMOS process and the temperature budget can further optimized such as that described in [14]. Under this condition, most CNTs were multiwall, the diameters were between 20 nm to 30 nm (d_{avg} was about 25 nm), and the density of the tubes was about 1.1×10^{11} tubes/cm^2. According to the Equation 2.1, about 54% porosity was expected. A layer of SiO_2 (or any other desirable dielectrics) is deposited by chemical vapor deposition to cover the CNTs [15]. The film was then partially polished to about 385 nm thick. More than half of the film was polished away to ensure all top ends of the CNTs are exposed. After carefully washing the wafer, it was kept in a vacuum oven at 110° C about an hour to remove any residual moisture. After the baking process, the wafer was immediately loaded into the O_2 plasma chamber. High power O_2 plasma was used to completely remove the CNTs leaving the VACP at the dielectrics as shown in Figure 2.3. The CNT etching and capping layer deposition were done consecutively to prevent any contaminant deposition and absorption in the pores. A thin layer of SiO_2 around 45 nm was then deposited to cap the VACP dielectrics. The top metal layer used in our process was formed by Ti/Au for capacitance measurement. The processing

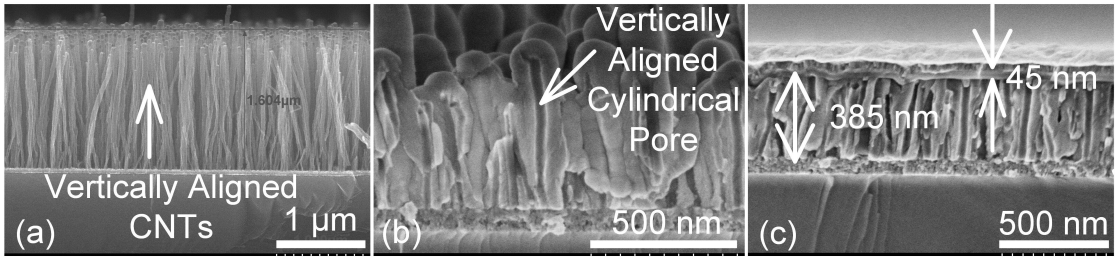

Figure 2.3: Formation process of vertically aligned cylindrical pores in dielectric assisted by vertically aligned nanotubes. (a) CNT growth on a substrate, (b) Desired oxide deposition, and (c) Chemical mechanical polishing (CMP) and CNT removal by O_2 plasma.

conditions in our experiment have not been optimized and fine-tuning is possible. The size of the pores can be controlled by the conditions of CNT growth. The temperature for CNT growth can also be reduced using other processes that can be applied at lower temperature such as that reported in [16]. At this stage, only a proof of concept is achieved. For implementation of VACP dielectric in advanced BEOL, small pore diameter, about 1 5 nm [4], would be required, which can be achieve by using vertically aligned single walled CNTs [13] as templates. In addition, CNTs need to be grown on top of dielectric with tip-growth mode [14], so that all nanoparticles remain at the top end of the CNTs. Later on, these nanoparticles would be removed during the polishing step. This will prevent any shorting between adjacent metals in the same level.

Capacitors with an area of 150×150 μm^2 were designed with SiO_2 containing the VACP as the dielectric. The measured capacitance is ranging from 0.889 pF to 0.945 pF. There was no DC bias (from -2 to +2 V) dependency observed in the measurement as shown in Figure 2.4. From the capacitance, we can extract the effective dielectric constant which is found to be in between 1.92 and 2.04. To check the reproducibility of the VACP dielectric, multiple samples were prepared and capacitance measurements were performed in various locations on those samples. The cumulative probabilities of dielectric constant are shown in Figure 2.5. The average dielectric constant was about 1.96.

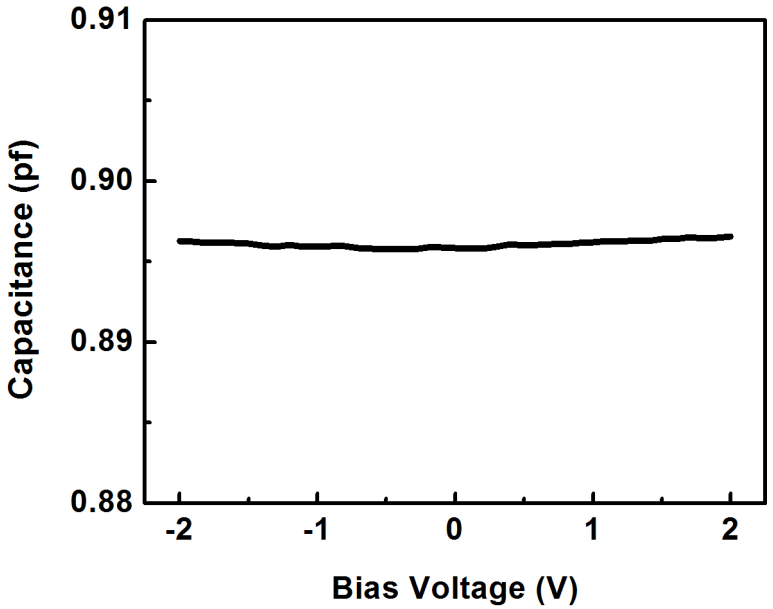

Figure 2.4: Capacitance measurement at different bias voltages.

The variation in the dielectric constant is mainly attributed to the nanotube density during the growth.

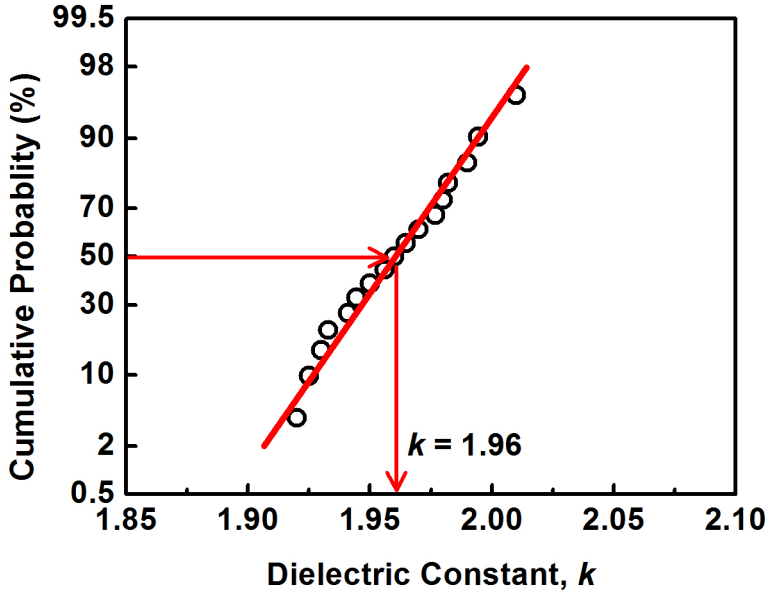

Figure 2.5: Cumulative probability of measured dielectric constants.

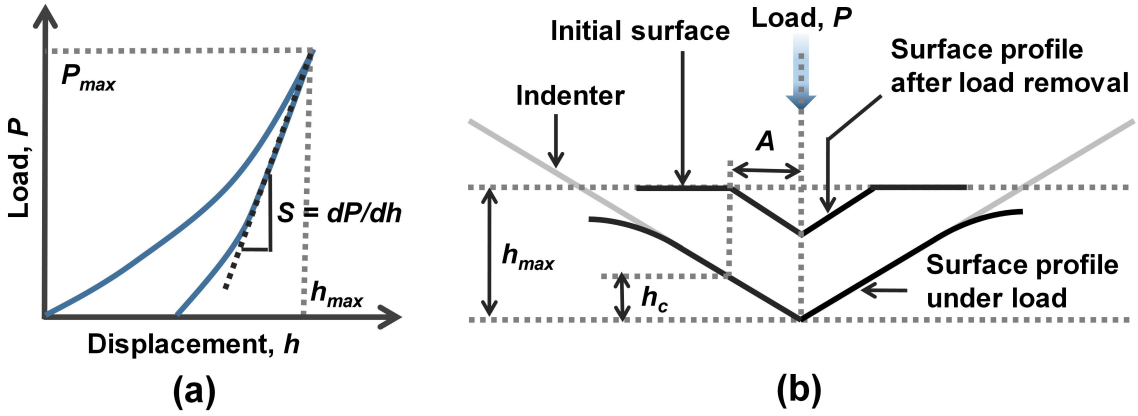

Figure 2.6: (a) Load versus displacement curve for a elastic material, the loading is followed by elastic unloading process. (b) Cross-section of indenter and sample interaction during loading and unloading indicating quantities used for analysis.

2.2 Improved Mechanical Properties of the Dielectric Through VACP

The elastic modulus of the VACP dielectric was characterized through nanoindentation experiment. The nanoindentation experiment involves application of force though diamond indenter on a desired sample. The force measured as a function of the depth during loading of the indenter. This represents the resistance of the sample to both plastic and elastic deformation. The applied force decreases during unloading of the indenter. The force versus the depth during unloading defines the sample's stiffness. Figure 2.6(a) shows a typical displacement curve during loading and unloading of an indenter. The applied load P and depth of penetration h into the sample are continuously monitored by the test equipment. The sample hardness, H and reduced elastic modulus E_r can be calculated from this load versus displacement curve. However, several critical information need to be evaluated for to extract those information, most importantly the projected contact area, A. A typical cross-section of an indentation shown in Figure

2.6(b). The contact penetration depth, h_c, is defined as

$$h_c = h_{max} - 0.75\frac{P_{max}}{S}. \tag{2.2}$$

The unloading stiffness is defined as $S = \frac{dP}{dh}$, as shown in Figure 2.6(a). Here, h_{max} is the indentation depth at the maximum applied force, P_{max}. The contact area is determine from the probe area function, $A(h_c)$, for a given h_c. The corrected area function can be expressed as sixth order polynomial function

$$A(h_c) = C_0h_c^2 + C_1h_c + C_2h_c^{1/2} + C_3h_c^{1/4} + C_4h_c^{1/8} + C_5h_c^{1/16} \tag{2.3}$$

where, the first coefficient, C_0, represent the ideal function of the indenter, it is 24.5 for a Berkovich indenter. To determine all the coefficient of the area function, a series of indentations are performed a various contact depth on a sample of known elastic modulus. Typically fused quartz is used for this calibration. Then coefficients were numerically fitted to obtain complete corrected area function. The hardness calculate as

$$H = \frac{Pmax}{A(h_c)}. \tag{2.4}$$

The reduced modulus is calculated as

$$E_r = \frac{S\sqrt{\pi}}{2\sqrt{A(h_c)}}. \tag{2.5}$$

To determine the elastic modulus of the sample, E_{sample}, the elastic modulus of the indenter, E_i, needs to be considered. The E_{sample} can be calculated as

$$E_{sample} = (1 - \nu_i^2)\left(\frac{1}{E_r} - \frac{(1 - \nu_i^2)}{E_i}\right)^{-1}. \tag{2.6}$$

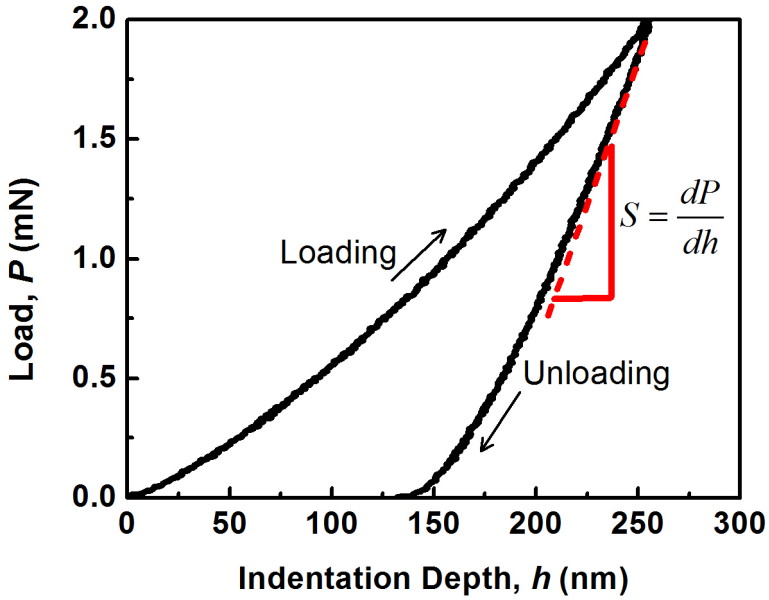

Figure 2.7: Experimentally obtained load versus displacement curve during elastic modulus measurement of VACP dielectric by nanoindentation.

For a standard diamond indenter probe, E_i is about 1140 GPa and the Poisson's ratio, ν_i, of the indenter is about 0.07.

The nanoindentation experiment was performed using Hysitron TriboIndenter, and a Berkovich type three sided pyramidal probe was used for indentation. The probe tip radius was about 150 nm. Because of this, minimum compliance of the indentation depth was about 40 nm. A large indentation depth ($>$ 40 nm) was required for accurate contact area determination. However, it is advisable to limit the maximum indentation depth to one tenth of the film thickness for minimizing the substrate effect [13]. A thick, about 4 μm, VACP dielectric was prepared for this measurement. The Figure 2.7 shows the load versus displacement during indentation. The penetration depth was up to 255 nm at a maximum load, P_{max}, of 2 mN. This load versus displacement data was directly translated into the elastic modulus. At his particular indentation test, the projected indentation area was about 1.25 μm^2.

The nanoindentation measurements have been carried out in several indentation

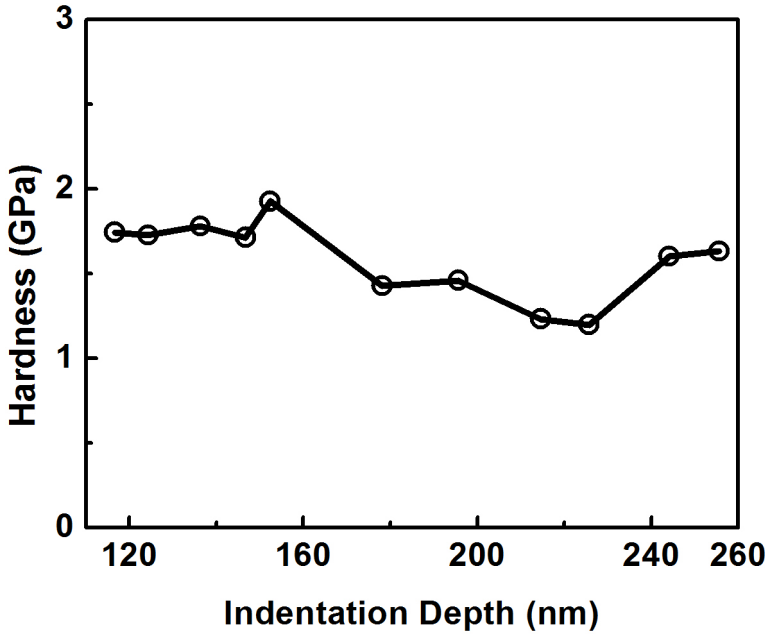

Figure 2.8: Experimentally obtained hardness of VACP dielectric at different indentation depths.

depths. The elastic modulus and hardness of the VACP dielectric was measured at various indentation depths. The hardness of VACP dielectric at different indentation depths is shown in Figure 2.8, and the elastic modulus measurement results shown in Figure 2.9. The hardness of the VACP dielectric varies between 1.23 GPa and 1.8 GPz, and the average hardness was about 1.58 GPa. The elastic modulus of the dielectric is ranging from 16.87 GPa to 18.10 GPa. The average elastic modulus of the VACP dielectric was about 17.5 GPa.

Two major contributing factors assisted this variations. The first cause was the surface roughness. It is a very important issue in nanoindentation test. Since the contact area is measured indirectly from the penetration depth, the surface roughness causes measurement errors in determination of the projected area of contact between the indenter tip and the sample. Careful polishing was carried out during the formation of VACP dielectrics. However, there was variation in surface roughness among different samples. Besides, there was CNT density variation during growth. Densely located VACP could weaken the dielectric and sparsely populated VACP could strengthen dielectric form the

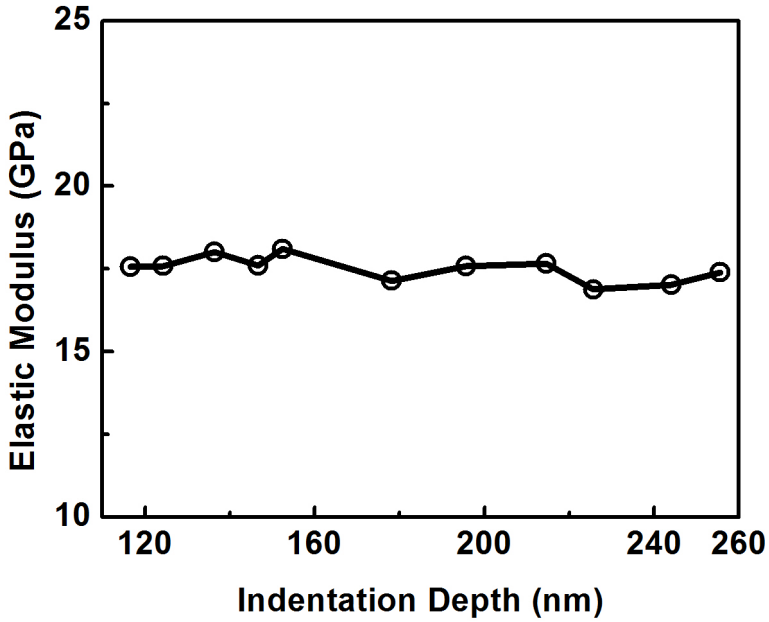

Figure 2.9: Experimentally obtained elastic modulus of VACP dielectric at different indentation depths.

nominal value. However, the variation elastic modulus were limited to 10% from the nominal value.

2.3 Impact of Pore Morphology on the Material Characteristics

It is important to understand how the mechanical and electrical properties of the material vary with porosity and their pore morphology. The overall mechanical properties of porous low-k dielectrics are determined by the properties of the solid matrix and the pore morphology. That's why, the successful integration of porous dielectric requires a detailed understanding of how the mechanical stability of porous dielectric varies with porosity and pore microstructures. Although significant advancement has been made toward porous dielectrics, there is still relatively little fundamental understanding of the impact of pore morphology on the mechanical properties of porous low-k dielectrics. In this section, theoretical studies have been carried out to model the effects of porosity on

the elastic and dielectric properties of materials.

The impact of pore morphology was investigated by comparing the mechanical and electrical properties using 3D finite element (FE) simulation [16]. As inputs of FE simulation, two different kinds of pore morphologies were used. These two pore morphologies are vertically aligned cylindrical pore (VACP) and spherical pores (SP). For the geometric models, a Cartesian coordinate was used. The pores were assumed to be uniformly and randomly distributed in the structure. The representative volume element approach was used to model the porous microstructures with different pore morphologies. The FE simulation was performed using COMSOL multiphysics sofware.

From the FE simulation results, an analytical relationship has been established between bulk elastic modulus E_B and elastic modulus E_P at a specific porosity. The relationship is described as,

$$\frac{E_P}{E_B} = \left(1 - \frac{P}{P_c}\right)^n . \tag{2.7}$$

Here, porosity value is defined as P, P_c is the porosity at which effective elastic modulus of the microstructure becomes zero, and n is the parameter dependent on the pore morphology. It is desirable to have small n, close to one, for a particular pore morphology. For a large value of n, effective modulus decreases sharply along with the porosity.

Table 2.1: Analytical parameters of elastic modulus for different pore morphologies.

Pore Morphology	n	P_c
Spherical Pores	1.8	0.85
VACP	1	0.95

The FE simulation of the microstructure at different porosity is summarized along with the analytical results in Figure 2.10. Analytical parameters for different pore morphologies have been extracted, which are shown in Table 2.1. The n value was found to be one, which indicates that in VACP elastic modulus decreases linearly with increasing porosity. Where as in spherical pores, the elastic modulus decreases sharply

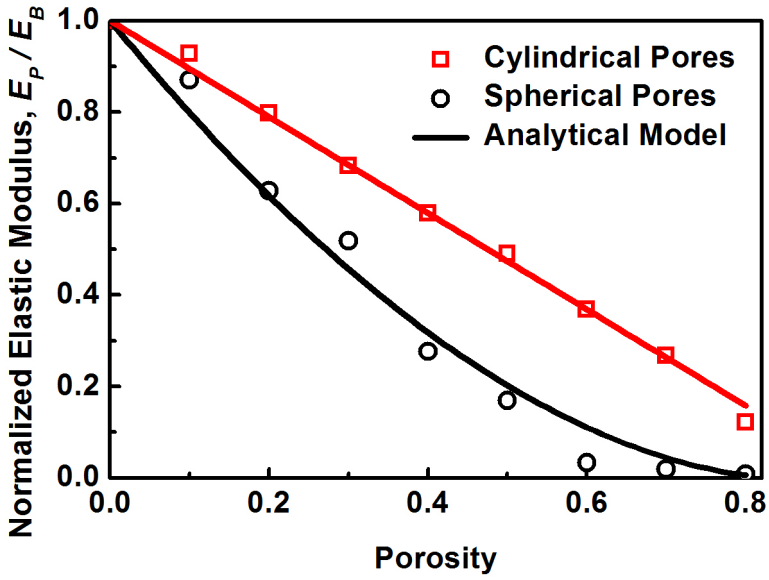

Figure 2.10: Normalized elastic modulus (E_P/E_B) as a function of porosity. Here, E_B is the elastic modulus of bulk dielectric.

with increasing porosity. For SP dielectric, the effective modulus practically vanishes at 80% porosity.

Table 2.2: Analytical parameters of shear modulus for different pore morphologies.

Pore Morphology	n	P_c
Spherical Pores	2.2	0.8
VACP	1.1	0.9

The FE simulation is also performed to evaluate shear modulus, G_P, at different porosity. Figure 2.11 shows the behavior of shear modulus at different porosity. The analytical model was also calibrated to describe nature of shear modulus behavior with porosity. The results are described in Table 2.2. The shear modulus in SP dielectric becomes zero at 80% porosity, and deteriorate sharply with increasing porosity. On the other hand, in VACP dielectric, the shear modulus shows a linear decrements (n value was about 1.1) with porosity. Even 80% porosity would be achievable at a considerably large shear modulus.

The overall dielectric property of porous film depends on the solid matrix and the pore morphology. That's why it is important to understand how the dielectric constant

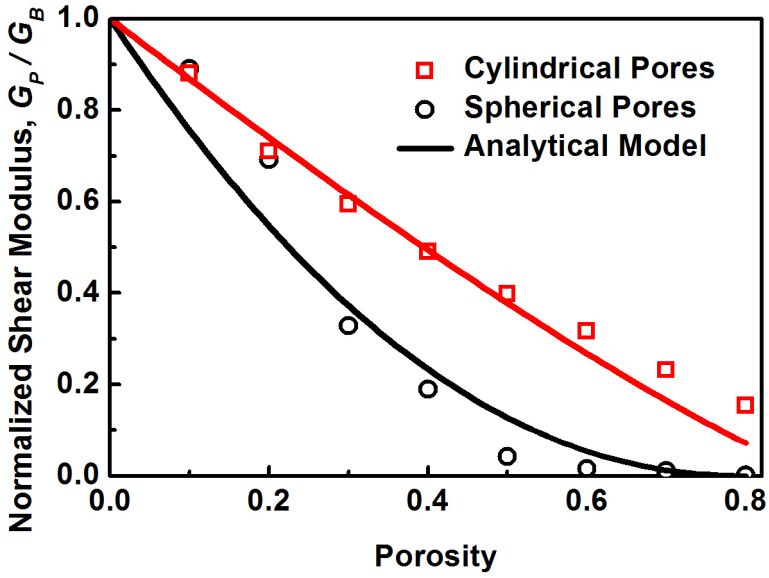

Figure 2.11: Normalized shear modulus (G_P/G_B) as a function of porosity. Here, G_B is the elastic modulus of bulk dielectric.

varies with porosity and the pore morphology. An effective medium approximation is the simplest way of investigating phenomena. The Maxwell Garnett approximation gives the functional description the composite dielectric constant. The dielectric constant of host matrix was assumed to be k_B. If the host matrix is diluted with another material, whose dielectric constant is k_1, the original dielectric constant of the host matrix will be changed according to the and the dilute volume fraction, δ. The effective dielectric constant, k, will be,

$$k = k_B \frac{k_1(1+2\delta) - k_B(2\delta - 2)}{k_B(2+\delta) + k_1(1-\delta)}. \tag{2.8}$$

For a porous material with spherical pores, the value of k_1 would be 1 and volume fraction would be represented by porosity P. The simplified effective dielectric constant would be

$$k = k_B \frac{(1+2P) - k_B(2P - 2)}{k_B(2+P) + (1-P)}. \tag{2.9}$$

However, this effective medium theory could not be extended for cylindrical pores, i.e. VACP dielectrics. Compete FE treatment would be required to evaluate the effect of pore morphology on the dielectric constant of the microstructure. Figure 2.12 describes the

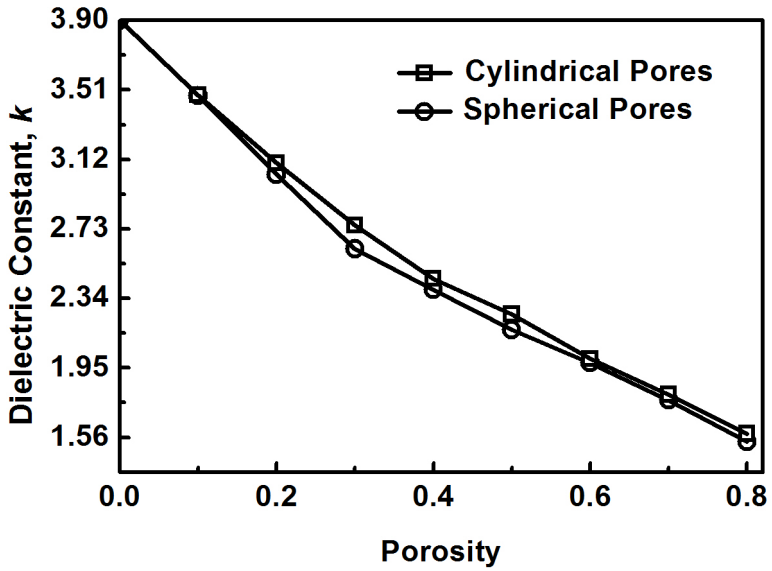

Figure 2.12: Impact on porosity and pore morphology on the dielectric constant of SiO_2.

impact of porosity and pore morphology on the SiO_2 dielectric. The dielectric constant of both cylindrical and spherical pore decreases similarly with the increase of porosity. The decrements of dielectric constant is slightly sharper than cylindrical pores. This is due to series parallel connection of pores in the SP dielectrics. However, the difference is not significant.

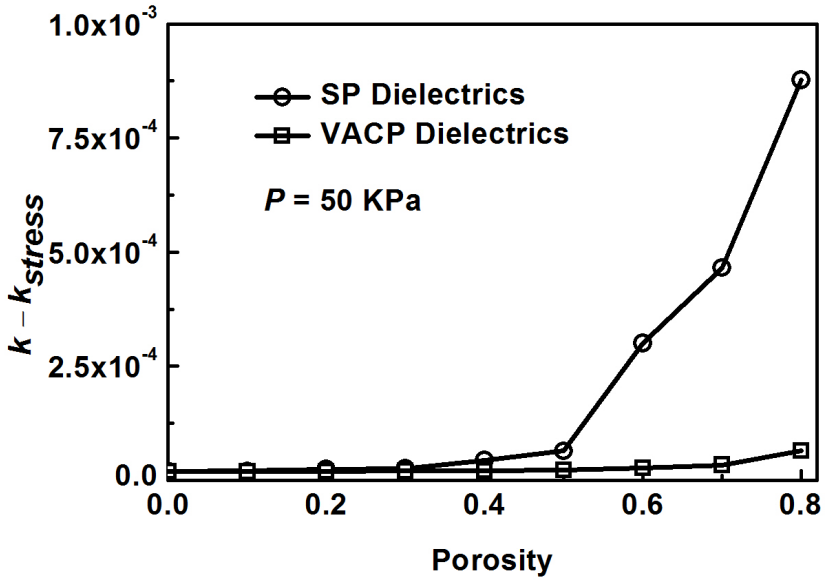

Figure 2.13: Impact of an external stress on the dielectric constant at different porosity and pore morphology.

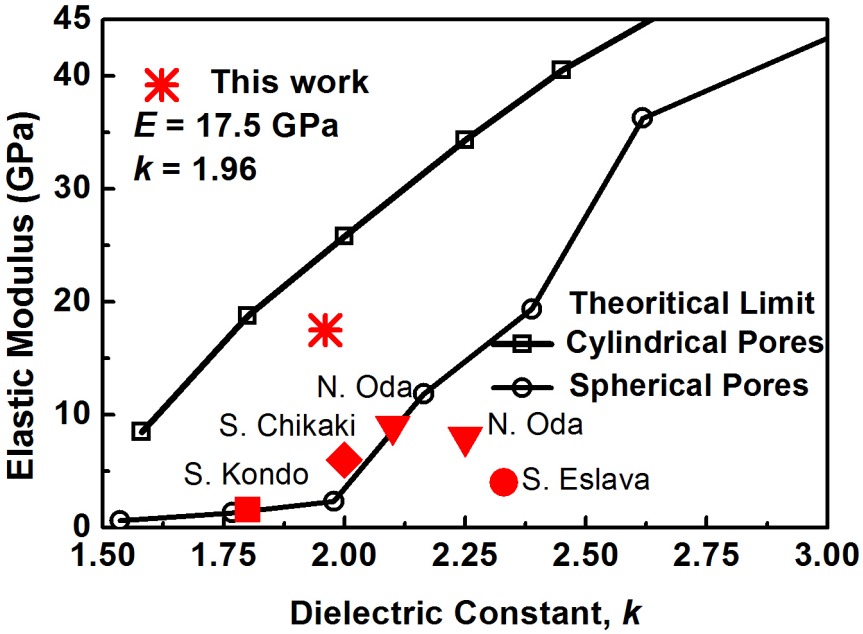

Figure 2.14: Comparison of VACP dielectric with other reported technologies. And the theoretical (elastic modulus and dielectric constant upon different pore morphologies) and measured elastic modulus as a function of dielectric constant.

From the measured k-value, we estimated the porosity achieved by the VACP is about 65%. Simulation result shows that VACP structure is capable of maintaining an acceptable E, equivalent to 30% of its bulk moduli (E_B) at this porosity, and experimentally it was to be found about 17.5 GPa. Whereas at the same porosity level, the elastic modulus, E_P, in SP dielectrics became less than 3 GPa. The impact of the pore morphology on the permittivity is shown in Figure 2.12. The k-value of both structures decreases with porosity in a similar manner. In such case, the VACP can structurally enhance the value E_P at the same value of k. As an example, SiO_2 having VACP structure with $k = 1.6$ and $E_P = 8$ GPa is feasible at a porosity of 80%.

The applied stress during processing, chemical mechanical polishing (CMP) and packaging, squeezes the porous material and increases the effective k value. This effect grows exponentially with the increased porosity as shown in Figure 2.13. The VACP structure can relief the impact of post-processing stress due to its low displacement. As an example, the typical 50 KPa stress in a CMP processing can increase the k value by

3×10^{-4} in 60% SP porous dielectrics on a 100 mm wafer. The increment in the VACP dielectrics is merely 2.7×10^{-5} as shown in Figure 2.13. Clearly the mechanical stability of the VACP dielectrics is better than SP dielectrics.

It is desirable to have large elastic modulus for any porous low-k material to sustain the manufacturing stress. Thats why it serves as a key metric for fair comparison among different porous material technologies. The elastic modulus and k value were compared with different types of low-k materials, as shown in Figure 2.14. In leading technologies [7], [17] – [25], elastic modulus always remains less than 5 GPa when the k-value is less than 2. The elastic modulus of the VACP dielectric is up to 17.5 GPa at a k-value of 1.96, clearly in terms of mechanical stability the VACP dielectrics is better than any other reported technologies.

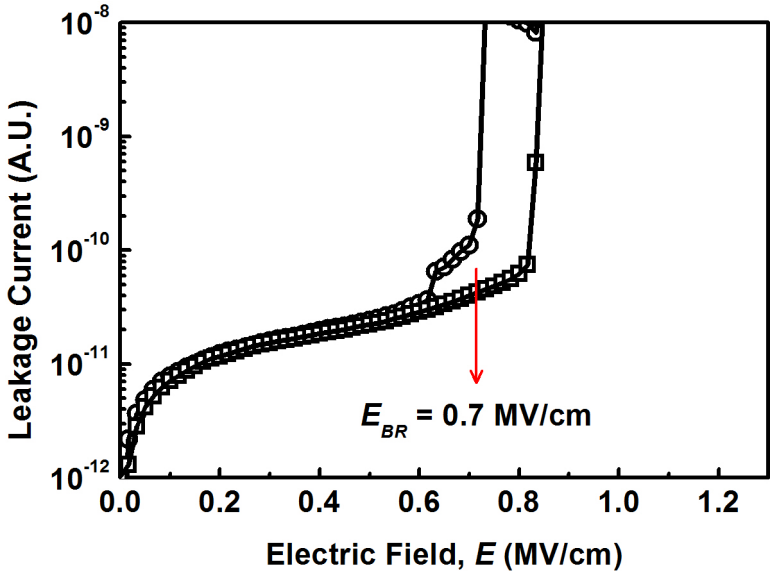

Figure 2.15: Leakage current in VACP dielectric at different applied electric field.

2.4 Reliability of Ultralow-k Porous Dielectrics

Ideally, a dielectric should be a perfect insulator. But in reality, it has finite resistivity and allows to leak current through the dielectric at certain applied voltage. That's why any dielectric system, the leakage behavior and dielectric strength needs

to be investigated. The leakage behavior and dielectric strenght of VACP dielectric is shown in Figure 2.15. The hollow pores act as defective trap sites in the material that enhances the breakdown process and reduces the breakdown field [9]. The defect site concentration of VACP dielectric should follow the density of of the CNTs, as they are used as templates. Due to such large defect density, the effective dielectric strength of the material is reduced to about 0.7 MV/cm as shown in Figure 2.15. The temperature dependence of the breakdown field is shown in Figure 2.16. The breakdown voltage deteriorates with at increased temperature.

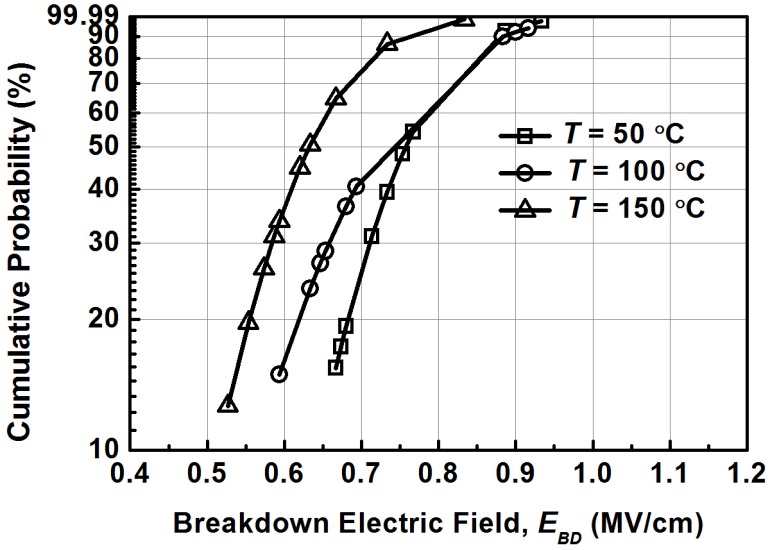

Figure 2.16: The temperature dependency of the dielectric breakdown field.

The temperature dependence of the dielectric constant is shown in Figure 2.17. This measurement was done to investigate the moisture uptake in the VACP dielectric. Due to the high dielectric constant of water (about 80), a small amount of water adsorption could signicantly increase the effective k-value. At a high temperature, trapped water molecules in the pores are expelled and the effective k-value drops. The measured reduction of k-value is less than 30% indicating the pores were well sealed with only minor opening for absorption of ambient moisture [3]. The impact of the external stress on capacitance was also investigated and the results indicated that capacitance

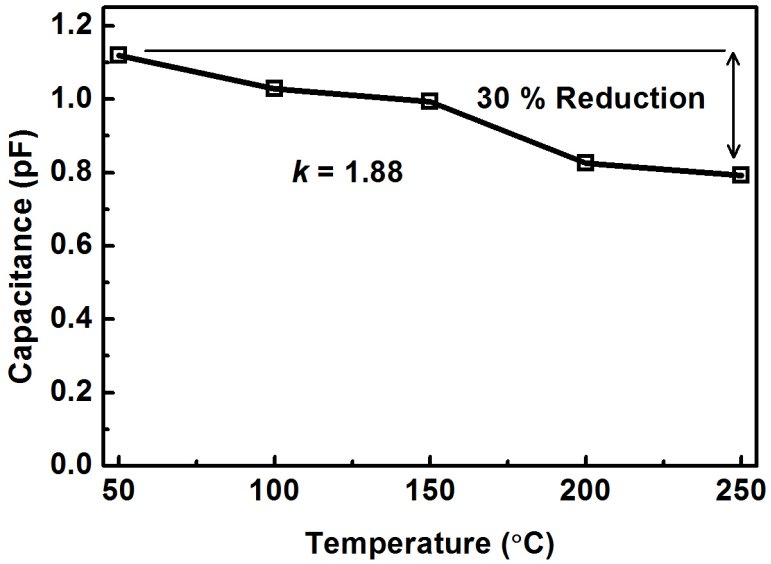

Figure 2.17: Measured capacitance at different temperatures, impact on moisture uptake.

increases with the increment of the stress as shown in Figure 2.18. It was observed that the capacitance increased by 0.045% for a stress of 17.65 MPa, equivalent to 0.46 nm displacement suggesting that the elastic modulus of the dielectric was 12.8 GPa, which is close to the observed value form the nanoindentation experiment.

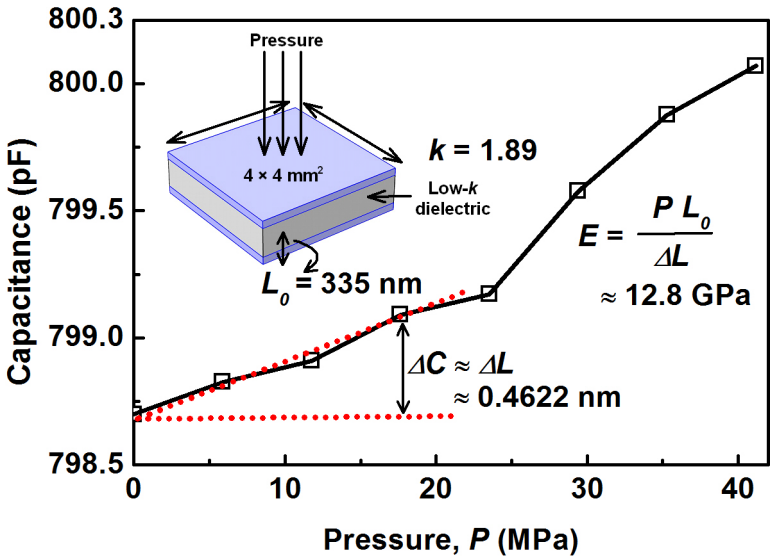

Figure 2.18: The impact on capacitance upon different applied stresses.

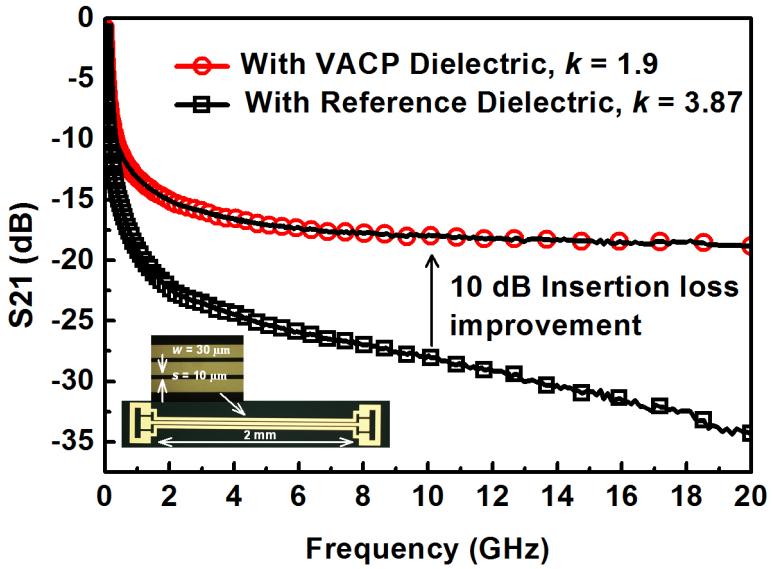

Figure 2.19: Frequency response (S21) of 2 mm transmission lines in different dielectric system.

2.5 Signal Integrity Improvement Utilizing VACP Dielectrics

The direct advantage of using low-k dielectric can be observed by the frequency response of transmission lines fabricated on it. Mainly the transmission lines are capacitively coupled. Any reduction in dielectric constant would enhance the insertion and isolation capability of the transmission line. The insertion capability (i.e. propagation delay and loss) of a transmission line and the isolation capability of adjacent traces were measured and shown in Figure 2.19 and Figure 2.20. Indeed the measurements verified that the dielectric with VACP can reduce the insertion loss by 10 dB, and the isolation capability is improved by 2.2 dB compared with the non-porous structure.

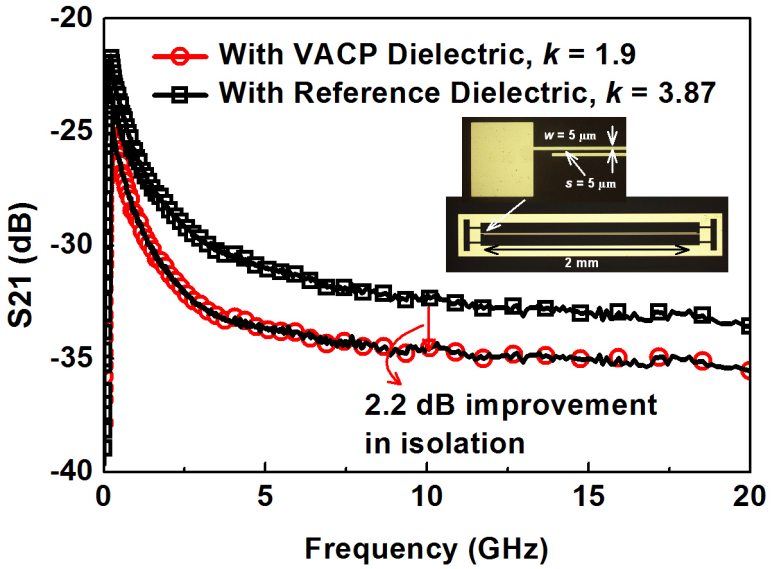

Figure 2.20: Crosstalk response of 2 mm long adjacent traces upon different frequency.

2.6 Concluding Remarks on VACP Dielectrics

In this work, we have demonstrated an interlayer dielectric based on silicon dioxide with vertically aligned cylindrical pores (VACP) that achieved an ultralow k-value of 1.96. The vertically grown CNTs as an imprinting template provides a straightforward way of making this highly porous ultralow-k dielectric with improved stability in electrical and mechanical properties. The structure has been shown to be useful to reduce dynamic power consumption and signal propagation delay in the integrated circuits.

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Chapter 3

Engineered Interconnects with Ultra-Thick Dielectric and Metal

In conventional interconnects, thin dielectric and metal is used due to its compact nature. This type of interconnects is highly suitable for digital circuitry. But, for analog and RF application it becomes a major sources of losses. To study this loss mechanism, on-chip inductors are most suitable circuit components. Inductors has a complex interaction among resistance, capacitance and inductance, and its losses are sensitive to the dimension of the used dielectric and metal. Typically, on-chip dielectric thickness is in between 10–15 μm, maximum metal thickness is in the range of 3–5 μm, and the silicon resistivity is about 10 Ω–cm. Due to small metal thickness, inductors suffer severe resistive loss, and for the thin dielectric devices suffer from substrate loss and low-self resonance frequency [1], [2]. Hence, in the conventional interconnects high performance magnetics can not be realized. Besides, any new proposal to overcome these barrier has to comply the CMOS compatibility issue. Mainly, it should take minimum number of steps, area minimization and temperature budget should limited to 200° C. Upon considering all these limitation, this work proposed a thick dielectric and metal processing technology. Eventually, using the proposed technology, large value inductors were fabricated and its practical applicability was also demonstrated.

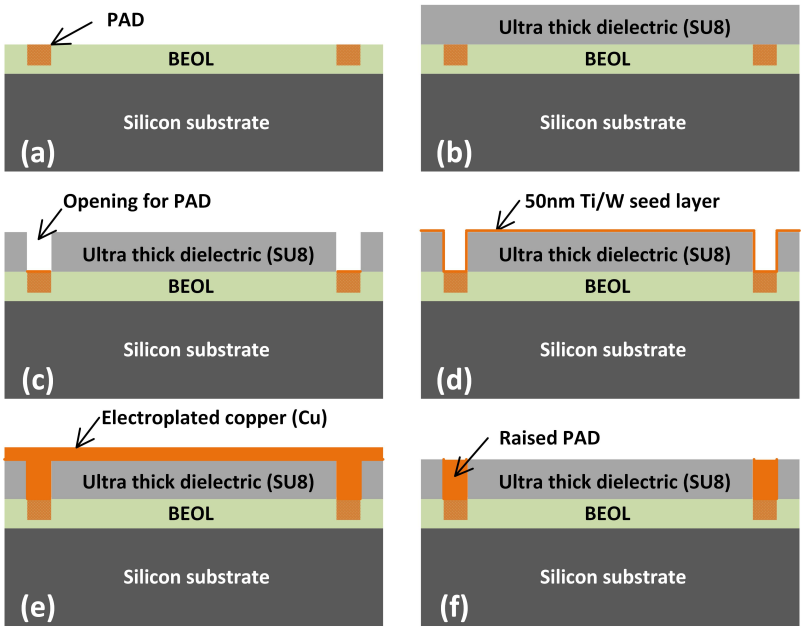

Figure 3.1: Fabrication process of ultra-thick dielectric process for interconnects. (a) A sample IC with BEOL, (b) Spin coating of the thick dielectric, (c) Photolithography to remove material over the PAD, (d) Ti/W seed layer deposition, (e) Copper electroplating, and (f) Polishing to remove overburden copper.

3.1 BEOL Compatible Ultra-Thick Dielectric Processing

To suppress substrate loss due to low resistivity CMOS IC substrate [1], [2], a thick low-k polymer dielectric (SU8, $k = 2.8$) was placed on top of the BEOL of the IC. The detail fabrication process is described in Figure 3.1. At the begining of the process, the polymer (SU8) was spin coated on top of the passivation layer of the IC. The thickness of the dielectric can be controlled by the spin speed. The thickness of the material depends on the viscosity, which is determined by the vendor. Viscous polymer need to be chosen for thick dielectric. In this work, SU8 2050 was used for 50 μm thick dielectric deposition. It is worth mentioning that the SU8 material is photo patternable.

After spin coating of polymer dielectric, photolithography was done to remove the dielectric on top of the PAD, as shown in Figure 3.1. At this stage, the dielectric

remains soft and some portion of the solvent remain inside. Hard baking was done for one hour at 150° C to remove the solvent. After the baking, the dielectric became strong, the measured elastic modulus was about 2 GPa. The dielectric strength was about 11 MV/cm, which is comparable to the silicon dioxide. Then, a 50 nm Ti/W layer was deposited as seed layer for electroplating. The Ti/W was also worked as adhesion layer between copper and the dielectric. Then copper was deposited using electroplating, and the overburden copper was removed by chemical mechanical polishing in the following step. Thus, the ultra-thick dielectric layer was achieved on top the passivation layer of BEOL. This thick dialectic will serve as a base of further processing. It will prevent substrate loss in the electromagnetic device, and also reduce the capacitive coupling.

3.2 Ultra-Thick Interconnect Metal Processing

To achieve a thick metal layer, another layer of dielectric was spin coated on top the thick dielectric. Then, a lithography was done to pattern the the dielectric. The aspect ratio of photopatternable SU8 dielectric can be very high (greater than 10) [3]. The detail fabrication process is described in Figure 3.2. Since, these deep trench patterns served as templates for metal tracks, the thickness of the metal directly proportional to the height of the trenches. Then, the trenches were filled by electroplated copper and polishing was done to remove overburden copper. It is worth mentioning that the temperature did not exceed 150° C during all these processes. Figure 3.3 shows the cross section of the wafer before and after the polishing process. It also shows that the void-free copper filled trenches, which will render ideal copper resistance during application. This thick metal processing will reduce the DC resistive loss in inductors.

In terms of CMOS compatibility, simple process steps were used in these technology, which includes photolithography, metal sputtering, electroplating and chemical mechanical polishing. These are the standard processes used in conventional BEOL.

Total number required photolithography steps would be one to three, depending upon the design. Most importantly, the process temperature was limited to 150° C. All these satisfied criteria justified the CMOS compatibility of the proposed technology.

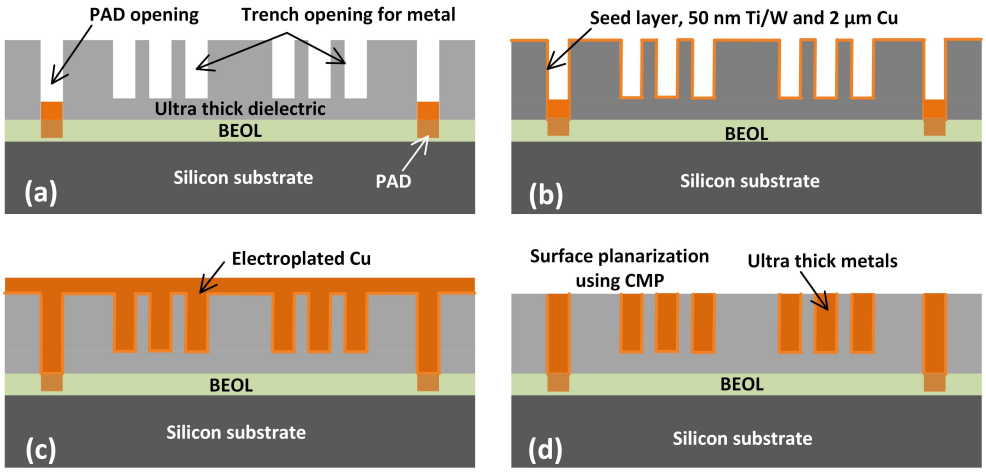

Figure 3.2: Fabrication steps of ultra-thick metal processing. (a) Deep trench patterns for thick metals, (b) Ti/W seed layer deposition for electroplating, (c) Copper electroplating, and (d) Overburden copper removal for thick metal tracks.

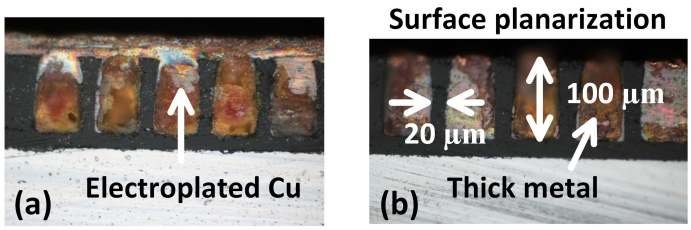

Figure 3.3: The cross-section of the wafer before (a) and after (b) the CMP process.

3.3 Engineered Interconnects for High Quality On-Chip Magnetics

Inductors were fabricated using above mentioned thick dielectric and metal processing. The micrograph of an inductor and its cross-section is shown in Figure 3.4(a). The dielectric thickness was about 50 μm and the metal thickness was about 40 μm. To

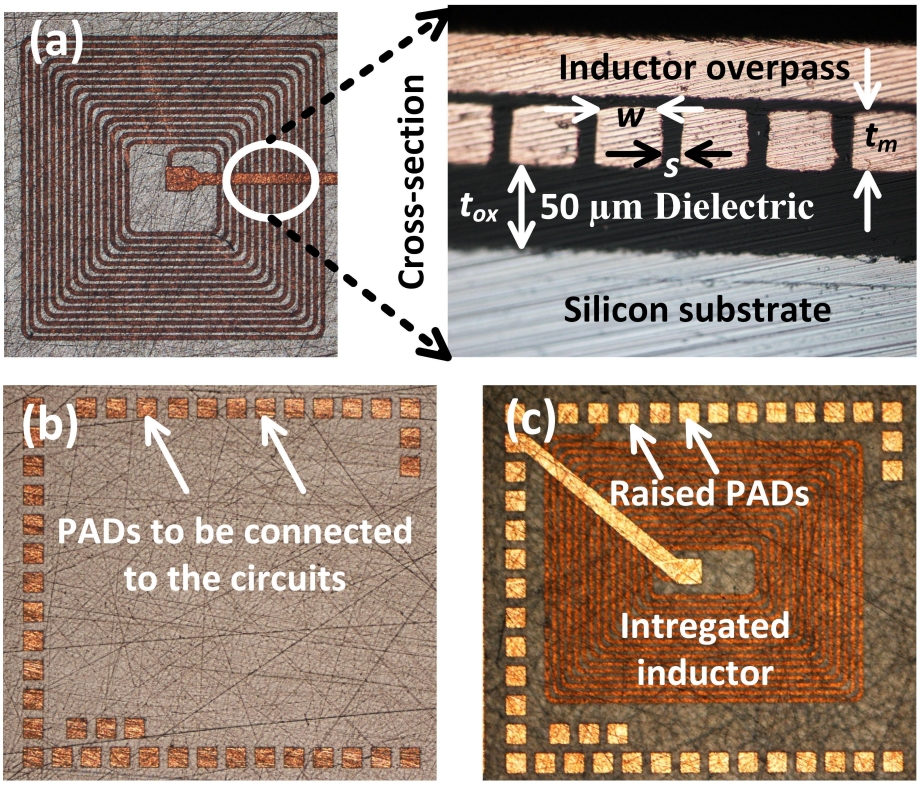

Figure 3.4: (a) The micrograph of a test-inductor and its cross-section. (b) Dummy PADs to mimic a CMOS chip configuration. (c) Integrated inductor.

demonstrate the CMOS integration capability, dummy PADs were created to mimic a CMOS die. When the inductor was fabricated on top of the IC, and the PADs were also raised in the process for external electrical connections, as shown in Figure 3.4(c).

3.3.1 Inductor Self-Resonance Frequency Improvement through Dielectric Engineering

Due to the thick dielectric in between the inductor metal tracks and the substrate, capacitance was reduced. The resonance frequency of the inductor was defined by $f_r = 1/\sqrt{LC}$. Here, L is the inductance value and C is the parasitic capacitance of the inductor. Due to the utilization of thick dielectric C is reduced, which contributed to the increased self-resonance frequency of the inductor. Multiple samples were prepared with different dielectric thicknesses. And the thickness dependency on self-resonance

frequency was studied. The measurement result is shown in Figure 3.5. When the dielectric thickness is 10 μm, the self-resonance frequency was at 100 MHz. But, the self-resonance frequency exceeded 300 MHz, when the inductor fabricated on top of 40 μm thick dielectric, as shown in Figure 3.5. Certainly, the self-resonance was improved due to the thick dielectric processing. The loss factor of the inductor is quantified by the quality factor, Q, quantitatively it is determined by $\omega L/R_S$, where the resistive loss is defined by R_S. The loss of the inductor is inversely proportional to the Q. At higher operating frequency the value of ωL increases, but at the same R_S increases a bit due to the skin effect. The skin depth, δ, of the metal is quantified by the operating frequency, f, and the conductivity, σ, of the metal. It is defined as $\delta = \sqrt{2/2\pi f\mu\sigma}$. If the skin depth is larger than the thickness of the metal tracks, R_S remains constant. In such a case, increase dielectric would be useful to reduce inductor loss. A benchmarking was performed to evaluate the improvement of the Q, as shown in Figure 3.6. The benchmarking was performed according to the TSMC 65 nm technology, in which top metal thickness was about 3.4 μm. At low frequency range, R_S remains unaffected by the operating frequency. That's why the is slight improvement of Q in the range of 10 MHz to 1 GHz. But, when the skin depth approaches the thickness of the metal, at frequency larger that 1 GHz, there was no improvement of the Q due to thick dielectric process.

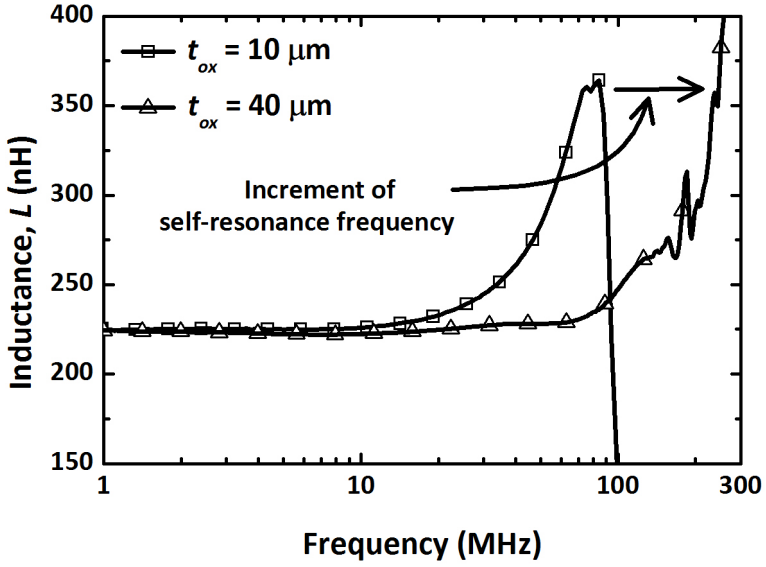

Figure 3.5: Improvement of self-resonance frequency due to thick dielectric.

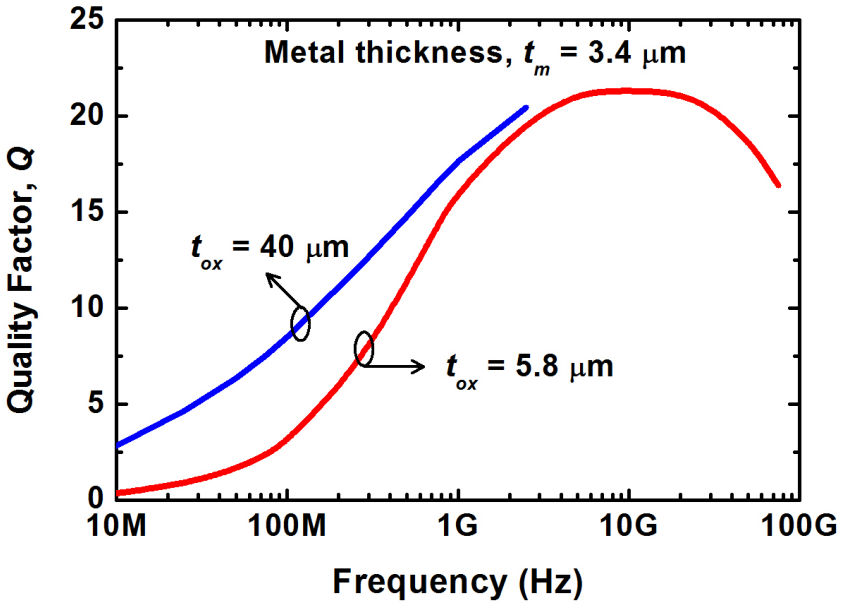

Figure 3.6: Benchmarking of thick dielectric process for integrated magnetics.

3.3.2 Resistive Loss Reduction in On-Chip Magnetics

There were two fundamental resistive losses in the inductor. One is the eddy current loss in the substrate, and another is resistive loss in the metal, which is discussed earlier. The substrate loss can be reduced by placing the inductor far away from the

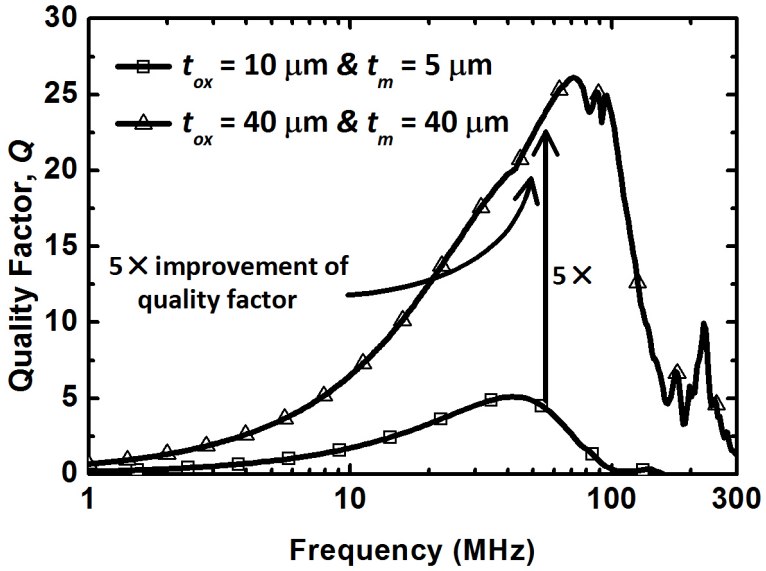

Figure 3.7: Improvement of indctor quality factor due to thick metal and dielectric.

substrate. By using the thick dielectrics, the substrate loss can be minimized. But the resistive loss will still be there due to thin metal. To minimize the resistive loss, thick metal processing technique was followed. For a low loss on-chip inductor both thick dielectric an metal process should be carried out. Figure 3.7 shows that the quality factor was improved five-fold due to the thick metal and dielectric processing. A benchmarking was also performed to show the theoretical effectiveness of the process, as shown in Figure 3.8. The benchmarking shows that significant improvement of of Q due to the thick metal and dielectric process. Effectively, this process is minimizing all losses of the interconnects associated with the integrated magnetics.

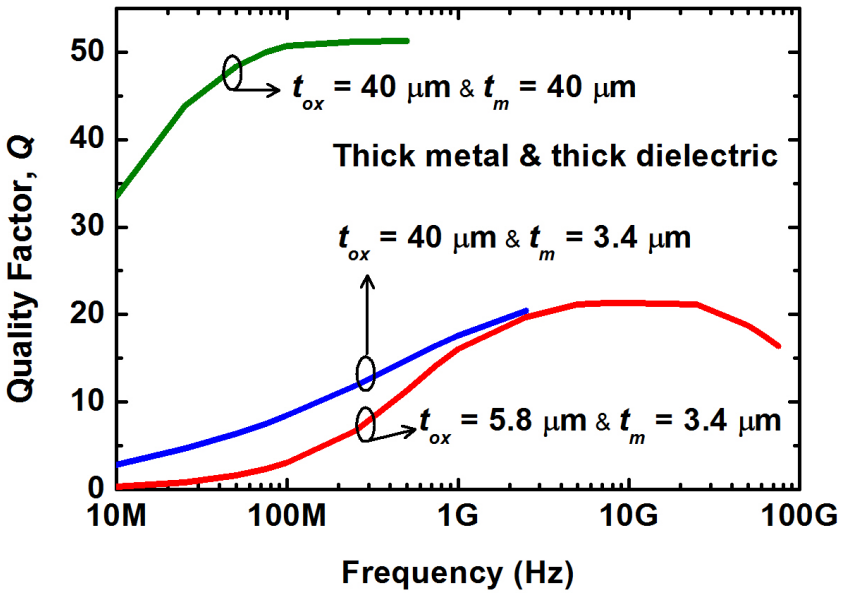

Figure 3.8: Benchmarking of thick dielectric and metal process for integrated magnetics.

On-chip large value inductor is one of the prerequisite of the integrated power management application. Integrate such a large value inductor is beyond the capability of the conventional interconnects. To demonstrate the effectiveness of the proposed interconnect technology, large value inductors were fabricated in top of a 10 Ω-cm silicon substrate. The area of the inductor was 4.5×4.5 mm^2. Various inductor turn numbers were used during the processing. By changing the turn numbers (N), measured inductances range from 3.47 μH to 4.4 μH with a peak quality factor Q_{Peak} range from 27 to 22 at 10–20 MHz frequencies, as shown in Figure 3.9. The DC resistance (R_{DC}) was reduced by increasing the thickness of the metal layer (Figure 3.10). As a result, a high L to R_{DC} ratio up to 1752 nH/Ω and the inductor efficiency of more than 90% [4] is achieved. These are state of the art figure of merits for power electronic applications [5], [6]. In any inductor technology, higher L and Q are desirable in the per-unit area of the silicon footprint to lower the solution cost. Hence, these two factors should be the ultimate metric for fair comparison among different technologies [7] – [19]. Mathematically, the Q and $L_{Density}$ product is defined as an equivalent performance curve. A comprehensive comparison is presented in Figure 3.11. Large inductance density may

be achievable using magnetic core but those inductor are very lossy, i.e. very low Q. Besides, there is a maximum currying capacity due to magnetic saturation. The air core inductors don't have such limitation. So, it is desirable to have large density inductors with high Q. The proposed integrated inductors fulfilled such stringent requirements, and can easily render an inductance density of 200 nH/mm^2, with a significantly high-Q (more than 20), to date, the best performance in leading magenitcs technologies, as compared in Figure 3.11.

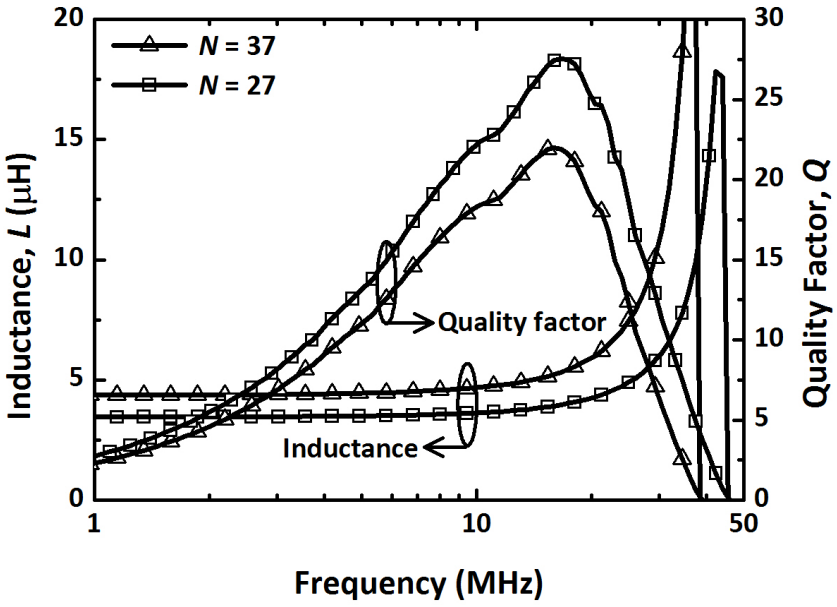

Figure 3.9: Frequency response of L and Q of 4.5×4.5 mm^2 inductors on top of a 10 Ω-cm substrate. Design parameters: track width $w = 30$ μm, spacing $s = 15$ μm, metal thickness $t_m = 40$ μm, bottom dielectric thickness $t_{ox} = 50$ μm, and turn number $N =$ 37 and 27.

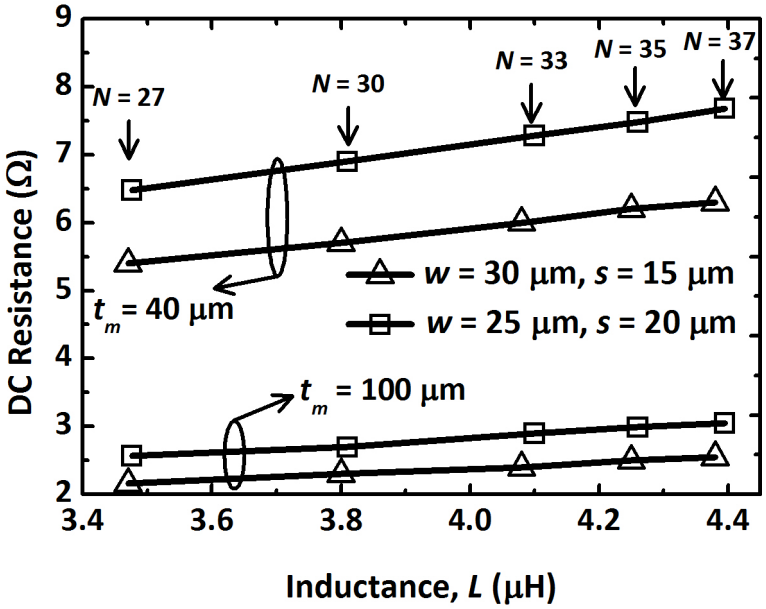

Figure 3.10: DC resistance was reduced by increasing the thickness of the metal (t_m).

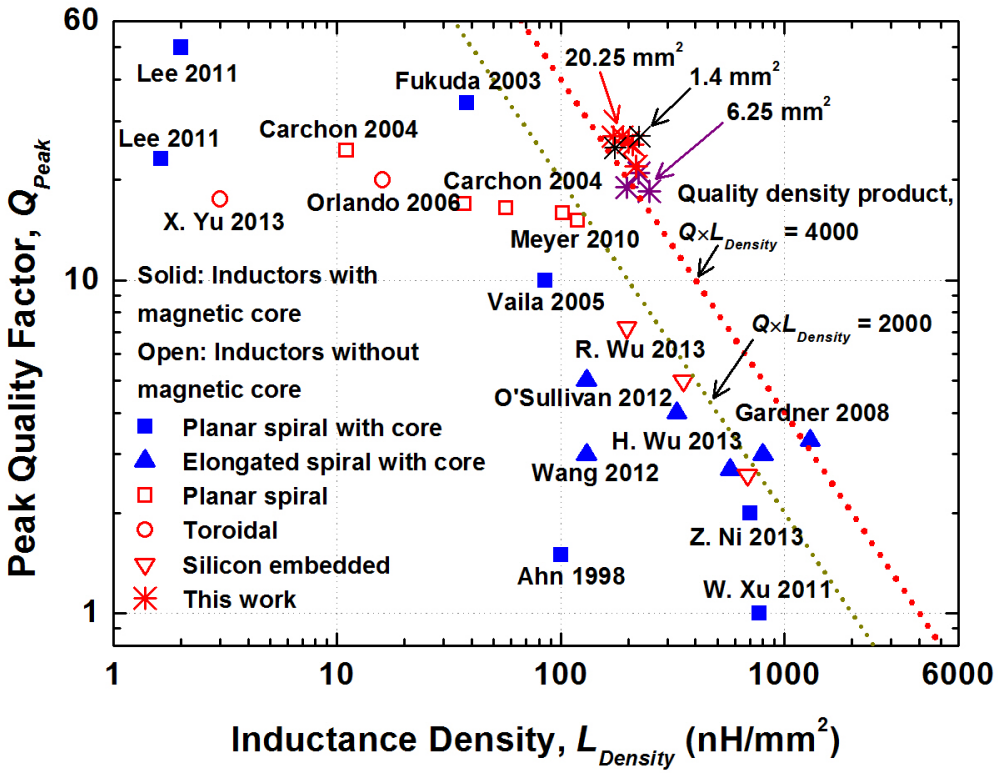

Figure 3.11: Measured peak quality factor (Q) and inductance density ($L_{Density}$) of the leading technologies for inductor integration on silicon. Here, $L_{Density}$ is defined as inductance per mm^2.

3.4 Engineered Interconnects for Power Supply On-Chip

To demonstrate integration capability the proposed ultra-thick dielectric and metal interconnects, a complete system was implemented for wireless power supply on-chip. The wireless power system requires a power management circuitry which converts the wirelessly-coupled RF signal into a stable DC supply voltage. The schematic of the wireless power supply system is described in Figure 3.12. The RF power transmitted from the primary transmitting inductor (L_1) to the secondary power receiving coil (L_2). The rectifier converts the coupled RF signal to usable DC source [20] – [23]. This integrated inductor could replace the traditional PCB or wire–wound inductors which usually take up a few cm. The ultra-thick dielectric and metal interconnect, as described in Figure 3.1 and 3.2, was used for implementing the receiving inductor on top of the CMOS chip. The design parameters are summarized in Table 3.1.

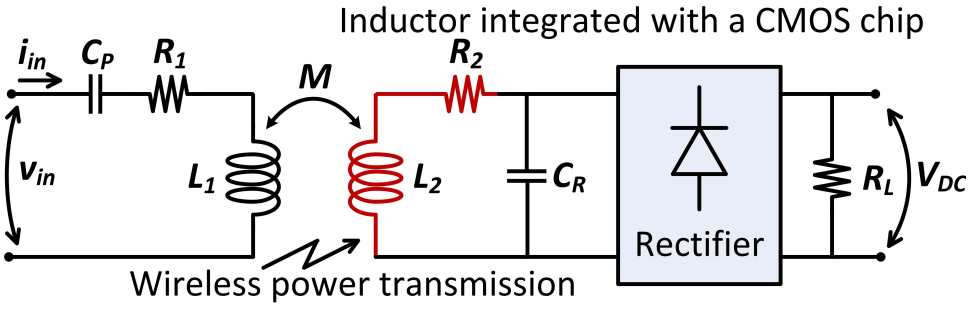

Figure 3.12: Complete schematic diagram of a wireless power system on-chip.

The ability of capturing electromagnetic energy by an inductor mainly depends on the number of turns (N) in a particular area [1] and the Q value. The integrated inductor offers significant advantages in terms of these metrics. The higher $L_{Density}$ lowers the required capacitance to the sub–100 pF range for operation frequency in the MHz range as shown in Figure 3.13. As a result, the proposed interconnect technology can effectively reduce the overall silicon footprint of a power electronic module.

Table 3.1: Design parameters of the on-chip wireless power supply system.

Specifications	Power Transmitting Inductor (Tx)	Power Receiving Inductor-1 (Rx-1)	Power Receiving Inductor-2 (Rx-2)
Inductor Area	20×20 mm^2	2.5×2.5 mm^2	1.1×1.3 mm^2
Technology	PCB	Proposed	Proposed
Turn Number	3	13	15
Metal Width	700 μm	30 μm	17.5 μm
Metal Spacing	300 μm	30 μm	12.5 μm
Inductance	250 nH	380 nH	175 nH
Quality Factor	81 at 27 MHz and 95 at 40 MHz	21 at 27 MHz	23 at 40 MHz

The detailed measurement setup is shown in Figure 3.13, and the results are described in Figure 3.14, Figure 3.15 and Figure 3.16, respectively. The mm–size receiver can harvest 27 mW to 1.1 mW power in a transmission distance ranging from 5.3 to 21.3 mm from a 250–mW transmitter as shown in Figure 3.15. More power could be harvested by the inductor by supplying more power from the transmitter. However, the rectifier IC has a breakdown voltage of about 7 V. To avoid breakdown, lower transmitted power was adopted to keep the DC voltage across the load to below 5 V, as shown in Figure 3.16.

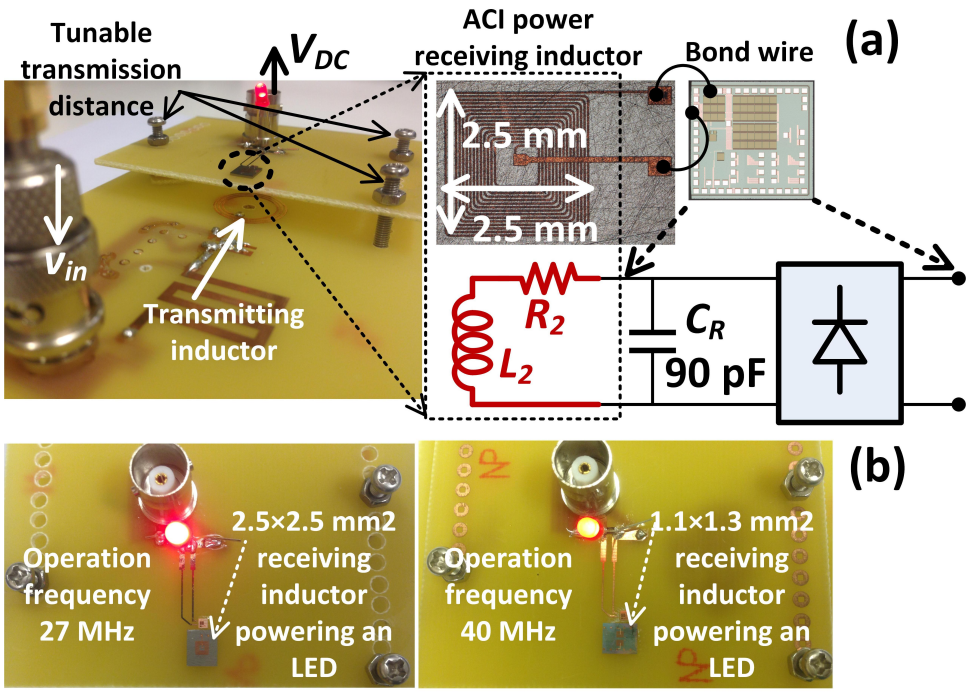

Figure 3.13: (a) The experimental setup for measuring the characteristics of the wireless power transmission system. (b) The mm-size power receiving inductor is powering an LED at 10 mm distance.

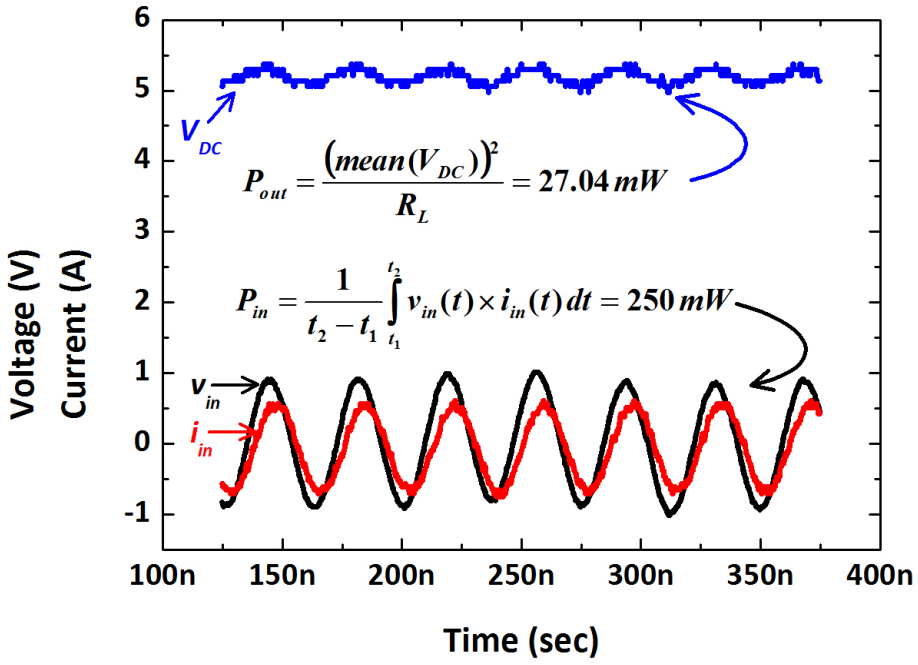

Figure 3.14: Time domain measurement of transmitting signals v_{in} and i_{in}, and the received DC voltage V_{DC} across the 1 KΩ load resistance, at 5.3 mm distance. The efficiency was calculated as $\eta = P_{out}/P_{in} = 10.8\%$.

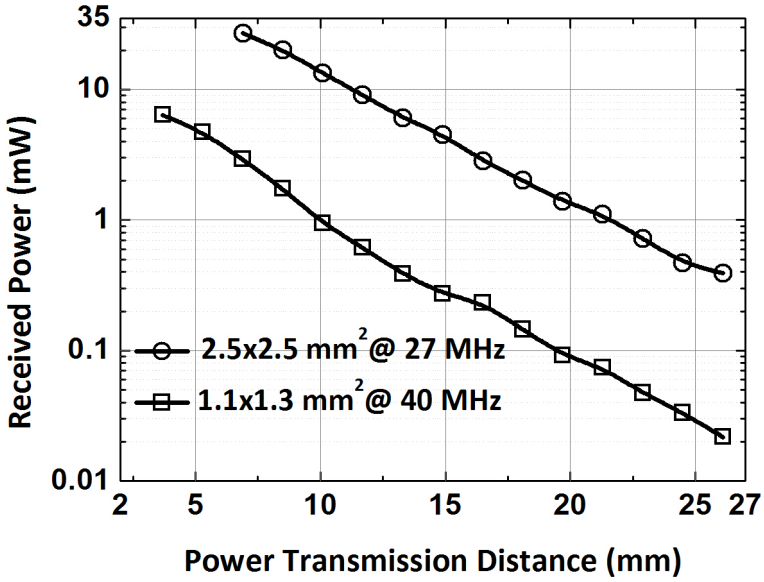

Figure 3.15: Received power by the mm–size wireless power receiver at different transmission distances, provided that the transmitted power was 250 mW.

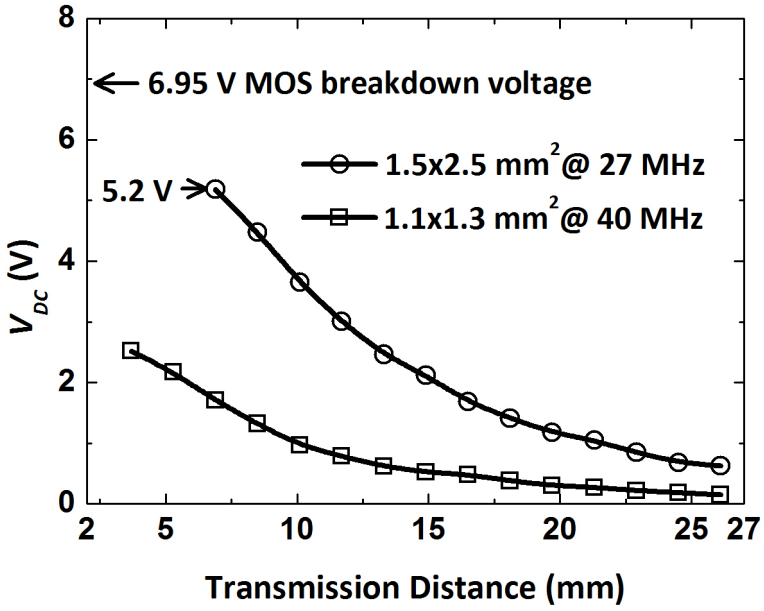

Figure 3.16: Measured rectified DC voltage across the load resistance ($R_L = 1$ KΩ) at different transmission distances.

A comparison is presented to evaluate the performance of the proposed on-chip wireless power supply system with others reported in the literature. Due to the different inductor technologies and sizes used, the received power per unit area ($P_{Density}$)

and the normalized transmission distance (D) are used as the performance metric for a fair comparison. The received $P_{Density}$ inversely varies with D^3. It is mainly due the reduction of mutual coupling between the transmitter and receiver [24]. Hence, the equivalent performance curve is defined as $P_{Density} \times D^3$. Figure 3.17 shows the received power density at different transmission distances. In terms of performance, the data presented at the right hand side of the equivalent performance curve is superior than the left, i.e. it was expected to receive large power at a long transmission distance. Figure 3.17 shows that the proposed wireless power transmission system outperforms any other technologies reported in the literature [25] – [35], transmitting mW levels of power even at a distance 10 times larger than the antenna size.

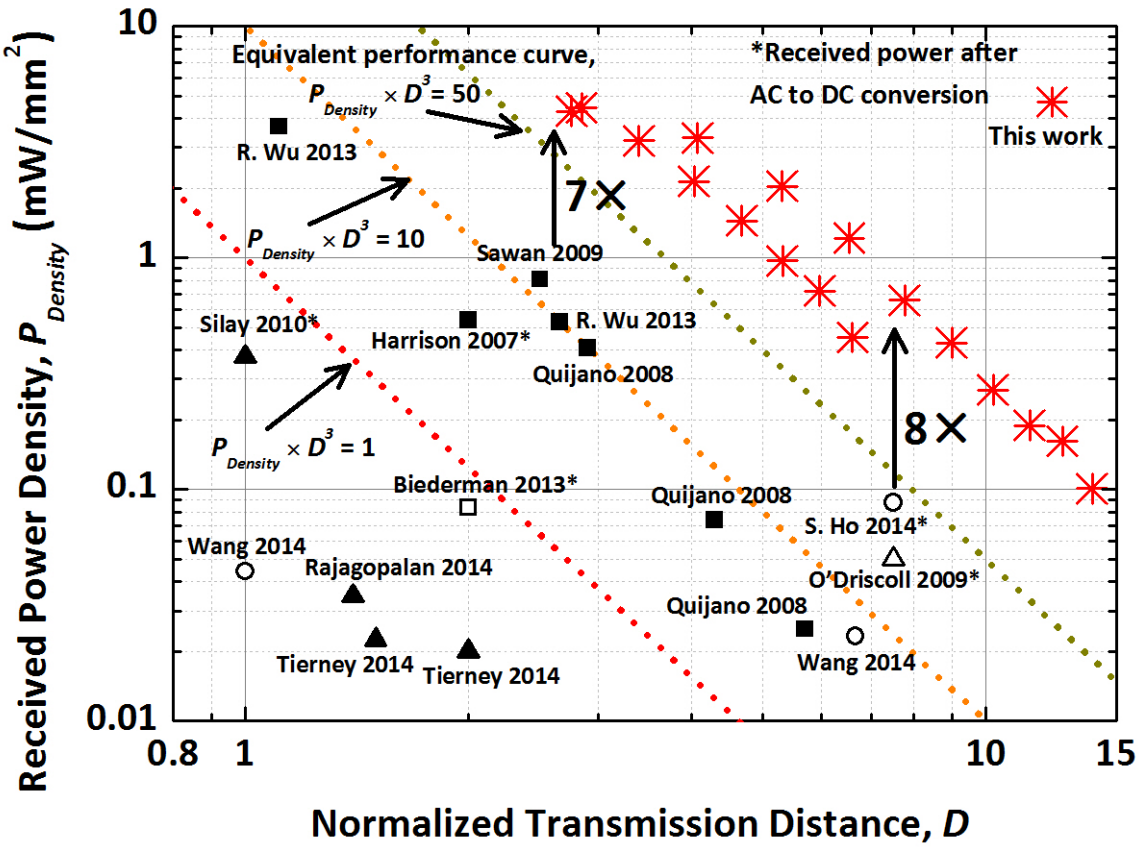

Figure 3.17: Summary of reported wireless power transmission systems with different inductor integration schemes in the literature. The normalize transmission distance, D, is defined as the ratio of transmission distance and the size of the power receiving inductor, and the received power density is defined as– $P_{Density} = P_{out}/Area = P_{in} \times \eta/Area$.

3.5 Conclusion on Engineered Interconnects

This work presented an interconnect technology in which ultra-thick dielectrics and metal were used. This interconnect technology proved to be useful to reduce losses in on-chip magnetics. Effectiveness of this technology was demonstrated by implementing large value high performance inductors. The fully integrated 4.5×4.5 mm^2 inductor can render 4.3 μH inductance, with a density of 200 nH/mm^2, on a low resistivity substrate while achieving a peak quality factor of 26. To demonstrate the application of this interconnect technology in miniaturized on-chip wireless power supply was implemented. A 2.5×2.5 mm^2 wireless power–receiving system was designed. It can wirelessly receive 27 mW from a 250 mW 27 MHz transmitting signal at a distance of 5.3 mm, and 1.1 mW at a distance of 21.3 mm. It is the best reported performance compared with published data.

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Chapter 4

Mitigation of Interconnect Radiation Loss on Silicon

On-chip integrated antenna on silicon is promising as radiating wavelength approaches in millimeter wave band. The millimeter wave band is defined as the portion of the electromagnetics spectrum extending from 30–300 GHz with corresponding wavelengths range of 10–1 mm. The millimeter wave frequencies were widely used for defense and radio astronomy applications. However, it is less commercially available, mainly due to high cost. The recent years millimeter wave consumer applications markets, such as automotive radars, high-resolution imaging and high-speed data transmission, rapidly growing. There is a necessity of development of highly integrated, and low cost wireless systems including high efficiency on-chip planar antennas. On-chip planar antennas have gained a lot of interest in the past years [1]–[7] for millimeter wave applications due to their integrated nature, ease of low cost fabrication and potential for high efficiency operation. The small wavelength at millimeter wave frequencies is an advantage for the design of small and efficient antennas. The size of the antenna is a fraction, typically one-half or one-quarter, of the operating wavelength. Therefore, millimeter wave f = 30–300 GHz (λ = 10–1 mm), it is feasible to build on-chip antennas that are physically small and at the same time electrically large enough to radiate electromagnetic wave.

However, the design of such millimeter wave antennas on silicon is challenging because of low radiation efficiency. The source of low radiation efficiency of on-chip antenna is mainly due to the low resistivity (10 Ω-cm), and high permittivity ($\epsilon_r = 11.9$) silicon substrate.

In this chapter, an interconnect technology is proposed to minimize the radiation loss of on-chip antennas. Utilizing the technology a broadband millimeter wave antenna was implemented and integrated to the CMOS chip to demonstrate the efficacy of the technology.

4.1 Improved Radiation Efficiency through Thick Dielectric Processing

When an antenna implemented on a silicon substrate substrate, two major loss mechanism dominates for low radiation efficiency. The first one is the conduction loss due to the conductive silicon substrate, and another is the surface-wave (SW) mode excitation [8] created by the thick silicon substrate with high permittivity. These two losses can be easily avoided if the radiated signal can be isolated form the lossy silicon substrate by using the lower metals as a screening ground plane. However, there will be another loss mechanism will be introduced to the antenna. Typically the dielectric thickness of the of the back end of line (BEOL) is about 10–15 μm. It is difficult to radiate energy to the space on top of a thin dielectric. Moreover, this very thin dielectric compared the the radiation wavelength will create a large conduction loss in the metal trace.

In addition to the thin dielectric, a minimum metal density is often required in the BEOL by the foundry in order to ensure the wafer planarity during the fabrication process. Metal fillers often added by the foundry to obtain minimum metal density.

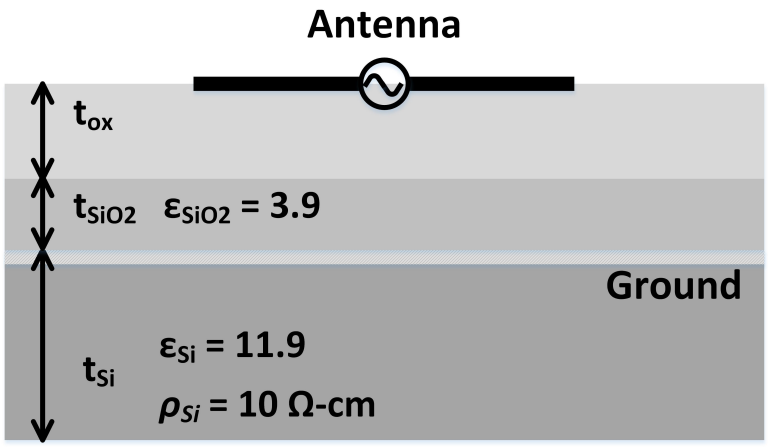


Figure 4.1: Cross-section of the thick dielectric process technology to reduce on-chip radiation loss.

These metal fillers increases the effective dielectric constant and loss tangent (tan δ) of the under layer dielectric [9], [10]. This will create additional degradation in antenna performance. Also, some foundry requires a chip-ring, usually by metal, that encloses the chip components in order to protect them from cracks during dicing. This chip-ring may interfere with the on-chip antenna, and could create unwanted radiation pattern.

To eliminate all those above mentioned effects, a thick dielectric process technology to reduce on-chip radiation loss. A chip cross-section is shown in Figure 4.1 to explain the process technology. A thick dielectric is place on top of the BEOL. This dielectric separates the antenna form the substrate and all non idealities of the BEOL. The permittivity of the proposed dielectric was about 2.8 [11]. Effectiveness of the proposed technology was investigated by evaluating antenna radiation efficiency with different dielectric thickness. A simple dipole was used for this investigation and the radiation frequency was 60 GHz. The dependency of oxide thickness on the radiation efficiency is shown in Figure 4.2. The radiation efficiency increases simply by using thick dielectric. All spurious effect, such as substrate surface wave, was eliminated by shielding the BEOL using a ground plane, as shown in Figure 4.1. The radiation pattern at different oxide thckness was also investigated, as shown in Figure 4.3. The antenna gain was improved

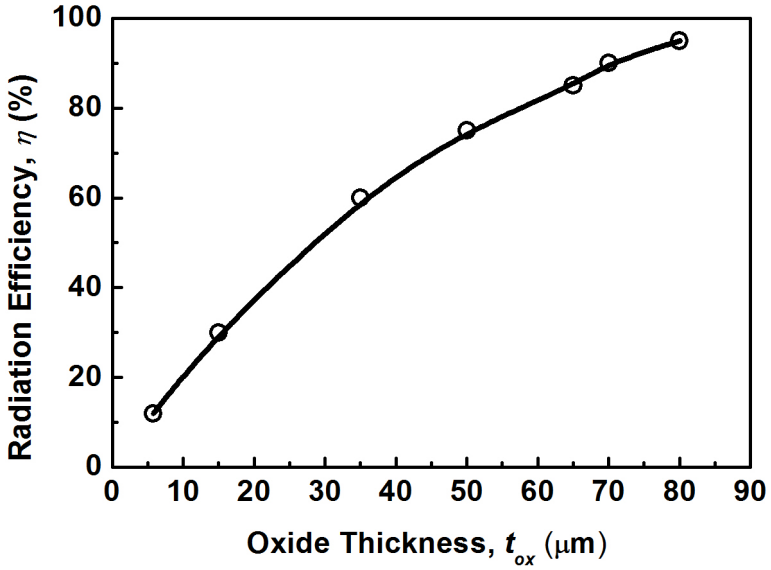


Figure 4.2: The dependency of oxide thickness on the radiation efficiency.

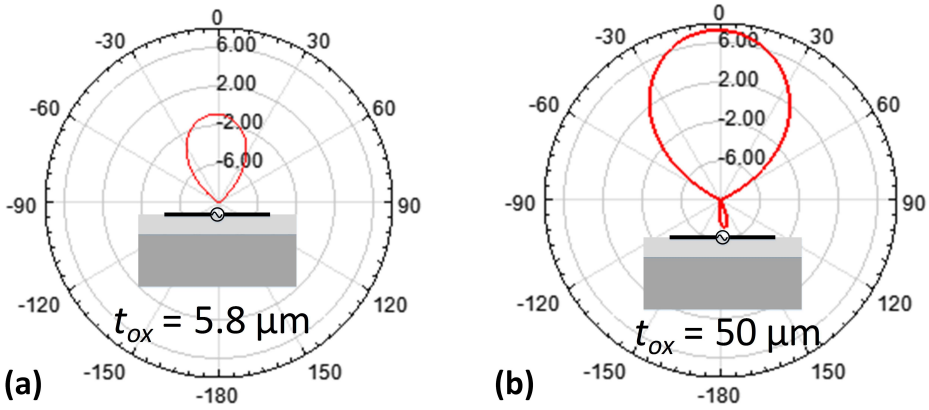


Figure 4.3: Antenna radiation pattern at different oxide thickness.

simply by using thicker oxide.

The planar inverted-F antenna (PIFA) antenna is a very popular compact antenna [12] which has extensive use in mobile communication [13]. Typically this antenna implemented on printed circuit board. PIFA antennas have been implemented on a modified silicon substrates using proton implantation or silicon-on-quartz [14], it has a good performance at frequencies up to 20 GHz. However, such technology is prohibitive for CMOS due to compatibility issue. The CMOS compatible thick dielectric process technology has been utilized to implement a PIFA antenna which operates at 60 GHz. The

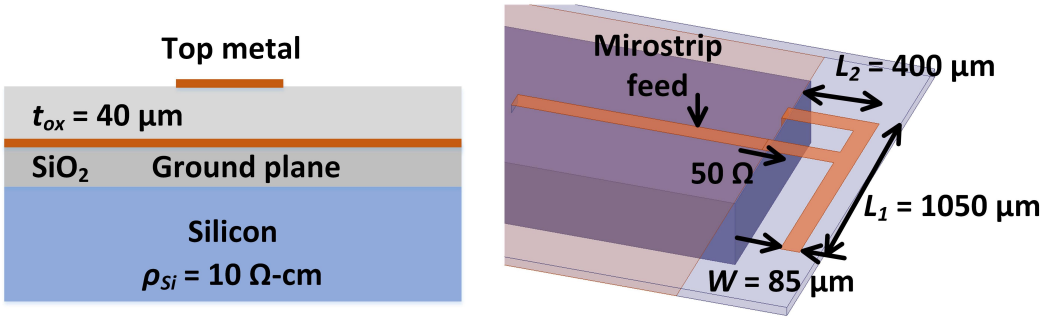


Figure 4.4: Cross-sectional view and layout of an an-chip planar inverted-F (PIFA) antenna.

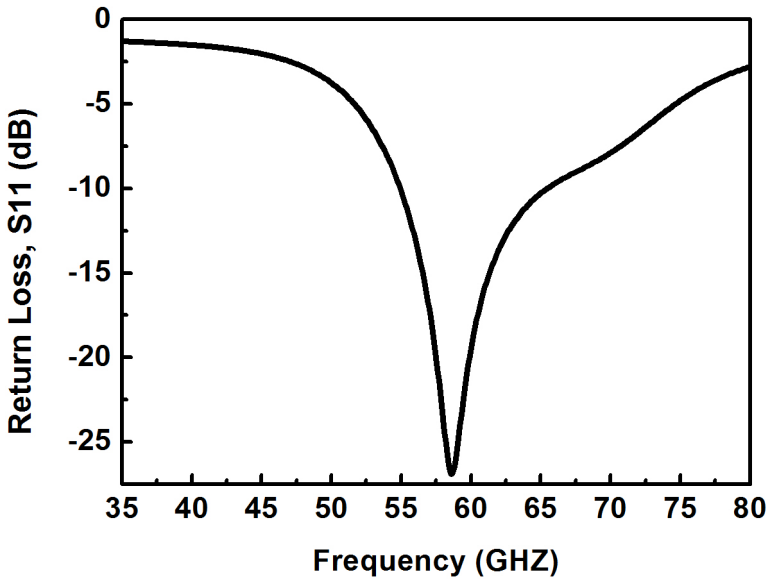


Figure 4.5: Return loss (S11) of the PIFA antenna implemented on thick dielectric process technology.

cross-sectional and top layout view is shown in Figure 4.4. The PIFA antenna consists of a horizontal line (L_1), a short vertical line (L_2), a signal-driven vertical line, and a ground plane, as shown in Figure 4.4. The total length of the PIFA antenna is comparable to $\lambda/4$, that's why small silicon footprint is required for this antenna. In particular, $L_1 + L_2 = \lambda/4$. The return loss of the antenna was evaluated as shown in Figure 4.5. It shows good matching at 60 GHz and has a bandwidth of 7 GHz. The efficiency of the antenna was about 84%.

A large ground plane was chosen for efficient radiation. If the ground plane is

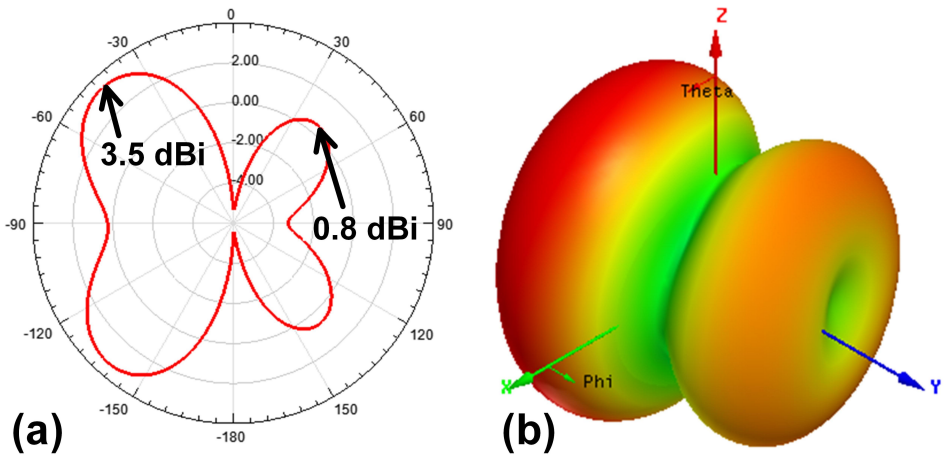


Figure 4.6: Radiation pattern of on-chip PIFA antenna.

not large enough, it works as a radiator. The edge of the smaller ground plane could diffract the wave to create multiple side lobes. The smaller ground plane could affect the radiation pattern and overall gain of the antenna. The radiation pattern and the gain of the antenna was investigated. The simulation results for radiation pattern is shown in Figure 4.6. Peak gain of 3.5 dBi can achieved at 60 GHz. The peak gain of the PIFA antenna also investigated at different frequency, as shown in Figure 4.6. The peak gain is about 3.5 dBi within the bandwidth of interest.

4.2 Broadband Millimeter-Wave On-Chip Planar Antennas

Broad antenna bandwidth is a necessary requirement for high speed wireless data communication. Antenna can be designed to have a very broad bandwidth and a relatively large gain. But, the size of those antennas usually several wavelengths long [15]–[17]. It is challenging to implement an broadband on-chip antenna with a high gain. The losses in the antenna should be as small as possible to obtain large signal to noise ratio in wireless data communication. Since, the antenna loss directly associated with

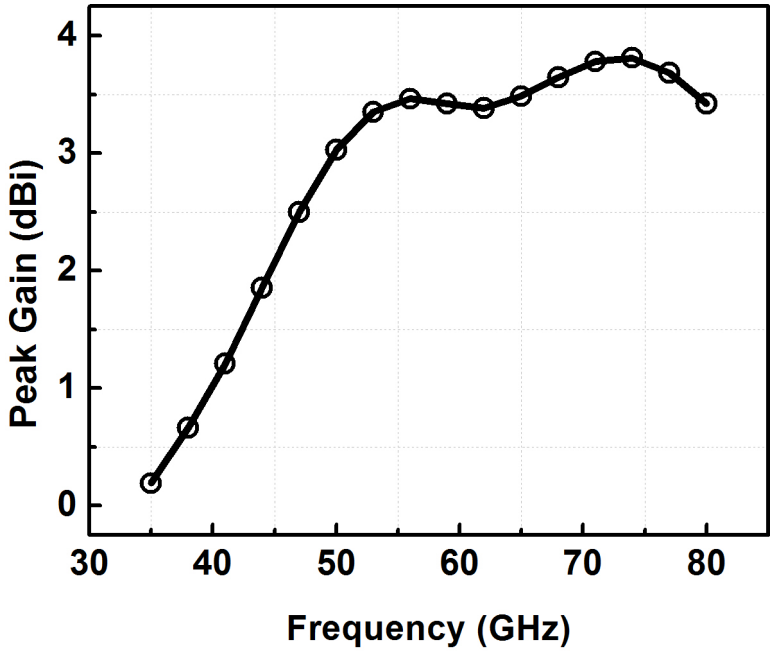


Figure 4.7: Peak gain of PIFA antenna at frequency.

antenna efficiency, it is also absolutely necessary to achieve high efficiency of an on-chip antenna, so that all input RF power radiates to the space.

Monopole antenna has been chosen for broadband application. The monopole antenna has several advantages compared to its half-wavelength counter part.

- The footprint is half of the corresponding dipole.
- The directivity improves by a factor of two.
- Broadband impedance matching compared to dipole.

Figure 4.8 presents the layout of a planar triangular broadband monopole antenna. The cross-sectional view of the antenna is also shown in Figure 4.8. The feeding input of the micro-strip line was 50 Ω. The micro-strip line was used as a quarter wave length impedance matching network. The length, L_1 of the triangle was chosen to be 1800 μm. At the beginning of the design process the flare angle, α, was varied. The input impedance of the antenna can be tuned by varying the flare angle. Three dimensional electromagnetic simulation, using HFSS, was performed to find out a flat impedance range for broadband matching. Figure 4.9 shows the resistance and reactance of the a

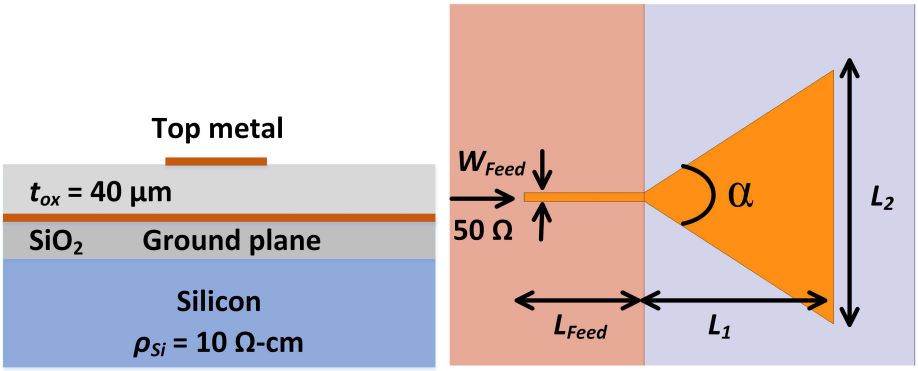


Figure 4.8: Cross-sectional view and top view of a triangular monopole antenna implemented by thick dielectric porocess technology.

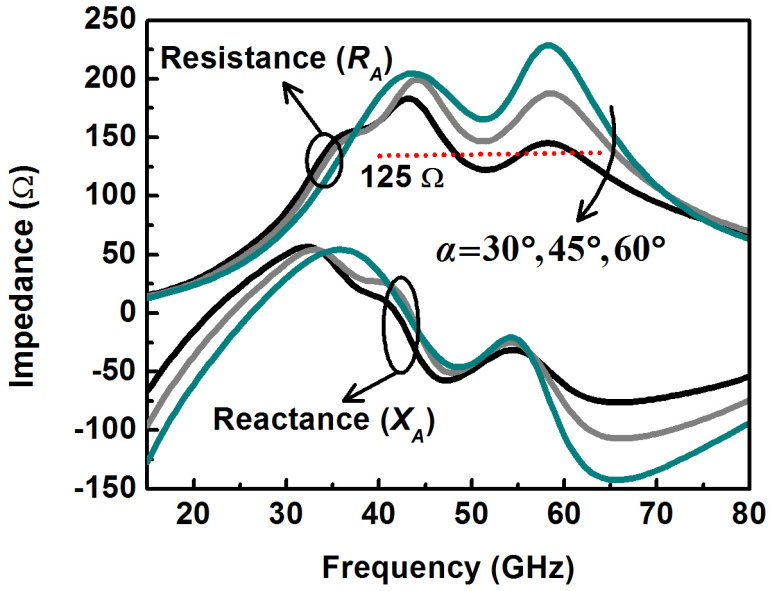


Figure 4.9: Input impedance of a triangular moropole antenna with different flare angles.

monopole antenna at flare angles of 30°, 45° and 60°. When the flare angle is 60° the resistance become flat over a large frequency range, i.e impedance become less sensitive to the frequency. A quarter wave micro-strip line was used to match the antenna input impedance to 50 Ω. The micro-strip dimensions are: W_{Feed} = 80 μm, and L_{Feed} = 1140 μm. The return loss of the triangular monopole is shown in Figure 4.10. The bandwidht changes depending on the flare angle of the antenna. A bandwidth of 26 GHz can be achieve, centering at 60 GHz can be achieved when the flare angle is 60°.

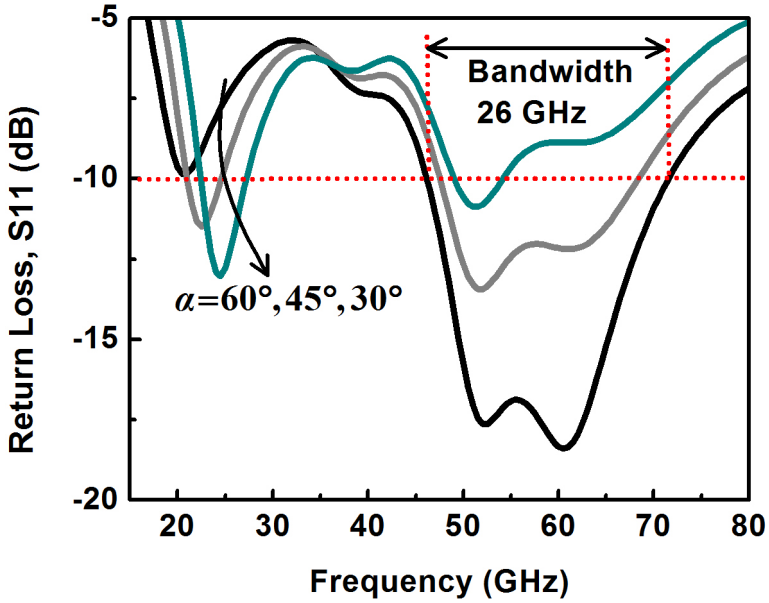


Figure 4.10: Return loss (S11) of the triangular monopole antenna at flare angle of 30°, 45° and 60°.

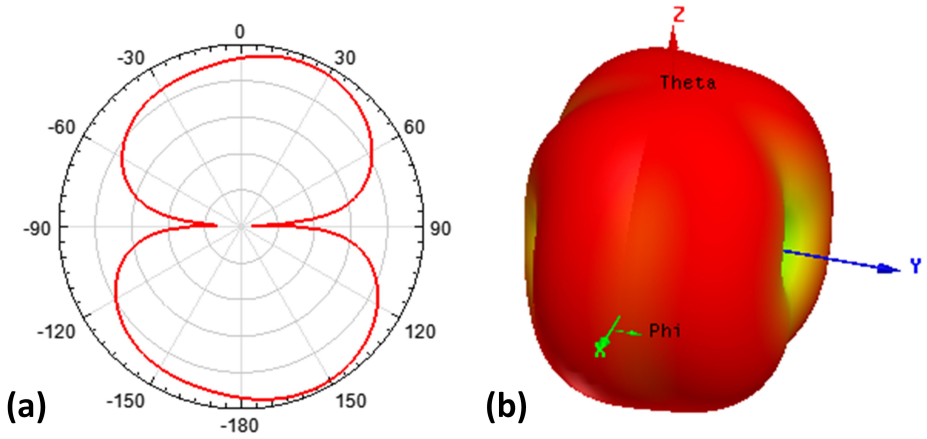


Figure 4.11: Radiation pattern of micro-strip fed triangular monopole antenna.

The antenna radiation pattern was also investigated. Figure 4.11 shows the radiation pattern of micro-strip fed triangular monopole antenna at 60 GHz. The gain was about 3.5 dB and the efficiency of antenna was about 90%.

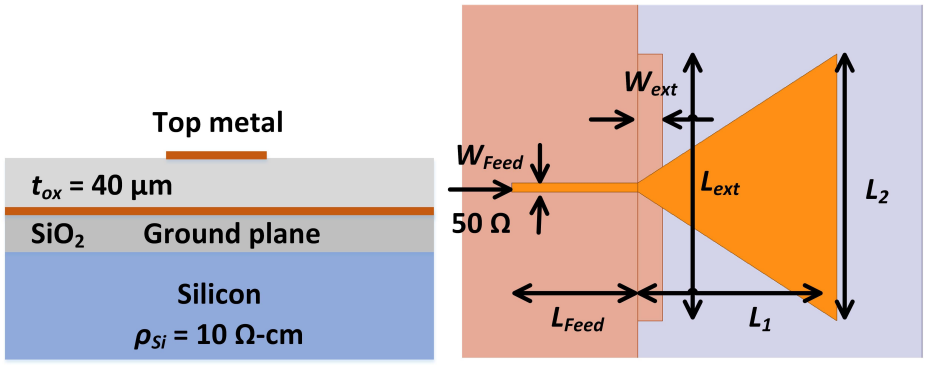


Figure 4.12: Cross-sectional and top view of a triangular sleeve monopole antenna.

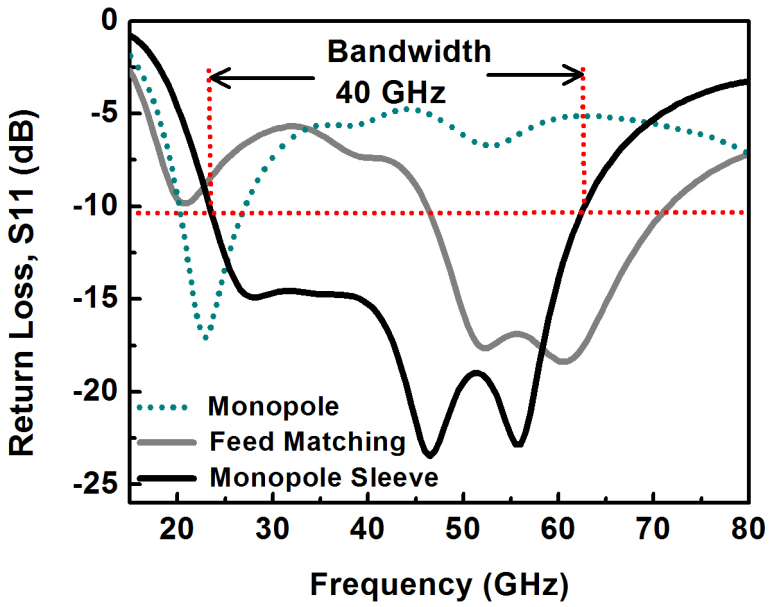


Figure 4.13: Return loss (S11) triangular monopole antenna, monopole antenna with quarter wave matching and triangular sleeve monopole antenna.

The bandwidth of the antenna was further improved by introducing a sleeve. Figure 4.12 described the configuration of the on-chip triangular sleeve monopole antenna. A portion of the ground plane was extended underneath the triangle, that works as a sleeve. The sleeve operates as a virtual feed point of the antenna. During operation, effective antenna length varies in between L_1 and $L_1 + W_{ext}$ due to this virtual feed point. Large sleeve length implies that the bandwidth of the antenna would be very wide. Theoretically, sleeve length may be any portion of L_1, but large extension of the sleeve may change the input impedance of the antenna. But, when the sleeve length,

the input impedance remains unchanged. It requires some iterations in simulation to find out the maximum allowed length of the sleeve. Complete design parameters of the sleeve monopole are: $W_{feed} = 80$ μm, $L_{feed} = 80$ μm, $W_{ext} = 225$ μm, $L_{ext} = 2700$ μm, $L_2 = 1200$ μm, and $L_1 = 1800$ μm.

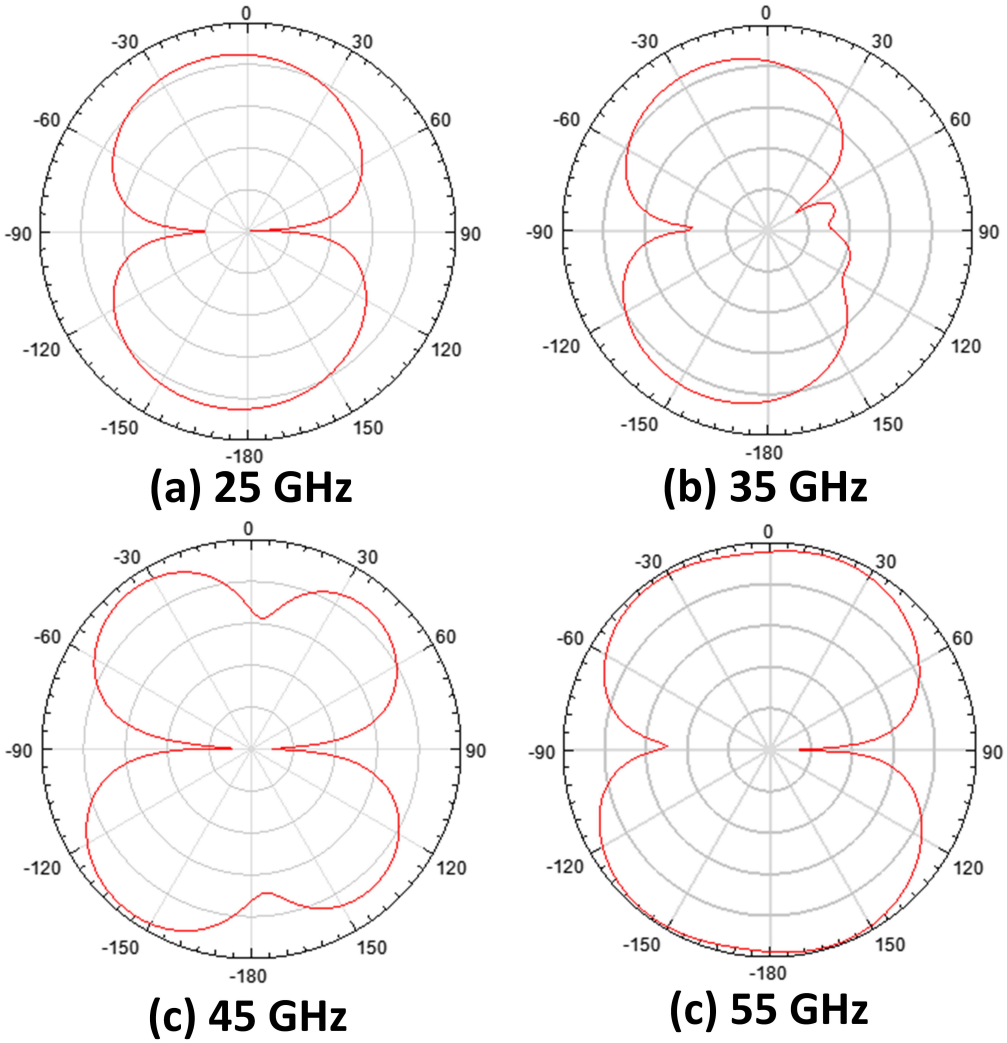


Figure 4.14: Radiation pattern of the micro-strip fed triangular sleeve monopole antenna at different operation frequency.

For comparison, return loss (S11) triangular monopole antenna, monopole antenna with quarter wave matching and triangular sleeve monopole antenna are shown in Figure 4.13. The resonance frequency of just the monopole antenna was at 23 GHz. Due to the feed matching the operation frequency was extended to 60 GHz. At that

time, the bandwidth was about 26 GHz. After introduction of the sleeve, the bandwidth of the monopole extend to 23 GHz to 63 GHz, about 40 GHz, as shown in Figure 4.13. The fractional bandwidth of the antenna is about 93% of the center frequency of 43 GHz. The radiation pattern of the micro-strip fed triangular sleeve monopole antenna is shown in Figure 4.14. The antenna showed almost omnidirectional radiation patterns over all frequency of interest. The antenna gain at different operation frequency is shown in Figure 4.15. The peak gain remained more 3 dBi over the whole bandwidth. The efficiency of the antenna remained same as the micro-strip fed triangular monopole antenna, it was about 98%.

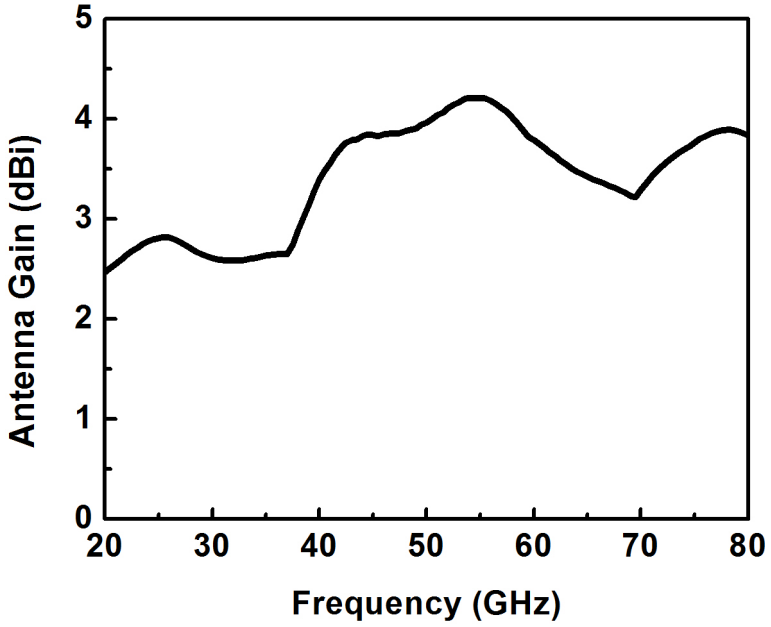
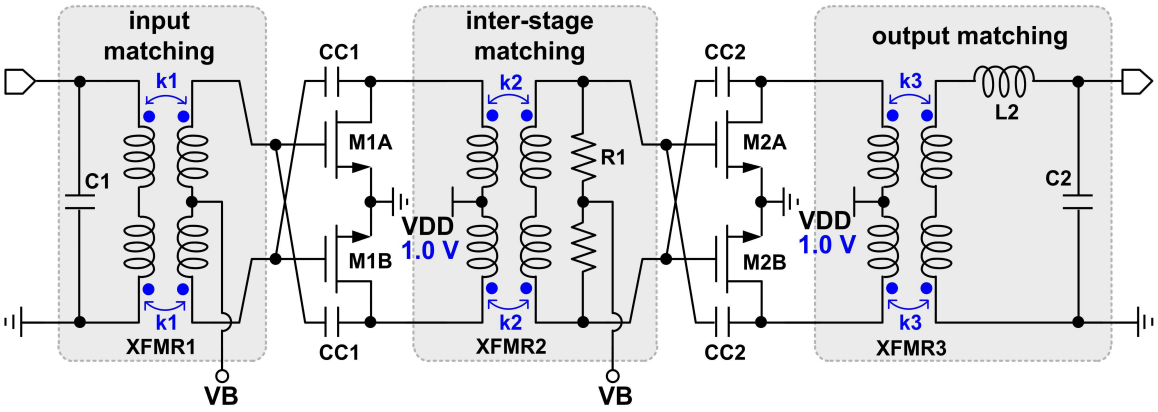


Figure 4.15: Peak gain of the micro-strip fed triangular sleeve monopole antenna at different operation frequency.

4.3 Integration of On-Chip Antenna with BEOL and System Demonstration

To demonstrate the integration capability of the proposed thick dielectric process technology, a broadband millimeter-wave power amplifier is designed in TSMC 65 nm



M1A/M1B	CC1	M2A/M2B	CC2
64μm/60nm	23fF	128μm/60nm	45fF

Figure 4.16: The schematic diagram of a wideband power amplifier (PA) [18] for 5th generation (5G) wireless system.

CMOS technology. The schematic diagram of the proposed power amplifier is shown in Figure 4.16. The wide bandwidth is desirable [19]–[23] to facilitate high data-rate wireless communications. This wide bandwidth millimeter-wave technology is becoming lucrative, especially for 5th generation (5G) wireless system and radar system. The power amplifier has two amplification stages. The value and sizes of the circuit components are shown in Figure 4.16. Coupled resonator based wideband matching technique via transformers were used in all the matching networks. As a result, the fractional bandwidth of the power amplifer was 63.3% from 21.6 to 41.6 GHz. The chip micrograph of the power amlifier is shown in Figure 4.17. According to the measurement results, the power amplifier can has an efficiency of 33% and can deliver 15 dBm power over the entire bandwidth.

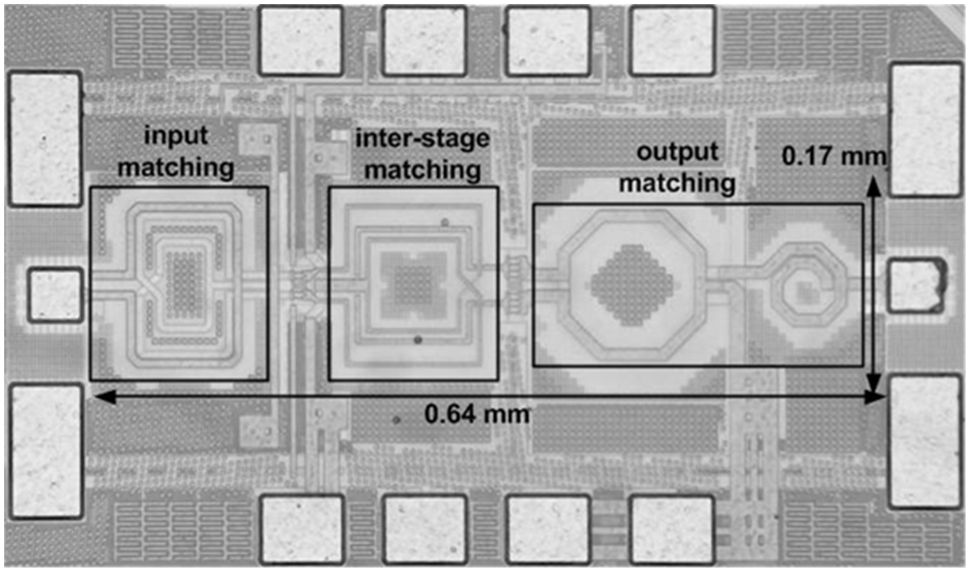


Figure 4.17: The micrograph of the wideband power amplifier (PA), the core area of which is 0.64×0.17 mm^2 [18].

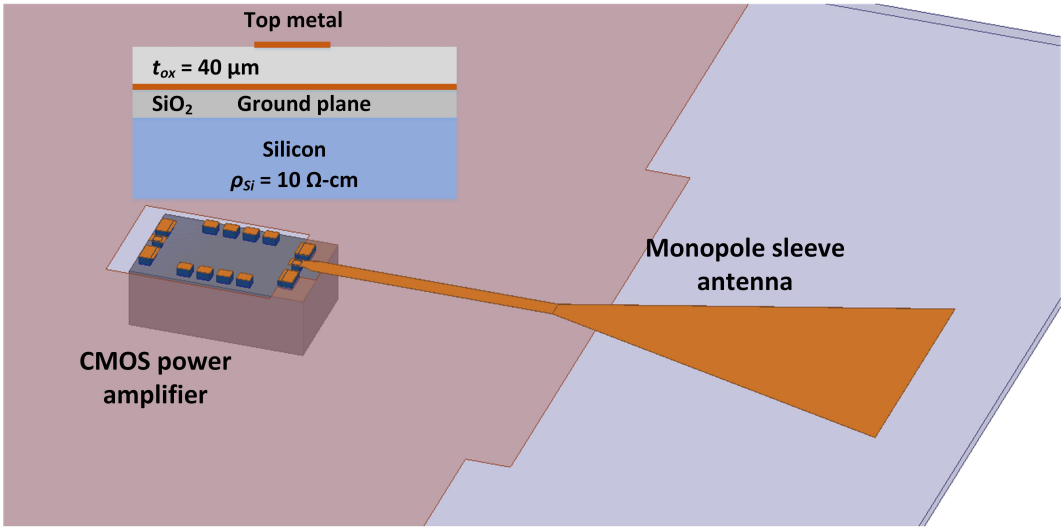


Figure 4.18: Integration of a thick dielectric base chip antenna with a foundry fabricate IC.

Figure 4.18 shows the integration of thick dielectric based chip antenna with a foundry fabricated power amplifier IC. The power amplifier chip was mounted on top of a supporting wafer. Dummy dies were placed in the four corner of the chip mechanical support during fabrication. The height of the dummy chip was same as the height of the chip. At the beginning of the process, a thin layer, about 10 μm, polymer (SU8) was

spin coated on top of the passivation layer of the IC. Then, 1 μm copper was deposited, which works the ground plane of the antenna. The thin dielectric actually separated the antenna ground plane and the top metal layer of the IC. Also there was no ground plane of the top of the IC, this helped minimize the noise coupling to the IC. Then, a thick layer, about 40 μm, of dielectric was deposited on top, which works as the substrate of the antennas. Finally, another metal layer was deposited for the antenna. It should be mentioned that during the processing all PAD of the chip also raised, as show in Figure 4.18. Since all PADs were raised and exposed from the top, the electrical connection of the chip was similar to that of isolated chip. At the end of the process, all dummy die and supporting wafer was removed leaving an antenna integrated CMOS IC.

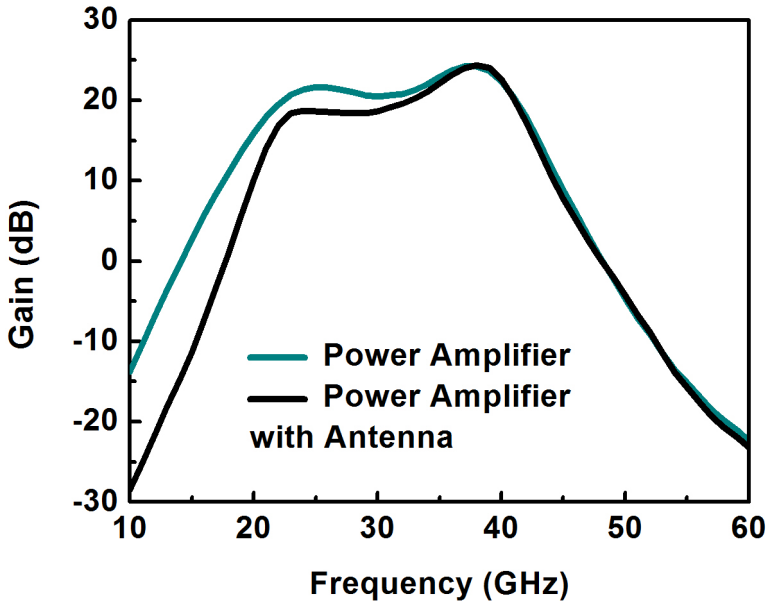


Figure 4.19: The overall gain of the wide band power amplifier.

The performance of the integrated system was investigate. Figure 4.19 shows the over all gain of the system. The gain of the power amplifier with the integrated antenna was about 20 dB, over a large bandwidth of 18.6 GHz from about 23 GHz to 41.6 GHz. Over 30 Gbps wireless data communications would feasible at this wide bandwidth.

4.4 Concluding Remarks on Integrated On-Chip Antennas

A thick dielectric interconnect technology is proposed to minimize the radiation loss of on-chip antennas. Several antenna topologies were pursued utilizing this technology. An on-chip triangular sleeve monopole was implemented which has a wide bandwidth, from 23 GHz to 63 GHz, with 3.5 dB gain and efficiency of 98%. The antenna was integrated with a foundry wideband power amplifier IC. Efficient radiation was observe over a wide bandwidth of 23 GHz to 41.6 GHz from the system, which proves to be useful for high speed data communication.

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Chapter 5

Conclusions

This work mainly focused on the reduction of interconnect losses in back end of line (BEOL). In practice, three major loss components are dominated, capacitive loss, inductive loss and radiation loss. The loss mechanisms were identified and integration technologies were proposed for the reduction. These integration technologies were experimentally demonstrated by connecting with CMOS circuitry. Detailed summary of each section is listed below.

- *Capacitive Loss Reduction Through Low-k Dielectrics:* Interlayer dielectric (ILD) with low dielectric constant (or k-value) is important for high speed operations with reduced inter-metal capacitance. In this work, we have demonstrated an interlayer dielectric based on silicon dioxide with vertically aligned cylindrical pores (VACP) that achieved an ultralow k-value of 1.96. The vertically grown CNTs as an imprinting template provides a straightforward way of making this highly porous ultralow-k dielectric with improved stability in electrical and mechanical properties. The structure has been shown to be useful to reduce dynamic power consumption and signal propagation delay in the integrated circuits.
- *Inductive Loss Reduction by Ultra-Thick Dielectric and Metal Technology:* Efficient magnetic components are required for analog and RF applications. An interconnect technology with ultra-thick dielectrics and metal were required to integrate large

on-chip inductance in μH range in MHz frequency. This integration is crucial for fully integrated power management ICs to reduce overall size and solution cost. This work demonstrated the ultra-thick dielectrics and metal technologies using photo-patternable SU8 dielectrics. The effectiveness of this technology was confirmed by implementing large value high performance inductors. The fully integrated 4.5×4.5 mm^2 inductor can render 4.3 μH inductance, with a density of 200 nH/mm^2, on a low resistivity substrate while achieving a peak quality factor of 26. To demonstrate the application of this interconnect technology in miniaturized on-chip wireless power supply was implemented. A 2.5×2.5 mm^2 wireless power–receiving system was designed. It can wirelessly receive 27 mW from a 250 mW 27 MHz transmitting signal at a distance of 5.3 mm, and 1.1 mW at a distance of 21.3 mm. It is the best reported performance compared with published data.

- *Mitigation of Radiation Loss by Thick Dielectric Processing:* On-chip integrated antenna on silicon is promising as radiating wavelength approaches in millimeter wave band. A thick dielectric interconnect technology is proposed to minimize the radiation loss of on-chip antennas. Several antenna topologies were pursued utilizing this technology. An on-chip triangular sleeve monopole was implemented which has a wide bandwidth, from 23 GHz to 63 GHz, with 3.5 dB gain and efficiency of 98%. The antenna was integrated with a foundry fabricated wideband power amplifier IC. Efficient radiation was observe over a wide bandwidth of 23 GHz to 41.6 GHz from the system, which proves to be useful for high speed wireless data communication.

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