Electromagnetic Interference-Related Common-Mode Noise Analysis and Mitigation Technique for High-Speed PAM-4 Transmitter

by

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To my father...

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Abstract

Entities such as telecommunications enterprises, online retailers, and social media generate huge amounts of data, and most of these entities use cloud computing to process and store the data in data centers having communication speeds of 200 Gbps or higher. Although advanced communication equipment for 200 GbE can produce a greater data rate with smaller size and lower cost and power, the size reduction can cause reliability issues in data centers, as electromagnetic interference (EMI) can become a significant problem in these highly dense facilities.

Optical transceivers supporting four-level pulse amplitude modulation (PAM-4) signaling are widely used in high-speed communication links in data centers, and while it is true that the optical communication channel is immune to EM radiation, the transmitter in the transceiver package consists of electronic components which can generate and radiate EMI. Additionally, to compensate for the bandwidth (BW) limitation of the laser and channel, different types of equalization are utilized. It is intuitive to believe that a fractional-spaced asymmetric feed forward equalizer (FSA-FFE) circuit could further increase the EM emission from the transmitters. Also, advanced

technology nodes like 14 nm FinFETs are extensively used for implementation of high-speed communication systems, and the technology scaling can significantly affect the EM emission from the transmitter. However, a systematic study of how asymmetric equalization and technology scaling affect the EM emission is still lacking. To fill this gap, this thesis analyzes the effect of technology scaling and the sources of EMI-related CM noise in PAM-4 transmitters, and then proposes an on-chip active technique to mitigate EMI-related CM noise.

In the first part of the thesis, the effects of the PAM-4 current-mode logic (CML) driver, different FFE configurations and technology scaling on EMI-related CM noise are analyzed mathematically, and then further evaluated by behavioral and transistor-level simulations in 40 nm CMOS and 14 nm FinFET technologies. It is observed that the CM current in differential circuits generates CM noise which radiates in the environment and causes EMI with electronic devices in proximity. This noise is generated due to the rising and falling time mismatch created by the driver circuit and asymmetric equalization. It is demonstrated that the intrinsic impedance variations of the CML driver circuit, amplitude of the equalization current, and offset in the FSA-FFE circuit are the main sources of EMI-related CM noise in transmitters. Additionally, the technology scaling is used to achieve higher data rates, which results in increase of the CM noise in advanced technology nodes.

In the second part of the thesis, we present a novel on-chip active circuit technique to mitigate EMI-related CM noise in high-speed PAM-4 transmitters. An automatic CM noise cancellation (CMNC) system architecture in 40 nm technology is designed for a 56 Gbps PAM-4 optical transmitter. This solution provides the benefits of small size and low cost by eliminating the need for discrete components to suppress EMI. It is demonstrated that the CM noise cancellation system efficiently mitigates EMI by suppressing the CM noise up to 90% while consuming 5 mW, with a core area of 17 $\mu m \times 9 \mu m$.

Chapter 1

Introduction

1.1 Background

The continuous evolution of communication technology from 1G to 5G has been driven by the increasing demand for higher data rates due to technological advancements, which are revolutionizing society by introducing applications like autonomous automobiles, intelligent internet of things (IoT) and augmented/virtual reality, as depicted in Figure 1.1 [1]. A study on digital data

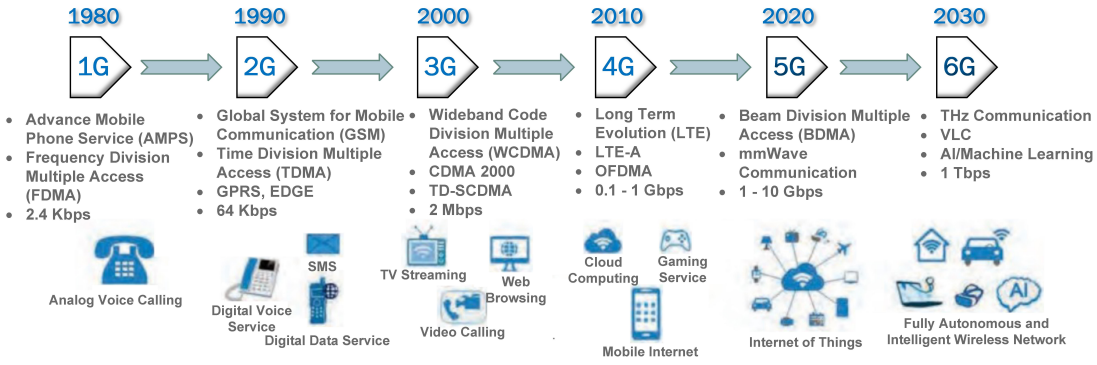

Figure 1.1: Evolution of wireless communication.

growth carried out by the International Data Corporation in 2012 found that 4 trillion gigabytes of data will be generated in 2020 [2]. Entities such as telecommunication enterprises, educational institutes, security surveillance

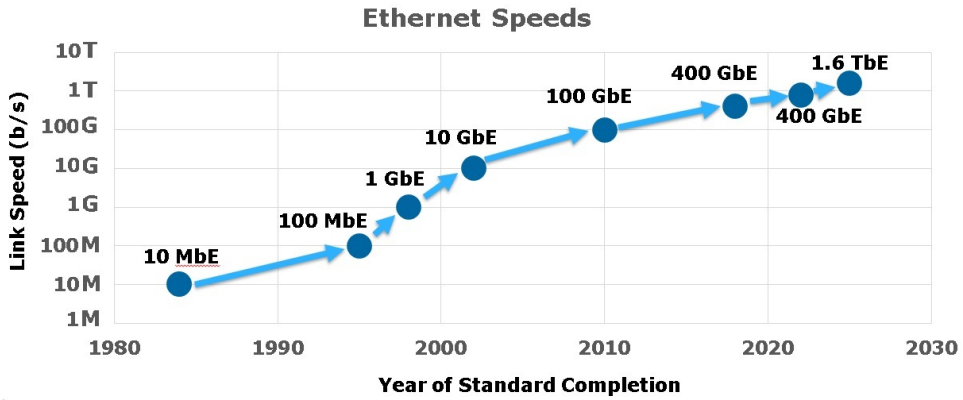

Figure 1.2: Evolution of Ethernet.

companies, online retailers, and social media generate huge amounts of data, and most of these enterprises use cloud computing to process and store the data in data farms known as data centers. These consist of many parallel rows of racks holding servers networked together to increase processing power and connected with a communication network using Ethernet to share data with remote users online.

Ethernet standards are advancing from 100 GbE to 200 GbE and beyond to meet high-speed demands, as presented in Figure 1.2, which clearly depicts the extensive growth in the speed of transmission in recent years. The most commonly used form factors of Ethernet ports are shown in Figure 1.3. It can

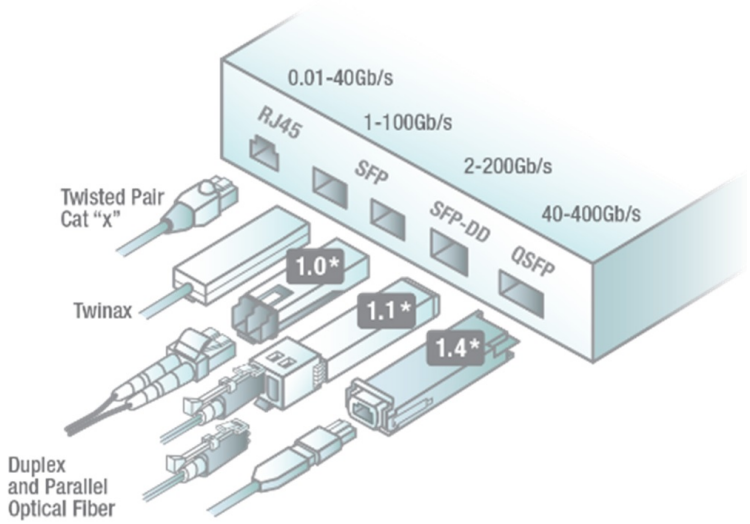

Figure 1.3: Ethernet port form factor [3].

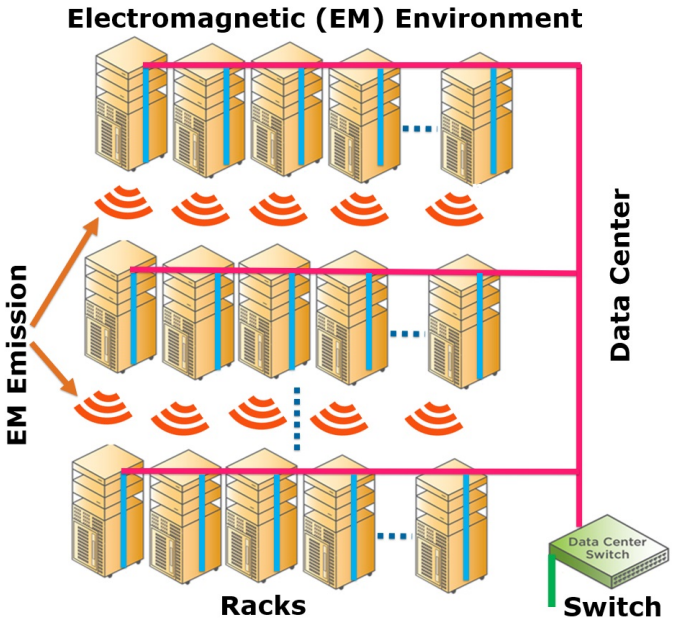

Figure 1.4: EMI in data center.

be seen that the sizes of the ports do not increase as much as the speed of communication. The growth in data pushes data centers to upgrade from the older 40 GbE to 200 GbE and higher. Although, advanced communication equipment for 200 GbE can produce a greater data rate with smaller size and lower cost and power, the size reduction in data centers can cause reliability issues. The electromagnetic interference (EMI), a disturbance signal that can degrade the performance of electronic devices by electromagnetic induction, electrostatic coupling, or conduction, can become a significant problem in highly dense data centers, as depicted in Figure 1.4. Equipment like cell phones, TV and radio transmitters, and electronic navigation systems deliberately generate an RF signal, while devices like computers, printers, power supplies, and TV sets produce an unintentional RF signal, which can cause undesirable behavior of electronic equipment. EMI can also be generated by natural events like solar and cosmic radiation, nuclear decay, and thunderstorms.

The emission of radiation causes a failure to meet standards of the electromagnetic compatibility (EMC) prescribed by the Federal

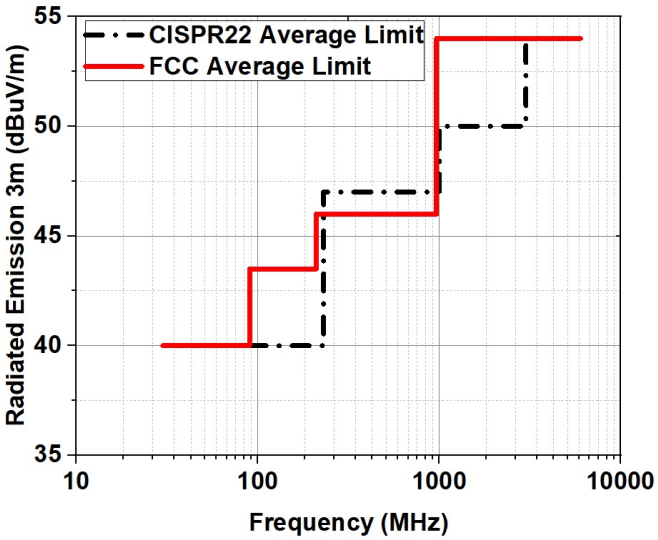

Figure 1.5: FCC and CISPR EMC limitations.

Communications Commission (FCC) and International Special Committee on Radio Interference (CISPR). The limitation of EMC is presented in Figure 1.5, which demonstrates that the radiation emission of high-speed equipment having 3 GHz or above frequency should not exceed the specification of 54 dBuV/m. Thus, it is quite challenging and costly to meet the EMC standards in the design of high-speed transmitters if it is not considered early in the design cycle.

Recently, analyses of the sources of EMI have been presented in [4–7], where it is reported that the source of EMI is common mode (CM) noise generated by the non-linear distortion of the differential signal, as presented in Figure 1.7. If rise time and fall of the differential signals are equal, then ideally CM noise transient signal is perfect DC and its Fourier transform in frequency spectrum has no tone at double the Nyquist frequency, as shown in Figure 1.6. However, if rise time and fall time are unequal, then the transient CM signal has non-zero value and its spectrum shows spectral tones of 71 dBuV at twice the Nyquist frequency, as presented in the Figure 1.7. This is known as non-linear distortion as it generates spectral tone in the CM noise spectrum at integer multiple of Nyquist frequencies.

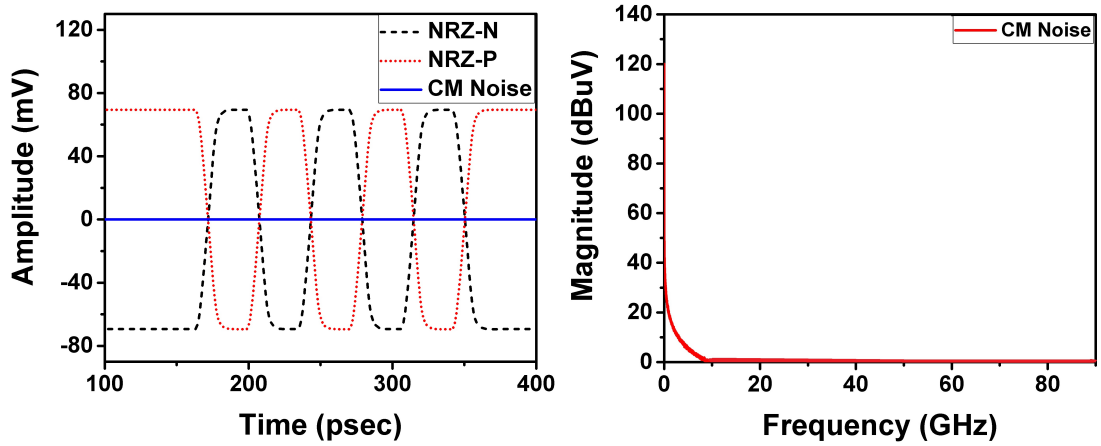

Figure 1.6: Ideal CM noise transient signal and its frequency spectrum without distortion.

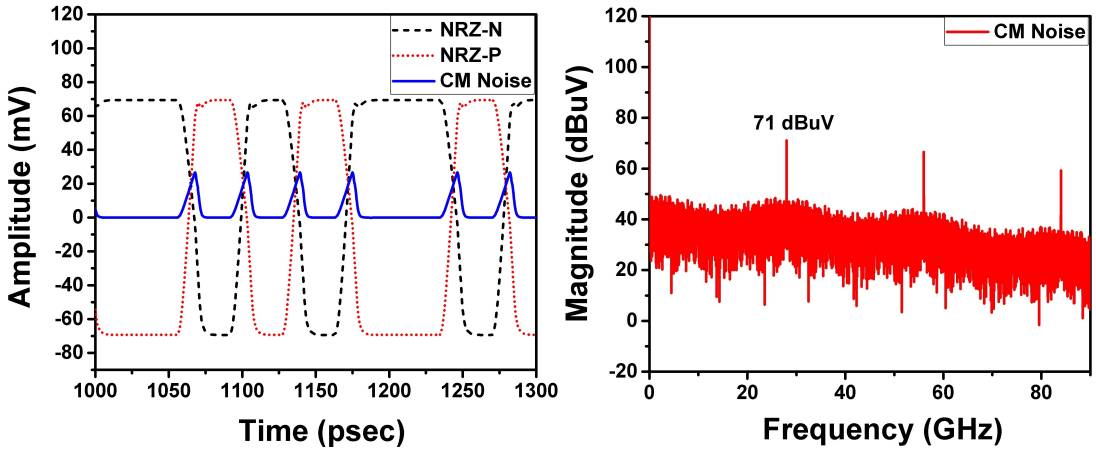

Figure 1.7: CM noise transient signal and its frequency spectrum with non-linear distortion.

The current-mode logic (CML) driver circuits are widely used in the transmitters. This circuit has an imbalance in the charging and discharging paths due to variation of the transistor's internal capacitance and resistance during switching [5], as depicted in Figure 1.8. The rising/falling edge is calculated using the following formula:

$$V_{out_{(rise/fall)}} = V_{initial} \pm I_D \times R_{total}(1 - e^{\frac{-1}{R_{total} \times C_{total}}}). \tag{1.1}$$

The differential transistor M1 goes from the ON to OFF state and M2 goes from the OFF to ON state during switching, which results in variation of transistor

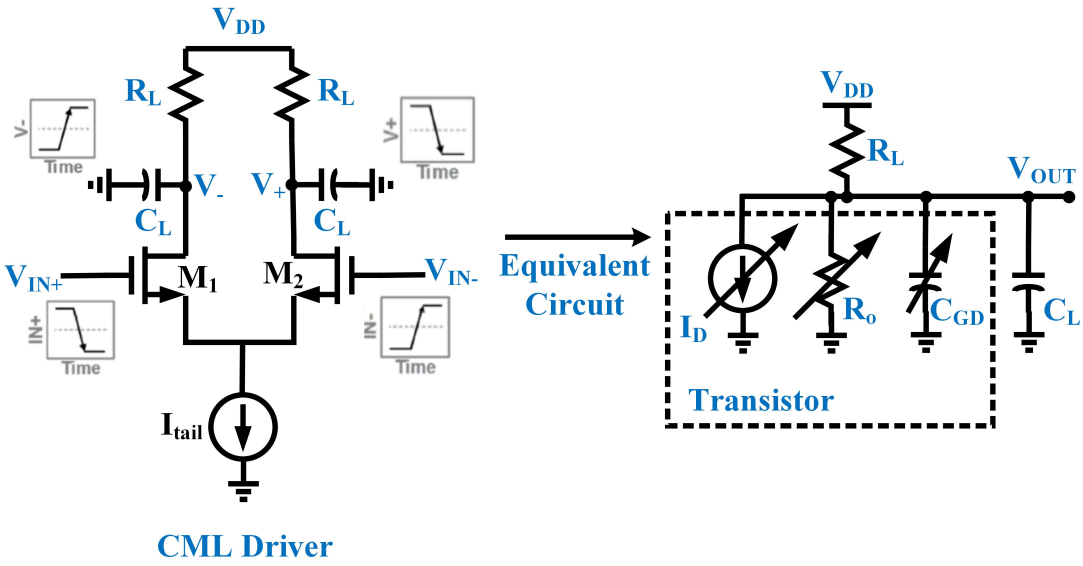

Figure 1.8: Charging and discharging path imbalance in CML driver.

parasitics (I_D, R_o *and* C_P). This imbalance creates a mismatch in the rise and fall time of the driver, and generates the CM signal, which radiates in the environment and causes an EMC problem in the transmitters.

1.2 Research Motivation

The extensive speed demands by the innovative applications, require high-speed and low-latency communication systems to be developed. Electrical systems are unable to meet these stringent requirements [8–13] due to their bandwidth (BW) limitation, and though many equalization methods [14, 15] have been developed to overcome this limitation, they cost area and power.

A suitable solution to meet the high speed demand is optical communication systems, which have the advantages of higher BW, lower cross-talk, shorter delay, lower power consumption, low transmission loss, and a smaller and lighter communication medium [16]. Such systems are used in a number of applications, like tele-/data communication, optical storage, printing, cable TV [17], avionic systems, industrial control systems, military

command, and control systems.

Non-return-to-zero (NRZ) is utilized in many communication systems. However, the dielectric and interface losses will increase at high data rates due to the rough surface between the conductor and PCB [18]. Pulse amplitude modulation-4 (PAM-4) can reduce these losses by using multiple parallel data paths with constant transmission speed. PAM-4 is used to double the throughput for the same baud rate while reducing the Nyquist frequency to half by encoding two bits of information into one voltage level, as shown in Figure 1.9. The PAM-4 data rate improvement is given by equation (1.2):

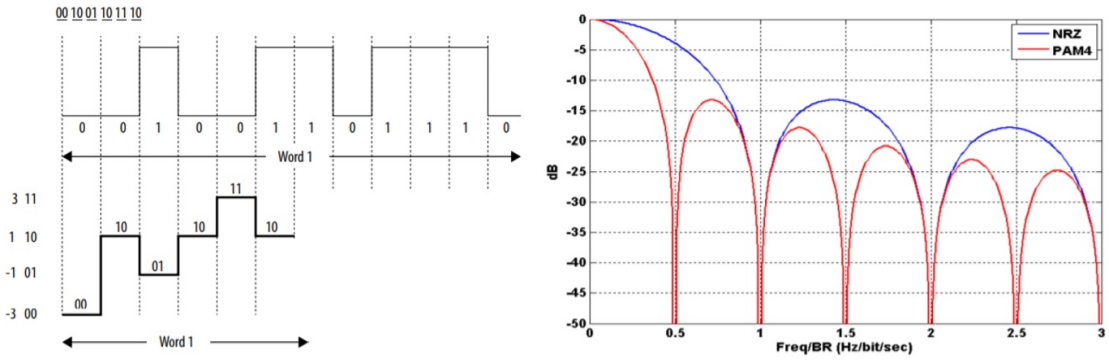

Figure 1.9: Advantages of PAM-4 signaling.

$$Data\_Rate_{PAM-4} = 2 \times Data\_Rate_{in} = 2 \times 28\ Gbps = 56\ Gbps. \tag{1.2}$$

While the PAM-4 signal delivers a higher data rate, due to multilevel amplitudes, the signal-to-noise ratio (SNR) decreases to 9.5 dB as compared to its NRZ counterpart, as calculated by equation (1.3) [19]:

$$SNR_{PAM-4_{Loss}} = -2 \times log\frac{1}{3} = -9.5\ dB. \tag{1.3}$$

This degradation in SNR will increase the bit-error-rate (BER) at the output.

Recently, optical communication standards have been widely adopting PAM-4 signaling for next-generation systems because of its higher spectral efficiency [20–24], and while it is true that the optical communication channel is

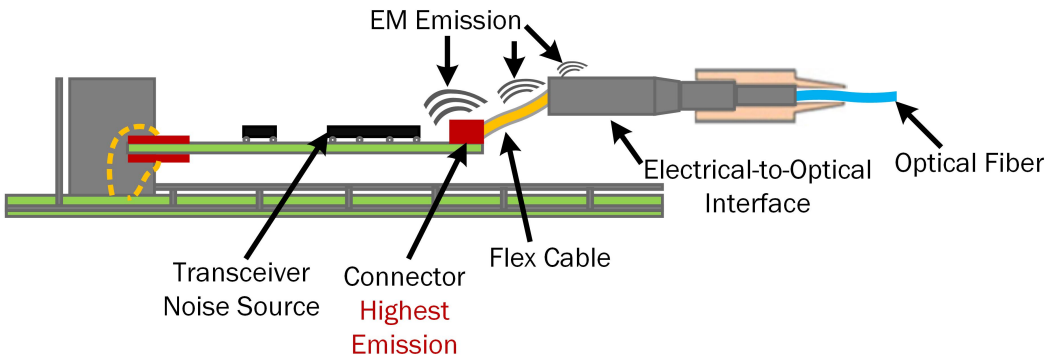

Figure 1.10: Optical transceiver module with three possible sources of EM emission: connector, flex cable and electrical-to-optical interface.

immune to EM emission, the transmitter in the optical transceiver package consists of electronic components which can generate and radiate EMI. It has been proved with measurement results in [25] that the EM radiation in the optical transceiver emits from the connectors, flex cable and electrical-to-optical interface (EOI), as depicted in Figure 1.10. The dimension of connector is 2.4 mm and the flex cable is 2.4 cm. To quantify the total radiation power (TRP) from these parts of the optical transceiver, a lossy material is used in [25] to suppress emission from each component and observe corresponding emission levels. The test setup used in [25] to study the dominant source of EM emission from the optical transceiver is shown in Figure 1.11, and the simulation and measurement results of three experiments in [25] are presented in Figure 1.12(a-c). It is proved by these results that the connector is the dominant source of EM emission above 15 GHz transmission.

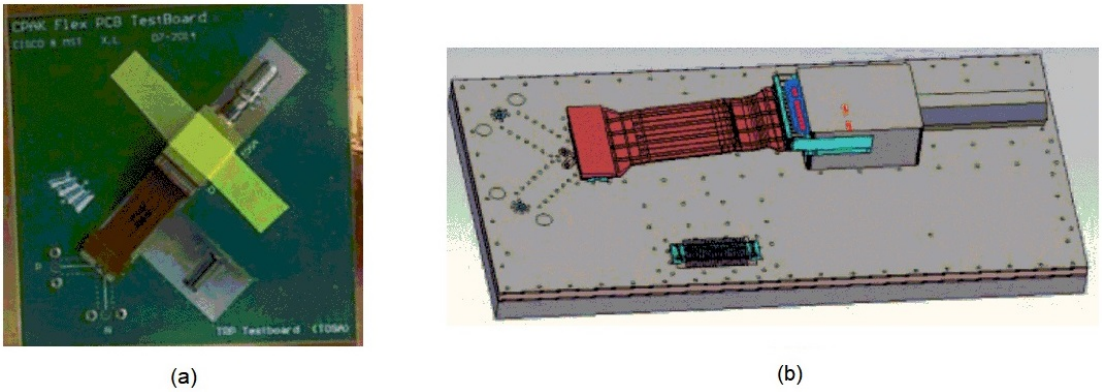

Figure 1.11: (a) Measurement test setup. (b) Simulation test model.

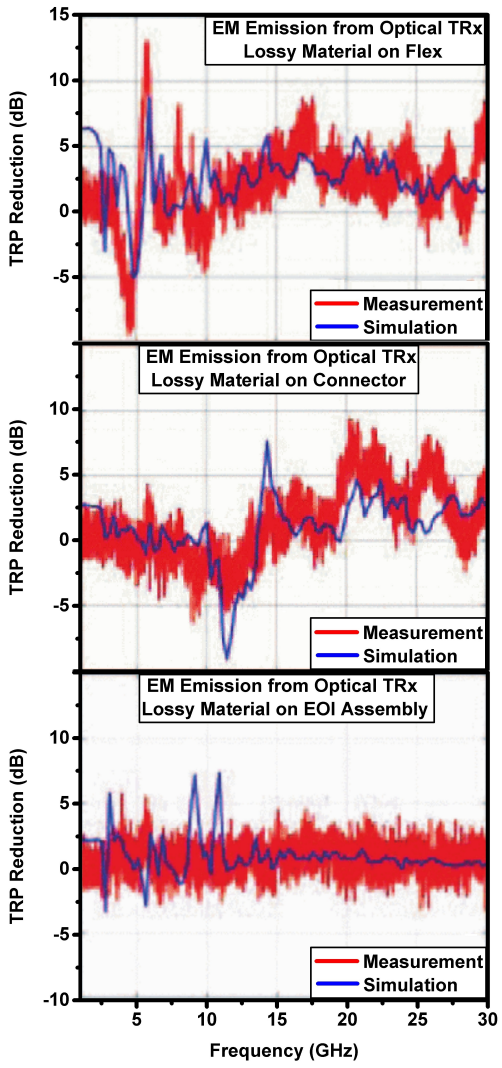

Figure 1.12: Measurement and simulation results of EM emission from optical transceiver module. (a) Reduction of TRP from optical transceiver after adding lossy material on flex cable. (b) On connector. (c) On EOI assembly [25].

The reason for higher EM emission from connector is due to the impedance of connector might change at higher frequencies, whereas the flex cable is well defined transmission line. Further to this, doubling the number of transceivers increases the EM emission with a square root relationship, i.e., $|E_{2n}| = 2^{1/2}|E_n|$, as demonstrated in [26].

This EM radiation can significantly affect the weak signal of the receiver, in the same transceiver package or nearby devices, which increases the BER and causes malfunction. Additionally, the BW limitation of the laser and

channel results in inter-symbol interference (ISI), which degrades the signal-to-noise ratio (SNR) at the receiver. To compensate for the non-linearity, different types of equalization are utilized [27–29]. Feed forward equalizers (FFE) are extensively used in high speed transmitters, which pre-distort the transmitter signal to compensate the non-linearity of laser and channel. It is intuitive to believe that a FFE would affect the rise and fall time of the transmitter output, which would further increases the EM emission from the transmitters. Thus, it is necessary to study how different FFE circuit configurations affect the CM noise, which is currently not presented in the literature.

Furthermore, advance technology node helps to design high speed circuits. These nodes provide transistor size scaling, and this sizing will directly affect the transistor internal parasitics. This will cause variation in the mismatch of the rise and fall time, and produce CM noise in the transmitters. The effect of technology scaling on the CM noise has also not been presented in the literature.

To mitigate the EMC issue, shielding is the most commonly used off-chip technique [30–32] used in the industry. In it, the number of gaskets is increased or the vent hole is made smaller to improve the shielding [33]. But adding gaskets is generally unsuitable in small areas, and making the vent hole smaller degrades thermal performance. An absorber is also frequently used around the trace or chip to reduce EMI [34]. However, it is costly and time-consuming to find the critical point for the absorber. This method can affect the thermal performance as well. Another approach to reduce EMI is to use filters [35–38], but these are not suitable for small-size architectures, and all of the above solutions are costly and area inefficient as compared to on-chip solutions.

An on-chip method to suppress EMI-related CM noise is reported in [39]. It reduces the CM noise by tuning the input signal swing and CM level of the driver circuit. Another on-chip solution is demonstrated in [40] to suppress the CM noise by tuning the input impedance, rise/fall time, time delay and amplitude

at the input of the driver circuit. It also requires a controller to tune the CM noise cancellation system, which increases the area and power of the system. A further, on-chip CM noise suppression technique from self-calibration of a source-series terminated (SST) driver is presented in [41, 42]. Although, all of the above solutions are background calibration techniques for driver circuit CM noise and support NRZ wireline transmitters up to 20 Gbps speed, they do not account for the effect of the FFE circuit on CM noise, and can not support PAM-4 signaling and optical transmitters.

1.3 Thesis Contributions

This thesis includes the following two contributions.

1.3.1 Contribution 1: Sources of EMI-related CM Noise in PAM-4 Transmitters

In this thesis, analyses of sources of EMI-related CM noise in a PAM-4 optical transmitters are presented, and the equation of CM noise in PAM-4 transmitter is derived. The sources analyzed in this thesis are the common mode logic (CML) driver and FFE circuit.

The effect of technology scaling on EMI-related CM noise is presented. To analyze the effect of technology scaling, the CM noise generated by PAM-4 optical transmitters designed in 40 nm CMOS and 14 nm FinFET technology are studied.

1.3.2 Contribution 2: Automatic CM Noise Cancellation System

An active on-chip circuit methodology is proposed to automatically cancel the EMI-related CM noise generated from sources such as the pre-driver stage, output driver stage and equalization circuit in high-speed transmitters supporting PAM-4 signaling. We design a 56 Gbps PAM-4 optical transmitter, which includes a FFE and an automatic CM noise cancellation (CMNC) system architecture in 40 nm CMOS technology.

1.4 Thesis Overview

This thesis is organized as follows. In Chapter II, the architecture of a PAM-4 optical transmitter is presented. The sources of EMI-related CM noise in the transmitter are analyzed in Chapter III. In Chapter IV, the effect of technology scaling on EMI-related CM noise is discussed. The design of an automatic CMNC system is demonstrated in Chapter V. Finally, a brief conclusion and future work are presented in Chapter VI.

1.5 Publications

1.5.1 Journal and Conference Papers

- R. Azmat, L. Wang, K. Q. Maqbool, C. Wang, and C. P. Yue, "Sensing and cancellation circuits for mitigating EMI-related common mode noise in high-speed PAM-4 transmitter," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 68, no. 11, pp. 4545–4555, 2021.

- R. Azmat and C. P. Yue, "Effect of feed forward equalization on EMI-related common mode noise in 56-Gbps PAM-4 optical transmitter," in *2021 Asia-Pacific International Symposium on Electromagnetic Compatibility (APEMC)*, pp. 1–4, IEEE, 2021.

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Chapter 2

PAM-4 Optical Transmitter

In this chapter, we give a brief introduction of modules of the optical transmitter designed in this thesis.

The 56 Gbps PAM-4 optical transmitter shown in Figure 2.1 is designed using the Cadence Virtuoso analog design environment to analyze the generation of CM noise and mitigate EMI. It consists of the following main modules.

- Pseudo-random binary sequence (PRBS) generator
- PAM-4 CML driver
- PAM-4 FFE
- Automatic CMNC system

The signal from the PRBS generator is fed into the CML driver, FFE module, and automatic CMNC system. A 50 ohm termination is connected at the output with a 50 fF load capacitance. Beads are used to block the high-frequency signals from the supply source.

A non-linear laser model is connected across output terminals V_{outP} and V_{outN} of the transmitter by a coupling capacitor, and a CML driver circuit drives

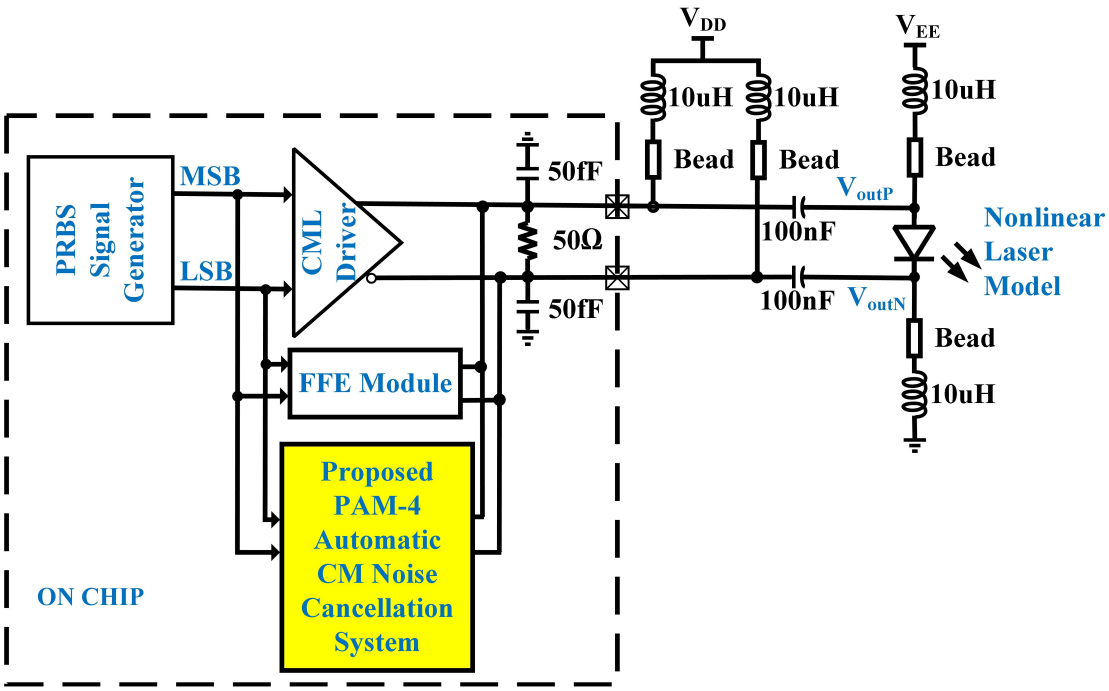

Figure 2.1: Schematic of 56 Gbps PAM-4 optical transmitter with FFE and automatic CM noise cancellation system.

this laser. The output signal of the CML driver, FFE module, and CMNC circuit are combined at the OUT_N and OUT_P terminals. The automatic CMNC system senses and suppresses the cumulative CM noise generated by the CML driver and the FFE circuit at these nodes. The effect of the bond-wire is not included in the test-bench, as it has already been demonstrated in [1] that a mismatched interconnection channel does not contribute considerably to CM noise.

In the following sections, we will discuss each block of the optical transmitter in more detail.

2.1 PAM-4 PRBS Generator

The input binary data signal to test a high-speed communication system should be a reasonable approximation of real signals, which the system has to transmit after deployment. This test signal must be standardized to make the measurement reproducible. A completely random signal may not be an option.

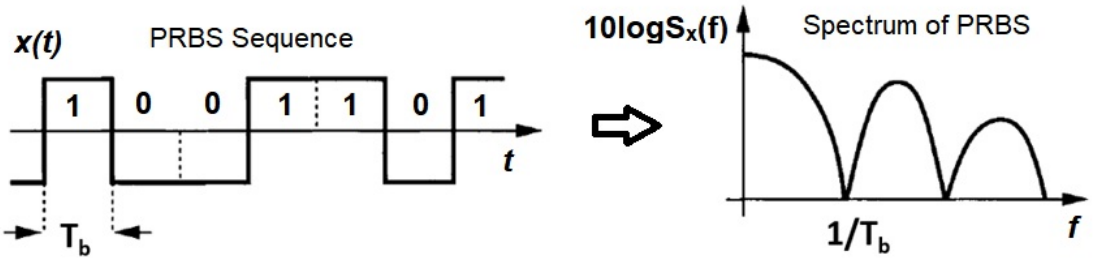

Figure 2.2: PRBS pattern and its frequency spectrum exhibiting null at 1/Tb.

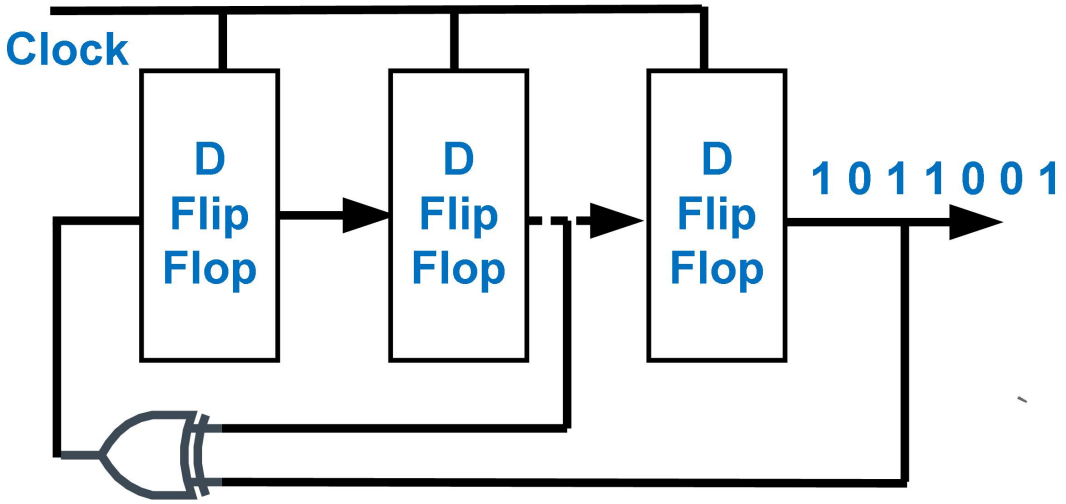

Figure 2.3: PRBS signal generator.

Thus, the PRBS is a good choice for repeatable measurement. The PRBS is similar to random signals as it has very long periodicity, and its spectrum exhibits no power at frequencies equal to $1/T_b$, $2/T_b$, $3/T_b$, . . ., n/T_b, as depicted in Figure 2.2. These signals can be produced by shift registers, as shown in Figure 2.3. Different output patterns are generated by feeding back some output of the shift registers to the input using an XOR gate. The maximum period is $2^L - 1$, where L is the number of registers. In this thesis, binary data to test the optical transmitter are produced by a PRBS generator, which generates the LSB and MSB of bit period (T_b).

2.2 PAM-4 CML Driver

Several types of driver architectures are used in communication systems. These include the CML, voltage-mode logic (VML), source-series termination logic (SSTL), CMOS driver (inverter based) and low-voltage differential signaling (LVDS). The CML driver circuit is widely used in optical communication systems due to its high speed, low noise and adjustable output swing and slew rate.

A CML driver circuit was presented in [2] as a new architecture for high-speed applications. The CML driver works on the principle of switching the current of a constant tail current source through a differential network of NMOS transistors, and produces a reduced-swing voltage drop across the differential load as the output voltage. Therefore, this architecture reduces the switching noise by providing reduced voltage swing and differential operation. It also provides the benefit of high speed and constant power dissipation independent of operating frequency. A CML driver is implemented in this thesis because of these advantageous characteristics.

A PAM-4 MOS CML driver is shown in Figure 2.4. It consists of a common source differential pair, an NMOS tail current source and a load resistor $2R_L$. The value of resistor $2R_L$ also provides source termination for the transmission line to improve the signal integrity. The transistors M_1 and M_2 are biased in the saturation region, and input voltages V_{IN+} and V_{IN-} are applied to alternately switch on or off both transistors M_1 and M_2 to steer the I_{tail} through M_1/M_2. The amount of the current driving the load is controlled by a voltage-controlled tail current source (I_{tail}).

This configuration of an only NMOS-based CML driver, has high bandwidth (BW), high modulation efficiency and relatively linear operation as compared to open drain and push-pull typologies. It has supply and ground bouncing resistance and only the output bond wire will affect the BW.

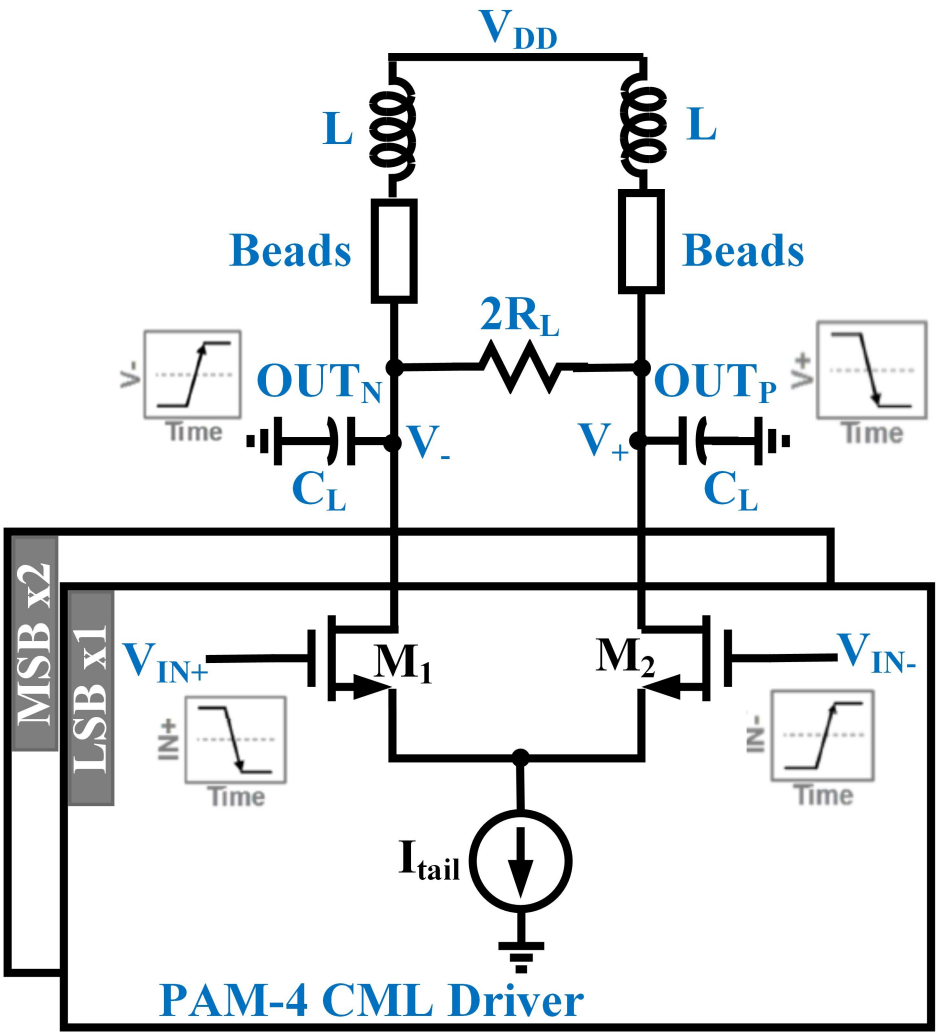

Figure 2.4: Schematic of PAM-4 CML driver.

However, off-chip biasing for the driver circuit and a separate supply for the laser are needed in this topology.

2.3 Laser Diode

Laser diodes are broadly classified into two categories, as shown in Figure 2.5. The first type have in-plane cavities and are called edge emitting lasers (EELs), and the second type have vertical cavities and are called vertical cavity surface emitting lasers (VCSELs). EELs emit light from the edge of the device because

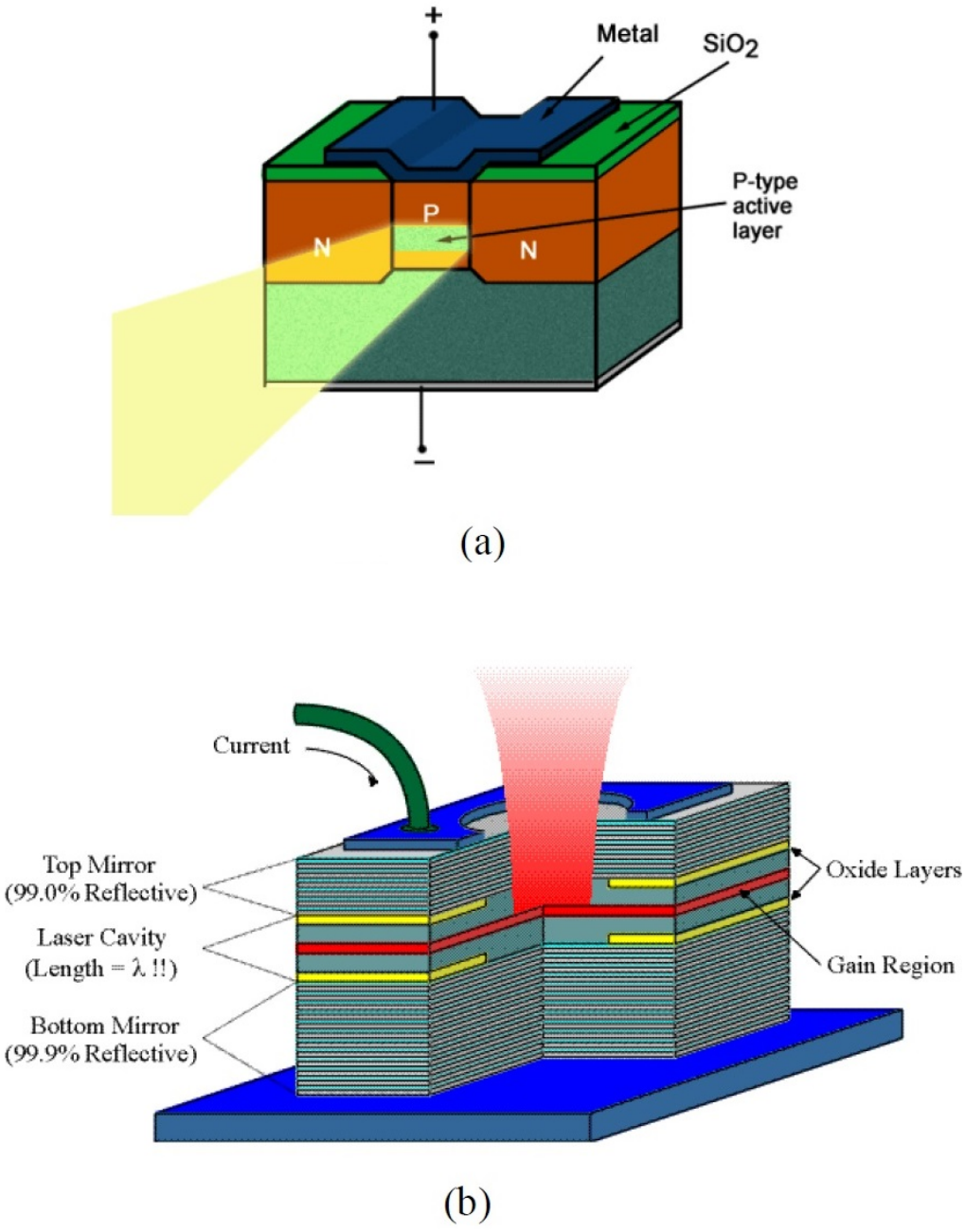

Figure 2.5: Structure of (a) EELs (b) VCSELs [3].

the optical cavity is in the lateral axis and feedback can be attained by a cleaved-facet mirror, whereas VCSELs emit light from the top surface of the device because the optical cavity is in the vertical axis and feedback can be realized using a multi-layer reflective stack grown below or above the active region.

Different types of lasers are used in different applications based on their

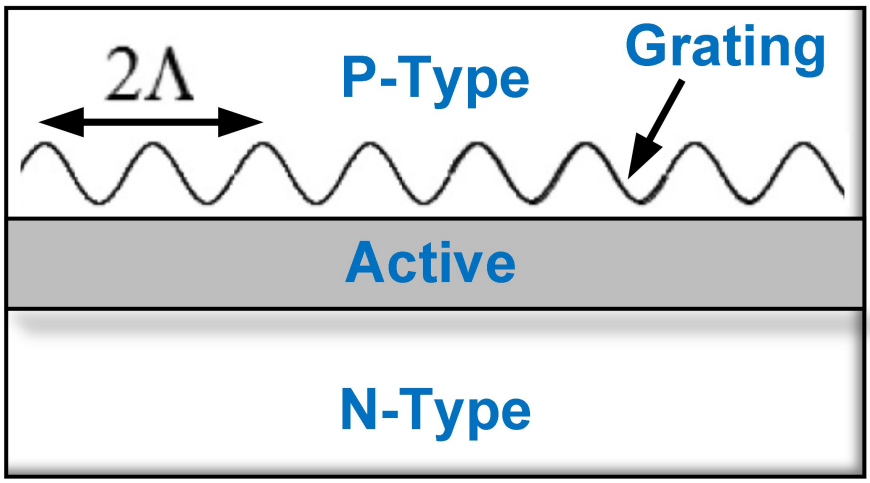

Figure 2.6: Structure of DFB laser.

emission frequency range and tunability. The types include Fabry-Perot (FP) lasers, distributed Bragg reflector (DBR) lasers, distributed feedback (DFB) lasers, and external cavity lasers.

DFB lasers are used in this work. These lasers are extensively used in optical communication systems because of their excellent monochromaticity. A DFB laser uses a grating mirror in which gain is included in the gratings, as depicted in Figure 2.6. A periodic grating is utilized for frequency selection in DFB lasers, which results in constructive interference between forward and counter propagating optical waves at a specific wavelength. The condition for resonance in a DFB laser is given by the following equation:

$$\lambda_g = 2 \times n \times \Lambda, \tag{2.1}$$

where λ_g is the Bragg wavelength, Λ is the grating period, and n is the effective refractive index of the optical waveguide.

The transmitter BW is determined by the capacitance of the CML driver, laser bias-dependent impedance and the rate equation-dependent process of the electrical-to-optical signal conversion. A Verilog-A model is used for the simulation of the non-linear behavior of the laser. The values of resistance and capacitance in the verilog-A model are changed by the bias current and

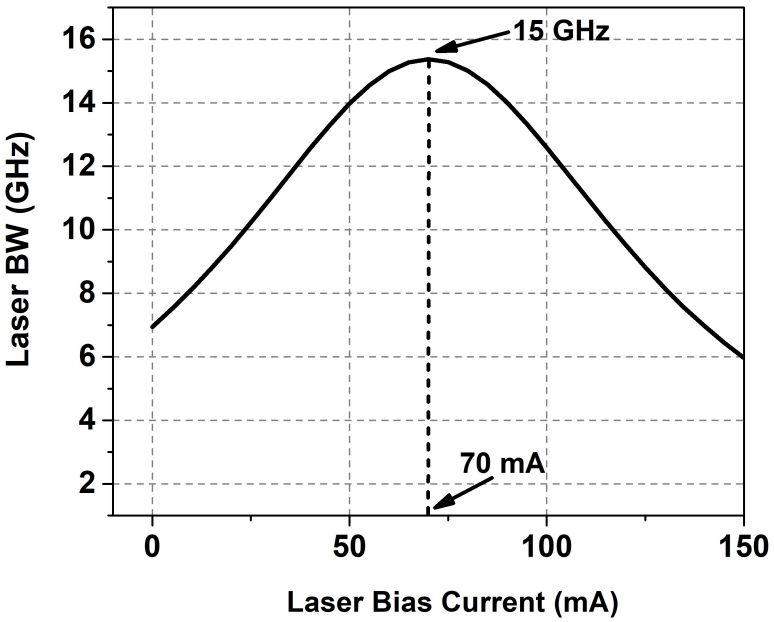

Figure 2.7: Schematic of PAM-4 CML driver.

temperature. The injection energy comes from the injection current of the diode active region's parasitic resistance, which is measured by the electrical-to-optical verilog-A module and fed to the rate equation. The BW of the laser is proportional to the bias current [4]. To achieve higher BW, the laser can be biased at a greater current. The maximum BW of the laser model is 15.3 GHz at 70 mA bias current, as depicted in Figure 2.7. However, a high value of the bias current can reduce the laser lifetime, extinction ratio (ER) and optical modulation amplitude (OMA) [5]. Therefore, the laser is biased at 60 mA. The non-linearity of the laser creates residual ISI in the output signal.

2.4 PAM-4 Feed Forward Equalizer (FFE)

A FFE is utilized to reduce the ISI produced due to the transient non-linearity and BW limitation of the laser or channel. The output stage of the equalization circuit generates pulses and pre-distorts the data signal at the output of the CML driver by adding the pulse into it. This pre-distortion reduces the ISI and makes the eye opening large. As discussed in the previous Section 2.3, the

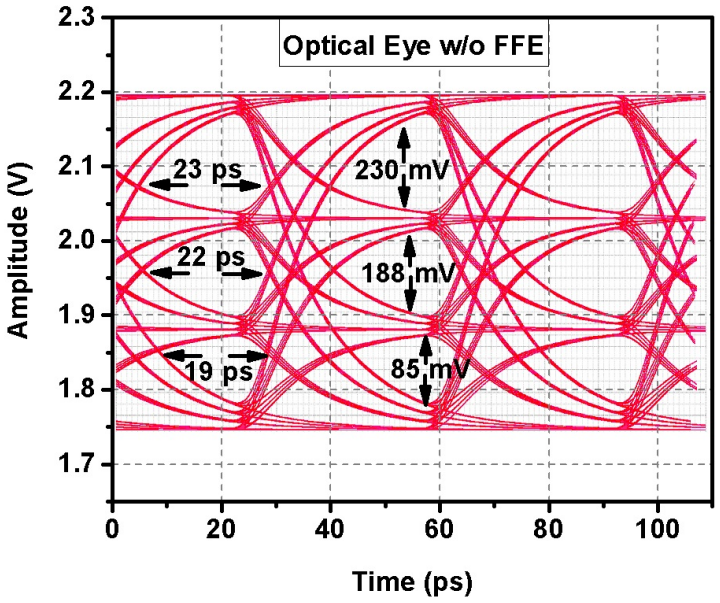

Figure 2.8: PAM-4 optical eye without equalization

BW of the laser depends on the bias current, and in PAM-4 communication the amplitude changes significantly during each transition, as depicted in Figure 2.8. This changes the bias current of the laser, which results in wide variations in the effective laser BW during PAM-4 transitions. The current varies from 45 mA to 75 mA for "00" to "11" transitions, respectively. The total variation of the current is 20 mA, which results in BW variation of 13.3 GHz to 15.28 GHz,

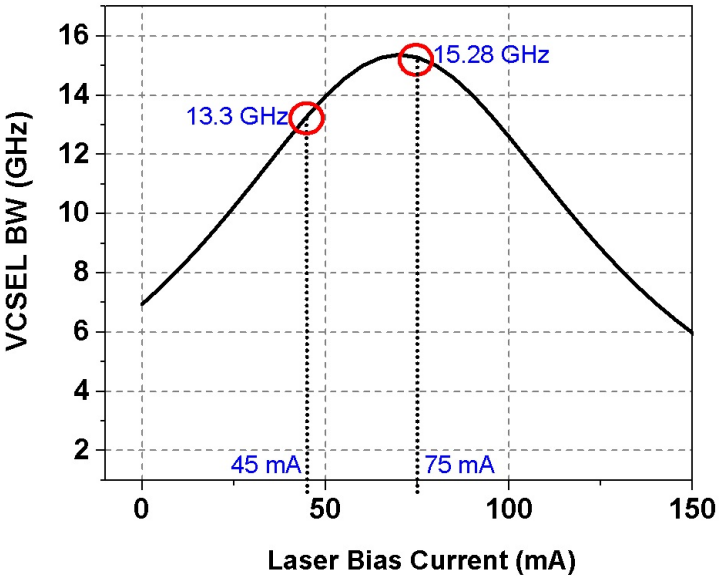

Figure 2.9: Laser BW variations with bias current.

as presented in Figure 2.9. This variation results in a non-linear optical eye opening, as shown in Figure 2.8. The bottom eye amplitude is 85 mV, mid eye is 188 mV, and top eye is 230 mV. The bottom eye is affected most because of the low current amplitude, which results in a small BW. This causes a complex ISI problem in transmission which cannot be compensated for easily with linear equalization.

Several non-linear equalization architectures have been presented in the literature [6] to solve the ISI problem. A $\frac{1}{2}$-UI FFE circuit is utilized in many applications, as reported in [7–9], to get a higher BW as compared to a 1-UI FFE circuit. This improves the timing margins and also reduces the residual ISI in high-speed PAM-4 communications. Gitlin et al. [10] demonstrated that $\frac{1}{2}$-UI equalization not only reduces the ISI but directly improves performance. The frequency domain range of FFE is increased by reducing the tab delay, which improves the equalization of high-frequency components at the cost of less total ISI span compensation[8].

The behavioral implementation of a fractional spaced asymmetric FFE (FSA-FFE) supporting PAM-4 signaling is depicted in Figure 2.10. It consists

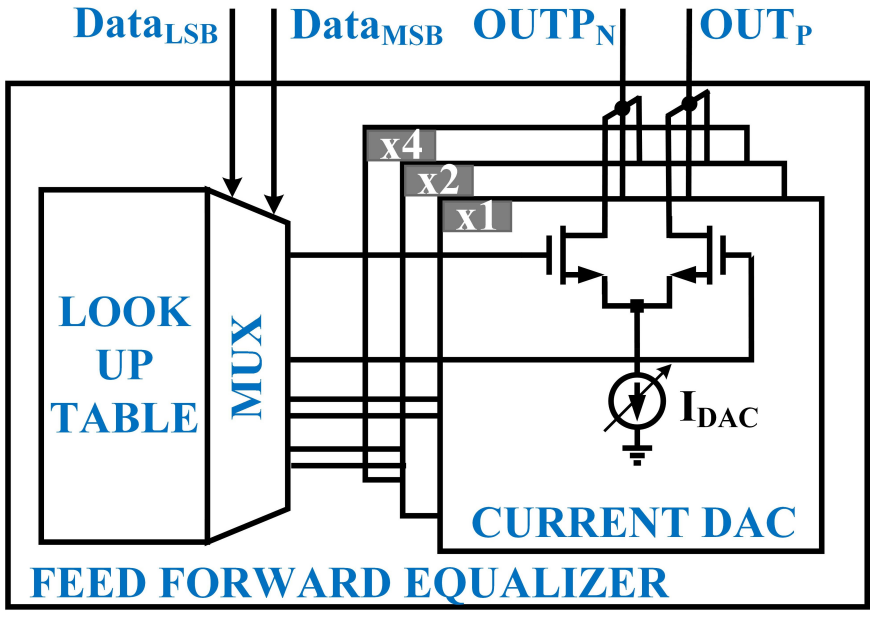

Figure 2.10: Schematic of the PAM-4 FFE circuit.

of a look-up table (LUT) which contains the equalization code to compensate for the ISI caused by the laser. The input data bits, $Data_{LSB}$ and $Data_{MSB}$, are used to switch the multiplexer (MUX) and select LUT entries, while the output of the MUX is utilized to control the CML digital-to-analog converter (DAC). This DAC steers the current from the output to produce an OUT_N and OUT_P equalization signal. The strength of the equalization current is controlled by the tail current sources (I_{DAC}) in the CML DAC.

2.5 Automatic CMNC System

The CM noise generated in the transmitter is cancelled by the proposed automatic CMNC system. It consist of three modules: a CM noise sensing circuit, automatic tuning logic and CMNC circuit, as shown in Figure 2.11. The CM noise sensing circuit measures the total CM noise at the output of the transmitter and generates a tuning decision signal for the automatic tuning module. The input of the sensing circuit is a differential PAM-4 signal from the output of the transmitter, as presented in Figure 2.11, and the CM noise is extracted from this PAM-4 output signal. The second module, the automatic

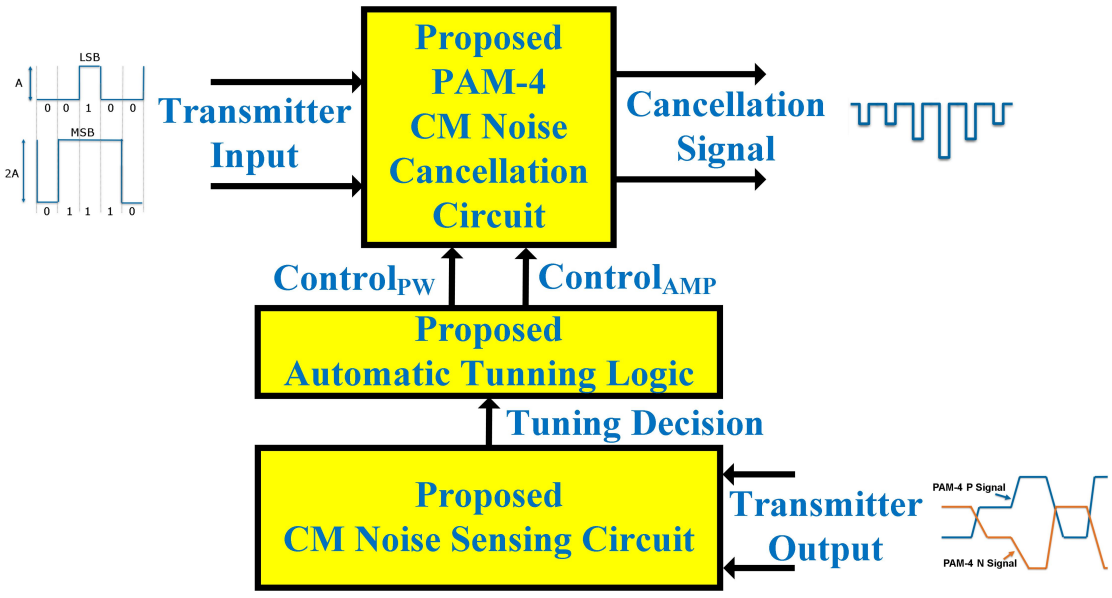

Figure 2.11: Automatic CMNC system.

tuning logic, generates the amplitude and pulse width control signal for the CM noise cancellation module. The cancellation circuit generates an opposite CM noise signal with a specific pulse amplitude and width to cancel the CM noise at the output of the transmitter. The input of the CM noise cancellation circuit is the LSB and MSB data signal generated by the PRBS generator, and the output is the CM noise cancellation signal, as depicted in Figure 2.11. The tuning circuit stops the tuning as soon as the CM noise at the output reaches its preset threshold value. The tuning is performed only once on the startup of the transmitter module. The design of each sub-module of the automatic CMNC system is discussed in more detail in Chapter 5.

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Chapter 3

Sources of EMI-related CM Noise in PAM-4 Transmitters

In this chapter, we present a detailed analysis of two potential sources of EMI-related CM noise in transmitters: the CML driver circuit and the FFE circuit.

3.1 Analysis of PAM-4 CML Driver Circuit

CML drivers are extensively utilized in high-speed optical communication systems [1] due to their better signal integrity as compared to other driver topologies like source-series terminated (SST) and push-pull driver circuits. The high performance of a CML driver is because of its ability to deliver the required current to the laser diode. However, it consumes higher power [2]. A PAM-4 signal is generated by a parallel-connected two-stage CML driver circuit, which combines the LSB and MSB signal, as presented in Figure 3.1, where V_{IN+} and V_{IN-} are the differential input data signal, OUT_P and OUT_N are the differential output signal, and R_L and C_L are the load capacitance and resistance at the output of the driver circuit. Beads are used to block the high-frequency signals from the supply source. The sizes of the transistors in

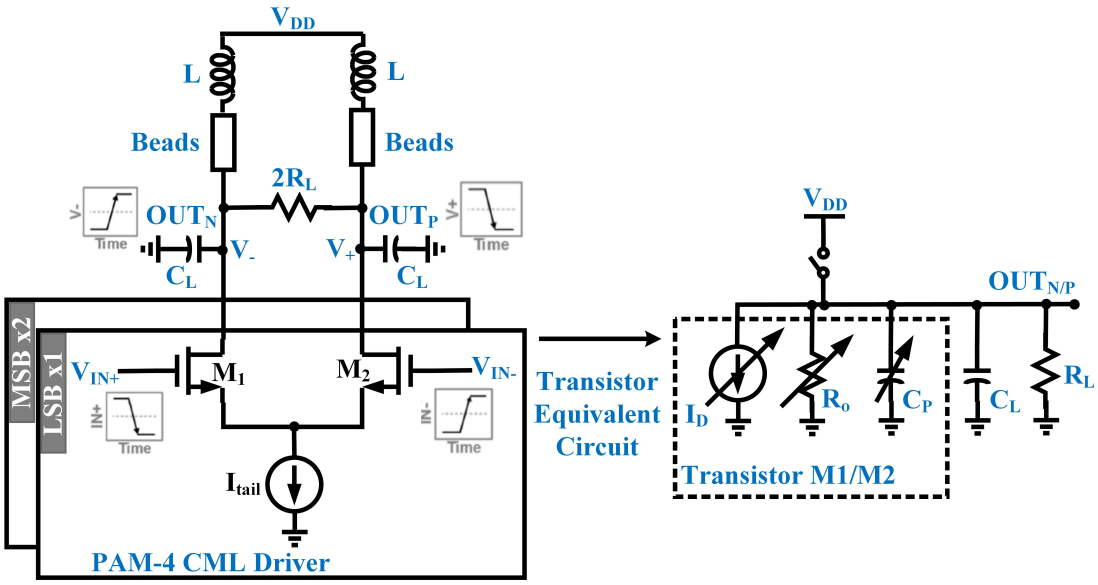

Figure 3.1: Schematic of PAM-4 CML driver and transistor equivalent circuit, presenting operating region-dependent internal capacitance, resistance and drain current.

the MSB CML stage are two times higher than those in the LSB stage.

The equivalent circuit of a transistor in the CML driver is shown in Figure 3.1, where I_D, R_O and C_P are the transistor's drain current, internal output resistance and capacitance, respectively. These circuit model parameters change with the operating region of the transistors. Derived by analyzing the equivalent circuit of the transistor, the equations for the rising ($V_{OUTrise}$) and falling ($V_{OUTfall}$) edge at the output terminal are given by

$$V_{OUTrise} = V_{initial} + I_D R_{total}(1 - e^{-\frac{1}{R_{total}C_{total}}t}), \tag{3.1}$$

$$V_{OUTfall} = V_{initial} - I_D R_{total}(1 - e^{-\frac{1}{R_{total}C_{total}}t}), \tag{3.2}$$

where I_D, R_{total}, and C_{total} are the drain current, total output resistance, and capacitance respectively, and $V_{initial}$ is the initial voltage at the output capacitor. The input differential signal switches both transistors in opposite directions. M1 is switched from the ON to OFF state, which creates a rising edge at the output

(OUT_N), while M2 is switched from the OFF to ON state, which creates a falling edge at the output (OUT_P). The values of R_{total} and C_{total} in the rising and falling edge at the output are different because of the different operating regions of the transistors. This creates imbalance in the rising and falling edge, as given by equations (3.1) and (3.2), which generates CM noise at the output of the transmitter.

A mathematical analysis of the dependency of CM noise on the rise and fall mismatch is presented in [3] for an NRZ wireline transmitter. The quantitative description of the CM noise signal generated due to rise and fall mismatch of the P-/-N path differential signal is presented in Figure 3.2. T_d is the bit period, t_{rise} and t_{fall} are the rising and falling times of the data signal, and T_{tr} is the total

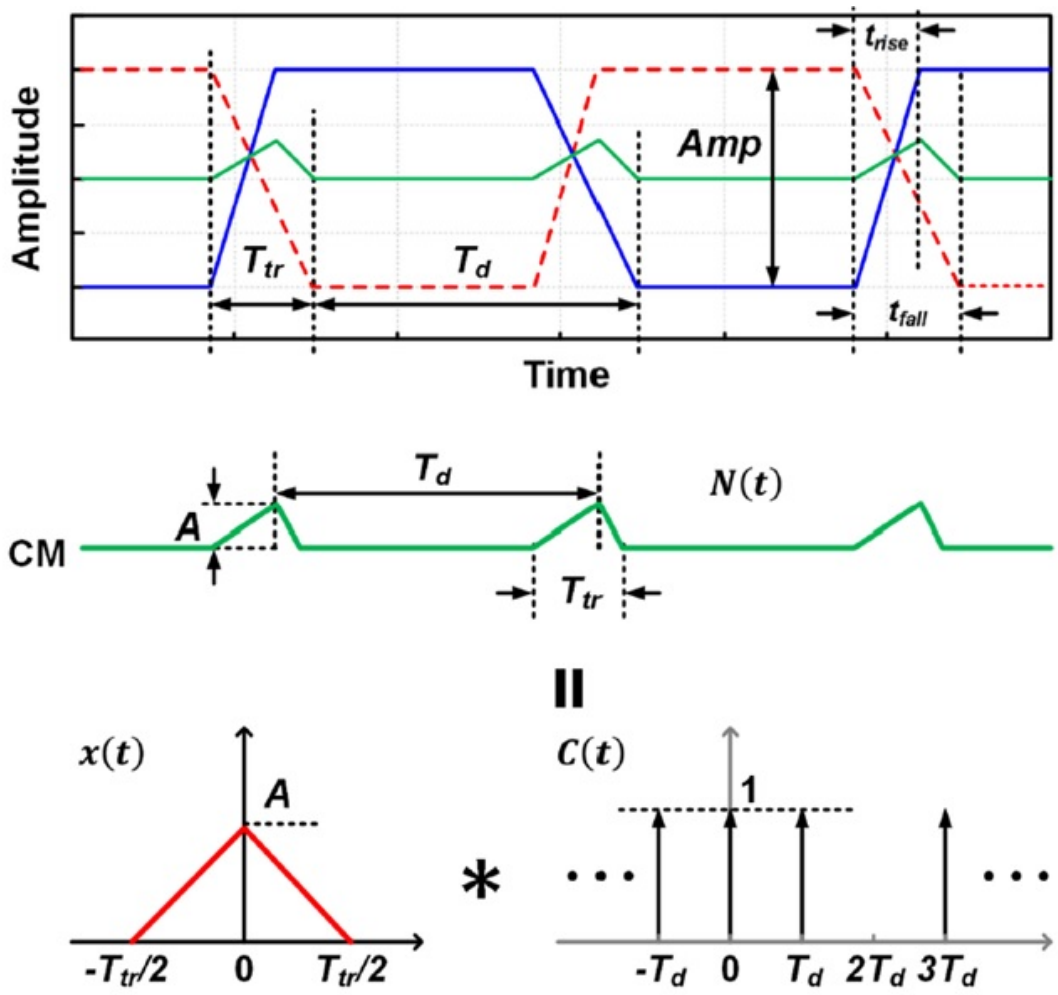

Figure 3.2: CM noise signal and its approximation for calculation [3].

data transition time, which is calculated as the maximum quantity between t_{rise} and t_{fall}, i.e, max(t_{rise},t_{fall}). The differential signal amplitude is Amp. Fourier transformation of the CM noise signal should be performed to determine the value of the CM noise at $2F_{Nyquist}$. However, the Fourier transform cannot be applied directly on the CM noise signal, as it is a random signal generated by the PRBS generator. Thus, the auto-correlation function and the corresponding power spectral density are utilized to estimate the CM noise spectrum.

A spike on the CM noise signal is generated during every data transition, which can be approximated as an isosceles triangle having height A and width T_{tr}. The height A of an isosceles triangle-shaped CM spike is calculated by equation (3.3), where the rising and falling edges are considered linear:

$$A = \frac{|t_{rise} - t_{fall}|}{T_{tr}} \times \frac{Amp}{2} = \frac{|t_{rise} - t_{fall}|}{max(t_{rise}, t_{fall})} \times \frac{Amp}{2}, \tag{3.3}$$

Meanwhile, the Fourier transform of a triangle-shaped CM noise signal $x(t)$ is, calculated as

$$X(f) = F(x(t)) = \frac{1}{2} A \times T_{tr} \times sinc^2\left(\pi \frac{T_{tr}}{2} f\right). \tag{3.4}$$

The final equation of the CM noise at $2F_{Nyuist}$ after the complete derivation in [3] is given as

$$N(2F_{Nyquist})_{NRZ} = \frac{1}{4} A \frac{T_{tr}}{T_b} sinc^2\left(\frac{\pi}{2} \frac{T_{tr}}{T_b}\right), \tag{3.5}$$

$$N(2F_{Nyquist})_{NRZ} = \frac{1}{8} Amp \frac{|t_{rise} - t_{fall}|}{T_b} sinc^2\left(\frac{\pi}{2} \frac{T_{tr}}{T_b}\right), \tag{3.6}$$

where Amp is the amplitude, t_{rise} is the rise time, t_{fall} is the fall time, T_b is the data time period, and T_{tr} is the data transition period, i.e., $max[t_{rise}, t_{fall}]$. The CM noise (N(f)) is power spectral density in W/Hz. The highest amplitude harmonic component of the CM noise, which is at twice the Nyquist frequency, is represented by $N(2F_{Nyquist})_{NRZ}$ in the above equation. Equation (3.6) demonstrates that the CM noise is calculated by the ratio T_{tr}/T_b and amplitude

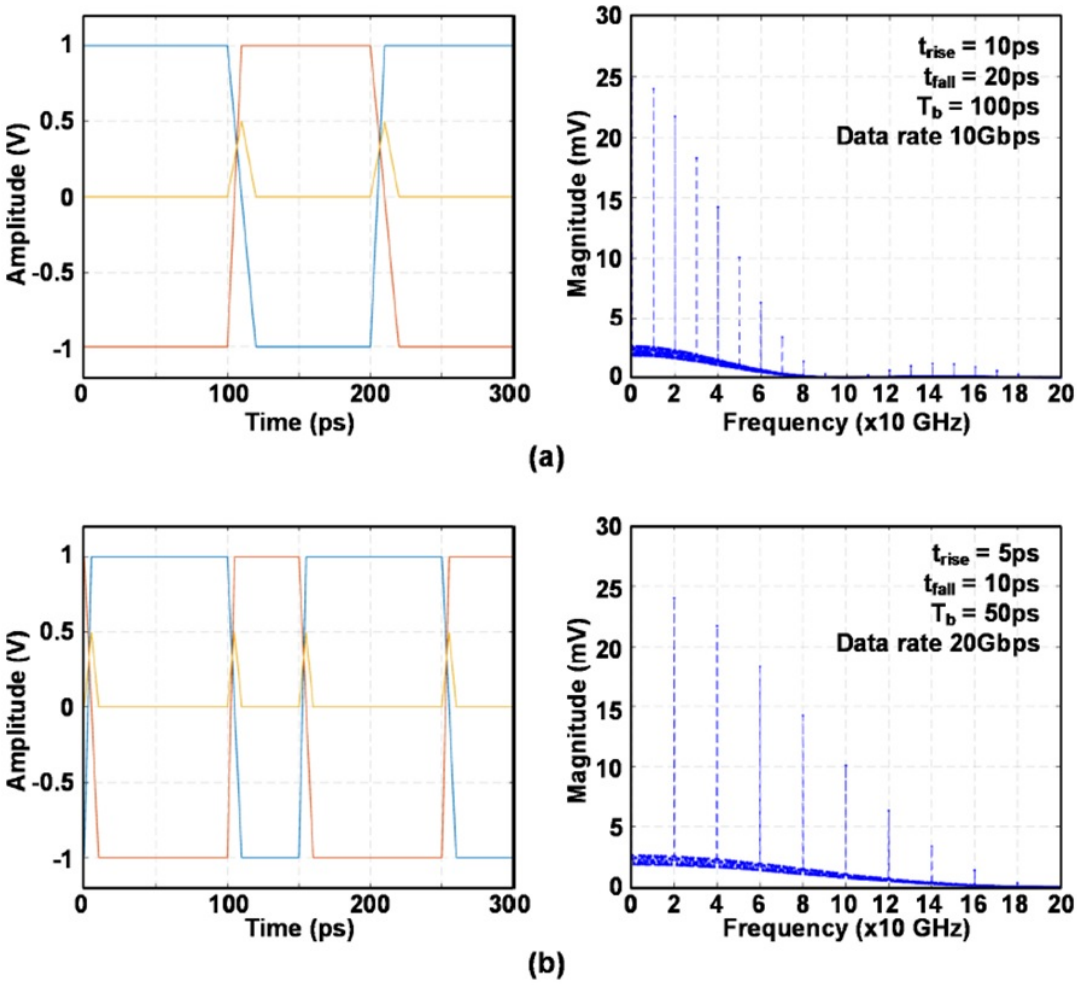

Figure 3.3: MATLAB simulation of CM noise transient waveform and its spectrum at input data rate of (a) 10 Gbps and (b) 20 Gbps for NRZ wireline transmitter [3]

A of the CM noise spike as A is positively correlated to Amp, as presented in equation (3.3). The CM noise generated from the CML driver $(N(2F_{Nyquist})_{NRZ})$ is directly proportional to the input signal swing, data rate $(1/T_b)$ and difference of the mismatch between the rise and fall time. These are the key factors designers need to optimize for minimum CM noise in an NRZ transmitter.

The behavior-level simulation to validate equation (3.6) in MATLAB is shown in Figure 3.3, where the sinc function providing the spectrum envelope and the noise tone at $1/T_b$ is the largest among all the harmonics.

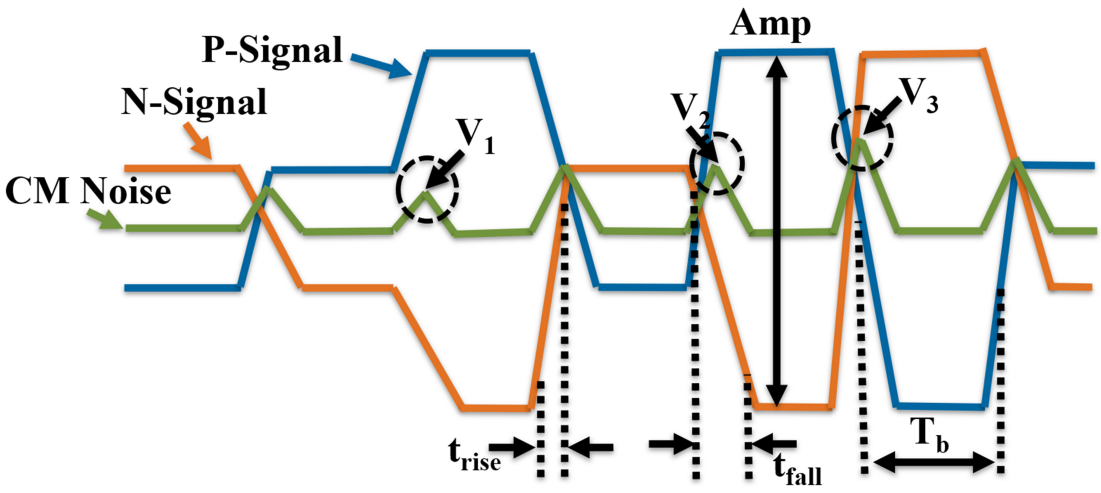

Figure 3.4: CM noise generation in PAM-4 transmitter due to rise and fall time mismatch in P- and N-signals [4]

The transient CM noise and differential PAM-4 positive (P-) and negative (N-) signals at the output of the PAM-4 transmitter are presented in Figure 3.4, where V_1, V_2 and V_3 are different amplitudes of the CM noise, Amp is the total amplitude, t_{rise} is the rise time, t_{fall} is the fall time, and T_b is the data time period of the PAM-4 signal. The CM noise generation in a PAM-4 transmitter is complicated as compared to the NRZ case discussed previously. In the latter case, there is only one amplitude of CM noise, whereas in the PAM-4 case, there are three different amplitudes, namely, V_1, V_2, and V_3, as shown in Figure 3.4, which depend on the number of bits switched at the output. Twelve possible transitions and only four switching cases exist in a PAM-4 transmitter, as listed in Table 3.1, where the LSB and MSB are the input data signal. The CM noise amplitudes under different data patterns and the corresponding ratios of amplitude (R factor) are presented in Table 3.1. As mentioned earlier, the sizes of the transistors in the MSB stage are two times greater than those in the LSB stage, so this stage will generate double the CM noise as compared to the latter stage. Hence, the LSB stage produces one third of the highest amplitude (V_3) of the CM noise in the CML driver. To incorporate variation of the CM noise with bit transition, an R factor (R_F) is introduced in equation (3.6) [4]. The mathematical formula of the CM noise generated from the CML driver

Table 3.1: Effect of bit switching in PAM-4 transmitter on CM noise.

Input Data		CM Noise Amplitude (mV)	R Factor
LSB	MSB		
0	0	0	0
1	0	V_1	0.33
0	1	V_2	0.66
1	1	V_3	1

$(N(2F_{Nyquist})_{CML})$ for a PAM-4 transmitter is given by

$$N(2F_{Nyquist})_{CML} = \frac{1}{8} R_F Amp \frac{|t_{rise} - t_{fall}|}{T_b} sinc^2\left(\frac{\pi}{2}\frac{T_{tr}}{T_b}\right), \tag{3.7}$$

where the factors Amp, t_{rise}, t_{fall}, T_b and T_{tr} are depicted in Figure 3.4 and are the same as in equation (3.6), while R_F is given in Table 3.1 based on the number of bit transitions. The CM noise in the PAM-4 case is also directly proportional to the rise and fall mismatch. When an equal probability of the occurrence of the twelve transitions is considered, the average value of the R factor is 0.5, which means CM noise generated by the CML driver in PAM-4 is smaller than in the NRZ case. Equation (3.7) gives the approximate value of the CM noise in the PAM-4 transmitter because of the non-ideal factors in the actual implemented circuit, and the CM noise signal is also approximated as an isosceles triangle in the derivation of equation (3.7).

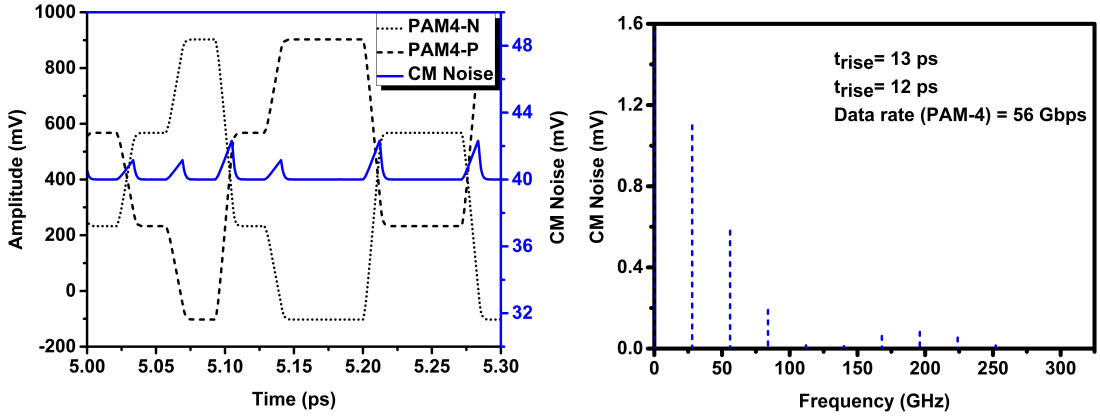

Figure 3.5: MATLAB simulation of transient PAM-4 P-/N-signal, CM noise signal and its spectrum.

The behavior-level simulation to validate equation (3.7) in MATLAB is shown in Figure 3.5, which depicts the transient PAM-4 P- and N-signal, CM noise signal and its spectrum.

3.1.1 PAM-4 Optical Transmitter Test Bench

The 56 Gbps PAM-4 optical transmitter test-bench shown in Figure 3.6 is used to analyze the CM noise sources using the Cadence Virtuoso analog design environment. The CML is implemented in 40 nm CMOS technology. The wavelength of PAM-4 56 Gbps signal is 2.14 cm. Binary data are produced by a PRBS generator, which generates the LSB and MSB data bits of a bit period (T_b) for the transmitter. The signal from the PRBS generator is fed into the CML driver. A 50 ohm termination is connected at the output with a 50 fF load capacitance, and beads are used to block the high-frequency signals from the supply source. A non-linear laser model is connected across output terminals V_{outP} and V_{outN} of the transmitter by a coupling capacitor, and a CML driver circuit drives this laser. The effect of the bond-wire is not included in the test-bench, as it has already been demonstrated in [3] that a mismatched interconnection channel does not contribute considerably to CM noise.

The CM noise at the output of the transmitter is noise generated by the

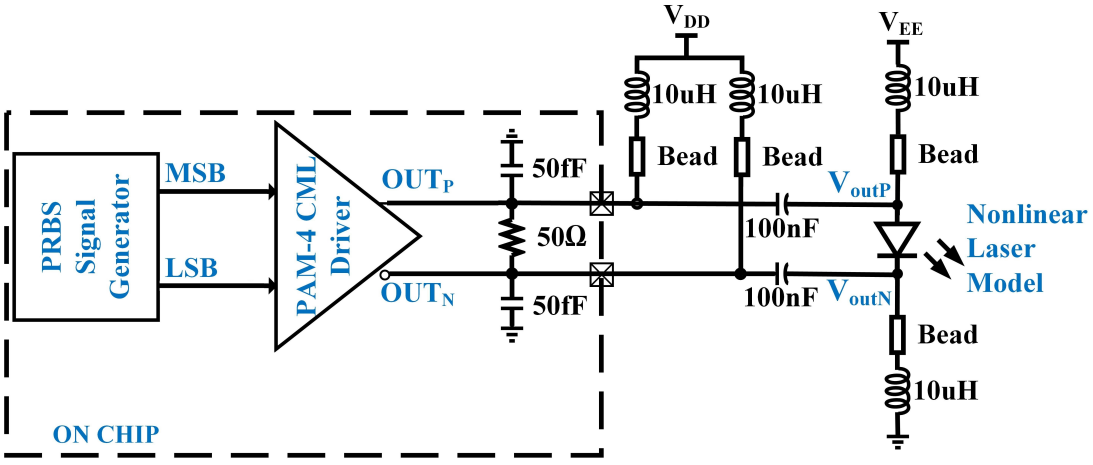

Figure 3.6: Schematic of 56 Gbps PAM-4 optical transmitter.

CML driver circuit, and is given by equation (3.7). To determine the value of the CM noise, its spectrum needs to be determined. The CM noise is calculated by taking the average of the differential output signals P-signal (V_{OUTP}) and N-signal (V_{OUTN}). The equation of the CM noise voltage at the output of the transmitter is given as

$$V_{CM}(t) = \frac{(V_{OUTP}(t) + V_{OUTN}(t))}{2}. \tag{3.8}$$

To find the spectrum of the above transient CM noise voltage, the discrete Fourier transform (DFT) is performed, as given by

$$\begin{aligned} F(\omega) &= DFT(V_{CM}(t)), \\ N(2F_{Nyquist})_{Total} &= |F(2f_{Nyquist})|. \end{aligned} \tag{3.9}$$

The harmonic components can be observed at integer multiples of the Nyquist frequency in the resultant frequency spectrum. However, the magnitude of the CM noise $N(2F_{Nyquist})_{Total}$ is determined by the harmonic at twice the Nyquist frequency which has the highest amplitude, as calculated in equation (3.9). Other harmonic components have smaller amplitudes and can be neglected. Therefore, to determine the CM noise, only the harmonics at twice the Nyquist frequency are considered in subsequent analysis.

3.1.2 Simulation Results and Discussion

Five cases are simulated to study their effect on CM noise. The transient PAM-4 P- and N-signal and the CM noise signal and spectrum of the differential mode (DM) and CM noise at the output terminals V_{outP} and V_{outN} of the transmitter are depicted in Figures 3.7– 3.11 for all five cases. Results are summarized in Table 3.2. The input data signal has an amplitude of 100 mV and rise/fall time of 12 ps with a data rate of 56 Gbps.

In the first case, the ideal differential PAM-4 signal is considered. It can be

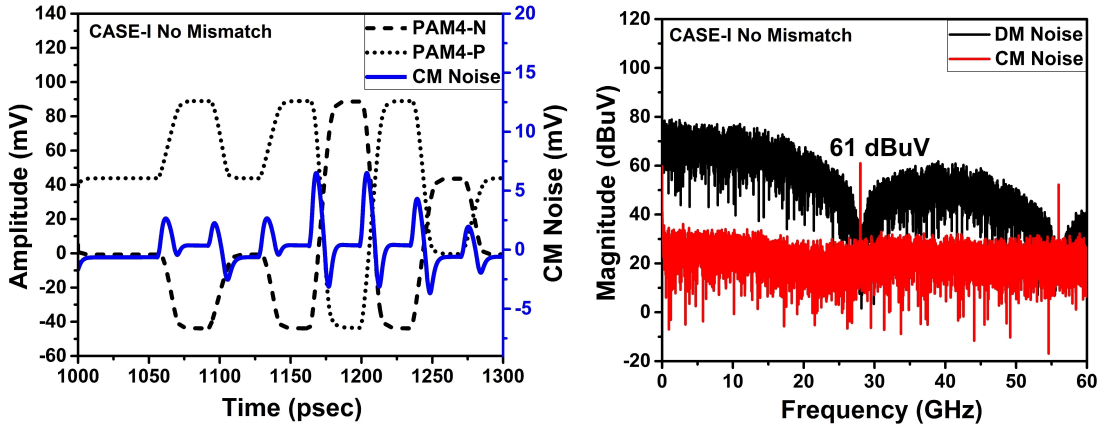

Figure 3.7: Simulation results of case without distortion, presenting transient PAM-4 N- and P-signal, CM noise signal, and spectrum of CM and DM signal at output of optical transmitter.

observed in the simulation graph depicted in Figure 3.7 that there are harmonics at the Nyquist frequency and its multiple. The amplitude of the harmonics at twice the Nyquist frequency is highest and considered as the CM noise, which is 61 dBuV in case of without distortion. The reason for these harmonics is discussed in the previous Section 3.1, and given by equations (3.1) and (3.2). There is an imbalance between the charging and discharging paths of the CML driver due to the variation in internal capacitance and resistance of the transistor, which generates CM noise. The DM signal has no tones at the Nyquist frequency and its multiple.

In the next three cases, the effects of linear distortion, specifically amplitude, skew and BW mismatch, are simulated. In the second case, we consider the amplitude, as depicted in Figure 3.8. The difference in amplitude occurs because of the device mismatch in the differential pair. The maximum imbalance between the transistors is around 2%, as observed in Monte Carlo analysis, because the CML driver has only NMOS transistors. The extreme case of 10% mismatch is considered. The amplitude of the positive input is 10% higher than the negative. The third case, the skew mismatch, is presented in Figure 3.9. The source of the skew is the different lengths of the positive and negative paths, which causes the differential signal to arrive at different times.

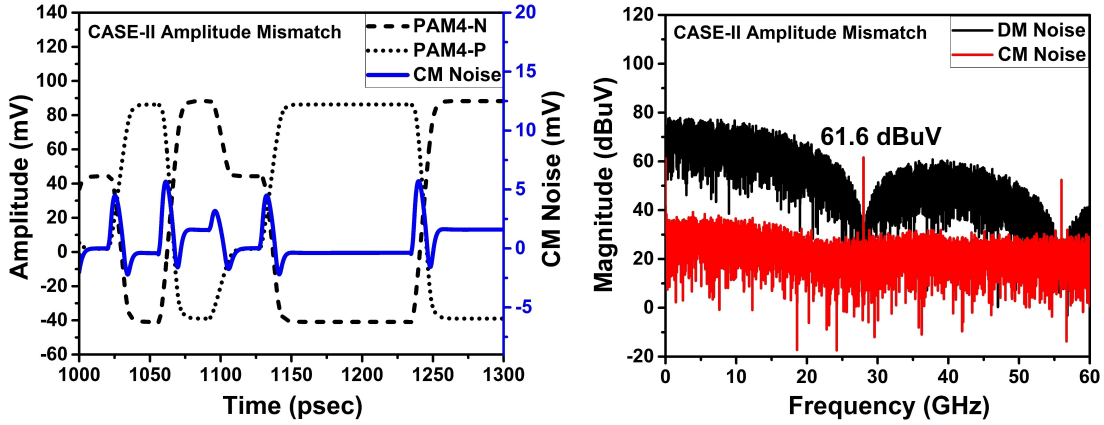

Figure 3.8: Simulation results of amplitude mismatch case, presenting transient PAM-4 N- and P-signal, CM noise signal, and spectrum of CM and DM signal at output of optical transmitter.

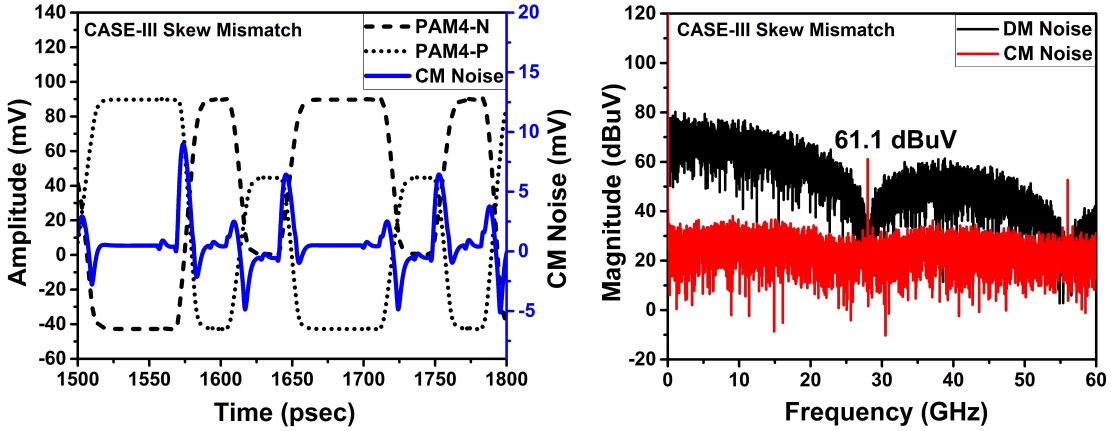

Figure 3.9: Simulation results of skew mismatch case, presenting transient PAM-4 N- and P-signal, CM noise signal, and spectrum of CM and DM signal at output of optical transmitter.

A time delay mismatch of 10% between the positive and negative input signal is introduced. In the fourth case, we consider the BW mismatch, as presented in Figure 3.10. The difference in BW occurs due to the imbalanced loading of the positive and negative signal path. Higher capacitive loading reduces the BW. The BW mismatch is introduced by making the rise and fall time of the negative signal 20% higher than that of the positive signal. None of these cases contributes significantly to the rise and fall time mismatch. Hence, there is no considerable increase in the CM noise, as presented in Table 3.2 and shown in Figure 3.7– 3.10.

In the last case, the non-linear distortion, which includes the effect of the rise and fall time imbalance, is observed. The unequal rise and fall times are due to the different charging and discharging paths of the signal. When the rise time of the negative and positive signal is 50% higher than the fall time, there is a significant increase in the CM noise, as demonstrated in Figure 3.11.

The simulation results are summarized in Table 3.2, where A_P/A_N is the input amplitude of the P-/N-signal, t_P/t_N is the delay in the input P-/N-signal, t_{rP}/t_{rN} is the rise time of the input P-/N-signal, t_{fP}/t_{fN} is the fall time of the input P-/N-signal, and V_{CM} is the CM noise level at the transmitter output. The

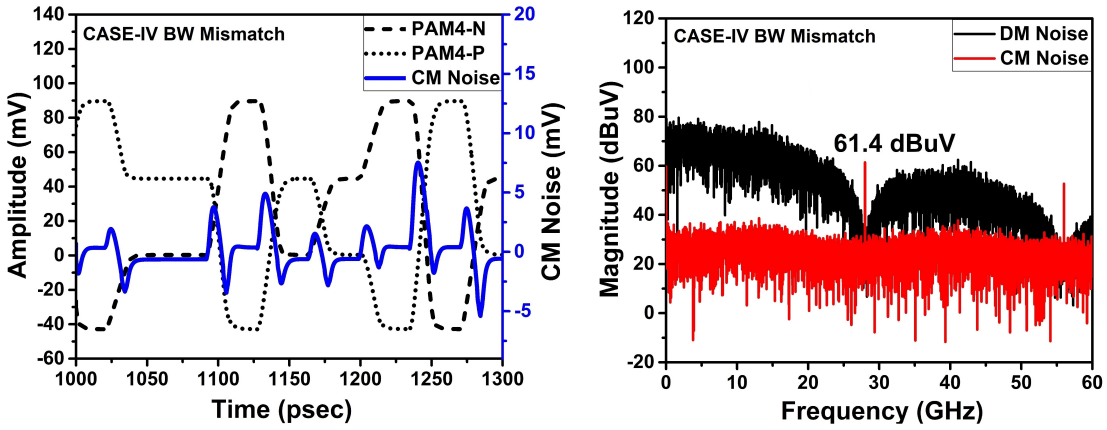

Figure 3.10: Simulation results of BW mismatch case, presenting transient PAM-4 N- and P-signal, CM noise signal, and spectrum of CM and DM signal at output of optical transmitter.

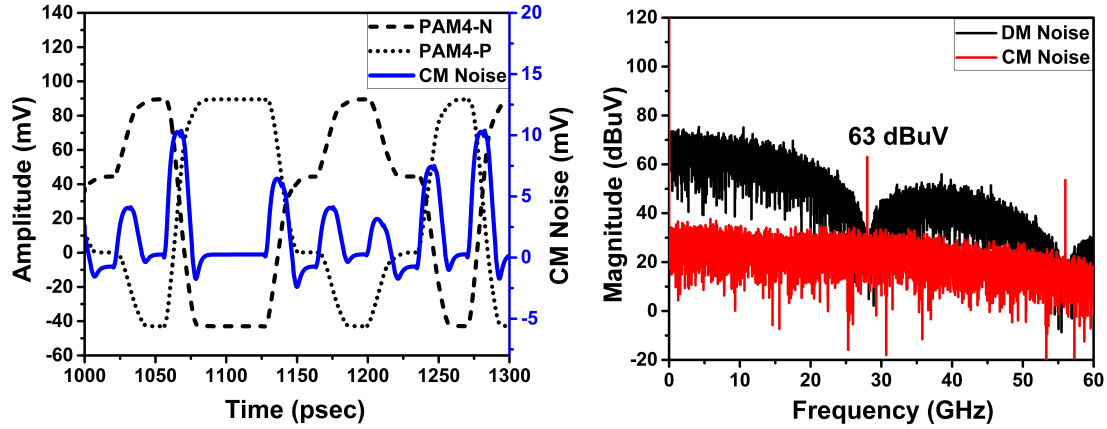

Figure 3.11: Transient PAM-4 N- and P-signal, CM noise signal, and spectrum of CM and DM signal at output of optical transmitter with rise time greater than fall time.

Table 3.2: Comparison of CM noise in linear and non-linear distortion in PAM-4 optical transmitter.

Mismatch	**Input Swing (mV)**		**Input Time Delay (ps)**		**Input Rise and Fall Time (ps)**				**Output CM Noise (dBuV)**
	A_P	A_N	t_P	t_N	t_{rP}	t_{fP}	t_{rN}	t_{fN}	V_{CM}
No Mismatch	100	100	0	0	12				61
Amplitude	110	100	0	0	12				61.6
Skew	100	100	13.2	12	12				61.1
Bandwidth	100	100	0	0	14.4	14.4	12	12	61.4
Fall & Rise time	**100**	**100**	**0**	**0**	**20**	**12**	**20**	**12**	**63**

last case is highlighted as it generates the highest value of noise in the transmitter. The simulation results show that the linear distortion, which includes amplitude, skew and BW mismatch, does not cause an EMI-related CM noise problem. Instead, it is the non-linear distortion and intrinsic impedance variations of the CML driver that are the contributors to the generation of EMI-related CM noise [4], as expected by the mathematical analysis presented in Section 3.1.

3.2 Analysis of PAM-4 FFE Circuit

The FFE is utilized to reduce the ISI produced due to the transient non-linearity and BW limitation of the laser or channel. The behavioral implementation of a FSA-FFE supporting PAM-4 signaling is discussed in Chapter 2, Section 2.4 and the block diagram is given in Figure 2.6. The FSA-FFE unequally increases/decreases the rise and fall time of the transmitter output, which can directly affect the CM noise. If the equalization increases the mismatch between the rise and fall time, then it will increase the EMI-related CM noise, as discussed in Chapter 1, Section 1.1. The principle of the FSA-FFE is presented in Figure 3.12. The rise and fall pulses introduced

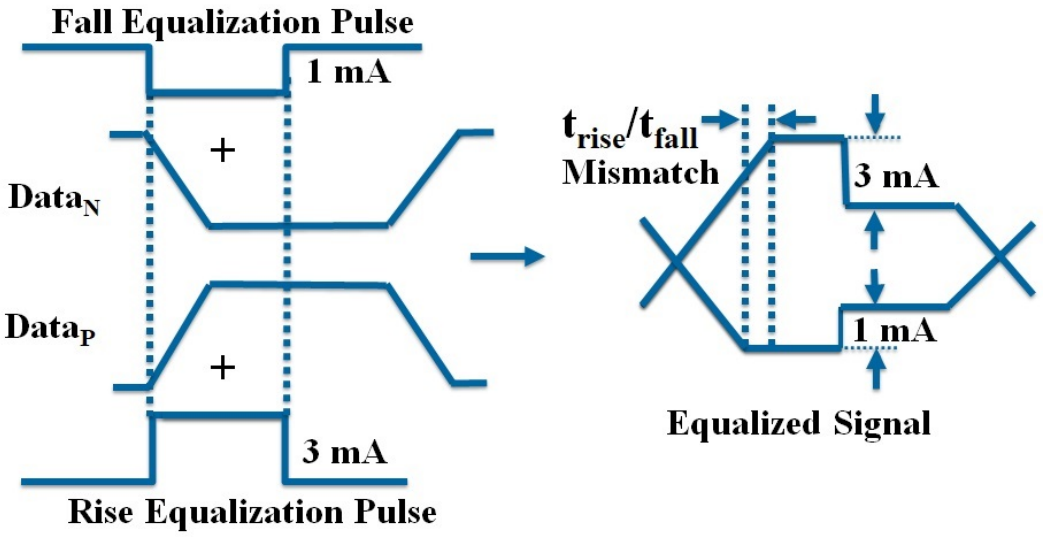

Figure 3.12: Increase in mismatch of rise and fall time due to FFE.

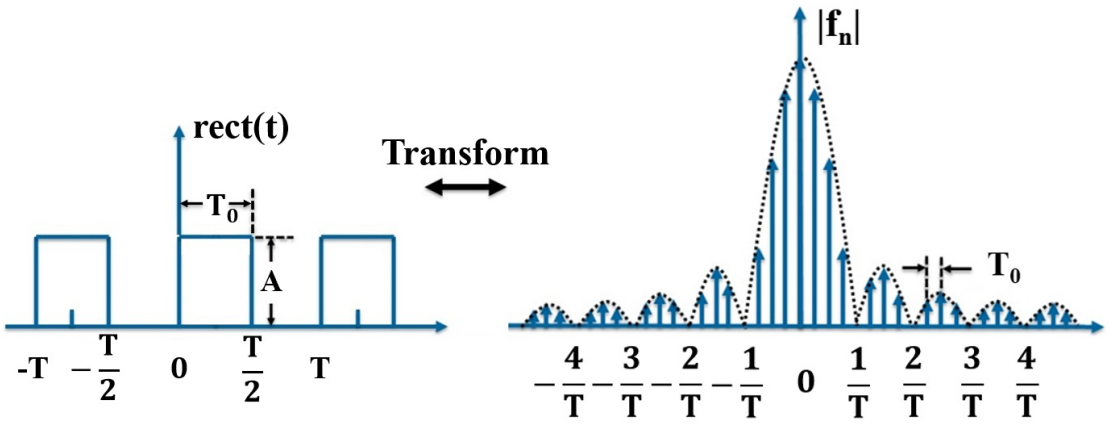

Figure 3.13: Rectangular signal and its spectrum.

by the equalization change the rise time by 3 mA and fall time by 1 mA, which results in a pre-distorted signal. The falling edge reaches its maximum earlier than the rising edge in a pre-distorted signal. This introduces a time mismatch, and hence EMI-related CM noise will be increased. Also, if there is offset in the output differential stage of the FFE, it will generate CM current, which further increases the CM noise.

To analyze the effect of FFE, we consider an input data signal constituted of consecutive 1s and 0s. Then we can approximate the FFE output pulses as a periodic rectangular signal, rect(t), as depicted in Figure 3.13, and we can apply

the Fourier transform to calculate the values of each frequency component shown in Figure 3.13. Consider $|f_n|$ as the required frequency spectrum of the rect(t) signal with amplitude A, time period T, and FFE pulse width (PW) equal to T_0. The Fourier equation for the rect(t) signal is given as

$$f_n = \frac{1}{T}\int_0^T rect(t) \times e^{\left(\frac{-j2.\pi.nt}{T}\right)}\, dt, \tag{3.10}$$

where rect(t) is given as

$$\begin{aligned} rect(t) = A \quad at\ t\ &=\ 0\ to\ \frac{T}{2} \\ 0 \quad at\ t\ &=\ \frac{T}{2}\ to\ T. \end{aligned} \tag{3.11}$$

Hence, equation (3.10) reduces to equation (3.12):

$$f_n = \frac{1}{T}\int_0^{\frac{T}{2}} rect(t) \times e^{\left(\frac{-j2.\pi.nt}{T}\right)}\, dt, \tag{3.12}$$

$$f_n = \frac{A}{n.\pi} sin\left(n.\pi.\frac{T_0}{T}\right) = \frac{A.T_0}{T} sinc\left(n.\pi.\frac{T_0}{T}\right). \tag{3.13}$$

The harmonic of the the FFE noise signal with the highest magnitude will be at twice the Nyquist frequency ($N(2F_{Nyquist})_{FFE}$), and can be determined by putting n =1 into equation (3.13):

$$f_1 = N(2F_{Nyquist})_{FFE} = \frac{A}{\pi} sin\left(\pi\frac{T_0}{T}\right). \tag{3.14}$$

The offset in the differential output stage of the FFE generates CM current which is directly added into the CM noise at the output of the transmitter. The CM noise generated by the FFE with offset is given by

$$N(2F_{Nyquist})_{FFE} = \frac{A}{\pi} sin\left(\pi\frac{T_0}{T}\right) \ +\ offset. \tag{3.15}$$

Equation (3.15) depicts that the amplitude (A), the FFE PW (T_0), and offset in the output stage directly affects the CM noise generated by the FFE ($N(2F_{Nyquist})_{FFE}$) [5]. The values of $N(2F_{Nyquist})_{FFE}$ with variation of the

Table 3.3: Effect of different PWs of FFE on CM noise.

PW of FFE (T_0) (ps)	**CM Noise ($N(2F_{Nyquist})_{FFE}$) (mV)**
1-UI	0 + offset
0.8-UI	0.58A + offset
0.5-UI	0.32A + offset
0.4-UI	0.3A + offset
0.25-UI	0.23A + offset

FFE PW are presented in Table 3.3, which shows that if the T_0 is equal to the T and the offset value is zero, then the CM noise is not generated from the FFE. Otherwise, the CM noise will increase. It can be inferred from Table 3.3 that an FFE PW of 0.25-UI results in smaller CM noise as compared to 0.5-UI. However, a higher equalization magnitude (A) is needed at the FFE PW of 0.25-UI to get greater compensation, which results in higher BW improvement at the cost of greater CM noise and power consumption.

The equation for total CM noise ($N(2F_{Nyquist})_{Total}$) at the output of the transmitter is given by

$$N(2F_{Nyquist})_{Total} = N(2F_{Nyquist})_{CML} + N(2F_{Nyquist})_{FFE}. \tag{3.16}$$

The $N(2F_{Nyquist})_{Total}$ is a combination of the CM noise generated by the CML driver circuit $N(2F_{Nyquist})_{CML}$, given by equation (3.7), and the FFE circuit $N(2F_{Nyquist})_{FFE}$, determined by equation (3.15). By putting the values of $N(2F_{Nyquist})_{CML}$ and $N(2F_{Nyquist})_{FFE}$ into equation (3.16), we get

$$N(2F_{Nyquist})_{Total} = \frac{1}{8} R_F Amp \frac{|t_{rise} - t_{fall}|}{T_b} sinc^2\left(\frac{\pi}{2}\frac{T_{tr}}{T_b}\right) + \frac{A}{\pi} sin\left(\pi \frac{T_0}{T}\right) + offset. \tag{3.17}$$

This equation can be used to predict CM noise in optical transmitters more accurately.

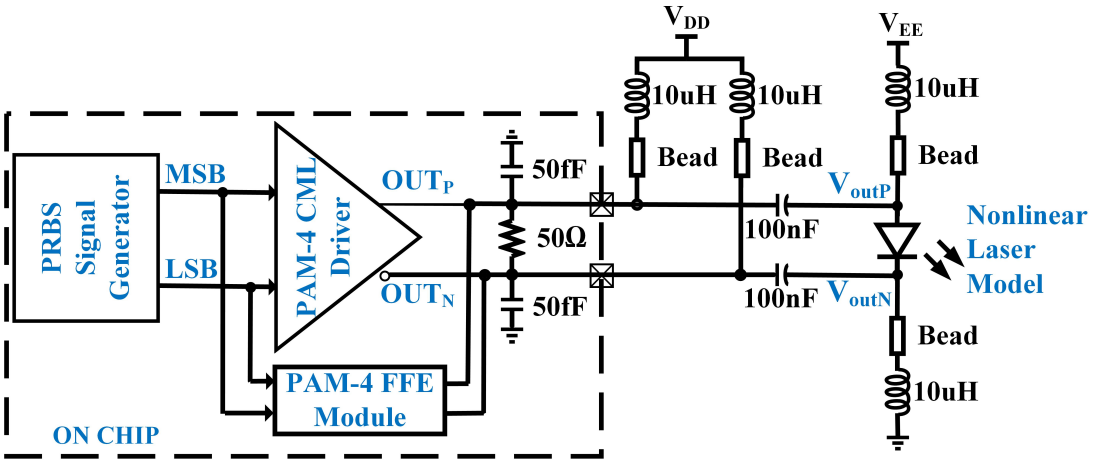

Figure 3.14: Schematic of test-bench to analyze CM noise under different FFE configurations in 56 Gbps PAM-4 optical transmitter.

3.2.1 Simulation Results and Discussion

The test-bench, as depicted in Figure 3.14, is designed in 14 nm FinFET SMIC technology and simulated using the Cadence Virtuoso analog design environment to investigate the effect of different FFE configurations on CM noise in a 56-Gbps PAM-4 optical transmitter. The test-bench is the same as explained in Section 3.1.1, except that an FFE module is included and the technology node is 14 nm FinFET instead of 40 nm CMOS. The cumulative CM noise is measured at the output terminals V_{outP} and V_{outN}, as given by equation (3.17).

Three configurations of the FFE circuit, symmetric, asymmetric and asymmetric with offset, are simulated with different FFE PW settings (1-UI, 0.8-UI, 0.6-UI, 0.5-UI, 0.4-UI and 0.25-UI) to study their effect on the CM noise. In the symmetric FFE configuration, the coefficients of the FFE rise and fall pulses are equal, whereas in the asymmetric configuration, the coefficients are unequal. To observe the effect of offset on CM noise, a 2% offset of the differential pair in the output stage of the FFE is included in the last configuration.

The CM noise of 62.3 dBuV is generated by the CML driver circuit, as presented in Figure 3.15. The optical eye and CM noise spectrum for the

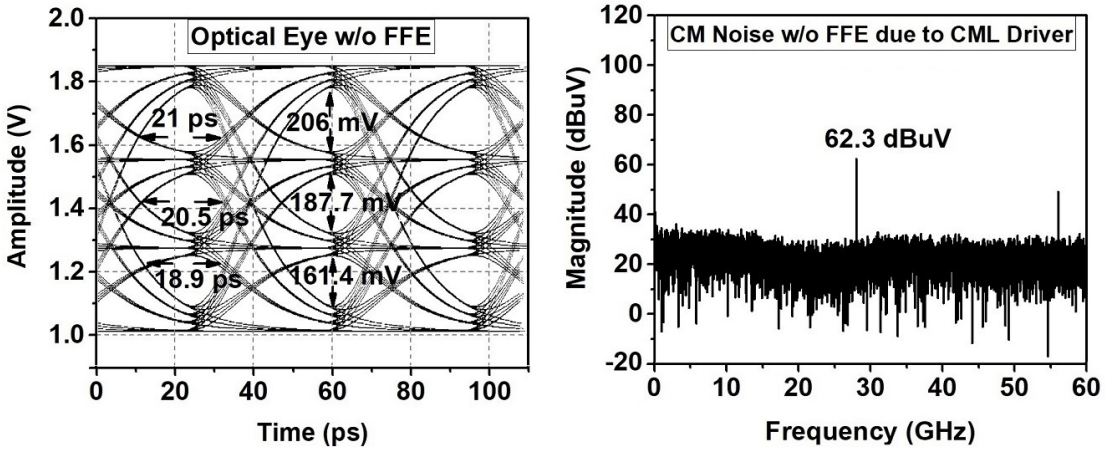

Figure 3.15: Simulation results showing optical eye and spectrum of CM noise signal without FFE at the output of the 56-Gbps PAM-4 optical transmitter.

symmetric and asymmetric 0.25-UI FFE configurations are depicted in Figure 3.16. The CM noise increases by only 1.3 dBuV in 0.25-UI symmetric FFE, whereas the increase in the 0.25-UI asymmetric FFE is much higher, at

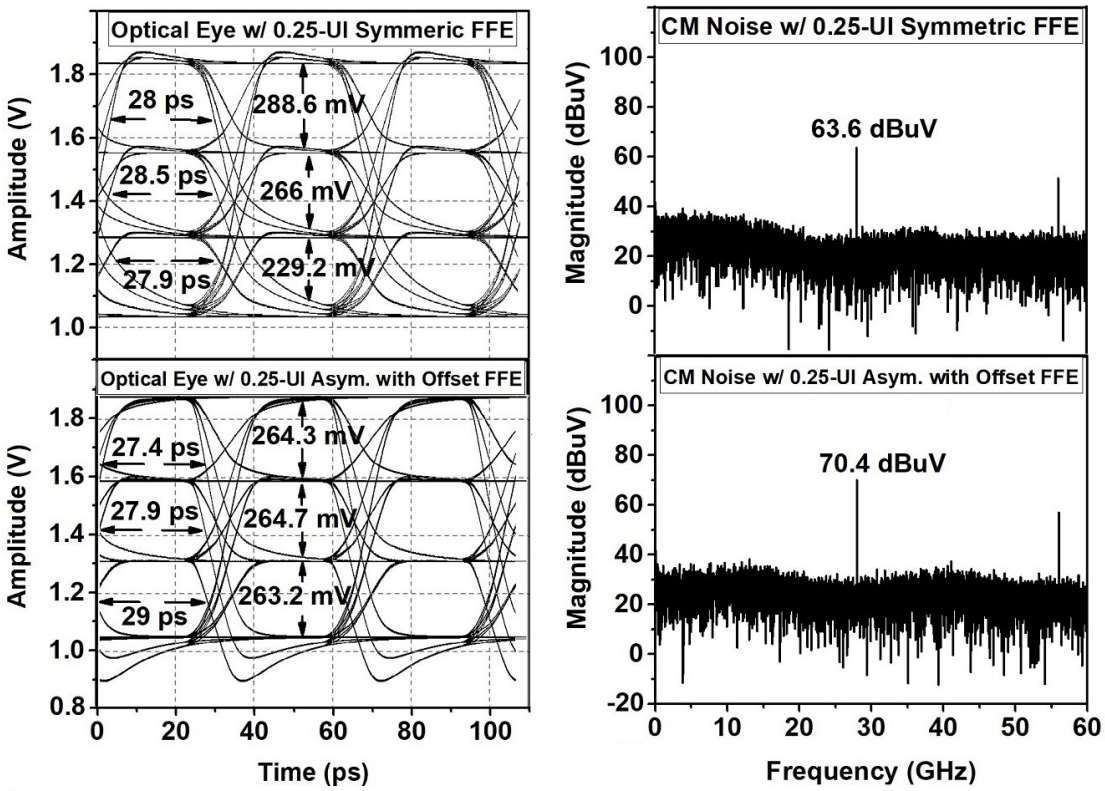

Figure 3.16: Simulation results showing optical eye with symmetric and asymmetric 0.25-UI FFE with offset configuration and respective spectrum of CM noise signal at the output of the 56-Gbps PAM-4 optical transmitter.

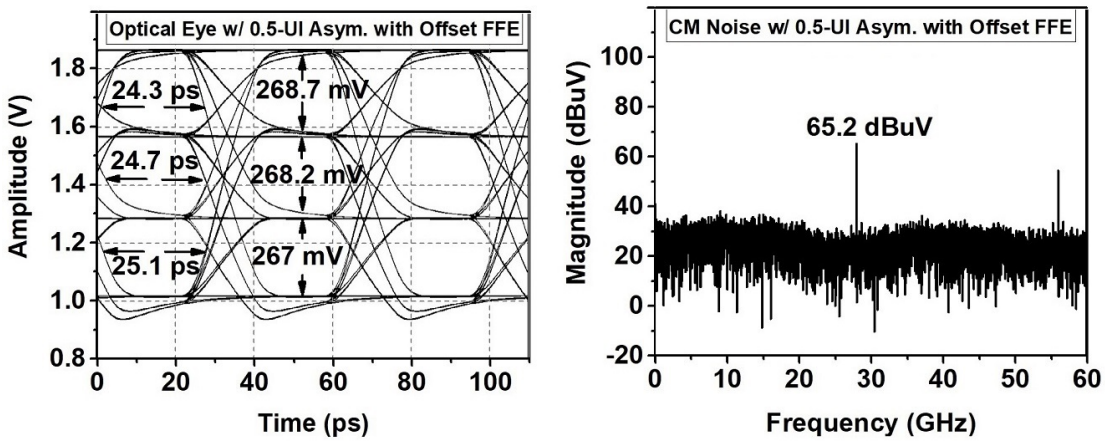

Figure 3.17: Simulation results showing optical eye and spectrum of CM noise signal with 0.5-UI asymmetric FFE with offset configuration at the output of the 56-Gbps PAM-4 optical transmitter.

about 8 dBuV. This is due to the higher value of the equalization current. The bottom eye needs more compensation as compared to the other eye openings, and the asymmetric FFE has more freedom of compensation because of the unequal coefficients, which results in a 39% improvement in the bottom vertical eye opening as compared to the 29% improvement of the symmetric configuration. It can also be observed that the optical eye opening and CM noise increase with the decrease of the FFE PW, as discussed in the mathematical analysis in Section 3.2. The CM noise increases by 154% at the FFE PW of 0.25-UI and 40% at the FFE PW of 0.5-UI in the asymmetric with offset configuration, as shown in Figure 3.16 and 3.17, respectively.

The percentage increases in the amplitude of the CM noise, equalization current and horizontal optical eye opening with different FFE configurations and PWs are presented in Figure 3.18 and 3.19. The asymmetric with offset configuration results in a highest increase in CM noise of 154% at the FFE PW of 0.25-UI, because the offset generates CM current, which directly increases the CM noise at the output of the transmitter, as presented in equation (3.15). The magnitude of the equalization current increases with the decrease of FFE PW, which results in higher power consumption and CM noise, as suggested by equation (3.15). However, BW improvement is also gained with a decrease in

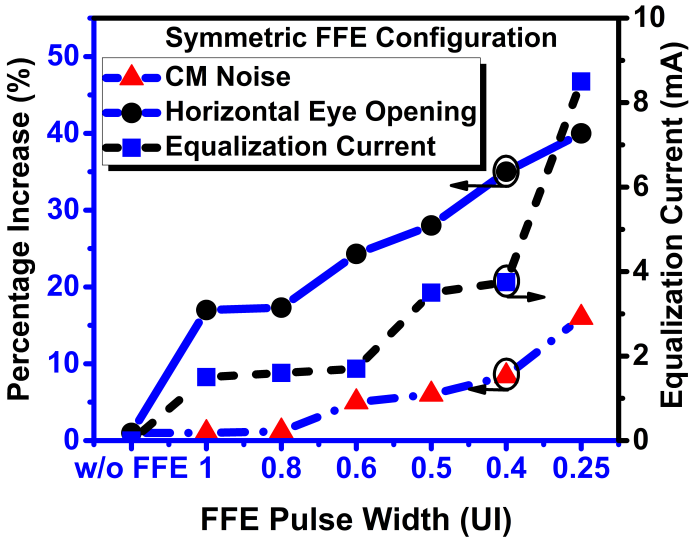

Figure 3.18: The increase in the amplitude of CM noise, equalization current and horizontal optical eye opening with different symmetric FFE settings, with reference to the without FFE case.

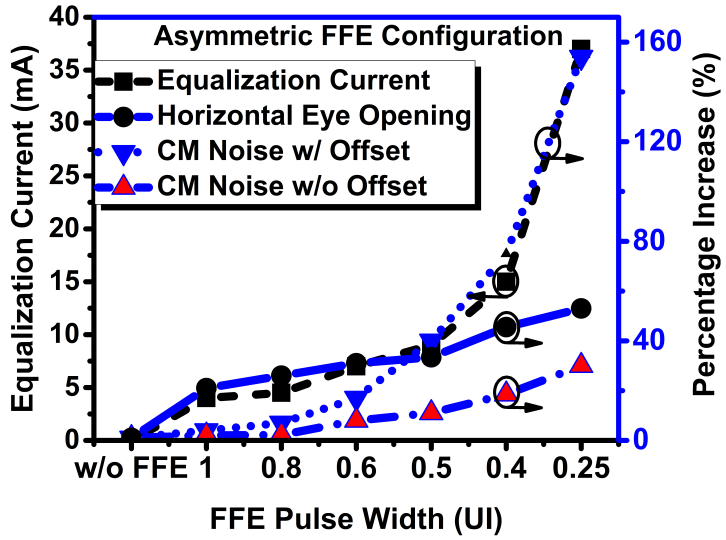

Figure 3.19: The increase in the amplitude of CM noise, equalization current, and horizontal optical eye opening with different asymmetric FFE settings, with reference to the without FFE case.

the FFE PW. The equalization current for the bottom eye is 4 mA at the FFE PW of 1-UI, whereas it is 37 mA at the FFE PW of 0.25-UI. Meanwhile, the horizontal eye opening improves by 13% at the FFE PW of 1-UI and 35% at the FFE PW of 0.25-UI in the asymmetric configuration. The optimal configuration

is 0.4-UI, as depicted in Figure 3.19, where BW improvement is higher with a moderate increase in CM noise and power consumption [5]. When the FFE PW is decreased further, the CM noise and equalization current increase rapidly, but it does not give much improvement in the BW.

To reduce the CM noise generated by FFE, offset should be minimized and the optimal FFE configuration should be selected carefully for each application.

3.3 Summary

The effects of the PAM-4 CML driver and different FFE configurations are analyzed in this chapter, and it is demonstrated that the intrinsic impedance variations of the CML driver circuit, amplitude of the equalization current, and offset in the FFE circuit are the main sources of EMI-related CM noise in transmitters.

The CM voltage should be a DC signal at the output of the transmitter. However, the mismatch between the rise and fall time of the differential signal generates monotonic spurs in the CM voltage, which creates a spectral tone at twice the Nyquist frequency. These tones radiate in the environment and cause EMI issues in the devices. The rise and fall mismatch is due to the internal impedance variations of the MOS devices in the circuits.

A systematic way of selecting an optimal FFE configuration is proposed, and it is suggested that reducing the offset of the FFE and selecting an optimal configuration reduces the CM noise significantly.

3.4 References

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Chapter 4

Effect of Technology Scaling on CM Noise

Since Gordon Moore's famous prediction in 1965, the trend in scaling in integrated circuit (IC) devices has continued, making advanced applications like artificial intelligence and augmented reality possible. The majority of digital and analog ICs have used MOSFET devices since the 1960s. However, due to channel length and leakage current limitations, FinFETs have become the dominant manufactured device in technology nodes of 16 nm or below, as used for advanced communication technologies like 4G and 5G, as presented in Figure 4.1.

As presented in Chapter 3, Section 3.1, the CM noise depends on the parasitic impedance of the device. This parasitic impedance scales down with the device size, and it is clear that CM noise reduces as it decreases. However, FinFETs have higher parasitic impedance due to their 3D structure, despite their smaller sizes. It is still unknown how device scaling, particularly of FinFET devices, affects the CM noise. In this chapter, we evaluate the effect of technology scaling on CM noise by comparing CM noise generation in CML driver circuits designed in the 40 nm CMOS and 14 nm FinFET technology nodes.

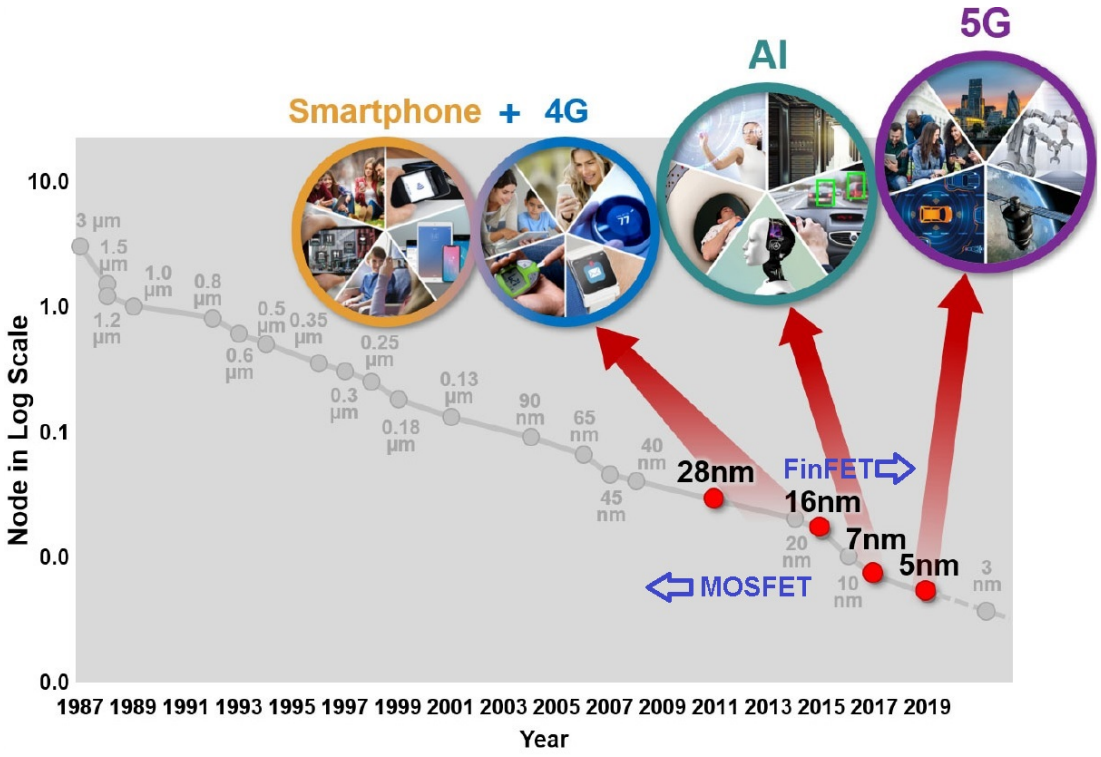

Figure 4.1: Scaling trend of semiconductor devices in TSMC foundry.

4.1 Analysis of CM Noise in 40 nm CMOS Technology

MOSFET devices have parasitic resistance and capacitance which affects the rising and falling time of the driver circuits, as presented in Chapter 3, Section 3.1. In the following sections, we will briefly discuss the parasitic resistances and capacitances in MOSFET devices and than analyse the CM noise in a CML driver circuit designed in 40 nm CMOS technology.

4.1.1 MOSFET Parasitic Resistances and Capacitances

The high-frequency parasitic model of a MOSFET is presented in [1]. Firstly, parasitic resistances at each terminal of the MOSFET are discussed. Afterwards, the parasitic capacitances are presented.

The performance of a MOSFET is affected by series resistance of the gate, drain, source and substrate regions if the circuit and layout is not carefully designed. The resistance model is shown in Figure 4.2. The equation of gate resistance (R_G) is given by

$$\begin{aligned} R_G &= R_{poly} + R_{ch}, \\ R_{poly} &= \frac{1}{3}\rho\frac{W}{n^2 L}, \\ R_{ch} &= \frac{1}{\delta}\frac{V_{DS}}{I_{DS}} || \frac{qL}{KT\mu W C_{ox}}, \end{aligned} \tag{4.1}$$

where ρ is resistivity, n is number of fingers, W is transistor width, L is transistor length, V_{DS} is voltage across drain-source terminal, I_{DS} is drain current, q is charge, K is the Boltzmann constant of value $1.38 \times 10^{-}23$, T is temperature in kelvin, μ is charge mobility and C_{ox} is oxide capacitance. The layout should be carefully designed to reduce R_G. Thus, multi-finger transistors are used in the layout to reduce the gate resistance.

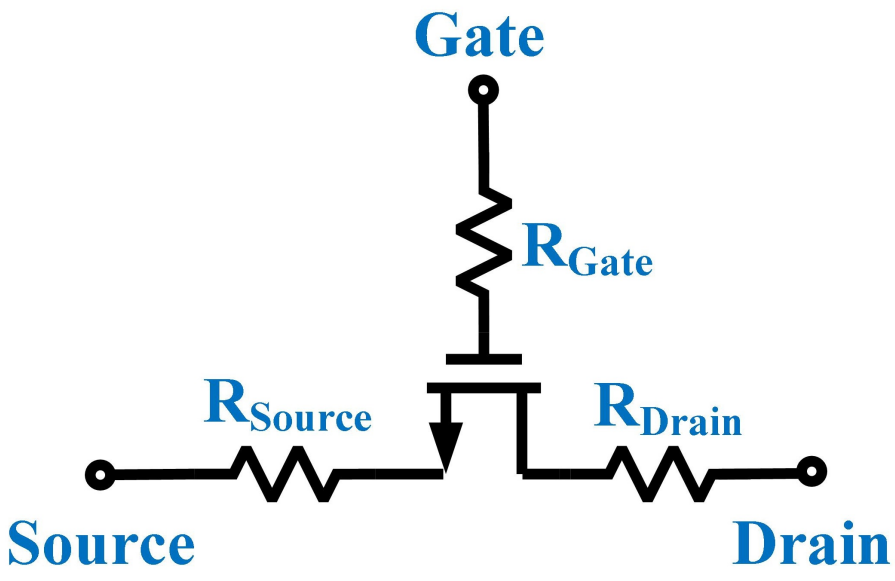

Figure 4.2: MOSFET resistance model.

The drain/source region resistance is calculated by

$$R_{S,D} = \frac{L_{S,D}}{W} R_{sq} + R_C, \tag{4.2}$$

where $L_{S,D}$ is the length of the drain/source region, W is the width of the transistor, R_{sq} is the sheet resistance and R_C is contact resistance, as presented in Figure 4.3. The value of $R_{S,D}$ reduces with an increase in the width of the transistors, and contact resistance can be minimized by using multiple contacts. Sheet resistance can be minimized by silicidation and using wider transistors in the design.

MOSFET devices have three main parasitic capacitances, which affect the high-frequency response. These are structure capacitance, channel capacitance and junction capacitance. The junction and channel capacitances are non-linear and depend on the operating region of the MOS devices whereas the structure capacitance is linear and has a fixed value. The details of each of the capacitances are discussed below.

The structure capacitance is due to the basic MOS structure and remains the same in all operating regions of the MOS device. The gate of the MOSFET is isolated from the channel by a SiO_2 layer having unit capacitance Cox, which

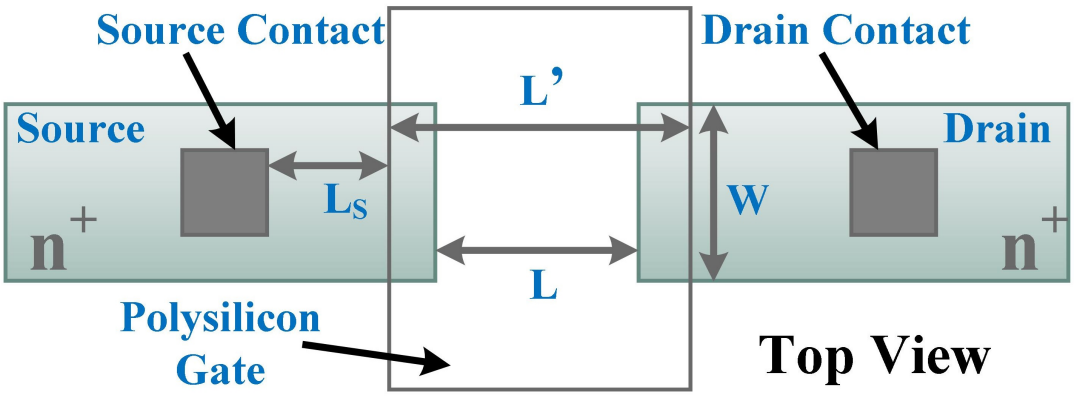

Figure 4.3: Top view of MOSFET device.

is given by

$$C_{ox} = \frac{e_{ox}}{t_{ox}}, \tag{4.3}$$

where e_{ox} is the permitivity of silicon oxide and t_{ox} is oxide thickness. The value of C_{ox} depends on the fabrication parameters and designers do not have control of this value. The total capacitance is called the gate capacitance C_g, which consists of two components. One is due to the channel and the other is from the structure of the transistor. Practically, in the lithography process the source and drain diffusion layers penetrate below the gate oxide layer by a specific amount, x_d, due to lateral diffusion. This phenomenon causes a parasitic capacitance between the gate and source/drain terminal known as overlap capacitance, as depicted in Figure 4.4. This is a linear capacitance having a fixed value that depends only

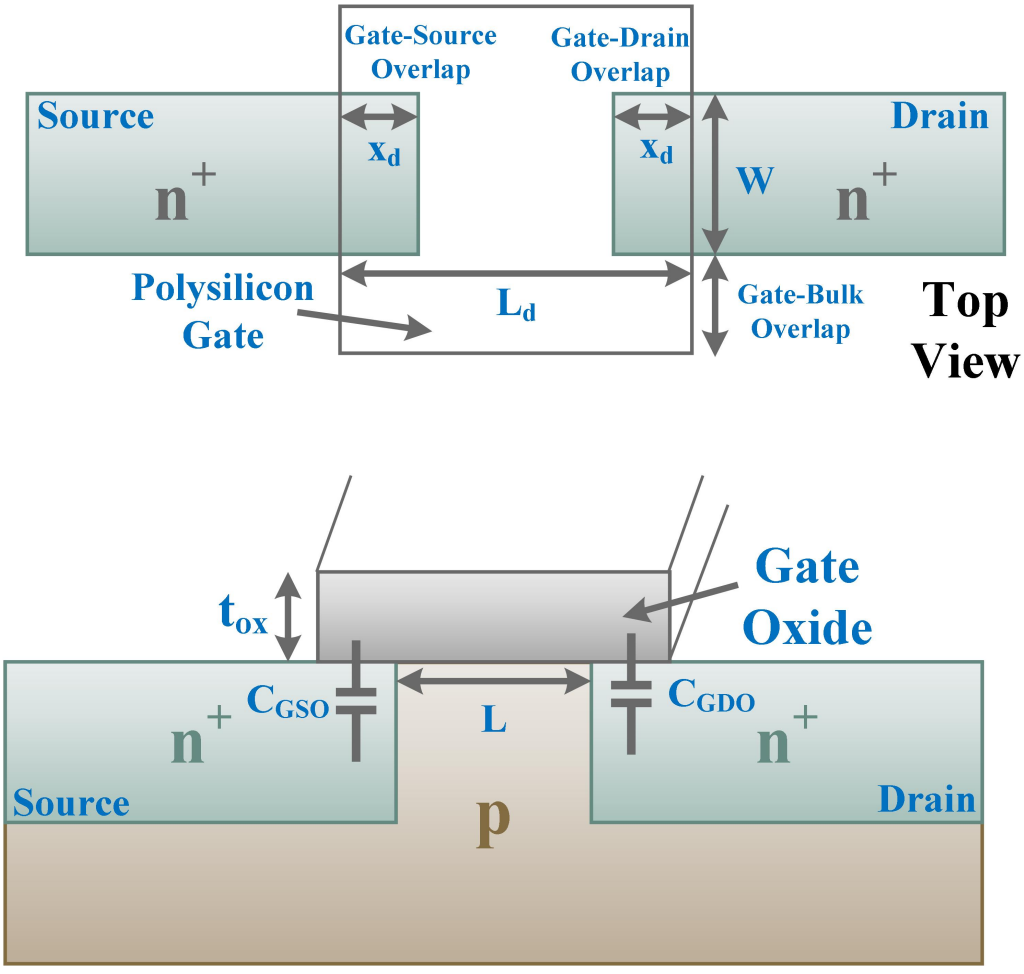

Figure 4.4: Structure capacitance of MOSFET due to lateral diffusion.

on the fabrication process. The value of this capacitance is calculated by

$$C_{GSO} = C_{GDO} = C_{ox}\ x_d\ W = C_o W, \tag{4.4}$$

where C_{ox} is given by equation (4.3), W is the width of the transistor, x_d is a technology-dependent parameter, and C_o is the overlap capacitance per unit width of the transistor. The value of the overlap capacitance increases with the width of the transistors.

The channel capacitance is called the gate channel capacitance C_{GC}, and is divided into three components: gate-channel source capacitance (C_{GCS}), gate-channel drain capacitance (C_{GCD}) and gate-channel bulk capacitance (C_{GCB}). These capacitances vary with the operating region and applied voltage of the transistor. The dependency of the gate channel capacitance on the applied voltage is presented in Figure 4.5. When the MOSFET is in the cutoff region, all the $C_{GC} = C_{GCB}$, and both C_{GCS} and C_{GCD} are equal to zero because the channel does not exist in this state. In the linear region where an inversion layer is formed, the $C_{GCB} = 0$ and C_{GC} are equally divided between C_{GCS} and C_{GCD}. When the MOSFET is in the saturation region, the $C_{GC} = C_{GCS}$ and both C_{GCB} and C_{GCD} are equal to zero because of the pinched off channel.

The junction capacitance is caused by the depletion region, which is created

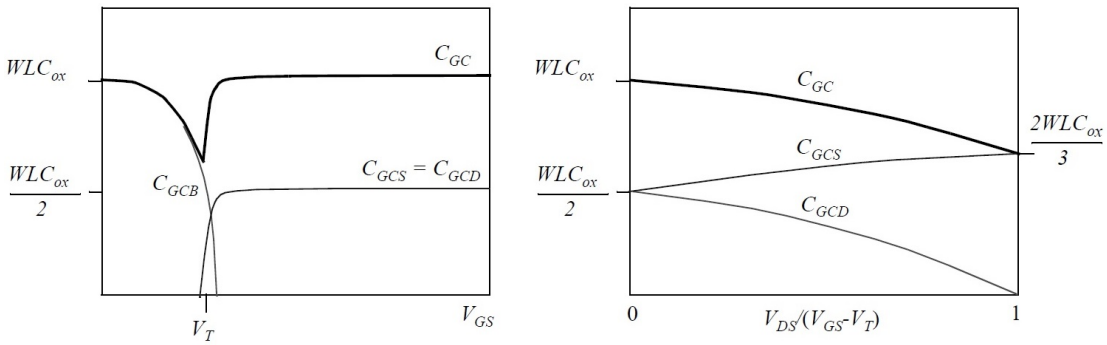

Figure 4.5: Dependency of channel capacitance due to operating region and applied voltage [2].

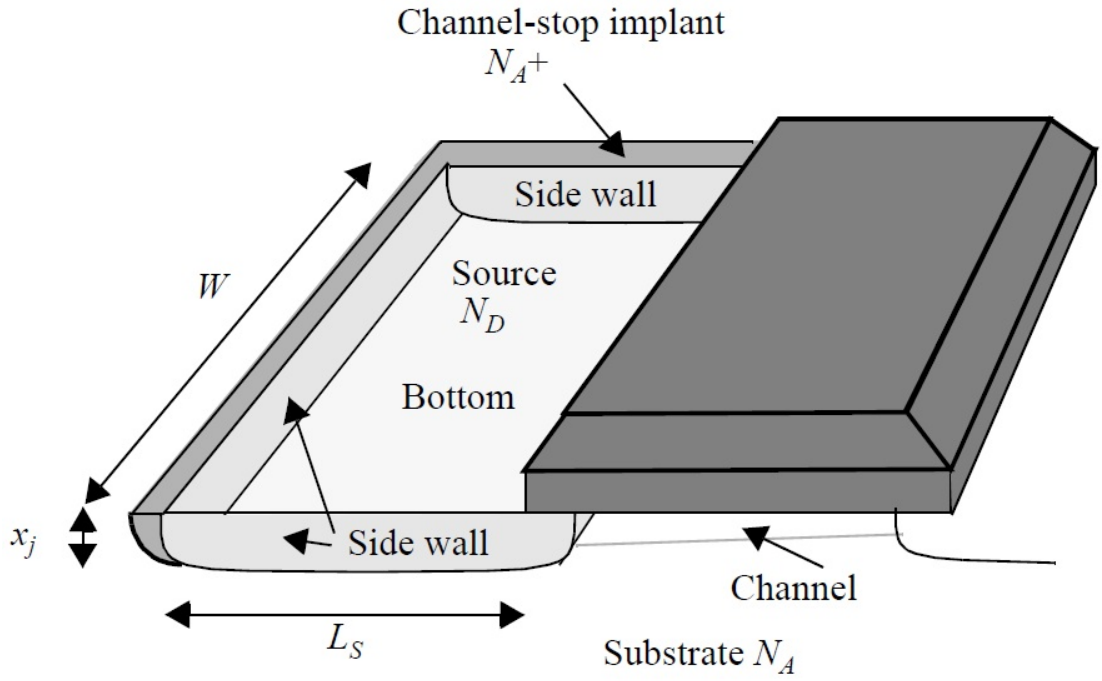

Figure 4.6: Junction (bottom-plate and side-wall) capacitance of MOSFET due to reverse bias pn-junction between source/drain and substrate [1].

due to the reverse-bias pn-junctions between the source/drain and substrate. It is a non-linear capacitance, and its value decreases with an increase in the reverse bias voltage. The junction capacitance consists of two components: bottom plate capacitance and side-wall capacitance, as shown in Figure 4.6.

The bottom plate capacitance is formed between the source region and substrate region with normal doping levels of N_D and N_A respectively. It is determined by the following equation:

$$C_{bottom} = C_j \; W \; L_s, \tag{4.5}$$

where C_j is given as

$$C_j = \frac{C_{j0}}{(1 - \frac{V_D}{\phi_o})^m}, \tag{4.6}$$

where C_{j0} is the capacitance under a zero bias condition, V_D is voltage across the pn-junction, ϕ_o is the built-in potential, and m is the grading coefficient. The value of the bottom plate capacitance is directly proportional to the width and

length of the transistor.

The side-wall capacitance, meanwhile, is formed between the normally doped (N_D) source region and channel-stop implant having a high doping level of N_A^+, which results in it being larger than the bottom plate capacitance. The value of the side-wall capacitance is given as

$$C_{sw} = C_{jsw}\ (W + 2 \times L_s), \tag{4.7}$$

where C_{jsw} is equal to $x_j \times C'_{jsw}$, called the capacitance per unit perimeter, x_j is junction depth, and W and L_s are the lengths of the side-walls, as depicted in Figure 4.6. The value of the side-wall capacitance is also directly proportional to the width and length of the transistor.

The total junction capacitance is calculated by adding the bottom-plate (C_{bottom}) and side-wall (C_{sw}) capacitance. The equation for total junction capacitance, also known as diffusion capacitance (C_{diff}), is given by

$$C_{diff} = C_{bottom} + C_{sw} = C_j \times\ L_s\ W + C_{jsw} \times (W + 2\ L_s). \tag{4.8}$$

In all, there are five different capacitances, as shown in Figure 4.7. Mathematically, these are given as

$$\begin{aligned} C_{GS} &= C_{GCS} + C_{GSO}, \\ C_{GD} &= C_{GCD} + C_{GDO}, \\ C_{GB} &= C_{GCB}, \\ C_{SB} &= C_{Sdiff}, \\ C_{DB} &= C_{Ddiff}. \end{aligned} \tag{4.9}$$

These capacitances can be determined by equations (4.4) to (4.8), given earlier in this section.

The overall variation of MOSFET capacitance with gate-source voltage is

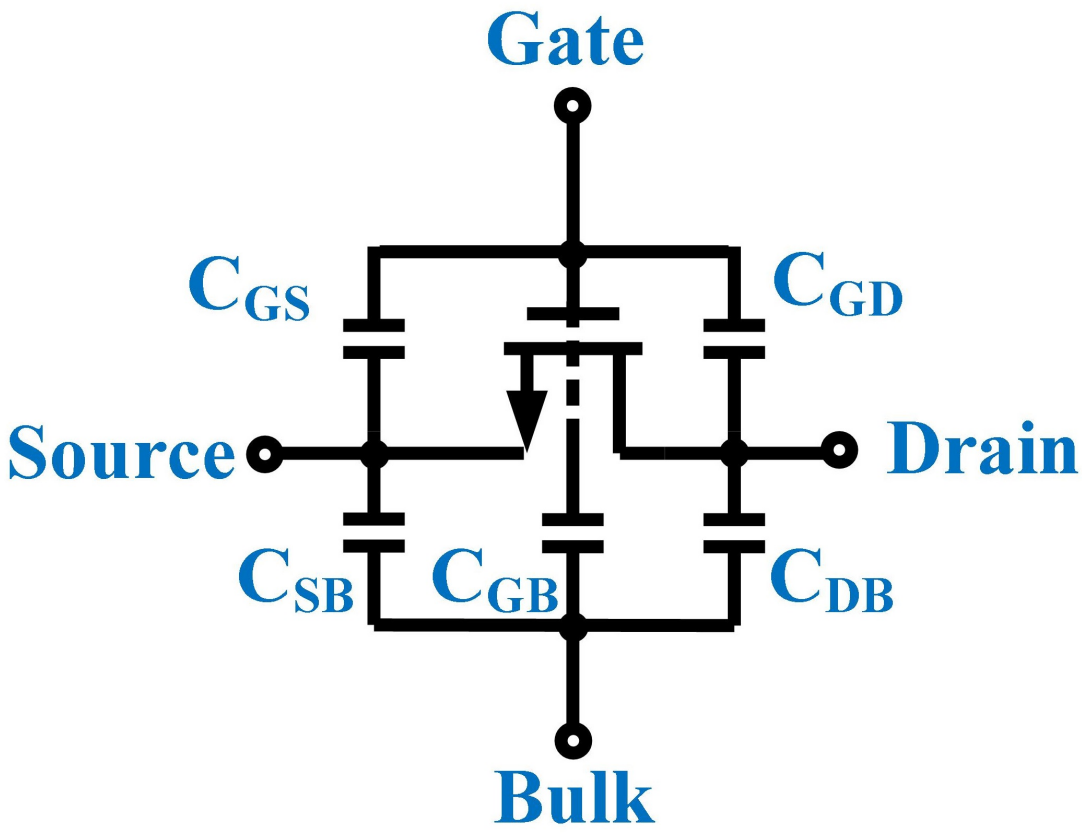

Figure 4.7: MOSFET capacitance model.

presented in Figure 4.8. It is observed that C_{GD} remains at the value of WC_{ox} in the cutoff and saturation regions, and its value increases to $WLC_{ox}/2+WC_{ox}$ in the triode region. The value of C_{GS} is the same as C_{GD} in the cutoff and triode regions, and its value increases to $2/3WLC_{ox}+WC_{ox}$ in the saturation region.

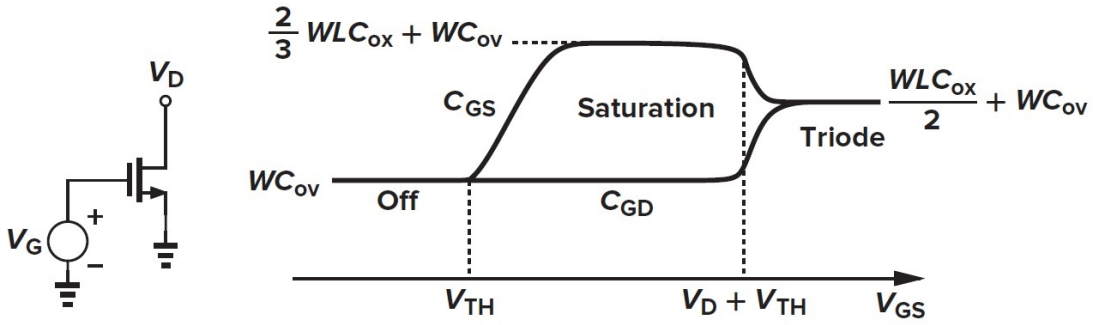

Figure 4.8: MOSFET gate-source and gate-drain capacitance variation with gate-source voltage [3].

A high-frequency parasitic model that includes the parasitic resistances and capacitances discussed above is depicted in Figure 4.9.

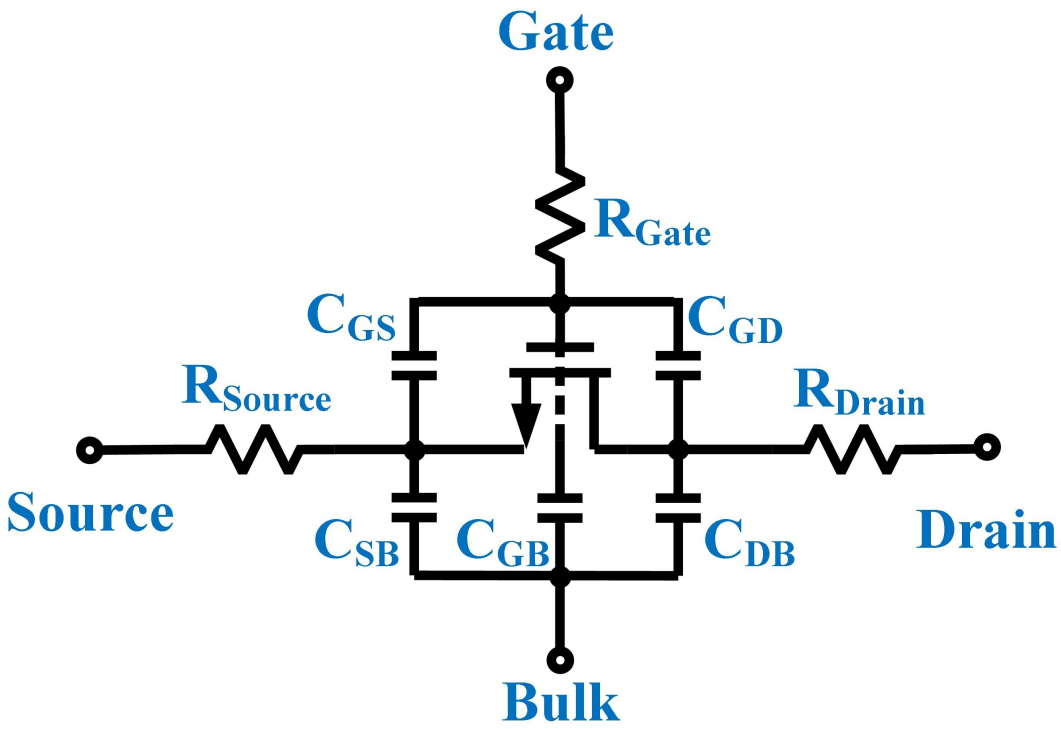

Figure 4.9: High-frequency MOSFET parasitic model.

4.1.2 Effect of MOSFET Parasitics on CM Noise in CML Driver

The CM noise depends upon the mismatch between the rising and falling edge at the output of the transmitter, as presented in Chapter 3. A CML driver circuit with output parasitics in 40 nm CMOS technology is shown in Figure 4.10. The rising/falling time depends on the output resistance and capacitance values, as given in equations (3.1) and (3.2). The output capacitance of the CML driver in 40 nm CMOS technology can be determined by the following equation:

$$C_P = C_{GD} + C_{DB}, \tag{4.10}$$

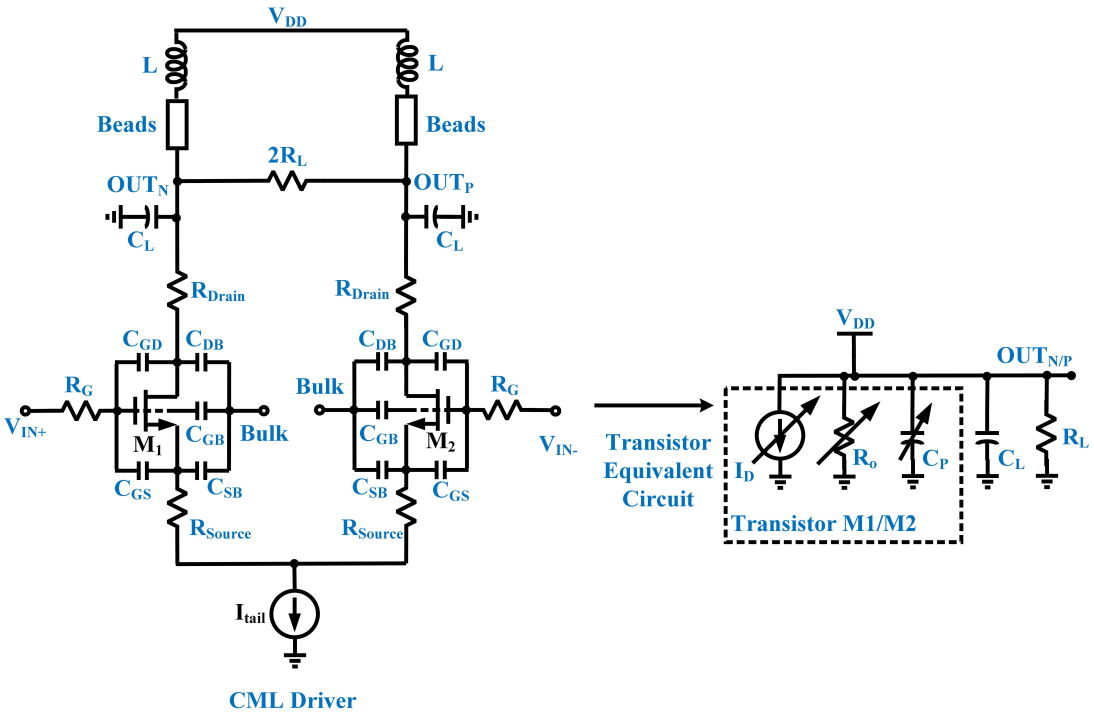

Figure 4.10: CML driver designed in 40 nm MOSFET technology with parasitics.

where C_{GD} is gate-to-drain capacitance, and C_{DB} is drain-to-bulk capacitance, as given by equation (4.9). The C_{GD} consists of gate-to-drain overlap capacitance having a fixed value, depending only on the fabrication process, as well as gate-channel drain capacitance, depending on the operating region of the MOSFET, as depicted in Figure 4.5. The C_{DB} is a structural capacitance, which depends on the structure of the MOSFET, as discussed in Section 4.1.

The output resistance of the CML driver at the output is calculated as

$$R_0 = R_{out}||R_L = (R_{Drain} + R_{Source})||R_L, \tag{4.11}$$

where R_L is the 25 ohm load resistance, R_{Drain} is the drain resistance and R_{Source} is the source resistance given by equation (4.2).

4.2 Analysis of CM Noise in 14nm FinFET Technology

The FinFET is a three dimensional device having vertical drain and source fins. The gate in a FinFET is wrapped around the source and drain, as shown in Figure 4.11, which results in better electrostatic control over the channel and low leakage current. In this section, we will briefly discuss the parasitic resistances and capacitances in FinFET devices.

4.2.1 FinFET Parasitic Resistances and Capacitances

The mathematical analysis of the parasitic resistances and capacitances of a FinFET are presented in [4]. Below, a discussion of the parasitic resistances in a FinFET device is given, followed by a discussion of parasitic capacitances.

FinFETs consist of three resistances: gate, drain and source resistance, as presented in Figure 4.12. The gate resistance further consists of two components: distributed gate electrode resistance $R_{g,eltd}$ and distributed channel resistance

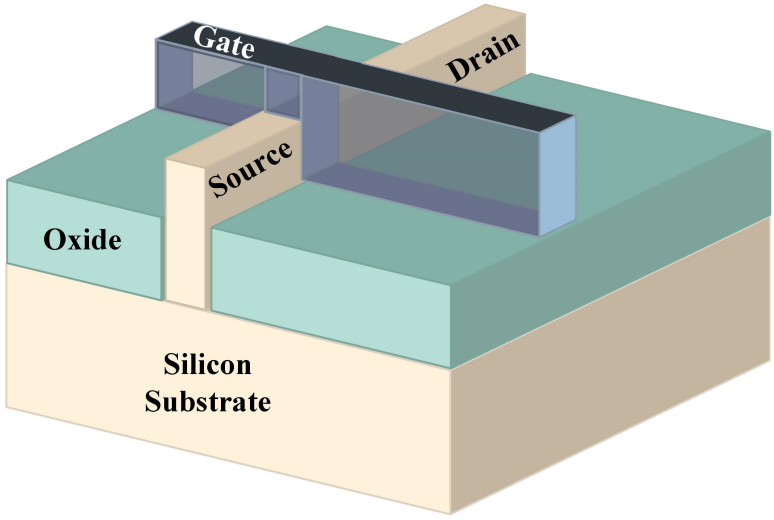

Figure 4.11: Structure of FinFET.

R_{ch}. Mathematically, this is given by

$$\begin{aligned} R_{g,eff} &= R_{g,eltd} + R_{ch}, \\ R_{g,eltd} &= \rho_{sh,geltd}\frac{W_{eff}}{L_{eff}}\alpha_g + \beta_g, \\ R_{ch} &= \gamma\frac{1}{R_{st}} + \frac{1}{R_{ed}}, \end{aligned} \tag{4.12}$$

where $\rho_{sh,geltd}$ is the gate electrode sheet resistance, β_g is the external gate resistance, R_{st} is the static channel resistance and R_{ed} is the excess-diffusion channel resistance and γ accounts for the distributed nature of the channel resistance.

The drain and source resistances consist of three components: contact resistance R_{con}, spreading resistance R_{sp} and extension resistance R_{sde}, as depicted in Figure 4.13.

R_{con} is the total contact resistance between the bulk raised source-drain (RSD) region and silicon-silicide region. It is determined by the following

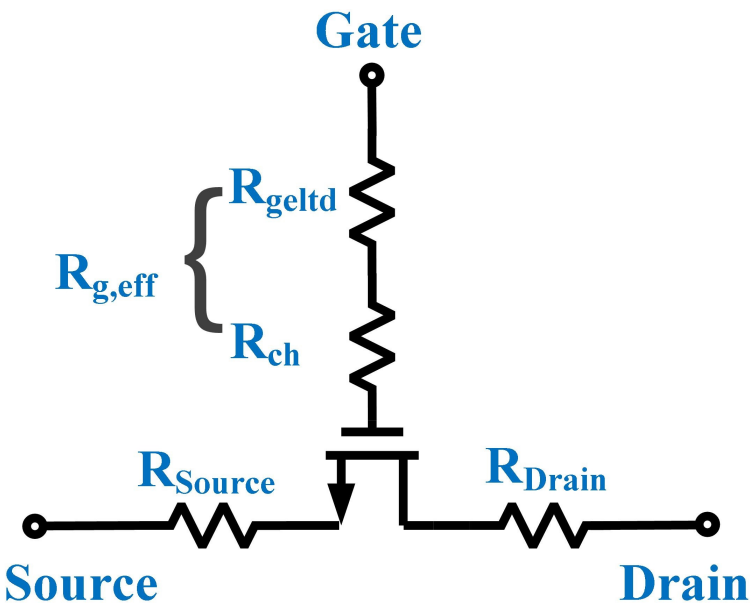

Figure 4.12: FinFET parasitic resistance model.

equation:

$$R_{con} = \rho . \frac{L_T}{A_{rsd,total}} . coth(\alpha), \tag{4.13}$$

where ρ is resistivity of the RSD region, L_T is total length, $A_{rsd,total}$ is the area of the RSD region and α is the ratio of the length of the RSD region to the total length L_{rsd}/L_T.

The R_{sp} is created because of the current crowding or spreading from the thin source-drain extension (SDE)-fin into the large RSD region. Mathematically, it is calculated by

$$R^2_{sp,real} = \frac{\rho cot\theta}{s} \left(\frac{1}{\sqrt{A_{fin}}} \frac{1}{\sqrt{A_{rsd}}} \right), \tag{4.14}$$

where s is the SDE and RSD shaping parameter, A_{fin} is the area of the SDE-fin and A_{rsd} is the area of the RSD region.

The R_{sde} is a resistance in the thin SDE-fin region under the spacer and

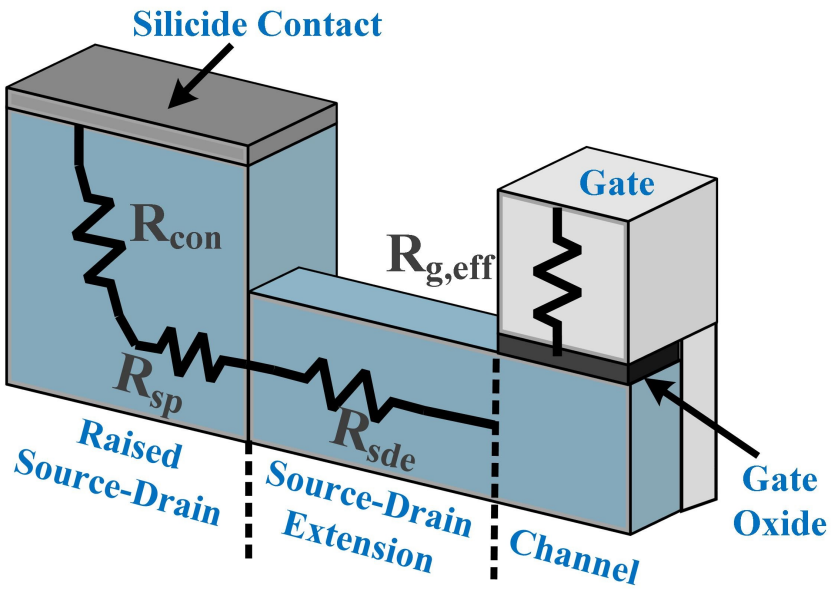

Figure 4.13: FinFET drain/source resistance.

depends on biasing. The equation to determine this resistance is

$$R_{sde}(S/D) = \frac{R_{S1/D1}}{1 + R_{S2/D2} \times (V_{gs/d} - V_{fbsd}))} + R_{S3}, \tag{4.15}$$

where V_{fbsd} is the flat band gate voltage of a SiO_2 MOS system and R_{S1}, R_{S2}, R_{S3}, R_{D1}, R_{D2}, and R_{D3} are determined by the measurement data of the required technology and calculated as

$$\begin{aligned} R_{S1} = R_{D1} &= \frac{R_{sde10}}{H_{fin} \times t_{fin}}, \\ R_{S2} = R_{D2} &= \frac{R_{sde10}}{R_{acc0} \times t_{fin}}, \\ R_{S3} = R_{D3} &= \frac{R_{sde20}(L_{sp} - \Delta L_{sde})}{H_{fin} \times t_{fin}}, \end{aligned} \tag{4.16}$$

where R_{sde10} depends on the distribution of the doping concentration in the SDE region, H_{fin} is the height of the fin, t_{fin} is the thickness of the fin, R_{acc0} is a technology-dependent parameter of accumulation resistance calculated by $\frac{l_{acc}}{\mu_{eff} \times C_{acc}}$, R_{sde20} is the technology-dependent constant defined as $\frac{1}{qn\mu}$, L_{sp} is the spacer length and L_{sp}-ΔL_{sde} is the effective length of the uniformly doped RSD region.

The FinFET parasitic capacitance consist of two components: overlap capacitance C_{ov} and fringing capacitance C_{fr}, as shown in Figure 4.15. The total parasitic capacitance is given by

$$C_p = C_{ov} + C_{fr}. \tag{4.17}$$

The C_{ov} is because of overlap between the gate and SDE region. The gate source/drain overlap capacitance is determined by

$$C_{ov} = C_{GSO} = C_{GDO} = 2C_{ox}H_{fin}l_{ov}, \tag{4.18}$$

where C_{ox} is oxide capacitance, H_{fin} is fin height and l_{ov} is the overlap distance. The detailed mathematical analysis is presented in [5].

The C_{fr} is created because of the proximity of different structural components of the FinFET, and consists of two components: fin-to-gate capacitance C_{fg} and source-drain contact to gate capacitance C_{cg}, as depicted in Figure 4.14. The C_{fg} is given by

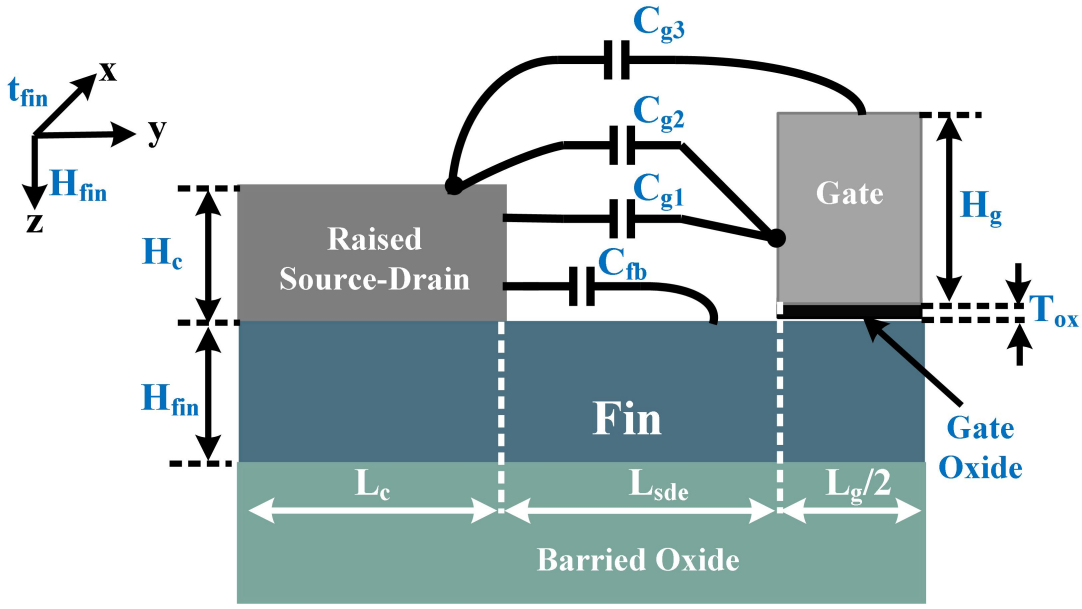

Figure 4.14: FinFET fringing capacitance.

$$C_{fg} = H_{fin}\left[C_{fg,sat} - \frac{1}{2}\left((C_{fg,sat} - C_{fg,log} - \delta) + \sqrt{(C_{fg,sat} - C_{fg,log} - \delta)^2 + 4C_{fg,sat}\delta}\right)\right], \tag{4.19}$$

where δ defines the transition from $C_{fg,sat}$ to $C_{fg,log}$, and the value of parameters $C_{fg,sat}$ and $C_{fg,log}$ depends on H_g, T_{ox}, L_{sde}, H_c, L_c and the dielectric constant of the source/drain spacer. The mathematical analysis for the fringing capacitance is presented in [6]. The gate-to-contact fringing capacitance is calculated by

$$C_{cg} = H_{fin} \times (C_{cg1} + C_{cg2} + C_{cg3}), \tag{4.20}$$

where C_{cg1} is the parallel plate capacitance between the gate and contact, C_{cg2} is the capacitance generated because of the electric field originating from the gate and terminates on top of the contact and C_{cg3} is created because of the electric field originating from the top of the gate and terminating on top of the contact. These three gate-to-contact fringing capacitances are shown in Figure 4.14.

The above analysis shows that the fringing capacitance consists of three components: one top, two side and two corner capacitances. For a multifin FinFET device, the total fringing capacitance is given by

$$C_{cg} = N_{fin} \times (2C_{corner} + 2C_{side} + C_{top}), \tag{4.21}$$

where N_{fin} is the number of fins.

A parasitic FinFET model with all the parasitic resistances and capacitances discussed above is depicted in Figure 4.15.

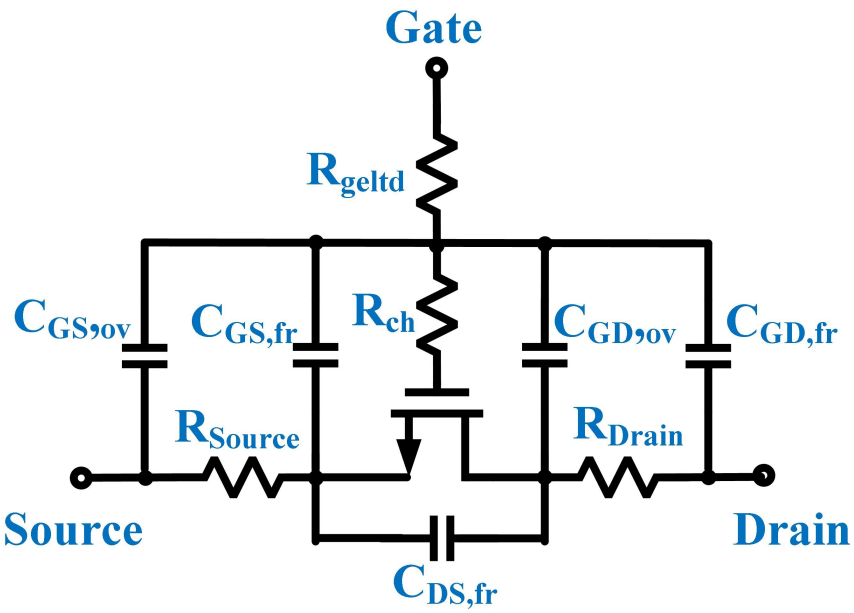

Figure 4.15: FinFET parasitic resistances and capacitances.

4.2.2 Effect of FinFET Parasitics on CM Noise in CML Driver

A CML driver circuit with parasitics in 14 nm FinFET technology is shown in Figure 4.16. The rising/falling time depends on the output resistance and capacitance values, as given in equation (3.1) and (3.2). The output capacitance of the CML driver in 14 nm FinFET technology can be determined

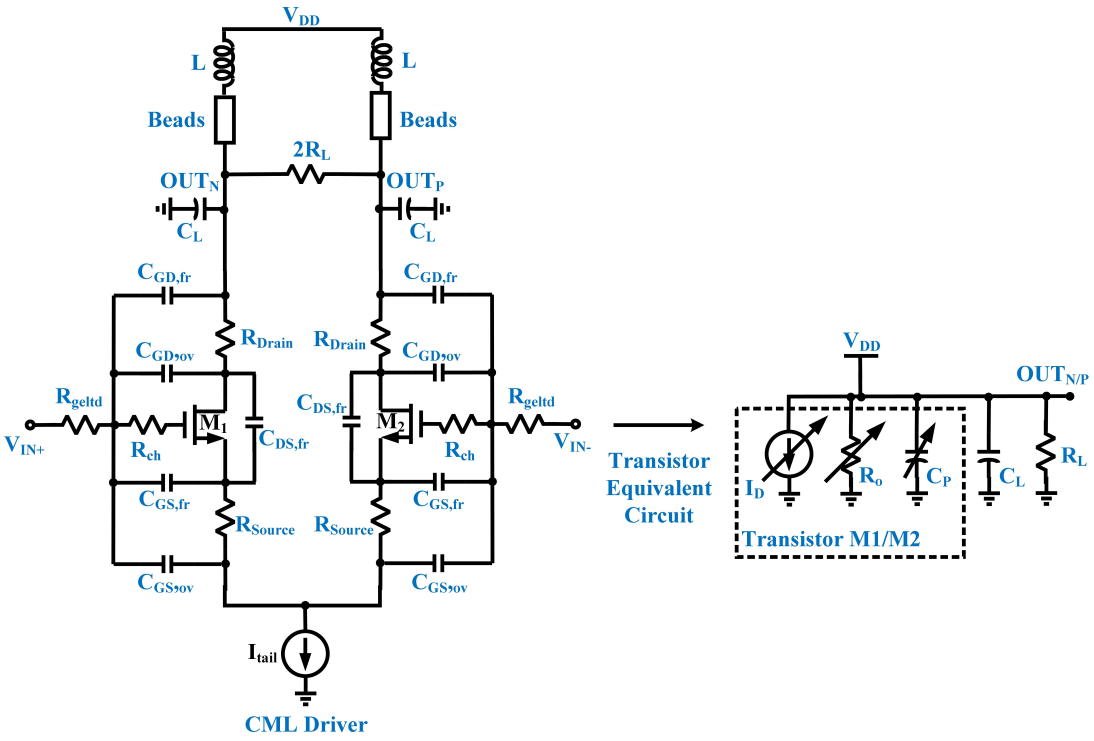

Figure 4.16: CML driver designed in 14 nm FinFET technology with parasitics.

by the following equation:

$$C_P = C_{GD,fr} + C_{GD,ov} + C_{DS,fr}, \tag{4.22}$$

where $C_{GD,fr}$ is the gate-to-drain fringing capacitance, as given by equation (4.21), $C_{GD,ov}$ is the gate-to-drain overlap capacitance, as given by equation (4.18), and $C_{DS,fr}$ is the drain-to-source fringing capacitance, as given by equation (4.21).

The output resistance of the CML driver at the output is calculated by

$$R_0 = R_{out}||R_L = (R_{Drain} + R_{Source})||R_L. \tag{4.23}$$

4.2.3 Simulation Results and Discussion

The values of the parasitic resistance and capacitance at the output terminal of the CML driver circuit depend on the technology used in the design. The test bench shown in Figure 4.17 is used to analyze the effect of technology scaling on the CM noise in the optical transmitter. It is similar to the test bench utilized in Chapter 3, Section 3.1.1. The CML driver is designed in both 40 nm CMOS and 14 nm FinFET technology, and these are simulated one after the other. The input data signal has an amplitude of 100 mV, rise time of 20 ps, and fall time of 10 ps with a data rate of 56 Gbps, and the laser is biased at 60 mA. The transient PAM-4 P-/N- path signal and CM noise spectrum at the output of the transmitter is presented in Figure 4.18 and 4.19. The CM noise in the 40 nm CMOS technology is 63 dBuV, while in the 14 nm FinFET technology it is 58.6 dBuV because the parasitic capacitance in this technology is lower due to the smaller sizing of the transistor. However, it is expected that the advance technology node should have higher CM noise because smaller sizes may result in higher asymmetry in the differential pair of driver circuit. The Monte-Carlo analysis should be performed to analyze the effect of asymmetry in differential pair on CM noise. Hence, before concluding the effect of technology scaling on CM noise, more analysis needs to be done. The optical eye performance is also better in the 14 nm FinFET technology as compared to the 40 nm MOSFET

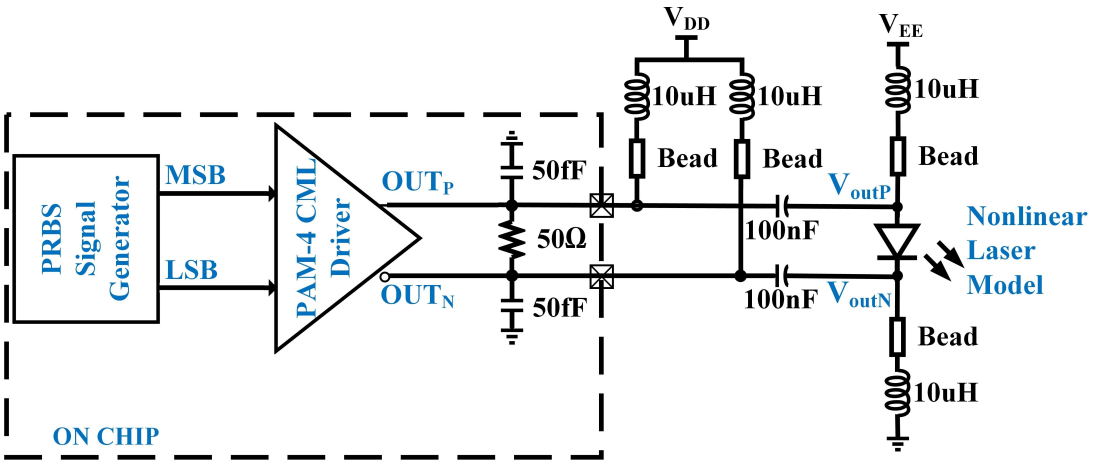

Figure 4.17: Test bench to simulate the CM noise in the CML driver.

technology. The output optical eye is depicted in Figure 4.20. The top horizontal eye opening in 14 nm technology is 200 mV, and in 40 nm technology, it is 132 mV, which is 34% lower. This demonstrates that the advanced technology can achieve higher speeds, although both need equalization due to the laser and channel non-linearity.

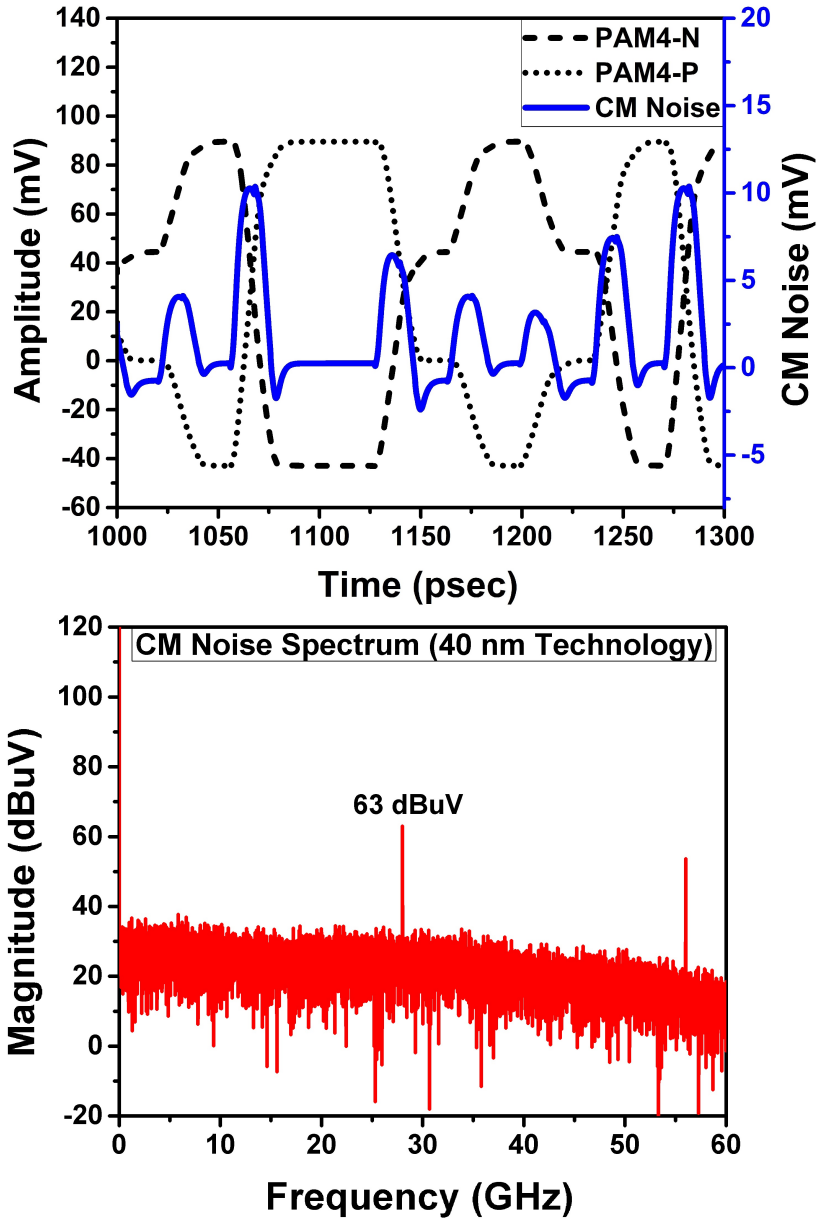

Figure 4.18: Simulation results in 40 nm CMOS technology, presenting transient PAM-4 N- and P-signal, CM noise signal, and spectrum of CM and DM signal at output of optical transmitter.

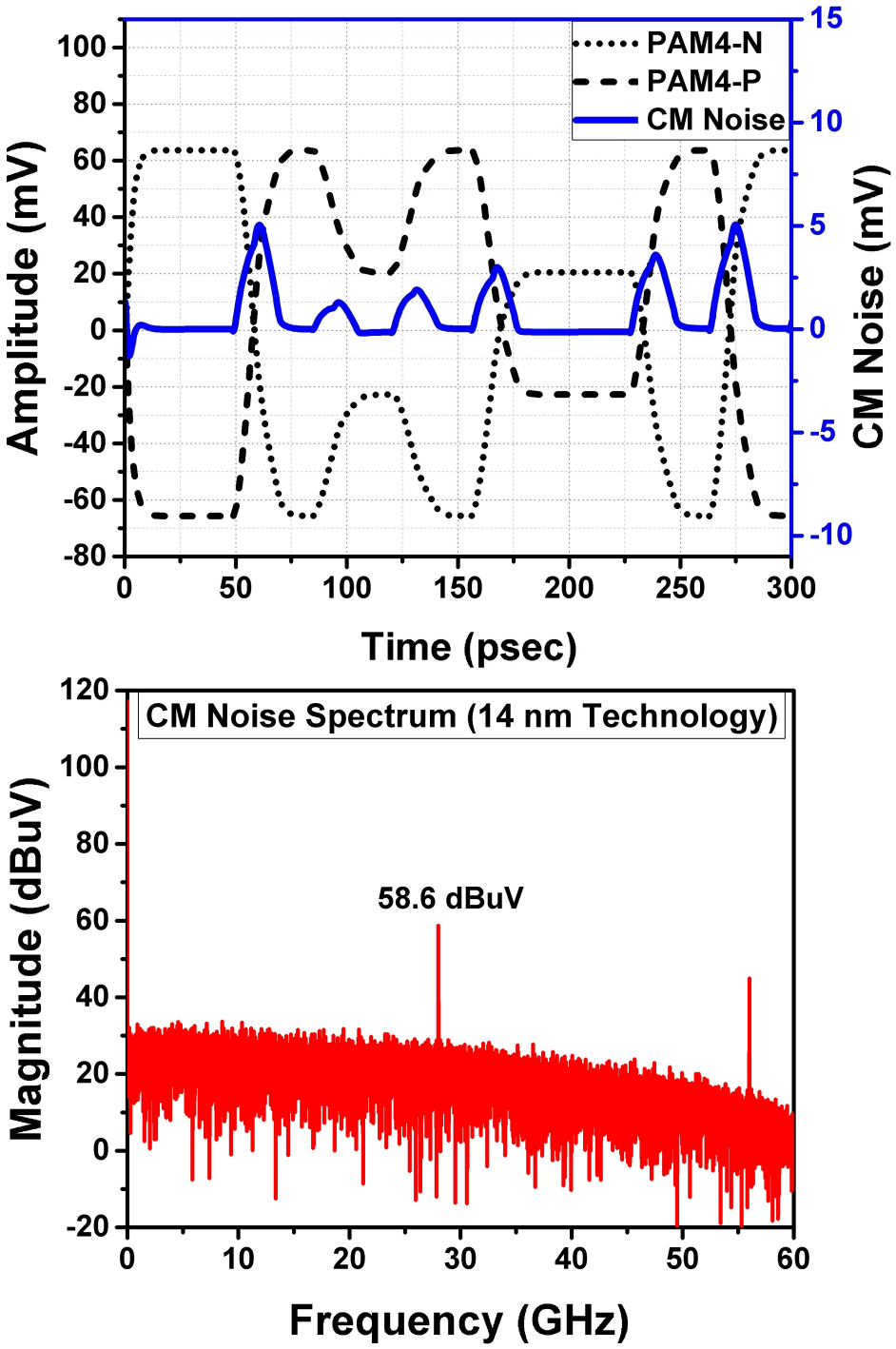

Figure 4.19: Simulation results in 14 nm FinFET technology, presenting transient PAM-4 N- and P-signal, CM noise signal, and CM noise spectrum at output of optical transmitter.

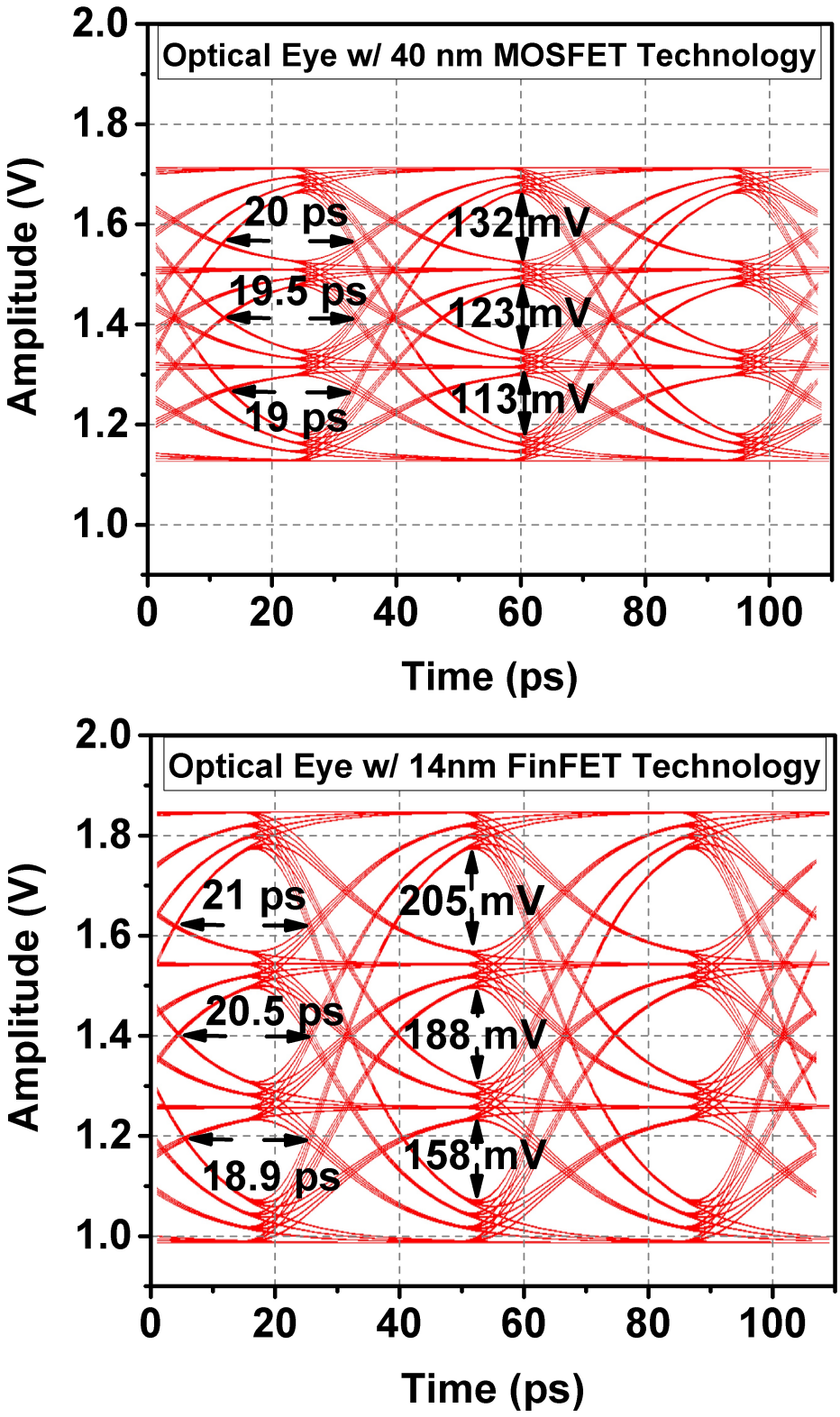

Figure 4.20: Comparison of optical eye in 14 nm and 40 nm technology.

4.3 Effect of Operating Frequency on CM Noise

The advanced technology nodes like 14 nm FinFET are used to support smaller sizes and higher data rates. The CM noise is affected by the speed of communication, and is inversely proportional to the data rate, as presented in equation (3.7) and repeated as follows:

$$N(2F_{Nyquist})_{CML} = \frac{1}{8} R_F Amp \frac{|t_{rise} - t_{fall}|}{T_b} sinc^2\left(\frac{\pi}{2}\frac{T_{tr}}{T_b}\right) \tag{4.24}$$

$$N(2F_{Nyquist})_{CML} \propto \frac{1}{T_b}, \tag{4.25}$$

where T_b is the data time period. The smaller the value of the data time period, the higher the CM noise. The test bench shown in Figure 4.17 is simulated with different PAM-4 data rates, and CM noise at the output of the transmitter is observed. It is noted that the CM noise increases with an increase in the data rate, as depicted in Figure 4.21, which validates the relationship presented in the

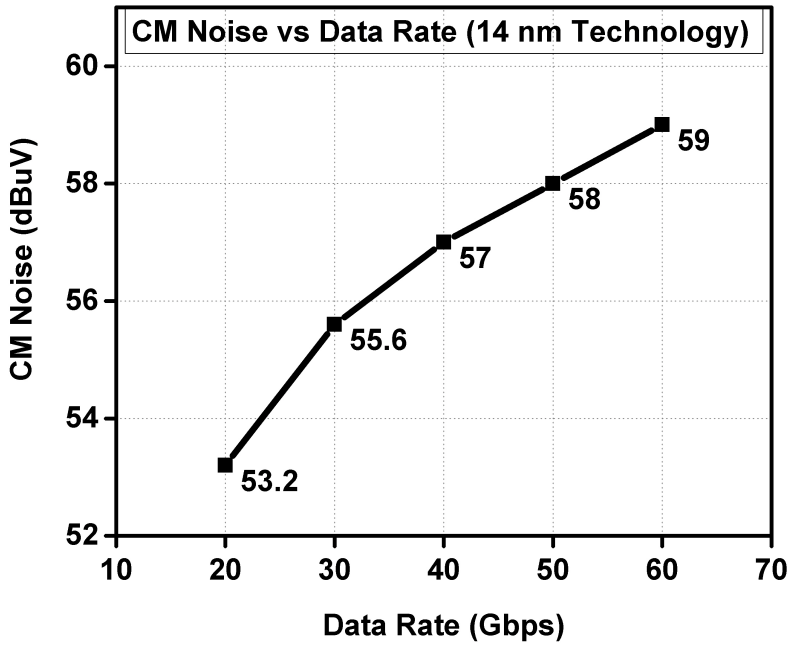

Figure 4.21: Effect of data rate on CM noise.

above mathematical equation (4.25). The higher data rates also require stronger equalization, which results in higher CM noise. This asserts the need for a CM noise cancellation circuit to meet the EMC standards prescribed by the FCC and CISPR, as the speed of communication is increasing day by day due to the introduction of advanced applications.

4.4 Summary

This chapter analyzed the parasitic resistances and capacitances in transistors in 40 nm CMOS and 14 nm FinFET technologies. A comparison between the CM noise generated in a CML driver circuit designed in both technologies is presented. It is demonstrated that technology scaling reduces the CM noise alongside the reduction in the sizes of the transistors. But before concluding the effect of technology scaling on CM noise, Monte-Carlo analysis should be performed, to see the effect of higher asymmetry of differential pair in the driver circuit in advance technology node. Moreover, advanced technology nodes are used to achieve higher data rates, which increases the CM noise significantly. This makes it more difficult for designers to meet EMC standards at higher data rates.

4.5 References

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Chapter 5

Automatic CM Noise Cancellation (CMNC) System

In this chapter, we first discuss our technique for canceling EMI-related CM noise, and then we present the design of an automatic CMNC circuit in 40 nm CMOS technology for a 56 Gbps PAM-4 optical transmitter.

5.1 Proposed PAM-4 CMNC Technique

EMI-related CM noise is generated due to the rise and fall time mismatch in the P-/N-signal path. Each source discussed in Chapter 3, increases the imbalance in the rise and fall time at the output of the transmitter, which increases the noise. CM noise in a PAM-4 transmitter is depicted in Figure 5.1 with positive peaks. It has three amplitudes due to the four levels used in PAM-4 modulation. To suppress this noise, another signal, called a CM cancellation (CMC) signal, is generated with the same PW and amplitude but the opposite direction [1], as demonstrated in Figure 5.2. The cancellation signal is determined by equation (5.1) and the resultant CM noise after

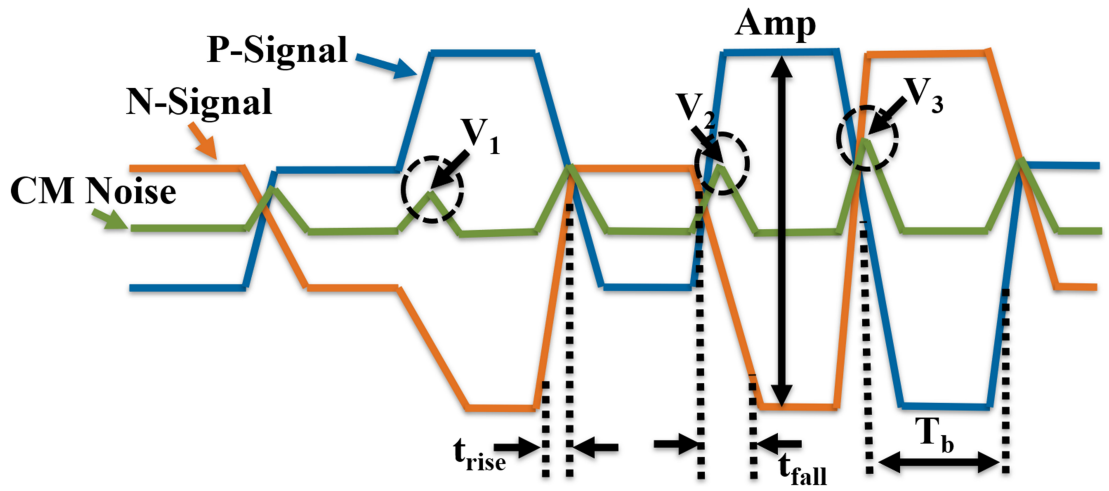

Figure 5.1: CM noise generation in PAM-4 transmitter due to rise and fall time mismatch in P- and N-signals [1]

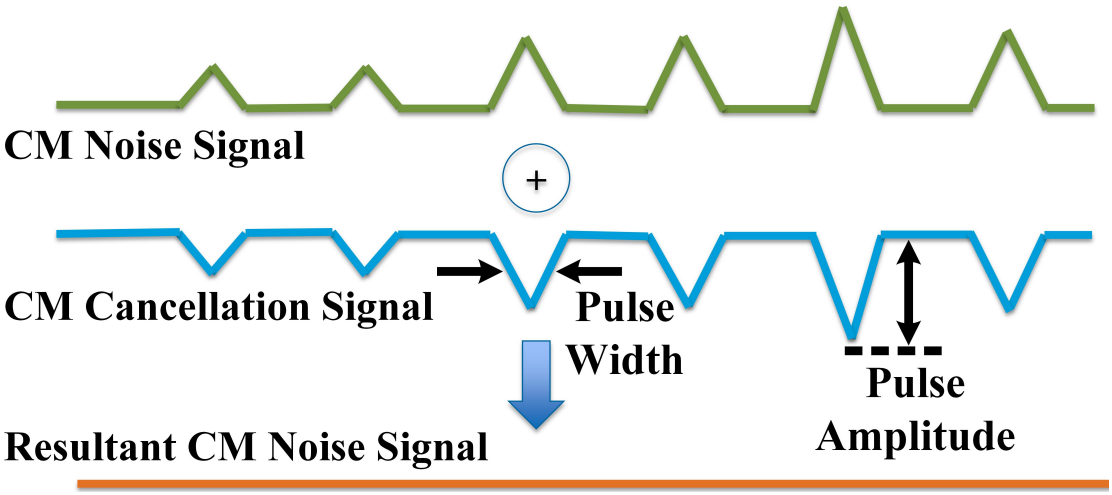

Figure 5.2: Suppression of PAM-4 CM noise with the proposed cancellation technique.

cancellation is calculated by equation (5.2):

$$NC(2F_{Nyquist}) = -\frac{A_{Comp}T_{Comp}}{T_0} sinc\left(\frac{T_{Comp}}{T_0}\right), \tag{5.1}$$

$$N(2F_{Nyquist})_{Total} = N(2F_{Nyquist})_{CML} + N(2F_{Nyquist})_{FFE} + NC(2F_{Nyquist}), \tag{5.2}$$

where A_{Comp} is the amplitude, T_{Comp} is the PW and T_0 is the time period of the cancellation pulses. When the CMC signal is added to the noise, ideally, the resultant output signal should not contain CM noise, as presented by the compensated CM noise signal in Figure 5.2. But, due to limitation in the control of the PW and height in the generated CMC signal, the noise is not canceled completely. Also, the skew in the cancellation signal can reduce the performance of this technique, which can be solved by using a re-timer circuit in the input data signal to compensate for the skew in the CM noise. Three parameters need to be detected for creation of the CMC signal: the time at which the cancellation signal should be generated and the width and height of the pulse.

As Figure 5.1 depicts, the CM noise is generated at every rising and falling edge of the input data signal, so the edge of the input data should be detected to create the CMC signal. After that, the width and height of the produced CMC pulse can be tuned to suppress the noise. It is also noted that the amplitude of the noise depends upon the switching of the PAM-4 signal between different levels. The noise amplitude is highest when a PAM-4 switches between 00 to 11 and minimum when it flips between two consecutive levels, e.g., 00 to 01, 01 to 10, or 10 to 11. To incorporate these switching variations, the CMC signal is generated based on the LSB and MSB of the input data signal.

A novel technique to minimize EMI-related CM noise is proposed here, and is presented in Figure 5.3. It consists of two main processes. The first is a pulse generation, in which the rising and falling edge of the input data signal

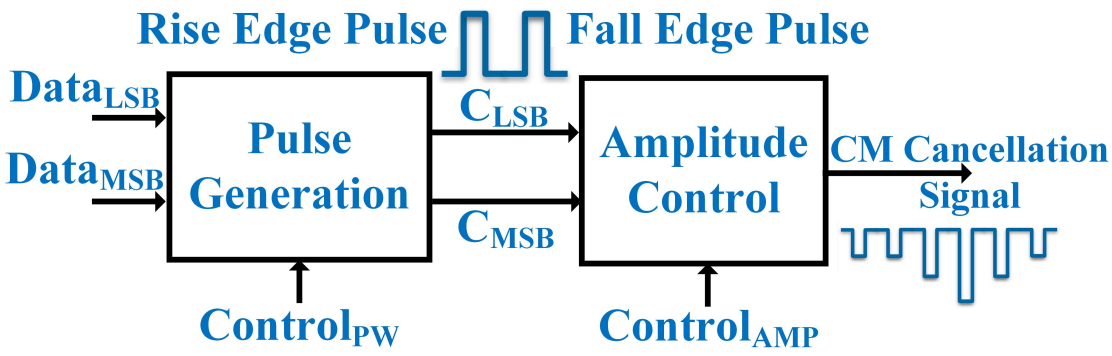

Figure 5.3: EMI-related CMNC module supporting PAM-4 signaling.

($Data_{LSB}$ and $Data_{MSB}$) are detected, and LSB and MSB cancellation pulses (C_{LSB} and C_{MSB}) are generated at each rising and falling edge of the input data signal. The width of the cancellation pulse is also controlled in this process by the $Control_{PW}$ signal. The phase of the cancellation signal does not change with the pulse width, as cancellation signal is generated at start of each edge of the input signal. The second process is amplitude control, in which the strength of the CMC signal is tuned to suppress EMI-related CM noise at the output of the transmitter by the $Control_{AMP}$ signal. The generated cancellation signal is connected to the transmitter output to suppress the cumulative CM noise generated from different sources.

5.2 Proposed PAM-4 Automatic CMNC System

A high-level flowchart of the PAM-4 automatic CMNC system is demonstrated in Figure 5.4. It comprises three processes: CM noise sensing, CM noise tuning and cancellation signal generation [1]. The CM noise sensing is performed by taking the average of the output signal at the transmitter and down-converting it to zero frequency. The value of the CM noise is extracted from this down-converted signal by measuring the direct current (DC) component. The CM noise value at the output of the transmitter is then compared with a preset threshold level. If the CM noise is lower than the prescribed limit, it ends the tuning. Otherwise, this CM noise value is utilized to generate a decision signal for the next process, the CM noise tuning. The tuning process is performed by a logic circuit which takes the decision signal from the CM noise sensing process and increases or decreases the amplitude and PW control signals. These control signals are then fed into the next process, the cancellation signal generation, which generates a cancellation signal according to the PW and amplitude control bits. Afterwards, the whole process repeats and keeps adjusting the PW and amplitude of the

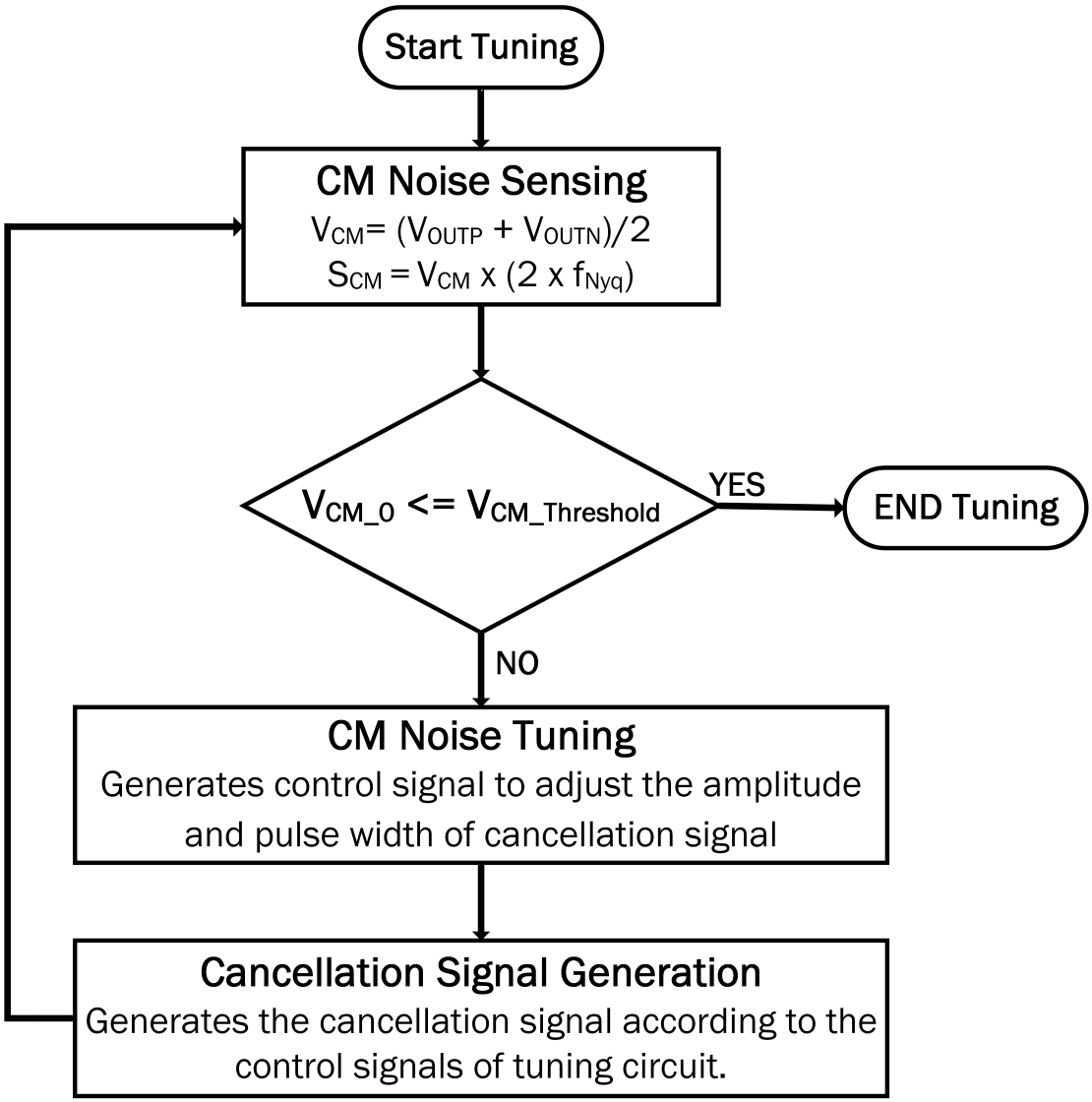

Figure 5.4: High-level flow chart of the PAM-4 automatic CMNC system.

cancellation signal to achieve the target CM noise level at the output of the transmitter.

The threshold CM current value is calculated using the following formula from [2]:

$$I_{CM_{th}} = \frac{r \times E_{CM}}{1.257 \times 10^{-}06 \times f \times L}, \tag{5.3}$$

where $I_{CM_{th}}$ is the threshold CM current, E_{CM} is the maximum radiated emission due to the CM current, f is the operating frequency, L is the length of the communication channel and r is the distance from the measurement point of the

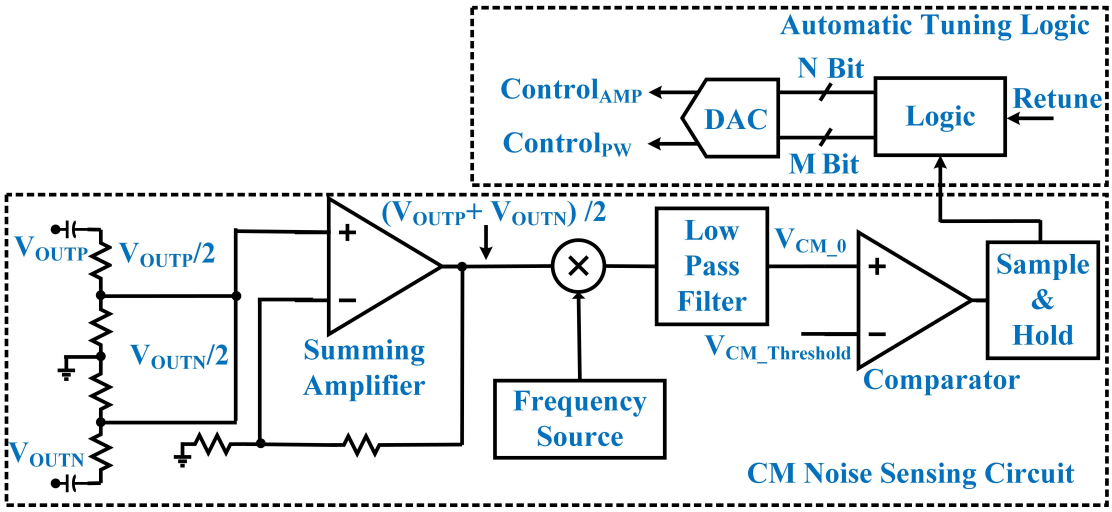

Figure 5.5: Behavioral implementation of the CM noise sensing and automatic tuning circuit.

EM emission. The laser model equivalent resistor is used to convert the $I_{CM_{th}}$ into $V_{CM_{th}}$.

5.2.1 CM Noise Sensing Circuit

The VerilogA behavioral implementation of the CM noise sensing circuit is shown in Figure 5.5. The CM noise sensing circuit consists of a summing amplifier to detect CM noise (V_{CM}) at the output of the transmitter by adding a P-signal (V_{OUTP}) and N-signal (V_{OUTN}), as calculated by

$$V_{CM} = \frac{(V_{OUTP} + V_{OUTN})}{2}. \tag{5.4}$$

A frequency mixer is used to down-convert the detected V_{CM} signal to zero frequency by multiplying it by a signal having a frequency of twice the Nyquist rate ($f_{Nyquist}$), as given by

$$S_{CM} = V_{CM} \times (2 \times f_{Nyquist}). \tag{5.5}$$

A low-pass filter is utilized to extract the DC component from the down-converted signal (S_{CM}). The extracted CM noise value (V_{CM_0}) is

compared to a preset or programmable threshold value ($V_{CM\_Threshold}$) to make a decision about the tuning of the cancellation signal PW and amplitude, and a sample and hold circuit is used to hold the sample for a cycle of conversion.

5.2.2 Automatic Tuning Logic

The VerilogA behavioral implementation of the automatic tuning logic is depicted in Figure 5.5. This circuit takes the decision signal generated by the sensing circuit and produces the PW and amplitude control signals ($Control_{AMP}$ and $Control_{PW}$) to tune the CMNC. The tuning is performed only once at the initial startup of the chip. However, retuning can be performed, if CM noise at the output of the transmitter changes due to aging of the circuit or any other factor. It comprises a logic circuit, which generates M- and N-bit control signals, and a DAC to convert this digital information into analog control voltages $Control_{AMP}$ and $Control_{PW}$.

A finite state machine (FSM) implementation of the logic circuit is presented in Figure 5.6. The FSM is designed in VerilogA. It starts from the initial state in which the initial values of the PW (M) and amplitude (N) control bits are set, and the CM noise level at the output of the transmitter detected by the CM noise sensing circuit is compared with the preset or programmable threshold CM noise value. If the CM noise level at the output of the transmitter is below this threshold value, then the automatic tuning logic ends the tuning as indicated by the FSM. If the level of the CM noise is greater than the required threshold value, then the automatic tuning circuit goes to the next state to increase the amplitude of the cancellation signal until the CM noise level at the output of the transmitter is below the threshold value or the amplitude control signal ($Control_{AMP}$) reaches its maximum value (2^N). If the CM noise level at the output of the transmitter is above the preset or programmable threshold value and the $Control_{AMP}$ reaches its maximum value, then the automatic tuning logic goes into the next state to adjust the

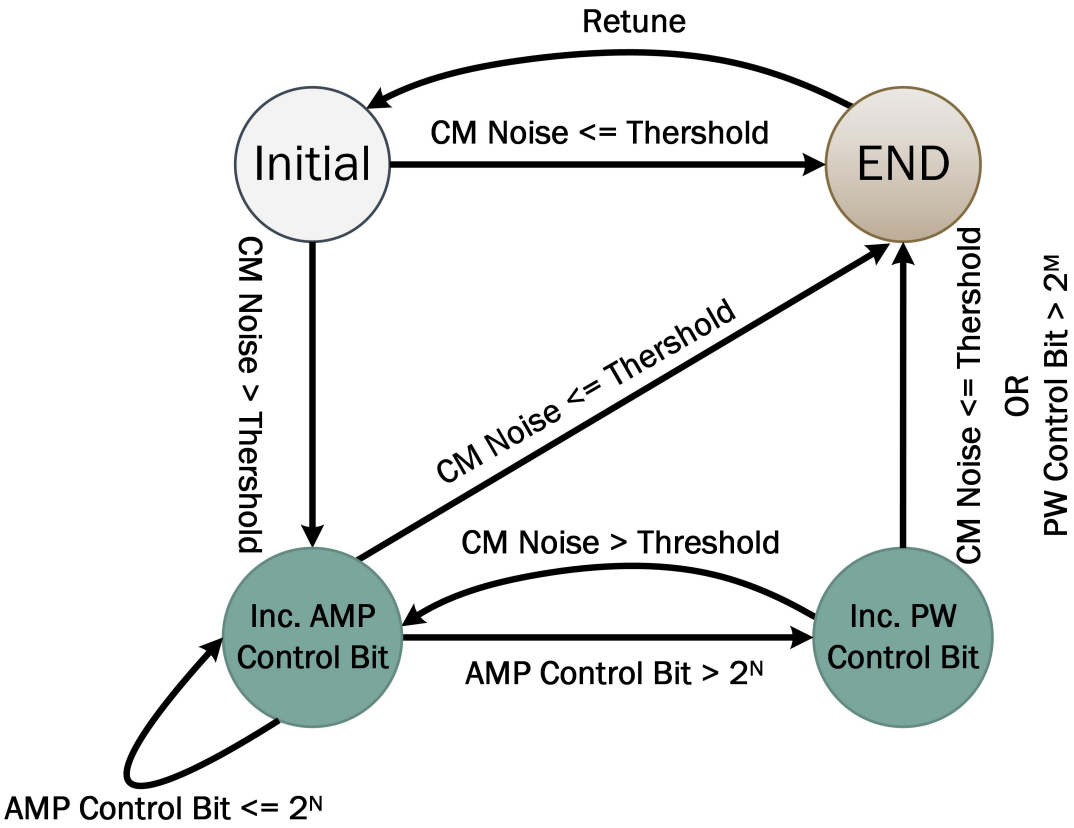

Figure 5.6: Finite state machine implementation of the logic circuit.

PW of the cancellation signal and reset the $Control_{AMP}$ signal.

The PW is adjusted by one step, and the CM noise level at the output of the transmitter detected by the CM noise sensing circuit is compared with the preset or programmable threshold CM noise value. If this CM noise level is below the threshold value, the automatic tuning logic ends the tuning, while if it is above the value, the automatic tuning logic returns to the previous state to adjust the pulse amplitude of the cancellation signal. This cycle keeps running until the CM noise level at the output of the transmitter is below the threshold value or the PW control signal ($Control_{PW}$) reaches its maximum value (2^M), which ends the tuning as indicated by the FSM. If a retuning signal is enabled, the automatic tuning logic returns to the initial state to retune the circuit and then repeats the same procedure as describe above. Once the tuning is complete, the PW and amplitude of the CMNC signal remain fixed at the optimum level.

The tuning range is defined by the values of M and N bit for $Control_{AMP}$ and $Control_{PW}$ signal. If we increase tuning range, it will increase the tuning time. Currently, one cycle needs 30 nsec. If value of N and M bit is set to 4 bits, than total 256 cycles can be tuned and the total time needed to test 256 cycles will be 7.6 us.

5.2.3 PAM-4 CMNC Circuit

The behavioral implementation of the PAM-4 CMNC circuit is depicted in Figure 5.7, where $Data_{LSB}$ and $Data_{MSB}$ are the LSB and MSB input data signals, $Control_{PW}$ and $Control_{AMP}$ are the PW and amplitude control signals generated by the automatic tuning logic, and OUT_N and OUT_P are the CMC signals connected to the transmitter output. This circuit consists of a pulse generator with a variable delay element to adjust the width of the pulse by the $Control_{PW}$ signal. The CMC signal amplitude is tuned by the $Control_{AMP}$ signal to adjust the tail current source in the amplitude control block. Two stages, the LSB and MSB, are utilized to compensate for the CM noise generated by the PAM-4 signal. The CM noise-level dependency is automatically incorporated using the two-stage architecture; e.g., switching between 00 to 11 generates pulses from both stages, and adding them together

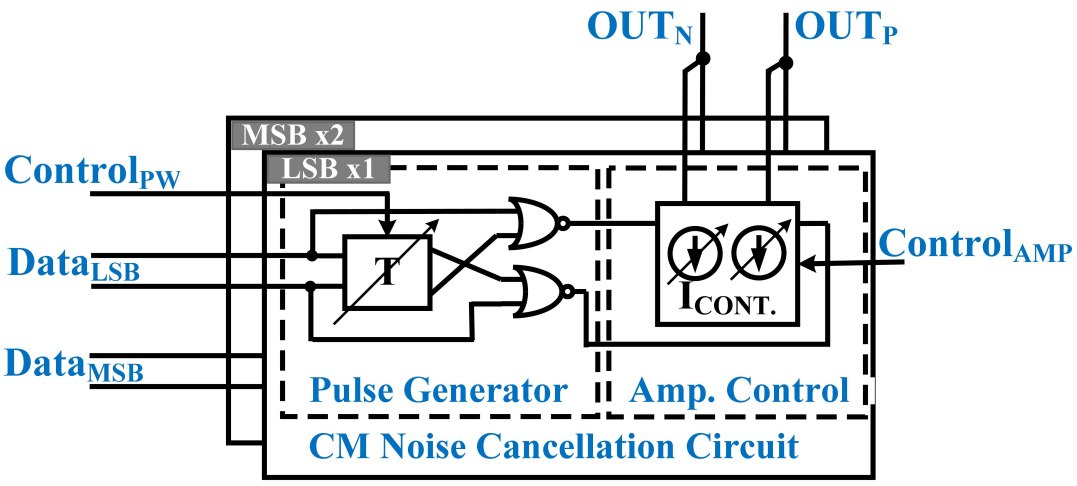

Figure 5.7: Schematic of PAM-4 CMNC circuit.

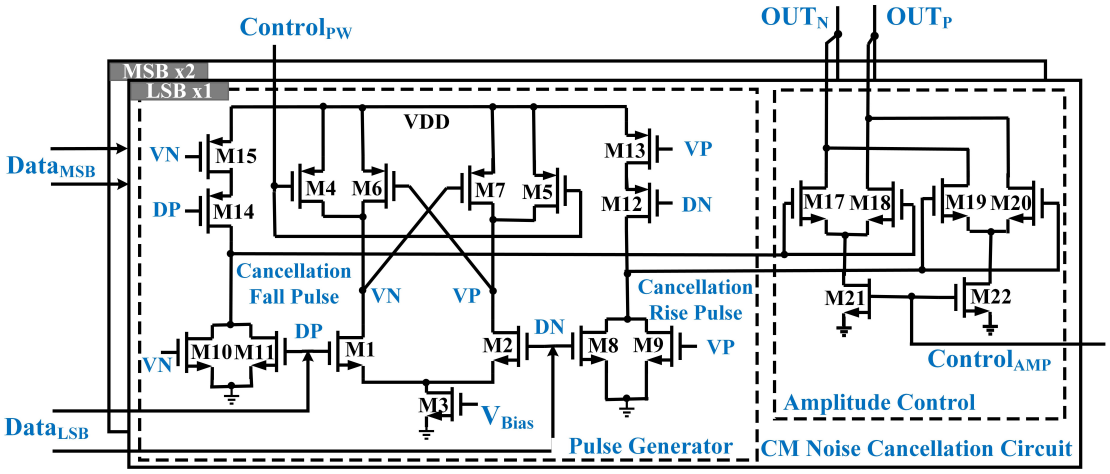

Figure 5.8: Circuit implementation of PAM-4 CMNC module.

creates a higher amplitude of the CMC signal.

The circuit is designed in 40 nm technology, and the schematic of the CMNC is shown in Figure 5.8, where the input and output signals are the same as in the behavioral implementation. An edge detector is utilized to implement the pulse generator. It consists of a differential delay cell and two NOR gates. The input data and its delay version are passed through each NOR gate, which produces a positive pulse of width equal to the delay at every rising and falling edge of the input signal. This pulse drives the transistor switches (M17-M20) in the amplitude control circuit to generate a CMC signal. It steers current from the output and introduces an opposite CM signal for cancellation of noise at the output of the transmitter. The cancellation of CM noise is optimized by tuning the width and amplitude of the cancellation module by the $Control_{AMP}$ and $Control_{PW}$ signals generated by the automatic tuning logic. The width of the pulse is controlled by the gate voltages of transistors M4 and M5, and the magnitude is tuned by the tail current source transistors (M21 and M22) of the amplitude control. The CMNC layout is implemented because it is the most critical circuit for the performance of the automatic CMNC system. The layout of the CMNC module is presented in Figure 5.9. The delay cell, NOR gate and amplitude control circuit are shown in the layout. The CMNC module is designed in 40 nm CMOS technology with a core area of 17 μm $\times$ 9 μm.

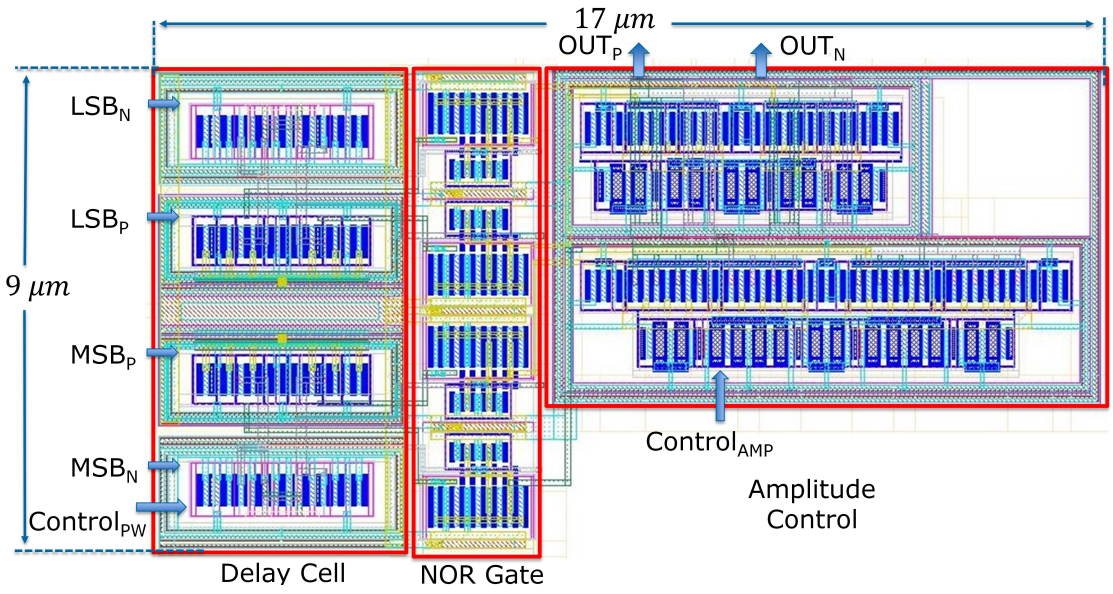

Figure 5.9: Layout implementation of PAM-4 CMNC circuit.

The RC-extraction is performed after the layout DRC and LVS tests for the simulation.

5.3 Simulation Results and Discussion

The 56 Gbps PAM-4 optical transmitter test-bench shown in Figure 5.10 is used to analyze the effectiveness of the proposed automatic CMNC system using the Cadence Virtuoso analog design environment. The test-bench is the same as explained in Section 3.1, except that an FFE module and automatic CMNC system are included. The FFE is the same as discussed in Chapter 3, Section 3.2. The signal from the PRBS generator is fed into the CML driver, FFE module and automatic CMNC system. The output signal of the CML driver, FFE module and CMNC circuit are combined at the OUT_N and OUT_P terminals. The automatic CMNC system senses and suppresses the cumulative CM noise generated by the CML driver and FFE circuit at these nodes. There are two types of interfaces used to connect the driver circuit with the laser. One is single-ended and other is differential. The proposed automatic CMNC system support both single-ended and differential driver interface without any change

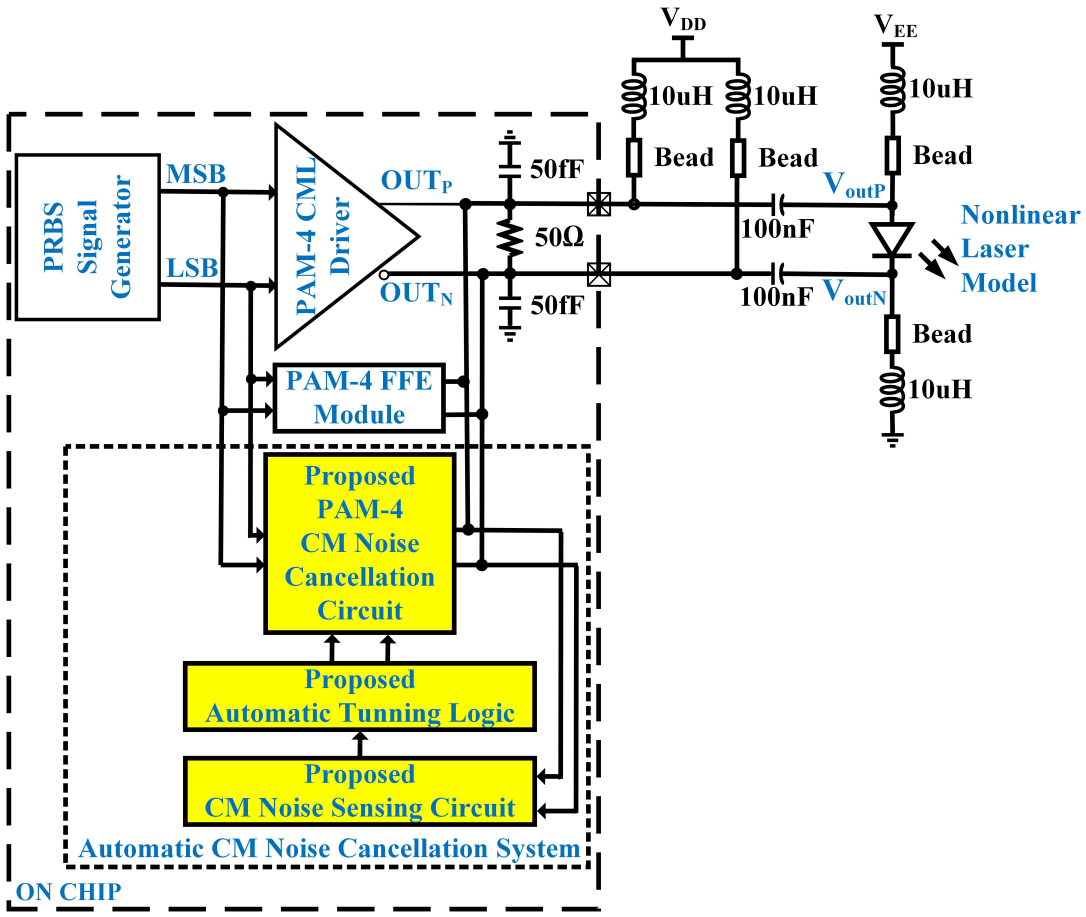

Figure 5.10: Schematic of test-bench to analyze and suppress the EMI-related CM noise in 56 Gbps PAM-4 optical transmitter with FFE.

in the implementation. In this thesis, the differential interface is used because of faster edge-speed and better noise performance.

The CMNC is implemented in 40 nm CMOS technology, and post-layout simulations are presented in this section. The fifth case presented in Table 3.2, the non-linear distortion in the CML driver, and the $\frac{1}{2}$-UI FSA-FFE case, which is the most important configuration of an FSA-FFE for practical applications, are considered for system-level simulation. The amplitude of input data signal is equal to 100 mV, as used in previous simulations. The higher input signal amplitude results in higher CM noise at the output of the transmitter, as predicted by equation (3.7), which need higher cancellation signal amplitude. The automatic CMNC system automatically adjust the cancellation signal

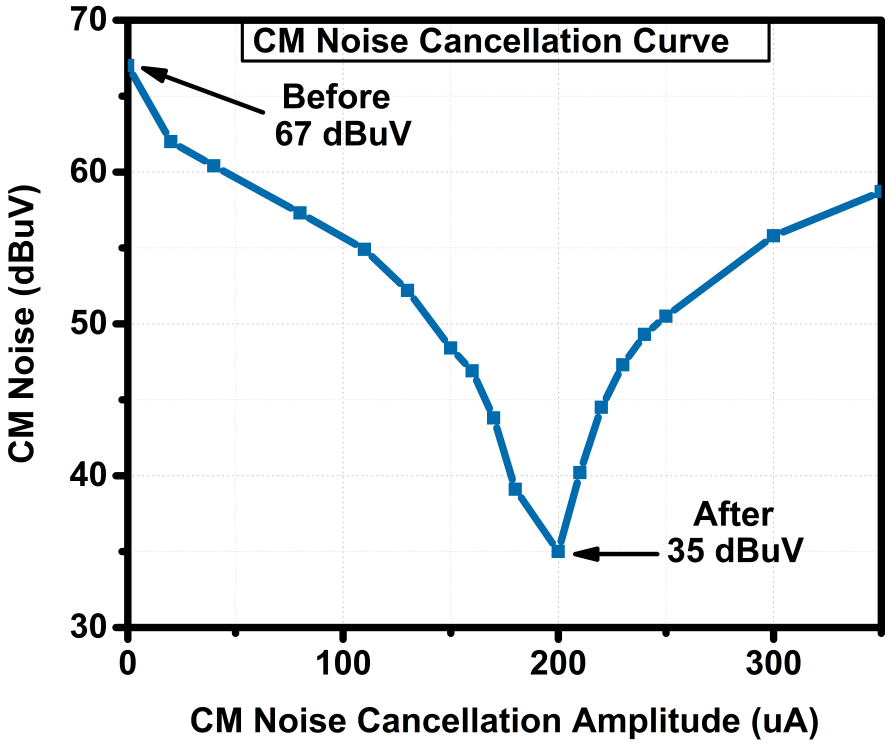

Figure 5.11: RC-extracted post-layout simulation results of CMNC for optimized value of CMC without automatic tuning.

amplitude if higher input amplitudes are applied. The RC-extracted post-layout of the CMNC is used in the test bench, as it is the most critical part for the performance of the automatic CMNC system. The results of the RC-extracted post-layout simulation of the CMNC circuit are depicted in Figure 5.11, where the CMC PW and amplitude are varied to achieve the highest cancellation without automatic tuning turned ON. A reduction of CM noise by up to 90% can be achieved at an amplitude of 200 uA and PW of 17 ps.

The simulation results of the automatic CMNC system are presented in Figure 5.12. It is observed that the cancellation amplitude control and PW control signal are set at initial values, and the CM noise value at the output of the transmitter is compared with the preset or programmable CM noise threshold level. At the start, the CM noise value is higher than the preset or

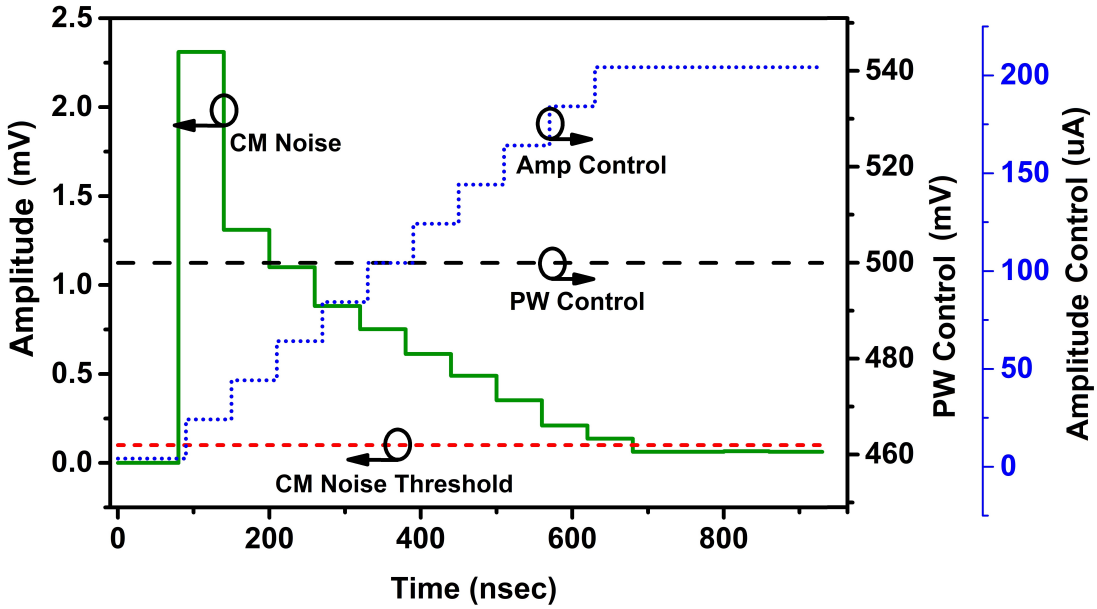

Figure 5.12: Simulation results of PAM-4 automatic CMNC system with RC-extracted post-layout of CMNC in 56 Gbps PAM-4 optical transmitter.

programmable CM noise threshold level and the amplitude control signal is increased step by step until the CM noise at the output of the transmitter is lower than the threshold value, which ends the tuning. The amplitude and PW control signal remain fixed after tuning at the optimized values.

The CM noise transient signal and its spectrum before tuning are shown in Figure 5.13. It is observed that the CM noise has three amplitudes because of the different transition levels of the PAM-4 signal, and the highest amplitude is about 10 mV with PW of 7 ps. The CM noise before tuning is 67 dBuV. Figure 5.14 shows the CM noise transient signal and its spectrum after tuning. It is observed in the transient CM noise signal that, after tuning, the CM noise PW and amplitude are reduced, and also that it contains positive and negative amplitudes, which reduce the cumulative CM noise at the output of transmitter. The highest amplitude of the transient CM noise signal after tuning is 4 mV with a very narrow PW and about the same amplitude of negative pulses, as introduced by the CMNC circuit. The CM noise can be suppressed by up to 90% at the PW of 17 ps and amplitude of 200 uA, as depicted in Figure 5.14, where the frequency component at twice the Nyquist frequency, known as total

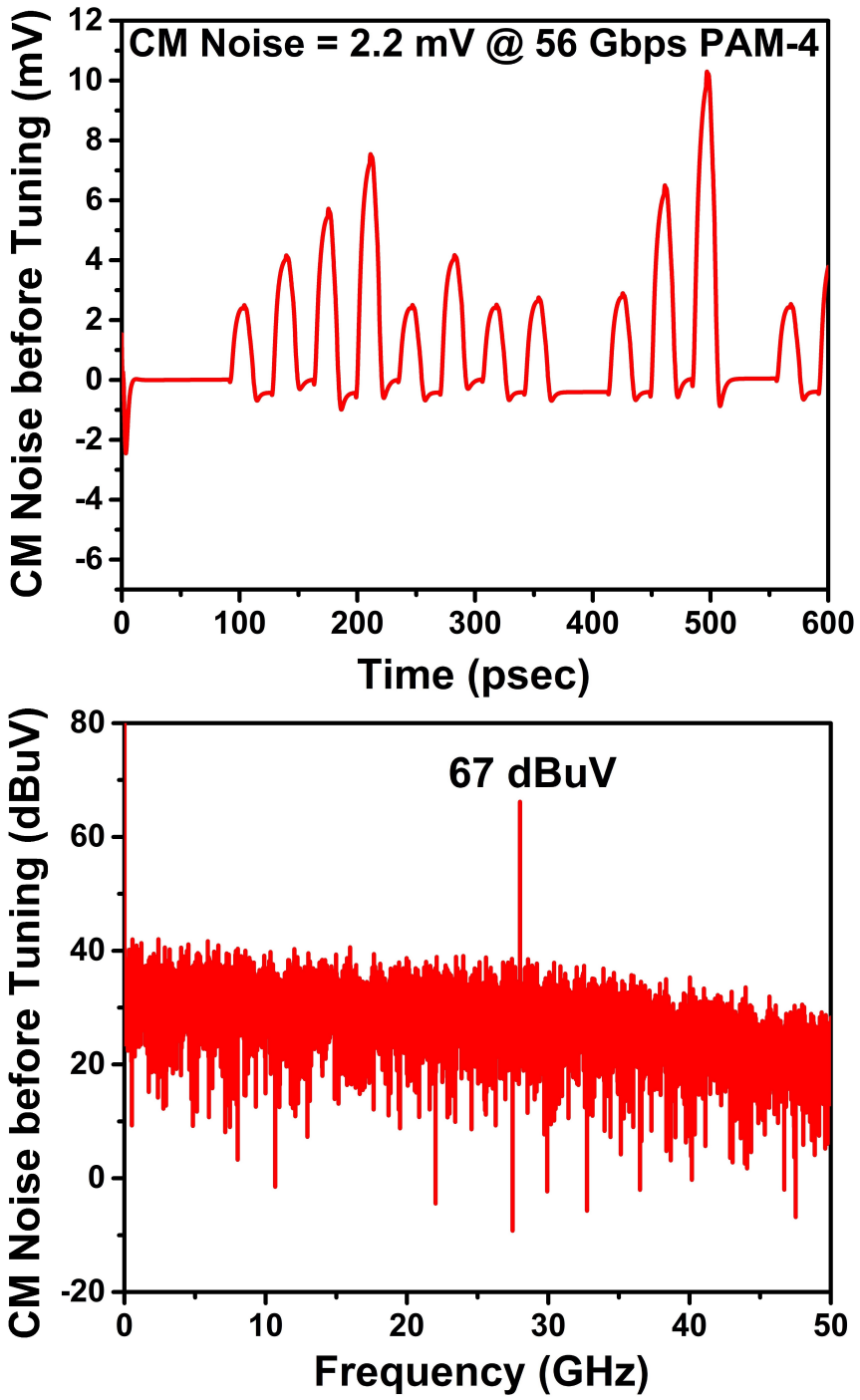

Figure 5.13: Simulation results of PAM-4 automatic CMNC system showing CM noise signal before tuning in 56 Gbps PAM-4 optical transmitter.

CM noise ($N(2F_{Nyquist})_{Total}$), is reduced from 67 dBuV to 35 dBuV [1]. This reduces the EMI significantly by suppressing the cumulative CM noise at the output of the transmitter.

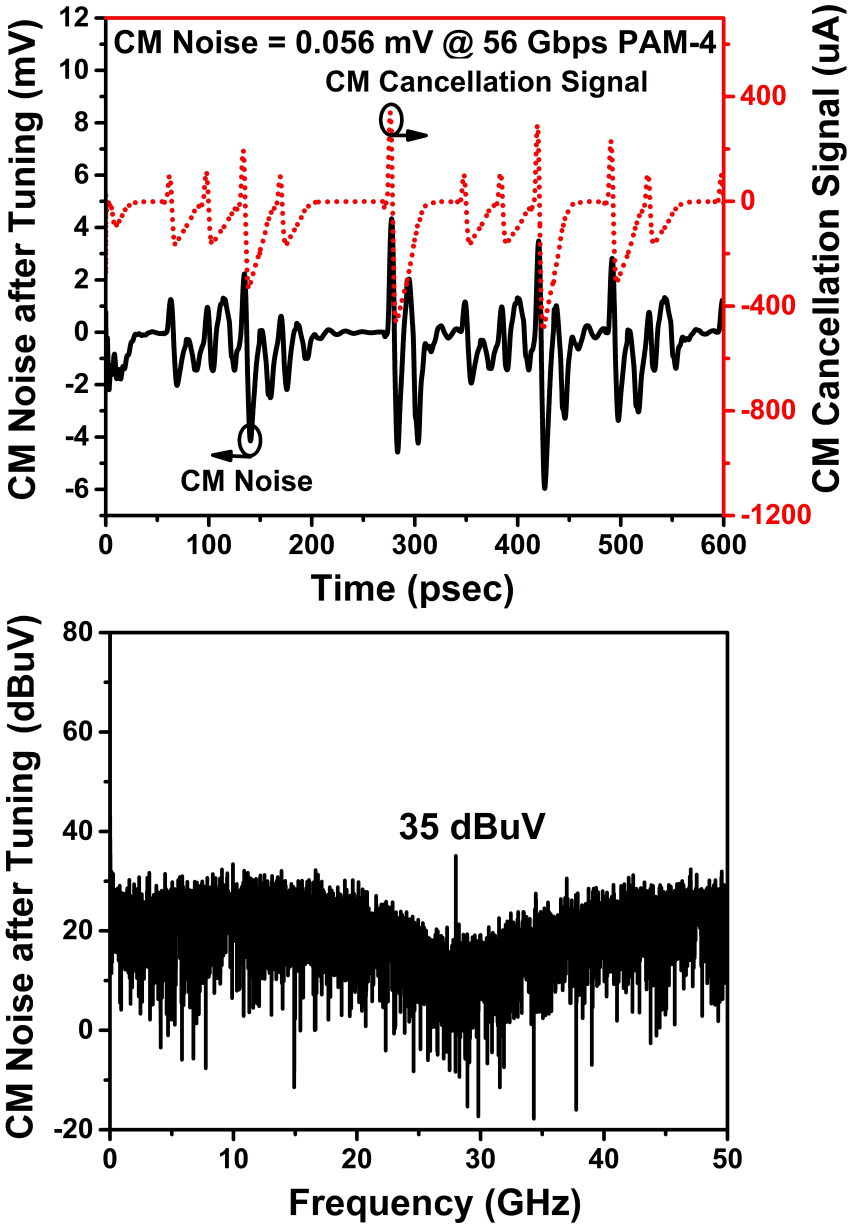

Figure 5.14: Simulation results of PAM-4 automatic CMNC system showing CM noise signal after tuning in 56 Gbps PAM-4 optical transmitter.

The optical eyes with and without CMNC at the output of the PAM-4 optical transmitter are shown in Figure 5.15. The three optical eye openings, namely, top, mid and bottom, are equalized using a $\frac{1}{2}$-UI FSA-FFE. The amplitude of the optical eye is 172 mV and PW is 26 ps. The optical eye performance remains about the same with and without compensation, as depicted in Figure 5.15, which demonstrates that this technique does not degrade the optical signal performance. This is due to the low amplitude of the

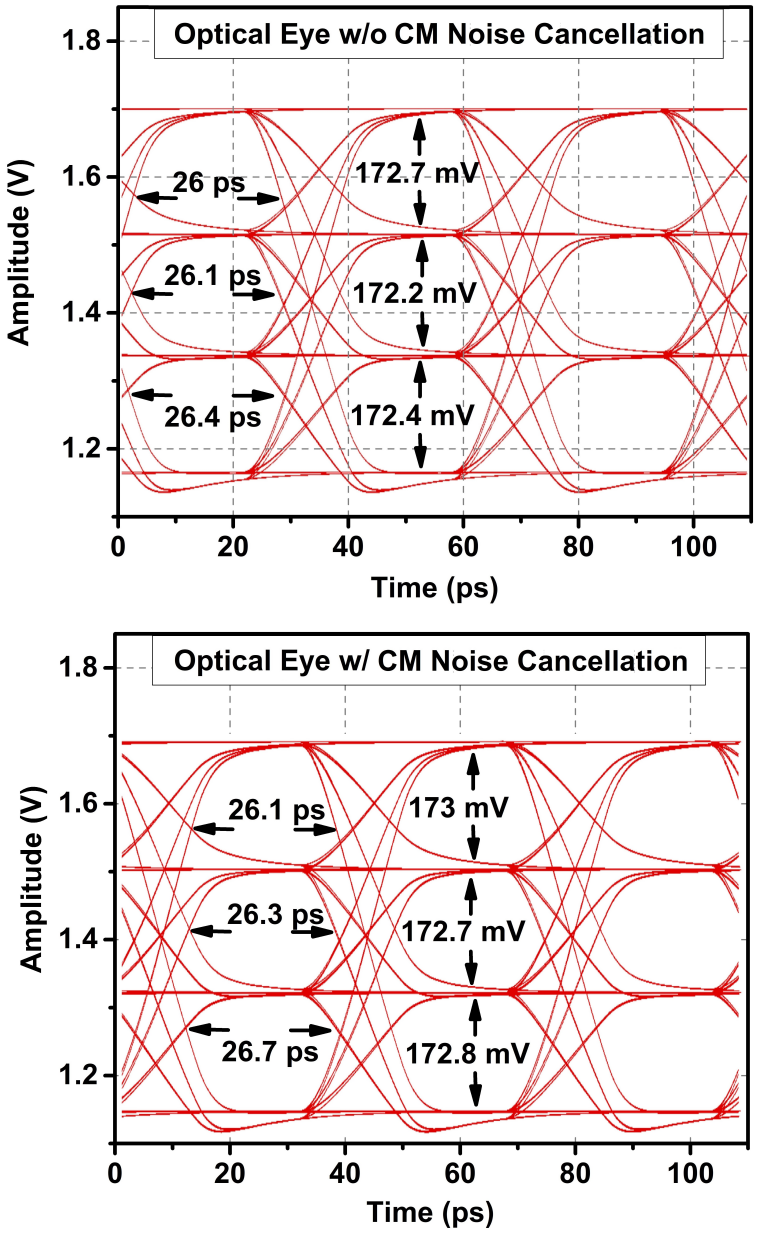

Figure 5.15: Optical eyes with and without CMNC in 56 Gbps PAM-4 optical transmitter.

compensation, at 200 uA, as compared to the bias current of 60 mA.

The effectiveness of the tuning is simulated with varying data rates. It is observed that the CM noise before tuning increases with the increase of the data rate. However, after tuning, the CM noise remains below the threshold value, as shown in Figure 5.16. There is no need of retuning if the data rate has changed after tuning the transmitter. The CMNC circuit automatically changes

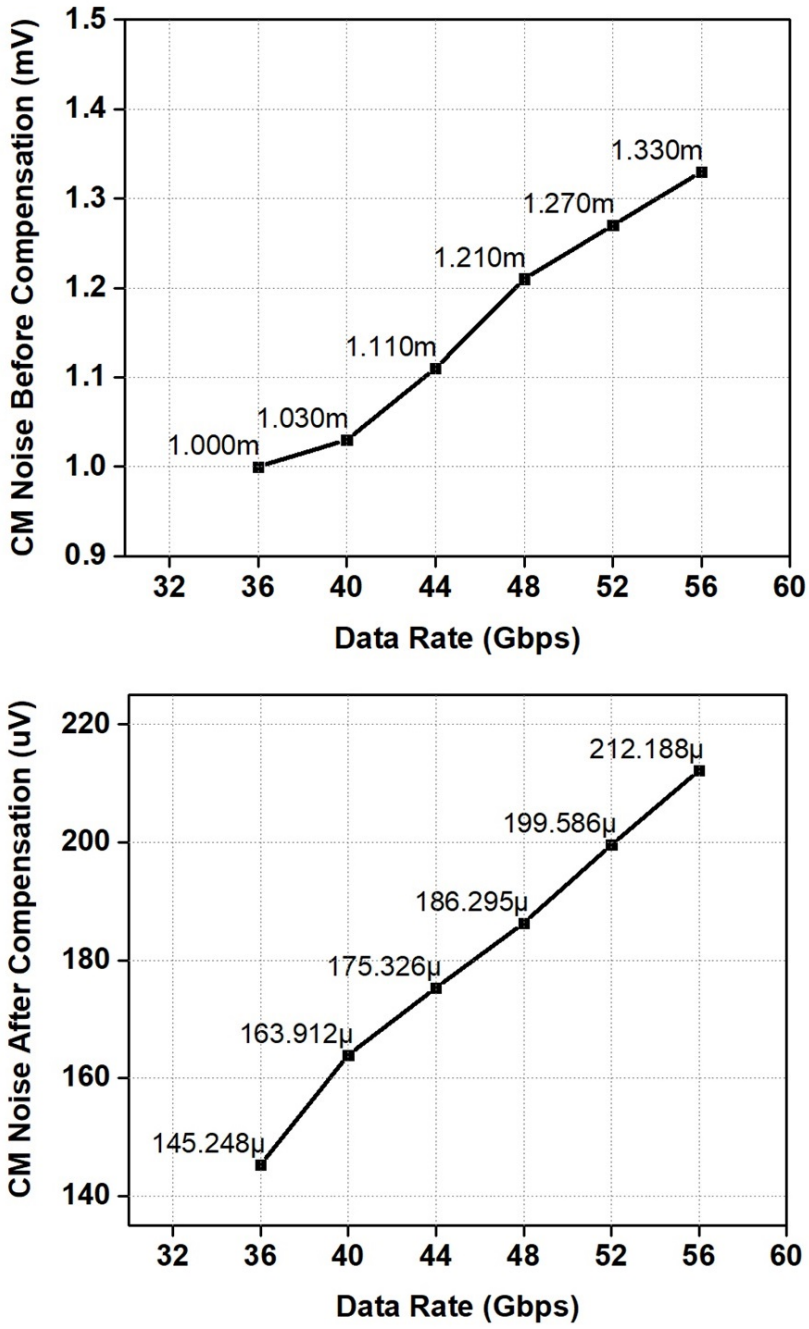

Figure 5.16: CM noise before and after tuning with variation in input data rate.

the cancellation signal according to the input data transitions.

The estimated power breakdown of the transmitter is depicted in Figure 5.17. The highest power is consumed by the CML driver circuit, which is 41%, and the CMNC circuit only consumes 3% of the total power of the transmitter.

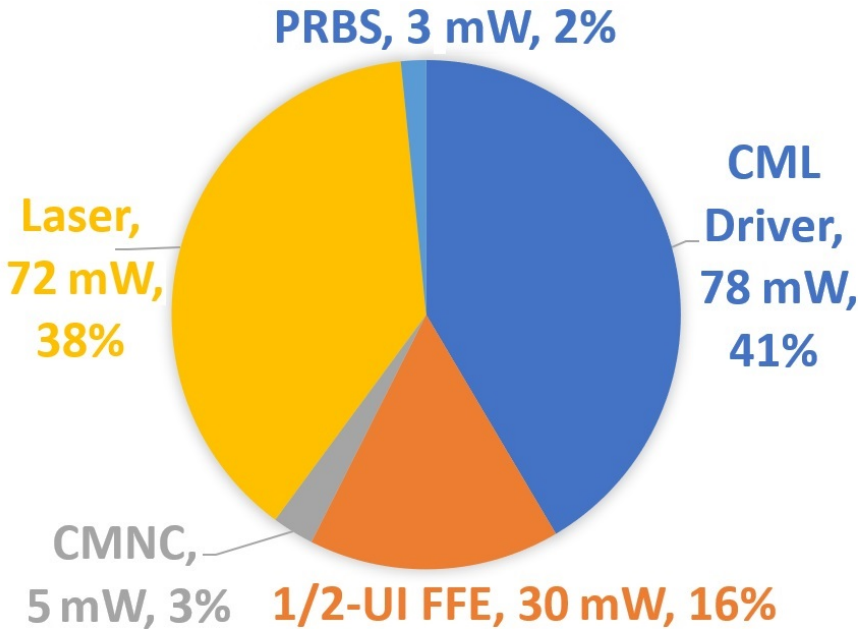

Figure 5.17: Power breakdown of the PAM-4 optical transmitter.

5.4 Summary

In this chapter, an automatic cancellation circuit technique supporting PAM-4 signaling is first proposed to suppress the CM noise generated by the driver and FSA-FFE circuit. Then, a PAM-4 automatic CMNC system is simulated with the layout implementation, which reduces the EMI by significantly suppressing the CM noise. This novel CMNC system provides a low-cost and small-size solution for high-speed transmitters supporting PAM-4 signaling to meet the EMC limitation prescribed by the FCC and CISPR, and also helps to reduce the EMC validation complexity of the design.

5.5 References

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Chapter 6

Conclusion and Future Work

6.1 Conclusion

This thesis presents CM noise analysis, and proposes an automatic CMNC system for PAM-4 transmitters.

In Chapter 2, the main modules of a 56 Gbps PAM-4 optical transmitter are briefly discussed. The data are generated by a PRBS generator, and a CML driver circuit is used as the laser driver. Further, and asymmetric FFE is used to compensate for the non-linearity of the laser and channel, while an automatic CMNC circuit is employed to cancel the CM noise generated in this optical transmitter.

The mathematical analysis of the CM noise in a PAM-4 transmitter is presented in Chapter 3. The mathematical analysis is then proved by behavioral- and transistor-level simulations. The PAM-4 CM noise is given by

$$N(2F_{Nyquist})_{Total} = N(2F_{Nyquist})_{CML} + N(2F_{Nyquist})_{FFE}, \tag{6.1}$$

$$N(2F_{Nyquist})_{Total} = \frac{1}{8}R_F Amp\frac{|t_{rise} - t_{fall}|}{T_b}sinc^2\left(\frac{\pi}{2}\frac{T_{tr}}{T_b}\right) + \frac{A}{\pi}sin\left(\pi\frac{T}{T_0}\right) + offset. \tag{6.2}$$

The total CM noise at the output of the transmitter is the sum of the CM noise generated by the CML driver and FFE circuit. It is demonstrated that the intrinsic impedance variations of the CML driver circuit, amplitude of the equalization current and offset in the FFE circuit are the main sources of EMI-related CM noise in the transmitters.

The speed requirements for advanced applications used in 5G are met by scaling of transistor devices. In Chapter 4, the effect of transistor scaling on CM noise is analyzed. The CML driver is designed in both the 40 nm CMOS and 14 nm SMIC technology nodes and simulation results are presented. The advance technology nodes utilized to achieve higher data rate which increase the CM noise significantly.

Reducing the CM noise to meet the EMC standards is a desired goal. In Chapter 5, the CMNC methodology is presented and an on-chip automatic CMNC system is designed for a PAM-4 optical transmitter. This circuit generates a CMNC signal which suppresses the noise at the output of the transmitter. This methodology can be used for both NRZ and PAM-4 optical and wireline transmitters.

6.2 Future Work

6.2.1 Automatic CMNC system for Advanced Modulation Scheme

With the rapid growth in the demand for data transmission, modulation techniques such as PAM-4, PAM-8, and coherent modulation, are under extensive research. For data rates higher than 50 Gbps, PAM-4 has replaced the NRZ modulation technique [1–5], and a 225 Gbps PAM-8 transmitter has been reported in [6]. To achieve higher data rates, more complex modulation techniques, like PAM-8, PAM-16 and coherent modulation, will be adopted in future.

The automatic CMNC technique in this thesis could be extended to support higher speed and more complex modulation schemes like PAM-8 and coherent modulation by modifying the CMNC design. The sensing and tuning logic circuit would remain the same, and only the CMNC would be modified to support advanced modulation techniques. The possible implementation of the CMNC for PAM-8 modulation is depicted in Figure 6.1. The CMNC consists of three

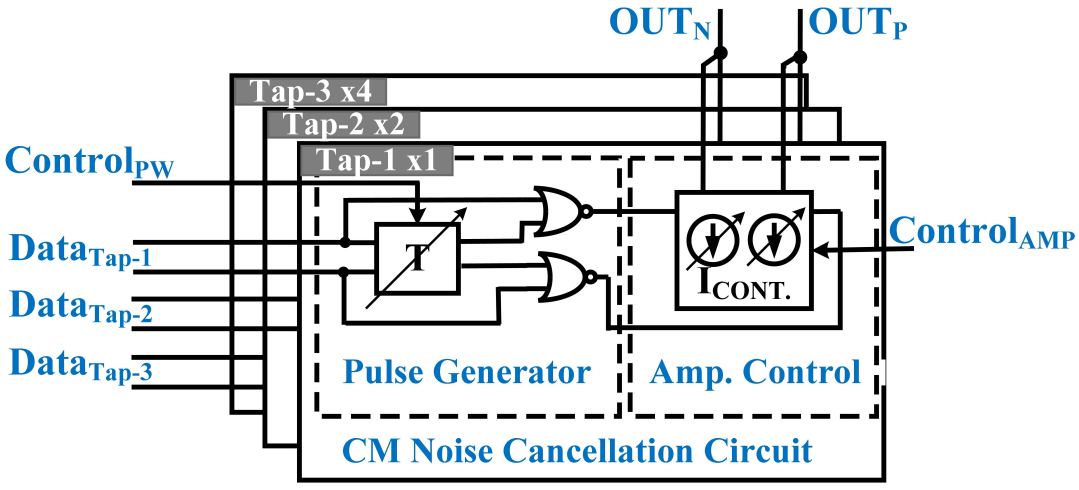

Figure 6.1: Implementation of PAM-8 CMNC circuit.

parallel modules instead of the two used in the PAM-4 implementation. The

sizing of the devices is to the power of 2^n in each module, where n is three, in the case of PAM-8 modulation.

6.2.2 Millimeter-Wave MOSFET Amplitude Detector for CM Noise Sensing Circuit

The CM noise sensing circuit uses a high frequency clock, which is a complicated design for a high-speed transmitters. The root mean square (RMS) or a peak detector can be used to measure high-frequency voltages, and many millimeter-wave detectors have been reported [7–9]. A millimeter-wave amplitude detector could replace the multiplexer and clock generator in the sensing circuit, which is used to determine the value of the CM noise at the output of the transmitter. The possible millimeter-wave circuit implementation is presented in Figure 6.2.

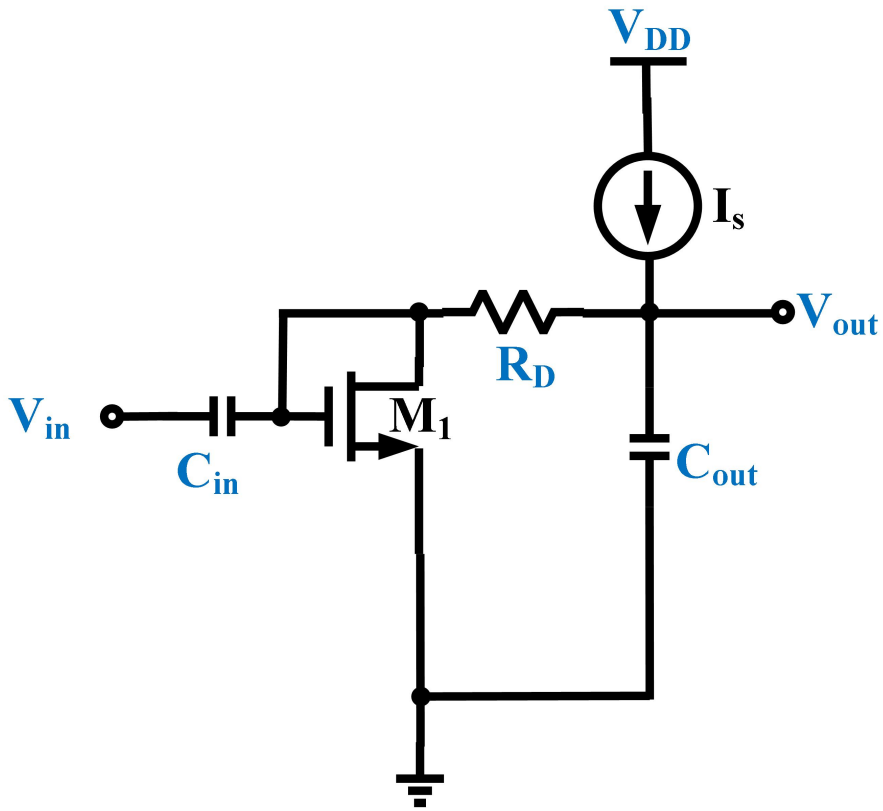

Figure 6.2: Millimeter-wave voltage detector.

6.3 References

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