Transceiver Design for Optical Wireless and Wireline Communication

by

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To my parents

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Abstract

Optical wireless and wireline communication technologies have attracted wide research efforts due to various advantages, such as high flexibility, security and wide unlicensed spectrum. In the emerging 5G network, optical wireless communication can provide ubiquitous access points for Internet-of-things (IoT) devices and ease the ever-increasing radio spectrum congestion problem. Optical wireline communication is rapidly migrating towards 400G Ethernet for high-speed and low-latency data center interconnections. This thesis focuses on the transceiver designs with novel and enhanced equalization and jitter compensation functions for high-speed optical wireless and wireline communication.

In the first part, a PAM-4 wireless optical communication system using a RGB LED as light source is presented. The RGB LED units are modulated separately using 3-bit thermometer codes. The three-path RGB NRZ optical signals superpose mutually in free space and produce the PAM-4 optical signal. A piece-wise FFE based pre-equalization and 3-stage continuous-time linear equalizer base post-equalization are employed to compensate for the RGB LED unit bandwidth difference. The highest data rate of the system can be extended from 28 Mbps to 75 Mbps using the proposed equalization scheme, achieving an extension ratio of 2.67.

In the second part, a quarter-rate PAM-4 receiver with a jitter compensate clock and data recovery (CDR) circuit is presented for optical wireline communication. The proposed CDR architecture can overcome the stringent trade-off between jitter transfer (JTRAN) and jitter tolerance bandwidth (JTOL BW). The Prototyped 40-nm CMOS Rx test chip achieves error-free operation with PAM-4 input from 30 to 60 Gb/s. The JCCDR achieves a 40-MHz JTOL BW with over 0.2-UIPP jitter amplitude while maintaining a -8-dB JTRAN. A jitter compensation ratio of around 60% has been achieved up to 40 MHz.

Finally, in the last part, the bandwidth extension schemes developed in the previous system is applied to a wireless power and data transmission system, which provides simultaneous wireless charging and communication accesses for IoT devices. A three-stage continuous-time-linear-equalizer (CTLE) is used to compensate for the narrow and distance-dependent bandwidth of wireless power and data transfer (WPDT) systems. A receiver front-end circuit

with the proposed CTLE and multiple-stage filter is implemented to decoupling the data and power signal. The highest data rate extension ratio of 85% has been achieved from 350 kbps to 650 kbps at a transmission distance of 0.6 m, which is 2.4 times the radii of the transceiver coil.

Chapter 1 Introduction

1.1. Brief Introduction to Optical Communication

The abundance of unlicensed optical spectrum from visible to infrared light range has attracted wide research interest for delivering high-speed communication link through wireless or wireline channels. Optical communication technology transmits optical signal by modulating the laser diode (LD) or light emitting diode (LED) on the transmitter side, and converts it back to electrical signal using photo diode (PD) on the receiver side. The optical signal can be transmitted through fiber for long-reach optical wireline communication, or through free space for short-reach optical wireless communication. Due to the high bandwidth of light emitting devices, optical communication technology can cover a wide application scenarios, such as high-speed Ethernet, backbone network and high security in-door wireless communication.

A typical optical communication system architecture is presented in Fig. 1.1, consisting of a transmitter, a LD or LED, a PD, and a receiver. The transmitter circuit consists of an encoder, a pre-equalization, and a driver circuit as output stage. The input data is encoded using a

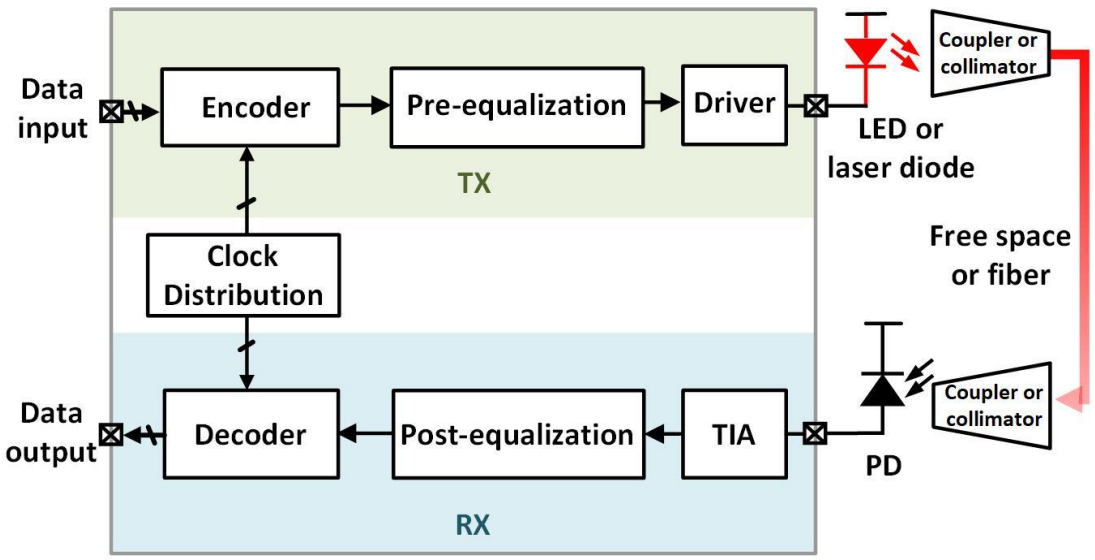

Figure. 1. 1. Typical block diagram of an optical communication system.

certain modulation format. A pre-equalizer circuit following the encoder compensates for the bandwidth limitations due to light emitting devices or transmission line connections. The driver modulates the output light intensity with the equalized data by directly controlling the light emitting device current, or driving an external modulator. On the receiver side, the optical signal is converted into a weak photo current signal using a photo diode, which is then amplified by a trans-impedance amplifier into a voltage signal. A post-equalization provides further bandwidth extension to boost the highest achievable data rate. The equalized signal can be decoded into digital signal using analog-to-digital converter (ADC) or multi-level slicers. A clock distribution circuit consisting of a phase-locked loop and clock recovery circuit is used to synchronize both the transmitter and receiver circuit.

1.1.1. Optical Wireless Communication

Optical wireless communication technology employs LED, micro-LED, or LD as light sources and transmits the optical signals in free space. Due to the dispersive nature of light, the transmission distances cover a few centimeters, several meters, and tens of meters, for LED, micro-LED and LD, respectively. The highest achievable data rates of optical wireless communication are constrained by light-emitting device architectures, and light emitting processes.

For LD, the output laser light is generated from a stimulated emission process. The carrier lifetime in LD can reach hundreds of picosecond, yielding an analog bandwidth of over GHz [1, 2]. The short carrier lifetime is achieved by two critical factors. First, the LD can sustain large current density without efficiency droop, which leads to a higher hot carrier recombination rate. Second, the recombination process is stimulated by the existing photons, therefore short carrier lifetime can be achieved through the stimulation process. Benefitting from the short lifetime, LD-based optical wireless communication can reach over Gbps data rate using simple non-return-to-zero (NRZ) modulation scheme [3]. Since LD can provide high enough signal-to-noise-ratio (SNR), high-level modulation schemes, such as M-quadrature amplitude modulation (M-QAM) have been adopted to boost the data rate up to tens of Gbps [4, 5].

Micro-LED have been widely adopted for micro-display arrays for wearable, virtual reality (VR) and augment reality (AR) devices. The spontaneous emission process in micro-LED device causes longer carrier lifetime up to a few nanoseconds, which produces a bandwidth of around hundreds of MHz [6]. In addition, only simple modulation formats such as non-return-to-zero, and short transmission distance of a few centimeter can commonly be supported, due to the very limited optical power of micro-LED, typically less than 1 mW per device [7].

The LED devices have been widely deployed in display backlighting and illumination. Existing LED infrastructures can potentially be reused as optical wireless communication light sources, with simple modification in the LED drivers. Compared to LD and micro-LED,

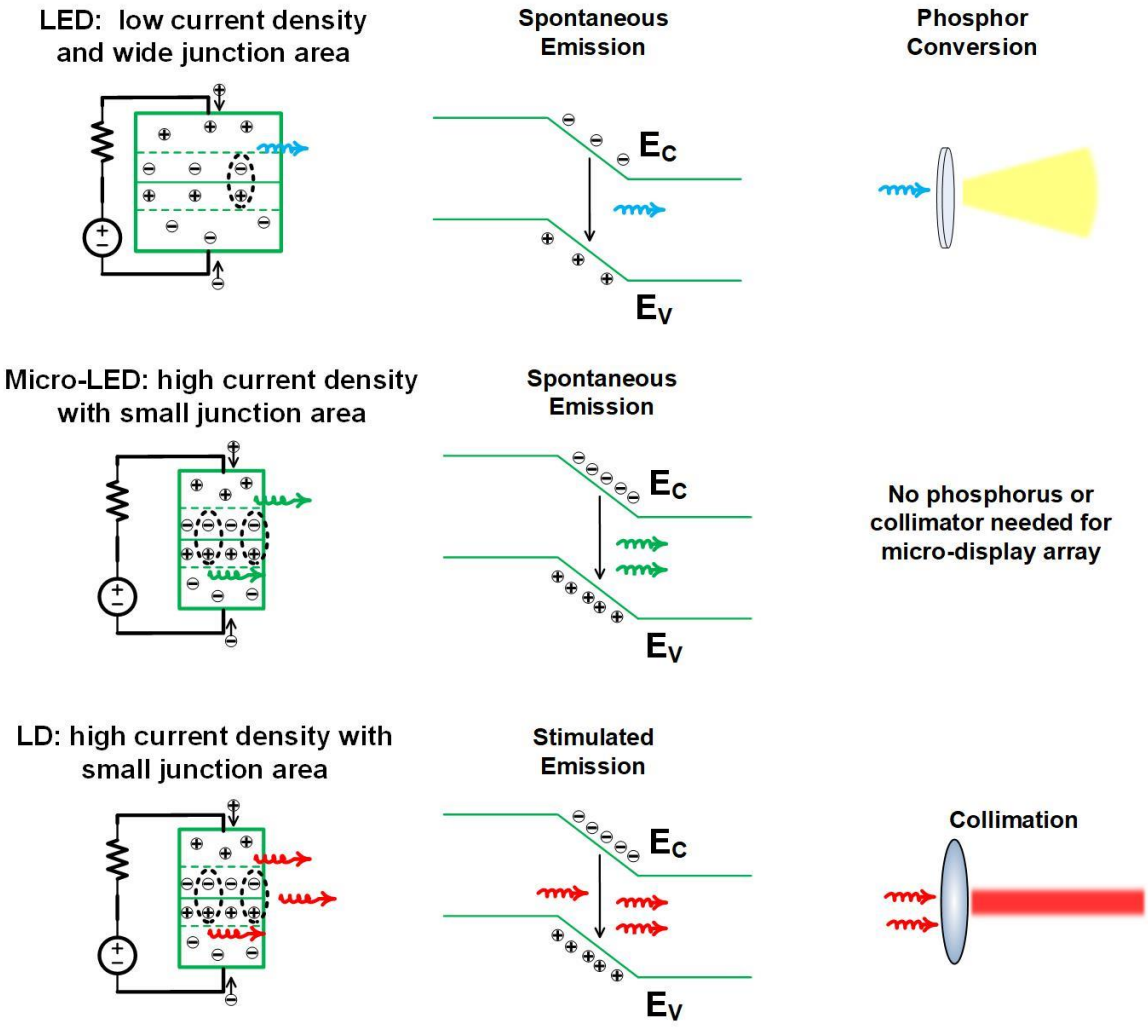

Figure. 1. 2. Comparison of optical wireless communication systems using LED, micro-LED, and LD as light sources.

LED devices is capable of covering a wider communication area, providing better SNR and is more cost-efficient. However, the analog bandwidth of LED is rather limited to below 10 MHz due to several reasons [8]. First, since the off-the-shelf LED devices are designed with wide junction area for high power illumination purpose, the large parasitic junction capacitance causes a significant RC delay limiting the bandwidth. Second, compare to LD and micro-LED, the current density in the LED junction area is much lower, due to the efficiency droop characteristic. The low current density reduces the carrier recombination rate, resulting in a longer carrier lifetime. Third, a yellow phosphorus is commonly adopted as light converter to convert the blue light into white light. However, the phosphorus causes an even more limited bandwidth of a few MHz.

1.1.2. Optical Wireline Communication

Optical wireline communication employs 850-nm, 1310-nm and 1550-nm LD as light sources and transmits optical signal through optical fibers. Due to the much lower channel loss of optical fiber, for example, 3-dB/km for 850 nm, 0.5-dB/km for 1310 nm, 0.4-dB/km for 1550 nm [9], the optical wireline communication can cover a wide transmission distance, from hundreds of meters, to tens of kilometers. This distance can be further extended to thousands of kilometers with the help of optical amplifier, such as erbium doped fiber amplifiers (EDFA).

Traditional optical wireline communication transceiver were implemented using III-V technology for long haul communication, such as wide area network (WAN) [10, 11]. The III-V technology achieves low noise, wide bandwidth and large driving current at the cost of increased investment. Recently, due to the proliferation of data intensive applications, such as massive parallel training of deep neural network, 8K display and could computing services, the data traffic within data center is going through an explosive growth. Optical wireline communication transceiver has been widely deployed and upgraded in data center to support the high-speed and low latency Ethernet. The communication data of a single channel is expected to support 56 Gb/s for the 400G Ethernet under deployment, and will reach over 100Gb/s for the next-generation 800G Ethernet. CMOS technology is becoming an attractive candidate against III-V technology for implementing the cost-efficient optical transceiver. Compared to traditional optical communication systems realized in the III-V technology,

CMOS monolithic optoelectronic integrated circuits (OEICs) ensures low-cost, small system form factor and high volume manufacturing capacity. However, the performance of OEICs is usually inferior, with lower speed but higher noise.

1.2. Application Scenario

The future service-driven 5G network aims to flexibly and efficiently meet diversified mobile

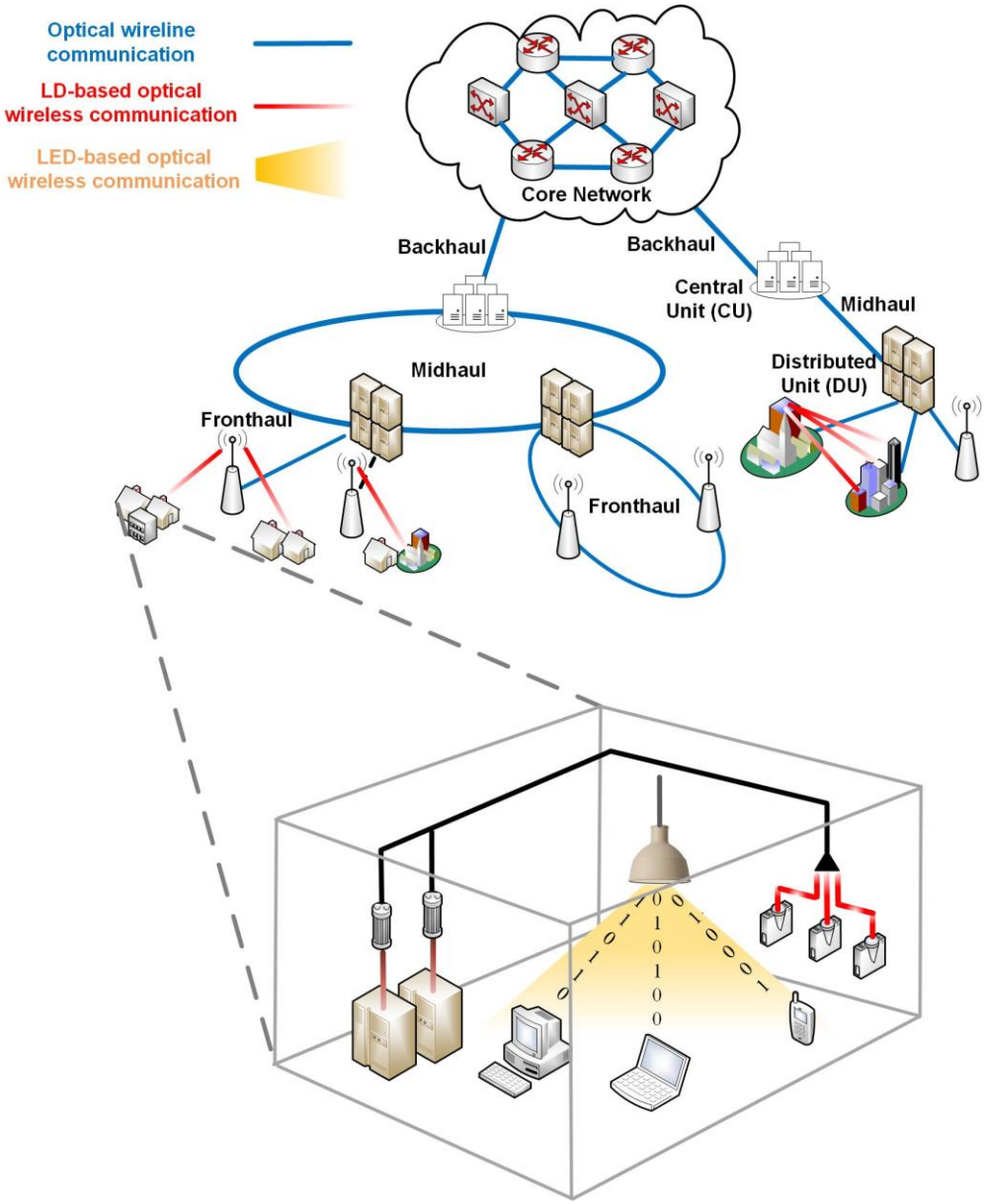

Figure. 1. 3. Application scenarios of optical wireless and wireline communication in 5G network.

service requirement, including Enhanced Mobile Broadband (eMBB), Ultra-reliable and Low-latency Communications (uRLLC), and Massive Machine Type Communications (mMTC) [12]. An overview of potential applications of optical wireless and wireline communication in 5G network is presented in Figure. 1. 3.

In indoor environment, mMTC aims to support the network connection demands for emerging digital electronic applications, such as internet-of-things (IoT) devices, AR/VR devices and medical implant devices. Due to the limited RF spectrum resources, the RF communication congestion problem is getting increasingly serious. Optical wireless communication with different kinds of light sources can potentially serve as complementary wireless data access points (APs) for various smart furniture. As shown in Figure. 1. 4, the LED-based optical wireless communication can support simultaneous illumination and high-speed data downlink for televisions, laptops and desktops. The uplink can adopt infrared optical wireless link or RF link, which requires low data rate for handshake, authentication, and data transfer protocol control. By integrating the wireless communication function with the existing LED infrastructure, the light intensity and color temperature can also be monitored in real-time. The users will be able to flexibly control the LED illumination level in different zones

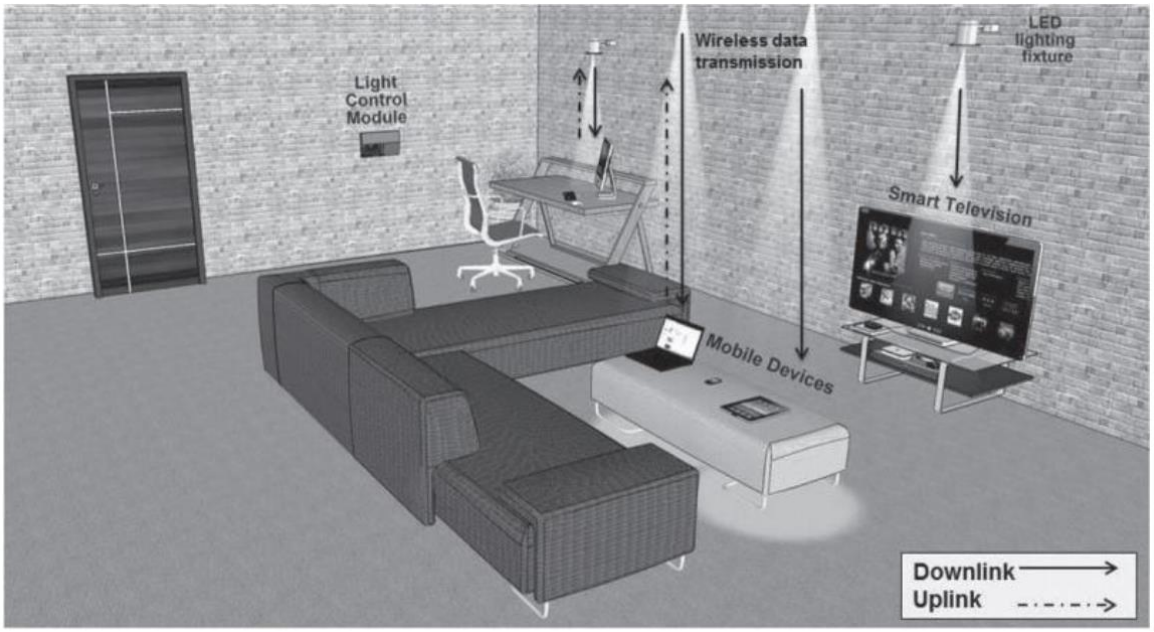

Figure. 1. 4. Application of LED-based optical wireless communication system in indoor environment [13].

according to occupancy conditions for better energy saving. Micro-LED display-based optical wireless communication can provide flexible near-field communication links, which allows face-to-face swift document transfer. For example, when two users both wearing smart watches with micro-LED display, they can share local data through micro-LED based optical wireless communication link without direct contact. In this application scenario, both downloading link and uploading link are realized using optical wireless communication technology.

In outdoor environment, eMBB focuses on supporting the services requiring ultra-high bandwidth, such as high-definition (HD) videos. The 5G wireless access is expected to provide an aggregated data rate of 10 Gb/s for around 10 users simultaneously. Therefore, Fronthaul connections with enhanced bandwidth need to be deployed. RF over fiber (RFoF) technology has been widely employed to achieve long-distance wired Fronthaul communication, since the channel loss in fiber is much lower than wireless link. However, laying down optical fibers underground is challenging in mountainous areas, and it causes difficulty in long-term maintenance and upgrading. Millimeter wave (mmWave) technology has received wide research attention towards high-speed wireless Fronthaul. However, various problems have been limiting the practical deployment, such as high power consumption, requiring advanced fabrication process and accurate beamforming. LD-based optical wireless communication is a potential choice for wireless Fronthaul due to several attractive features. First, narrowed laser beam with small footprint, and precise point-to-point alignment can be achieved by using a collimator. Second, compared to mmwave technology, baseband signal can be transmitted directly through LD-based optical wireless link. Without requiring tens of GHz carriers, traditional CMOS process such as 90mm and 180nm can be employed for cost-efficient transceiver development. Finally, the typical output stage of LD driver adopt current mode logic architecture. Compared to mmwave power amplifier, the current mode driver can steer the current directly to the off-chip LD, without flowing through an on-chip VDD. Therefore, the heating problem due to the high power consumption can be avoided.

Moreover, uRLLC aims to meet the demands for latency sensitive applications, such as assisted and autonomous driving, remote management, and remote surgery. In 5G network, by processing user data in distributed units, the large latency due to backhaul data transmission in traditional 4G network is significantly alleviated. Therefore, data center development is critical to meet the rapidly increasing local data processing demand. Optical wireline communication has been widely adopted to handle the high-density data traffic in data centers. Compared to conventional copper cable connection, optical interconnects provide some outstanding features, such as higher layout flexibility, longer transmission distance, and smaller form-factor. Short reach optical transceivers using direct-modulated VCSELs and multi-mode fiber are used for connecting the servers with nearby Top-of-Rack (ToR). Long reach transceivers using distributed feedback lasers (DFB) can be used for

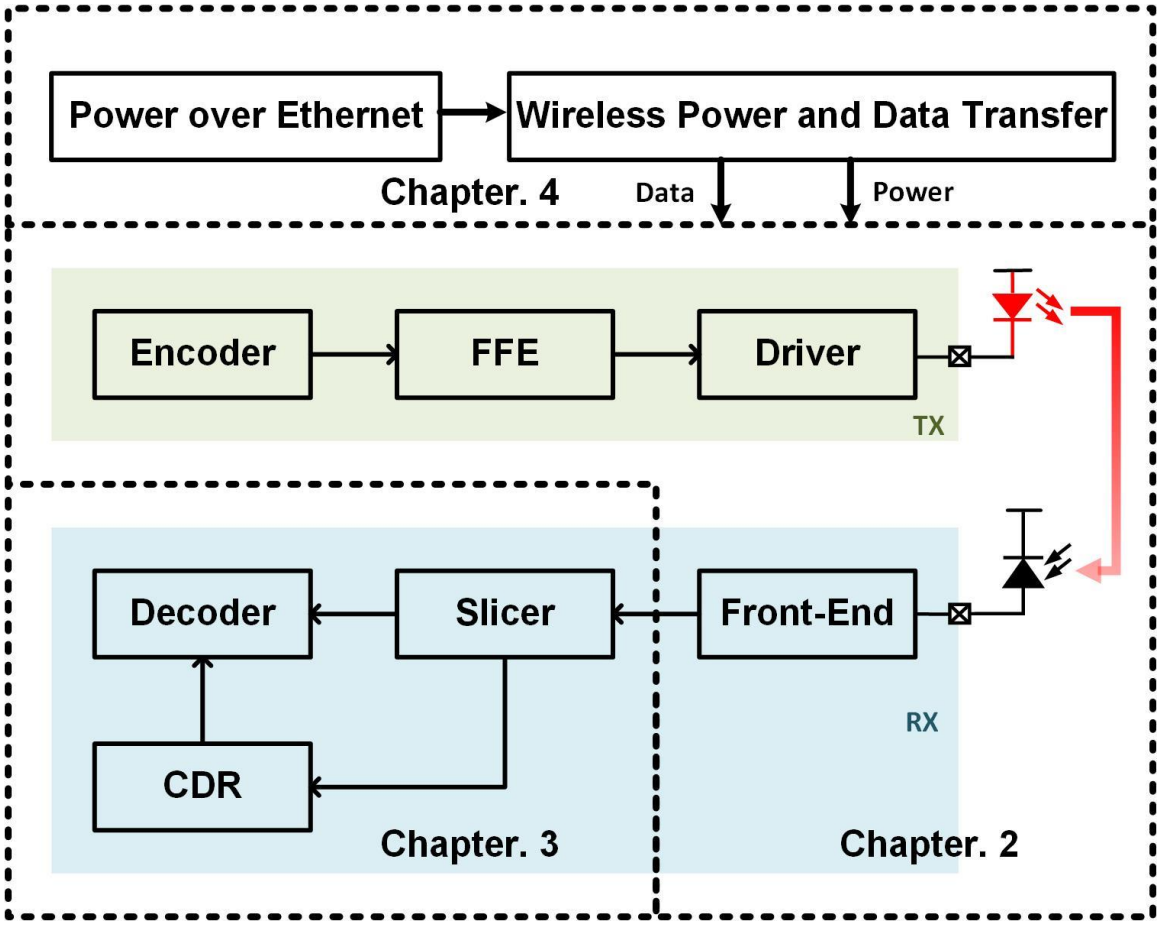

Figure. 1. 5. Thesis organization.

connecting the ToR, aggregation switches, and core switches, with a distance up to 10 km. In the next generation Ethernet, the directly-modulated-laser transceiver will be replaced with silicon-photonic-based transceiver, which will provide smaller form factor and higher connection density.

1.3. Thesis Organization

This thesis consists of three main portions. In chapter 2, an RGB PAM-4 optical wireless communication transceiver system is presented. Feed-forward equalization-based pre-equalization and continuous-time linear equalizer (CTLE) based post-equalization is proposed to extend the highest achievable data rate and compensate for the LED device nonlinearity. Chapter 3 focuses on the clock and data recovery (CDR) system for the optical wireline communication system. A complementary jitter compensation CDR architecture is proposed to decouple the trade-off between jitter transfer and jitter tolerance bandwidth. Finally, the bandwidth extension methodologies proposed in the previous two chapters are extended into a wireless power and data transfer system. A three-stage cascaded CTLE is implemented on the receiver side enabling variable channel bandwidth compensation.

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Chapter 2 Design of a RGB PAM-4 Optical Wireless Communication Transceiver System

2.1. Introduction

Optical wireless communication (OWC) technology employing light-emitting diodes (LEDs) as light sources has the advantages of using the license-free spectrum, being power and cost-efficient and having high security. However, common LED devices have the limitations of narrow bandwidths, nonlinear optical and frequency responses over different bias current levels, which cause inter-symbol interference and signal distortion, especially under high order modulation schemes with large current swings. In view of this, a compact PAM-4 OWC transceiver system employing a white LED as the light source with pre- and post-equalization is proposed. The white LED consists of a red, a green and a blue LED unit (RGB LED). Controlled by 3-bit thermometer codes, three separate drivers with feed-forward equalizers (FFEs) drive the RGB LED units to produce the PAM-4 optical signal. The driving currents from the three drivers with FFEs can be calibrated using digital and analog tunings to eliminate the differences in optical and frequency responses of the RGB LED units. A cascaded continuous-time linear equalizer (CTLE) is used at the receiver side as post-equalization to compensate for the narrow bandwidth of LED units. Based on experimental results, the proposed RGB PAM-4 OWC system can improve the highest achievable data rate by 1.67 times from 28 Mb/s to 75 Mb/s using the pre- and post-equalization scheme.

2.2. Research Background

Over the past few years, there has been an increasing demand for smart Internet-of-Things (IoT) devices, such as tablet computers, smart watches, glasses, speakers, and domestic robots, which requires ubiquitous wireless communication accesses, and results in severe radio frequency (RF) spectrum congestion. Therefore, there has been a strong desire to explore the optical spectrum for wireless communication applications. Using the optical spectrum in the visible range with a wavelength from 400 nm to 700 nm, Optical wireless communication (OWC) technology transmits data by modulating a light-emitting diode (LED) to generate an optical signal, and receives the signal using a photodiode (PD). Compared to RF

communication, OWC technology has the advantages of having a wide unlicensed spectrum, being power and cost-efficient, and having high security [1-6]. Additionally, with the widespread usage of LEDs in various applications scenarios, such as illuminations [7], display [8] and signage [9], the OWC functions can be supported using the existing LED infrastructures and achieve a wide range of IoT applications, such as indoor communications [10-12], broadcasting [13], high-precision location [14-15] and intra-vehicle communications [16]. Furthermore, benefit from the high-power LED devices in illumination and display systems, the signal-to-noise ratio (SNR) of the OWC optical signals can be much stronger compared to RF signal, which potentially supports higher order modulation schemes and longer transmission distances.

A typical OWC system is presented in Figure. 2. 1 (a). The baseband receives the signal from the data source and performs the source and channel encodings. Controlled by the encoded

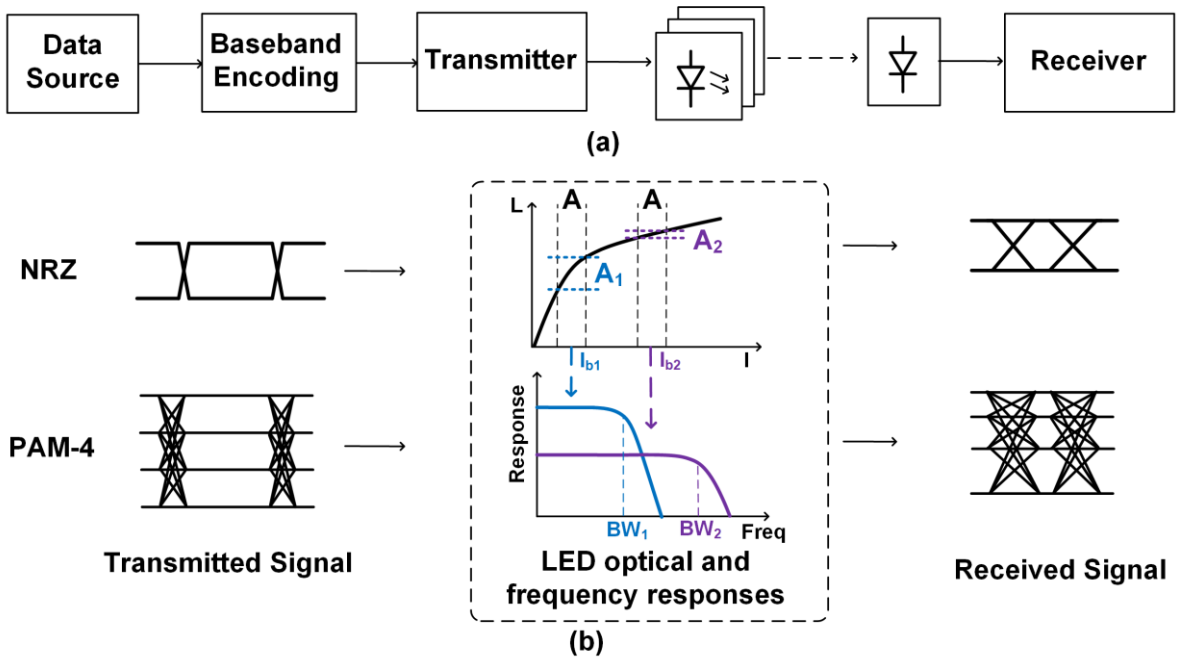

Figure. 2. 1. Research background.

(a) Typical system architecture of an OWL system. (b) Effects of LED non-ideal characteristics on NRZ and PAM-4 signal transmissions, such as narrow bandwidth, nonlinear optical response and frequency response.

data, the transmitter (Tx) modulates the LED current to produce the optical signal. After transmission through free space, the optical signal is converted back to an electrical signal using a PD at the receiver (Rx). The received signal is then equalized, amplified and decoded to recover the original data.

In order to achieve higher data rate in OWC technology, the design of the transceiver system is critical in serving as the interface between the LED devices and the data sources. Various research efforts have been devoted to the transceiver designs with bandwidth extension techniques. A high-speed LED driver supporting OWC function was demonstrated to increase the data rate by 88% from 27.5 Mb/s to 51.8 Mb/s by sweeping out the remaining carriers in LED devices [7]. A OWC Tx system-on-a-chip (SoC) integrating a baseband digital processing unit using white LEDs as the light sources was proposed in [17] and [18], which supported on-off keying (OOK) modulation and variable pulse-position modulation (VPPM). A 24-Mb/s CMOS OWC Rx SoC supporting OOK modulation with a post-equalization and an ambient light rejection function was reported in [19]. A complete OWC transceiver enabling an interactive software module control was also demonstrated in [20]. [21] presented a low power CMOS Rx for plastic optical fiber (POF) communication with a line equalizer as post-equalization to extend the channel bandwidth.

In addition to OOK and VPPM modulations, OWC systems supporting higher order modulation schemes have also been reported with off-the-shelf equipment platforms such as using 4-level pulse-amplitude modulation (PAM-4), M-quadrature amplitude modulation (M-QAM) and carrierless amplitude and phase (CAP) modulation [22-24]. A duobinary transceiver in 0.13-μm SOI CMOS was demonstrated in [25], which doubled the data rate compared to NRZ data transmission. A pre-distortion scheme was proposed for PAM-2 and PAM-4 signals to enhance the OWC transmission performance [26]. However, there has been lack of the circuit level innovations to support high-level modulation schemes, which are critical in compensating for the LED device non-ideal characteristics and achieving robust and compact OWC systems.

To implement PAM OWC transceiver systems at the circuit level, various non-ideal factors need to be considered. First, the typical commercial LED modulation bandwidth is around 10 MHz due to the large parasitic capacitance. Second, due to the LED device nonlinear

characteristics, the frequency responses and optical responses can vary when an LED is biased at different DC current levels. As illustrated in Figure. 2. 1 (b), under a same input driving current swing A, when biased under different current levels I_{b1} and I_{b2}, the LED output optical signals can have different amplitudes (A_1 and A_2) and bandwidths (BW_1 and BW_2). Therefore, when a large driving current is applied to the LED for supporting high order modulation scheme, the output optical signal waveform can be distorted. A few previous researches have proposed to employ optical domain digital-to-analog converter architecture to compensate for the nonlinear LED characteristics. [27] implemented a 5-bit optical wireless Tx using discrete power level stepping, which could support 2-, 4- and 16-QAM signals under 12, 24 and 48 Mb/s, and OFDM signal with good linearity. [28] summarized the ideas of optical domain digital-to-analog converter architectures, such as hybrid optical/electrical domain converter and dimming method. [29] divided the OFDM subcarriers into groups and transmitted the divided groups separately through an LED array. [30] employed 4 mLEDs to produce PAM-16 signal at 6.25 Gb/s data rate over 10 m plastic optical fiber with offline equalization. However, when multiple LEDs are employed to achieve high order modulation, the differences in the LED frequency and optical responses, the distance from each LED to the Rx, and the responses of the PD to different LEDs can still cause distortion to the received signal, as shown in Figure. 2. 1 (b).

In this work, a PAM-4 OWC transceiver system-on-a-module (SOM) is proposed using feed-forward equalization (FFE) and a cascaded continuous-time linear equalizer (CTLE) as the pre- and post-equalization, respectively. A white LED consisting of a red, a green and a blue LED unit (RGB LED) is used as the light source. Each of the three LED units is driven by an individual main driver with an FFE driver and contributes to one of the three eyes in the optical PAM-4 signal. The three separate main drivers with FFE drivers can not only extend the narrow LED bandwidth, but can also eliminate the differences in the optical and frequency responses of the RGB LED units. The cascaded CTLE on the Rx side provides smooth and wide-range bandwidth compensation to further extend the highest achievable data rate. The OWC Tx and Rx occupy 10 × 10 cm, and 6 × 6 cm areas, respectively. Experimental results demonstrate that the proposed system can compensate for the RGB LED units nonlinear characteristics, and support high quality PAM-4 optical signal transmission with equally distributed eye openings. The highest achievable PAM-4 data rate can be extended by 1.67 times from 28 Mb/s up to 75 Mb/s using the proposed pre- and post-equalization.

2.3. PAM-4 Optical Wireless Communication System Architecture

As shown in Figure. 2. 2, the complete PAM-4 OWC system consists of a Tx with RGB LED units and a Rx. On the Tx side, 2-bit binary codes including the most significant bit (MSB) and least significant bit (LSB) are generated in baseband as data sources. The 2-bit binary codes are converted into 3-bit thermometer codes (T-codes) to control the three main NRZ drivers for the RGB LED units. The 3-bit T-codes are to represent a natural number, N ($0 \leq N \leq 3$), using N bits of ones, followed by zeros. The mapping table from a natural number, to 2-bit binary codes and 3-bit T-codes is illustrated in Figure. 2. 2 (b). Driven by the three main NRZ drivers, the RGB LED units generate three NRZ optical signals with the same amplitude. The intensities of the three optical signals will superpose each other linearly in free space, which produces a PAM-4 optical signal. By using the T-codes to control the three NRZ drivers for the RGB LED units, the four levels of the PAM-4 optical signal correspond to the

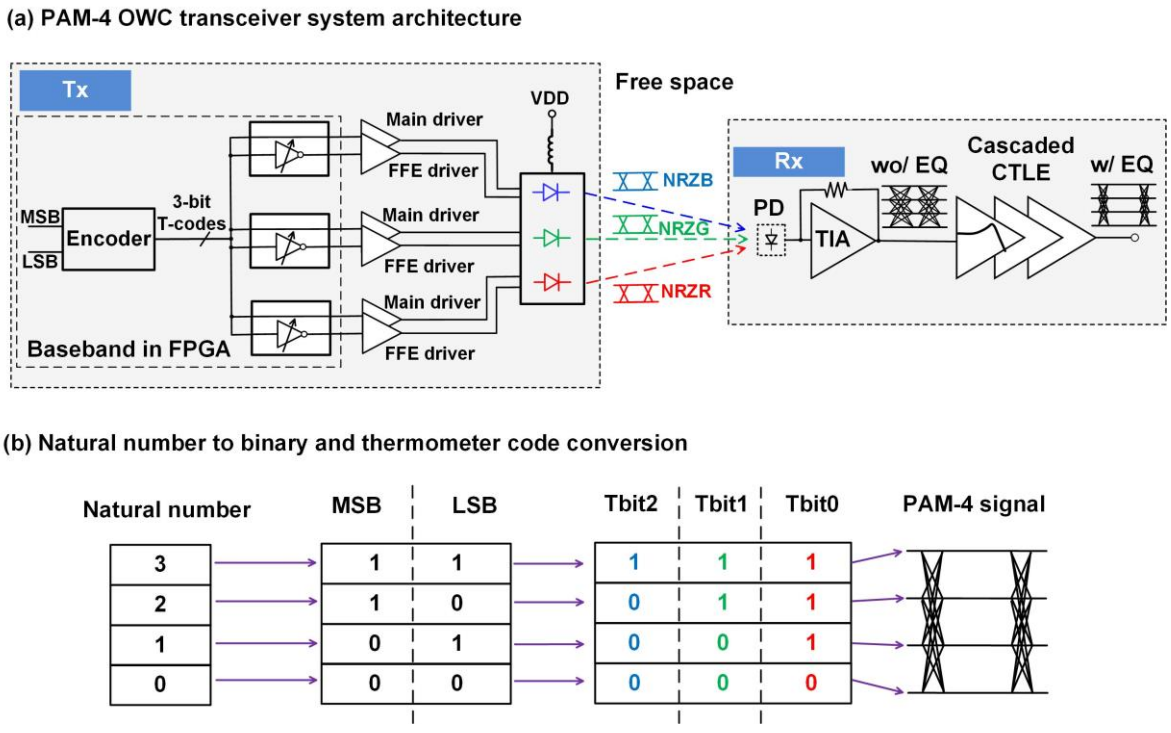

Figure. 2. 2. Architecture and principle of the proposed OWC transceiver system.

(a) Architecture of the proposed PAM-4 OWC transceiver system. (b) Mapping rule from a natural number to 2-bit binary codes and 3-bit thermometer codes.

numbers of LED units with output optical signal '1'. The optical signals from the RGB LED units contribute to the three eyes in the PAM-4 optical signal, respectively. In addition, for each LED unit, an FFE driver is implemented with the main driver to produce a driving current with pre-emphasis, which can extend the LED unit bandwidth. Therefore, with the proposed Tx architecture, the differences in optical responses of the RGB LED units and PD spectrum responses can be eliminated by adjusting the three main driving current amplitudes individually. The differences in frequency responses of the three LED units can also be compensated by tuning the pre-emphasis strengths of the three FFE drivers individually.

On the Rx side, the optical PAM-4 signal is converted back to an electrical signal by a high-

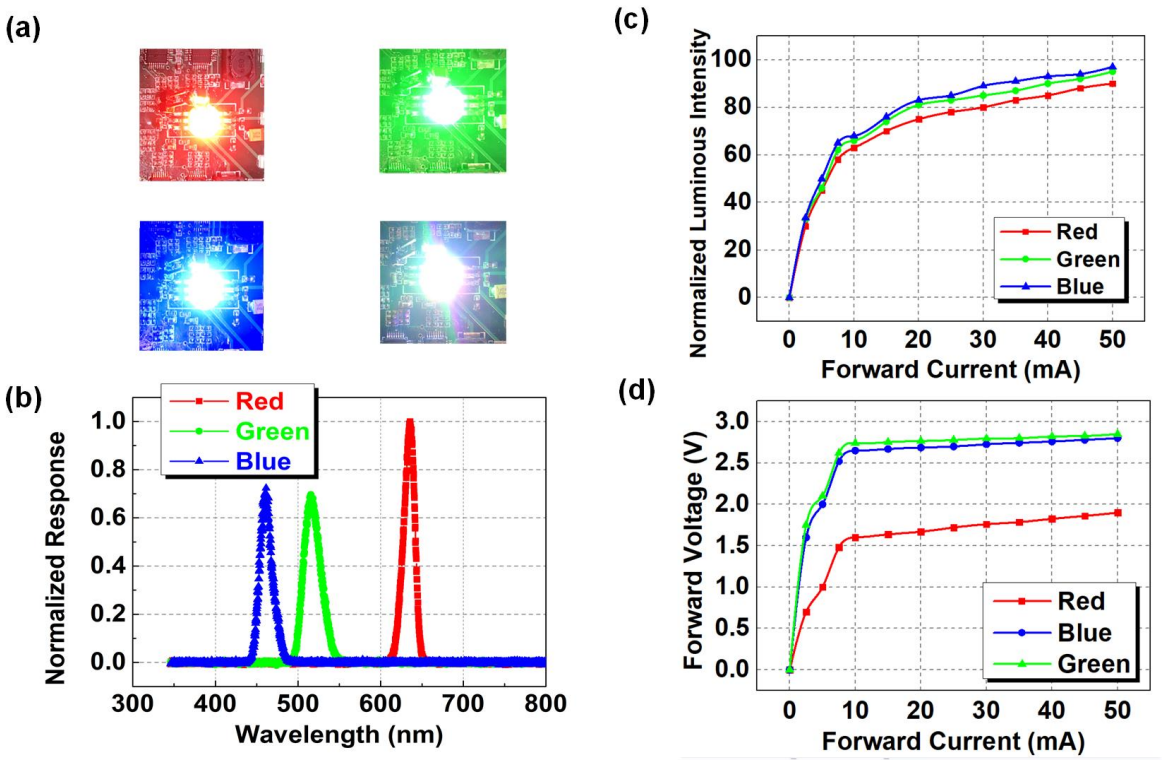

Figure. 2. 3. Light sources for the OWC system.

(a) Pictures of the white LED consisting of a red, a green and a blue LED unit. (b) Measured optical spectrums of the RGB LED units. (c) and (d) Measured normalized L-I and V-I characteristics of the RGB LED units.

speed p-i-n PD and trans-impedance amplifier (TIA). A cascaded continuous-time linear equalizer (CTLE) provides further bandwidth extension to the received PAM-4 signal to extend the limited LED unit bandwidths.

2.4. System Implementation

This section provides implementation details on the employed light sources, PD, Tx and Rx circuits.

The light source is a commercially available white LED consisting of a red, a green and a blue LED unit placed close to each other. The three LED units together consume a total power of around 0.15 W under proper thermal control. The light intensities of the three LED units can be controlled individually at the Tx board. White light can be generated by adequately mixing the RGB lights, as shown in Figure. 2. 3 (a). The spectrums of the three LED units are measured and presented in Figure. 2. 3 (b), which indicates that the wavelengths of the RGB lights are located at 630 nm, 515 nm and 460 nm respectively. The normalized L-I and V-I responses of the three LED units are shown in Figure. 2. 3 (c) and (d).

The intrinsic frequency responses of the three LED units are characterized based on the PAM-

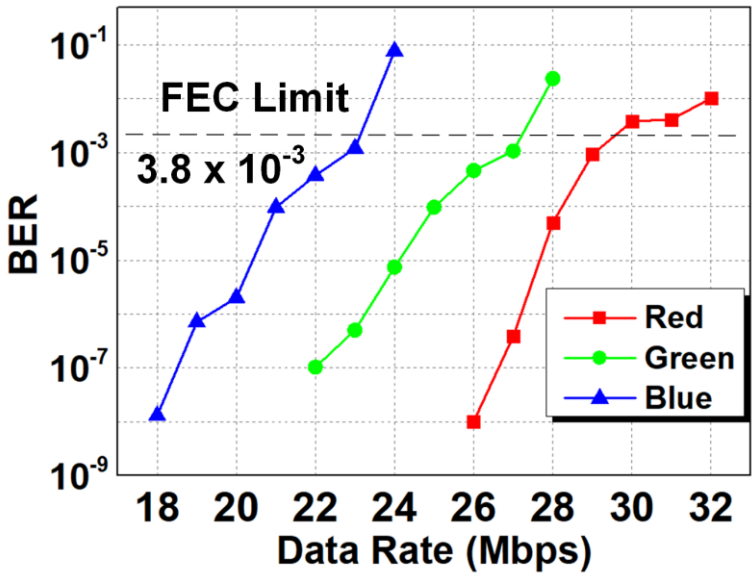

Figure. 2. 4. Measured BERs under different data rates of the RGB LED units

4 OWC system presented above without enabling the pre- and post- equalization. A pseudo-random binary sequence-7 (PRBS-7) is used as an input testing data pattern, and each LED unit is enabled and characterized separately. On the Rx side, the output of the Rx is collected

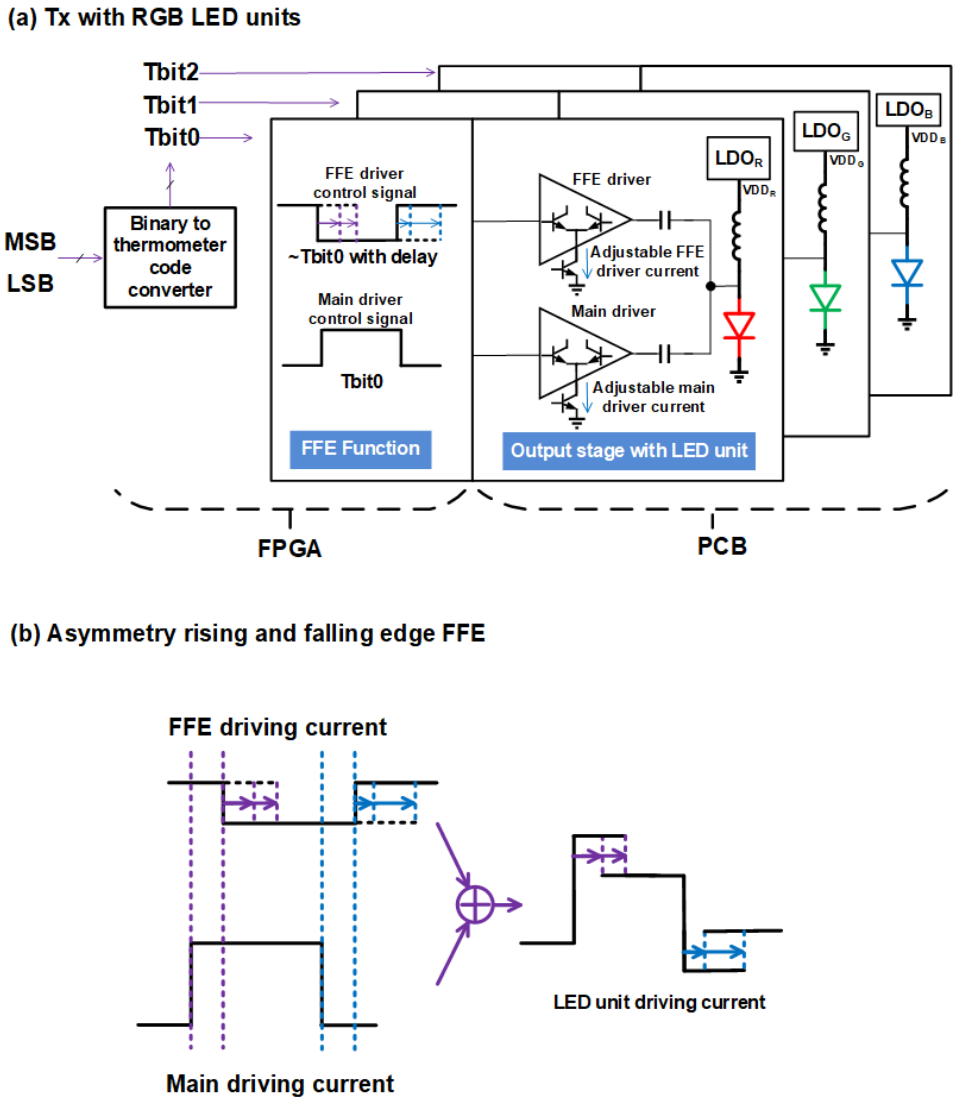

Figure. 2. 5. Proposed architecture and asymmetric FFE.

(a) Architecture of the proposed Tx including the main drivers and FFE drivers. (b) Principle of the asymmetry rising and falling edge FFE.

using an oscilloscope for plotting the eye diagrams and calculating the bit-error-rates (BER). The measured BERs of the three LED units under different data rates are presented in Figure. 2. 4. Based on a forward-error-correction (FEC) limit of 3.8×10^{-3}, the results indicate that the

highest achievable data rates of the RGB LED units are 29.5 Mb/s, 27.0 Mb/s and 23.5 Mb/s, respectively. The Nyquist frequencies of the highest achievable data rates are approximately equal to the LED unit bandwidths. Therefore, individual bandwidth extension is needed to compensate for the differences in frequency responses of the three LED units. It worth mentioning that, although red LED unit provides the highest data rate in our case, it is not a general rule. The optical bandwidth of each LED is determined by the individual device structure, including junction capacitance and carrier density.

As shown in Figure. 2. 5 (a), the proposed PAM-4 OWC Tx consists of two parts, a baseband implemented in FPGA responsible for data format conversion and FFE code generation, and a Tx module implemented on a printed circuit board (PCB) including the LED drivers, FFE circuits and low dropout regulators (LDOs).

The baseband generates the 2-bit binary MSB and LSB codes and converts them into 3-bit T-codes, consisting of Tbit0, Tbit1 and Tbit2. Each of the three main drivers is controlled by one of the T-codes to provides the main driving current for one of the RGB LED units. In addition to the main drivers, three FFE drivers, controlled by the 3-bit inverted and delayed ~T-codes, consisting of ~Tbit0, ~Tbit1 and ~Tbit2, produce three FFE currents, as shown in Figure. 2. 5 (a). The output currents from each main driver and the corresponding FFE driver add together and generate the LED unit driving current with fractional pre-emphasis, as shown in Figure. 2. 5 (b). The pre-emphasis peak widths are set by the delays between the T-codes and ~T-codes, while the pre-emphasis peak heights are determined by the amplitudes of the FFE currents. Wider delays between the T-codes and ~T-codes and larger FFE current amplitudes can deliver higher FFE strengths, which also degrade the optical signal SNR.

To control the pre-emphasis peak widths flexibly, an external clock at 20 times the symbol rate is provided to the baseband FPGA from a signal generator. The pre-emphasis peak widths can thus be fine-tuned with a step size equal to 1/20 of the symbol period, T_s. The ratio of the peak width versus the symbol period, R_{p2s}, sets the compensating frequency [31]. R_{p2s} is determined based on the measured highest achievable data rate of each LED units (D_{LEDU}) from Figure. 2. 4, and the target symbol rate (S_T). In experiment, R_{p2s} is initially set close to D_{LEDU}/S_T and then fine-tuned for the rising and falling edges to achieve the lowest BER [31].

For each of the LED unit, both main driver and FFE driver are implemented with max3668 devices with current steering architectures. The upper limit for the driving current amplitude is set by the LED unit bias current of around 15 mA. A driving current amplitude higher than 15 mA causes the signal crossing level to deviate from the middle. The lower limit for the

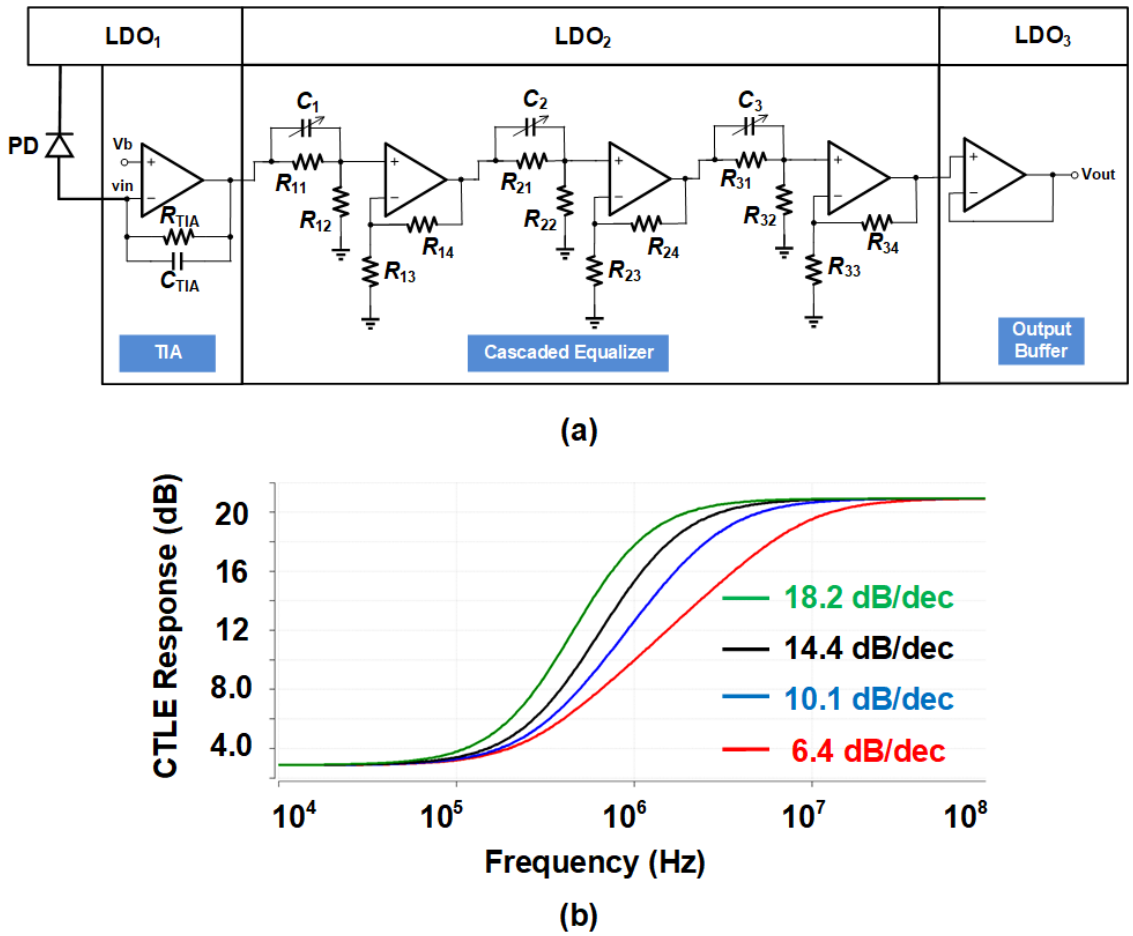

Figure. 2. 6. Architecture and simulation results of the proposed OWC receiver.
(a) Architecture of the proposed OWC receiver. **(b)** CTLE frequency responses with different rising slopes under different degeneration resistors and capacitors configurations.

driving current amplitude is constrained by the optical receiver sensitivity. The main driver current and FFE driver current are determined experimentally to obtain a wide bandwidth extension without over-degrading the SNR.

Due to the LED nonlinearity, the rising and falling edges of the optical signal are generally asymmetric. Therefore, the FFE is designed so that the peak widths on the rising and falling edges of the driving current can be controlled individually, which provides flexible equalization to the two edges, as shown by the purple and blue dashed lines in Figure. 2. 5 (b). This is achieved in the baseband algorithm, which enables the rising and falling edges of the ~T-codes to have individual delay controls.

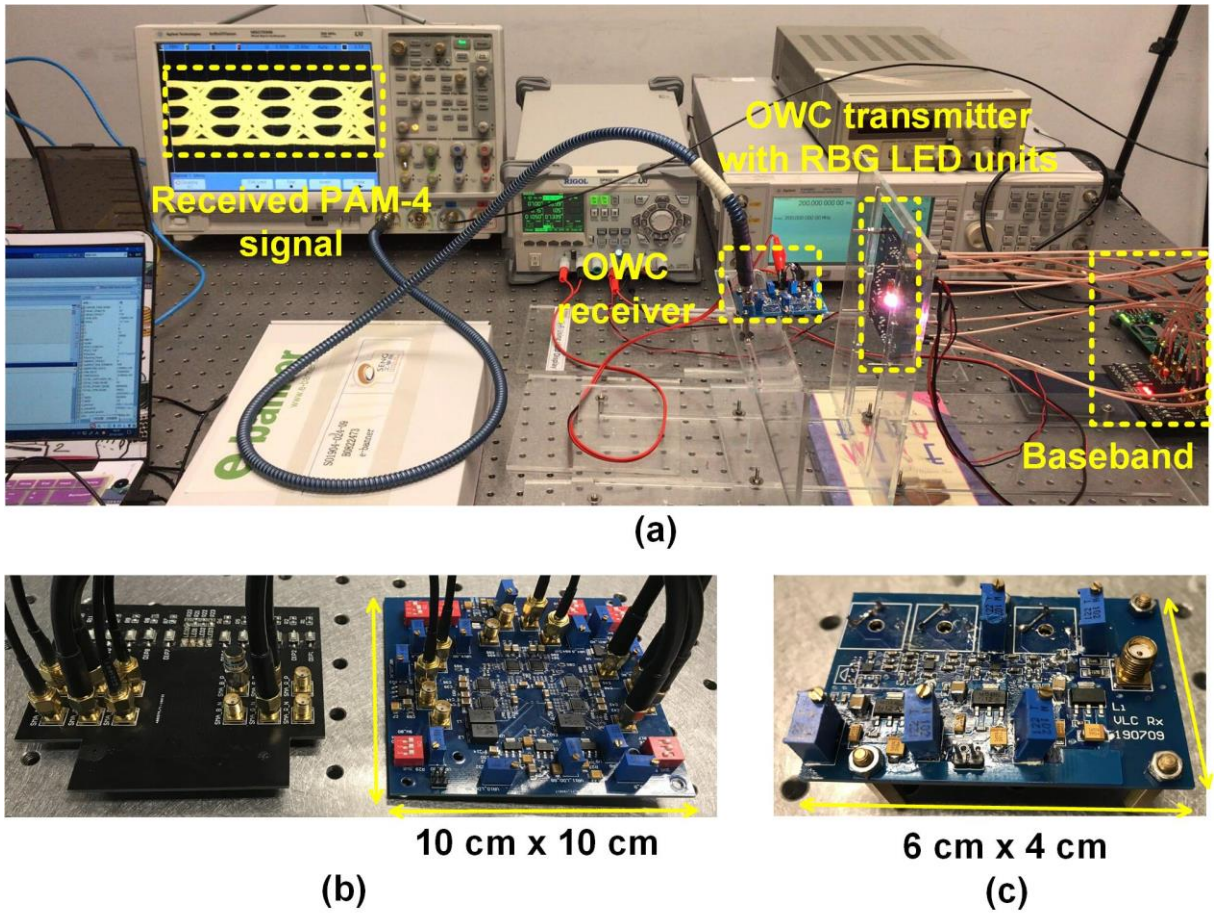

Figure. 2. 7. Experimental setup.

(a) Experimental setup of the PAM-4 OWC testing system. (b) PAM-4 OWC Tx with baseband. (c) OWC Rx.

The OWC transmitter feeds the output driving currents into the RGB LED units at the positive nodes, which are connected through three choke inductors with small DC resistances to the LDO outputs, as shown in Figure. 2. 5 (a). In this way, the DC operating points can be

set flexibly by adjusting the LDO output voltages, which ensure the LED units are biasing at the DC levels with the largest bandwidths.

The schematic of the OWC Rx is presented in Figure. 2. 6 (a). It consists of a high-speed PD, a TIA, a cascaded CTLE and an output buffer. The TIA employs an inverter-based architecture with a large trans-impedance resistor of 15 KΩ, which provides a trans-impedance gain of around 83 dBΩ and bandwidth of around 18 MHz. The relatively narrow TIA bandwidth is extended by the following cascaded CTLE up to 25 MHz in order not to limit the overall Rx bandwidth. The small capacitor C_{TIA} of around 200 fF is implemented with a trimmable parallel matal strips on the PCB top layer, which is used in parallel with the trans-impedance resistor R_{TIA} to stabilize the TIA from oscillation. Considering the PD can produce a DC optical current due to the LED bias current, ambient light and dark current, V_b on the positive node of the TIA is adjusted to compensate for the DC offset at the TIA output.

The cascaded equalizer consists of three first-order CTLEs with the same RC degeneration architecture to provide tunable bandwidth compensation to the received PAM-4 signal and the TIA [32]. As shown in Figure. 2. 6 (a), taking the first stage CTLE as an example, the high pass filter composed of R_{11}, C_1 and R_{12} at the positive input node of the core amplifier suppress the low-frequency gain and produce a rising frequency response, which compensates for the low-pass filtered PAM-4 signal spectrum due to OWC system bandwidth limitation. The CTLE frequency response is presented below:

$$H_{CTLE}(j\omega)=\frac{R_{eq13}+R_{eq14}}{R_{eq14}}\cdot\frac{R_{eq12}}{R_{eq11}+R_{eq12}}\cdot\frac{1+j\omega C_{eq11}R_{eq11}}{1+j\omega C_{eq11}(R_{eq11}//R_{eq12})} \quad (1)$$

The equation indicates that a zero is created from the degeneration capacitor C_1 and resistor R_1, which produces the peaking in the simulated frequency response shown in Figure. 2. 6 (b). The peaking frequency and height can be controlled by tuning the degeneration resistors and capacitor in each CTLE stage and thus different frequency response rising slopes can be produced, as presented in Figure. 2. 6 (b), which provides flexible and wide range bandwidth compensation. The equalized signal is buffered using a voltage follower and sent to the oscilloscope for waveform collection. The complete Rx can achieve an optical sensitivities of -34.30 dBm, -33.15 dBm and -32.28 dBm for 630 nm, 515 nm and 460 nm light wavelengths

of the RGB LED units, towards the FEC limit of 3.8×10^{-3}. The parameters of all devices employed in the transceiver are shown in Table 2. 1.

The proposed system employs FFEs at the Tx as the pre-equalization and a cascaded CTLE at the Rx side as the post-equalization. Based on the previous analysis, the cascaded CTLE at the Rx side can only perform uniform equalization to the entire received PAM-4 signal, while the three separate FFEs at the Tx are capable of optimizing the three eyes of the PAM-4 signal individually. Therefore, a two-step equalization tuning scheme is proposed to achieve the optimal bandwidth extension. First, the peaking frequency and the equalization strength of the cascaded CTLE on the Rx side are optimized to compensate for the narrow bandwidths of the LED units and the TIA by adjusting the degeneration resistors and capacitors. Second, the FFE current amplitudes and the delays between T-codes and ~T-codes are tuned to extend the bandwidths of the RGB LED units up to the same frequency. The complete equalization process will be demonstrated in Section. IV.

2.5. Measurement Results

Table 2. 1 Component Parameters

Parameters	Values	Parameters	Values
PD	S10784	C_1~C_3	Variable from 20~100 pF
TIA core amplifier	OPA855	R_{11}	470 Ω
CTLE core amplifier	OPA859	R_{12}	470 Ω
LED Driver	MAX3668ehj	R_{13}	470 Ω`
LDO	LM1117IMP-adj	R_{14}	Variable from 100 ~ 1000 Ω
Choke inductor	100 uH	TIA capacitor	200 fF (estimated)
TIA resistor	15 KΩ		

The experimental setup of the PAM-4 OWC system is presented in Figure. 2. 7 (a). The signal generator provides a synchronized clock to the baseband, which clocks the PRBS generation, binary-to-thermometer conversion, and the digital control of the FFE delay implemented in the FPGA. The two PRBS-7 data patterns generated within the baseband are used as the MSB and the LSB testing data for the Tx. The PRBS-7 pattern provides a good approximation to

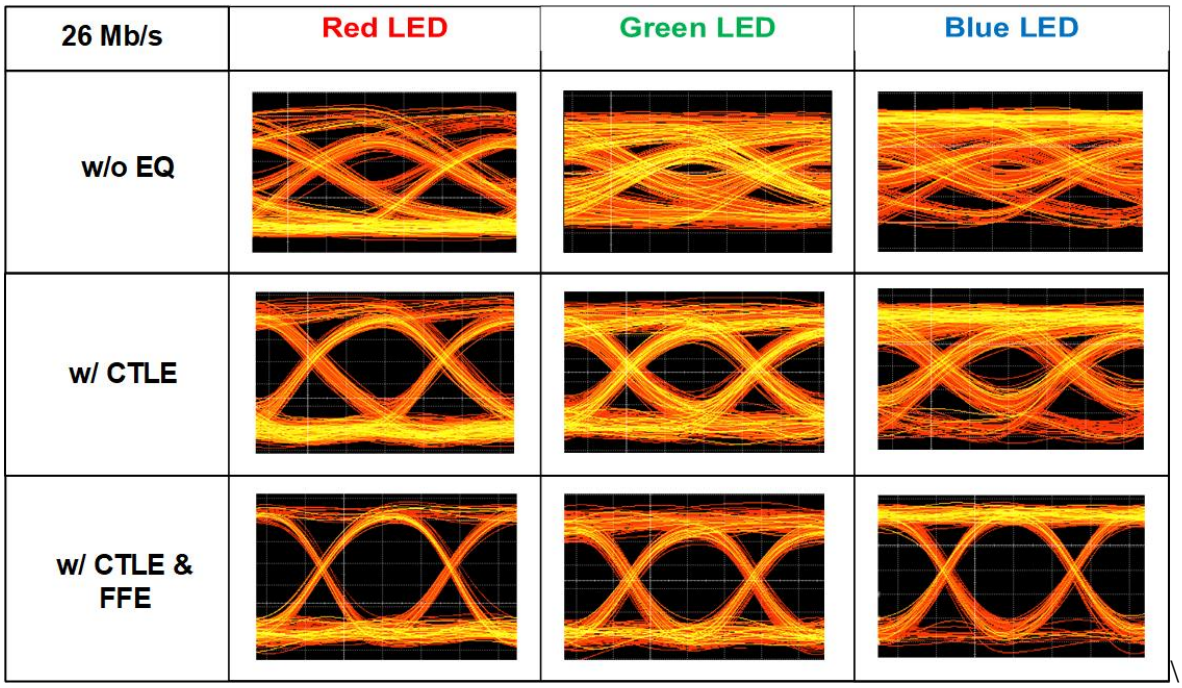

Figure. 2. 8. Measured eye diagrams at 26 Mb/s for the RGB LED units under the three different equalization configurations: without equalization, with CTLE only, and with both CTLE and FFE.

the 4B/6B, 8B/10B or Manchester encoding schemes used in display or illumination based OWC systems for signal DC balance and fast clock recovery. The Rx output signal is collected with RTO1044 oscilloscope with 4-Gsample/s sampling rate and used for BER calculation in MATLAB. The three threshold voltages used for decoding the received PAM-4 signal are fixed at the middle voltage levels of the three eyes for obtaining the widest sampling headroom. By sweeping over one symbol period, the sampling point is determined to provide the highest vertical eye opening. The received analog PAM-4 signal is first decoded into 3-bit T-codes and then converted to 2-bit binary codes using the three threshold voltages and sampling point. After matching the decoded data with PRBS-7 pattern to get the

starting bit, the offline program continuously calculates the BER for MSB and LSB until the BER value converges. For each BER level, the number of accumulated bits are typically higher than 20 times 1/BER.

The baseband is implemented on the Virtex-7 FPGA platform, and the output 3-bit T-codes and 3-bit ~T-codes are connected to the OWC Tx board using six coaxial cables. A heat sink is assembled on the Tx PCB close to the LED units with thermal paste to protect the LED units and driver circuits. The transmission distance between the Tx and Rx PCBs can vary from 5 cm to 10 cm depending on the LED output power. After the optical signal is received, equalized and buffered, it is fed into an oscilloscope, where the waveform is collected and processed offline to calculated the BERs and plot the eye diagrams. The transmitter and Rx boards are shown in Figure. 2. 7 (b) and (c), respectively.

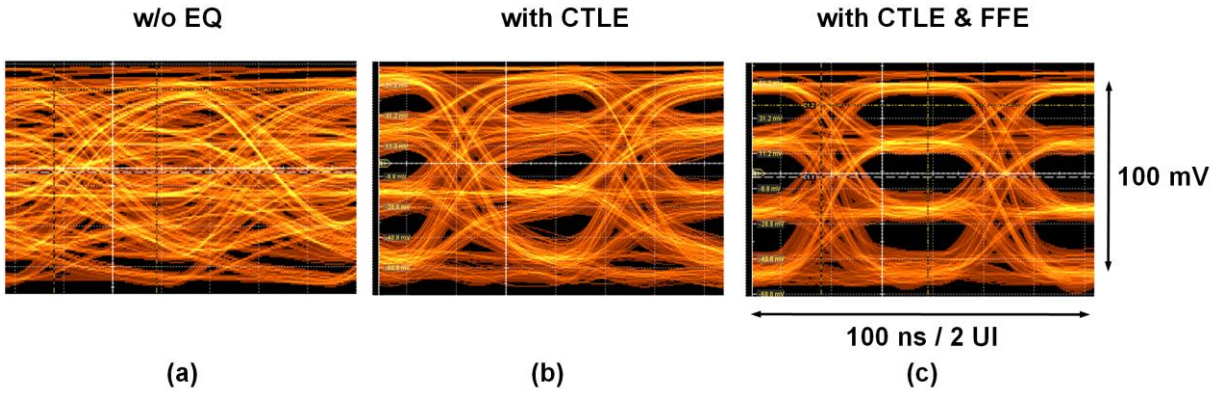

Figure. 2. 9. Measured PAM-4 eye diagrams at 50 Mb/s at around -16.5 dBm received optical power under different equalization configurations.

(a) PAM-4 eye diagram with no equalization enabled. (b) PAM-4 eye diagram with only CTLE enabled. (c) PAM-4 eye diagram with both CTLE and FFE enabled.

The effects of the pre- and post- equalizers on the NRZ data transmission using each LED unit are demonstrated first. Using the proposed system, only one of the RGB LED units is turned on each time to investigate the data transmission capability under different equalizer configurations.

First, the FFE at the Tx is turned off, and only the first stage CTLE is enabled to compensate for the TIA bandwidth. Under this condition, the highest achievable data rates are limited by the LED units' bandwidths. The received eye diagrams from the RGB LED units are presented in the first row of Figure. 2. 8. Under the data rate of 26 Mb/s, the eye diagram of the red LED unit is still open while that of the blue LED unit has been completely closed, which is consistent with the BER measurement results presented in Section. III. Next, the other two stage CTLEs are enabled and provide equal equalization strength to the RGB LED units. The measured eye diagrams in the second row of Figure. 2. 8 (b) show that the received signal qualities of all three LED units are significantly improved compared to the previous condition. However, the horizontal and vertical eye openings of the three LED units are still markedly different from each other, which can distort the optical signal in PAM-4 signal transmission. Finally, after the FFEs and cascaded CTLE are enabled together, the widest bandwidth extension is achieved and the bandwidth differences between the three LED units are almost eliminated. The measured eye diagrams are presented in the third row of Figure. 2. 8 (c), which shows that the eye qualities of all three LED units have been enhanced to almost the same level, and the eye openings are much wider than the previous two cases. The highest, middle and lowest level FFE strength are applied to the blue, green and red LED units respectively.

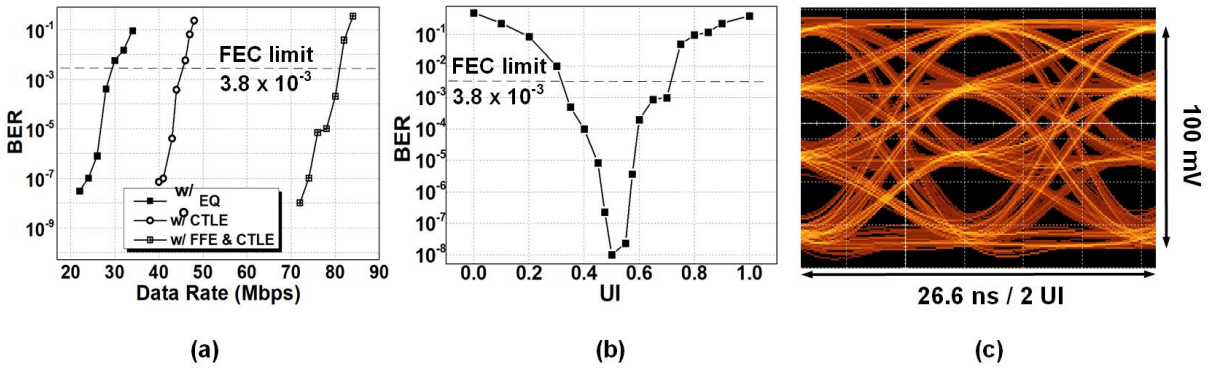

Figure. 2. 10. Measured BER improvement with pre- and post- equalization.

(a) Measured BERs for PAM-4 data transmission under different equalization configurations. (b) Measured bathtub curve at 75 Mb/s. (c) 75 Mb/s eye diagram with around -16.5-dBm received optical power.

The PAM-4 data transmission performance is verified with the measured eye diagrams, BERs and bathtub curve with RGB LED units enabled together.

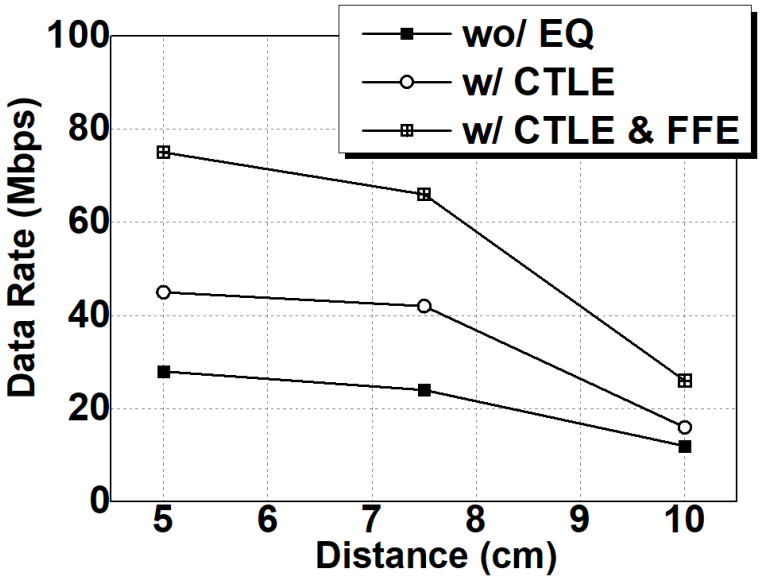

Figure. 2. 11. Measured highest achievable data rates under different transmission distances.

In the PAM-4 data transmission, each LED unit generates a NRZ optical signal and contributes to one of the eyes in the PAM-4 optical signal. However, since there are in total 12 different transitions among all four levels in the PAM-4 signal, the distortion or bandwidth limitation of each eye will couple with the other two eyes. Therefore, the overall PAM-4 signal quality is limited by the LED unit with the lowest bandwidth. In addition, the PAM-4 signal quality is also sensitive to the over- and under-shootings in each transition. Therefore, the FFE and cascaded CTLE need to be carefully adjusted to obtain adequate equalization with a combination of the digital and analog tuning methods. The measured PAM-4 eye diagrams at 50 Mb/s are presented in Figure. 2. 9 (a), (b) and (c) under the configurations of no equalization enabled, only the cascaded CTLEs enabled, both FFE and cascaded CTLE enabled, respectively. The measurement results show that a completely closed PAM-4 eye in Figure. 2. 9 (a) can be openned with the help of only the cascaded CTLE shown in Figure. 2. 9 (b). By enabling FFE and cascaded CTLE together, a widely-opened and equally-distributed eye diagram can be achieved shown in Figure. 2. 9 (c), which ensures error-free data decoding.

The output data from the Rx is collected from the oscilloscope and processed offline. The collected data is synchronized, decoded, matched with the input PRBS-7 pattern and used to calculate the BER in MATLAB. The calculated BERs at different data rates under the three equalization configurations shown previously are presented in Figure. 2. 10 (a). The results demonstrates that the highest achievable data rate of the PAM-4 OWC system can be improved from 28 Mb/s to 46 Mb/s by only enabling the cascaded CTLE, and can be further increased up to 75 Mb/s with a combination of cascaded CTLE and FFEs, based on the FEC limit of 3.8×10^{-3} [33, 34]. The measured bathtub curve at 75 Mb/s shows a 0.4-UI horizontal data sampling headroom, which ensures the BER to be lower than the FEC limit. The corresponding eye diagram at 75 Mb/s is presented in Figure. 2. 10 (c).

The maximum achievable data rate at the transmission distances from 0.05 m to 0.1 m under the three equalization configurations are presented in Figure. 2. 11. The highest data rates are 75, 62 and 34 Mb/s respectively at 0.05, 0.075 and 0.1 m. Under the transmssion distance of 0.05 m, the highest achievable data rate is limited by the LED bandiwdth, while at 0.1 m, the data rate is mainly limited by the attenuated SNR. A performance comparison table is provided in Table 2. 2 summarizing the system architectures and bandwidth extension methods from similar work.

2.6. Conclusion

This work proposed a compact PAM-4 OWC transceiver SOM design employing three main drivers with FFE drivers to control the RGB LED units separately. The experimental results confirm that the proposed architecture can eliminate the differences in both optical and frequency responses of the RGB LED units. The cascaded CTLE on the Rx side further extends the narrow LED bandwidth and improves the highest achievable data rate. The overall SOM increases the highest achievable data rate by 1.67 times from 28 Mb/s to 75 Mb/s.

The proposed transmitter architecture can potentially be extended to support high power LED arrays and achieve long-distance communication. Since the output of the transmitter is current signal, it can drive multiple LEDs connected in series to provide a stronger output optical

signal power, as shown in Figure. 2. 12. Here we make two projections with a higher LED power budget for longer transmission distance.

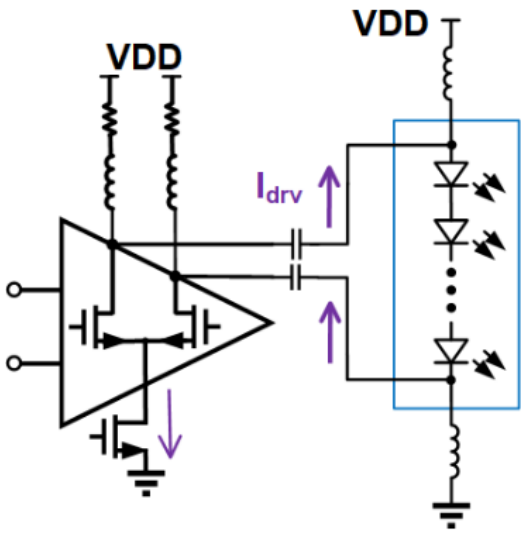

Figure. 2. 12. Using multiple LEDs to improve the optical signal intensity.

Without using a lens, the SNR is limited at long transmission distance. Therefore, the projection is made with reference to the SNR limited measurement results at 0.075m and 0.10 cm. At a distance of 1 m, a minimum LED driving power from 15 W to 17 W is required to support a data rate from 36 Mb/s to 62 Mb/s, based on the inverse relation between the LED driving power and square of the transmission distance.

By using a lens, considering a lens transmission ratio of 90%, diameter of 1 cm with short focal length, and PD effective photosensitive area of 7 mm^2, the SNR can be improved by 10.1 times. Therefore, referring to the measurement result at 0.05 m, an LED driving power of 6 W will be necessary to support a data rate of 75 Mb/s at 1 m distance.

The proposed Tx architecture can also support coarse wavelength division multiplex (WDM) or PAM-8 modulation. For WDM modulation, three sets of Rx circuits, PDs and color filters will be necessary to separate the three light wavelengths and obtain three parallel data transmission channels. For PAM-8 scheme, the output optical signal intensities of the RGB LED units should be configured to a ratio of 1:2:4, which requires around 4-times higher SNR compared to the presented PAM-4 OWC system.

2.7. References

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Table 2. 2 Comparison table for optical wireless communication

Ref	LED Driving Power (W)	LED Types/ Bandwidth	Architectures	Bandwidth Extension Methods	Transmission distances (m)	Data Rates (Mb/s)
[7]	0.300	Blue LED / 34.5 MHz*	Off-chip OOK current switch driver	Remaining carriers sweeps out	0.0150	95.0
[7]	0.0330	Blue LED / 13.7 MHz*	On-chip OOK current switch driver	Remaining carriers sweeps out	0.00500	51.8
[17]	16.0	White LED / 3 MHz	OOK current switch	None	2.05	2.50
[35]	80.0	White LED / None	Burst mode LLC converter	None	10.0	0.0470
[36]	8.00	White LED / None	OOK power switch	Keep and restore techniques with auxiliary switches	1.00	8.00
[37]	< 2 W**	Deep Blue LED / 10 MHz	Differential digital-to-Light conversion	64-QAM with off-line equalization	0.3	120
[38]	None	RGB LED /None	RGB color shift keying with 4-QAM DCO-OFDM	None	2	60***
This wor	0.150	RGB LED / 14.7, 13.5, 11.8 MHz for R, G, B LED units***	T-code controlled PAM-4 transceiver	FFE based pre-equalization and CTLE based post-equalization	0.0500	75.0

* and *** Estimated from the transmission of PRBS-7 pattern.
**Estimated from the LED operation power.

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Chapter 3 A 60 Gb/s PAM-4 Receiver with a Jitter Compensation Clock and Data Recovery

3.1. Introduction

This chapter presents a 60-Gb/s PAM-4 receiver (Rx) with a jitter compensation clock and data recovery circuit (JCCDR), supporting decoupled jitter transfer (JTRAN) and jitter tolerance (JTOL) under quarter-rate (1/4-rate) architecture. The proposed JCCDR adopts a first-order delay-locked loop (DLL) for wideband JTOL, a jitter compensation circuit (JCC) for JTRAN detection and suppression, and a 400-MHz second-order phase-locked loop for multi-phase clock generation. The JCC acquires the JTRAN information by detecting the DLL loop filter voltage *VLF*, and produces a complementary signal VLF_{INV} with the same amplitude but inverted phase as *VLF*. The VLF_{INV} modulates a group of complementary voltage-controlled delay lines connected at the DLL outputs to negate the JTRANs on both recovered data and clock signals. Prototyped in 40-nm CMOS, the proposed Rx achieves error free operation with PAM-4 signaling from 30 Gb/s to 60 Gb/s. The JCCDR is capable of supporting a 40-MHz JTOL bandwidth with a 0.2-UI_{PP} jitter amplitude, while maintaining an ultra-low <-8-dB JTRAN over all jitter frequency. A jitter compensation ratio up to 78% can be support from DC to 10 MHz, with a -3-dB corner frequency of 35 MHz.

3.2. Research Background

Driven by the proliferation of data intensive applications such as 5G communications, cloud services, autonomous vehicles, deep neural networks and 8K display panels, high speed and low power data movements from processors to processors and from processors to off-chip memories become crucial problems in high-performance computing (HPC) systems [1]-[3]. The explosive rise in processor I/O bandwidth demands for massive low-power links with advanced signaling schemes such as four-level pulse amplitude modulation (PAM-4) [4]-[7]. As the data rate reaches over 50 Gb/s/lane with PAM-4 signaling, the signal quality is getting increasingly susceptible to jitter generated from both channel and circuits. Therefore, the clock distribution circuit requires extra design efforts to handle the jitter issues and ensure robust system synchronization.

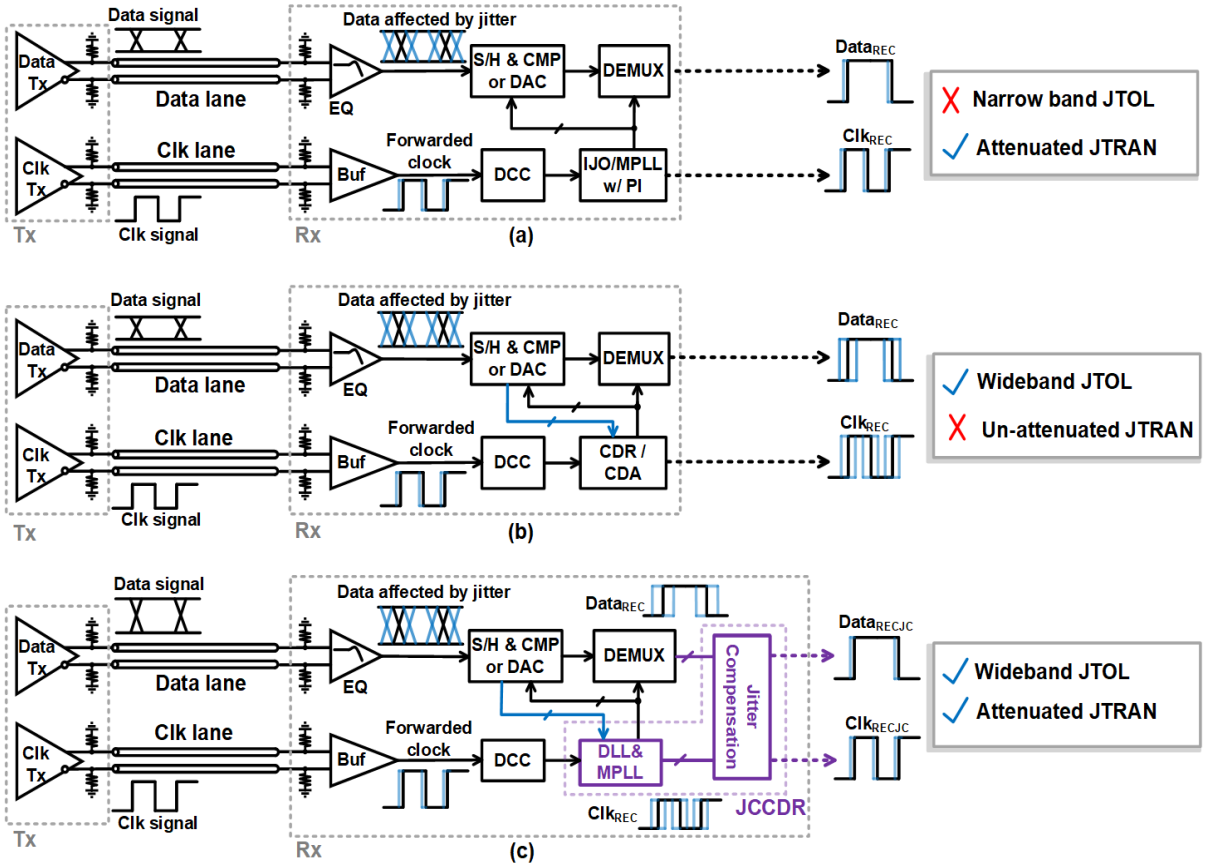

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Figure. 3. 1. Comparison of conventional and proposed source synchronous I/O architectures.
(a) Conventional architecture using IJO/MPLL with PI for deskew and multi-phase clock generation. Since the uncorrelated jitter remains untracked, this architecture provides attenuated JTRAN but poor JTOL. (b) Conventional architecture using a CDR or a CDA to track the uncorrelated jitter, supporting wideband JTOL but un-attenuated JTRAN. (c) Proposed architecture using a JCCDR consisting of a DLL, a MPLL and a jitter compensation circuit to achieve wideband JTOL, and attenuated JTRAN simultaneously.

Source synchronous I/O is an attractive technique in chip-to-chip optical interconnections due to its low latency and high reliability in frequency recovery, wide jitter tolerance (JTOL) bandwidth and implementation simplicity. A widely adopted source synchronous I/O architecture consists of a differential clock lane and a differential data lane is shown in Figure. 3. 1 (a) [8]-[10]. In the clock lane, after the clock signal is transmitted from the Tx through the channel, a buffer (Buf) with a duty cycle correction (DCC) block reproduce a high-quality

clock for data signal sampling. An injection-locked oscillator (IJO) or a multi-phase phase-locked loop (MPLL) use the reproduced clock as reference and generate the four or eight phase (4/8-PH) clocks. A phase interpolator (PI) generates the final sampling clocks by interpolating among the multi-phase clocks to synchronize the decoder and deserialization blocks.

In order to achieve robust synchronization, several jitter and phase skew related issues need to be carefully handled in the clock distribution circuit [11].

First, the data phase and clock phase are typically precisely aligned at the transmitter outputs in source synchronous I/Os. The correlated jitter between clock and data can be properly accommodated by the wideband MPLL or IJO. However, the difference in latencies between the data and clock lanes cause a phase skew between the equalized data and reproduced clock from Buf and DCC. The unfolded phase skew induced by the delays from channels, EQ, Buf, DCC, IJO/MPLL and PI can reach several UIs [9].

Second, except from phase skew, uncorrelated jitter exists between data and clock. For electrical interconnections, the uncorrelated jitter originates from ground and supply noises, temperature drift [12], front-end circuit flicker noises, channel coupling and electro-magnetic interference (EMI). For optical interconnections, the uncorrelated jitter is mainly due to the noises of photo detector and front-end circuit[13]-[15].

Third, even though these uncorrelated jitters are sufficiently tracked, the jitter transfer (JTRAN) on the recovered clock signal CLK_{REC} and data signal $DATA_{REC}$ can still cause error when synchronized to the local clock on the following digital processing systems. For massively parallel communication, the uncorrelated jitters are different from lane to lane, which also induce synchronization challenges.

Various solutions have been reported against the previously mentioned challenges. [16] Employed a delay-locked loop (DLL) for multi-phase clock generation and a PI with coarse and fine phase selection to eliminate the skew between clock and data. To avoid the multi-phase clock mismatch produced by the DLL due to the VCDL asymmetry, an IJO could be used for global I/Q phase generation with better phase matching using proper dummy and

frequency calibration techniques, which was followed by a PI [8] or a local IJO [9] for phase skew elimination. [14] And [15] demonstrated parallel optical interconnections with source synchronous clocking scheme, where digital-controlled delay line in data path [14] and IJO in clock path [15] were employed as deskew methods. The architectures proposed in [8], [9], [14]-[16] are summarized in Figure. 3. 1 (a). Although the methods presented in [8], [9], [14]-[16] properly handled the static phase skew induced by the differences in lane latencies, the uncorrelated jitter between data and clock remained untracked. The narrow JTOL amplitude and bandwidth could stress the decoding circuit.

To support sufficient jitter tracking, various techniques such as time-to-time phase update, clock and data alignment (CDA) and clock and data recovery (CDR) had been proposed. A current integration-based phase rotator was used to handle both static phase skew and jitter, by updating the synchronization clock phase every 50 ms [17]. The equivalent 20-Hz bandwidth could track the jitter caused by slow power and temperature drifts. Similar function was support in [18] employing a 128-Hz CDR loop with alexander phase detector. [12] And [19] used low bandwidth CDA loops with bang-bang type phase detectors and PIs to adjust the sampling phases in background. A 1-MHz baud-rate CDR, a 4-MHz baud-rate CDR and a 5~10-MHz dual path CDR using PIs were presented in [20], [21] and [22], respectively (The CDR bandwidths are read from JTOL measurement results). The architectures proposed in [12], [17]-[22] can be summarized in Figure. 3. 1 (b). So far, the reported JTOL bandwidths had been limited to below 20 MHz, and the undesirable JTRANs on the CLK_{REC} and $DATA_{REC}$ remain as challenges.

JTOL and JTRAN decoupling techniques can be used to support wide JTOL bandwidth with suppressed JTRAN to the recovered clock and data of each lane. A dual-loop configuration consisting of a wideband DLL and narrow-band PLL was proposed to achieve JTOL and JTRAN bandwidth decoupling in [23]-[25]. A novel low-pass loop filter with adjustable loop bandwidth for data and edge samplings was demonstrated in [26] to achieve a wide 20-MHz JTOL bandwidth with a narrow 4-MHz JTRAN bandwidth, under 40-Gb/s 1/4-rate Rx architecture. Nonetheless, the previously reported methods could only narrow the JTRAN bandwidth down to a few MHz, not enough to sufficiently filter out lower frequency jitters from power and ground noises, temperature drift and CMOS device flicker noise. In addition,

the JTOL and JTRAN decoupling technique had only been implemented with non-return-to-zero (NRZ) Rx architecture at data rate below 50 Gb/s.

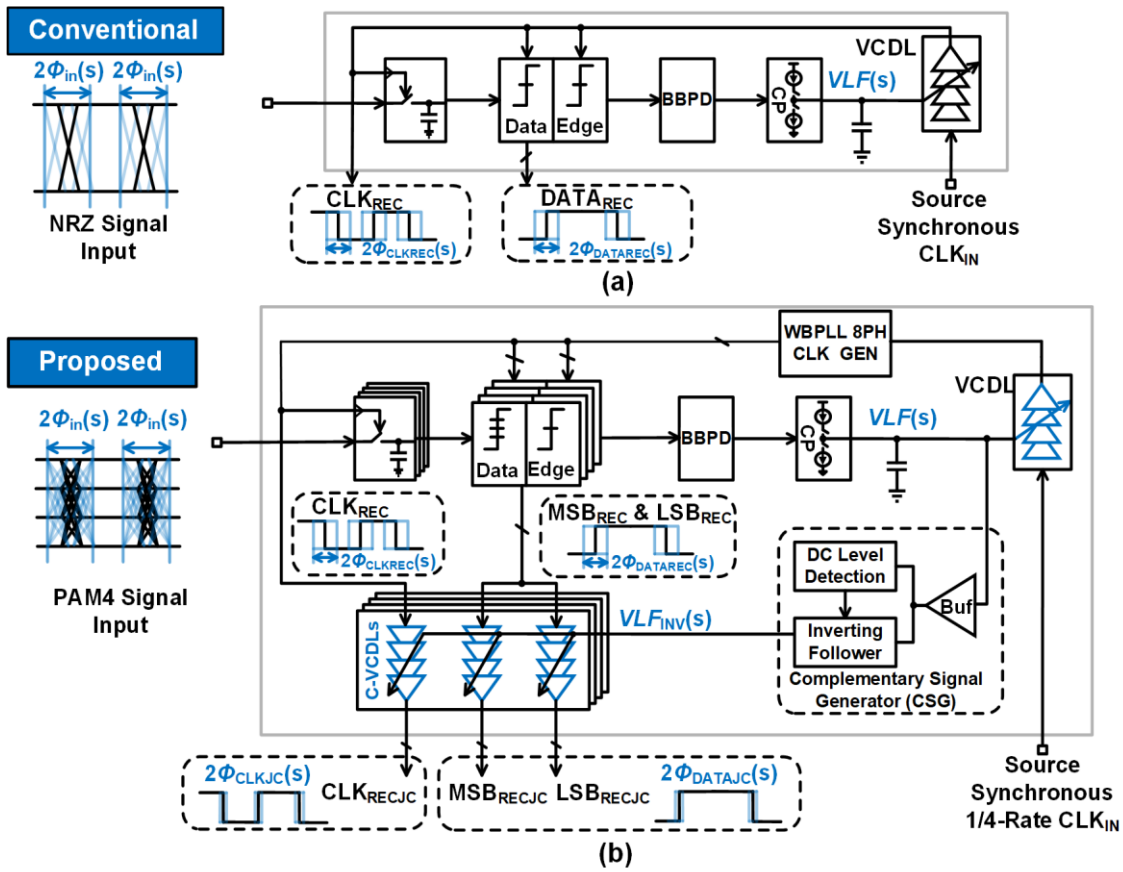


Figure. 3. 2. Principle of the proposed JCCDR.

(a) System diagram of a conventional DLL based CDR. The jitter on the input data is directly tracked and transferred to the CLK_{REC} and $DATA_{REC}$ via *VLF*(s). (b) System diagram of the proposed PAM-4 JCCDR. The JTRANs on the CLK_{RECJC}, MSB_{RECJC} and LSB_{RECJC} are attenuated by the JCC consisting of a CSG and C-VCDLs.

To solve the above-mentioned challenges, this work presents a 60-Gb/s 1/4-rate PAM-4 Rx with a jitter compensation CDR (JCCDR) in 40-nm CMOS technology, achieving a wide 40-MHz JTOL bandwidth and an ultralow <-8-dB JTRAN. The proposed architecture is illustrated in Figure. 3. 1 (c). A first-order DLL employs a bang-bang phase detector and VCDL supporting 40 MHz jitter tracking bandwidth and static phase skew elimination. A second-order wideband PLL (WBPLL) using the 1/4-rate clock as reference provides multi-

phase clock generation with negligible latency. To suppress the consequent JTRAN, a jitter compensation circuit (JCC) acquires the JTRAN amplitude and frequency information by detecting the DLL loop filter voltage (*VLF*), and generates a complementary *VLF* signal, denoted as VLF_{INV}. The VLF_{INV} modulates a group of complementary VCDLs (CVCDL) to attenuate the JTRAN on both recovered clock and data. A jitter compensation ratio up to 78% can be supported from DC to 10 MHz, with a -3-dB corner frequency of 35 MHz. Therefore, this work provides a solution to the three challenges in source synchronous I/O, including clock phase deskew, wideband JTOL and JTRAN attenuation.

The chapter is organized as follow. Section II describes the principle of the JCCDR using a complementary signal generator (CSG) and CVCDLs. Section III presents the overall architecture of the 1/4-rate PAM-4 Rx. Section IV explains the circuit design technique of each block. Experimental results are presented in Section V, and conclusions are drawn in Section VI.

3.3. Principle of JCCDR

The JCCDR needs to support wideband JTOL, JTRAN attenuation, and multiphase clock generation. A conventional DLL based CDR is shown in Figure. 3. 2 (a) as a comparison. The jitter $\Phi_{in}(s)$ and static phase on the input signal is converted proportionally to the loop filter voltage *VLF*(s) through the bang-bang phase detector (BBPD) and charge pump (CP). The *VLF*(s) modulates the VCDL to generate the recovered clock CLK_{REC}, which then samples and decodes the input NRZ signal to produce the recovered data $DATA_{REC}$. Therefore, the input jitter within DLL bandwidth is transferred directly to both CLK_{REC} and $DATA_{REC}$.

In order to attenuate the undesirable JTRAN, a JCCDR supporting 1/4-rate PAM-4 operation is presented in Figure. 3. 2 (b). A first-order DLL tracks the jitter on the input PAM-4 signal using a PAM-4 BBPD, a charge pump (CP), a loop filter, and a VCDL. The VCDL is controlled by *VLF*(s) to generate the 1/4-rate CLK_{DLL}, which carries a jitter almost identical to input PAM-4 signal. A second-order WBPLL uses the CLK_{DLL} as reference to produce the 8-phase (PH-0/45…/270/315) clocks, denoted as CLK_{REC}, for the PAM-4 signal decoding. The 400-MHz WBPLL bandwidth ensures fast frequency and phase update, which does not affect the DLL dynamics. The recovered 8-PH CLK_{REC}s synchronize the PAM-4 decoder to

generate the recovered most significant bit (MSB_{REC}) and least significant bit (LSB_{REC}). A JCC consisting of a complementary signal generator (CSG) and VCDL replicas is used to attenuate the JTRANs on both CLK_{REC}, MSB_{REC} and LSB_{REC}. The CSG yields an inverted loop filter voltage $VLF_{INV}(s)$ for controlling the VCDL replicas to create the complementary-VCDLs (C-VCDL). The $VLF_{INV}(s)$ is designed to have the same amplitude but inverted phase as $VLF(s)$. The CLK_{REC}, MSB_{REC}, and LSB_{REC} are fed to the C-VCDLs controlled by $VLF_{INV}(s)$ to negate the JTRAN, and deliver the jitter-compensated outputs CLK_{RECJC}, MSB_{RECJC}, and LSB_{RECJC}, which theoretically carry no transferred jitters from the input PAM-4 signal.

The principle of jitter compensation can also be illustrated using loop dynamic analysis. The close loop transfer function (CLTF) from input jitter $\Phi_{in}(s)$ to $VLF(s)$ can be derived as shown in Eq. (1):

$$H_{VLF}(s)=\frac{VLF(s)}{\phi_{in}(s)}=\frac{R_T K_{BBPD} K_{CP}\frac{1}{sC}}{1+R_T K_{BBPD} K_{CP}\frac{1}{sC}} \tag{1}$$

where R_T stands for transition ratio (typically equal to 0.5). K_{BBPD} and K_{CP} represents the gains of the BBPD and charge pump (CP). The effect of WBPLL is not include since its loop bandwidth is ten times higher than the DLL.

The CLTF from $\Phi_{in}(s)$ to the recovered clock phase $\Phi_{CLKREC}(s)$ is presented in Eq. (2):

$$H_{\phi_{CLKREC}}(s)=\frac{\phi_{CLKREC}(s)}{\phi_{in}(s)}=\frac{R_T K_{BBPD} K_{CP} K_{VCDL}\frac{1}{sC}}{1+R_T K_{BBPD} K_{CP} K_{VCDL}\frac{1}{sC}} \tag{2}$$

K_{VCDL} represents the gain of the VCDL. Eq. (2) illustrates the JTRAN behavior of the DLL. The 3-dB bandwidth of Eq (2) determines the JTOL bandwidth, as show in Eq. (3).

$$JTOL\ Bandwidth=\frac{R_T K_{BBPD} K_{CP} K_{VCDL}}{C} \tag{3}$$

The CLTF from $\Phi_{in}(s)$ to the phase of jitter compensated clock $\Phi_{CLKRECJC}(s)$ is shown in Eq. (4):

$$H_{\phi_{CLKRECJC}}(s) = \frac{\phi_{CLKREC}(s) + \phi_{in}(s)H_{VLF}(s)K_{CSG}(s)K_{VCDL}}{\phi_{in}(s)}$$

$$\approx \frac{R_T K_{BBPD} K_{CP} \frac{1}{sC}}{1 + R_T K_{BBPD} K_{CP} K_{VCDL} \frac{1}{sC}} \times (K_{VCDL} + K_{CSG}(s) K_{PV} K_{VCDL}) \quad (4)$$

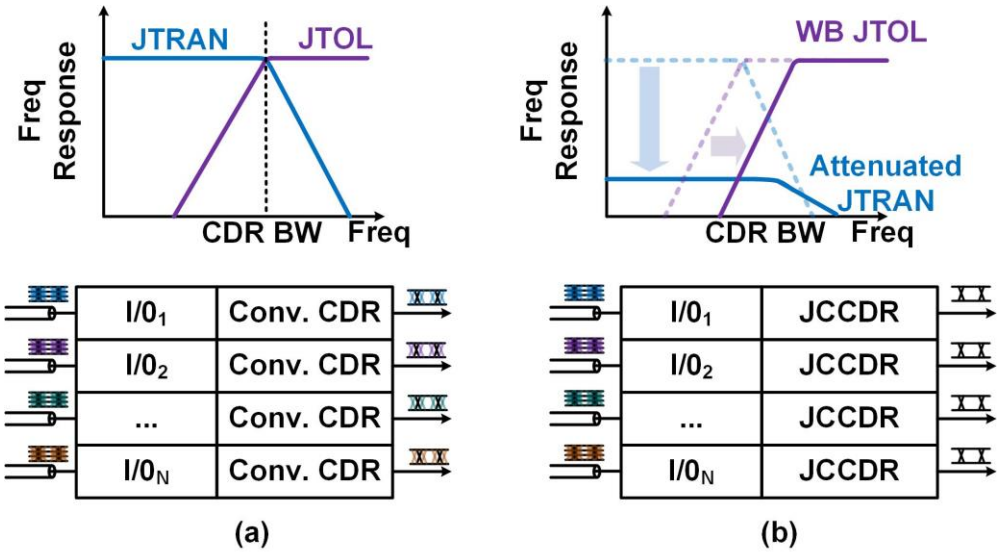


Figure. 3. 3. Comparison of JTRAN and JTOL of conventional CDR (Conv. CDR) and JCCDR.

As described previously, the function of CSG is to produce the $VLF_{INV}(s)$ with the same amplitude and inverted phase as $VLF(s)$. Therefore, represented as K_{CSG}, the gain of CSG ideally is equal to -1. The mismatch factor between K_{VCDL} and K_{CVCDL} due to local process variation is included in K_{PV}, which is close to 1 with fully symmetry layout. Assuming no mismatch between VCDL and C-VCDL, and K_{CSG} is equal to -1, complete JTRAN compensation can be achieved. In real CMOS implementation, the offset and gain error in CSG, and the mismatch between VCDL and C-VCDL due to process variation can degrade the JTRAN compensation performance. The detailed analysis of K_{CSG} will be presented in Section.III.C.

A comparison of JTRAN and JROL performance of conventional CDR and the proposed JCCDR is presented in Figure. 3. 3. The JCCDR is capable of providing a wide band JTOL. The jitter attenuation can cover all jitter frequency, including the low frequency range, which is the major jitter contributor. By employing the proposed JCCDR in high density I/O system, as shown in Figure. 3. 3, the uncorrelated jitter in different I/O clock domain can be compensated, and deliver a theoretically jitter-free output clock and data signal.

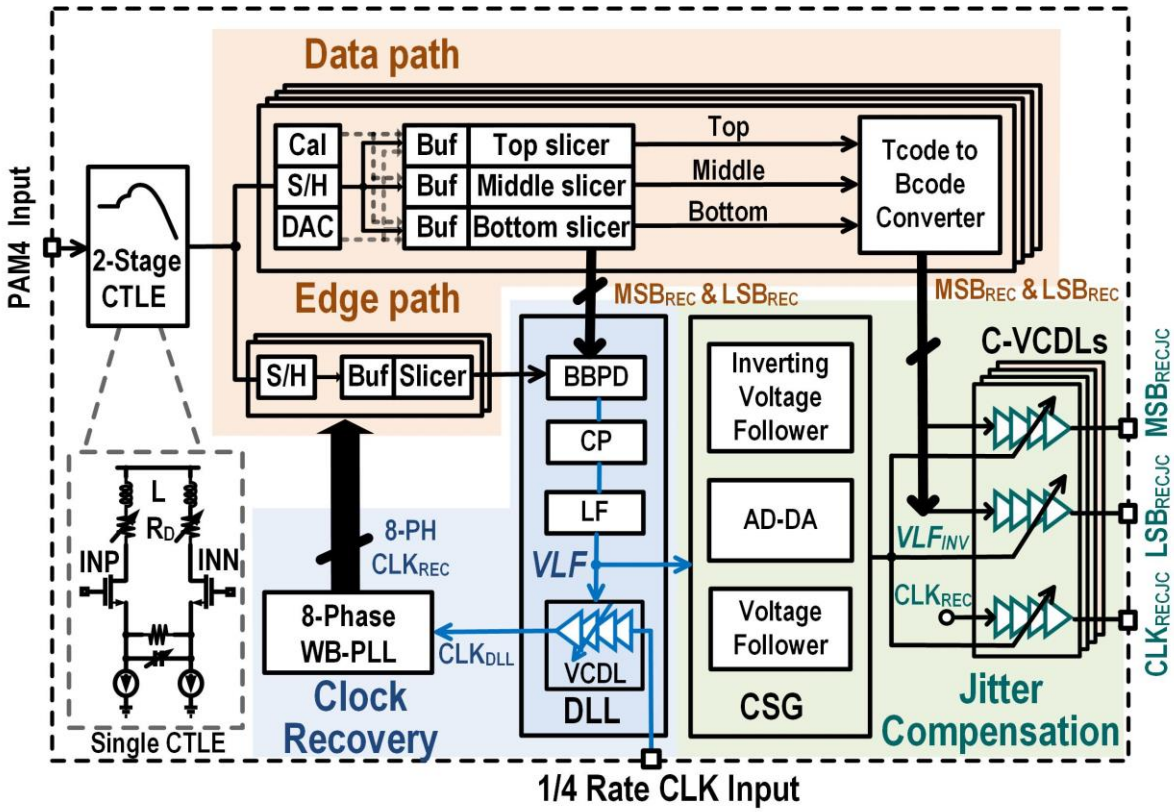


Figure. 3. 4. Complete system diagram of the proposed 60-Gb/s PAM-4 receiver with jitter compensation CDR.

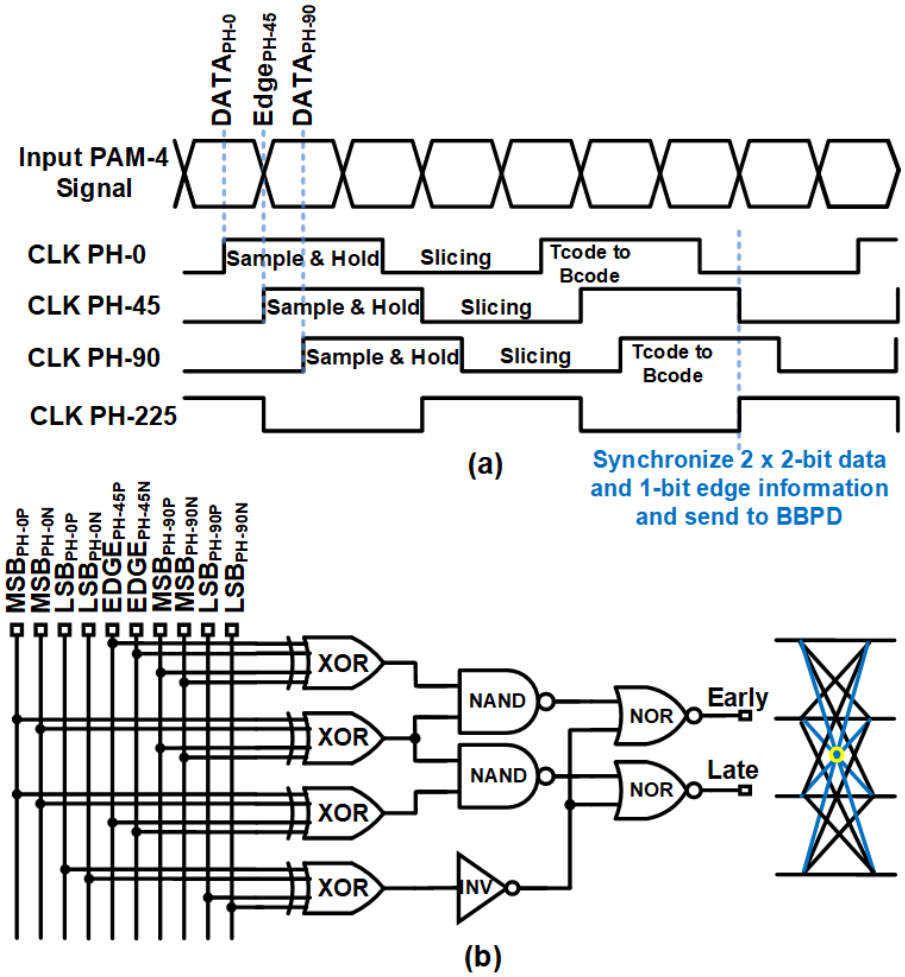


Figure. 3. 5. Receiver timing diagram and BBPD diagram.

(a) Timing diagram for the 1/4-rate decoding circuit using CLK PH-0, 45 and 90. The same timing sequence applies to the other half decoding circuit using CLK PH-180, 225 and 270. (b) Circuit diagram of the PAM-4 BBPD and the valid transitions for phase detection.

3.4. Proposed PAM-4 Receiver Architecture

Figure. 3. 4 depicts the detailed architecture of the proposed PAM-4 Rx utilizing the JCCDR. On the data recovery path, a two-stage continuous-time linear equalizer (CTLE) with R-C source degeneration and inductor shunt peaking architecture is implemented as the front-end to compensate for moderate channel loss. The degeneration capacitor and shunting peaking resistor can be controlled to provide a 2.5~11-dB peaking and 4-dB gain tuning range. Then, the input PAM-4 signal is sampled and deserialized by four sample-and-hold circuits (S/H)

with the PH-0/90/180/270 CLK_{REC} signals. Next, the sampled signals are decoded using three StrongARM comparators (CMP) with individual reference voltages generated from a 6-bit current-mode DAC for slicing the top, middle, and bottom data eyes. The offsets at the input MOSFET devices of the StrongARM CMPs are calibrated upon startup using 6-bit DACs. The decoded 4 × 3-bit thermometer codes (Tcode) are then converted into 4 × 2-bit binary codes (Bcode) as MSB_{REC} and LSB_{REC}.

On the clock recovery path, the PAM-4 signal edge information is detected by two additional S/Hs and CMPs clocked by PH-45/225 CLK_{REC} signals. The decoded data signals are synchronized with the edge signals using a retiming latch before they are applied to the BBPD in the DLL. The phase error detected by BBPD is converted to *VLF*(s) by the capacitor-resistor-capacitor (C-R-C) loop filter and CP with 50~100-uA output current. Since the on-off switching of CP current can cause a relatively large supply variation, the C-R-C loop filter decouples the variation on CP power supply and VCDL power supply. The *VLF*(s) regulates the VCDL to generate the CLK_{DLL}, which tracks the jitter from the input PAM-4 signal. The CLK_{DLL} is then fed into the WBPLL consisting of a 4-stage ring oscillator for producing the 8-PH recovered clocks. The output clock frequency of the WBPLL has a tuning range from 3.75 to 7.5 GHz to support 30-to-60-Gb/s PAM-4 operation. The WBPLL bandwidth is set at 400 MHz to ensure its phase and frequency updates can settle much faster than the CDR DLL, whose bandwidth is designed to be 40 MHz for good JTOL. The 400-MHz PLL bandwidth also supports wideband correlated jitter tracking and pattern-dependent uncorrelated jitter filtering.

The DLL control voltage *VLF*(s) consists of a DC component VLF_{DC} for fixing the locked timing point and an AC component VLF_{AC}(s) for tracking high-frequency jitter. Typically, the VLF_{DC} varies from 0.15 V to 0.85 V, while VLF_{AC}(s) exhibits an amplitude of tens of mV and a bandwidth within 40 MHz. In the JCC, a CSG circuit is used to derive VLF_{INV}(s) from *VLF*(s) with the same DC level, AC amplitude but opposite AC phase. The CSG consists of a unite gain voltage follower, an 8-bit SAR ADC-based DC level detector, and an inverting unite gain follower. The *VLF*(s) is buffered by the unite gain voltage follower and then quantized by the AD/DA to obtain the VLF_{DC} level. The inverting follower generates the VLF_{INV}(s) using the detected VLF_{DC} and the buffered *VLF*(s).

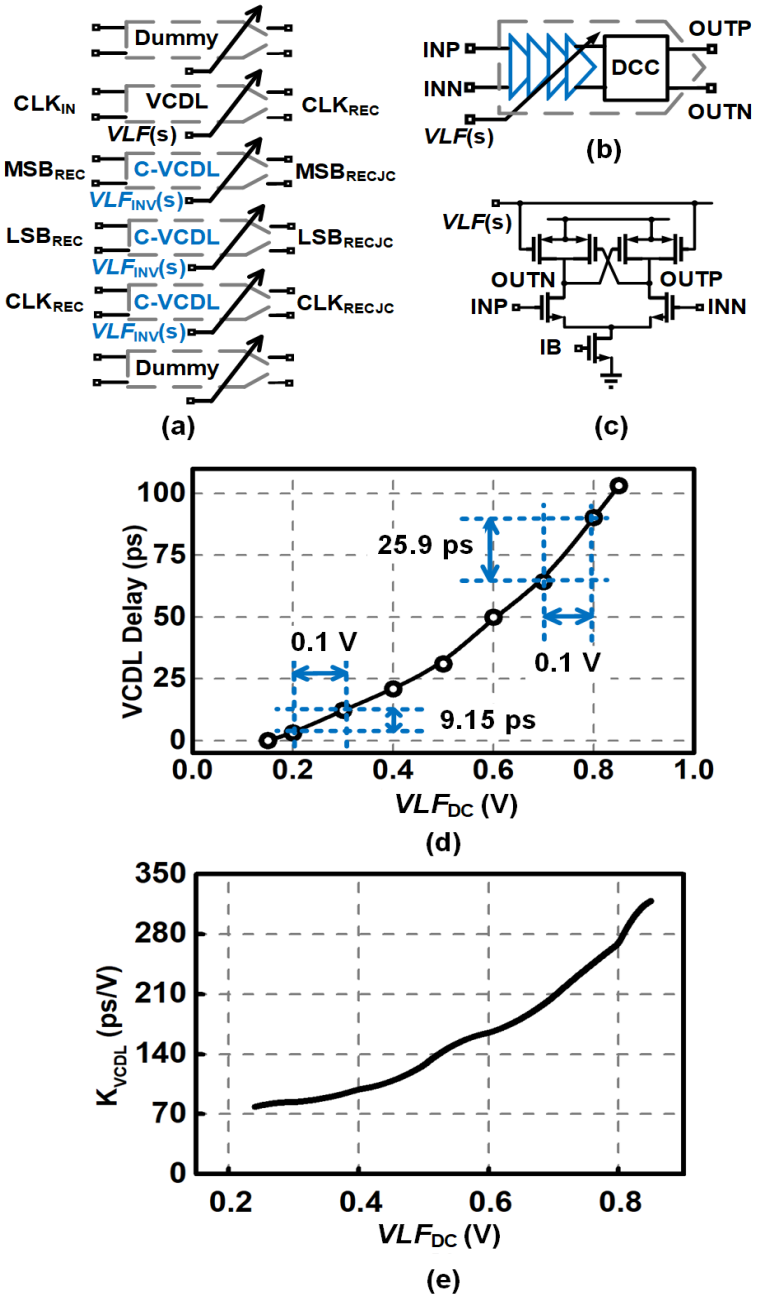


Figure. 3. 6. C-VCDL schematic and simulated delay versus control voltage.

(a) Alignment of VCDL and C-VCDL in layout. (b) VCDL architecture. (c) Schematic of a single delay cell. (d) Simulated VCDL delay versus VLF_{DC}. (e) Calculated K_{VCDL} versus VLF_{DC}.

Three C-VCDLs with identical architecture and symmetrical layout as the VCDL are cascaded at the outputs of the DLL and controlled by $VLF_{INV}(s)$. Since *VLF(s)* and $VLF_{INV}(s)$ have the same amplitude but opposite phase, the jitter produced by VCDL and C-VCDL also carry the same amplitude but opposite phase. Therefore, the JTRAN induced by the VCDL

can be attenuated by the cascaded C-VCDLs to produces jitter-compensated outputs CLK_{RECJC}, MSB_{RECJC}, and LSB_{RECJC}.

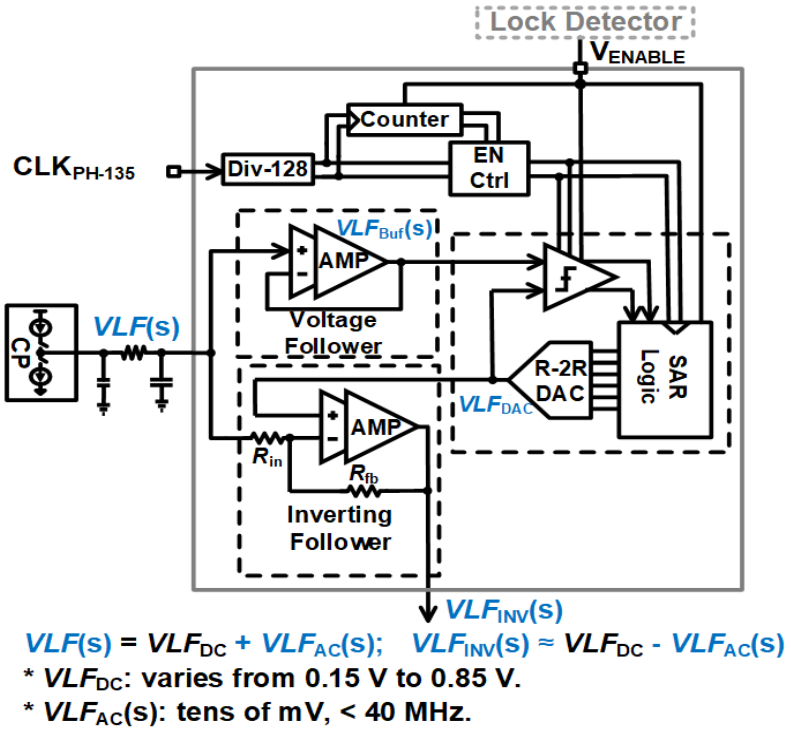


Figure. 3. 7. Block diagram of the CSG circuit

The operation of the JCCDR circuit can be divided into three stages. In the first stage, the WBPLL locks to the input source synchronous clock almost instantaneously thanks to the 400-MHz PLL loop bandwidth. The DLL then corrects the clock skew and captures the jitter. In the second stage, the CSG circuit in the JCC starts operation to produce the $VLF_{INV}(s)$. In the third stage, after the CSG converges and a valid $VLF_{INV}(s)$ is obtained, the JCC controls the CVCDLs to produce the final MSB_{RECJC} and LSB_{RECJC} outputs with suppressed JTRAN.

3.5. System Implementation

3.5.1. 1/4-rate BBPD

The timing diagram for decoding the data signals at clock PH-0, 90 and edge signal at clock PH-45 is shown in Figure. 3. 5 (a). The same timing sequence applies to data and edge decoding on clock PH-180, 270 and 225. At the first rising edges of PH-0, 90 and 45, the data and edge signals are sampled and held on sampling capacitors. On the following falling edges, the data and edge signals are decoded using CMPs with three reference levels. The decoded data signals are in the Tcode format, which are converted into Bcode format at the second clock rising edges. The decoded data and edge information are synchronized by clock PH-225, and then sent to the BBPD for phase detection.

The BBPD logic used for clock PH-0, 45 and 90 is shown in Figure. 3. 5 (b). The same circuit is also employed for PH-180, 225 and 270. The BBPD only produces the Late and Early signals when the MSB and LSB data on the rising edges of two consecutive clock cycle are both different from each other. The valid transitions for phase detection are shown in Figure. 3. 5 (b) with a yellow circle.

3.5.2. VCDL and C-VCDL

In order to ensure better matching, the VCDL and C-VCDLs are aligned close to each other, and protected by dummies at both ends in the layout, as shown in Figure. 3. 6 (a). The VCDL is composed of four single voltage-controlled delay cells and a duty cycle correction block. Each delay cell consists of a pair of NMOSs as input devices and a pair of PMOSs controlled by VLF(s) or VLF_{INV}(s) to determine the delay time. A cross coupled PMOS pair is used to correct the duty cycle. The delay cell with current source transfers less supply variation into output jitter.

The simulated VCDL delay versus VLF_{DC} is plotted in Figure. 3. 6 (d). The derived K_{VCDL} is shown in Figure. 3. 6 (e). The VLF_{DC} can vary from 0.15 V to 0.85 V to set the VCDL delay from 0 to 105 ps, respectively, according to the simulated transfer characteristics. The 105-ps delay range is equivalent to 2.24 UI at 60-Gb/s PAM-4 input. However, Figure. 3. 6 (e) indicates that, the K_{VCDL} varies significantly over different VLF_{DC} levels. For example, changing the VLF_{DC} level from 0.25 V to 0.85 V causes K_{VCDL} to vary from 70 ps/V to 280 ps/V.

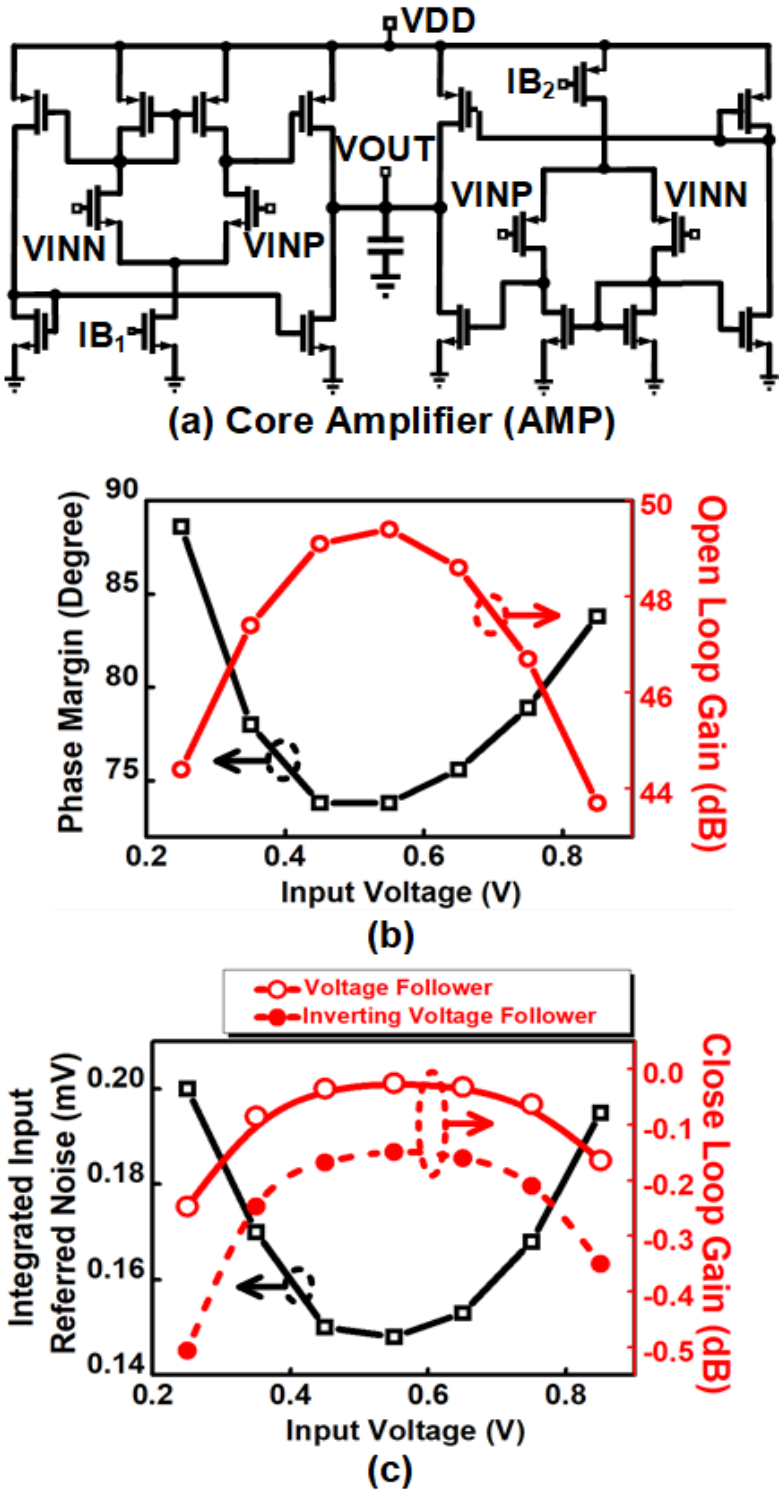


Figure. 3. 8. Design and simulation of the core amplifier.

(a) Schematic diagram of the rail-to-rail core AMP circuit. (b) Simulated open loop gain and phase margin. (c) Simulated close loop gain and integrated input referred noise.

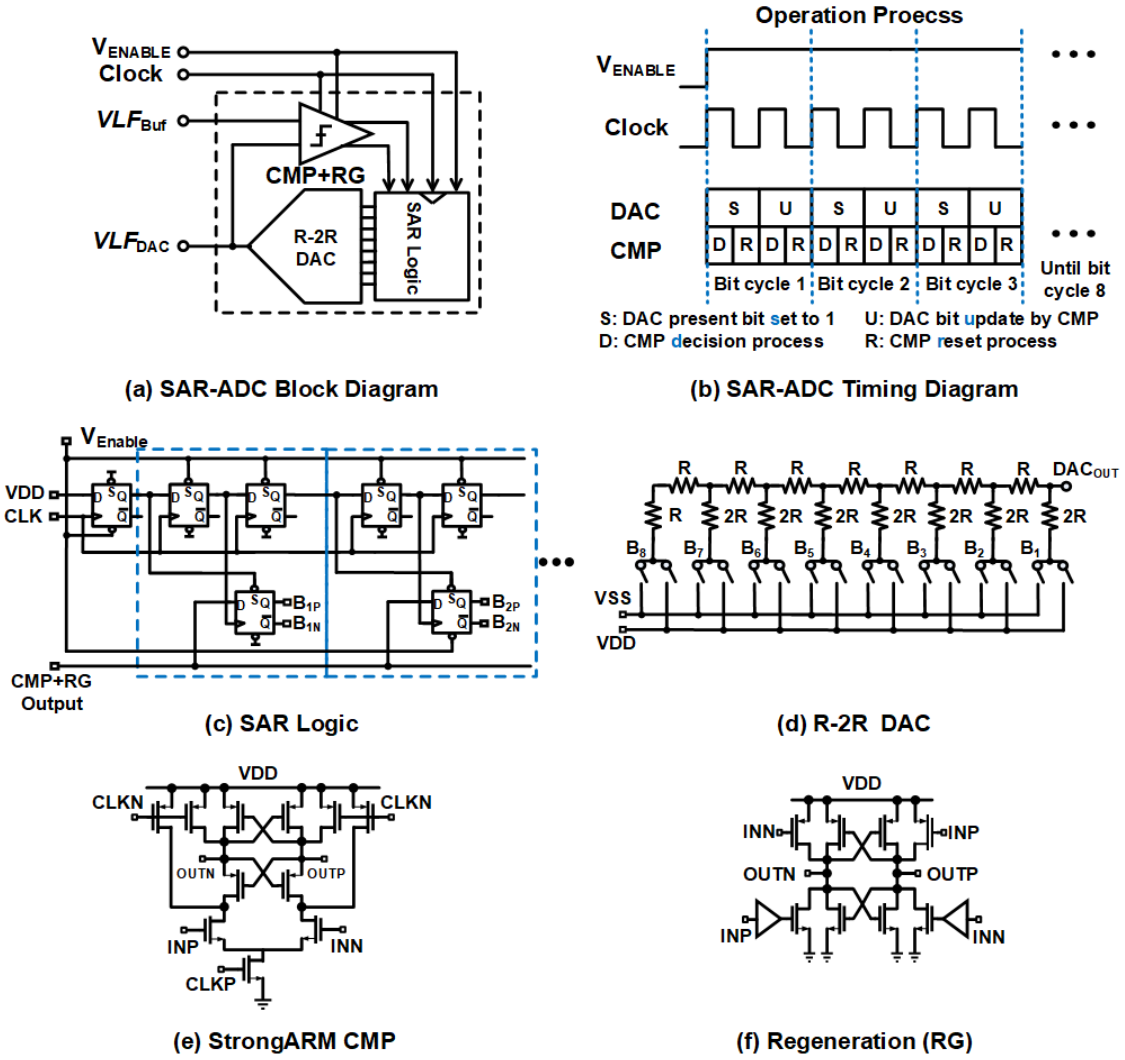


Figure. 3. 9. Block diagram, timing sequence and circuit implementations of the SAR-ADC.

3.5.3. CSG

Since the K_{VCDL} varies by four times at most over different VLF_{DC} values, CSG needs to generate VLF_{INV}(s) with the same DC level, same AC amplitude but inverted AC phase as VLF(s). The CSG presented in

Figure. 3. 7 mainly consists of a voltage follower, a SAR-ADC, an inverting follower and a clock control circuit. The voltage follower employs a 2-stage core amplifier (AMP) with rail-to-rail input and output ranges connected as unit gain feedback to produce the buffered VLF_{Buf}(s). An 8-bit SAR ADC, consisting of a CMP, an R-2R DAC, and a SAR logic, detects

the DC level of $VLF_{Buf}(s)$. The output of the R-2R DAC, VLF_{DAC} is designed to track VLF_{DC} with an error less than 7 mV. Upon receiving the enabling signal V_{ENABLE} from the lock detector, the SAR-ADC starts operation to detect, reproduce, and maintain the DC level of VLF_{Buf} on the R-2R DAC as VLF_{DAC}. The inverting follower receives the $VLF_{Buf}(s)$ and VLF_{DAC} and generates the $VLF_{INV}(s)$ by setting its input and feedback resistors, R_{in} and R_{fb}, both equal to 10 KΩ, which generates the inverting gain close to -1. The DC level of $VLF_{INV}(s)$, denoted as VLF_{INVDC}, is fixed close to VLF_{DC} with a negligible error caused by the insufficient gain of the core AMP and the ADC nonlinearity. The CSG block is synchronized by the clock PH-135 from PLL after divided by 128.

3.5.4. Core AMP

The architecture of the core AMP used in the voltage follower and the inverting voltage follower is shown in Figure. 3. 8. The AMP unit gain bandwidth (UGB) is designed to be ten times higher than the $VLF(s)$ bandwidth, which can be derived from Eq. (1), as shown below.

$$VLF_{BW} = \frac{R_T K_{BBPD} K_{CP}}{C} \tag{5}$$

Calculated from Eq. (5), the $VLF(s)$ signal occupies a bandwidth of around 12 MHz. Since only 120-MHz UGB is needed, larger mosfet devices can be used to obtain lower flicker noise and higher open loop gain. A higher open loop gain minimizes the DC and AC following error when the core AMP is configured as voltage follower or inverted voltage follower. Two 2-stage amplifiers with PMOS and NMOS as input devices can support a rail-to-rail input and output ranges, which completely cover the VLF_{DC} range from 0.25 V to 0.85 V. Sweeping over the rail-to-rail input range, the open loop gain and phase margin are obtained from the post layout simulation, as presented in Figure. 3. 8

3.5.5. SAR ADC

Figure. 3. 9 (a) shows the overall block diagram of the SAR ADC, consisting of a StrongARM comparator (CMP) with regeneration (RG), an 8-bit SAR logic and an 8-bit R-2R ladder-based DAC. The timing diagram of the SAR ADC is shown in Figure. 3. 9 (b). The

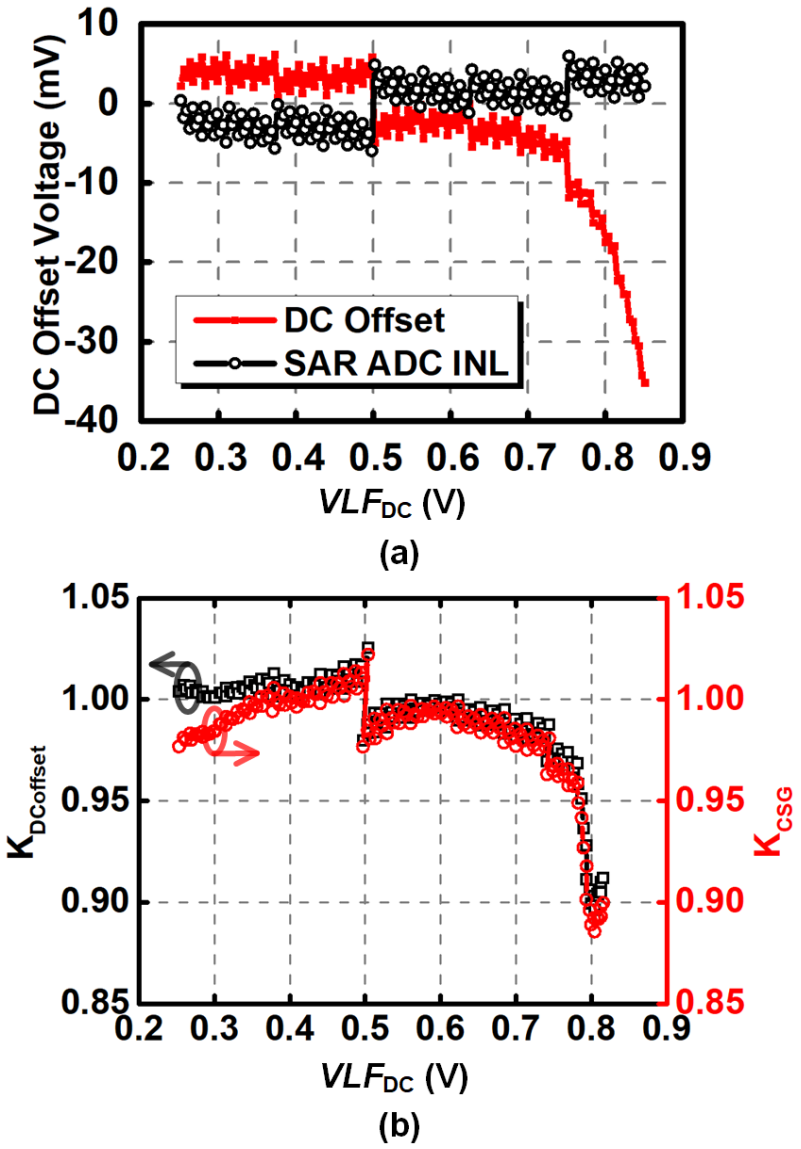


Figure. 3. 10. SAR ADC simulation results.

(a) Simulated SAR ADC INL and the overall DC offset between VLFDC and VLFINVDC. (b) Calculated KDCoffset and KCSG.

SAR logic circuit consists of eight identical units shown in Figure. 3. 9 (c). Each SAR logic unit contains two sequence-control D-Flip-Flops (SDFF) and one coding DFF (CDFF) to produce the switch control bit for the corresponding R-2R unit. The R-2R DAC shown in Figure. 3. 9 (d) directly uses VDD and VSS as reference levels to cover the whole VLF_{DC} range. The principle of the SAR ADC is to pre-set each DAC control bit to 1 as a predicted value successively, and then update the control bit after comparing the predicted value with the input. The operation of each SAR ADC unit takes two clock cycles. In the first clock cycle, the CDFF sets (S) the R-2R unit control bit to 1 for prediction. The StrongARM CMP starts the comparison process at the clock rising edge, and is reset at the following clock falling edge. The return-to-zero (RZ) code produced by the CMP is converted into NRZ format by the RG circuit. In the second clock cycle, the CDFF output is updated (U) with the CMP comparison result, as illustrated in timing diagram in Figure. 3. 9 (b).

3.5.6. K_{CSG} Analysis

Ideally, K_{CSG} is equal to -1 to generate an $VLF_{INV}(s)$ signal with completely the same amplitude and inverted phase as $VLF(s)$. However, two non-ideal factors deviate K_{CSG} from -1, including the AC gain errors in voltage follower and inverting follower, and the DC offset between VLF_{DC} and VLF_{INVDC}. Therefore, K_{CSG} can be represented using the equation below.

$$K_{CSG} = K_{ACgain} K_{DCoffset} \tag{6}$$

The AC gain errors of the voltage follower and the inverting follower cause difference between amplitudes of $VLF_{AC}(s)$ and $VLF_{INVAC}(s)$, as presented in Figure. 3. 8 (c). The DC offset between VLF_{DC} and VLF_{INVDC} is caused by the integrated nonlinearity (INL) of the SAR ADC and the DC following error. In order to calculate $K_{DCoffset}$, the SAR ADC INL is simulated and shown in the black curve of Figure. 3. 10 (a). The overall DC offset caused by the INL and DC following error is also simulated and presented in the red curve of Figure. 3. 10 (a). The maximum DC offset voltage is 36 mV due to the drop in voltage following gain at 0.85-V VLF_{DC}, which is close to the edge of the input rail. Based on the simulated DC offset voltage, the $K_{DCoffset}$ under different VLF_{DC} level can be calculated using the equation below.

$$K_{\mathrm{DCoffset}} = \frac{K_{\mathrm{VCDL}}(VLF_{\mathrm{DC}} + \mathrm{DCoffset})}{K_{\mathrm{VCDL}}(VLF_{\mathrm{DC}})} \tag{7}$$

$K_{\mathrm{VCDL}}(VLF_{\mathrm{DC}})$ represents the K_{VCDL} value at VLF_{DC}. The calculated K_{DCoffset}, and $K_{\mathrm{DCoffset}} \bullet K_{\mathrm{ACgain}}$ are presented in Figure. 3. 10 (b). In most of the VLF_{DC} range, $K_{\mathrm{DCoffset}} \bullet K_{\mathrm{ACgain}}$ can be kept within 0.95~1.05. A relatively high deviation down to 0.88 can happen as VLF_{DC} approaches the higher end of 0.85 V.

3.5.7. CSG Simulation

Transient simulation is performed on the CTLE, PAM-4 decoder, DLL and CSG circuits to verify the $VLF_{\mathrm{INV}}(t)$ generation function.

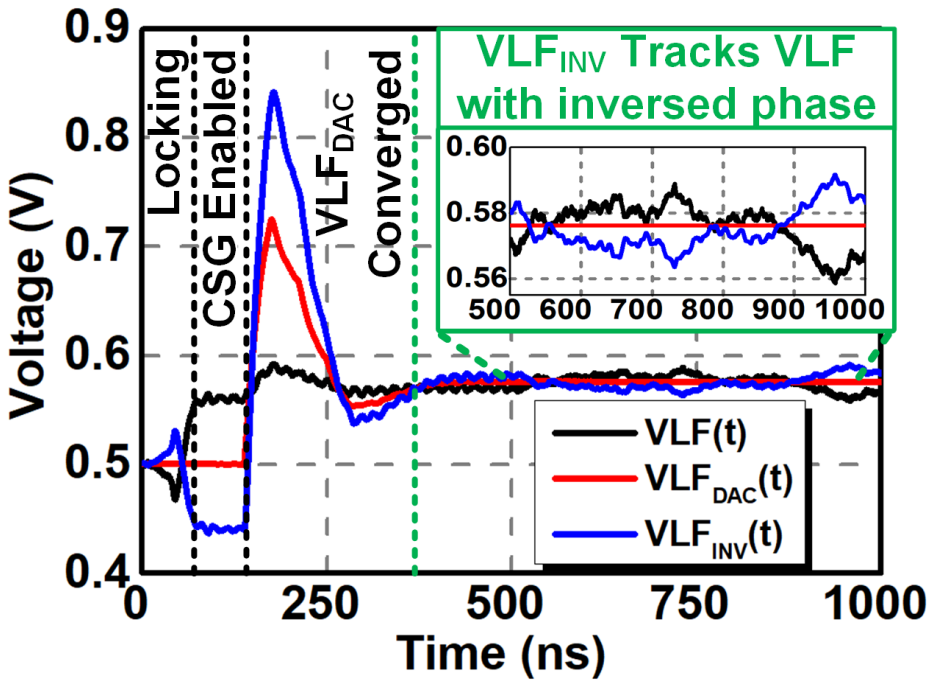


Figure. 3. 11. Transient simulation results of the CSG.

A 60-Gb/s jitter free PAM-4 signal is transmitted into the Rx through a 3-cm 50-Ohm transmission line. The collected *VLF*(t), VLF_{DAC} and VLF_{INV}(t) curves shown in Figure. 3. 11 verified the three operation stages explained in Section. III. The DLL locking state is obtained within 20 ns in the first stage. Then the CSG converges and produces a valid VLF_{DAC} signal using 200 ns in the second stage. Next, the VLF_{INV}(t) is generated by the CSG, which precisely tracks the *VLF*(t) signal, as shown with black and green curves in Figure. 3. 11 (a).

Although no jitter is added to the input signal, the simulation verifies that the CSG can still track the pattern-dependent *VLF*(t) variation.

3.5.8. WBPLL

The second-order WBPLL and its linear model are presented in Figure. 3. 12. The WBPLL uses the synchronous 1/4-rate clock as reference and produces 8-PH output clocks with the same frequency as input. Thanks to the high frequency reference clock, the WBPLL can support 400-MHz loop bandwidth without stability issue. The wide loop bandwidth of PLL benefits faster locking, higher ring oscillator phase noise suppression, and lower VCO power consumption.

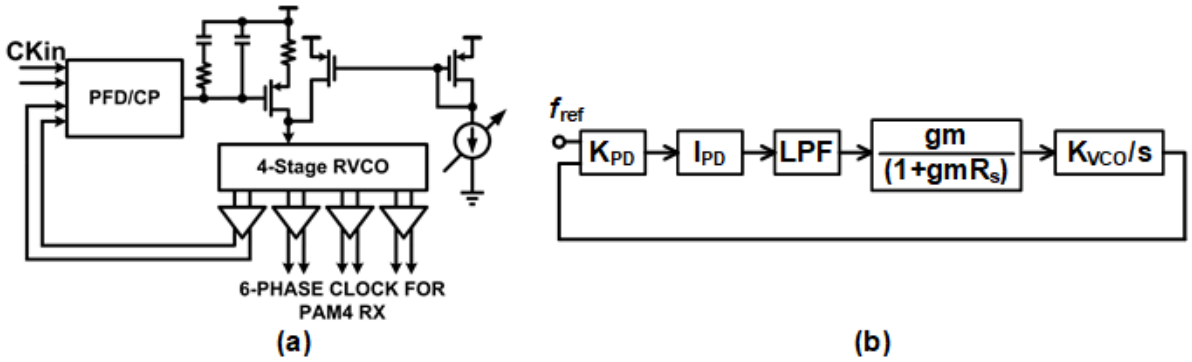
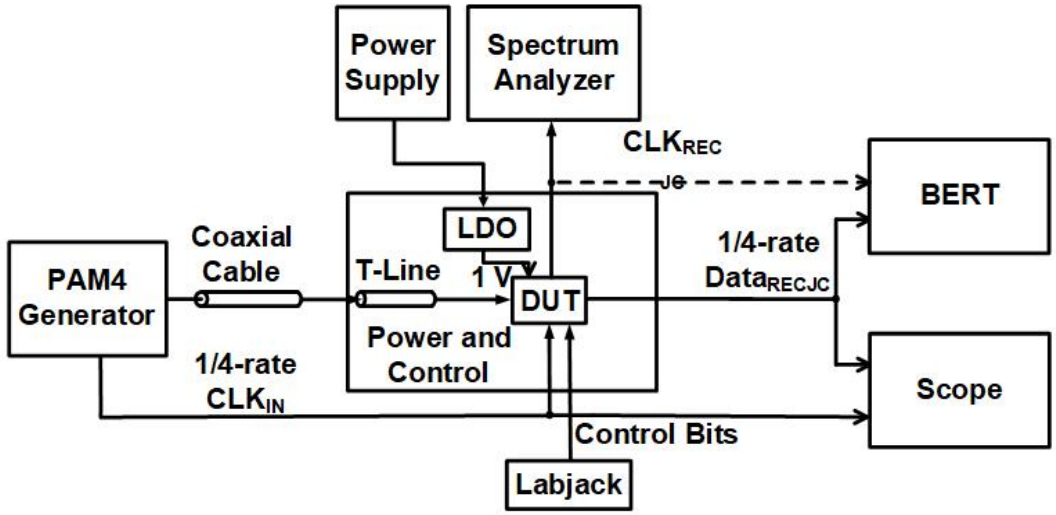


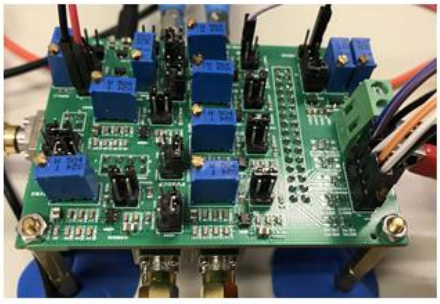
Figure. 3. 12. System diagram and linear model of the WBPLL.

The ring oscillator is implemented using four delay cells with a current source for frequency control. By adjusting an external coarse control current, the oscillation frequency be tuned from 3.75 to 7.5 GHz. Compared with other multi-phase clock generation techniques such as

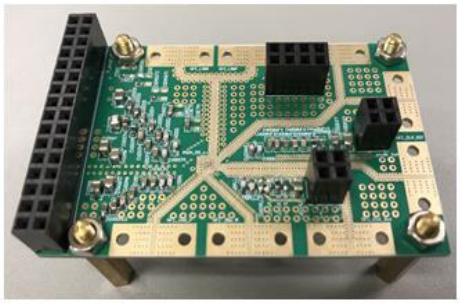
IJO and DLL, WBPLL causes minor phase mismatch due to the intrinsic symmetry of the ring oscillator. Among the eight output phases, PH-0, 90, 180, 270 are used for synchronizing the data sampling, decoding, and thermometer to binary format conversions, PH-45 and 225 are used for edge sampling. PH-135 is applied to the CSG block. PH-315 serves as the feedback for the PLL phase frequency detector.



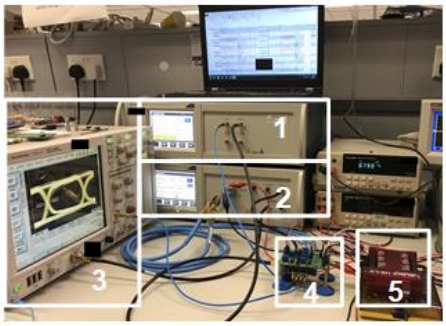
(a) System Diagram of the Experimental Setup



(b) Power and Control PCB module



(c) Chip Mounting PCB Module



(d) Experimental Setup

1. Bit error rate tester (BERT)
2. Pattern generator
3. Scope
4. Chip on power and control PCB module
5. Labjack

Figure. 3. 13. Experimental Setup. (a) System diagram of the test bench. (b) ~ (d) Testing PCB modules and experimental setup.

3.6. Experimental Results

The system diagram of the experimental setup is shown in Figure. 3. 13 (a). The PAM-4 data and 1/4-rate clock signals from the pattern generator is transmitted through a pair of high frequency coaxial cables and 3-cm PCB transmission line into the chip. The labjack feeds the control bits to the on-chip I2C module. The recovered and jitter-compensated 1/4-rate data and clock signals are sent to the BERT and sampling oscilloscope respectively. A low frequency power and control PCB is used for setting the VDD, bias point and control bits. Another high frequency PCB is employed for chip mounting and transmission lines routing. The overall experimental setup is shown in Figure. 3. 13 (d). The measurement is divided into three parts, basic clock and data recovery, JTOL, JTRAN and Jitter compensation.

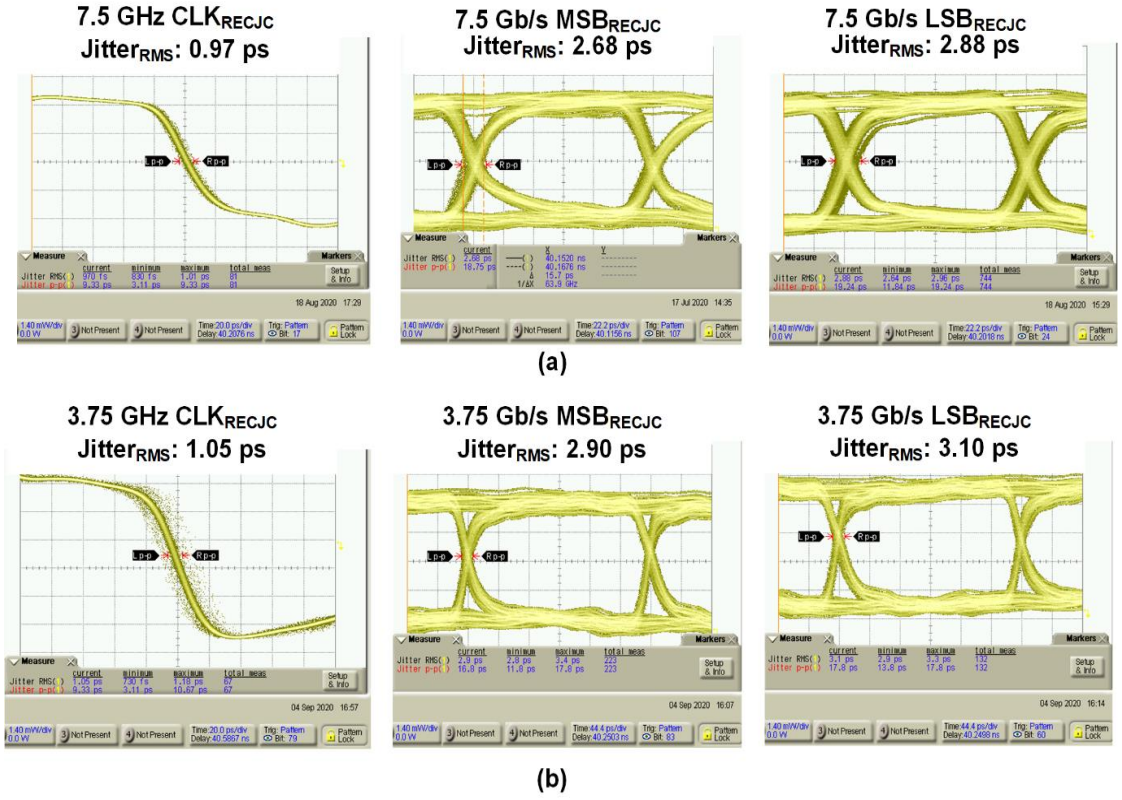


Figure. 3. 14. Measured eye diagrams of CLKRECJC, MSBRECJC, and LSBRECJC.
(a). 60-Gb/s PAM-4 input; (b). 30-Gb/s PAM-4 input.

3.6.1. Clock and Data Recovery Measurements

The input PAM-4 signals from 30 Gb/s to 60 Gb/s are used as input for testing the clock and data recovery function. The decoded quarter-rate MSB and LSB data eyes are shown in Figure. 3. 14. At 60 Gb/s with <10-12 bit error rate (BER), the measured RMS jitter for the 7.5-GHz clock and the 7.5-Gb/s MSB and LSB are 0.97, 2.68, and 2.88 ps, respectively. Figure. 3. 15 plots the measured bathtub curves at 60 Gb/s, achieving 0.25-UI opening with PRBS7 pattern, and 0.1-UI opening with PRBS-15 pattern respectively.

3.6.1.1 JTOL Measurements

A single tone Jitter sweeping from 10 kHz to 80 MHz (frequency limited by equipment) is added to the data for testing maximum tolerable Jitter amplitude ensuring error-free decoding. The measured JTOL versus jitter frequency shown in Figure. 3. 16 (a) demonstrates a 40-MHz bandwidth with a minimum Jitter amplitude of 0.2 UIPP. The measured WBPLL phase noise (PN) is presented in Figure. 3. 16 (b), which shows a 400-MHz loop bandwidth ensuring wideband VCO phase noise suppression and correlated jitter tracking.

3.6.1.2 JTRAN and Jitter Compensation Measurements

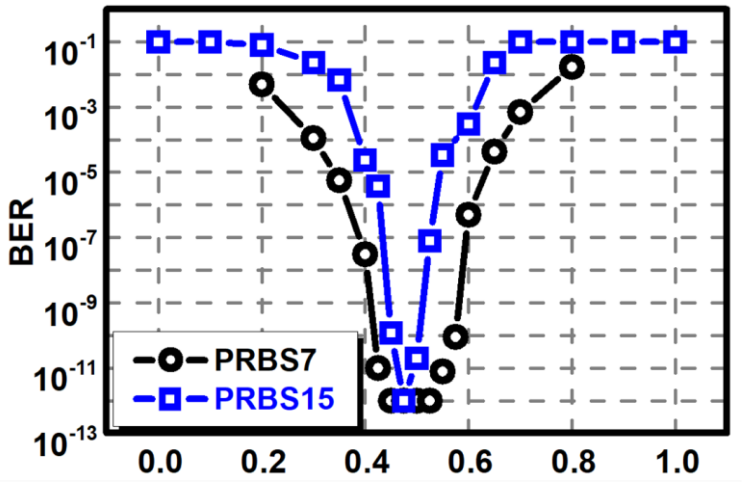


Figure. 3. 15. Measured bathtub curves with PRBS7 and PRBS15 testing pattern.

By stressing the input PAM-4 signal with an additional 50- ps peak-to-peak Jitter, the measured recovered data eye diagrams with and without JCC function are presented in Figure. 3. 17 (a), under 100-kHz, 1-MHz, and 40-MHz Jitter frequencies respectively. The eye diagram comparison illustrates that the JTRAN can be significantly suppressed by the proposed JCCDR. The JTRAN is attenuated by the JCC to be lower than -8 dB in all jitter frequencies, as presented in Figure. 3. 17 (b). Jitter compensation ratio close to 80% can be maintained from DC to 10 MHz, with a -3-dB corner frequency of 35 MHz, as shown in Figure. 3. 17 (c). The performance comparison table demonstrates that this work achieves the highest JTRAN suppression with the widest JTOL bandwidth for PAM-4 Rx over 50-Gb/s data rate reported to date. The chip micrograph and its power consumption breakdown are shown in Figure. 3. 18.

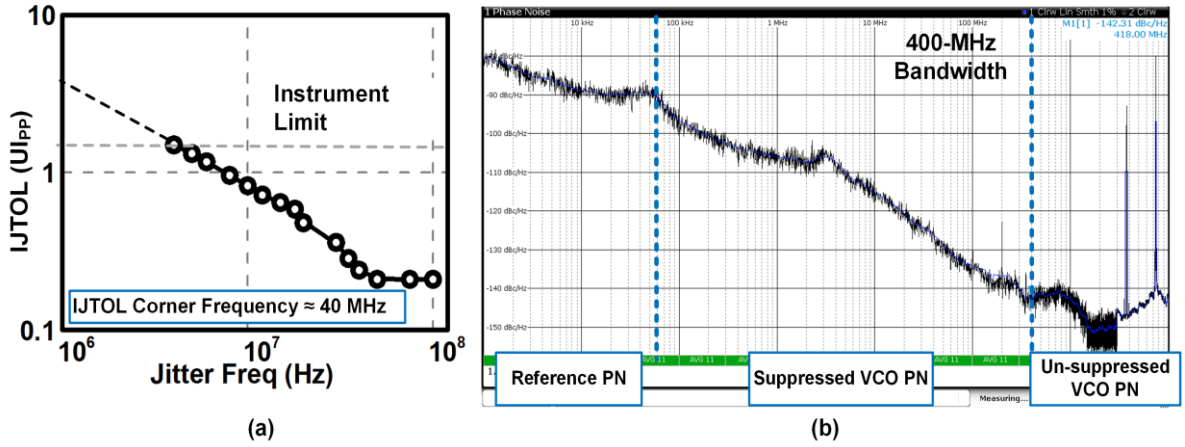


Figure. 3. 16. Measured JTOL and WBPLL phase noise.

(a) Measured IJTOL versus I-jitter frequency (b) Measured WBPLL output phase noise (PN).

3.7. Conclusion

Design of clock distribution circuit for source synchronous communication needs to handle three critical challenges, including the channel latency induced static phase skew elimination, wideband JTOL and JTRAN suppression. This paper presents a 30~60-Gb/s 1/4-rate PAM-4 Rx with a JCCDR, achieving 40-MHz JTOL bandwidth accommodating 0.2-UIPP jitter

amplitude, while maintaining an ultra-low <-8- dB JTRAN over all jitter frequency. The proposed method provides a complete solution to the three challenges mentioned above.

	[13] [ISSCC'15]	[16] [JSSC'19]	[25] [JSSC'20]	[26] [VLSI'14]	[2] [JSSC'17]	[18] [JSSC'19]	This work
Technology	28-nm	28-nm	28-nm	65-nm	65-nm	40-nm	**40-nm**
Architecture	1/4-rate NRZ	1/4-Rate NRZ	Half-rate PAM-3	1/4-rate NRZ	1/4-rate NRZ	1/4-rate NRZ	**1/4-rate PAM4, JCCDR**
IJTOL [UI_{PP}] @ bandwidth	None	None @ 1 MHz	None	0.1 UI_{PP} @ 1 MHz	0.41 UI_{PP} @ 20 MHz	0.22 UI_{PP}* @ 4 MHz	**0.2 UI_{PP} 40 MHz**
IJTRAN [dB] @ bandwidth	None	None	None	0 ~ -3 dB @DC ~ 1 MHz	0 ~ -3 dB @DC ~ 4 MHz	0 ~ -3 dB @DC ~ 4 MHz	**<-8 dB @All band**
CJTOL Architecture Bandwidth	IJO 150 MHz	IJO 150 MHz	DCDL/PL All band	IJO/PI 100 MHz	PI All band	None	**WBPLL 400 MHz**
Data Rate [Gb/s]	16-32	16 (32/pair)	30	14	40	25	**30-60**
Power [mW]	4.87	58.5	33.3	7.8	225	52**	**70.8**
Eff. [pJ/bit]	0.153	1.83	1.11	0.56	5.625	2.1**	**1.18**
Supply (V)	1.0	0.9	0.6	0.8	1.2	None	**1.0**

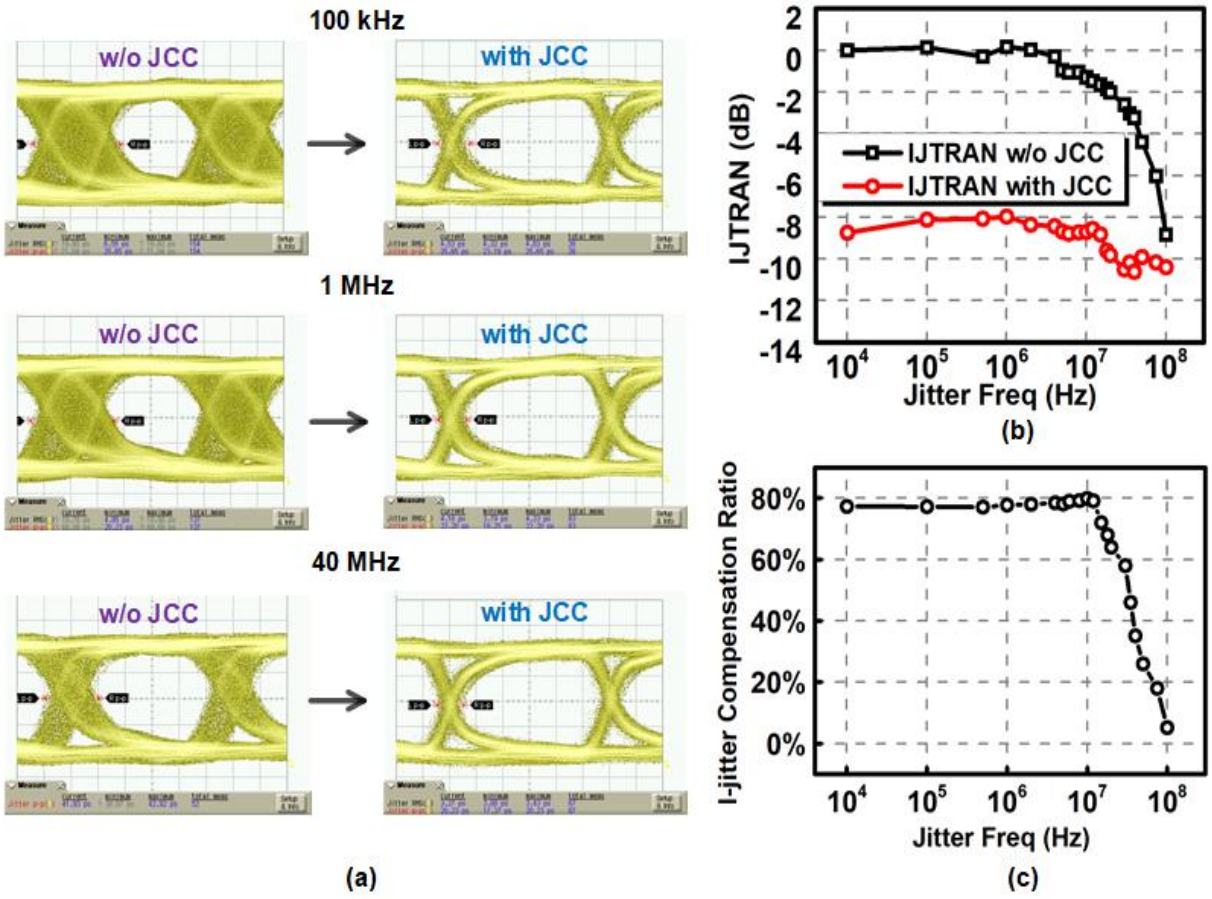


Figure. 3. 17. Jitter compensation performance measurement

(a). Comparison of measured eye diagrams of CLK_{RECJC}, MSB_{RECJC}, and LSB_{RECJC} with and without enabling the JCC function, under different I-jitter frequencies.

(b). Measured JTRAN versus jitter frequency.

(c). Calculated jitter compensation ratio versus Ijitter frequency.

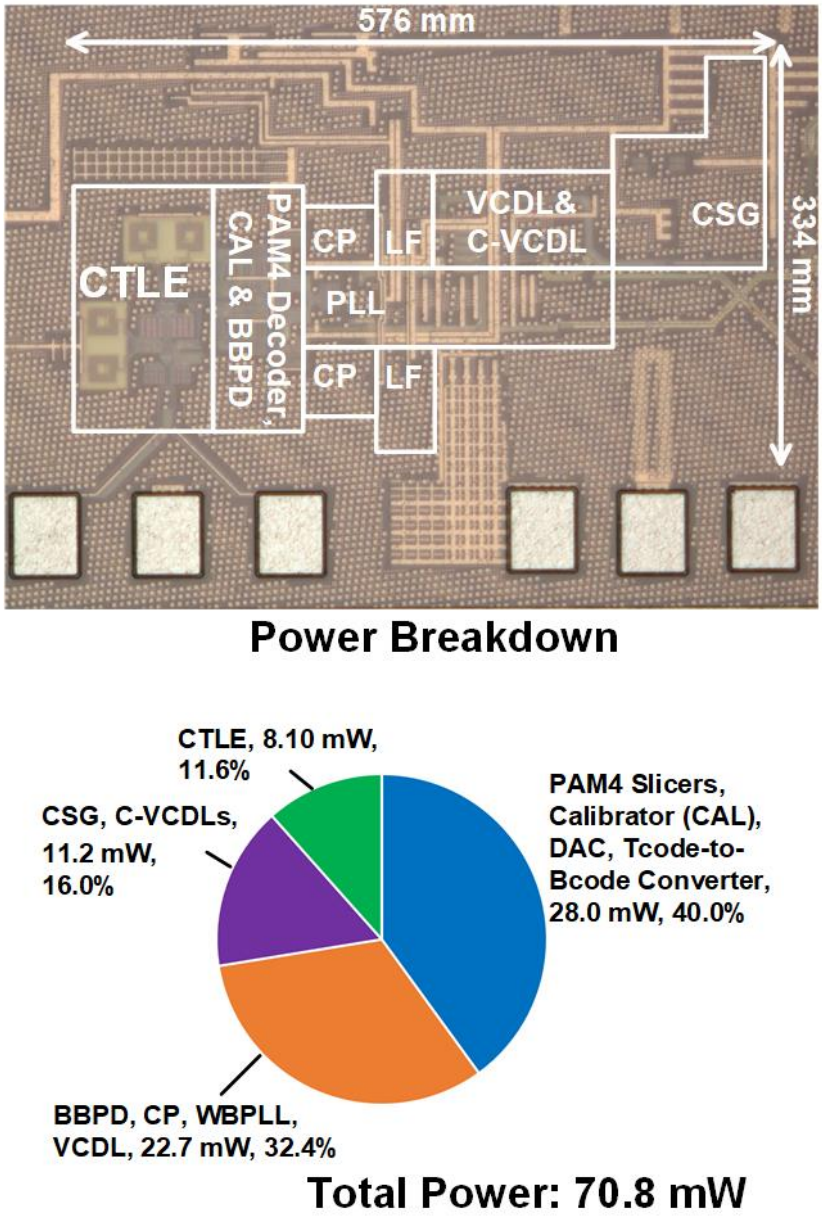


Figure. 3. 18. Chip micrograph and power breakdown

(a). Chip micrograph.

(b). Power consumption breakdown.

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Chapter 4 Wireless Power and Data Transfer System with Variable Channel Bandwidth Compensation

4.1. Introduction

Wireless power transfer (WPT) systems can potentially provide simultaneous power and data transfer for Internet-of-Things devices, such as smart speakers, glasses and watches. However, due to the high-quality factor of coils, the intrinsically narrow WPT channel bandwidth severely limits the data transmission capability of the system, especially for data downloading links requiring higher data rates. In addition, the channel bandwidth varies with power transfer distances, which is also undesirable for wireless communication. In this chapter, the channel features of a two-coil series-series matching magnetic resonance wireless power and data transfer (MWPDT) system, including the bandwidth and the roll-off slope are characterized analytically. Based on the characterization results, a receiver front-end circuit with a three-stage cascaded equalizer (EQ) is proposed and implemented to extend the bandwidth of a MWPDT system at different distances. The proposed EQ can provide a frequency response with a variable roll-up slope from 10 to 45 dB/dec to compensate for the distance-dependent channel response of a MWPDT system. A complete MWPDT system is built and tested to verify the performance of the proposed method. Experimental results demonstrate that the data rates can be extended from 650, 500 and 350 kbps to 850, 700 and 650 kbps at 0.4, 0.5 and 0.6 m distances, respectively. The highest data rate extension ratio is 85% at a transmission distance of 0.6 m, which is 2.4 times the radii of the coil employed in the system.

4.2. Research Background

Wireless power transfer (WPT) technology has attracted wide research efforts since Tesla demonstrated the first WPT system prototype to power up a light bulb [1, 2]. Recently, with the ever-increasing demand for Internet-of-Things (IoT) devices, WPT technology is playing an important role in charging portable devices due to its high flexibility. Among the most popular WPT techniques, such as inductive coupled power transfer (IPT) and capacitive coupled power transfer (CPT), magnetic resonance wireless power transfer (MWPT)

technique achieves a good balance between operation distance and power transfer efficiency [3]. MWPT systems are capable of transmitting power from a few milliwatts to several kilowatts over distances from a few millimeters to more than one meter [4, 5]. Therefore, MWPT systems can provide reliable charging accesses for vehicles, smart portable devices and implant devices [6-8]. The rapid growth in the number of IoT and portable devices not only challenges the existing charging systems, but also causes unprecedented pressure on wireless communication systems. Conventional radio frequency (RF) communication technology is lacking in spectrum resources and cannot provide enough communication accesses, especially under environments with a high density of users, such as airports and shopping malls. Since MWPT systems are essentially resonance tanks, the power transfer channels can potentially be used for simultaneous data transmission to support the communication function. As shown in Figure. 4. 1, magnetic resonance wireless power and data transfer (MWPDT) technology can be implemented seamlessly with the rapidly developing power line communication (PLC) technology to provide simultaneous power and internet connections for IoT devices, such as smart speakers, glasses and watches [9].

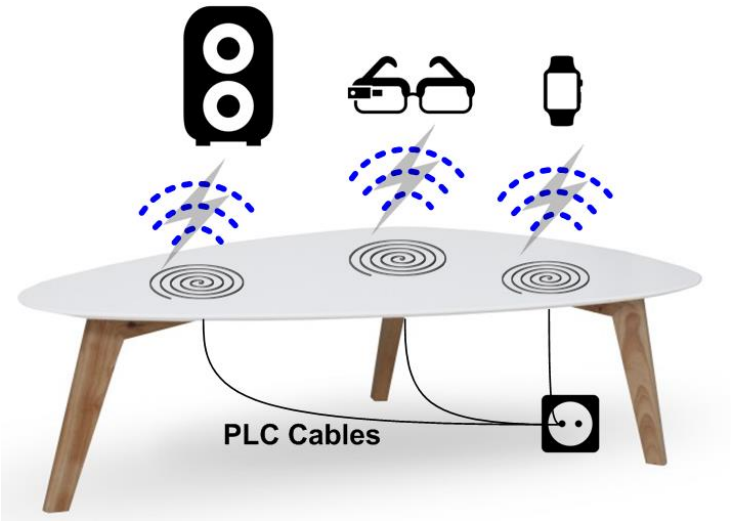

Figure. 4. 1. Integrating MWPDT and PLC technology for simultaneous charging and communication of IoT devices.

The critical problem in implementing MWPDT systems for IoT devices is the tradeoff between the high quality (Q) factor of the coils and data transmission bandwidth. With a

larger coil inductance, and therefore higher Q factor, a longer transmission distance and a higher efficiency can be achieved, but at the cost of a narrower bandwidth. There have been significant research efforts focusing on developing novel MWPDT system architectures. In [10–15], power and data were transmitted using carrier waves with separate frequencies to extend the data transmission bandwidth and reduce the cross talk. By centering the power and data carriers at lower and higher frequencies respectively, data rates of 19.2 kbps [10, 11], 20 kbps [12], 100 kbps [13], 119 kbps [14] and 560 kbps [15] were achieved and the cross talk between power and data was suppressed. In [16] and [17], power and data were transmitted at two different pairs of coils with different resonance frequencies, which was suitable for short-distance biomedical applications. In [18], backwards data transmission was achieved to send a control command from the receiver side to the transmitter side for vehicle charging and status monitoring. In [19], a novel system was proposed using trapezoidal current to transmit power and data simultaneously. The fundamental component of the trapezoidal current waveform was used to transfer power and its third order harmonic component was selected to transmit information.

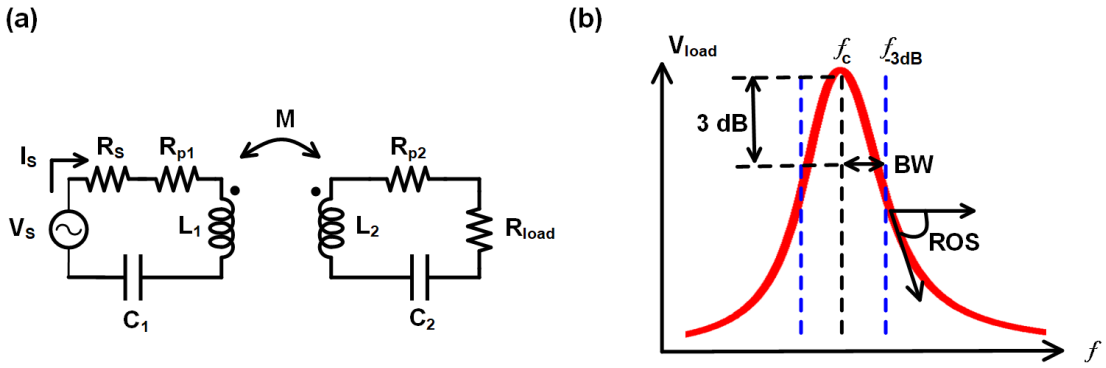

Figure. 4. 2. Principle of wireless power transfer.

(a) Circuit model of a typical two-coil s-s matching MWPT system. (b) Received voltage on the load resistor at different frequencies.

However, there still exist some challenges limiting the practical implementation of MWPDT systems. First, the method of separating power and data requires either multi-resonance structures or multi-coil systems, which increase the design complexity. Second, the problem

of the intrinsically narrow channel bandwidth has not yet been solved. In addition, the channel features of a MWPDT system, such as bandwidth and roll-off slope (ROS), varies with operation distances, which results in an unstable communication channel undesirable for wireless communication.

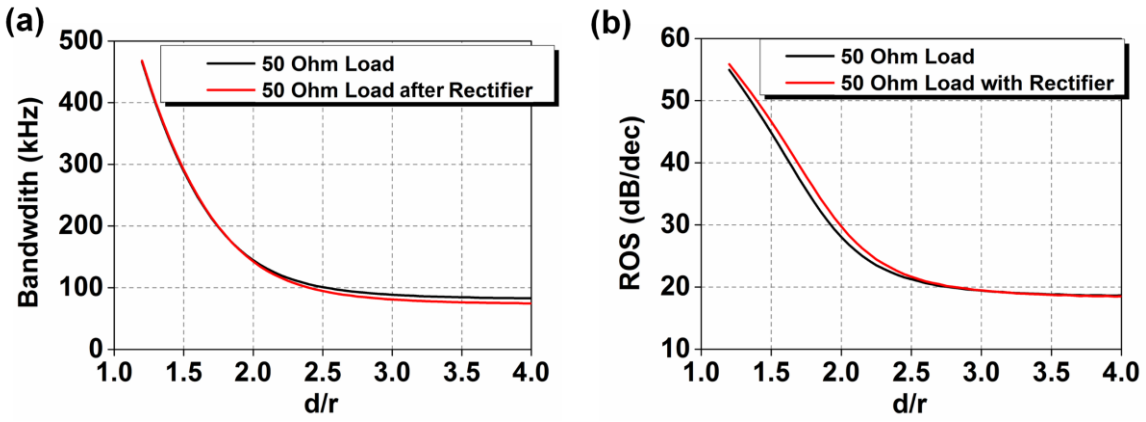

Figure. 4. 3. Calculated *BW* and *ROS* versus *d/r*. (a) Calculated variation of *BW* versus *d/r*. (b) Calculated variation of ROS versus *d/r*.

In order to solve these problems, we propose a receiver front-end (RX) circuit with three-stage cascaded equalizer (EQ) to compensate for the limited bandwidth and the distance–dependent channel response of MWPDT systems. The cascaded EQ consists of two first-order EQ stages and one second-order EQ stage. It is capable of providing a variable compensation frequency (CF), a roll-up height (RUH) and a roll-up slope (RUS) from 10 to 45 dB/dec. A complete MWPDT system with a typical series-series matching two-coil structure is built to verify the circuit performance. Experimental results demonstrate that the highest data rate can be extended from 650 kbps, 500 kbps and 350 kbps up to 850 kbps, 700 kbps and 650 kbps at distances of 0.4, 0.5 and 0.6 m, respectively with the received power as high as 2 W.

4.3. Principle of MWPDT and Variable Channel Bandwidth Equalization

The channel bandwidth and out-of-band ROS of a typical two-coil MWPT system is characterized analytically to provide a guideline for the RX circuit design. Here we consider the case when the data and power are transmitted via a shared channel and received

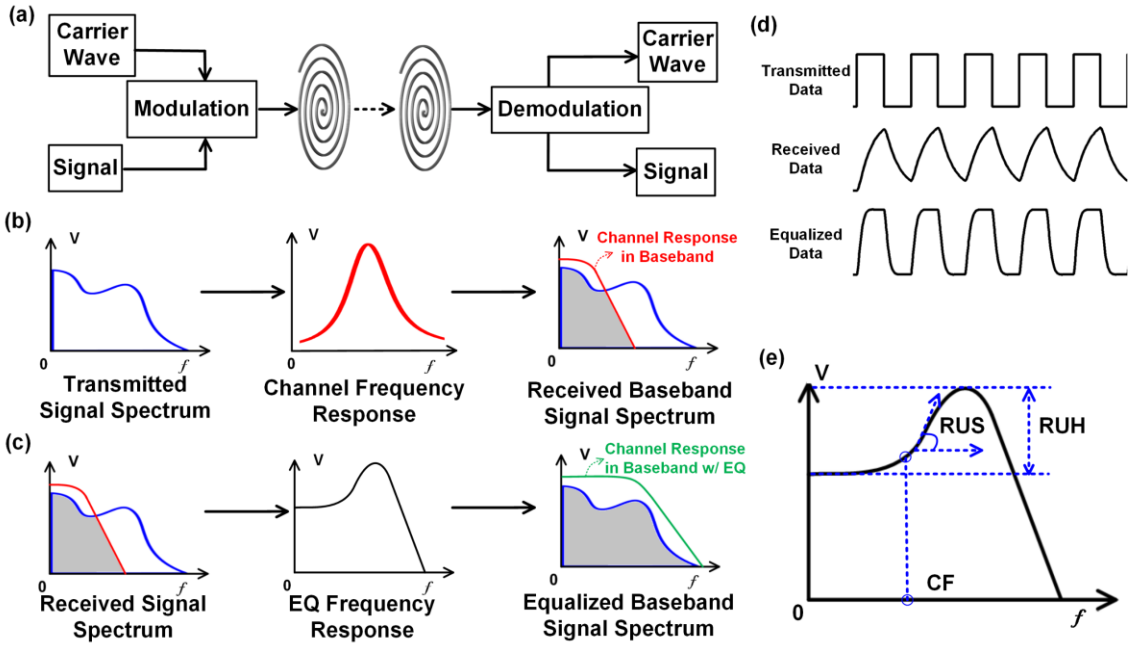

Figure. 4. 4. Principle of equalization in a MWPDT system.

(a) Block diagram of a MWPDT system.

(b) Evolution of a signal spectrum when transmitted through the MWPDT system.

(c) Principle of using an EQ circuit to extend the channel bandwidth and recover the original signal spectrum.

(d) Evolution of the baseband data signal dynamic behavior when transmitted through the MWPDT system.

(e) Definition of CF, RUS and RUH of an EQ circuit.

simultaneously on a load. A series-series (s-s) matching MWPDT system is shown in Figure. 4. 2 (a). The system consists of a signal source V_s with a source impedance R_s, a load resistor R_{load}, a transmitting L_1 , a receiving coils L_2, the coil parasitic resistances R_{p1}, R_{p2} and two matching capacitors C_1 ,C_2,. The center frequency f_c, at which maximum power transfer can be achieved on R_{load}, is determined by the resonance condition of L_1, C_1 and L_2, C_2 as follows:

$$f_c = \sqrt{\frac{1}{L_1 C_1}} = \sqrt{\frac{1}{L_2 C_2}} \tag{1}$$

The received voltage across R_{load} (V_{load}) gradually decreases when the source signal frequency deviates from f_c. The frequency point when the received voltage across R_{load} reduces by 3 dB compared to the received voltage at f_c is denoted as f_{-3dB}, as shown in Fig. 2 (b). The channel bandwidth (*BW*) is thus determined as follows:

$$BW = \left| f_{-3dB} - f_c \right| \tag{2}$$

A transmitted signal can be successfully recovered on the receiver side when the Nyquist frequency of the signal falls within *BW*. When the signal's Nyquist frequency goes outside *BW*, the intensity of the out-of-band spectrum component drops sharply so that the signal cannot be recovered properly. Out-of-band ROS describes how fast the frequency response of a MWPT system drops at frequencies outside the *BW*. As shown in Figure. 4. 3 (b), the ROS can be calculated using the following equation:

$$ROS = \left| \frac{1}{V_s} \frac{\partial V_{load}}{\partial f} \right| \tag{3}$$

In order to calculate the BW and ROS, V_{load} at different frequencies needs to be analytically calculated. The circuit equations of Figure. 4. 2 (a) are shown as follows:

$$V_s = I_s(R_s + R_{p1} + j(2\pi f L_1 - \frac{1}{2\pi f C_1})) + j2\pi f M I_L \tag{4}$$

$$0 = I_L\ (R_{load} + R_{p2} + j(2\pi f L_2 - \frac{1}{2\pi f C_2})) + j2\pi f M I_s \tag{5}$$

The mutual inductance *M* can be calculated using coupling factor *k* with the following equation:

$$M = k\sqrt{L_1 L_2} \tag{6}$$

Under the condition of symmetric transmitting and receiving coils with equal inductance *L*, equal source and load *R*, based on the (1) and (4–6), V_{load} can be calculated as follows:

$$V_{load} = \frac{-j2\pi f^3 kLR}{4\pi^2 f^4 k^2 L^2 + f^2 R^2 - 4\pi^2 L^2 (f^2 - f_c^2)^2 + j4\pi fRL(f^2 - f_c^2)} \tag{7}$$

V_{center} is also calculated as follows:

$$V_{center} = \frac{-j2\pi f_c^3 kLR}{4\pi^2 f_c^4 k^2 L^2 + f_c^2 R^2} \tag{8}$$

The design parameters of the MWPDT system are coil radii r, inductance L and resonance frequency f_c, which are determined by application specifications. Other parameters such as matching capacitors C_1 and C_2 and coupling factor k can be calculated based on the design parameters. In our system, both the transmitting and receiving coil inductances are set to 30 uH, and the coil radii are set to 0.25 m. The resonance frequency f_c is set to 4.25 MHz. The R_s is 50 Ω considering the typical RF power amplifier (PA) output load. The parasitic resistances R_{p1} and R_{p2} are 14 Ω and 7 Ω respectively.

In the case that the two coils share the same radii r and are separated by a distance of d, their coupling factor can be calculated using the following equation when d is comparable to r [20, 21]:

$$k = \frac{1}{\left[1 + 2^{2/3}(d/r)^2\right]^{3/2}} \tag{9}$$

The equation indicates that the ratio of the power transfer distance over the coil radii d/r is more meaningful and convenient for analysis.

The *BW* and out-of-band ROS can be calculated using (2), (3) and (7)–(9). The calculation is performed under two different loading conditions, a pure 50-Ω resistive load and a 50-Ω resistive load after a full bridge rectifier. The latter loading condition is in accordance with our designed MWPDT system. The equivalent resistance of a 50-Ω load after a full bridge rectifier with large filtering capacitor is 40.52 Ω [22]. The calculated *BW* and ROS versus *d/r* are presented in Figure. 4. 3 (a) and (b), respectively, which indicate that both ROS and *BW* drop with increased transmission distance. The ROS varies from 17 to 55 dB/dec when *d/r*

increases from 1.2 to 4. The bandwidth drops to below 100 kHz when *d/r* is beyond 2.5. The reason why *BW* drops with distance can be explained using the equivalent impedance seeing on the transmitter side to the receiver side as follows:

$$Z_{eq} = \frac{k^2 L_1 L_2 (2\pi f)^2}{R_{load}} \tag{10}$$

At longer distances, the coupling factor k is smaller and causes the equivalent impedance Z_{eq} to decrease. Therefore, the Q factor of the transmitter side resonant tank is larger, which leads to a narrower *BW*.To transmit data and power simultaneously through the MWPDT channel, the data signal can be modulated with a power carrier centered at f_c and transmitted through the matched coils. On the receiver side, the data signal and carrier wave are separated as shown in Figure. 4. 4 (a). Compared to transmitting data and power using separate carriers, this method requires no extra carrier for data transmission and is suitable for middle range IoT devices charging and communication. However, when transmitting a high-speed data signal with wide baseband spectrum occupation, as shown with the blue curve in Figure. 4. 4 (b), the demodulated signal is low-pass filtered due to the narrow channel *BW*. Only the signal spectrum component shown by the gray area is left as indicated in Figure. 4. 4 (b). In order to recover the original signal spectrum properly, an EQ circuit with a high-pass frequency response shown with the black curve in Figure. 4. 4 (c) needs to be implemented to compensate for the frequency response roll-off of the MWPDT channel. The overall channel frequency response with the EQ circuit is shown with the green curve and the equalized signal spectrum is shown in the gray area in Figure. 4. 4 (c). Considering transmitting a periodic square wave as a data signal, the evolution of the dynamic behavior of the signal in baseband during the transmission and equalization process are shown in Figure. 4. 4 (d). The low-pass frequency response of the MWPDT channel suppress the signal high frequency spectrum components and results in slow rising and falling edges, which can be compensated and recovered by using an EQ circuit with high-pass response.

Three parameters are used to characterize the performance of an EQ circuit, CF, RUH and RUS, as shown in Figure. 4. 4 (d). The CF specifies the frequency point when the EQ frequency response rolls up by 3 dB, which should be set as equal to $f_{\text{-3dB}}$ of the channel under compensation. The RUH describes the gain difference in frequency response between the roll-up peak and low frequency range. The RUS is the slope of the roll-up curve and should be set

variably based on the ROS of the channel. Depending on the channel features, the three parameters need to be properly optimized to extend the channel bandwidth without causing over- or under-shooting.The data signal extracted from the demodulation circuit generally features a distance-dependent narrow spectrum and unavoidably consists of some carrier wave component. Therefore, the RX circuit needs to be properly designed for variable channel bandwidth extension and carrier suppression. The basic principle of designing an EQ circuit is to create a zero in its transfer function, which provides a high-pass frequency response. The most common circuit structures to introduce zeros in EQ circuits are resistive-capacitive (RC) degeneration and inductive peaking structures. The former is capable of providing a smooth and variable CF, RUS and RUH, but at the cost of suppressing the intensity of low frequency gain, which reduces the signal-to-noise ratio (SNR). The latter has the advantages of a higher CF and easy implementation, but unavoidably leads to over- and under-shooting in the time

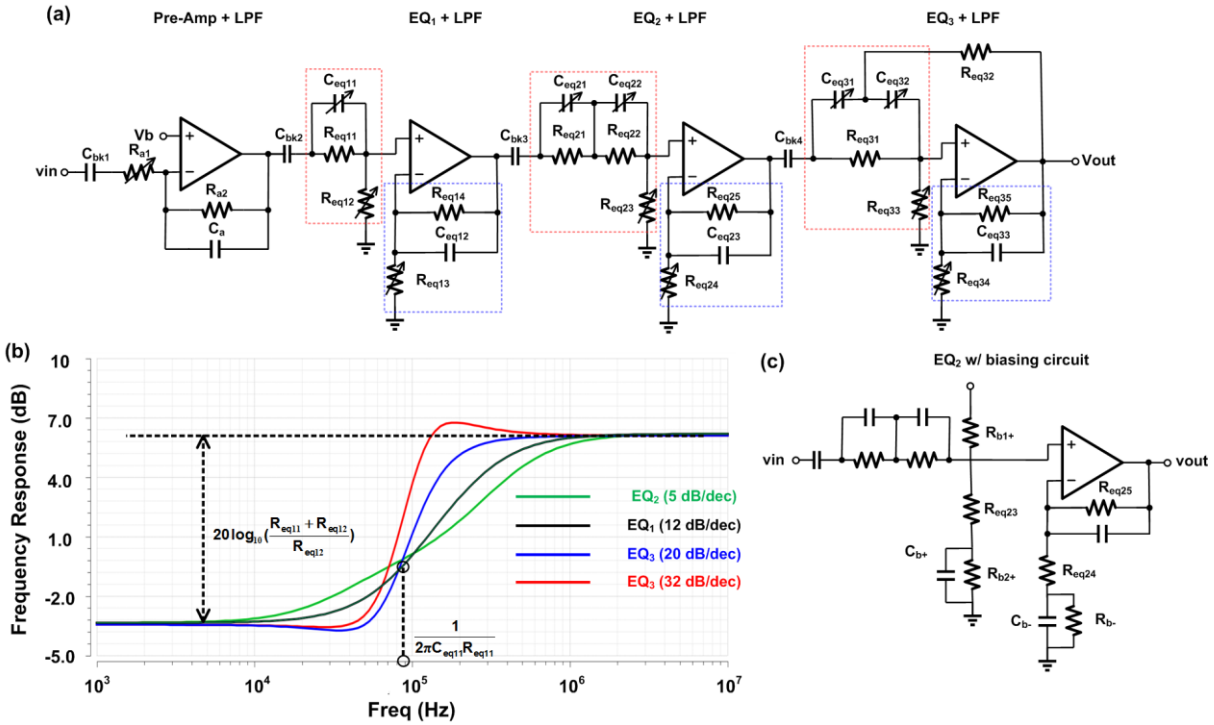

Figure. 4. 5. Schematic and simulation results of the RX circuit.

(a) Schematic of the RX circuit.

(b) Simulated frequency response of each EQ stage.

(c) Biasing method of EQ_2.

response. In addition, the CF and RUH cannot be tuned separately in inductance peaking structures. Here, targeting variable CF, RUS and RUH, we choose to use the RC degeneration active EQ structure.

4.4. System Implementations

As shown in Figure. 4. 5 (a), the proposed RX circuit is composed of a pre-amplifier (pre-Amp) and a three-stage cascaded active EQ. The pre-Amp amplifies the demodulated signal to provide enough amplitude gain for equalization. Each EQ stage consists of two sections, an RC degeneration equalization section (shown in the red box) and a gain section (shown in the blue box) to compensate for the loss in the signal's low frequency component during equalization process. A low-pass filter with a 1.5-MHz 3-dB bandwidth is implemented at the pre-Amp to suppress the carrier wave component and to keep the circuit stable [23]. The 1.5 MHz cut-off frequency is three times higher than the channel bandwidth and has little effect on the data signal spectrum.

The cascade EQ consists of three stages, EQ_1, EQ_2 and EQ_3, as shown in Figure. 4. 5 (a). EQ_1

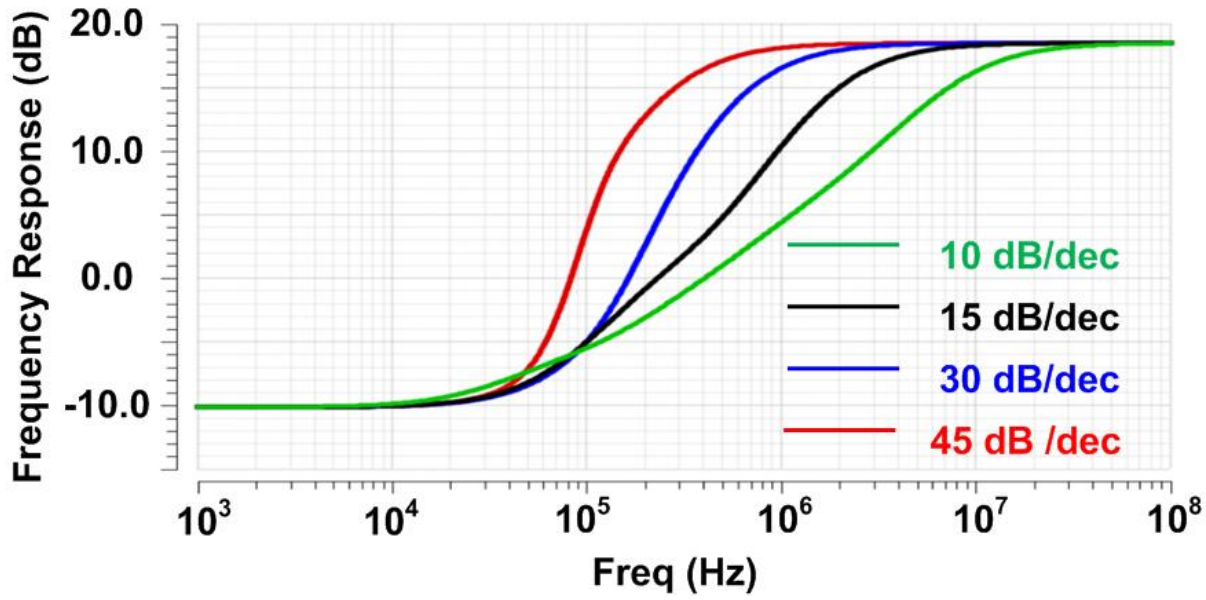

Figure. 4. 6. Simulated frequency response of the entire three-stage EQ.

is a simple first-order equalizer with R_{eq11} and C_{eq11} in parallel to introduce a single zero into the EQ section. The transfer function is shown with (11):

$$H_{EQ1}(j\omega)=\frac{R_{eq13}+R_{eq14}}{R_{eq14}}\cdot\frac{R_{eq12}}{R_{eq11}+R_{eq12}}\cdot\frac{1+j\omega C_{eq11}R_{eq11}}{1+j\omega C_{eq11}(R_{eq11}//R_{eq12})} \tag{11}$$

$$H_{EQ2}(j\omega)=\frac{R_{eq24}+R_{eq25}}{R_{eq24}}\frac{R_{eq23}(1+j\omega R_{eq21}C_{eq21})(1+j\omega R_{eq22}C_{eq22})}{(R_{eq21}+R_{eq22}+R_{eq23})+j\omega(R_{eq22}R_{eq21}C_{eq21}+R_{eq21}R_{eq22}C_{eq22}+R_{eq23}R_{eq21}C_{eq21}+R_{eq23}R_{eq22}C_{eq22})-\omega^2R_{eq21}R_{eq22}R_{eq23}C_{eq21}C_{eq22}} \tag{12}$$

$$H_{EQ3}(j\omega)=\frac{g\cdot(R_{eq33}+j\omega R_{eq32}R_{eq33}(C_{eq31}+j\omega C_{eq32})-\omega^2R_{eq31}R_{eq32}R_{eq33}C_{eq31}C_{eq32})}{R_{eq31}+R_{eq32}+j\omega R_{eq31}R_{eq32}(C_{eq31}+C_{eq32})+j\omega R_{eq32}R_{eq33}(C_{eq31}+C_{eq32})+j\omega R_{eq31}R_{eq33}C_{eq32}(1-g)-\omega^2R_{eq13}R_{eq32}R_{eq33}C_{eq31}C_{eq32}} \tag{13}$$

The first term in (11) determines the amplification of the gain section and the second term determines the suppression of the low frequency component. The third term contains a zero at $1/2\pi C_{eq11}R_{eq11}$, which determines the CF. The transfer function indicates that the RUH and CF can be controlled separately by tuning R_{eq12} and C_{eq11}. The first-order equalizer can theoretically provide around a 20-dB/dec RUS when frequency is higher than CF, but the initial RUS around CF is actually much less than 20 dB/dec. As a result, the actual simulated RUS of EQ_1 is 12 dB/dec for a 9.54-dB RUH as shown in Figure. 4. 5 (b).

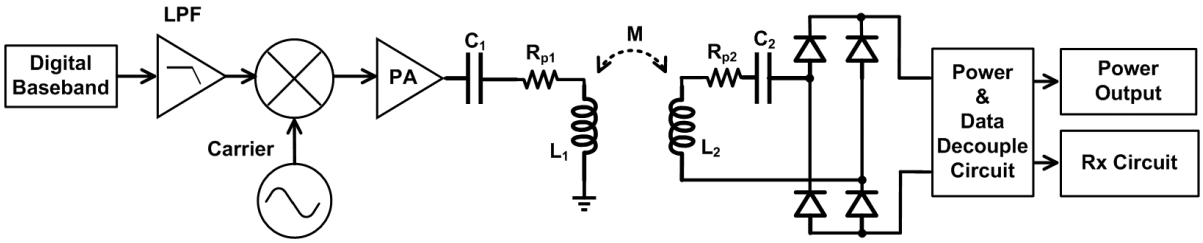

Figure. 4. 7. Block diagram of the designed MWPDT system

The slow roll-up feature around the CF is exploited in EQ_2, which is still a first-order EQ but consists of two zeros introduced by C_{eq21}, R_{eq21} and C_{eq22}, R_{eq22}. By changing the separation

between the frequencies of the two zeros, a variable smooth RUS can be generated within 12 dB/dec. A slow roll-up frequency response of EQ_2 with a 5-dB/dec RUS is obtained in simulation and shown with the green curve in Figure. 4. 5 (c). The transfer function of EQ_2 is presented in equation (12).

By cascading EQ_1 and EQ_2, a wide range of the RUS, from 5 ~ 24 dB/dec can be covered by tuning the frequencies of the three zeros. However, the slow initial RUS around the CF

Table 4. 1 Component Parameters for Rx Circuit

Parameters	Values	Parameters	Values
Req11	10 kΩ	Ceq22	1 nF
Req12	5 kΩ	Req31	10 kΩ
Req13	5 kΩ	Req32	3.5 kΩ
Req14	5 kΩ	Req33	5 kΩ
Ceq11	200 pF	Req34	5 kΩ
Req21	5 kΩ	Req35	5.3 kΩ
Req22	5 kΩ	Ceq31[a]	400 pF
Req23	5 kΩ	Ceq32[a]	400 pF
Req24	5 kΩ	Ceq31[b]	275 pF
Req25	5 kΩ	Ceq32[b]	580 pF
Ceq21	160 pF		

a. Capacitor values for generating 32-dB/dec RUS

b. Capacitor values for generating 20-dB/dec RUS

significantly limits the compensation performance when a higher RUS is necessary. Therefore, a second-order equalizer EQ_3 is cascaded to provide a variable RUS from 20 to 32 dB/dec. The equalization section of EQ_3 is still based on the RC degeneration structure but a positive voltage feedback is applied through R_{eq32} to introduce an extra zero into the transfer function, which effectively increases the RUS. To ensure stability, the gain of EQ_3 is kept below 1.5. Variable RUS can be achieved by properly setting the values of the two capacitors C_{eq31} and C_{eq32}. The transfer function is shown in equation (13), where g denotes the gain provided by the gain section of EQ_3. The simulated two different frequency responses are plotted with blue and red curve in Figure. 4. 5 (b) using different sets of degeneration capacitors C_{eq31} and C_{eq32}, as shown in Table 4. 1.

The biasing method is shown in Figure. 4. 5 (c) using EQ_2 as an example. R_{b1+}, R_{b2+} and R_{b-} are selected to be equal and much larger than R_{eq23}, R_{eq24} and R_{eq25}. Therefore, the bias voltages at the core amplifier input and output nodes are fixed to half of the supply voltage. A Capacitive coupling method is used between each stage in the RX circuit to isolate the DC bias of each circuit stage.

The entire EQ circuit is capable of providing a wide RUS tuning range from 10 dB/dec to 45 dB/dec, as shown in Figure. 4. 6. The CF and RUH can be variably set by the proper selection of degeneration capacitors and resistors. With a 6 V voltage supply from a power management circuit connected with the power filter, the RX circuit consumes a power of 30 mW. All simulation parameters for the EQ circuit are summarized in Table 4. 1.

4.5. Design of the MWPDT System

To verify the performance of the proposed RX circuit, a MWPDT system is designed, as shown in Figure. 4. 7. A series-series capacitive matched two-coil structure with a resonance frequency f_c at 4.25 MHz is employed for a shared power and data transfer channel. The Amplitude-Shift-Keying (ASK) modulation scheme is adopted here to simplify the receiver design. Compared with other modulation schemes such as Frequency-Shift-Keying (FSK) and Phase-Shift-Keying (PSK), the ASK modulated data can be recovered on the receiver side

Table 4. 2 Component Parameters of MWPDT System

Parameters	Values	Parameters	Values
Rload	50 Ω	Diode	ES3D
Cpf	400 uF	L_1	31.1 uH
Rdf1	5 Ω	R_1	14 Ω
Cdf1	31.2 nF	L_2	30.88 uH
Rdf2	50 Ω	R_2	7 Ω
Cdf2	3.12 Nf	C_1	45.1 pF
Lf	100 nH	C_2	45.41 pF

using only passive components such as rectification diodes and cascaded filters, which gets rid of active circuits such as mixers and local oscillators and is more suitable for low power IoT devices. The data signal from the baseband is modulated with a 4.25-MHz power carrier wave, amplified using an RF PA and then transmitted through the MWPDT channel. After rectification using a full bridge rectifier, a PDD circuit based on cascaded filters is applied to recover the power and data signal and the RX circuit is connected in series following the PDD circuit for the variable channel compensation.

The received signal from the receiving coil consists of three frequency components, DC power, low-frequency data signal and high-frequency carrier wave component. A cascaded three-stage filter is applied to separate different frequency components as shown in Figure. 4. 8 (a). The normalized frequency response of each stage is calculated analytically and presented in Figure. 4. 8 (b). For power extraction, a 400-uF capacitor is connected in parallel with a standard 50-Ω load to create a low-pass filter to separate the DC power component. A second-order low-pass filter consisting of C_{df1}, R_{df1}, C_{df2} and R_{df2} is used to extract the data signal. The small signal input impedance of the RX circuit is 5 kΩ and does not affect the performance of the filter. The frequency response of the second-order filter features a sharp out-of-band ROS and can better suppress the influence of the carrier component, as shown with the blue solid curve in Figure. 4. 8 (b). Since $R_{df1} << R_{load}$, the data filter has very little effect on the power extraction at low frequencies. The pole of the second-order filter is set to 1 MHz, which is over two times higher than the channel bandwidth under testing and does not affect the high-speed data extraction. The extracted data signal across C_{df2} will be fed into the RX circuit for further processing. A small inductor is connected in parallel to suppress the effect of the carrier on power and data extraction. The transfer functions of the power, data and carrier filters are shown in equations (14)–(16). All component parameters used in the design are shown in Table 4. 2.

.

$$H_{power}(j\omega)=\frac{R_{load}(1+j\omega C_{df1}R_{df1})}{R_{load}(1+j\omega C_{df1}R_{df1})+R_{df1}(1+j\omega C_{pf}R_{load})+j\omega L_f(1+j\omega C_{df1}R_{df1})(1+j\omega C_{pf}R_{load})} \tag{14}$$

$$H_{data}(j\omega)=\frac{R_{df1}\dfrac{1+j\omega C_{pf}R_{load}}{1+j\omega C_{df2}R_{df2}}}{R_{load}(1+j\omega C_{df1}R_{df1})+R_{df1}(1+j\omega C_{pf}R_{load})+j\omega L_f(1+j\omega C_{df1}R_{df1})(1+j\omega C_{pf}R_{load})} \tag{15}$$

$$H_{carrier}(j\omega)=\frac{j\omega L_f(1+j\omega C_{df1}R_{df1})(1+j\omega C_{pf}R_{load})}{R_{load}(1+j\omega C_{df1}R_{df1})+R_{df1}(1+j\omega C_{pf}R_{load})+j\omega L_f(1+j\omega C_{df1}R_{df1})(1+j\omega C_{pf}R_{load})} \quad (16)$$

4.6. Experimental Setup and Measurement Results

Figure. 4. 9 shows the fabricated PCB for the rectifier, power management circuit, PDD circuit and RX circuit. Figure. 4. 10 shows the complete system with a 1.5 W light emitting diode (LED) used as the load and a pseudo random binary sequence-7 (PRBS-7) used as the testing data pattern. The decoupled power and data are fed into the load and an oscilloscope respectively after transmission through the MWPDT system. The received waveforms are

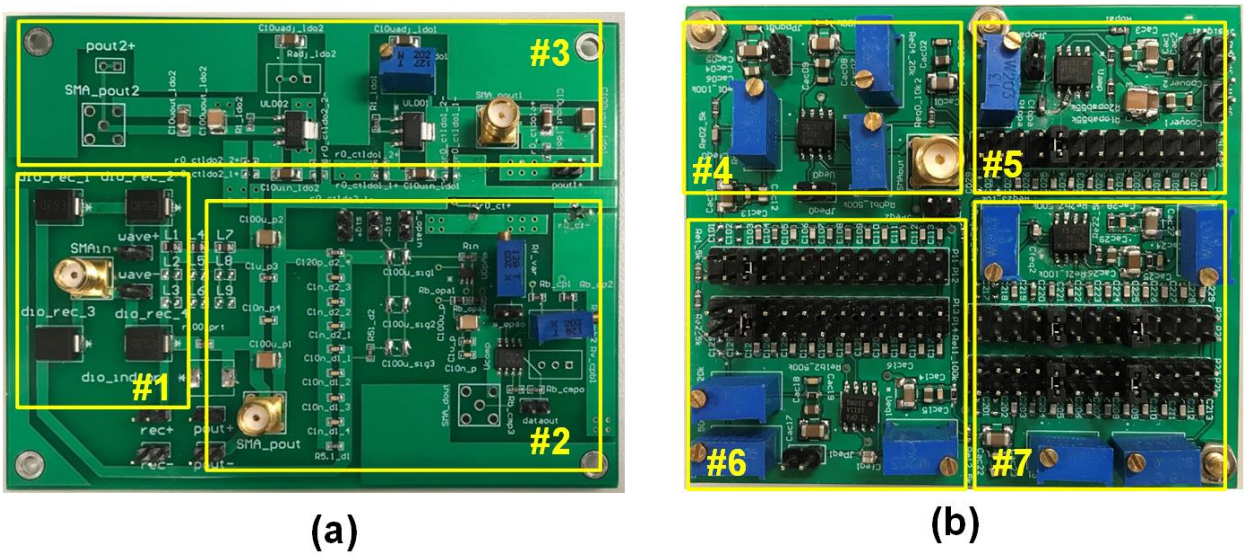

Figure. 4. 9. PCB modules of the receiver system.

(a) The PCB of the full bridge rectifier (#1), the PDD circuit (#2) and the power management circuit (#3).

(b) The PCB of the RX circuit, including the pre-Amp (#4), EQ1 (#5), EQ2 (#6) and EQ3 (#7).

plotted into eye diagrams to directly show the data transmission quality. The radii of the coils are 0.25 m and the system is tested at 0.4, 0.5 and 0.6 m, which correspond to a *d/r* ratio of 1.4, 2.0 and 2.6, respectively. The highest transmitted power is 2 W across a 50-Ω load at 0.4 m distance.

First, we show the variation of data transmission quality with transmission distances. Eye

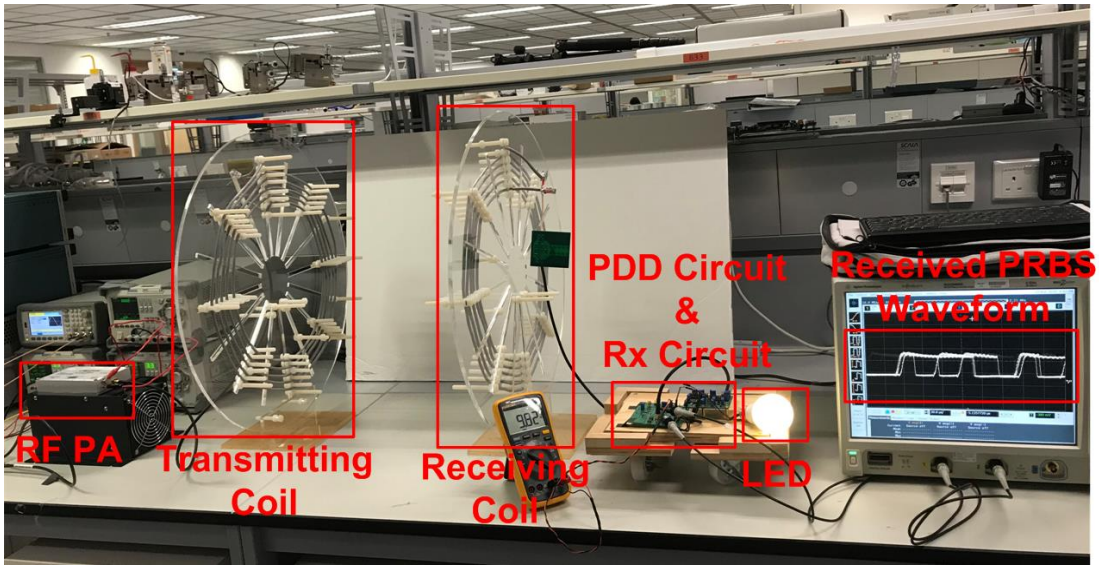

Figure. 4. 10. Experimental setup of the complete MWPDT system.

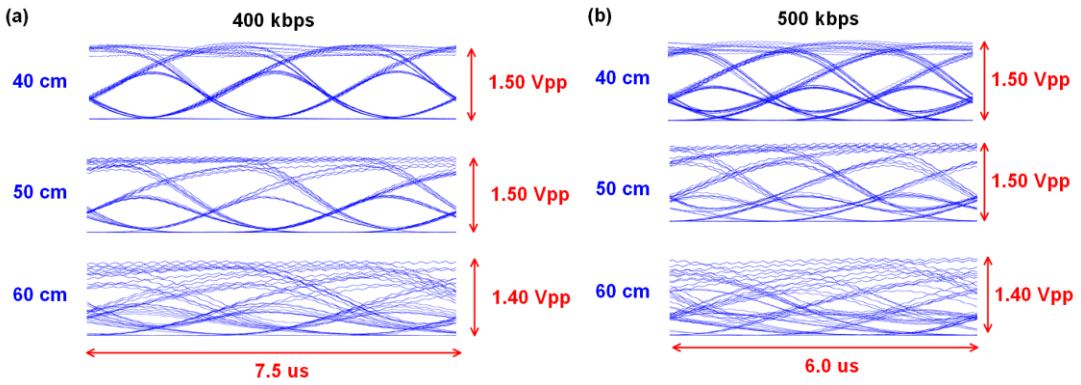

Figure. 4. 11. Measured eye diagrams without equalization

(a) Eye diagrams at 400 kbps over 0.4, 0.5 and 0.6 m distances, respectively.

(b) Eye diagrams at 500 kbps over 0.4, 0.5 and 0.6 m distances.

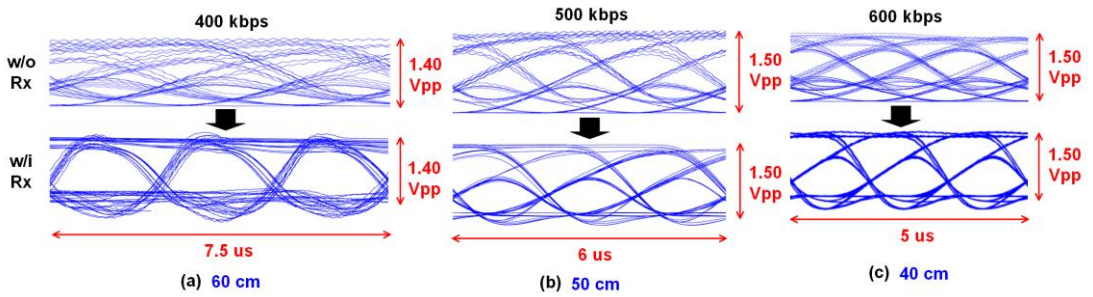

Figure. 4. 12. Measured eye diagrams with equalization.

(a) Eye diagrams at 400 kbps over 0.6-m distance.

(b) Eye diagrams at 500 kbps over 0.5-m distance.

(c) Eye diagrams at 600 kbps over 0.4-m distance.

diagram is a common tool for evaluating the quality of received data signal, which is generated by repetitively overlapping the data patterns of PRBS-7 within 3-bit time. The eye diagrams (*Eye*) can be plotted from data signal (V_{data}) using the equation below.

$$Eye(t) = V_{data}(t + n \times 3T_b) \qquad 0 < t < 3 \times T_b \qquad (17)$$

Here n is any integer number no less than 0 and T_b is the bit period.

The measured eye diagrams under different distances without employing the proposed RX are presented in Figure. 4. 11 (a) and (b) for 400 and 500 kbps respectively. At a 400-kbps data rate, the eye diagram over a 0.4-m transmission distance is still widely opened. However, the eye opening is smaller when the distance is increased to 0.5 m and become completely closed at 0.6 m. When the data rate is further increased to 500 kbps, the eye diagrams at the three distances become obviously worse compared to 400 kbps due to the limited bandwidth. Eye diagrams at both 50 and 60 cm are closed. However, by applying the proposed RX circuit to compensate for the narrow and distance-dependent bandwidth, the data transmission quality is significantly improved. The comparison of eye diagrams with and without the RX circuit at various distances are shown in Figure. 4. 12. Under all these distances, the original eyes are completely closed, which means the tested data rates exceed the upper limit of the original MWPDT system. After applying the RX circuit, the recovered eye diagrams are widely opened with a sufficient signal amplitude for eyes digitizing. The measured bit error rates (BERs)

under different transmission distances and data rates are presented in Figure. 4. 13. Based on the forward-error-correction limit of 3.8×10^{-3}, a highest data rate extension ratio of 85 % can be achieved from 350 kbps to 650 kbps at 0.6 m. The highest data rates of the implemented MWPDT system under different conditions with and without the RX circuit are summarized in Figure. 4. 13.

The power transfer capacity is measured at different data rates and distances by directly testing the received voltage across a 50-Ω resistive load, which is the typical resistance for general electronic application. Targeting at the charging and data transmission for IoT devices, the typical received power of around 2 W is measured at 100 kbps over a 0.4 m distance. The measurement setup, waveforms and received voltage are shown in Figure. 4. 14 (a) and (b). The received power at different distances and data rates are presented in Figure. 4. 14 (c). Under each distance, the received power gradually decreases at higher data rate. The reason is that after modulating the power carrier with the data signal, the spectrum of the transmitted signal is broadened and distributes evenly around f_c. Therefore, at higher data rate, the transmitted signal spectrum partly deviates from the f_c and causes the received power to decrease. The power transfer efficiency is obtained by dividing the received power with the total transmitted power, which is calculated from the integration of the output voltage and current from the PA. Here the current is obtained by measuring the voltage across a series 3.9-

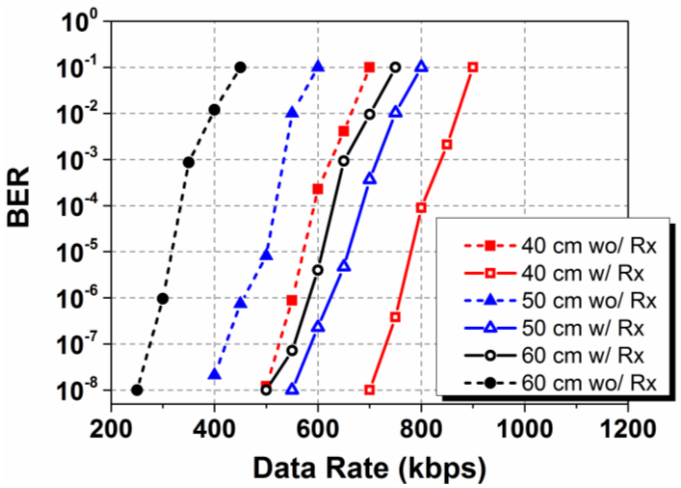

Figure. 4. 13. BERs at different data rates under 0.4, 0.5 and 0.6 m transmission distances.

Table 4. 3. Highest data rates under different distances

	d = 0.4 m	d = 0.5 m	d = 0.6 m
wo/ Rx circuit	650 kbps	500 kbps	350 kbps
w/ Rx circuit	850 kbps	700 kbps	650 kbps

Ω testing resistor on the transmitter side, as shown with light pink curve at the bottom of Figure. 4. 14 (b). The efficiency is limited to below 50% due to the fact that a 50-Ω resistor is applied at the output of the RF PA for impedance matching. The power transfer efficiencies at all three distances gradually decrease at higher data rates. The reason is that when the transmitted signal spectrum gets broadened and deviates from the center resonance frequency, the coil inductances and the matching capacitors cannot completely cancel with each other, therefore the power factor of the system drops, which leads to a higher loss on the parasitic impedance in the system.

4.7. Conclusion and Discussions

This paper presents a RX circuit consists of a pre-Amp and a three-stage cascaded EQ, which is capable of providing a variable CF, RUH and RUS to compensate for the distant-dependent MWPDT channel BW and out-of-band ROS. The three-stage cascaded EQ is composed of two first-order EQ stages and a second-order EQ stage. The proposed EQ can cover a wide RUS tuning range from 10 dB/dec to 45 dB/dec. A complete MWPDT system based on a two-coil structure is built to verify the performance of the RX circuit. Experimental results demonstrate that an 85 % data rate extension from 350 kbps to 650 kbps has been achieved at a transmission distance of 0.6 m, which is 2.4 times the radii of the coils. The proposed method is also applicable to other MWPDT architectures, such as dual resonances structures and multi-coil structures, to extend the narrow channel bandwidth.

The proposed design modulates the data signal onto the power carrier and transmits the modulated wave through the single channel. This method gets rid of using an extra carrier wave for data transmission and simplifies the design to a single channel system, which is suitable for

middle range operation. For short-range and high power MWPDT systems, directly modulating the data on power carrier leads to a higher signal peak to average ratio (PAPR), which requires PA with larger linear range. Therefore, a dual coils or dual resonances systems can be implemented to transmit power and data simultaneously through separate channels. The proposed equalization method is still applicable to these data transmission channels to extend the communication bandwidth.

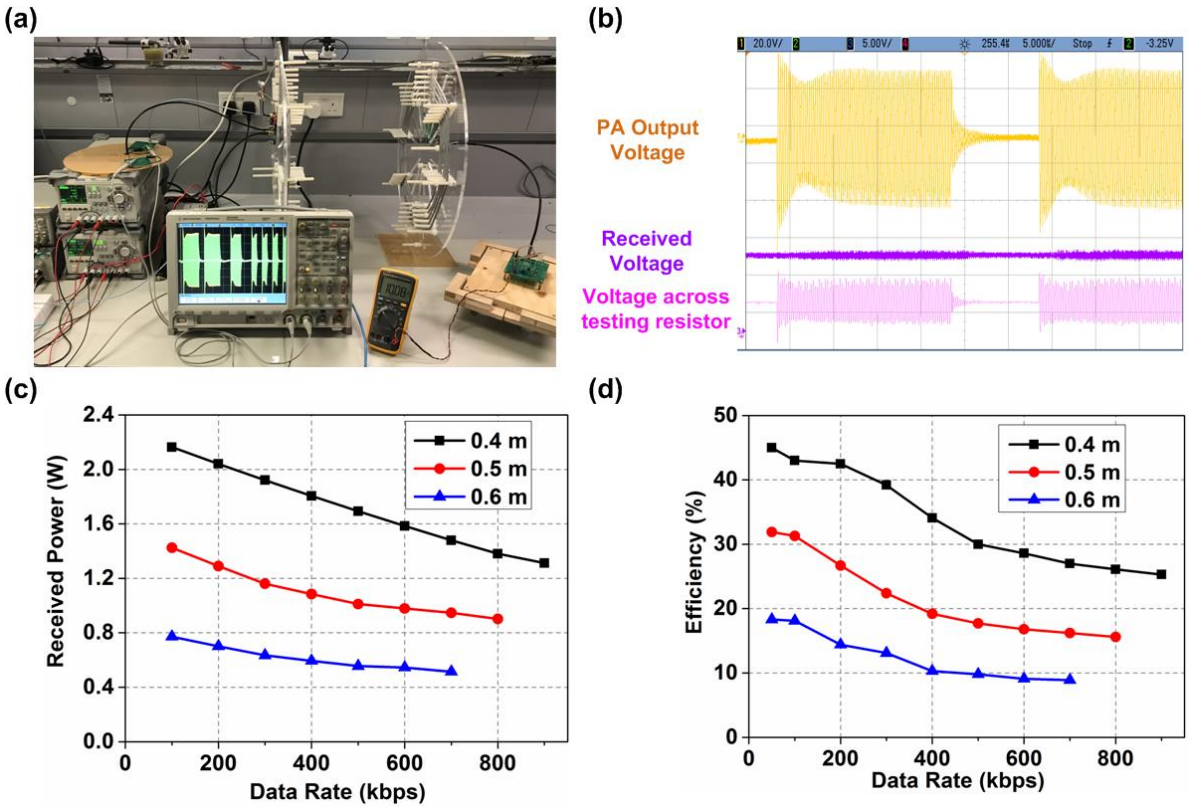

Figure. 4. 14. Experimental setup and results on power transfer capacity measurement.

(a) Measurement setup for the power transfer capacity and efficiency testing at 100 kbps over 0.4 m distance.

(b) Collected waveforms of the PA output voltage at the transmitter side, received voltage across a 50-Ω load resistor and voltage across a 3.9-Ω testing resistor for calculating the PA output current.

(c) And (d) measured received power and power transfer efficiency at different data rates over 0.4, 0.5 and 0.6 m distances, respectively.

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Chapter 5 Conclusion, Future Work and Publications

5.1. Summary of contributions

This thesis focuses on developing bandwidth extension, device nonlinearity compensation and jitter attenuation schemes for optical wireless and wireline communication systems.

This work first proposed a thermometer-code controlled RGB PAM-4 optical wireless transceiver system. First, benefitting from the thermometer-coded transmitter architecture, the three eye heights of the optical PAM-4 signal can be balanced through tuning the RGB LED units individually. Second, by optimizing the FFEs accompany the RGB LED drivers separately, the difference in LED frequency responses can be eliminated. Third, a three-stage cascaded CTLE is used as post-equalization is employed to further extend the overall system bandwidth. The equalization and nonlinearity compensation schemes proposed in this work can be extended to other optical communication systems with different light sources.

Second, a 60-Gb/s 1/4-rate PAM4 Rx with a JCCDR to overcome the stringent trade-off between JTRAN and JTOL BW. The jitter compensation circuit utilizes the DLL filter voltage to produce a complementary control signal VLF_{INV}, which modulates a group of complementary voltage-controlled delay lines so to negate the JTRANs on the recovered data and clock signals. The proposed 40-nm CMOS Rx test chip achieves error-free operation with PAM4 input from 30 to 60 Gb/s. The JCCDR achieves a 40-MHz JTOL BW with over 0.2-UIPP jitter amplitude while maintaining a -8-dB JTRAN. A jitter compensation ratio of around 60% has been achieved up to 40 MHz.

Finally, a wireless power and data transmission system is developed with enhanced communication bandwidth using the proposed cascaded equalization system. The cascaded CTLE is capable of providing a variable high-pass frequency response, which can compensate for the WPT system bandwidth variation.

5.2. Future work

Although this work proposed a PAM-4 transceiver to extend the bandwidth for optical wireless communication, much more research efforts will be needed to develop a practical system compatible with 5G network. The present LED-based optical wireless communication is only suitable for indoor communication with IoT devices requiring low communication speed. In outdoor wireless Fronthaul application, LD-based optical wireless communication will be an attractive solution. The architecture for LD-based optical wireless communication will consist of digital-to-current LD driver, look-up-table for controlling the driving and equalization current, and clock synthesizer using ring oscillator. The overall transceiver can operate in full-rate to simplify the system architecture. Benefitting from the high signal-to-noise ratio of LD, higher-level modulation scheme, such as PAM-8, can be adopted to further boost the data rate within the same analog bandwidth.

In the optical wireline communication side, the present system relies on a voltage-controlled delay line to achieve phase locking. However, when there is small frequency error between the reference clock and the symbol rate of input data, the DLL control signal will be periodically disturbed, and cannot achieve a stable locking state. In future work, phase interpolator-based CDR can be used to accommodate small frequency error, and still enjoy the jitter compensation merits using the proposed architecture. On the other hand, by using scaled process, such as 14-nm or 28-nm CMOS, the future receiver design will focus on extending the data rate up to 224 Gb/s. At such data rate, the receiver architecture needs to adopt several enhancements, such as using 28-GHz LC-PLL to provide quarter-rate clock, using active inductor to reduce the chip area, and using inverter-based front-end to support down-scaled power supply.

5.3. Publications

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