Electromagnetic Interference Related Common-Mode Noise Issues in High-Speed CMOS Serializer/Deserializer Transmitter

by

Khawaja Qasim Maqbool

A Thesis Submitted to
The Hong Kong University of Science and Technology
in Partial Fulfillment of the Requirements for
the Degree of Doctor of Philosophy
in the Department of Electronic and Computer Engineering

Jan 2018, Hong Kong

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Department of Electronic and Computer Engineering

Jan 2018

To my wife

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ABSTRACT

All electronic systems have inherent noise sources and a certain percentage of energy radiating from the system. The distorted differential signal in a communication link generates an unwanted common-mode (CM) component more severely at the backplane connector at twice the Nyquist frequency or at data rate frequency and harmonics (F_{dr}). The CM components are eventually radiated by the PCB parasitic antennas and degrade electromagnetic compatibility (EMC) performance. Regulatory bodies, for instance the Federal Communication Commission (FCC) and International Special Committee on Radio Interference (CISPR), prescribe a limit to control maximum radiation. It is therefore essential for systems-on-chip (SOCs) with high-performance digital large-scale integration (LSI) and RF/analog circuits to have less electromagnetic radiation and to minimize electromagnetic interference (EMI) inside active devices. Meeting these guidelines becomes more challenging at high speed, as higher frequencies radiate more efficiently through small openings. Therefore, EMI is a challenging issue for packaging and PCB design at high speed. The EMI issue usually comes up late in the system, around the developmental stage, and requires a costly solution that is difficult to implement. Therefore, it is essential to counter the EMI issue during the product design phase instead of handling it at the end of product development. In this thesis, EMI-related common-mode noise is investigated in three stages: (1) identification of CM noise sources, (2) analysis and prediction of CM noise of the output driver and parallel I/Os and (3) suppression of CM noise.

In the first stage, the predominant source of CM noise is identified by a simplified communication link model, which only considers the non-idealities of the signal source and passive link. The signal source is an output of a high-speed serializer/deserializer (SERDES) transmitter (Tx), and the passive link is comprised of packaging and PCB interconnections. The CM voltage spectrum profile is categorized into two types of distortions, namely, linear distortion and non-linear distortion. The linear distortion is produced by skew, loading and amplitude mismatch between P/N channels, whereas the rising/falling edge mismatch is categorized as non-linear distortion since it produces a large power component at $F_{dr,}$ causing a radiation issue and degrading the EMC performance. Analysis reveals that the non-linear active circuit predominantly produces the asymmetric rise and fall time of the output signal and is an intrinsic source responsible for generating the CM noise.

In the second stage, we present a novel methodology to systematically analyze and predict the CM noise of an output driver from various dependent parameters, including CMOS process corners, input signal, power supply and passive interconnections. Comprehensive analysis and prediction of EMI-related CM noise for a 20-Gb/s output driver in a 65-nm CMOS process is presented. Due to the NMOS-PMOS configuration in the push-pull driver, CM noise level variations are aggravated under process corners. The process corner variations can increase the CM noise up to 7.6x from a baseline level, a far greater impact than that of the other parameters. The EMI issue grows in complexity as the data rate per lane and the number of parallel lines continue to grow rapidly. Due to the high integration density, the CM noise can become a serious issue and can result in an inablility to meet FCC's code of regulations.

Finally, we present the CM noise suppression of 20-Gb/s parallel I/Os using an on-chip slew-rate controller circuit in a 65-nm CMOS process. The critical step in controlling the CM noise is at the source, rather than improving the matching of passive interconnections. The CM noise issue is effectively circumvented by producing a matched slew-rate. The proposed arhcituecture balances the pull-up and pull-down network of ouput driver results in 20% increase in symmetry of rising and falling edge and reduce the peak CM noise by 5.4x. The calibrated output driver-produced matched slew-rate, besides providing a CM noise improvement, also helps in achieving better signal quality by increasing the vertical eye opening by 18 mV. Circuit design guidelines to control CM noise from the signal source during the design stage are also presented.

ACKNOWLEDGEMENT

First and foremost, I express my sincere gratitude to my supervisor Prof. C. Patrick Yue for his high-level guidance, farsighted advice, and consistent encouragement. He was more than a supervisor to me; his endless energy, innovative ideas and dedication always motivated me to work harder in the lab. Any good result originating from my research is a tribute to his conviction and forbearance. Apart from research, I learned the art of putting faith in one's students, making them independent and letting them walk on their own. His guidance and training has left indelible imprints on the corridors of my mind and will always remain an integral part of my life. I will cherish it throughout my life, and deal with my own students as he does.

Appreciation and deep gratitude are also due to my school, college and university teachers, all of whom have had a part in shaping me to be a better student, engineer, and researcher. I would like to thank my teachers at HKUST Prof. Mansun Chan, Prof. Philip K.T. Mok, Prof. Kevin Chen, Prof. Amine Bermak, Prof. Howard Cam Luong and Prof. Wing-Hung Ki for teaching me the fundamental and advanced concepts of analog and high-frequency IC design, for which I will remain truly grateful. I would like to thank my thesis proposal committee: Prof. Chi-Ying Tsui and Prof. Wei Zhang for giving me valuable comments to widen the scope of my research from various perspectives. I would also like to thank Prof. Nan Sun for serving as the external committee member.

At the Optical Wireless Lab (OWL), my research group, I have been lucky to have Babar Hussain as my friend, colleague and brother. His support, appreciation and confidence in me meant a lot during my hard times. I would like to thank Duona Luo for the collaborative work on the Huawei project; I have learned so much from him through our conversations. I would also like to thank Guang Zhu, Milad Kalantari Mahmoudabadi, Dr. Haikun Jia, Dr. Quan Pan, Xianbo Li, Dr. Yipeng Wang, Liwen Jing, Zhixin Li, Fengyu Che, Liusheng Sun, Dr. Xiangyu Meng, Dr. Zhao Zhang, Clarissa Prawoto and Salahuddin Raju for all the inspiring discussions and enjoyable time I have had in the last four years. Thanks must also be given to all the conscientious technicians and staff at HKUST, in particular, S.F. Luk, K.W. Chan and Fred Kwok for their technical assistance; Kenny Pang for computing server maintenance; and Foner Chan for accounting assistance.

As they say, the best things in life are the people you love, the places you've been and the memories you've made along the way. I am fortunate to have travelled to the USA and Taiwan for conferences and China for the advanced CMOS summer school during my graduate studies.

I can't thank my supervisor and university enough for the support and travel funding. Apart from those in the OWL lab, other friends from HKUST have been equally supportive and gracious during my research journey in Hong Kong. I have had a great time with Dr. Moaaz, Irfan, Asad, Faheem, Saqib, Zubair, Dr. Khawar, Dr. Awais, Salman, Dr. Kashif and many others. We made lots of fond memories at weekend dinners, on hiking trails and on kayaking trips, which really helped to detox me from the stress and strain of graduate research.

I would like to thank my parents and siblings for being a constant source of support and inspiration. Their prayers and unconditional love have always raised me up during the hard times. I dedicate this work to my wife, Raazia Altaf, and son, Ahmad, who have sacrificed a lot during the past four years. I consider myself the luckiest man on earth to have such a beautiful, supportive and considerate wife. She looked after our autistic son with the utmost care, love and forbearance when I was busy working late nights in the lab. I know I couldn't give much time to my family, for which I render my deepest apologies and will try my best to make up for in the future.

Last, but not the least, I am deeply indebted to the people of Pakistan and Hong Kong. It is with their tax money that I was able to acquire a world-class education and research training via fully-funded scholarships over most of my academic career.

I would like to conclude with a quote by Hazrat Ali ibn Talib,

There is no greater wealth than wisdom, no greater poverty than ignorance; no greater heritage than culture and no greater support than consultation.

and

"Stay Hungry. Stay Foolish." a motto for my life ahead.

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Chapter 1 INTRODUCTION

1.1 Research Background

With an increasing data rate and number of parallel I/Os, transmitter (Tx) power continues to increase, and, as a result, more energy is present inside shielded enclosures [1]. The radiating energy issue thus becomes more complex as the data rate increases [2]. It is therefore essential for systems-on-chip (SOCs) with high-performance digital large-scale integration (LSI) and RF/analog circuits to have less electromagnetic radiation and to minimize electromagnetic interference (EMI) inside active devices [3]. In the high-speed backplane interconnection on PCB board, EMI is always a challenge for package and PCB designers.

As shown in Figure 1, the signal goes from the chip, through the package passive path on board and reaches the backplane interconnector with the motherboard. Generally, electromagnetic compatibility (EMC) issues become most severe at the interconnector, which is the location of V_c in Figure 1, and signal energy is easily radiated at that spot, especially the common-mode component of the output. Before the signal reaches the backplane connectors and gets radiated, it goes through the passive interconnection from the chip output and any distortion in between affects the final signal profile. Then to control the radiated power for the purpose of EMC, the noise power before the backplane connector must be minimized.

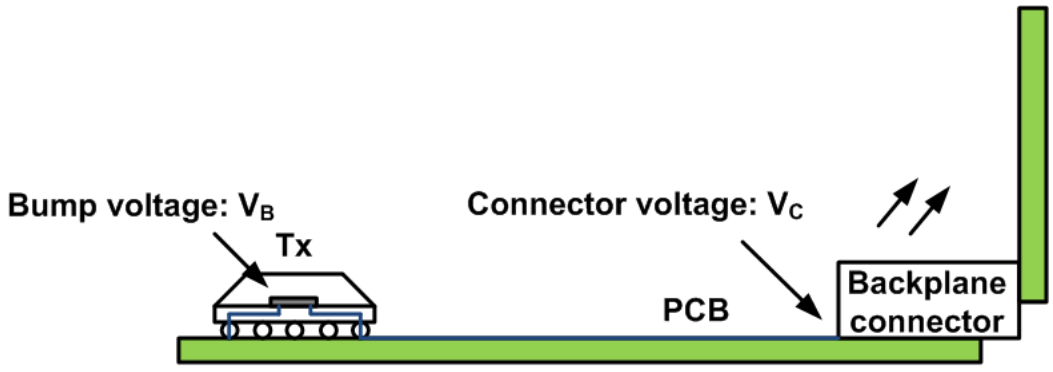

Figure 1. SERDES backplane environment: goes through the package then to passive PCB path and interconnections.

Theoretically, the spectrum of an ideal differential pseudorandom binary signal (PRBS) signal has a notch near the data rate frequency and its harmonics, while its common-mode (CM) voltage contains only the DC component. The distorted differential signal in a communication link generates an unwanted common-mode component more severely at the backplane

connector at double the Nyquist frequency or at data rate frequency and harmonics (F_{dr}), as shown in Figure 2.

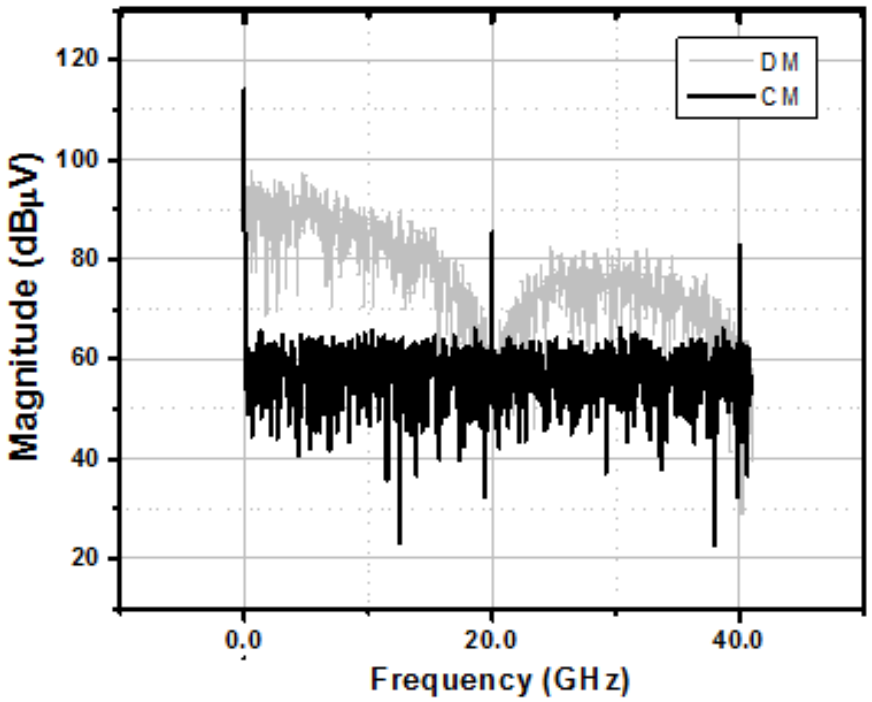

Figure 2. DM and CM spectrum of output signal at 20 Gb/s.

The CM components are eventually radiated by the PCB parasitic antennas and degrade EMC performance. The CM radiation is generally more significant than differential-mode (DM) radiation and therefore suppressing CM noise is essential for improving EMC performance. Regulatory bodies, such as the Federal Communications Commission (FCC) and International Special Committee on Radio Interference (CISPR), prescribe a limit on maximum radiation. For instance, the FCC's Code of Federal Regulations (CFR), Part 15, Subpart B refers to unintentional radiation for class A and B devices, including high-speed serializer/deserializer (SERDES) Txs, and their radiation limits are shown in Figure 3 [4].

The maximum allowable limit translates into a far electric field limit of 0.5 mV/m and 1 mV/m for class B and class A devices, respectively, at a distance of 3m, where class B devices' radiated emission limit is usually desired. Meeting these guidelines becomes more challenging at high speed as higher frequencies radiate more efficiently through small openings. The EMI issue usually comes up late in the system, around the developmental stage, and requires a costly solution that is difficult to implement [5]. Therefore, it is essential to counter the EMI issue during the product design phase instead of handling it at the end of product development [1], [5].

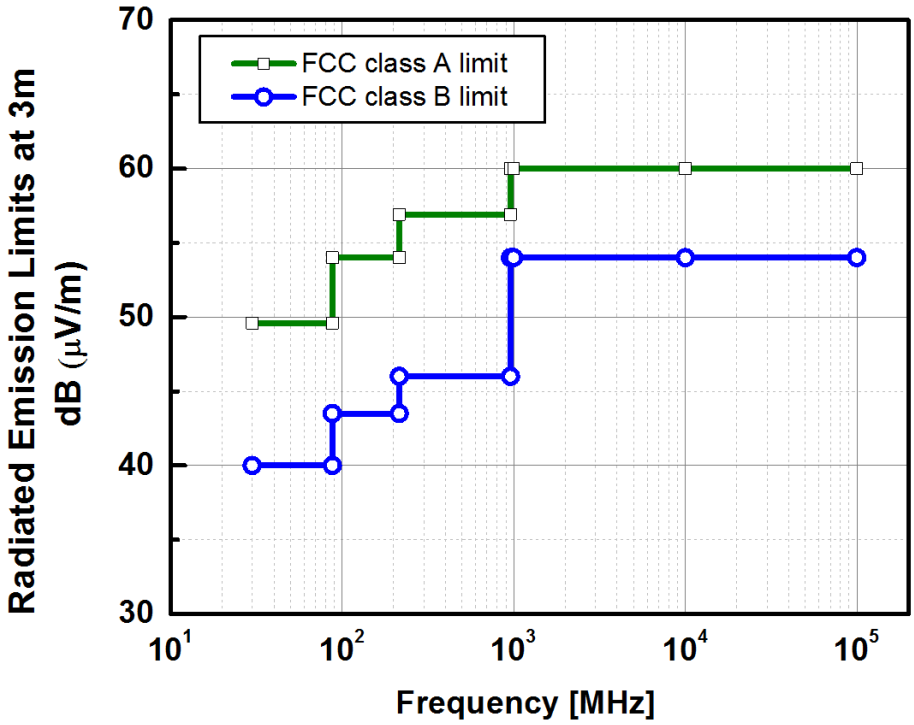

Figure 3. CFR, Part 15, Subpart B radiated emissions limits for class B and class A devices translated for a 3 m distance.

The relationship between the EMI and signal slew-rate is presented in [6] and [7], and reduction of the slew-rate as a means of suppressing EMI is proposed. A slew-rate controller and process, voltage and temperature (PVT) variation detector, regulating the slew-rate of the output driver is implemented in [7] and [8]. However, the CM noise is dependent on the mismatch of the rise and fall time rather than the absolute or RMS value of the rise and fall time [9]. Therefore, reducing the slew-rate will not result in improving the overall EMC performance.

A few recent studies on EMI issues on passive paths and high-speed I/O connectors have been reported. A quantitative EMI analysis of electrical connectors is presented in [1]. Similarly, in [2], it is shown that lack of signal path symmetry results in channel-generated skew, and its compensation and potential impacts on EMI performance are discussed. However, the CM noise is mainly contributed by the non-linear active circuit, and the CM noise from the signal source alone effects most of the output CM noise profile, whereas the mismatch between the P and N channels only provides slight mode conversion between the DM and CM. Therefore, the matching of passive links cannot improve the CM noise performance significantly [10].

Filtering and shielding are the conventional techniques to control CM noise by reducing the parasitic capacitance and CM current, and also to provide a local and compact CM current path to return to its source [11]. However, filtering is dependent upon the particular PCB, requiring specialized expertise, and can still lead to multiple PCB iterations. Shielding, meanwhile, is an expensive solution and not an option in open-box equipment, such as computer cards, which are intended to be plugged into another unit [11], [12].

1.2 Thesis Contributions

Due to the non-idealities in the active and passive parts of a communication link, CM noise analysis and prediction is non-trivial. Consequently, comprehensive CM noise analysis and prediction of a SERDES I/O driver has rarely been reported. Similarly, while lots of work has been done on conventional EMI reduction techniques and on matching of passive interconnections, little has been done on CM noise suppression from the signal source.

In this thesis, the predominant source of CM noise is identified for the first time, and a mathematical analysis of CM noise is presented. The spectral tones at twice the Nyquist frequency are explained by the deterministic nature of the CM signal, which produces strong autocorrelation function periodicity at the symbol rate due to data-independent, non-linear distortion. A novel methodology is proposed to predict the CM noise level from various dependent parameters. As a result, we can present, for the first time, a comprehensive qualitative and quantitative CM noise analysis and prediction of the output driver. We also identify that controlling the source, i.e., the non-linear active circuit, is an effective way of suppressing the CM noise, rather than improving the matching of passive interconnections or using the conventional EMI reduction techniques.

1.3 Thesis Organization

The remainder of this thesis focuses on analysis, prediction and suppression of CM noise of high-speed SERDES I/O drivers. Chapter 2 and Chapter 3 present the background of SERDES I/O drivers and their associated EMI-related CM noise issue, respectively. Chapter 4 focuses on identification of CM noise sources and their determining factors. Chapter 5 covers the analysis of CM noise for high-speed output drivers, while Chapter 6 presents the prediction of the CM noise level for high-speed output drivers. Chapter 7 presents the CM noise level prediction for high-speed parallel I/Os, and Chapter 8 focuses on circuit design guidelines and

a slew-rate controller circuit to suppress the CM noise. Finally, Chapter 9 presents future work and conclusion of the thesis. The organization of the thesis is depicted in Fig. 4.

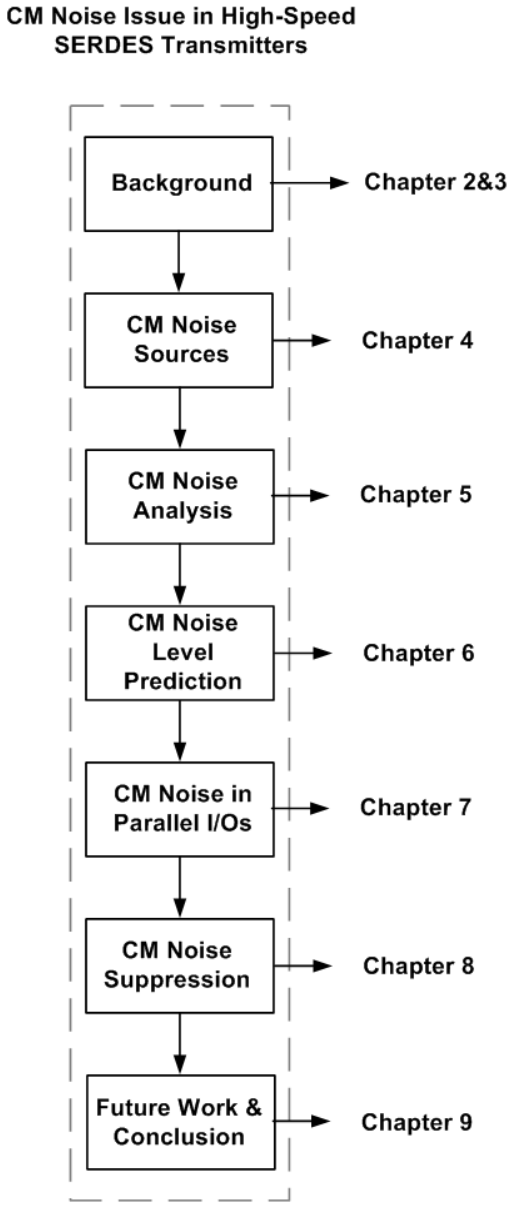

Figure 4. Thesis organization.

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Chapter 2 SERDES TRANSCEIVERS FOR SERIAL COMMUNICATION

Data are constantly exchanged between systems, and also between functional blocks inside a system, in order to process and redistribute information. Parallel and serial communications coexist in modern telecommunication and computer systems to serve various requirements of intra- and inter-system data exchange. In parallel communications several symbols are sent at one time over a communications link, while in serial communications only one symbol is sent at one time. The choice of one method over another is usually a tradeoff of factors such as speed, cost of materials, power consumption, and difficulty of physical realization [1].

2.1 Background of SERDES Transceivers

A simplified SERDES transceiver block diagram is shown in Figure 5. A SERDES Tx serves to transmit parallel data links to the receiver through a high-speed serial data link, and is widely deployed in backplane links such as peripheral component interconnects (PCI) express, Ethernet, computer to peripheral devices, such as universal serial bus (USB), multimedia interfaces such as high-definition multimedia interface (HDMI) and high-speed memories. A SERDES receiver (Rx) receives data from the serial data link and delivers parallel data to the next-stage electronic circuits for further signal processing. Internal buses of integrated circuits and short distance chip-to-chip data links use parallel communications to increase the data transfer rate and signal processing speed. In addition, massive data are usually stored in slow devices such as RAM, and they have to be accessed in parallel to achieve high-speed.

In high-speed data links, serial communication is replacing parallel communication due to its low cost. The parallel data links in chip-to-chip communications require more pins, which increases the cost of packaging, and packaging already represents more than 25% of the total system cost of most electronic products [2]. The other challenges in parallel communication are clock skew, data skew and crosstalk.

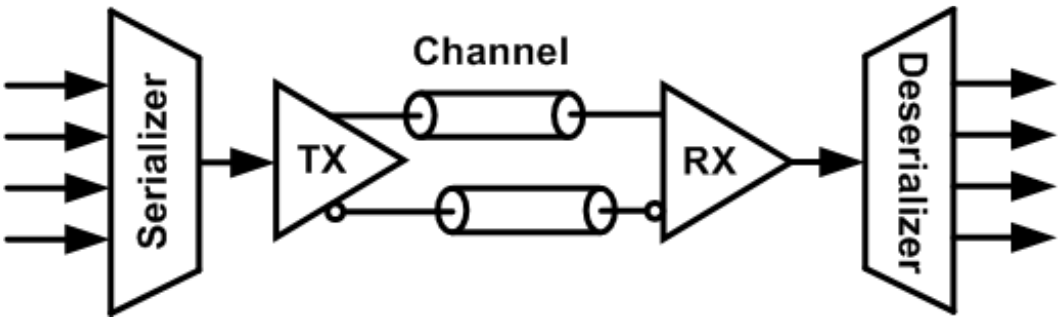

Figure 5. SERDES transceiver block diagram.

2.2 Design Challenges in SERDES Transceivers

With the ever-increasing demand for high data rates, power consumption is becoming a major concern in SERDES systems. In a high-speed serial transceiver, one of the most power-hungry blocks is the output driver in the Tx chain [4]. Therefore, it is desirable to implement SERDES transceivers in mainstream CMOS technologies because of their low power consumption and low cost. The speed of CMOS circuit is getting faster with as we move towards more advanced technology nodes and the power consumption is decreasing with scaling. Therefore, new architectures and circuit styles enabling low power and high speed are critical for high-speed serial data links. SERDES transceivers are predominantly mixed signal circuits, and proceeding towards advanced technology nodes, the supply voltage and threshold voltage are dropping, leaving less headroom for signal processing and creating vulnerability to process, voltage and temperature (PVT) variations. Recent attempts have been made to replace analog blocks with digital ones to increase the transceiver's robustness against PVT variations and noise.

High-speed SERDES transmitters must drive a high-speed channel that is usually much longer than the representative wavelength of the signal. The driver is unable to provide maximum power to the channel because of reflection at the transmitter side if the impedance of the driver does not match the characteristic impedance of the channel. Some energy will be reflected from the terminal and cause another reflection at the transmitter side because of mismatch on both sides. ΔT time is required for this energy to complete this round-trip and suffer loss, and when it comes back, it is added to the signal that is sent at ΔT later. Therefore, impedance matching is important to high-speed SERDES transceivers.

2.3 Circuit Styles

A high-speed SERDES transceiver is a mixed-signal system, and it must be able to drive the physical channel. The physical channel distorts and adds noise to the digital signals that travel through it, and the received signals become analog. A high-speed SERDES transceiver is usually a sub-system of a large system, but it can also be used for portable devices. Thus low power consumption is critical, and the circuit style must be tailored to meet these requirements. The main transmitter interface styles prevalent in today's communication systems are current-mode logic (CML); voltage-mode logic (VML), including source-series terminated logic (SSTL); CMOS drivers (inverter based); and low-voltage differential signaling (LVDS). The output driver stage in different IC chips varies, and several typical IC output buffer structures will be introduced in this section.

2.3.1 Current Mode Logic (CML) Driver

CMOS CML logic, which is shown in Figure 6, is based on differential pairs. There are no pMOS transistors, and it is potentially faster than static CMOS logic. This structure has excellent immunity to common-mode noise because it is a fully differential circuit. When the input voltage V_{in} is sufficiently large, one of the two branches can be switched off, while the other takes all the tail current I_B. The minimum input voltage can be derived using the following equations:

$$I_{1,2} = \mu C_{ox}/2\ (W/L)(V_{gs1,2} - V_{th})^2 \quad (1)$$

$$I_1 + I_2 = I_0 \quad (2)$$

$$V_{in} = V_{gs1} = V_{gs2}\ . \quad (3)$$

For the CML driver, the transistors are biased in the saturation region and during the operation period, M1 and M2 are alternately switching on or off and steering the tail current I_B through R1 or R2, and the current through R1/R2 further results in output voltage swing. Because the whole structure only contains N type devices, the output swing is not able to reach rail-to-rail and headroom is necessary for the tail current device to work properly. The voltage swing is the product of the load resistance and the tail current. Therefore, it is possible to reduce the voltage swing to improve the speed of the circuit. However, excessive reduction of voltage swing reduces the noise margin. In addition, it may not be able to fully switch the next-stage differential pairs.

$$\Delta V = V(i=0) - V(i=I_B) = RI_0 \quad (4)$$

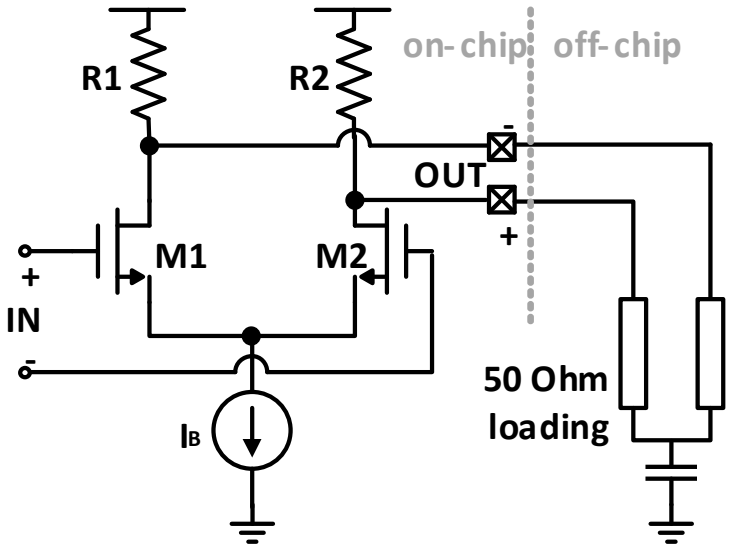

Figure 6. CML output buffer structure.

2.3.2 Push-Pull Driver

The push-pull driver used for the LVDS interface standard is shown in Figure 7. It consists of a current source which drives the differential lines terminated with a 100 Ω load. The LVDS receivers have high input impedance and the drive current mainly flows through the terminating resistor, generating a differential voltage across the receiver inputs. When the driver switches, it changes the direction of the current flow through the resistor, thereby creating a differential signal.

Differential signaling increases the interface's tolerance to ground mismatch between the transmitter and receiver and improves signal EMI immunity and compliance. SERDES transmitters often utilize an LVDS interface, leading to lower power, better noise immunity and reliable clock recovery. They also exhibit large bandwidth for high-speed data transmission. The main advantages offered by LVDS are its low voltage swing, high-speed interface operation at lower power consumption, and compatibility with the IEEE 1596.3-1996 [5] standard. In high-speed SERDES transceivers, the signals traveling through the channels are broadband signals, and it is difficult to achieve impedance matching in the presence of parasitic capacitance [6].

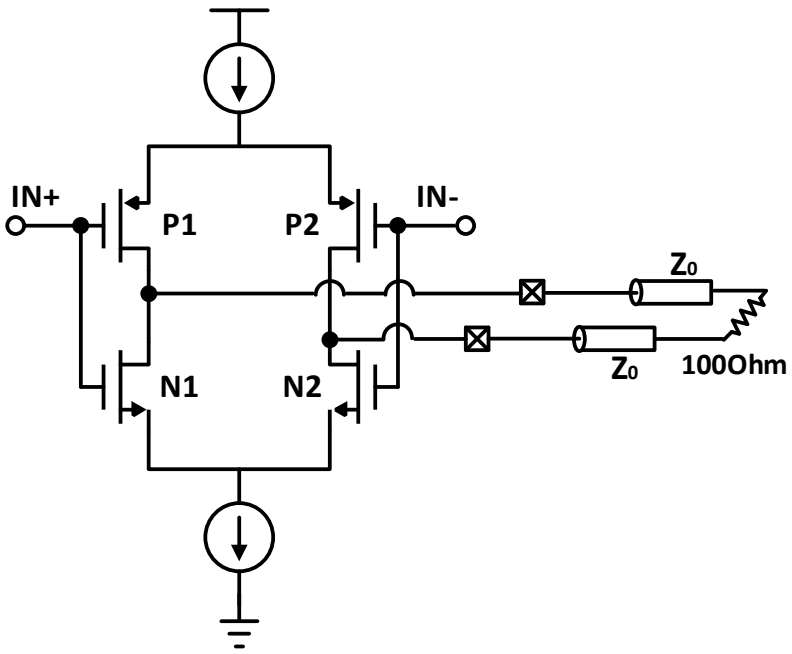

Figure 7. Push-pull driver structure.

2.3.3 Source-Series Terminated (SST) Driver

The source-series terminated (SST) driver shown in Figure 8 contains a pull-up and a pull-down branch implemented with a PMOS or NMOS transistor in series with a poly resistor (R_{SERIES}). The resistance of the transistor is nonlinear and susceptible to PVT variations, so the series resistor is used to dominate the total impedance. The modified SST driver is implemented with a single series resistor in the signal path, which will reduce the parasitic capacitance associated with the resistor by half.

The CML driver maintains good signal integrity because the current source has high output impedance and the internal resistor provides good impedance matching at the expense of more power consumption [7]. The SST transmitter, on the other hand, can provide a high-speed, lower power solution for SERDES signal transmission. It can be subdivided into two branches, namely, a pull-up and pull-down branch, implemented as a PMOS and NMOS switch transistor followed by a termination resistor. For the same differential output swing, the SST driver consumes one-quarter of the output stage power of the CML driver and allows different termination options [4], [8]. Due to these advantages, the SST driver is compatible with multiple termination standards [8], [9]. However, the SST driver suffers from poor signal integrity and its impedance matching is achieved using various techniques.

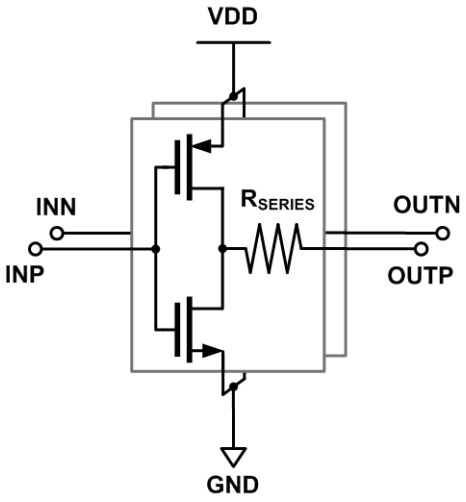

Figure 8. SST driver structure.

2.3.4 CMOS Driver

As shown in Figure 9, the inverter based CMOS driver is actually a pseudo-differential structure [10] and the output swing is rail-to-rail, but obviously, due to the pseudo-differential feature, the noise rejection performance of this type of output driver is much worse than that of the other types.

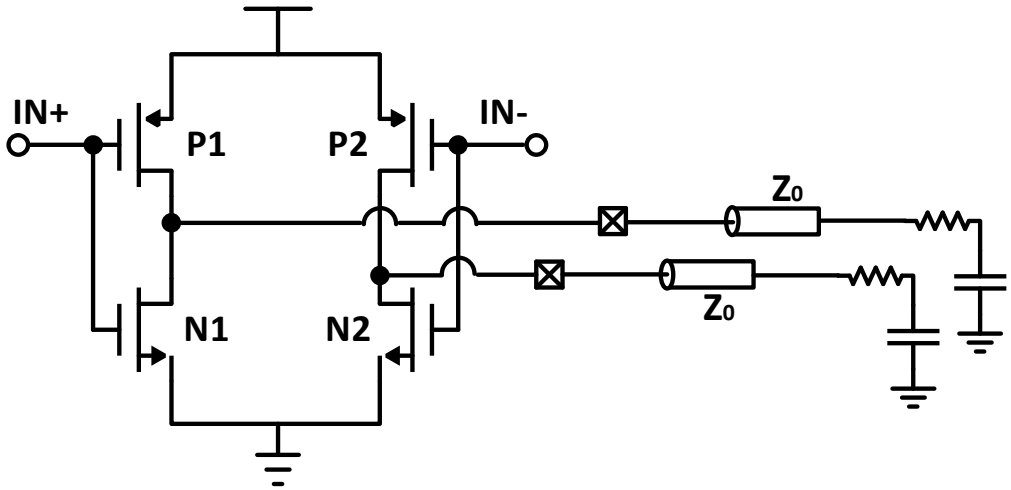

Figure 9. Inverter based CMOS driver.

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Chapter 3 COMMOM-MODE (CM) NOISE ISSUE IN HIGH-SPEED SERDES TRANSMITTERS

There are two types of noise that exist in a communication link, namely common-mode (CM) noise and differential-mode (DM) noise. An in-depth understanding of both types of noise is critical for predicting electromagnetic radiation, and it is of paramount importance to identify the predominant source of electromagnetic radiation. Furthermore, the prediction model should be based on the dominant source of electromagnetic radiation.

3.1 CM Noise Vs DM Noise

Consider a pair of wires carrying currents I_1 and I_2, as shown in Figure 10 [1]. The currents can be decomposed into two auxiliary sets of currents. I_D is the DM currents, and these currents in the two wires at the same cross-sectional position are equal in magnitude and phase but travel in opposite directions. Equivalently, they are 180^0 out of phase. The DM currents are the functional signal carried by the PCB traces as they are the desired signal and carry information. The other set of currents are CM currents that at the same cross-sectional positon travel to the right and are equal in magnitude and phase.

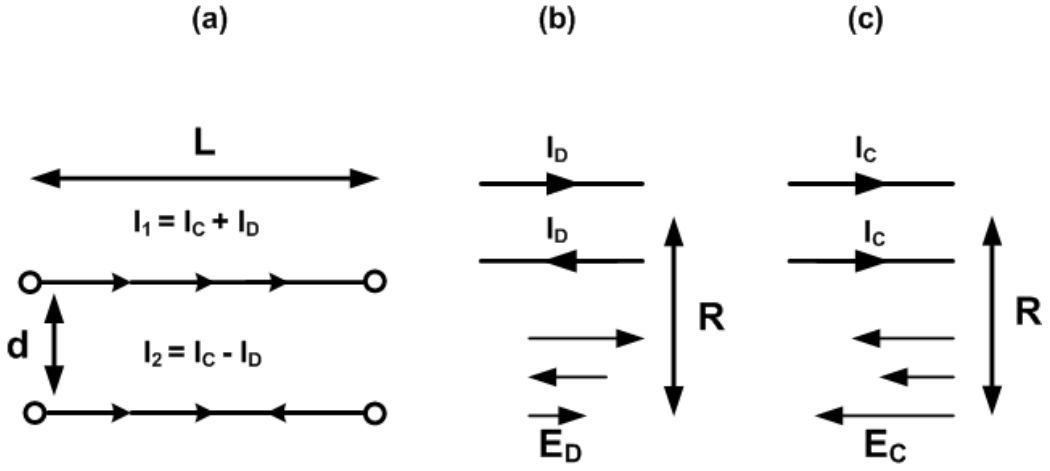


Figure 10. CM versus DM currents: (a) total current decomposed into CM and DM currents, (b) radiation emissions from DM currents and (c) radiation emissions from CM currents.

The DM currents, being the functional signal, are easy to predict and are high in magnitude. Kirchhoff's current law (KCL) can be applied to predict their levels. However, CM currents are difficult to predict, and one has to take displacement current into account to calculate them.

The currents depicted in Figure 3 can be decomposed into CM and DM currents, and they can be written as

$$I_1 = I_C + I_D \quad (1)$$

$$I_2 = I_C - I_D. \quad (2)$$

Subtracting and adding the above equations give

$$I_C = (I_1 + I_2) / 2 \quad (3)$$

$$I_D = (I_1 - I_2) / 2. \quad (4)$$

The DM and CM waveforms are shown in Figure 11.

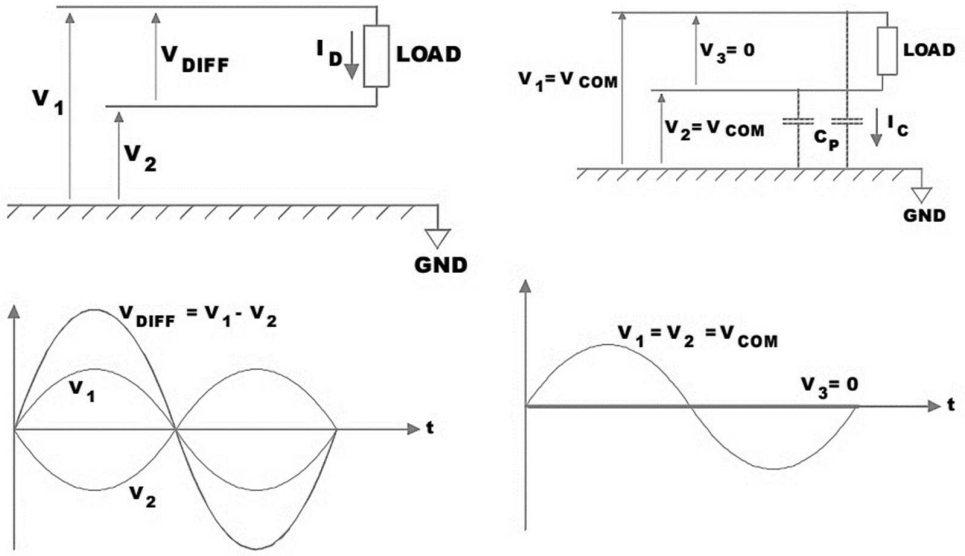


Figure 11. DM waveform (left) and CM waveform (right) [2].

The phase difference between I_1 and I_2 should be considered. The CM currents are usually of several orders less in magnitude than DM currents, but can usually produce considerably larger levels of radiated electric fields, as shown in Figure 10. The radiated fields of DM currents subtract from each other but do not exactly cancel each other out as the two wires are not collocated. In contrast, the emissions of the CM currents can be superimposed on

each other. CM currents on the passive interconnections are the dominant factor responsible for radiated emissions.

The simulated total radiated energy, which is the ratio of radiated energy to input energy is shown in Figure 12. The total radiated energy from the CM currents is -12 dB, and from the DM currents is -20 dB, equivalently 8 dB higher at 10 GHz [3].

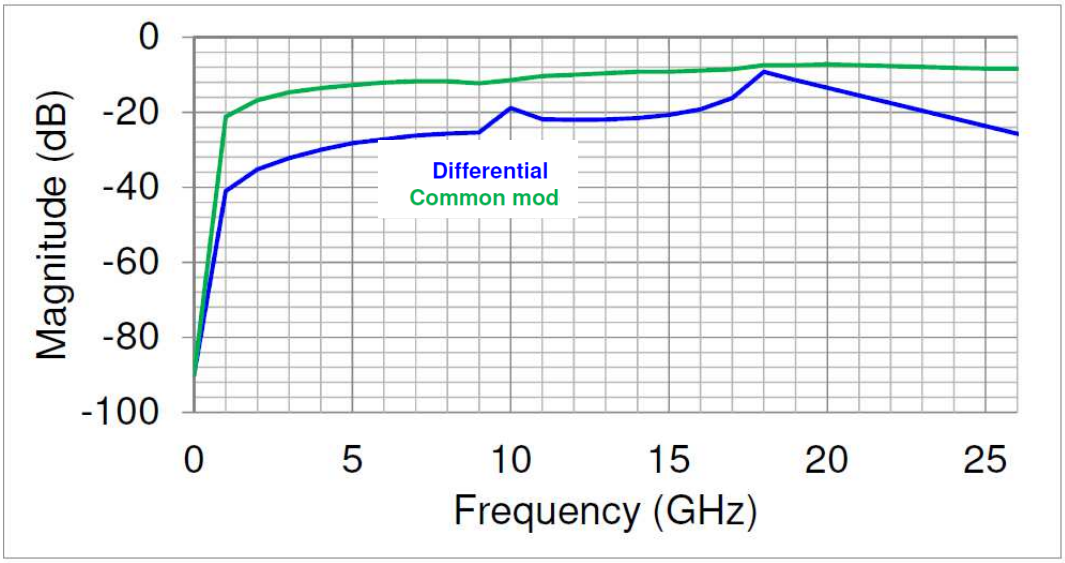


Figure 12. Total radiated energy ratio, radiated energy/ input energy.

The following comparison can be drawn for the DM and CM noise. The DM noise involves normal operation of current, whereas the CM noise does not relate to the normal operation of the circuit. The DM current flows around the loop, whereas the CM current flows around the loop involving parasitic capacitance, as shown in Figure 11. The DM noise is documented in the schematic and PCB layout, whereas the CM noise is not documented and is difficult to understand. Finally, the DM noise can be predicted with reasonable accuracy, whereas for the CM noise source, the current path must first be visualized and understood before a solution can be determined [4].

3.2 Prediction of DM and CM Noise

A frequently used model for predicting DM and CM emissions is based on the fields of the simple Hertzian dipole, as shown in Figure 13 [5]. The Hertzian dipole is an extreme simplification, and following are its assumptions: The length of dipole L is infinitesimally small and phasor current I is assumed to be of the same magnitude and phase at all points along the dipole.

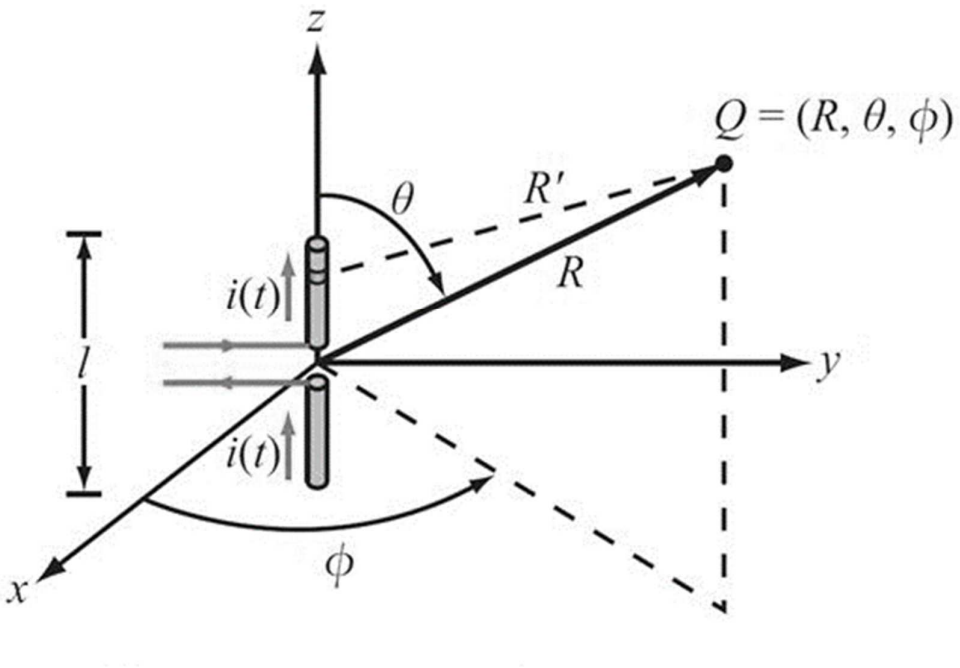


Figure 13. Short dipole placed at the origin of a spherical coordinate system.

From Figure 10, if we approximate each structure as two Hertzian dipoles and by combining the fields given for DM currents, we can obtain [6]

$$E_{Dmax} = 1.316 \times 10^{-14} I_D f^2 L d / R. \quad (5)$$

Similarly, for CM currents after approximation, we can obtain

$$E_{Cmax} = 1.257 \times 10^{-6} I_C L f / R. \quad (6)$$

The CM currents are several orders of magnitude lower than the DM currents, but can produce the same levels of radiated electric fields, as shown in Figure 10. For a 1m length of cable and wires separated by 50 mils, a DM current of 20 mA at 30 MHz will produce a radiated electric field of 100μV/m at a distance of 3 m, whereas 8 μA of CM current is required to produce the same level of radiated emissions [1].

3.3 CM Noise Measurement

CM noise at F_{dr} is evaluated and reported in this thesis. The dominant spectral tone appears at F_{dr} and higher-order harmonics will be attenuated by the limited channel bandwidth.

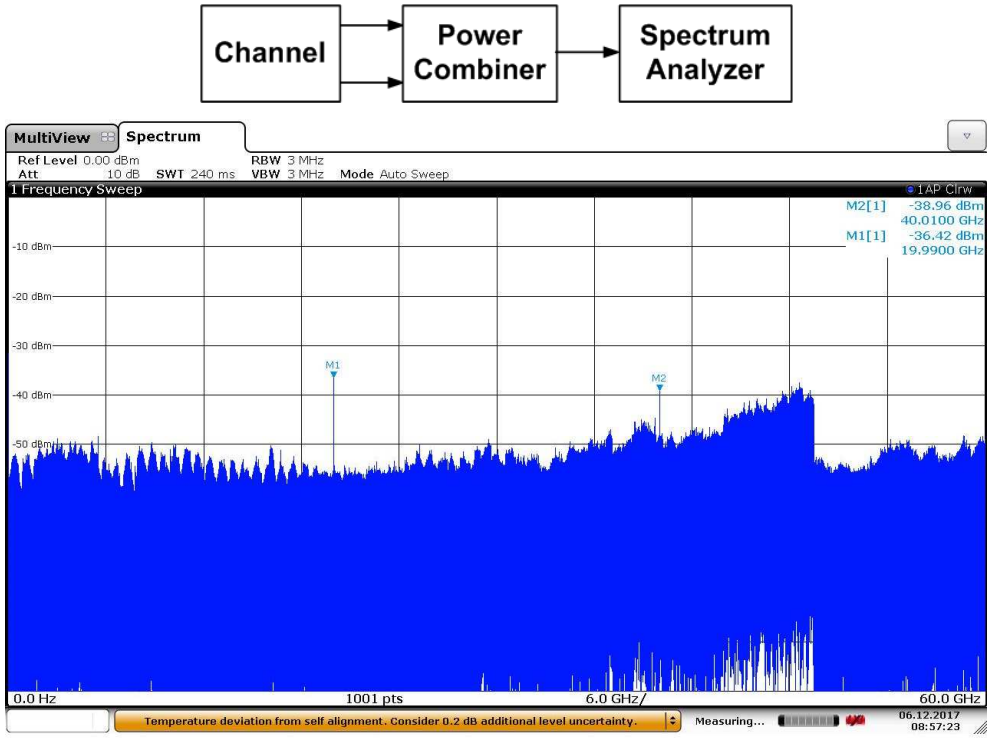
3.3.1 Simulation

The discrete Fourier transform is performed on the CM noise voltage waveform and converted to the dB scale, i.e., 20 $\log_{10}$ (V_{CM}/V_0), where V_0 is 1V, and is then evaluated at $2f_{Nyquist}$. The magnitude obtained has the unit of dBV. The dBμV unit is commonly used in industry, and regulatory requirements are often expressed in dBμV. A value of 120 is added to dBV to get the CM noise value in dBμV.

3.3.2 Measurement

The measurement setup for CM noise tone measurement at 2fNyquist is shown in Figure 14. The output of P and N channel are combined using passive combiner to extract the output CM component, which is analyzed by a 40 GHz bandwidth spectrum analyzer. The spectrum of DM and CM both is plotted by taking the output of one channel and fed to a spectrum analyzer.

(a)



(b)

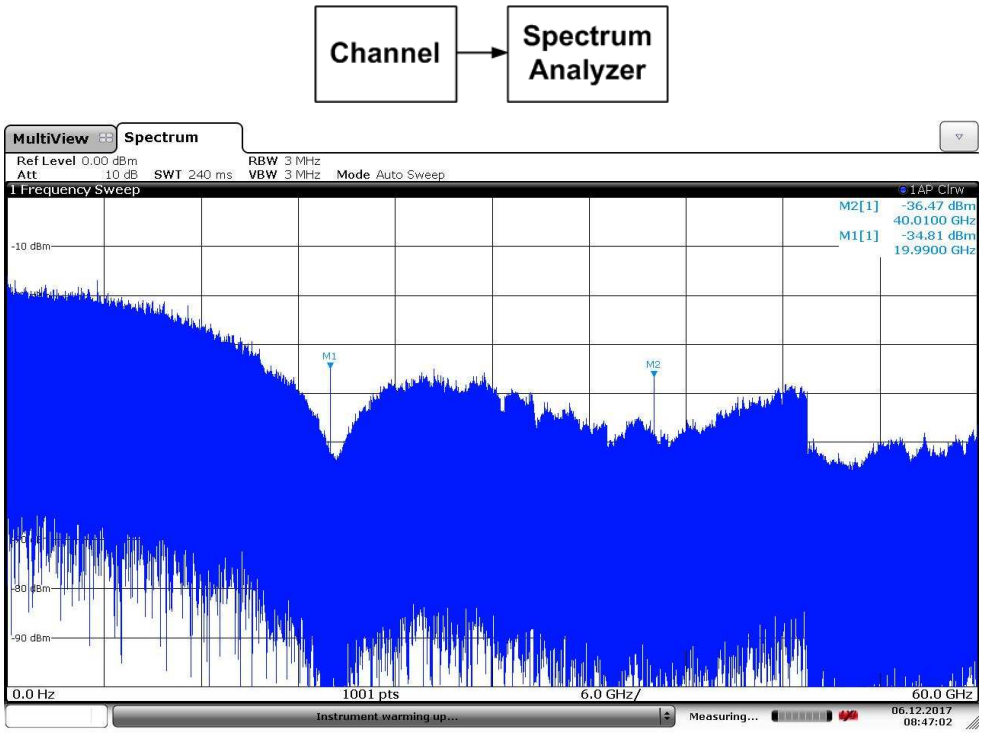


Figure 14. (a) CM noise tone measurement at twice the Nyquist Frequency and (b) CM and DM noise tone measurement.

3.4 Chapter Conclusion

CM current radiation is higher than DM radiation; therefore, CM currents are the primary contributor to radiated emissions. Furthermore, predictions of radiated emissions based solely on DM currents bear little resemblance to actual measured emissions. It is important to identify the source of CM noise, identify all dependent parameters that affect it, and predict the parameters' contribution to the overall output CM noise.

3.5 References

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Chapter 4 CM NOISE SOURCES AND THEIR DETERMINING FACTORS

CM noise is the predominant source of electromagnetic radiation [1]; therefore, it is of critical importance to identify the main source(s) of CM noise. In this chapter, we identify the source of CM noise for the first time. The analysis is performed by considering only the non-idealities of the signal source and passive link. From the output CM spectrum profile, the non-linear distortion responsible for the creation of CM noise is analyzed and the relationship between EMI and signal components is presented. A mathematical analysis of CM noise is presented for the first time. Furthermore, the auto-correlation function of non-linearly distorted CM signals, which explains the spectral tones occurring at twice the Nyquist frequency and its multiples, is presented.

4.1 Signal Source and Passive Link

For simplicity of analysis, a communication data link is divided into active and passive parts. The active part is the signal source, which is the IC chip used for high-speed communication, while the passive part contains all the passive components in the data link, as shown in Figure 15.

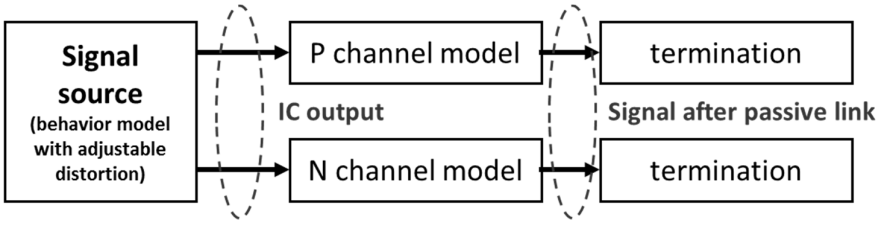


Figure 15. Simplified behavior-level system diagram.

4.1.1 Ideal Signal Source and Non-Ideal Passive Link

First, we consider the ideal signal source (ISS) and non-ideal passive link (NIPL). The output of the signal source is the ideal differential PRBS signal, as shown in Figure 16, while the unbalanced P/N channel is considered based on S-parameters measured from different PCB traces. The waveform after the P/N channel is both amplitude and phase distorted as shown in Figure 17; however, its CM spectrum contains no significant tone at F_{dr}. The output DM and CM signals have the same spectrum profile as that of the ideal PRBS data stream, as shown in Figure 18 and Figure 19.

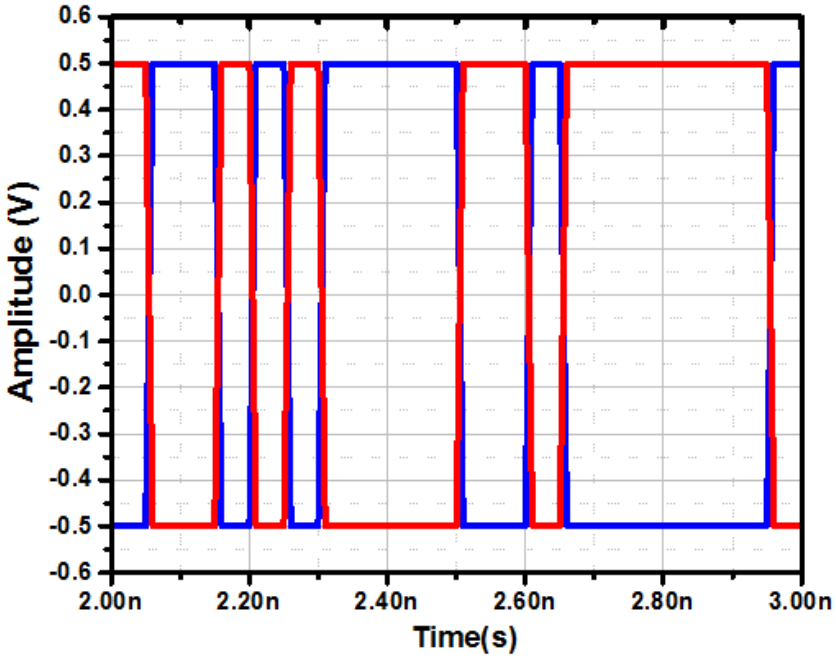


Figure 16. Ideal signal source.

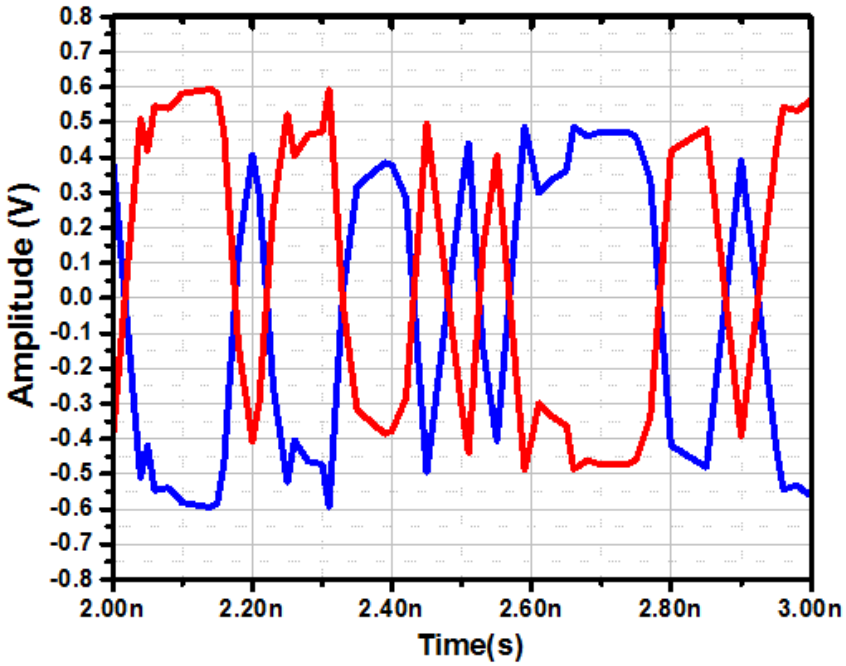


Figure 17. Distorted output signal of ISS and NIPL.

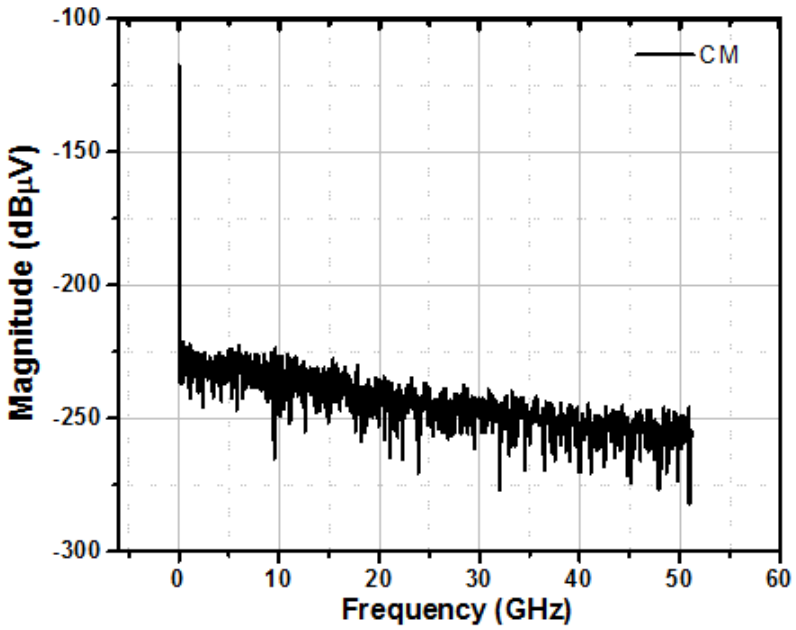


Figure 18. CM signal of ISS and NIPL.

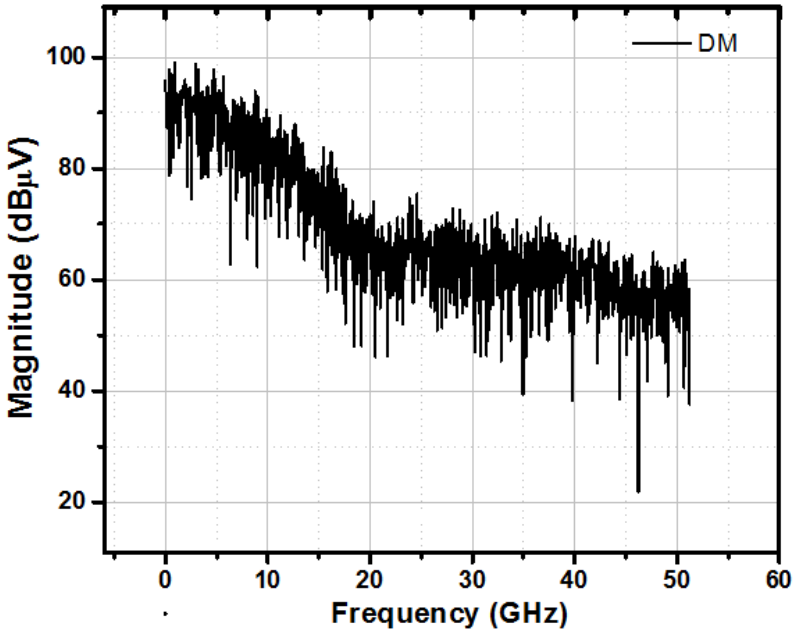


Figure 19. DM signal of ISS and NIPL.

4.1.2 Non-Ideal Signal Source and Ideal Passive Link

Next, we consider the non-ideal signal source (NISS) and ideal passive link (IPL). The signal source generates the distorted PRBS differential signal with rising/falling edge mismatch, as shown in Figure 20, that goes through the well-matched passive link. The output CM

spectrum has a significant tone at F_{dr}, as shown in Figure 22, whereas the output DM spectrum is roughly the same as that of the ideal PRBS data stream, as shown in Figure 23.

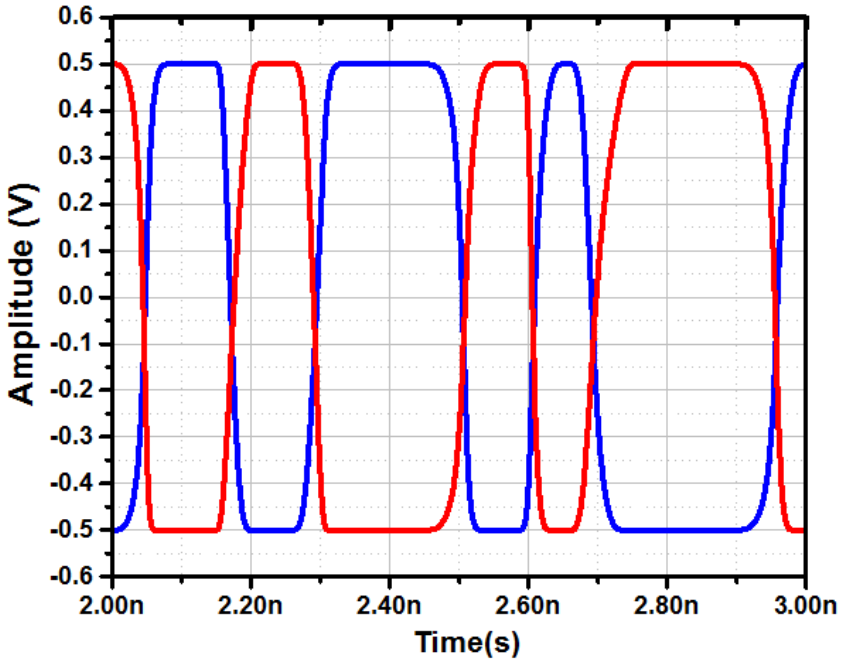


Figure 20. Non-ideal signal source.

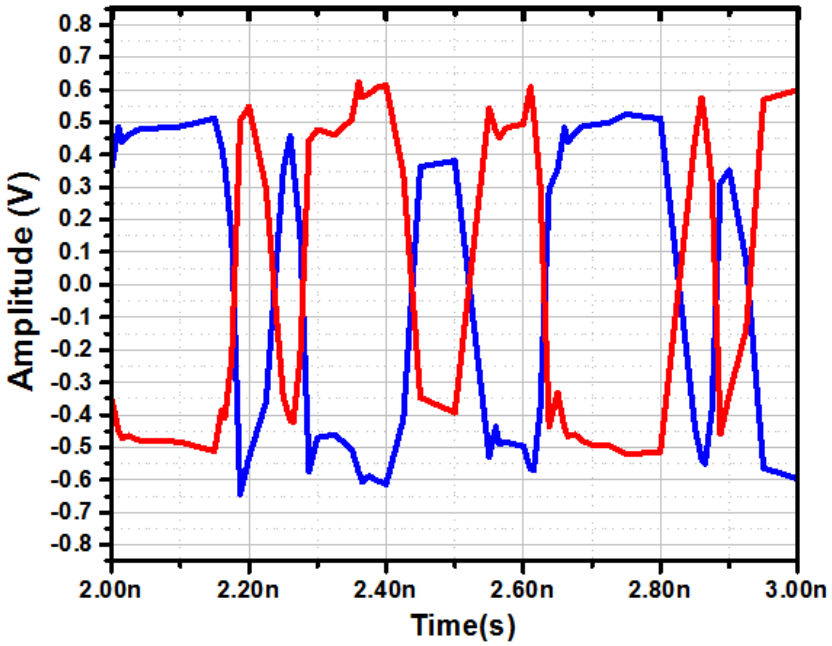


Figure 21. Distorted output signal of NISS and IPL.

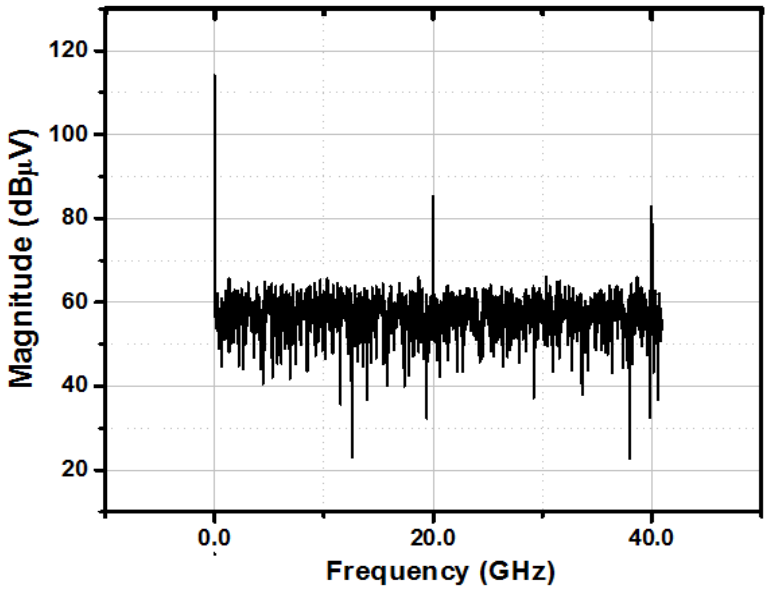


Figure 22. CM signal of NISS and IPL.

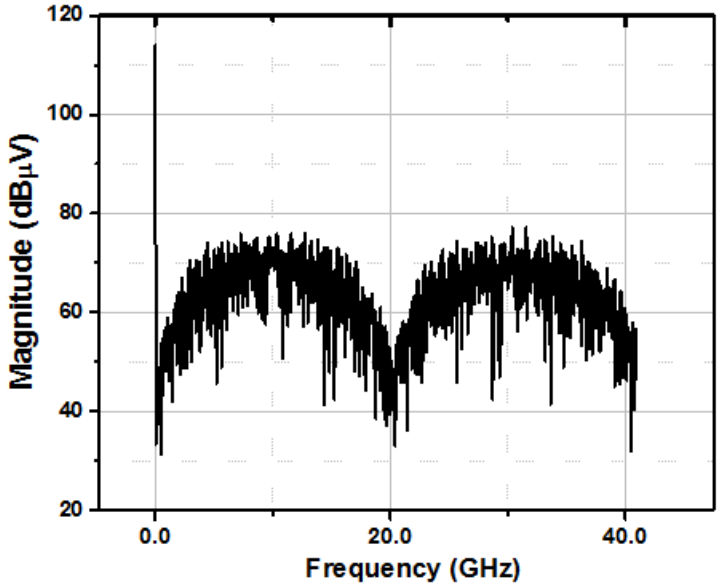


Figure 23. DM signal of NISS and IPL.

4.1.3 Non-Ideal Signal Source and Non-Ideal Passive Link

Finally, we consider the NISS and NIPL. The signal source generates a distorted differential PRBS signal, as shown in Figure 24, that goes through the passive link with P/N channel mismatch. The distorted signal source and unbalanced passive link together produce the distorted output signal, including amplitude, skew and rising/falling edge mismatch, as

shown in Figure 25. The final output CM spectrum has a significant tone at F_{dr}, and the output DM spectrum is no longer ideal, as shown in Figure 26 and Figure 27, respectively. Comparing the results of NISS + IPL and NISS + NIPL, the CM noise tone at F_{dr} changes by only a few dB; however, the NIPL also generates the DM tone at F_{dr}. With the NIPL, the asymmetry also results in mode conversion between the DM and CM, besides producing a significant spectral tone at $F_{dr.}$

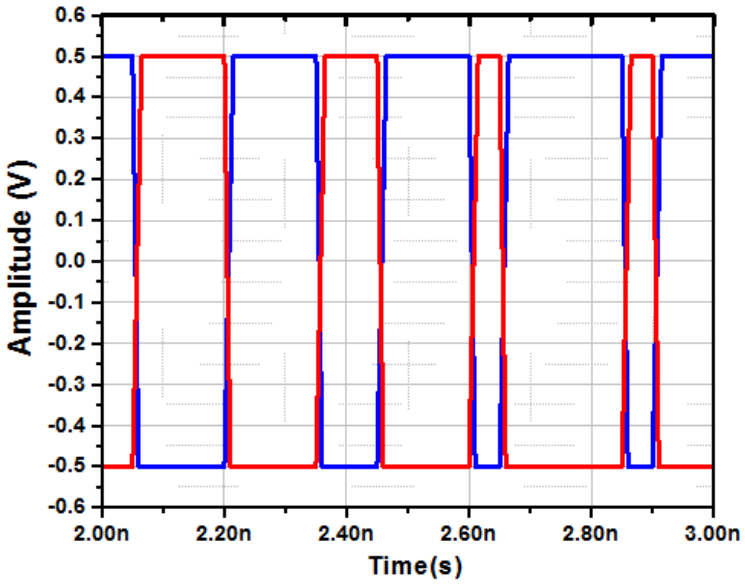


Figure 24. Non-ideal signal source.

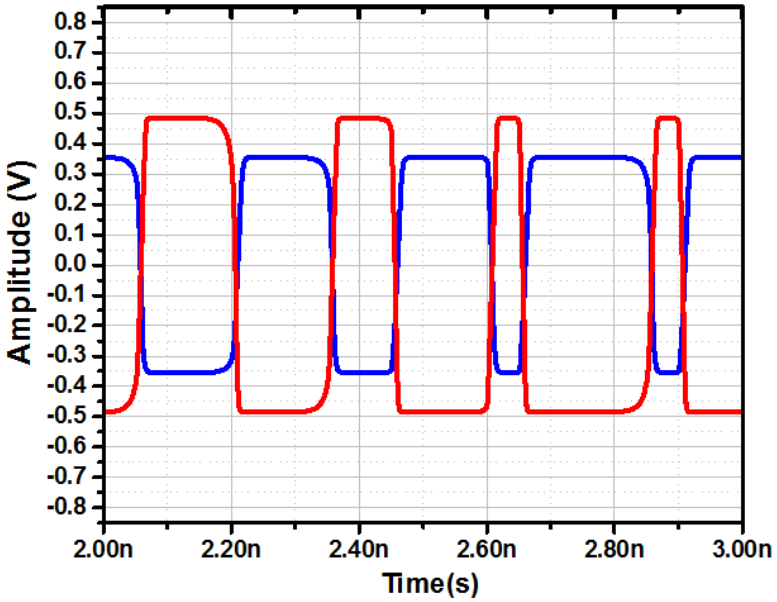


Figure 25. Distorted output signal of NISS and NIPL.

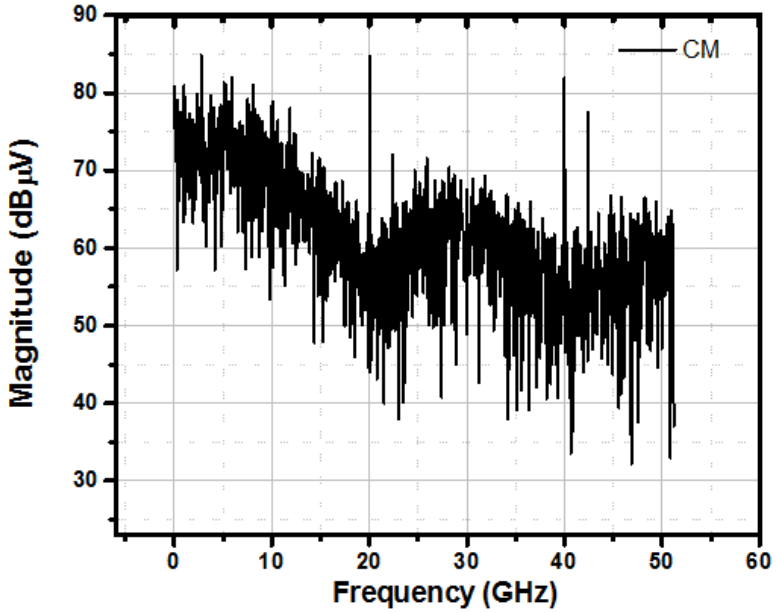


Figure 26. CM signal of NISS and NIPL.

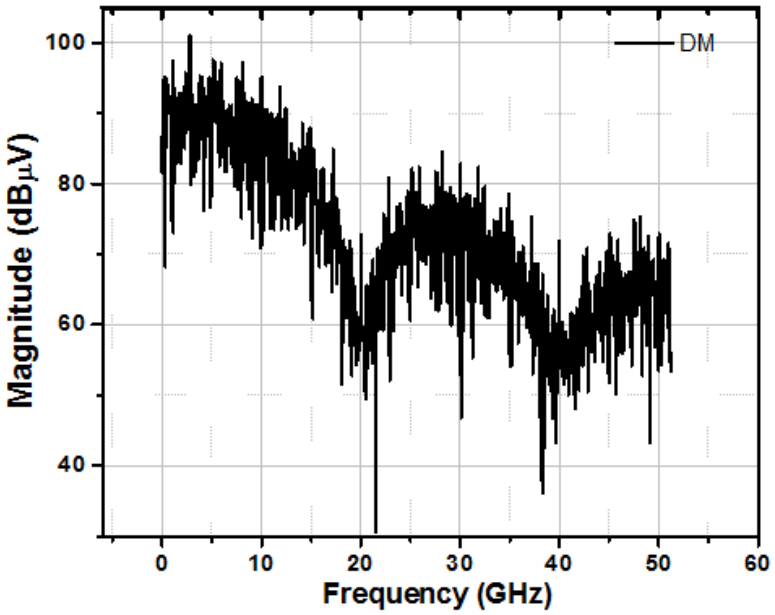


Figure 27. DM signal of NISS and NIPL.

The results of the above analysis are summarized in Table 1.

Table 1. CM noise identification results.

Signal source	Passive link	CM and DM noise
Ideal non-distorted differential PRBS signal	Non-ideal mismatched P/N channel	No CM and DM noise tone
Non-ideal rise/fall time mismatched signal	Ideal matched P/N channel	CM noise tone at F_{dr} no DM noise tone
Non-ideal rise/fall time mismatched signal	Non-ideal mismatched P/N channel	Mode conversion both CM and DM noise tone at F_{dr}

4.2 Linear and Non-Linear Distortion

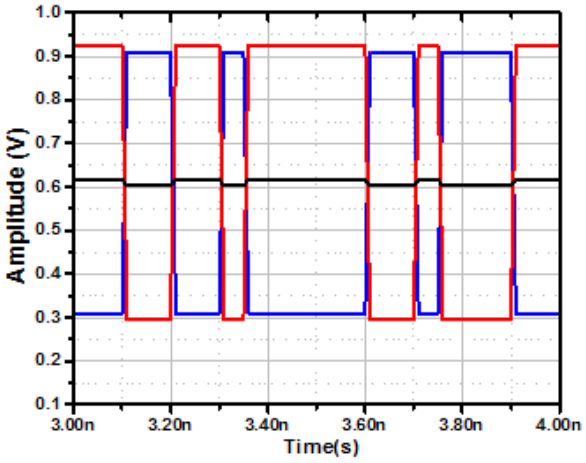
From the above analysis, the CM voltage spectrum profile can be categorized into two types of distortion, namely, linear distortion and non-linear distortion.

Linear distortion is produced by several factors, including skew, loading (bandwidth) and amplitude mismatch between the P and N channels, as shown in Figure 28(a–c). Skew occurs due to the relative delay between the P and N channels, and the loading of the P and N channels cannot be perfectly matched in practical cases. Heavier capacitive loading with a larger time constant leads to a smaller bandwidth and slower rising/falling edge, and vice versa. Within the same channel, the rising time and falling time are the same because, for both periods, the loading time constants are the same; however, the time constants between the P and N channels are different. In the linear distortion of the differential signal, the CM voltage spectrum follows roughly the same profile as that of the ideal pseudo random bit sequence (PRBS) spectrum, and no significant tone is generated, as shown in Figure 29. Also, the CM voltage output spectrum shows that the linear distortion only causes energy leakage from the DM to CM component in a wide frequency range, but creates no significant spectrum component to be radiated, which can cause EMC failure.

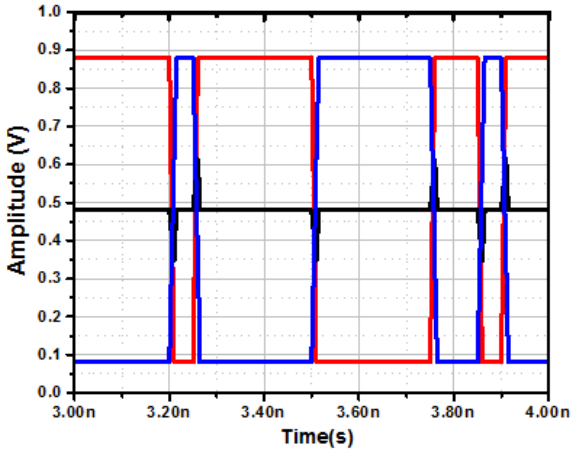
Rising/falling edge mismatch, as shown in Figure 30, is categorized as non-linear distortion since it produces mismatched PRBS waveforms and CM component. Unlike linear distortion, the CM spectrum of rising/falling edge distortion has a large power component at F_{dr} aligned with the notch of the differential PRBS spectrum, as shown in Figure 31. The new

spectrum component that is generated in this type of distortion is later radiated and causes EMC failure. Spurs on the CM voltage in a transient waveform are always monotonic and data-independent, as shown in Figure 30. This feature is also different from the data-dependent linear distortion. The spectral content is proportional to the signal amplitude. Since the amplitude of the CM voltage signal is in the order of $\pm$ 10 mV, the envelope of the CM noise spectrum is less than that of the DM, except at F_{dr}, as shown in Figure 31.

(a)



(b)



(c)

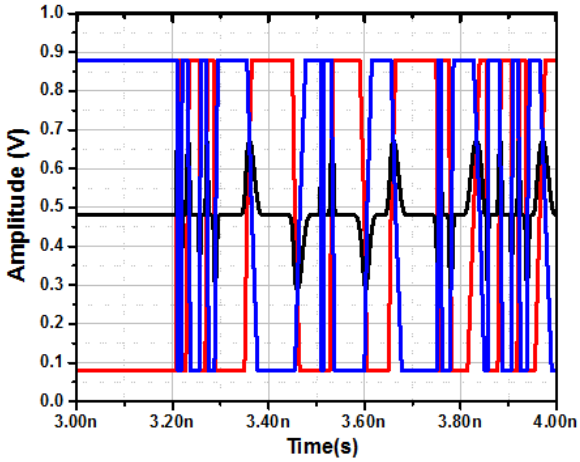


Figure 28. Linear distortion: (a) amplitude mismatched, (b) loading mismatched, (c) skewed mismatched.

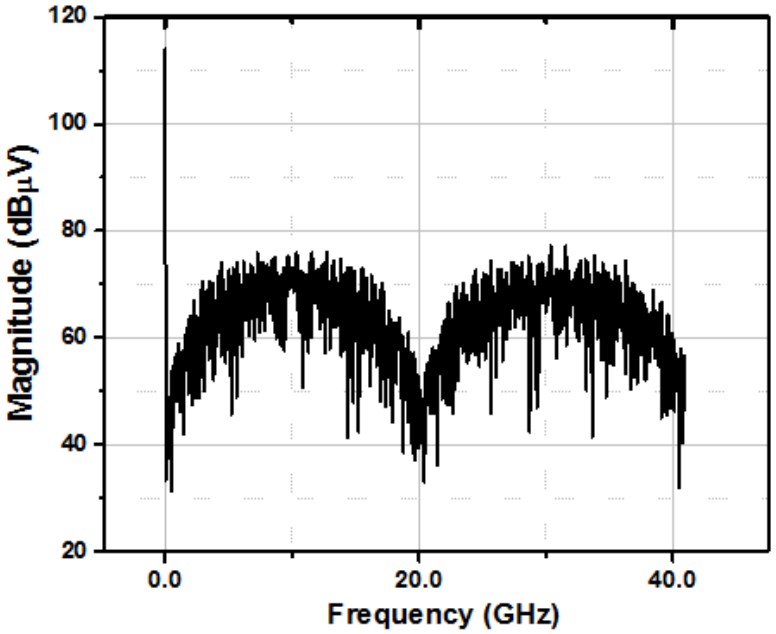


Figure 29. CM spectrum of linearly distorted differential signal.

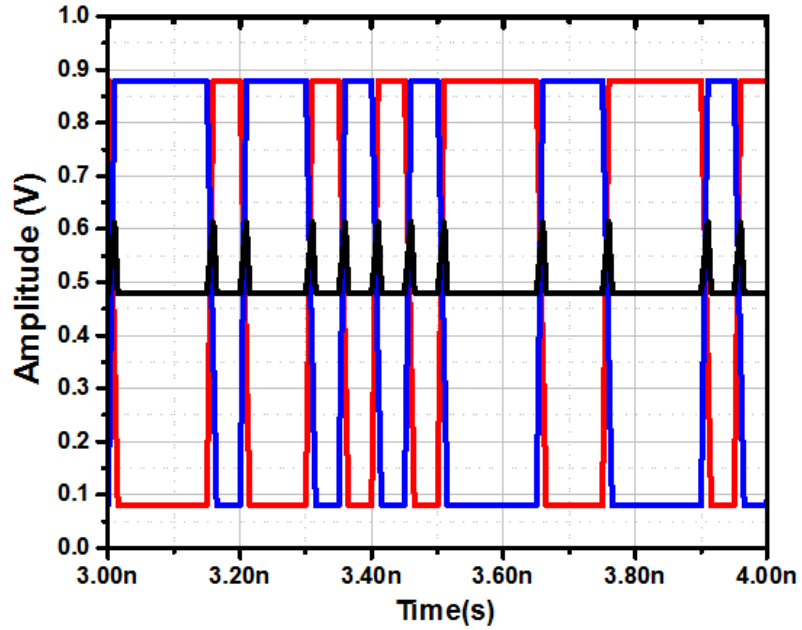


Figure 30. Non-linear distortion rise/fall time mismatched output waveform.

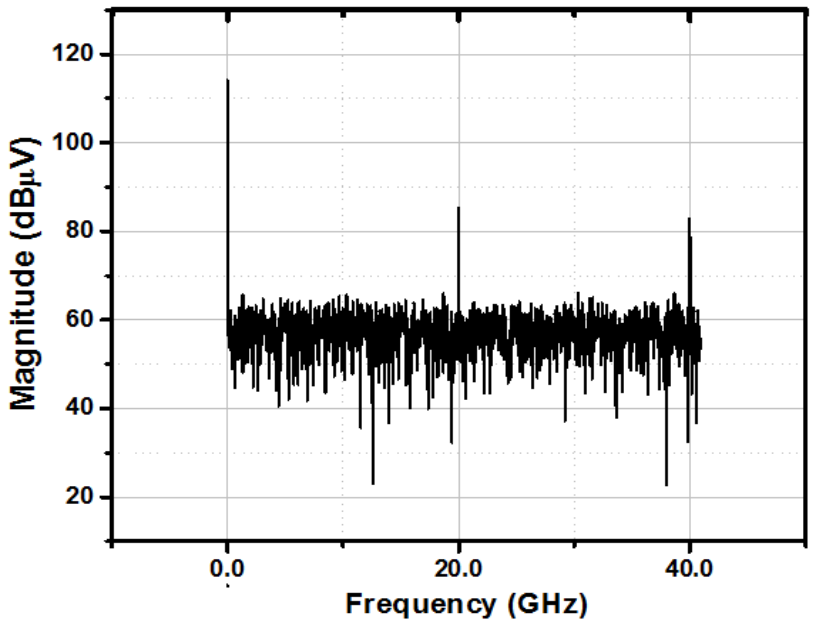


Figure 31. CM spectrum of non-linearly distorted differential signal.

4.3 Mathematical Analysis of CM Noise

The output signal (single-ended) can be represented as periodic trains of trapezoid-shaped pulses described by an amplitude A, a pulse rise time t_r, a pulse fall time t_f and a pulse width T, as shown in Figure 32 [2], [3]. In order to obtain the complex-exponential Fourier coefficient c_n^+ for a one-sided spectrum of this waveform, we will take the first derivative of the waveform shown in Figure 33(a). Differentiating this once again to yield impulses gives the waveform shown in Figure 33(b).

Since the waveform contains impulses, we expand it to give the expansion coefficients, which are expressed as

$$C_n^{(2)} = \frac{1}{\mathrm{T}}\frac{\mathrm{A}}{t_r} - \frac{1}{\mathrm{T}}\frac{\mathrm{A}}{t_r}e^{-jn\omega_0 t_r} - \frac{1}{\mathrm{T}}\frac{\mathrm{A}}{t_f}e^{-jn\omega_0\left[\mathrm{T}+\frac{t_r-t_f}{2}\right]} + \frac{1}{\mathrm{T}}\frac{\mathrm{A}}{t_f}e^{-jn\omega_0[\mathrm{T}+\frac{t_r+t_f}{2}]} \quad (1)$$

$$C_n^{(2)} = \frac{\mathrm{A}}{T}\left[\frac{1}{t_r}e^{-jn\omega_0\frac{t_r}{2}}\left(e^{jn\omega_0\frac{t_r}{2}} - e^{-jn\omega_0\frac{t_r}{2}}\right) - \frac{1}{t_f}e^{-jn\omega_0\frac{t_r}{2}}e^{-jn\omega_0\mathrm{T}}\left(e^{jn\omega_0\frac{t_f}{2}} - e^{-jn\omega_0\frac{t_f}{2}}\right)\right] \quad (2)$$

$$C_n^{(2)} = j\frac{\mathrm{A}}{2\pi n}(n\omega_0)^2 e^{-jn\omega_0\left[\frac{\mathrm{T}+t_r}{2}\right]}\left[\frac{\sin\left(\frac{1}{2}n\omega_0 t_r\right)}{\frac{1}{2}n\omega_0 t_r}e^{jn\omega_0\frac{\mathrm{T}}{2}} - \frac{\sin\left(\frac{1}{2}n\omega_0 t_f\right)}{\frac{1}{2}n\omega_0 t_f}e^{-jn\omega_0\frac{\mathrm{T}}{2}}\right]. \quad (3)$$

The expansion coefficients for the original trapezoidal waveform are

$$c_n = \frac{1}{(jn\omega_0)^2}C_n^{(2)}, n \neq 0 \quad (4)$$

$$c_n = -\frac{c_n^{(2)}}{(n\omega_0)^2} \tag{5}$$

$$c_n = -j\frac{\mathrm{A}}{2\pi n} e^{-jn\omega_0\left[\frac{\mathrm{T}+t_r}{2}\right]} \left(\frac{\sin\left(\frac{1}{2}n\omega_0 t_r\right)}{\frac{1}{2}n\omega_0 t_r} e^{jn\omega_0\frac{\mathrm{T}}{2}} - \frac{\sin\left(\frac{1}{2}n\omega_0 t_f\right)}{\frac{1}{2}n\omega_0 t_f} e^{-jn\omega_0\frac{\mathrm{T}}{2}} \right). \tag{6}$$

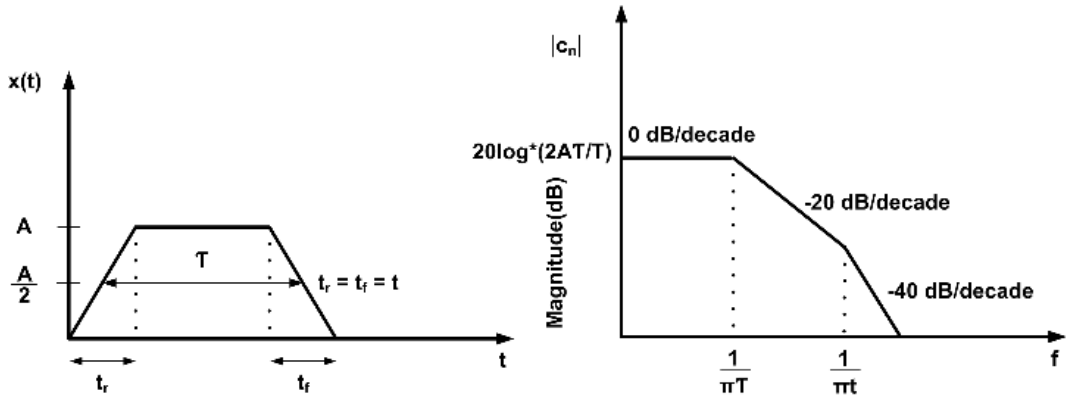


Figure 32. The periodic, trapezoidal pulse train representing clock and data signals of digital systems.

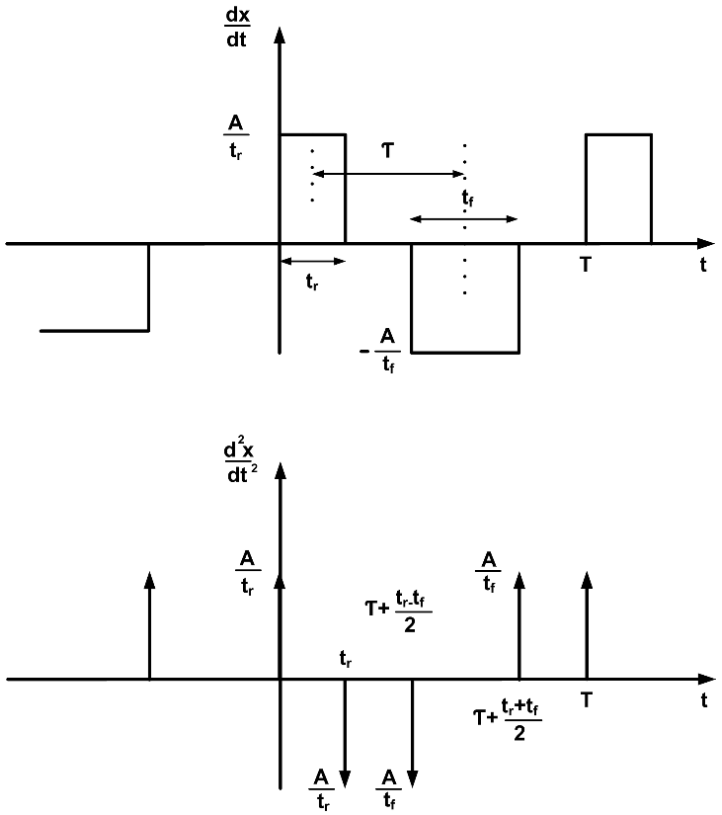


Figure 33. Various derivatives of the trapezoidal pulse train: (a) first derivative, (b) second derivative.

The above result cannot be combined any further to yield useful results. However, if the pulse rise time equals the fall time, $t_r = t_f$, a very useful result can be obtained. Substituting $t_r = t_f$ into above expression gives the expansion coefficients as

$$c_n = A\frac{\mathrm{T}}{T}\frac{\sin\left(\frac{1}{2}jn\omega_0\mathrm{T}\right)}{\frac{1}{2}jn\omega_0\mathrm{T}}\frac{\sin\left(\frac{1}{2}jn\omega_0 t_r\right)}{\frac{1}{2}jn\omega_0 t_r}e^{-jn\omega_0\left[\frac{\mathrm{T}+t_r}{2}\right]}\ t_r = t_f. \tag{7}$$

The above expression is valid only for the special case where the rise and fall time of the signal are equal.

We can also obtain the expansion coefficients for the one-sided spectrum (positive frequencies) c_n^+, where

$$x(t) = c_0 + \sum_{n=1}^{\infty}|c_n^+|\cos(n\omega_0 t + < c_n) \tag{8}$$

$$|c_n^+| = 2\,\mathrm{A}\frac{\mathrm{T}}{\mathrm{T}}\left|\mathrm{sinc}(n\pi\frac{\mathrm{T}}{T})\right|\left|\mathrm{sinc}(n\pi\frac{\mathrm{t}}{T})\right| \text{ for } n \neq 0\ \&\ t_r = t_f = \mathrm{t} \tag{9}$$

$$c_0 = \mathrm{A}\frac{\mathrm{T}}{\mathrm{T}}\ \ (t_r = t_f) \tag{10}$$

$$\omega_0 = \frac{2\pi}{\mathrm{T}} \tag{11}$$

$$< c_n = \pm n\pi\frac{\mathrm{T}+t_r}{T}\ (t_r = t_f) \tag{12}$$

For a 50% duty cycle, $\left|\sin(n\pi\frac{\mathrm{T}}{T})\right| / \left|(n\pi\frac{\mathrm{T}}{T})\right| = \left|\sin(\frac{1}{2}n\pi)\right| / \left|\frac{1}{2}n\pi\right|$, there are theoretically no even harmonics.

The bounds on the spectral content is shown in Fig.3 and can be obtained as:

$$Envelope = 2\,\mathrm{A}\frac{\mathrm{T}}{\mathrm{T}}\left|\mathrm{sinc}(n\pi\frac{\mathrm{T}}{T})\right|\left|\mathrm{sinc}(n\pi\frac{\mathrm{t}}{T})\right| \tag{13}$$

$$Envelope(dB) = 20\log_{10}(2\mathrm{A}\frac{t}{\mathrm{T}}) + 20\log_{10}|\mathrm{sinc}(\pi\mathrm{T}f)| + 20\log_{10}|\mathrm{sinc}(\pi tf)|\ ,$$

substituting $f = \frac{n}{T}$

$$Plot\ 1 = 20\log_{10}(2\mathrm{A}\frac{t}{\mathrm{T}}) \tag{14}$$

$$Plot\ 2 = 20\log_{10}|\mathrm{sinc}(\pi\mathrm{T}f)| \tag{15}$$

$$Plot\ 3 = 20\log_{10}|\mathrm{sinc}(\pi tf)|. \tag{16}$$

The DM spectrum envelope shown in Figure 32 depicts spectral content as proportional to the signal amplitude, and pulses having a smaller rise/fall time will have larger high-frequency spectral content.

For a distorted differential signal, consider the P channel with a rise time t_{rp}, a fall time t_{fp} and an N channel with a rise time t_{rn} and a fall time t_{fn}, with a pulse width T for both channels. The rise/fall time distortion can be expressed as

$$t_{rp} = t_{rn} \neq t_{fp} = t_{fn}. \tag{17}$$

The trigonometric coefficients of the CM signal can be expressed as

$$c_0 = \mathrm{A}\frac{\mathrm{T}}{\mathrm{T}}. \tag{18}$$

For the P channel,

$$c_n = -j\frac{\mathrm{A}}{2\pi n}e^{-jn\omega_0\left[\frac{\mathrm{T}+t_{rp}}{2}\right]}\left(\frac{\sin\left(\frac{1}{2}n\omega_0 t_{rp}\right)}{\frac{1}{2}n\omega_0 t_{rp}}e^{jn\omega_0\frac{\mathrm{T}}{2}} - \frac{\sin\left(\frac{1}{2}n\omega_0 t_{fp}\right)}{\frac{1}{2}n\omega_0 t_{fp}}e^{-jn\omega_0\frac{\mathrm{T}}{2}}\right) \tag{19}$$

$$c_n = -j\frac{\mathrm{A}}{2\pi n}\left[\mathrm{sinc}\left(\frac{1}{2}jn\omega_0 t_{rp}\right)e^{jn\omega_0\frac{\mathrm{T}}{2}} - \mathrm{sinc}\left(\frac{1}{2}jn\omega_0 t_{fp}\right)e^{-jn\omega_0\frac{\mathrm{T}}{2}}\right]\left[cosn\omega_0\left[\frac{\mathrm{T}+t_{rp}}{2}\right] - jsinn\omega_0\left[\frac{\mathrm{T}+t_{rp}}{2}\right]\right]. \tag{20}$$

Using the expression,

$$a_n = 2Re\{c_n\} \tag{21}$$

$$b_n = -2Im\{c_n\} \tag{22}$$

$$a_{nP} = -\frac{2A}{2\pi n}\left[\mathrm{sinc}\left(n\pi f t_{rp}\right)e^{jn\pi f\mathrm{T}} - \mathrm{sinc}\left(n\pi f t_{fp}\right)e^{-jn\pi f\mathrm{T}}\right]\left(sinn\pi f\left(\frac{\mathrm{T}+t_{rp}}{2}\right)\right) \tag{23}$$

$$b_{nP} = \frac{2A}{2\pi n}\left[\mathrm{sinc}\left(n\pi f t_{rp}\right)e^{jn\pi f\mathrm{T}} - \mathrm{sinc}\left(n\pi f t_{fp}\right)e^{-jn\pi f\mathrm{T}}\right]\left(cosn\pi f\left(\frac{\mathrm{T}+t_{rp}}{2}\right)\right). \tag{24}$$

For the N channel,

$$c_n = j\frac{\mathrm{A}}{2\pi n}e^{-jn\omega_0\left[\frac{\mathrm{T}+t_{fn}}{2}\right]}\left(\frac{\sin\left(\frac{1}{2}n\omega_0 t_{fn}\right)}{\frac{1}{2}n\omega_0 t_{fn}}e^{jn\omega_0\frac{\mathrm{T}}{2}} - \frac{\sin\left(\frac{1}{2}n\omega_0 t_{rn}\right)}{\frac{1}{2}n\omega_0 t_{rn}}e^{-jn\omega_0\frac{\mathrm{T}}{2}}\right) \tag{25}$$

$$c_n = j\frac{\mathrm{A}}{2\pi n}\left[\mathrm{sinc}\left(\frac{1}{2}jn\omega_0 t_{fn}\right)e^{jn\omega_0\frac{\mathrm{T}}{2}} - \mathrm{sinc}\left(\frac{1}{2}jn\omega_0 t_{rn}\right)e^{-jn\omega_0\frac{\mathrm{T}}{2}}\right]\left[cosn\omega_0\left[\frac{\mathrm{T}+t_{fn}}{2}\right] - jsinn\omega_0\left[\frac{\mathrm{T}+t_{fn}}{2}\right]\right] \tag{26}$$

$$a_{nN} = \frac{2A}{2\pi n}\left[\mathrm{sinc}\left(n\pi f t_{fn}\right)e^{jn\pi f\mathrm{T}} - \mathrm{sinc}\left(n\pi f t_{rn}\right)e^{-jn\pi f\mathrm{T}}\right]\left(sinn\pi f\left(\frac{\mathrm{T}+t_{fn}}{2}\right)\right) \tag{27}$$

$$b_{nN} = \frac{-2A}{2\pi n}\left[\mathrm{sinc}\left(n\pi f t_{fn}\right)e^{jn\pi f\mathrm{T}} - \mathrm{sinc}\left(n\pi f t_{rn}\right)e^{-jn\pi f\mathrm{T}}\right]\left(cosn\pi f\left(\frac{\mathrm{T}+t_{fn}}{2}\right)\right) \tag{28}$$

$$a_{n\_CM} = \frac{a_{np}+a_{nN}}{2} \tag{29}$$

$$b_{n\_CM} = \frac{b_{np}+b_{nN}}{2} \tag{30}$$

$$a_{n\_CM} = \frac{A}{2\pi n}\left\{\left[\left[\mathrm{sinc}\left(n\pi f t_{fn}\right)e^{jn\pi f\mathrm{T}} - \mathrm{sinc}\left(n\pi f t_{rn}\right)e^{-jn\pi f\mathrm{T}}\right]\left(sinn\pi f\left(\frac{\mathrm{T}+t_{fn}}{2}\right)\right) - \left[\mathrm{sinc}\left(n\pi f t_{rp}\right)e^{jn\pi f\mathrm{T}} - \mathrm{sinc}\left(n\pi f t_{fp}\right)e^{-jn\pi f\mathrm{T}}\right]\left(sinn\pi f\left(\frac{\mathrm{T}+t_{rp}}{2}\right)\right)\right\} \tag{31}$$

$$b_{n_{CM}} = \frac{A}{2\pi n}\{[sinc(n\pi f t_{rp})e^{jn\pi fT} - sinc(n\pi f t_{fp})e^{-jn\pi fT}](cosn\pi f\left(\frac{T + t_{rp}}{2}\right) -$$

$$[sinc(n\pi f t_{fn})e^{jn\pi fT} - sinc(n\pi f t_{rn})e^{-jn\pi fT}](cosn\pi f\left(\frac{T+t_{fn}}{2}\right))\}. \quad (32)$$

Due to the mismatch of the rise/fall time in the P/N channel the trigonometric coefficients a_n and b_n are non-zero, the differences of the sinc function with different fundamental periods creates spectral tones at the symbol rate and multiples of the symbol rate, and the above expression of the expansion coefficients cannot be simplified further. For a non-distorted differential signal with a symmetric rise and fall time in the P and N channel $t_{rp} = t_{rn} = t_{fp} = t_{fn}$,the trigonometric coefficients a_n and b_n cancel each other out and the CM noise spectrum only consists of a single tone at the DC, as shown in Figure 34.

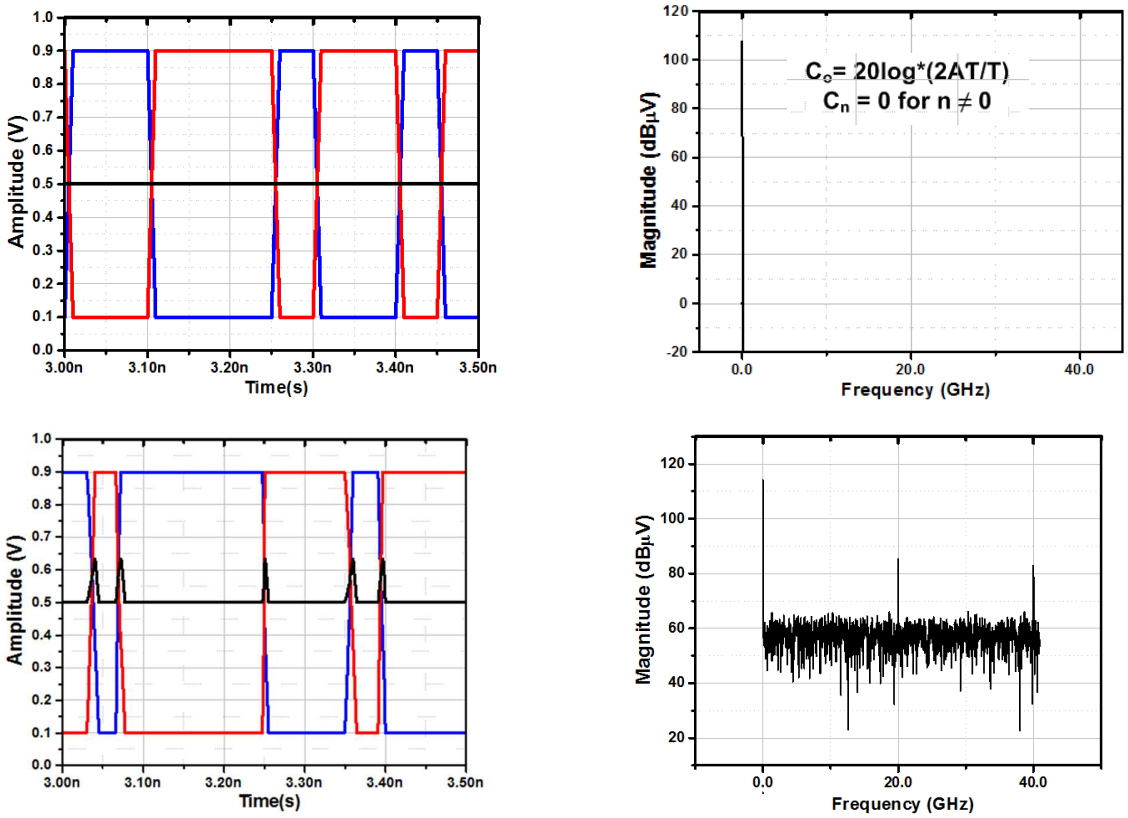


Figure 34. (a) Non-distorted differential signal and its output CM spectrum. (b) Distorted differential signal and its output CM spectrum.

4.4 Auto-Correlation Function of Distorted CM signal

The auto-correlation function measures the correlation of a signal x(t) with itself shifted by some time delay T, and it is used to detect repetition or periodicity in a signal. It is given by

$$c(\tau) = \frac{1}{t-\tau} \int_{0}^{t-\tau} x_{CM}(t) x_{CM}(t+\tau) dt. \tag{33}$$

This function is also used to quantify the effect of noise on a periodic signal [4]. In the absence of noise, the function oscillates with a constant amplitude and a maximum of 1, and the period of the auto-correlation corresponds to the period of the signal. However, in the presence of noise, the envelope of the auto-correlation function decreases exponentially, with higher noise, meaning higher decay. The half-life of the auto-correlation can be used to quantify the effect of noise.

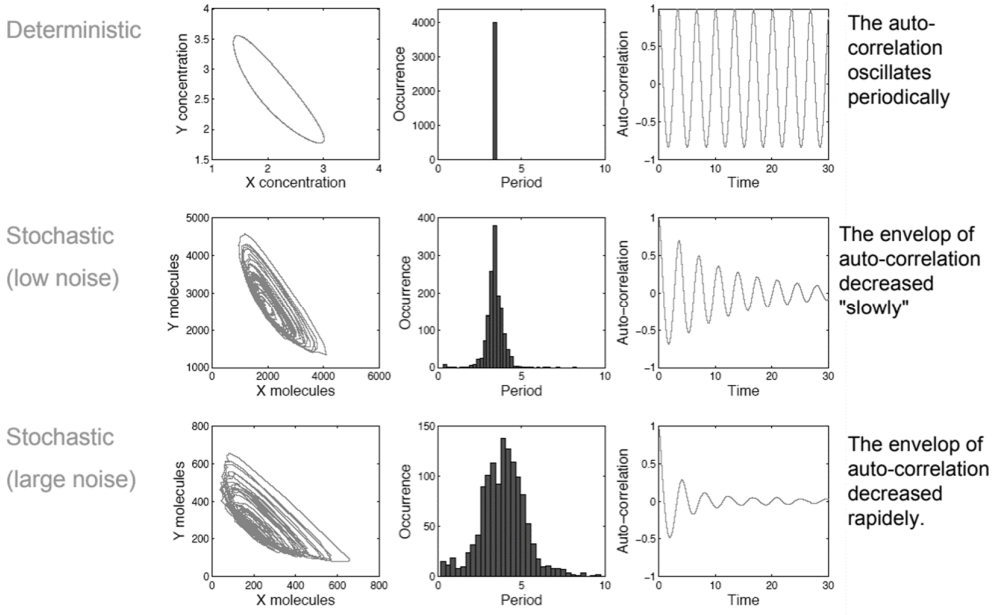


Figure 35. Use of the auto-correlation function to quantify the effect of noise on a periodic signal [5].

The CM voltage from a linear distortion of the differential signal is data-dependent, and therefore is stochastic in nature. For random data, the spurs on the CM voltage are randomly distributed, as is the noise energy. For a stochastic signal, the auto-correlation function decreases sharply, as shown in Figure 36.

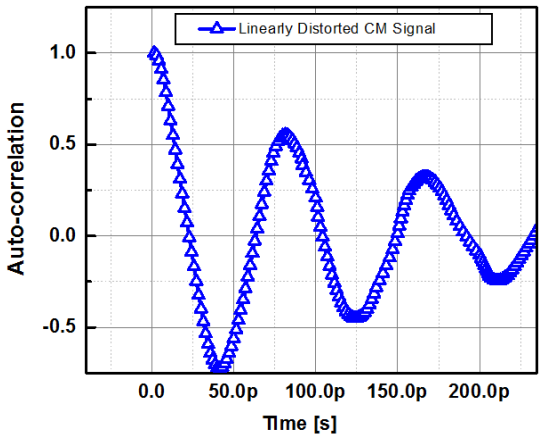


Figure 36. Auto-correlation of linearly distorted CM signal decaying slowly.

However, for a non-linear distortion, the polarity of the spurs on the CM voltage in a transient waveform are always monotonic and data-independent. Due to monotonic spurs and their polarity independent of data there exists a strong auto-correlation of the CM signal at the symbol interval, as shown in Figure 37. As a result, there exists a large power component or spectral tones at twice the Nyquist frequency or symbol rate and multiples of the symbol rate.

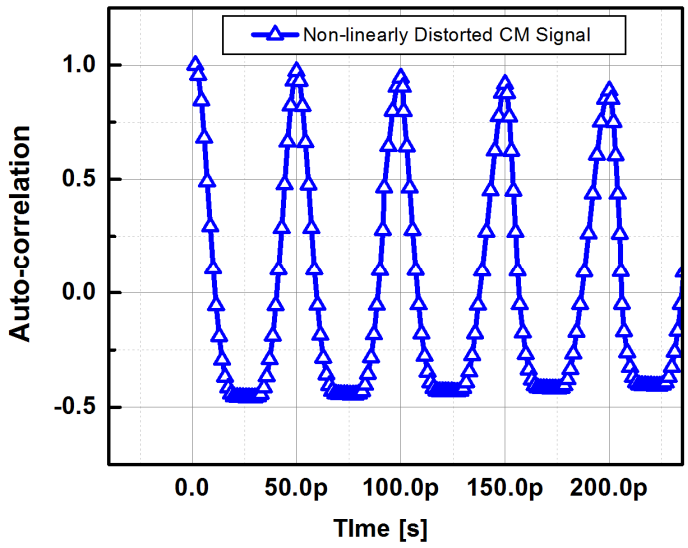


Figure 37. Auto-correlation of non-linearly distorted CM signal oscillates periodically at symbol interval.

4.5 Chapter Conclusion

CM noise is mainly contributed by the non-linear active circuit. The rise and fall time mismatch from the Tx circuit produce deterministic spurs on the CM voltage that generate certain spectral tones at twice the Nyquist frequency, which can lead to EMC failure. Therefore,

the absolute CM noise from the signal source alone affects most of the output CM profile. On the other hand, mismatch between the P/N channels only provides slight mode conversion between DM and CM.

4.6 References

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Chapter 5 CM NOISE ANALYSIS OF OUTPUT DRIVER

The rise/fall time mismatch from the Tx circuit is the source of CM noise. It is responsible for producing a large power component at F_{dr} and degrades the EMC performance, as explained in Chapter 4. The slew-rate is mainly determined by the output driver [1] and is an important component of high-quality signal integrity due to the rapid growth in interface speed. The aim of this chapter is to identify the intrinsic source of the rise/fall time mismatch in the output driver that eventually leads to output CM noise.

5.1 Output Driver Design

The CM noise analysis is performed on SST designed and simulated in a 65-nm CMOS process. The analysis is applicable to all SERDES transmitter interfaces. The SST driver shown in Figure 38 contains a pull-up and a pull-down branch implemented with a PMOS or NMOS transistor in series with a poly resistor (R_{SERIES}). The resistance of the transistor is nonlinear and susceptible to PVT variations. If the impedance of the driver does not match the characteristic impedance of the channel, the driver is unable to provide maximum power to the channel because of reflection at the transmitter side [2]. Furthermore, if the characteristic impedance of the channel does not match the impedance of the terminal, the channel is unable to deliver maximum power to the terminal because of reflection at the receiver side. The modified SST driver is implemented with a single series resistor in the signal path, which reduces the parasitic capacitance associated with the resistor by half. An R_{SERIES} value of 50Ω is selected in the design, as the input reflection coefficient S_{11} parameter of the driver from an ideal transmission line is below -13 dB over the wide-band frequency domain, and hence the impedance of the output driver is well-matched to the transmission line.

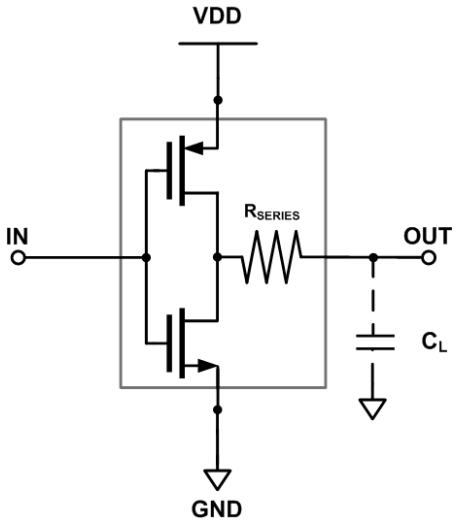

Figure 38. SST driver with capacitive loading.

Source impedance calibrated by adding adjustable resistance in series with pull-up and pull-down networks of all transmitter slices to compensate for device mismatch and process variations is presented in [3]. However, the technique has a voltage headroom penalty and requires a large number of resistors that need to be manually tuned. Independent impedance matching and equalization tuning by enabling identical parallel slices to be partitioned into four segments is proposed in [4]. The tuning is carried out by a complex calibration cell and requires external resistance. In [5], parallel identical slices are proposed and different unit weights are implemented through the values of the series resistance connected to the output terminal. However, the weight ratio of each tap changes with the PVT variations. A process-tolerant semi-self-impedance calibration method that produces process-dependent output is proposed in [6]. The method requires an analog-to-digital converter (ADC) and external resistance for impedance calibration. A process sensor circuit is proposed in [7] to generate a reference current, and it produces output that is process corner- dependent. It also requires an ADC for digitization of the signal and detects corners for the NMOS only.

Different termination options, namely, series, parallel, Thevenin and AC termination, exist in the SST driver in order for impedance to be matched to the transmission line, and these are shown in Figure 39. The problem of impedance matching in the SST driver is still an active research area [8].

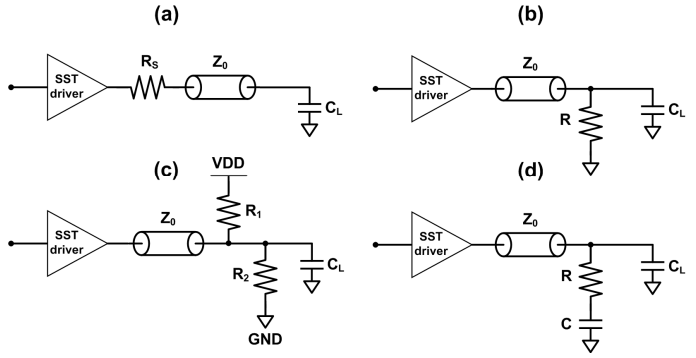

Figure 39. SST driver with termination options (a) series termination, (b) parallel termination, (c) Thevenin termination, and (d) AC termination.

5.2 First-Order Charging and Discharging Process Calculations

For simplification of calculations, an SST driver with ideal capacitive loading is considered. With first-order approximation, the charging/discharging calculations for the SST driver shown in Figure 40 are

$$V_{RISE} = V_{DD}(1 - e^{-\frac{1}{R_P' C_L} t}), \tag{1}$$

$$V_{FALL} = V_{DD} e^{-\frac{1}{R_N' C_L} t}, \tag{2}$$

where $R'_{P/N} = R_{P/N} + R_{SERIES}$ and for both the rising/falling edge, the time constant is determined by the non-linear resistance of the MOS devices, series termination resistor and output capacitance. The exponential part is the same for both the charging and discharging procedure.

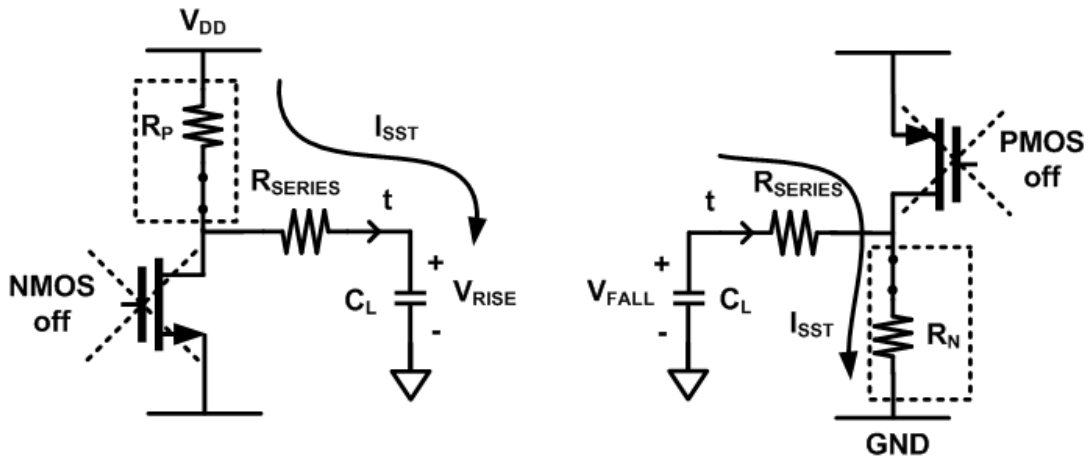

Figure 40. First-order charging/discharging process calculations.

5.3 Intrinsic Source of Rising and Falling Edge Mismatch

The operation region of MOS devices during OFF/ON switching varies from the cut-off region (region 3: VGS < Vth) to the saturation region (region 2: VGS > Vth / VDS > VGS – Vth), and finally gets into the triode region (region 1: VGS > Vth / VDS > VGS – Vth), as shown in Figure 41.The parasitic gate-source capacitance (C_{GS}) and gate-drain capacitance (C_{GD}) vary widely with the operation region of the transistors. At the output node, not only are the loading capacitance and resistance driven by the output driver, but also the parasitic capacitance of the transistors itself. The loading and self-parasitic capacitance are summed together to be the total loading of the output driver. However, during the switching period, cycling of the operation region leads to dramatic variation of C_{GS} (gate-source capacitance) and C_{GD} (gate-drain capacitance), which means the loading time constant will no longer be constant during the whole switching period. In practical switching, the loading is non-linear, and an intrinsic source of edge mismatch is the non-linear parasitic capacitance variations of the switching devices. The unbalanced edges directly create the CM noise tone at double the Nyquist frequency. Furthermore, the charging/discharging loop can be uncontrollable due to the complexity of the application environment, as it is possible that the parasitic inductance and capacitance in the charging and discharging loop are different.

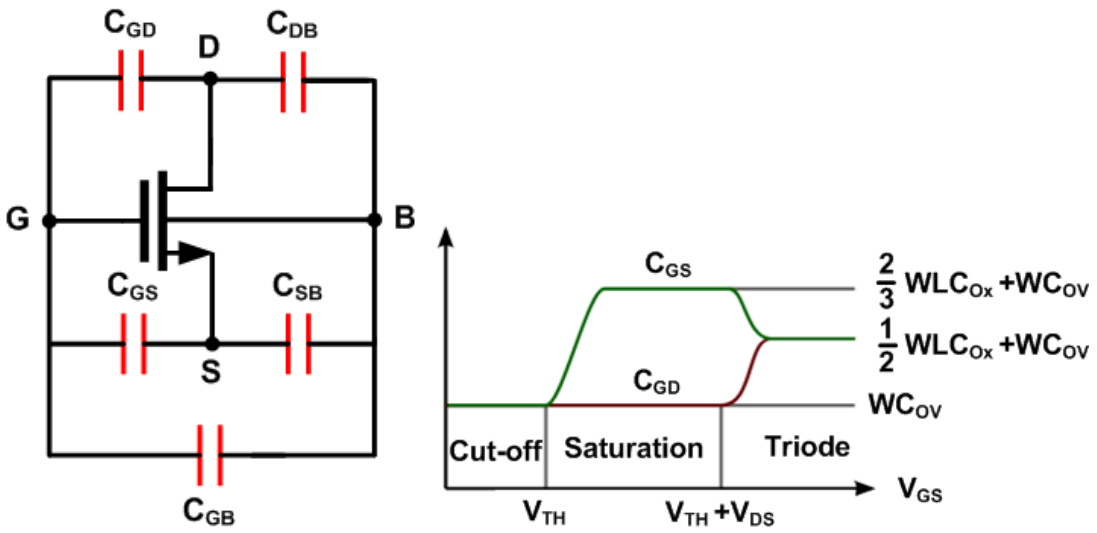

Figure 41. Change of MOSFET parasitic capacitances during various operation region.

5.4 CM Noise Dependency on Input Swing Amplitude and Operating Frequency

A higher input signal swing leads to higher parasitic impedance variation and therefore results in higher CM noise., whereas a small input driving signal swing leads to less transistor parasitic loading variation, which further indicates that smaller input swing necessarily reduces the impedance variation. Then, the reduction of parasitic loading variation finally reduces the CM noise by improving the matching of time constants in rising and falling edges. However, by adjusting the input swing, the output swing is affected as well. Therefore, for practical output driver design, higher input swing leads to unnecessary CM noise performance degradation, and the trade-off between the CM noise level and output swing should be carefully considered in the design procedure.

The non-linear active circuit, during the switching process, produces large time varying voltages (dV/dt), and through parasitic capacitances, generates the CM current that is finally converted into the CM voltage at the load impedance. The CM currents (I_{CM}) in the traces flow in the same direction and return to GND via the parasitic capacitor (C_P), as shown in Figure 43. The fields generated by the currents are equal in magnitude and polarity, thus emitting radiation proportional to I_{CM} and acting like an antenna. The energy of the emitted radiation (E_{CM}) is directly proportional to I_{CM} and the operating frequency (F_{OP}), as switching at higher frequencies results in higher CM current and noise [9],[10], as shown in Figure 42. The relation can be expressed as

$$E_{CM} \propto f(I_{CM}, F_{OP}). \quad (5)$$

Therefore, in order to suppress the radiation, it is critical to locate all possible loops in the design, as shown in Figure 43. The return path of the CM current to its source should be local and as compact as possible.

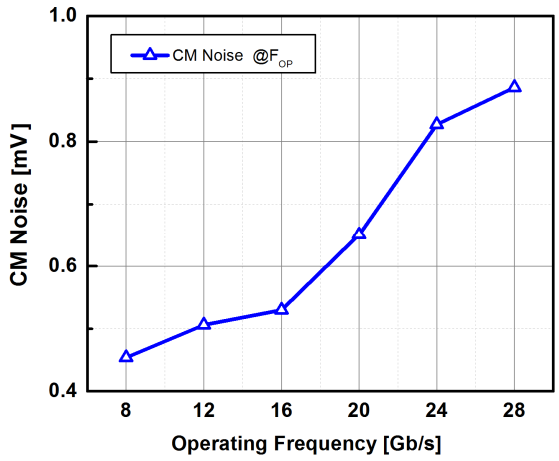

Figure 42. Relationship of CM noise with operating frequency for SST driver.

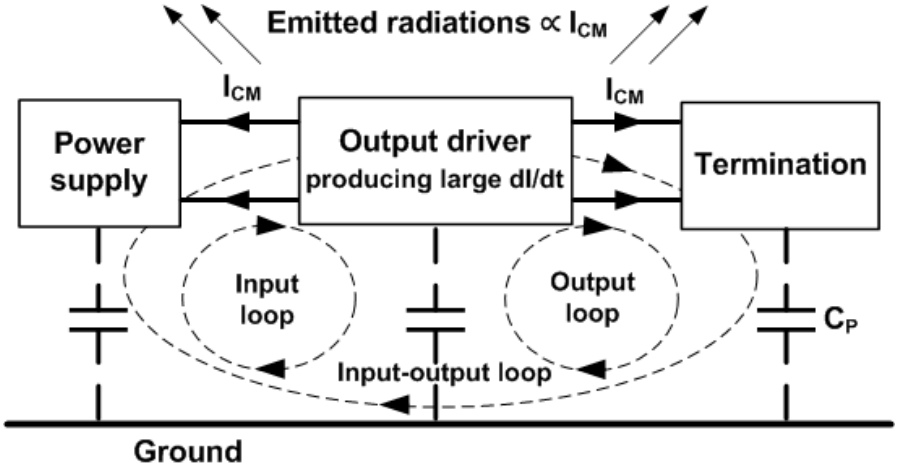

Figure 43. Possible concealed loops in the design formed from the parasitic capacitances.

5.5 Chapter Conclusion

Non-linear parasitic impedance variations of the switching devices are an intrinsic source for mismatch of the rising and falling edge and produce monotonic spurs on the CM voltage that generate certain spectral tones at twice the Nyquist frequency, causing the EMC failure. For practical cases, the charging and discharging procedure is not balanced due to the large parasitic impedance variations of MOS devices.

5.6 References

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Chapter 6 CM NOISE LEVEL PREDICTION OF OUTPUT DRIVER

Rise and fall time mismatch is produced by non-linear parasitic impedance variations of MOS devices, and it is key to identify all dependent factors that affect output CM noise. In this chapter, a novel methodology is proposed to analyze and predict the CM noise level of the output driver from various dependent parameters. The objective is to develop a prediction model to obtain the individual contribution of all dependent parameters to the CM noise. The presented methodology can be applied to all SERDES Tx circuit styles.

6.1 Proposed Methodology for CM Noise Level Prediction

Only the NISS produces a distorted differential signal with rising/falling edge mismatch, generating spectral tones at F_{dr}, as shown in Figure 22, whereas the NIPL only results in a slight mode conversion between DM and CM, thus producing a DM tone in addition to the CM noise tone produced by the NISS. It is concluded that the CM noise is primarily produced by the non-linear active circuit. Due to the complexity of CM noise analysis and level prediction, the influences on the output driver of non-idealities from the input signal swing, power supply and passive interconnections are analyzed independently to investigate the predominant factor of CM noise and to predict the individual contributions to the overall noise of the system. The proposed methodology is shown in Figure 44.

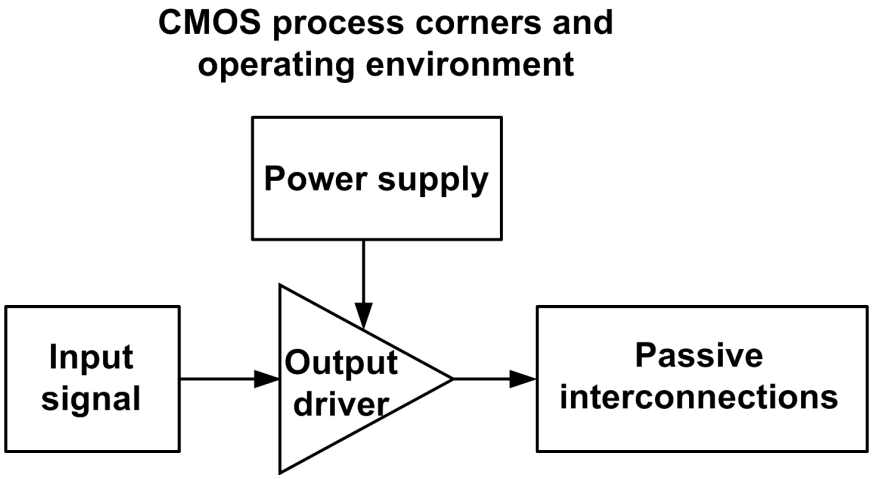


Figure 44. CM noise level prediction methodology for the output driver.

6.2 Description of Various Dependent Parameters

The detailed description of various dependent parameters is presented in the following section, along with the justification for why these parameters need to be investigated for accurate prediction of the output CM noise level.

6.2.1 CMOS Process Corners and Operating Environment

Process corners are a design-of-experiments technique that refers to fabrication parameter variations when applying an IC design to a semiconductor wafer. On a circuit with NMOS/PMOS devices fabricated at some process corners it may run slower or faster than specified within an adequate design margin. The naming convention for process corners is to use two-letter designators, where the first letter refers to the NMOS corner, and the second letter the PMOS corner. Three types of corners exist: typical, fast and slow. Fast and slow corners exhibit carrier motilities that are higher and lower than normal, respectively. Therefore, there are five possible corners: typical-typical (TT), fast-fast (FF), slow-slow (SS), fast-slow (FS), and slow-fast (SF). The first three corners (TT, FF, SS) are called even corners, because both NMOS and PMOS devices are affected evenly. The last two corners (FS, SF) are called skewed corners. This is because one type of device is much faster than the other. The five corners are depicted in Figure 45. In a push-pull driver, both NMOS and PMOS devices exist, so all process corners are included. In contrast, only NMOS devices exist in a CML driver; therefore, there are only even corners.

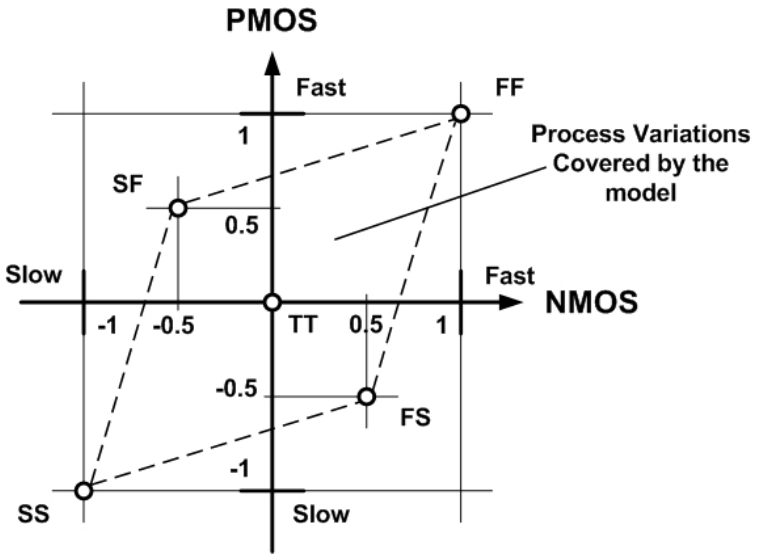


Figure 45. CMOS process corners.

During the fabrication of circuit devices, random variations occur, resulting in behavioral differences in identically designed devices. Device mismatches can be observed lot to lot, wafer to wafer, die to die and device to device due to manufacturing variations. It is non-trivial to analytically predict the variations or device mismatches due to accumulation of mismatch errors from individual devices. Monte Carlo analysis is used to investigate how individual device mismatches of a circuit accumulate and affect the circuit performance as a whole. For the advanced CMOS process, only PVT corners are insufficient to deal with the increased process variability. Foundries model the local and global process variations as distributions and the circuit designer's goal is to improve the statistical quantities, like parametric yield. The analysis is achieved by a large number of circuit runs where circuit devices have each been individually randomized in accordance to the mismatch model of the particular device type. The analysis is used to predict how well a transistor-level design will meet specifications and yield once manufactured. To summarize, process corners determine the mean value, while Monte-Carlo analysis gives the standard deviation. For Monte-Carlo analysis, the minimum run counts depend on how many sigma we are designing for. From such analysis we can provide the range of CM noise at 20GHz.

Temperature also affects device performance. The circuit should be robust enough to perform in a wide temperature scale. The broadly accepted grade for industrial applications is the temperature range from -40^{o}C to 85^{o}C. Therefore, the circuit should be simulated at a room temperature of 27^{o}C and at two extreme temperatures, -40^{o}C and 85^{o}C.

6.2.2 Output Driver Design

The output driver should be optimized to meet the output swing and bandwidth requirements with minimum power consumption. Furthermore, the circuit should also be optimized to attain the lowest CM noise level.

6.2.3 Input Signal Swing

Higher input signal swing leads to higher parasitic impedance variation and therefore results in higher CM noise, whereas a small input driving signal swing leads to less transistor parasitic loading variation, which further indicates that smaller input swing necessarily reduces the impedance variation. The reduction of parasitic loading variation reduces the CM noise by improving the matching of time constants in rising and falling edges. However, by adjusting the input swing, output swing is affected as well. Therefore, for practical output driver design,

higher input swing leads to unnecessary CM noise performance degradation, and a trade-off between CM noise level and output swing should be carefully considered in the design procedure.

6.2.4 Packaging and PCB Interconnections

The off-chip parasitic include packaging, PCB traces and connectors, and are shown in Figure 46. For practical cases, the packaging parasitic inductance should be taken into consideration.

The impact of PCB interconnections on the CM noise is investigated by including a different measured S-parameter-based model.

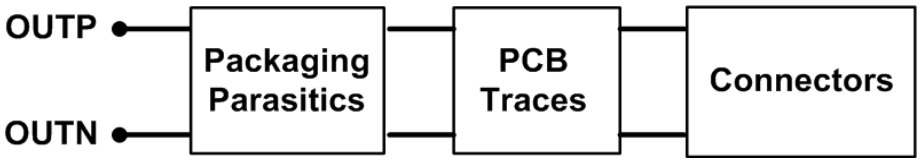


Figure 46. Off-chip parasitic.

6.2.5 Power Supply

In practical cases, depending upon the packaging, there may be parasitic resistance, capacitance or inductance degrading the power supply signal, and their effect on CM noise is investigated by including an equivalent lumped element model are shown in Figure 47.

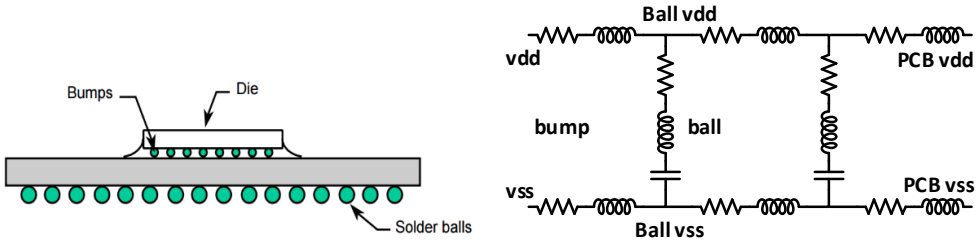


Figure 47. Power network model.

6.3 Push-Pull Output Driver

6.3.1 Driver Design

The minimum length of the technology is selected to minimize the capacitive load for the pre-driver stage. The push-pull current mode driver shown in Figure 48 has current sources at the top and bottom for improved signal integrity [1]. The topology precisely controls the output voltage swing through current limiting, provides a better common-mode rejection ratio (CMRR) and protects against damage caused by the signal at the input stages. The width of the

PMOS (W_p) is fixed, while the width of the NMOS (W_n) is varied. The ratio is referred to as a scaling factor, and an optimal value is found, yielding a lowest CM noise of 0.6 mV, referred to as the baseline level, at an input swing of 400 mV, without packaging and PCB trace parasitic and with an ideal power supply, as shown in Figure 48. The power consumption is around 4 mW for the output driver with V_{DD} of 1.2 V.

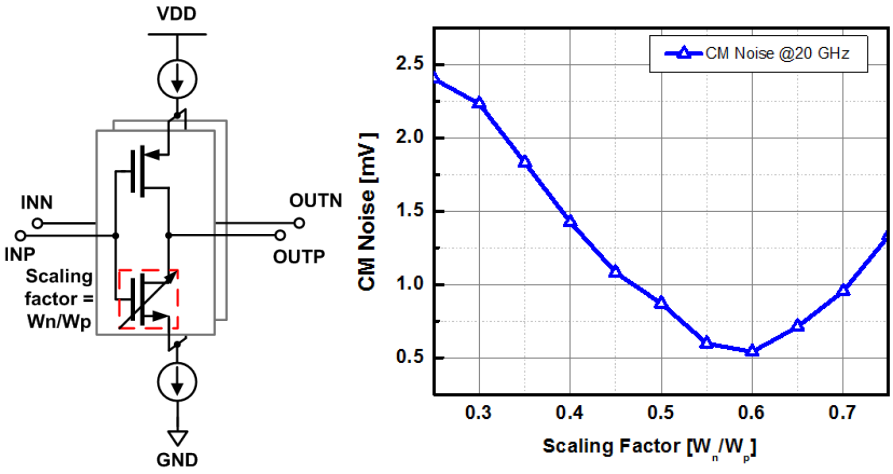


Figure 48. CM noise vs scaling factor at TT corner.

The complete test-bench to predict the CM noise level of an output driver with baseline conditions is shown in Figure 49. The output driver with passive loading shown in Figure 49 is comprised of C_{PAD}, which is the capacitance of the input/output pads. R_{LOAD} is the termination resistance to be impedance matched to the transmission line, C_G models the common-mode capacitor, which eliminates both differential-skew and CM noise, and C_{RCV} models the capacitance of the receiver input pads [2]. The current across the termination resistor creates the voltage signal at the receiver input.

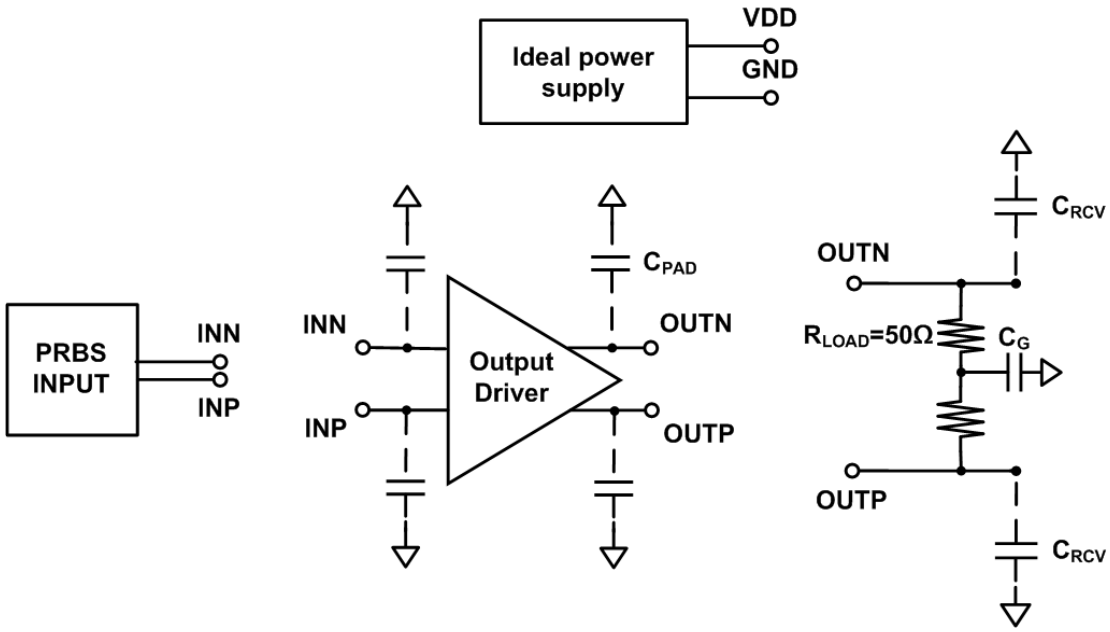


Figure 49. Test-bench for output driver with baseline conditions.

For practical cases, the packaging parasitic inductance should be taken into consideration. L_{PKG} models the inductance of the bonding wire or other packaging, and the transmission line and passive interconnection non-idealities are taken into consideration by the N-port model, as they affect the signal quality, as shown in Figure 50.

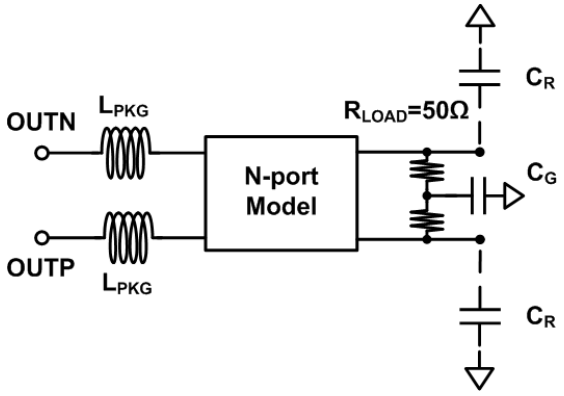


Figure 50. Impact of PCB interconnections on the CM noise investigated by including a measured S-parameter-based model.

In practical cases, depending upon the packaging, there may be parasitic resistance, capacitance and inductance degrading the power supply signal, As an example, the flip-chip packaging and its equivalent lumped element model are shown in Figure 51, as provided by our industrial partner Huawei.

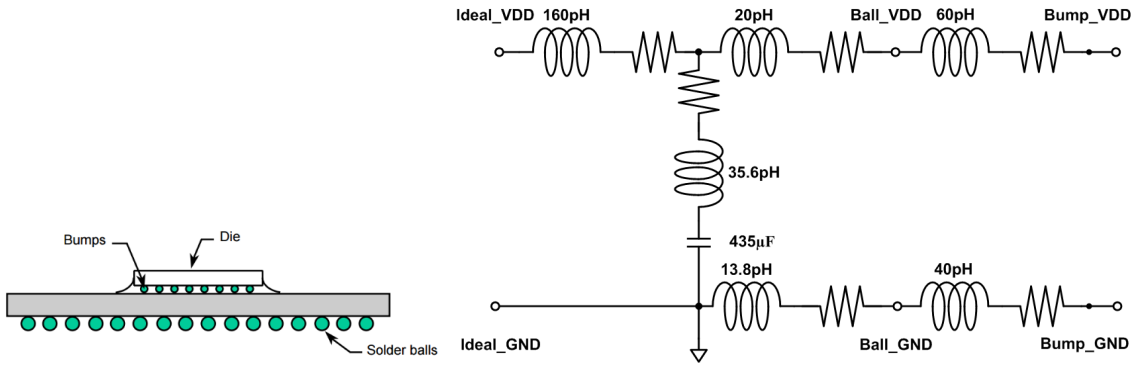


Figure 51. Non-ideal lumped power supply model.

6.3.2 CMOS Process Corners

Close to ideal switching from MOS devices leads to a higher symmetric rise and fall time of an output signal. Therefore, the FF corner has a lowest CM noise of 0.4 mV, whereas the SS corner, due to delayed switching, has a CM noise of 0.8 mV and the TT corner has CM noise of 0.6 mV. The skewed SF and FS corners, where imbalance switching is significantly higher, are the most problematic, and they have a CM noise of 4.6 mV and 3.5 mV, respectively.

Monte Carlo simulations

Monte-Carlo simulations need to be applied under different process corners because they reveal the random mismatch of devices, but process corners represent the global manufacturing difference. Under different process corners, the Monte-Carlo simulation results will be different. The Monte-Carlo simulation results under the TT corner are the most trustworthy because for commercialized ICs, the TT corner covers most cases and SS/FF corner products are not applicable. Therefore, Monte Carlo simulations are performed to quantify the random mismatch. The CM noise due to random mismatch is $\mu \pm 3\sigma$ is 0.53 mV.

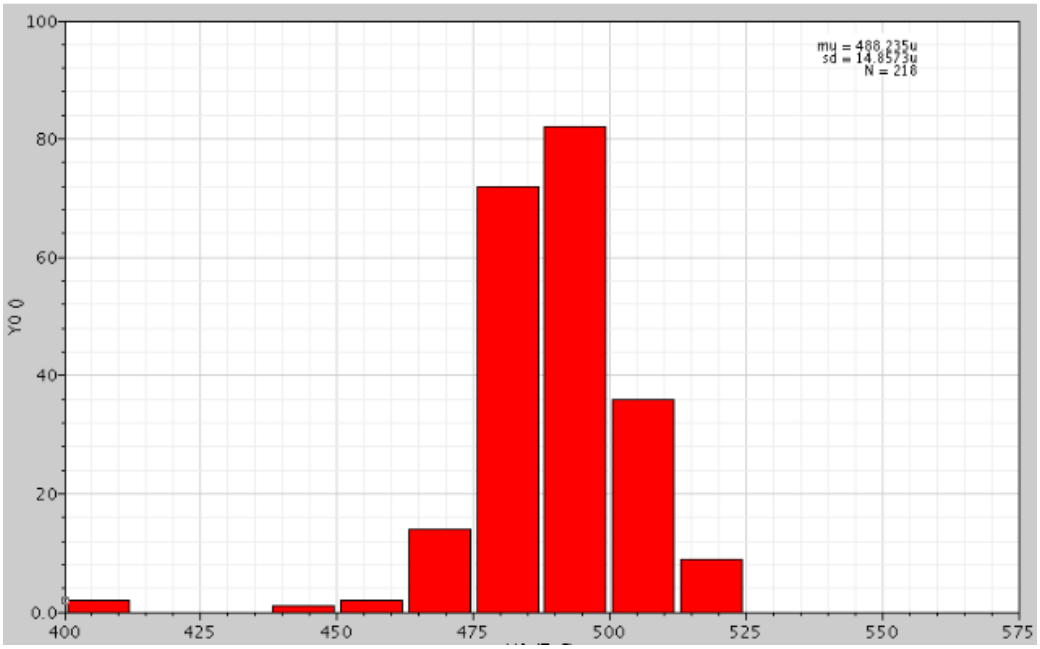


Figure 52. Monte Carlo simulations to quantify the random mismatch.

The above analysis is performed for non-return-to-zero (NRZ) code where one is represented by the positive voltage and zero is represented by the rest conditions. Return-to-zero (RZ) is a line code where signal drops to zero between each pulse. For RZ a separate clock does not need to send along with the signal but it will consume twice the bandwidth to achieve the same data-rate as compared to NRZ scheme and therefore is not considered in this work.

The threshold voltage of the NMOS is the applied gate voltage required to achieve the threshold inversion point, when the surface potential is $\phi_S = 2\,\phi_{Fn}$, and it is given by (1) and (2)

$$V_{THn} = \frac{2\sqrt{eN_D\varepsilon_S\phi_{Fn}}}{C_{ox}} + V_{FB} + 2\phi_{Fn} \quad (1)$$

$$\text{where } V_{FB} = \phi_{ms} - \frac{Q'_{ss}}{C_{ox}} \text{ and } \phi_{Fn} = V_t \ln\frac{N_D}{n_i}. \quad (2)$$

The threshold voltage (V_{TH}) has strong dependence on C_{ox}, which is a process-corner-dependent parameter. V_{TH} changes significantly during process corner variations, directly affecting the biasing and operation region of the transistors, and therefore results in imbalanced switching. The graph between the CM noise and edge time is plotted in Figure 53, and the direct relation affirms that the fast switching leads to less CM noise.

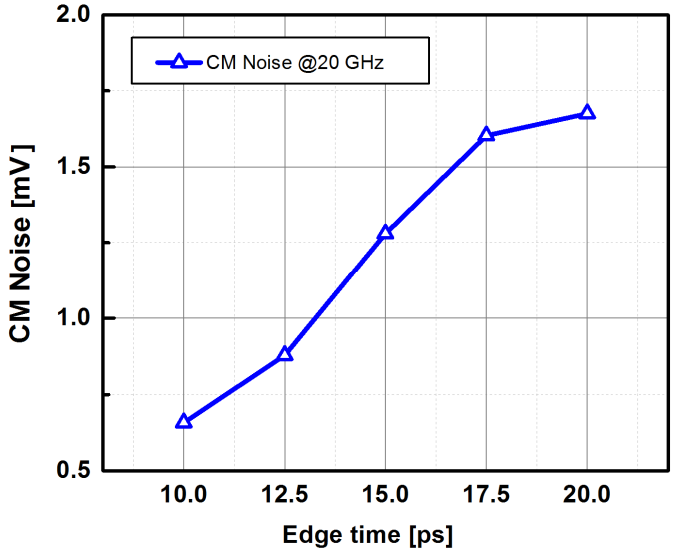


Figure 53. Relationship between edge time and CM noise at TT corner.

The correlation between the input CM voltage level and output CM noise at the FS, TT and SF corners is presented in Figure 54. The CM noise plot at the TT corner indicates that the "minimum" CM noise occurs when the input CM voltage is about 550 mV. A proper input CM level biases the transistors in the fast switching operation region (large transconductance g_m), where the transistor behaves most similarly to the ideal switch and generates the minimum amount of CM noise. For the push-pull driver, when either the input common mode is below or above the optimal point, it will be unable to fully set the NMOS transistor and PMOS transistor, respectively, into saturation operation, and therefore the CM noise levels will be higher. A decreased input CM level can compensate for the FS corner, making the NMOS slower and PMOS faster. In contrast, an increased input CM level can compensate for the SF corner by making the NMOS faster and PMOS slower. CM noise below 1 mV can be achieved at these skewed corners by adjusting the input CM level as shown in Figure 54. Therefore, proper biasing and operation conditions for the output buffer circuit improve the CM noise performance.

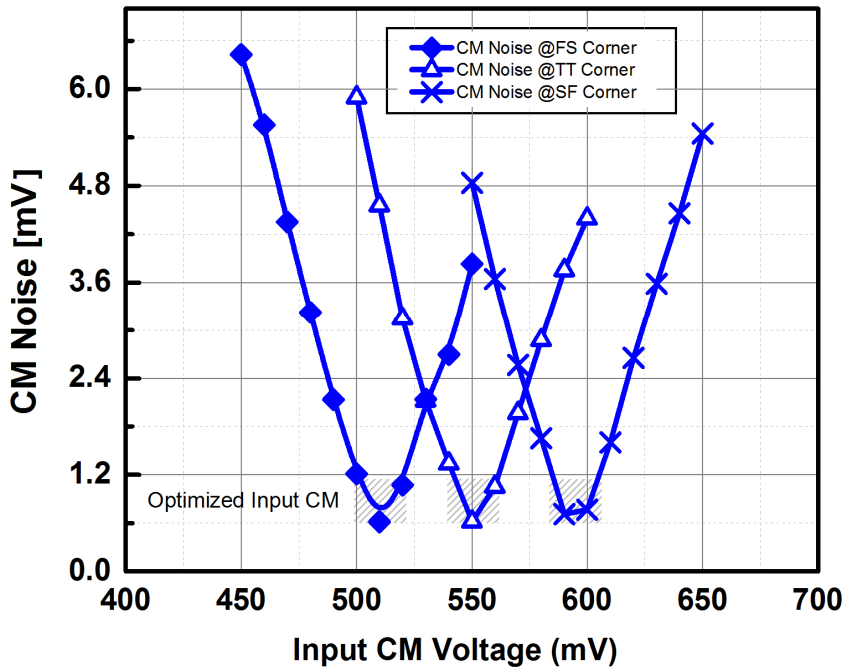
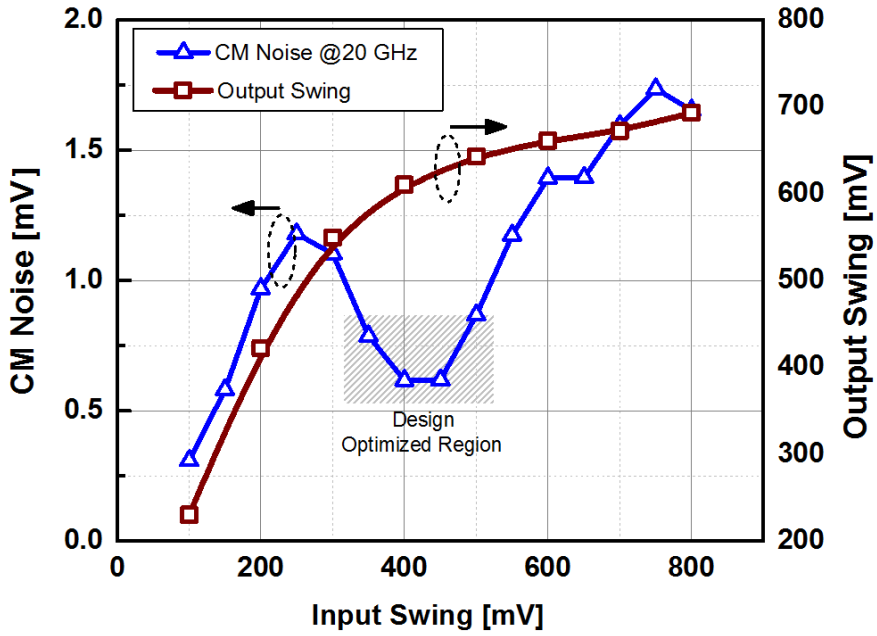


Figure 54. Input CM voltage vs output CM noise at different process corners.

6.3.3 Input Signal Swing

Higher input signal swing leads to higher parasitic impedance variation and therefore results in higher CM noise. Figure 55 shows the increase in CM noise at high input swing, beyond the designed optimized region. The decrease in CM noise around the region of 400 mV is due to the optimization of the core driver at that input signal swing level, which results in a higher symmetric rise and fall time of the output signal. Below the optimization point, the rise time is steeper than the fall time, and beyond the optimization point the fall time is steeper than the rise time, as shown in Figure 56 and Table 2, which is due to the differences in the overdrive voltages of MOS devices. In practical design, the trade-off between CM noise level and output swing should be carefully considered because any unnecessary increase in input swing leads to CM noise performance degradation, as shown in Figure 55.

(a)



(b)

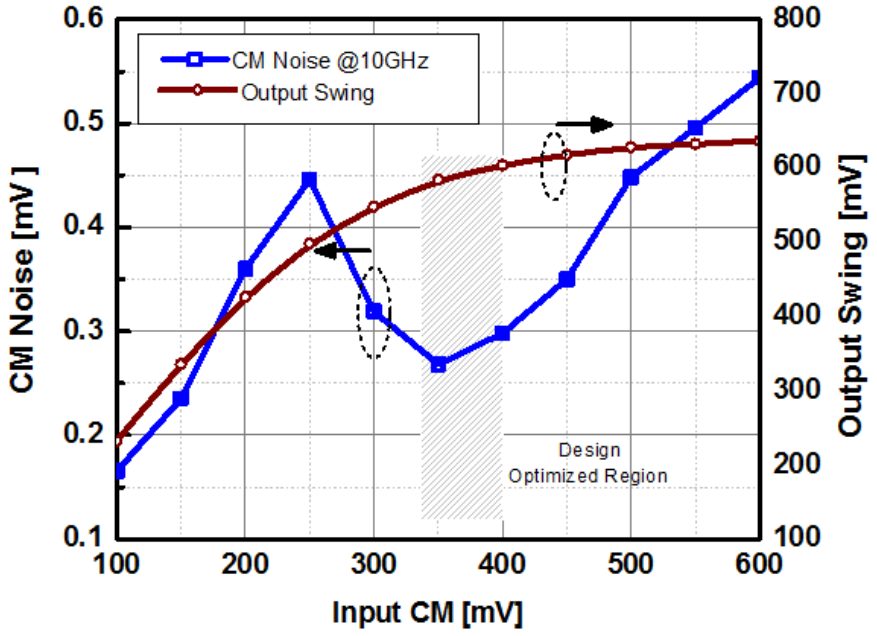


Figure 55. (a) Relationship of input swing, output swing and CM noise at data rate of 20-Gb/s, (b) relationship of input swing, output swing and CM noise at data rate of 10-Gb/s.

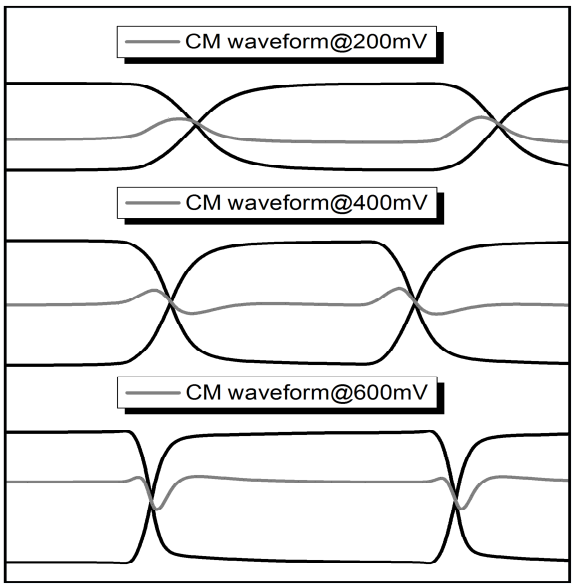


Figure 56. Output and CM waveform at different input swing.

Table 2. Rise and fall time at different input swing.

Input Swing (mV)	t_r (ps)	t_f (ps)	$(t_r - t_f) / 0.5*(t_r + t_f)$
200	12.6	13.0	-3.1%
400	11.0	10.8	+1.8%
600	9.3	7.9	+16.3%

6.3.4 Packaging and PCB Interconnections

The off-chip parasitic include packaging, PCB traces and connectors, and these are shown in Figure 46. For practical cases, the packaging parasitic inductance should be taken into consideration. Therefore, packaging inductance of 50–100 pH is included in the simulation, and the CM noise variation is only 8% from baseline level.

The impact of PCB interconnections on the CM noise is investigated by including a measured S-parameter-based model. The RF plot of the different channels studied is shown in Figure 57. It is observed that the PCB interconnects increase the CM noise by 7% from baseline level but degrade the signal quality, as shown in Figure 58. The signal quality can be improved by equalization that compensates for the frequency-dependent channel loss.

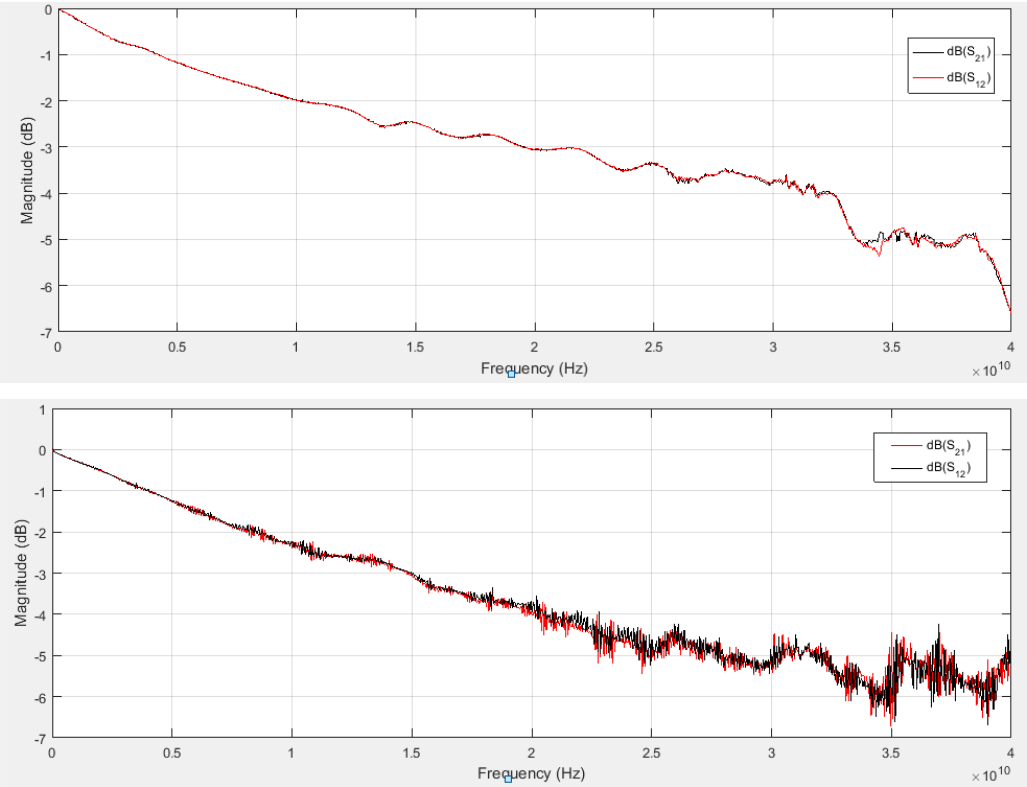


Figure 57. RF plot of different channels studied.

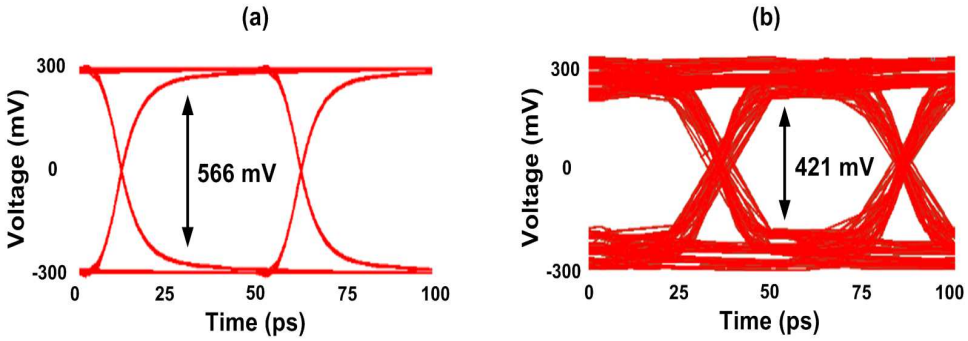


Figure 58. Eye diagram (a) without PCB interconnections, and (b) with PCB interconnections.

6.3.5 Power Supply

An on-chip decoupling capacitor between VDD and GND provides a low-impedance path for the return current at high frequencies and can be used to reduce the power supply noise. The power supply network becomes an LC resonant tank with the addition of a decoupling capacitor, and the resonant frequency of the LC tank should be less than the operating frequency; otherwise it will result in higher CM noise and be unable to provide a low-impedance path for

the return current [3–5]. The optimal decoupling capacitance of 0.5 pF employed in our case pushes the resonant frequency below the operating frequency to achieve a CM noise level of around 0.6 mV, as shown in Figure 59.

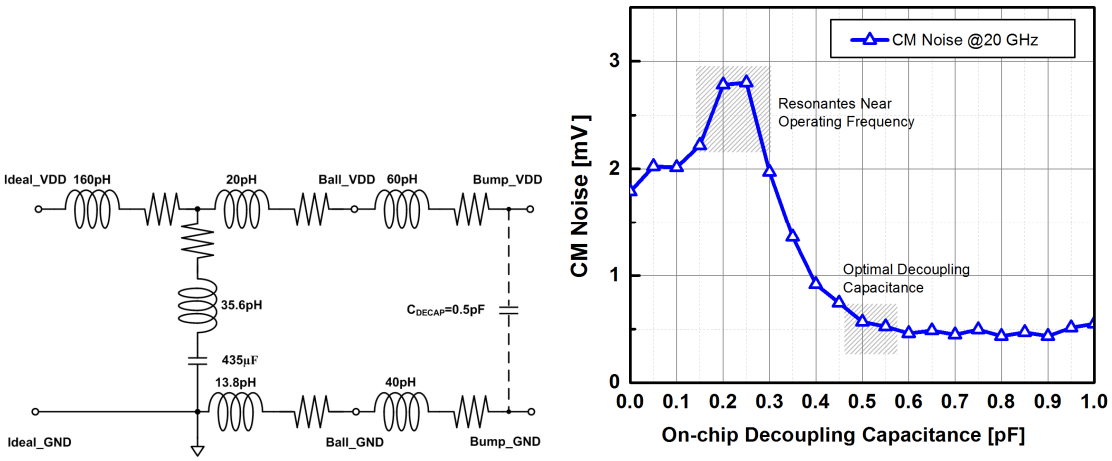


Figure 59. CM noise vs on-chip decoupling capacitance.

6.3.6 Predicted CM Noise Levels

The predicted CM noise levels from different dependant parameters are shown in Figure 60. In the worst-case scenario, the CM noise of the whole system is 5.9 mV. The process corner variations can increase the CM noise up to 7.6x from baseline level, a far greater impact than that of the other parameters.

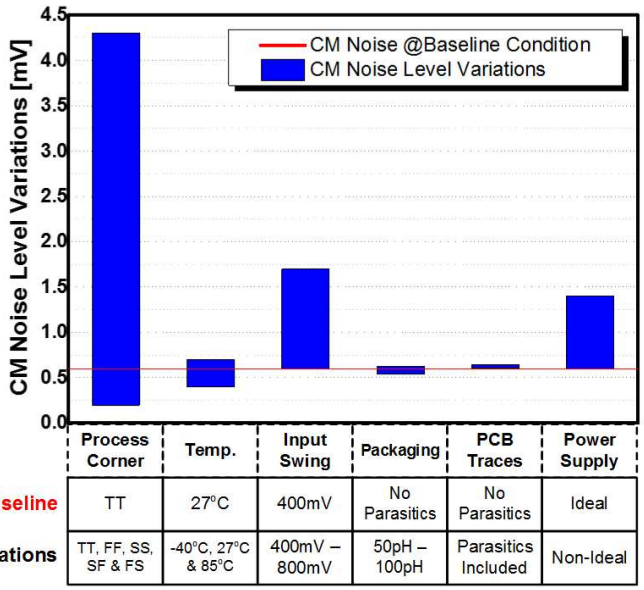


Figure 60. CM noise prediction from various dependent parameters.

6.4 Chapter Conclusion

A methodology to predict CM noise from various dependent parameters has been proposed. The output swing and CM noise is positively correlated, therefore minimizing the input signal swing, improving both the CM noise performance and power consumption. Furthermore, carefully designing the biasing/operation point of the output buffer circuit reduces the output CM noise and maintains sufficient gain in terms of output swing. For the push-pull driver, there also exists an optimal scaling factor and input swing amplitude that produce the lowest CM noise when the rising and falling edges are most symmetrical. The process corner variations in the push-pull driver can aggravate the CM noise level up to 7.6x from baseline level, a far greater impact than that of the other dependent parameters.

6.5 References

[1] “Application report SLLA120,” Texas Instruments, – Dec. 2002.

[2] “Application report SNLA034B,” Texas Instruments, – Aug.1993.

[3] P. Larsson, “di/dt noise in CMOS integrated circuits,” *Analog Integrated Circuits and Signal Processing*, vol. 14, no. 2, pp. 113–129, Sep. 1997.

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Chapter 7 CM Noise Level Prediction of High-Speed Parallel I/Os

EMI is becoming a serious issue as the data rate per lane and the number of parallel lines continue to grow rapidly. As data rates and system power continue to increase, more energy is present inside shielded enclosures [1]. Backplane and other dense interconnects for most applications are electrically long compared to the signal wavelengths they are transmitting, and can potentially radiate considerable amounts of energy. In this chapter, the CM noise level prediction for high-speed parallel I/Os is presented. As an example, the case of the Peripheral Component Interconnect - Express (PCIe) standard with different numbers of lanes having channels of a 16 Gb/s Tx link is simulated in the Keysight Advanced Design System (ADS) tool. The far electric field is observed at a distance of 3m and compared with the FCC regulatory requirements of unintentional radiation. The results affirm that CM noise is the dominant source of noise, and the worst-case scenario happens when radiation adds up constructively.

7.1 Transmitter Functional Block Diagram

The functional block of a transmitter is shown in Figure 61 [2]. The data is first encoded and then converted from a parallel bit stream to serial using a multiplexer, and finally reaches the transmitter's differential driver.

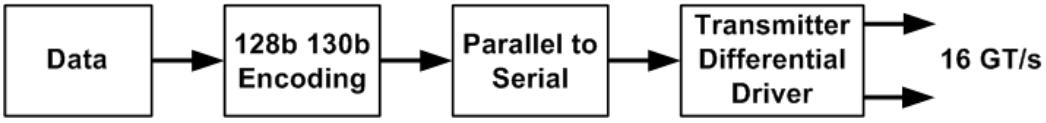

Figure 61. Transmitter block diagram for PCIe 4.0 standard.

The PCIe architecture is a high-performance I/O bus used to interconnect peripheral devices in applications such as computing and communication platforms. PCIe interconnects consist of either a x1 x2 x4 x8 x12 x16 or x32 point-to-point link [3], [4], as shown in Figure 62.

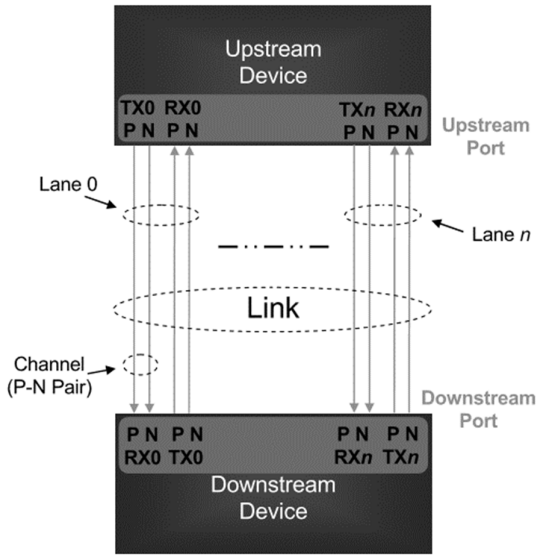

Figure 62. PCIe point-to-point Link.

Each lane consists of an upstream and downstream channel, i.e., a differential signal pair in each direction. For instance, a x32 link will comprise 32 lanes or 32 signal pairs in each direction.

7.2 Simulation Setup

Each lane consists of two channels, one for upstream and one for downstream. The channel is comprised of a P-N pair, as shown in Figure 65. The length of the PCB traces is selected as 3 cm and is terminated to 50 Ω loading. The close differential intra-pair air gap spacing is selected as 5 mils. The thickness of the PCB trace is 1.4 mils, and the thickness of the FR-4 substrate is 7.8 mils. The ground plane has a thickness of 0.7 mils. The differential pair-to-pair spacing is taken as 20 mils. to minimize crosstalk, as specified in the PCIe PCB design recommendations [4].

The P and N channel are excited with CM and DM noise of 1-V AC signal and maximum E-filed emission at 1 m is observed.

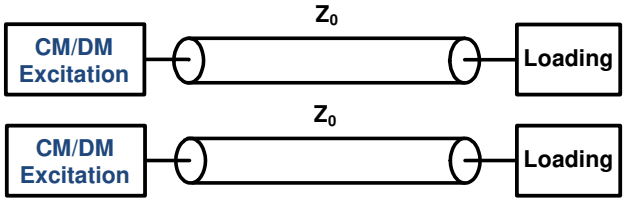

Figure 63. CM/DM excitation of 1-V AC signal in ADS.

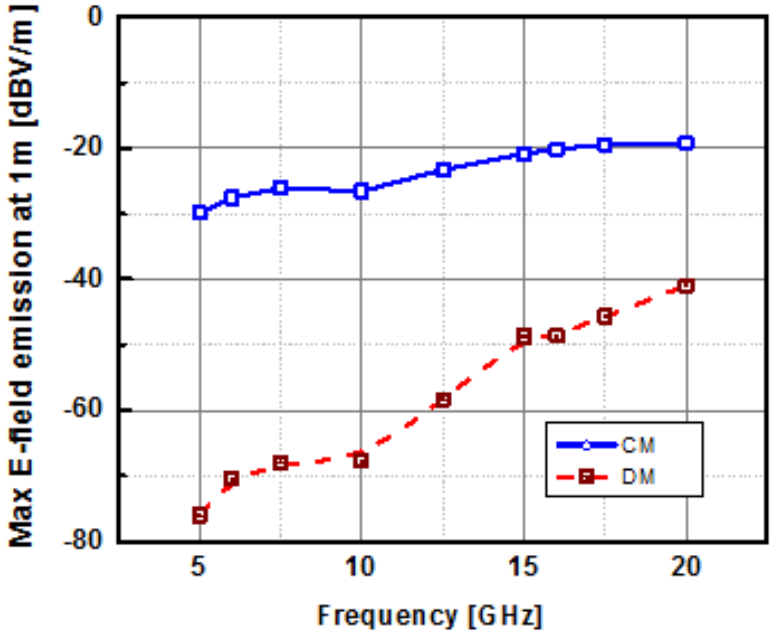

Figure 64. Maximum E-filed emission at 1 m from CM and DM excitation.

The CM excitation generates higher radiation power (29 dB @16 GHz) than DM excitation. That affirms that CM is the dominant source of electromagnetic radiations.

7.2.1 Case 1

First, we consider upstream case on the left-hand side of Figure 65. The link is composed of 4 Lanes. The transmitter ports are excited by the dominant CM signal of 5 mV produced at F_{dr} in the worst-case scenario, as explained in Chapter 6. Whereas the ports on the right-hand side are terminated at 50 Ω loading and the electromagnetic radiation from the parallel I/Os is investigated.

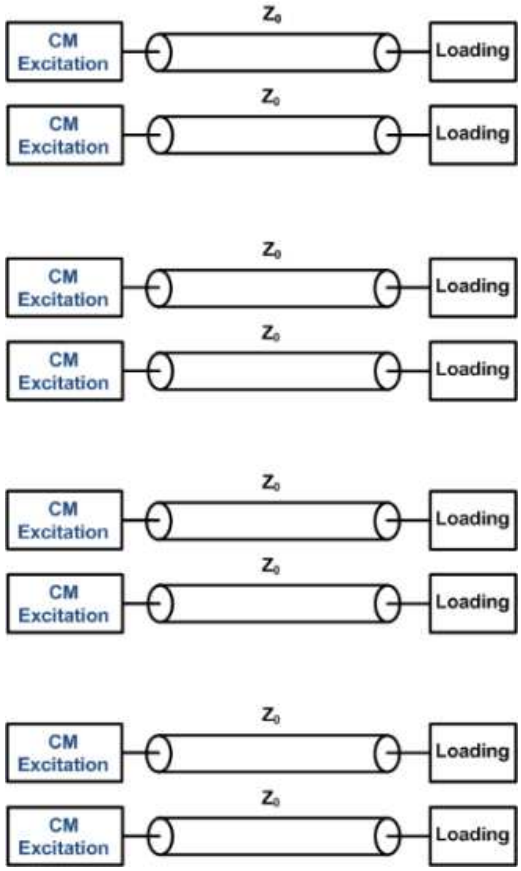

Figure 65. x4 lane PCB traces of 3cm length model in ADS.

For Case 1 with 5 mV as the CM voltage excitation, the far electric field at a frequency of 16 GHz at a distance of 3 m is shown to be 0.33 mV/m.

7.2.2 Case 2

The second case has eight Lanes and the ports are excited by the dominant CM signal of 5 mV. The ports on the right-hand side are terminated at 50 Ω loading. This case is compared with Case 1 to find out the effect of increasing the number of parallel I/Os from four lanes to eight lanes and its impact on overall electromagnetic radiation.

For Case 1 with 5 mV as the CM voltage excitation, the far electric field at a frequency of 16 GHz at a distance of 3 m is shown to be 0.67 mV/m.

7.3 Chapter Conclusion

The analysis in this chapter has affirmed CM noise is the dominant source of electromagnetic radiation. The DM excitation is 20 times higher, but since the currents are out of phase, the impact on electromagnetic radiation is not significant. In the case of parallel, I/Os, for instance in PCIe, the problem grows in complexity with the increase in the number of channels. The worst-case scenario occurs when CM noise tones at F_{dr} are in phase. As a result the radiation adds up constructively. By increasing the number of lanes from four to eight the radiated far electric field doubles at a 3 m distance. CM noise can become a serious issue and prevent the FCC's code of regulations being met. Therefore, it is of paramount importance to control the CM noise at the signal source, the Tx IC.

7.4 References

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Chapter 8 CM NOISE SUPPRESION OF HIGH-SPEED PARALLEL I/OS

Unwanted electromagnetic radiation is considered a packaging issue, and it is falsely believed that it is dependent on the RMS or absolute value of the slew-rate [1– 3]. The rise/fall time mismatch predominantly produces a deterministic spur on the CM voltage waveform, and as a result, there exists a strong auto-correlation function at the symbol rate and multiples of the symbol rate that in turn produces a large power component at twice the Nyquist frequency and its harmonics. Certain spectral tones are later radiated and can cause EMC failure. The CM spectrum is usually higher than the DM spectrum, and therefore, suppressing CM noise is critical to achieve better EMI performance

The conventional techniques to control CM noise from the packaging perspective involve reducing the parasitic capacitance, the CM current, and providing a local and compact CM current return path to its source. Filtering reduces the CM current on the traces and grounding provides the local return path for the CM current, whereas shielding simultaneously provides the return path for the CM current and reduces the parasitic capacitance [4]. Shielding prevents certain percentage of energy radiating from the system and its effectiveness also called shielded effectiveness (SE) expressed in dB. SE ratio is defined as the field strength without the shield interposed and with the shield interposed. The SE is around 20 dB or higher depending upon the construction and material of the shielding. Shielding is an effective way of suppressing electromagnetic radiations. However, it is costly solution and sometimes it is not viable such as in computer cards as they are intended to plugged into other system. Filtering requires specialized PCB expertise and often involves multiple iterations, while shielding is not a feasible solution in open-box equipment. CM choke can provide 8-10 dB reduction in radiation emissions. The CM choke require large area and work only at low frequencies. Reducing the slew-rate, as suggested by [1–3] will not result in improving the overall EMC performance because the EMI, usually dominated by the CM noise, is dependent on the mismatch of the rising/falling edge. Lots of work has been done on impedance calibration of the output driver to impedance-match it to the transmission line, and to decouple impedance matching and equalization. However, CM noise suppression techniques for the driver have rarely been reported.

8.1 Circuit Design Guidelines to Suppress CM Noise

CM noise is only generated by the intrinsic non-linearity of the signal source, namely the active circuit. Therefore, CM noise generated by the signal source dominates the output CM

noise profile, while the mismatch of the differential passive channels is not the most critical factor. Mismatch between differential channels provides slight mode conversion between CM and DM noise. Therefore, the most effective method to suppress the CM noise is by controlling it at the source, namely, the non-linear active circuit. The EMI issue usually comes up late in the system, around the developmental stage, and requires a costly solution that is difficult to implement. Therefore, it is essential to counter the EMI issue during the product design phase instead of handling it at the end of product development [5], [6]. The following are the circuit guidelines that can be taken into account in the design stage:

1. In an output driver with an NMOS-PMOS configuration, there exists an optimal P/N scaling ratio that gives the lowest CM noise.
2. The on-chip decoupling capacitor between the power rails reduces the power supply noise and also reduces the CM noise.
3. The reduced input swing leads to limited transistor parasitic loading variations, which eventually improves the rising and falling matching and reduces CM noise.
4. The output swing and CM noise trade-off should be carefully considered as higher output swing reduces the noise margin but increases the power consumption and the CM noise.
5. A proper input CM level biases the transistors in the fast switching operation region (large transconductance gm), where the transistor behaves most similarly to the ideal switch and generates the minimum amount of CM noise.

Due to the push-pull NMOS PMOS configuration in the output driver, the CM noise levels are aggravated under process variations. Therefore, it is of paramount importance to address the process corner variations for the suppression of CM noise. Ideally, the design parameters of the output driver should be self-adjustable, with little or no area/power overhead, and the output waveform should have a symmetric rising/falling edge. Unlike related works, our solution circumvents the essential and cumbersome EMI issues from the signal source by improving the matching of rise/fall time.

8.2 Proposed Architecture and Implementation

The system-level diagram of the proposed architecture to suppress CM noise is shown in Figure 66. The architecture comprises a differential push-pull driver and a slew-rate replica bias circuit with an external resistance. The replica bias circuit generates the slew control bias V_P and V_N and is used to make the pull-up and pull-down path resistance of the output driver constant over PVT variations. The driving capacitance of the output driver is mainly the gate

capacitance of the receiver, which is fairly constant over PVT variations, so the RC time constant of the output driver is conserved over PVT variations. Therefore, the output driver has a constant rising and falling edge. The proposed open-loop architecture is scalable and is amortized by enabling SOCs integrating several drivers to share one control circuit, as shown in Figure 66.

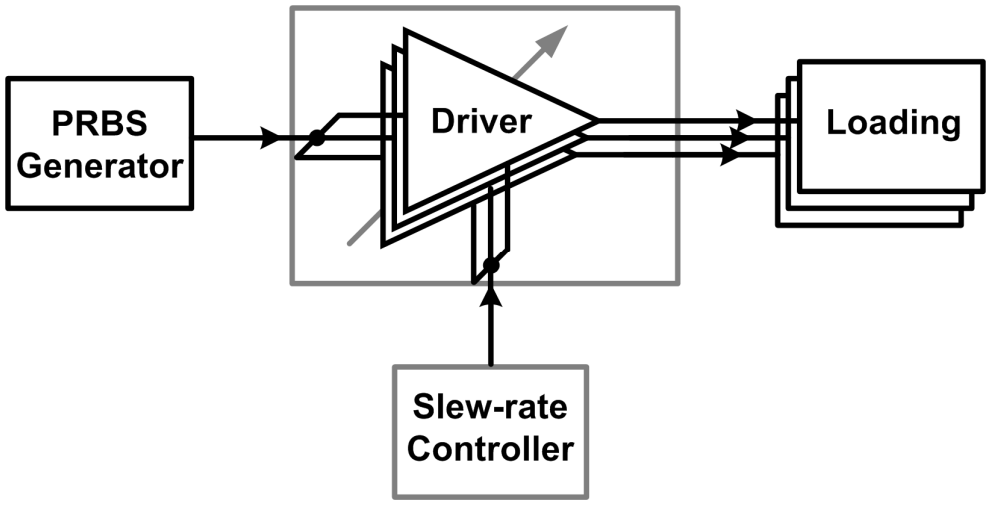

Figure 66. Proposed architecture.

8.3 Slew-Rate Controller

The slew-rate controller is designed to keep the pull-up and pull-down resistance constant over the PVT variations [7], and as a result, increase the matching of the rising and falling edge. NMOS and PMOS biased transistors are utilized to achieve this goal, and the path resistance of the output driver is controlled by the bias voltages generated by the replica circuit, as shown in Figure 67. R_{EXT} is the external resistance, and it is insensitive to the PVT variations. V_N is determined to be the value that makes voltages V_1 and V_{REF} the same by the negative feedback operations of M1, M2, OPAMP and R_{EXT}. V_{ref} is set to be ½ V_{dd}, and thus the resistance of the pull-down path comprised of M1 and M2 is the same as that of R_{EXT}. The pull-down path is the replica of the output driver pull-down path, and to reduce static power consumption, the resistance of the replica circuit is five times that of the output driver. The pull-up path resistance is adjusted to the pull-down path resistance by the negative feedback operation of the loop composed of MP1, MP2, OPAMP and R_{INT} (fixed pull-down path). The resistance of the pull-down path is equal to R_{EXT}, and as a result, the resistance of the pull-down and pull-up path is the same as that of R_{EXT}.

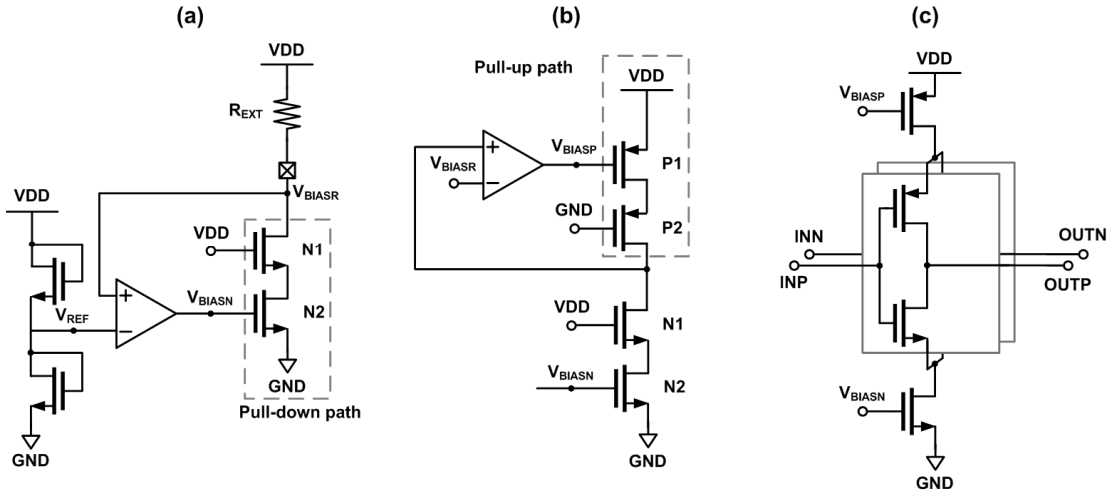

Figure 67. Implementation of proposed architecture: (a) pull-down replica bias, (b) pull-up replica bias, and (c) output driver.

8.4 Results and Discussions

The slew-rate of a 20-Gb/s output driver is controlled by an on-chip replica bias circuit to compensate for the process corner variations and is simulated in a 65 nm CMOS process. The waveforms before and after compensation at the SS, SF and FS corners, respectively, are shown in Figure 68.

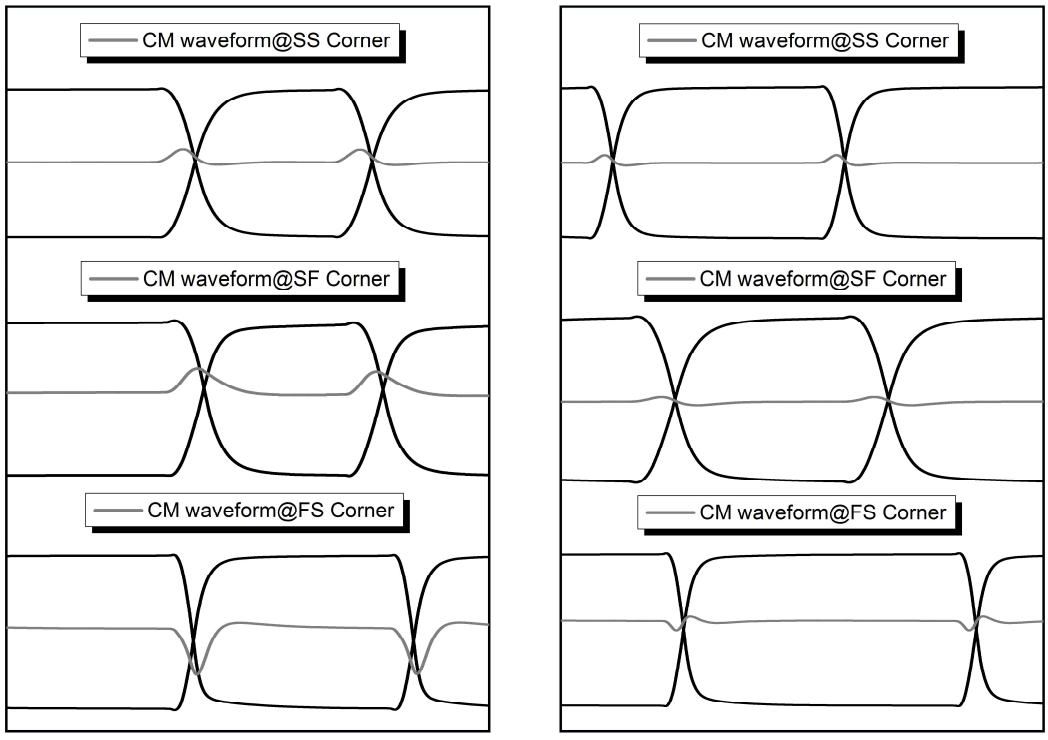

Figure 68. Output waveform (a) without compensation, and (b) with compensation.

Table 3. Rise and fall time at different process corners: (a) before compensation, (b) after compensation.

(a)

Process Corner	**t_r (ps)**	**t_f (ps)**	**$(t_r - t_f) / 0.5*(t_r + t_f)$**
SS	11.78	12.56	-6.4%
SF	9.78	13.13	-29.2%
FS	11.29	8.79	+24.9%

(b)

Process Corner	**t_r (ps)**	**t_f (ps)**	**$(t_r - t_f) / 0.5*(t_r + t_f)$**
SS	10.35	9.95	+3.9%
SF	10.17	11.10	-8.7%
FS	11.96	12.39	-3.5%

Monte-Carlo simulation is conducted under different process corners and results are shown in Table 4.

Table 4. Monte-Carlo simulation under different process corners.

	Schematic		
Process Corner	SS	SF	FS
Mean	0.28 mV	0.54 mV	0.20 mV
SD	0.02 µV	0.24 µV	0.06 µV

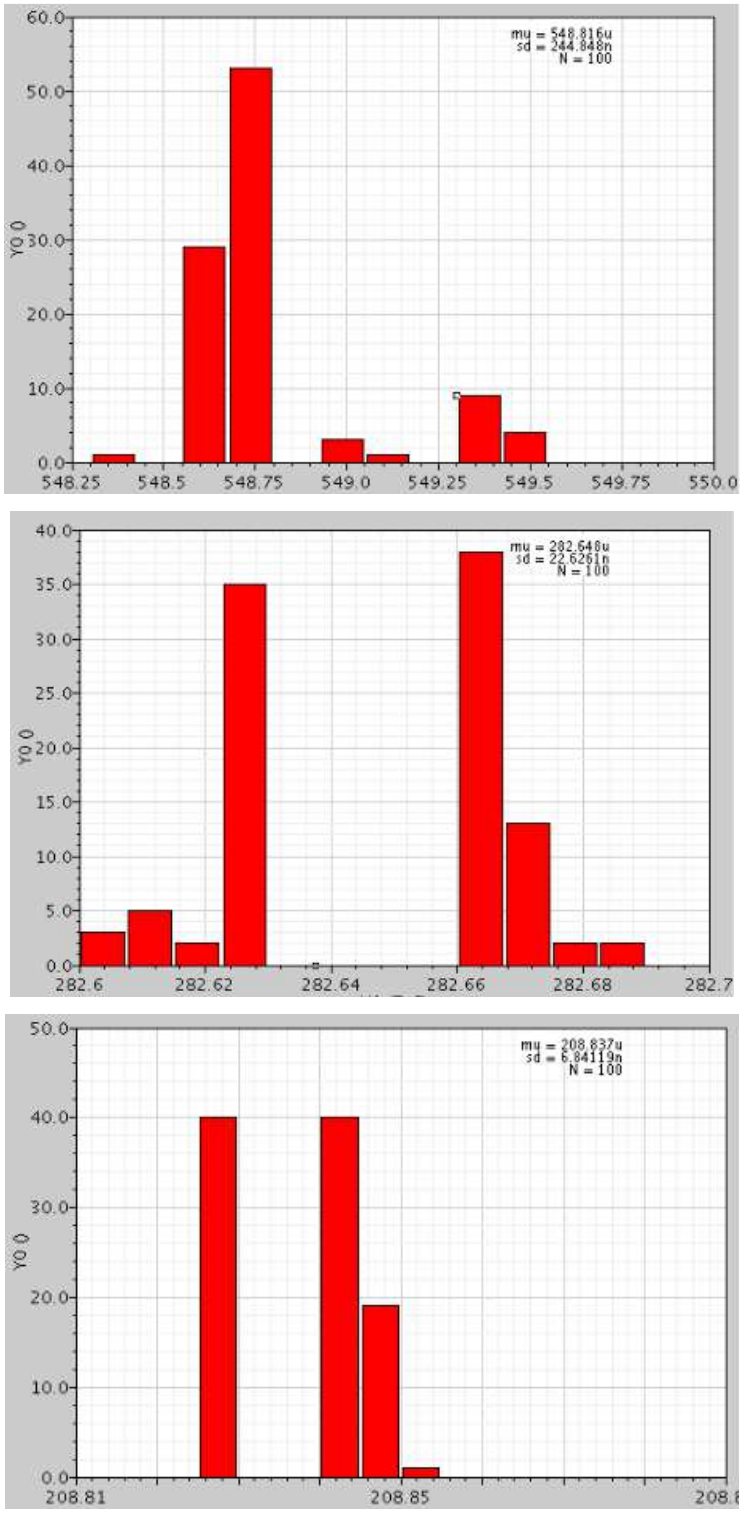

Figure 69. Monte Carlo simulation at different process corner (top to bottom) SF, SS and FS corner respectively.

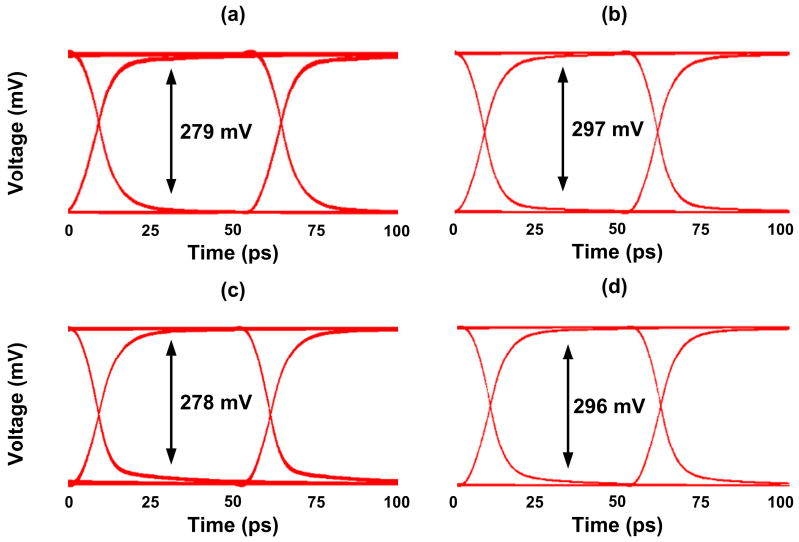

Figure 70. Eye diagram (single-ended) at (a) SF corner before M&C, (b) SF corner after M&C, (c) FS corner before M&C, (d) FS corner after M&C.

Besides CM noise reduction, a symmetric rising and falling edge is also desirable in many applications, including USB interfaces, for its improvement of signal quality. The vertical eye opening is increased by 18 mV for the SF and FS corners, respectively, as shown in Figure 70, and the peak CM noise for the output driver due to process corner variations is reduced by 5.4x (-81%).

Table 5. Work comparison.

SERDES Output Driver		Other Works	This Work
CM Noise Problem		Packaging Issue [5]	Circuit Issue
Source of EMI (Dominated by the CM Noise)		Absolute Value of Rise/Fall Time [1–3]	Mismatch of Rise/Fall Time
CM Noise Reduction Techniques	Packaging Technique	Filtering, Grounding and Shielding [4]	CM Noise Reduction Techniques
	Circuit Technique	Reducing the Slew-Rate [1],[2] and [7]	
CM Noise Reduction From the Signal Source		None	This Work

8.5 Chapter Conclusion

In this chapter, the results have elucidated that CM noise can be effectively reduced by controlling it at the non-linear active circuit that effects most of the output CM noise profile. The proposed architecture self-calibrates the output driver by mainting a constant slew-rate to compensate for process corner variations, resulting in improved matching of the time constants in the rising and falling edge. The proposed technique applied on a push-pull driver results in a 20% greater symmetric rise and fall time of the output signal, improves the signal quality by increasing the vertical eye opening by 18 mV and reduces the peak CM noise by 5.4x for the worst-case scenario.

8.6 References

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Chapter 9 CONCLUSION AND FUTURE WORK

This thesis presents CM noise analysis, prediction and suppression for high-speed CMOS SERDES transmitters. The work started from the system top-level and moved down to the transistor-level of ICs to investigate the EMI issue in a typical SERDES link.

The CM noise is mainly contributed by the non-linear active circuit, as explained in Chapter 4. The rise and fall time mismatch from the Tx circuit produces monotonic spurs on the CM voltage that generate certain spectral tones at twice the Nyquist frequency and can lead to EMC failure.

In Chapter 5 the intrinsic source for mismatched rising and falling edges is presented as the non-linear parasitic impedance variations of the switching devices.

In Chapter 6 a novel methodology is proposed to analyze and predict the CM noise from various dependent paramenters in a TSMC 65-nm CMOS process. The output swing and CM noise is positively correlated, therefore minimizing the input signal swing to improve both the CM noise performance and power consumption. Carefully designing the biasing/operation point of the output buffer circuit reduces the output CM noise and maintains sufficient gain in terms of output swing.

The EMI issue grows in complexity as the data rate per lane and the number of parallel lines continue to grow rapidly, as highlighted in Chapter 7.

Circuit design guidelines are presented in Chapter 8 for suppressing the CM noise during the design stage, and are applicable on all SERDES transmitter interface styles. The results have elucidated that CM noise can be effectively reduced by controlling it at the non-linear active circuit that effects most of the output CM noise profile.

9.1 Future work

The analysis, prediction and suppression work for high-speed parallel I/Os has been performed for non-return-to-zero (NRZ) signals. Next-generation optical networks will be based on the 200 and 400-GbE systems. As a result, the conventional NRZ modulation may no longer be sufficient to meet the requirements. By employing pulse-amplitude modulation (PAM)-4 or PAM-8, the circuits can operate at half or one third of the baud rate to reduce the high-frequency losses at the electrical/optical interface. For NRZ signals, we have seen that the rising/falling edge leads to spectral tones at twice the Nyquist frequency. The PAM-4 signal, on the other hand, has four levels, three eyes and twelve edge transitions. The EMI issues will

become more complex in the PAM-4 signaling technique due to the increasing number of edge transitions. Amplitude mismatch can also happen between the top, middle and bottom eye. Future work can be directed to investigating the CM noise issue for different signal modulation schemes such as PAM-4 or even PAM-8. The CM analysis can also be performed for return-to-zero coding scheme and compare which data scheme minimize the CM noise.

9.2 Original Contributions

The main contributions of this thesis are summarized as follows:

1. The predominant source of CM noise is the mismatched rise/fall time of the output signal produced due to the non-linear parasitic impedance variations of the MOS device is identified for the first time.
2. A mathematical analysis of CM noise is presented.
3. The spectral tones at twice the Nyquist frequency are explained by the monotonic CM signal spurs categorized as non-linear distortion.
4. A novel methodology is proposed to predict the CM noise level from various dependent parameters. As a result, a comprehensive qualitative and quantitative CM noise analysis and prediction of the output driver are presented.
5. Process corner variations are identified as the predominant factor aggravating the CM noise level compared to all other dependent parameters.
6. Controlling the source, namely the non-linear active circuit, is identified as the most effective way of suppressing the CM noise, rather than improving the matching of passive interconnections or using conventional EMI reduction techniques, as it effects most of the output CM noise profile.
7. Circuit design guidelines are presented for suppressing the CM noise during the design stage, and are applicable on all SERDES transmitter interface style.