# *Silicon-based Transmitter Design for Optical Fiber Communications*

by

**Fuzhan CHEN**

A Thesis Submitted to

The Hong Kong University of Science and Technology

In Partial Fulfillment of the Requirements for

The Degree of Doctor of Philosophy

in the Department of Electronic and Computer Engineering

January 2025, Hong Kong

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This is to certify that I have examined the above PhD thesis

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*To my parents*

# Acknowledgement

I would never have finished the research work covered in this thesis without my supervisors, Prof. C. Patrick YUE and Prof. Quan PAN. They provide me with opportunities for trial and error and support me through good and bad times. Their enthusiasm for research, years of patient guidance and valuable insights have not only laid the foundations for this thesis but also shaped my academic character.

I would like to express my gratitude to Prof. Wei-Zen CHEN, Prof. Kam Tuen LAW, Prof. Man Hoi WONG and Prof. Fengbin TU for serving as my thesis examination committee members and providing valuable insights and suggestions to my research. I also would like to thank Prof. Kam Sing WONG for serving as the chairperson for my thesis defense.

I extend my heartfelt appreciation to my colleagues at HKUST and SUSTech. I am grateful to Dr. Li WANG, Dr. Weimin SHI, Dr. Ziyang HONG, Dr. Yiru WANG, Dr. Bo XU, Dr. Lin WANG, Dr. Rehan AZMAT, Dr. Babar HUSSAIN, Mr. Chongyun ZHANG, Mr. Hoi Chuen CHENG, Mr. Can WANG, Mr. Xinyi LIU, Mr. Zilu LIU, Mr. Tianxin MIN, Mr. Johar ABDEKHODA, Mr. Jian KANG, Mr. Shuo FENG, Mr. Shaokang ZHAO, and Mr. Ruitao MA. My thanks also go to Mr. Jian YANG, Mr. Zhenghao LI, Mr. Liping ZHONG, Mr. Xiongshi LUO, Mr. Yangyi ZHANG, Mr. Hongzhi WU, Mr. Xuxu CHENG, Mr. Weitao WU, Mr. Wenbo XIAO, Mr. Wentao ZHOU, Mr. Xuewei YOU, Mr. Yunyun HOU, Mr. Kun ZHANG, Mr. Dongshen ZHAN, Mr. Zhenyu YAO, and Mr. Pingyi CAI. Our numerous discussions and collaborations have been indispensable cornerstones of my progress. Our friendships, forged through shared experiences and challenges, will last a lifetime.

Finally, I would like to express my gratitude and love to my family, especially my mother and father. Their unconditional love and support are the fuel for my driving alongside this long journey. Their happiness is the motivation of all my endeavors.

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# Silicon-based Transmitter Design for Optical Fiber Communications

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Abstract

Explosive increase of the data created by cutting-edge information technologies such as artificial intelligence and cloud computing demands intra- and inter-data center interconnects with higher data rate, higher power efficiency and lower latency. Fiber-based optical links outperform copper-based electrical links especially in terms of channel loss and bandwidth, and hence becoming the mainstream choice for communication scenarios with data rate-distance products beyond 100 Gb/s·m. However, imperfections of optical devices such as VCSEL and optical modulators emerge as bottlenecks for further improvements of the link speed and power efficiency. This thesis focuses on the silicon-based transmitter design for resolving those imperfections, to enhance the qualities of short-reach and long-haul optical fiber communications.

In the first part, a 56-Gb/s PAM-4 transmitter with piecewise compensation scheme in 40-nm CMOS is proposed to settle the non-idealities of VCSELs including electrical-to-optical (E/O) gain nonlinearity, E/O bandwidth nonlinearity and asymmetric responses to rising/falling transitions. A unary-based architecture with variable Gm-cells, 2-tap feed-forward equalizer (FFE), continuous-time linear equalizer (CTLE) and falling edge pre-emphasis is adopted to separately control the amplitudes, widths, and skews of three optical PAM-4 sub-eyes. Measurements at 56-Gb/s PAM-4 demonstrate that the proposed piecewise compensation scheme enhances the average sub-eye amplitude/width, ratio-of-level mismatch (RLM) and horizontal skew of the optical PAM-4 signal by 14%/12%, 38% and

63%, respectively. Fabricated in 40-nm CMOS, the transmitter achieves a de-embedded OMA of 1.18 mW and delivers an energy efficiency of 2.05 pJ/b at 56-Gb/s PAM-4.

In the second part, a 56-Gbaud half-rate linear transmitter in 130-nm SiGe BiCMOS is presented for optical modulators. The transmitter features an analog multiplexer with inherent feed-forward equalizer (AMUX-FFE) and a large-swing linear driver. The AMUX-FFE provides 2-to-1 analog serialization as well as 3-tap re-configurable FFE to boost the bandwidth of the E/O system. The linear driver adopts a dynamic triple-stacked topology where the bases of stacked transistors are dynamically biased according to the input signal, to achieve large output swing while avoiding breakdown issues. Measurements show that the output driver achieves a DC gain of 17 dB, a 3-dB bandwidth of 38 GHz, and a THD of 1.6% at 1-GHz 6-$V_{ppd}$ sinusoidal output, and the whole transmitter is capable of outputting 56-Gb/s 7.3-$V_{ppd}$ NRZ and 112-Gb/s 4.2-$V_{ppd}$ PAM-4 signals.

Finally, in the third part, a 100-Gbaud distributed linear driver with built-in 5-tap FFE in 130-nm SiGe BiCMOS is presented to further improve the data rate and equalization capability of optical modulator-based links. A distributed topology with cross-folded transmission line and cross-coupled Gm cells is proposed to simultaneously utilize transmission lines as inductance for parasitics compensation and delay elements for equalization. Measurements confirm that the proposed driver achieves a DC gain of 10 dB, a 3-dB bandwidth of >67 GHz, and a gain peaking of 6.9 dB at 50 GHz with the FFE turned on. The driver can support the generation of 100-Gb/s 4-$V_{ppd}$ NRZ signal and 160-Gb/s 3.8-$V_{ppd}$ PAM-4 signal with a RLM of 95.8%.

# CHAPTER I

## INTRODUCTION

### 1.1 Research Background

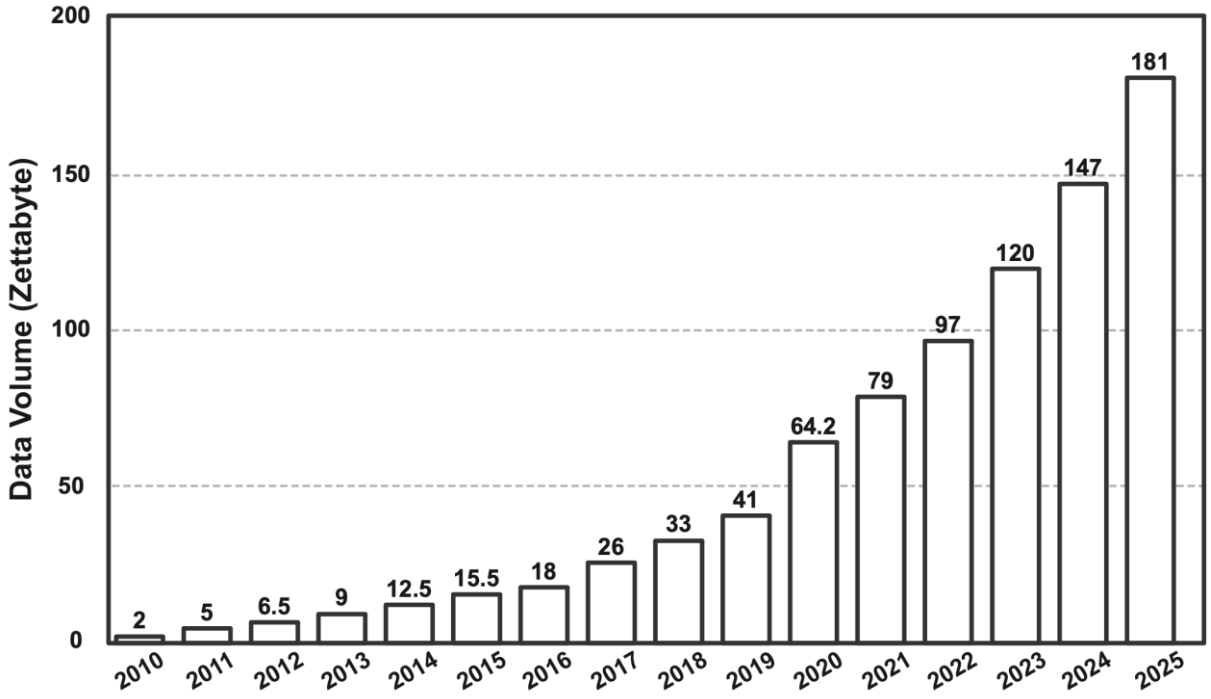


**Fig. 1.1 Volume of data/information created, captured, copied, and consumed worldwide from 2010 to 2025 [1].**

Leapfrog growth of artificial intelligence, cloud computing and big data technologies create explosive increase in data volume worldwide. As shown in Fig.1.1 [1], it is predicted that the data created, captured, copied, and consumed worldwide in 2025 will reach a precedent amount of 181 zettabytes. To support the transmission of those data, the 800-GbE Ethernet standard is being designed and expected to be deployed around 2025 to 2026 [2]. The communication infrastructures are being upgraded correspondingly towards higher data rate, higher power efficiency and lower latency.

Wireline interconnect acts as an indispensable role in modern communication

infrastructures. Different from wireless interconnects not requiring physical medium but with limited spectrum resources, each wireline interconnect has a dedicated physical medium to transmit and receive the data and hence can achieve broadband communications with a data rate much higher than typical wireless interconnects. Specific implementations of wireline interconnects vary with communication distance and data rate. Basically, they can be categorized into electrical links and optical links.

### 1.1.1 Comparison between Wireline Interconnects

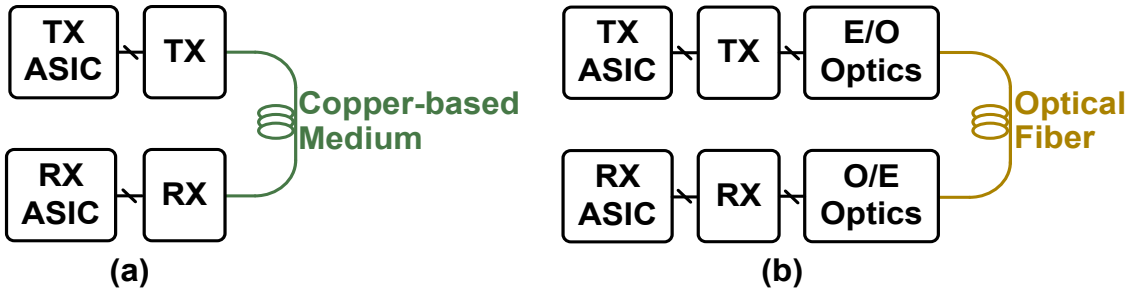


**Fig. 1.2 Simplified block diagrams of (a) an electrical link and (b) an optical link for wireline communications.**

Fig. 1.2(a) depicts the simplified block diagram of a typical electrical link. The transmitter (TX) is implemented to perform data serialization signal pre-distortion, and signal amplification, while the receiver (RX) is utilized to perform signal equalization, signal amplification, and data de-serialization. Copper-based materials such as twist pair and coaxial cable are adopted as the medium to connect the TX and RX. Electrical links have advantages of low power overhead, low hardware complexity, and low packaging cost. However, the limited bandwidths of copper-based medium restrict the application of electrical links within scenarios with data rate-distance products smaller than 100 Gb/s·m [3]. For the applications with the product beyond 100 Gb/s·m, optical links emerge as the mainstream. Fig. 1.2(b) shows the simplified block diagram of a typical optical link. Different from the electrical link, an electrical-to-optical (E/O) optical component is implemented following the TX to perform the electrical-to-optical signal conversion. Accordingly, an optical-to-electrical (O/E) optical

component is implemented preceding the RX to convert the optical signal back to electrical signal. Between the E/O and O/E optical components, an optical fiber is utilized as the transmission medium. Compared with copper-based mediums, optical fiber has advantages of high bandwidth and low loss, and hence it can be adopted for communications with longer distance and higher data rate. Further, depending on the wavelength of the used optical signal, optical links can be categorized into multi-mode and single-mode optical links.

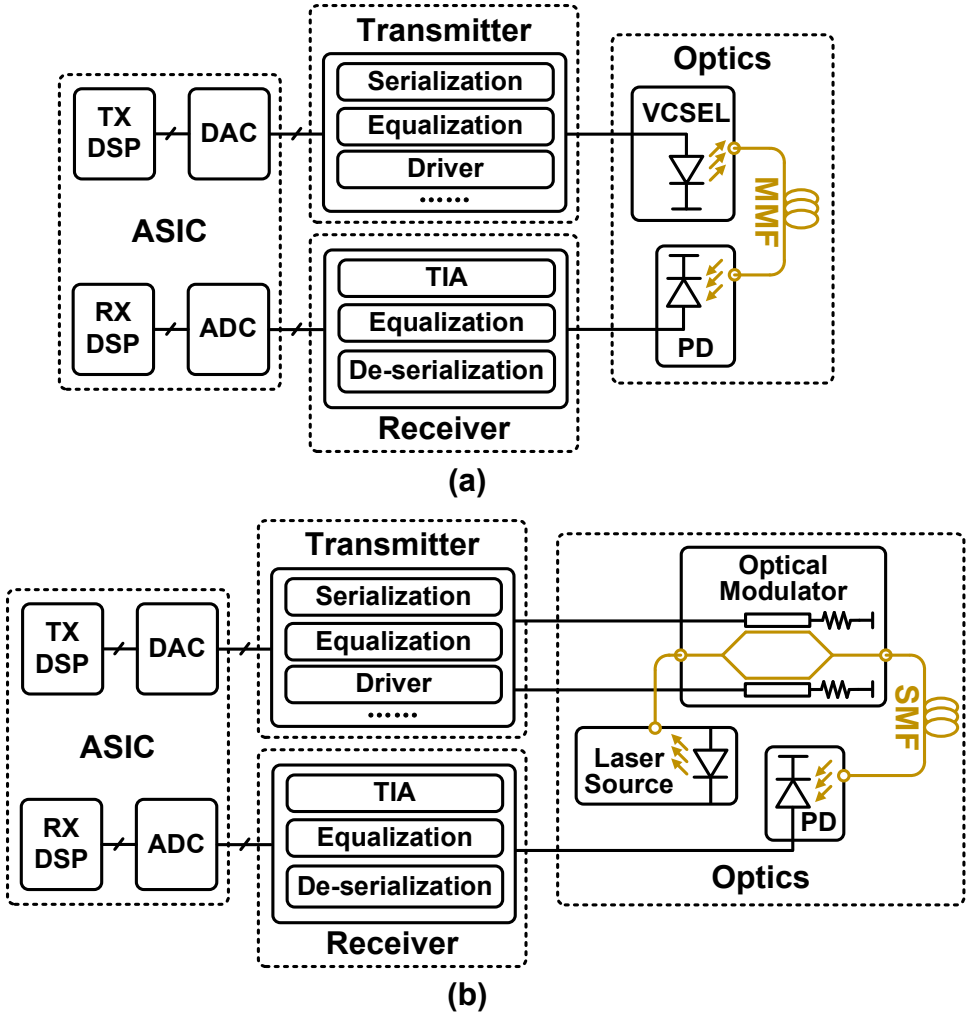


**Fig. 1.3 Simplified block diagrams of (a) a multi-mode optical link and (b) a single-mode optical link.**

Fig. 1.3(a) and Fig. 1.3(b) depict the simplified block diagram of the multi-mode and single-mode optical links, respectively. For the optical part, there are two main differences between the two types of links.

Firstly, the multi-mode optical link utilizes multi-mode fiber (MMF) as the transmission medium, while the single-mode optical link uses single-mode fiber (SMF) as the transmission medium. Compared with SMF, MMF has a larger core diameter and is more cost-effective. However, since MMF allows multiple spatial mode to propagate, it has a defect named modal dispersion which will distort the optical signal during propagation [4]. The modal dispersion will be severer with the increase of the fiber length. And therefore, multi-mode optical links are only used for medium-reach optical communications with distances ranging from tens of meters to hundreds of meters. In contrast, SMF allows solely one spatial mode to travel through. This feature makes it outperform MMF in terms of both dispersion and attenuation [5]. Therefore, single-mode optical links are widely adopted for long-haul optical communications with distances up to hundreds of kilometers.

Secondly, the E/O and O/E optics for the two links are different. At the transmitter side, multi-mode optical links typically use lasers such as light-emitting diode (LED) and vertical-cavity surface-emitting laser (VCSEL) for E/O conversion [6-8]. With the data rate of multi-mode optical links increasing to tens of gigabits per second nowadays, VCSEL has already replaced LED and become the major choice due to its merits of low cost, low power overhead and relatively high bandwidth [9]. For single-mode optical links, optical modulators such as Mach-Zehnder modulator (MZM) are widely adopted as the E/O optics [10-12]. Compared with optical signals which are directly modulated by the cavity of VCSEL, the optical signals modulated by the external optical modulators have purer spectrum and better tolerance to imperfections from long-length optical fibers [13]. However, as the optical modulators themselves cannot generate light, extra laser diodes are demanded to act as the optical source, and hence the implementation of E/O optics for single-mode optical links is typically more complicated and costly than that for multi-mode optical links. At the receiver side, the difference in the O/E optics between the two types of links is smaller than that in the E/O optics. Both multi-mode and single-mode optical links adopt photodetectors (PDs) for O/E signal conversion. But the optimal operation wavelengths of the PDs for the two types of

links are surely different.

Discrepancies in optical building blocks lead to different implementations of the electrical components. The biggest difference in the electrical part between the multi-mode and single-mode optical links are the implementations of the transmitter. For receivers, since both links adopt PD to perform O/E converter, their receivers achieve the same functions, including current-to-voltage conversion, amplification, equalization and de-serialization for the weak current signals generated by the PD. And hence, the implementations of the receiver for both links are similar. However, as the principles and characteristics of VCSEL and optical modulator are totally different, the implementations of the transmitter for multi-mode and single-mode optical links vary a lot. The design challenges for the VCSEL transmitter and optical modulator transmitter will be described in 1.1.2 and 1.1.3, respectively.

### 1.1.2 Design Challenges for the VCSEL Transmitter

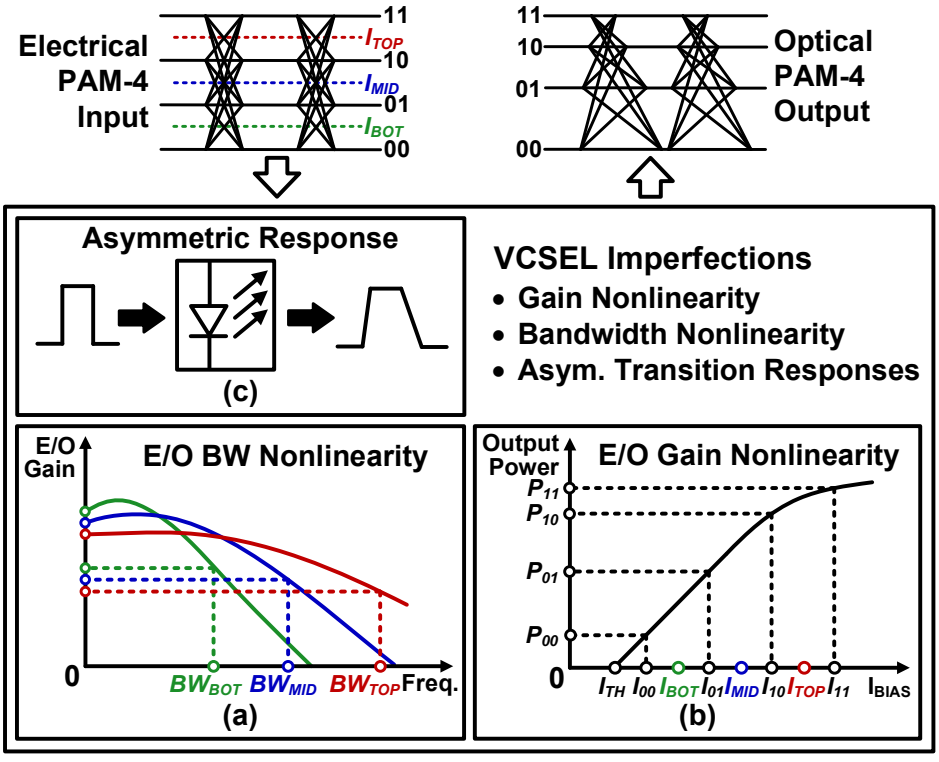


**Fig. 1.4 Imperfections of the VCSEL in E/O conversion gain, E/O conversion bandwidth and responses to rising and falling transitions.**

VCSEL requires a single-ended current signal input with swings of 5~10 mA. Therefore, in addition to providing serialization and equalization, the transmitter for multi-mode optical links is supposed to convert the signal from voltage mode to current mode before feeding the signal to VCSEL. Moreover, the biggest challenges for the VCSEL transmitter design are the non-idealities of the VCSEL, which will degrade the signal integrity during E/O conversion and limit the data rate of the optical link, as illustrated in Fig. 1.4.

Firstly, as shown in Fig. 1.4(a), the E/O conversion gain of VCSEL is nonlinear with the bias current [14]. With the increase of the bias current, the E/O conversion gain decreases. This non-ideality is negligible when using VCSEL for modulating non-return-to-zero (NRZ) signals which have only two levels and hence are not sensitive to non-linearity. However, for optical links using pulse amplitude modulation-4 (PAM-4) signals which have four possible levels in each symbol to improve the modulation efficiency, the non-linearity becomes issues. When the VCSEL transforms the top, middle, and bottom PAM-4 electrical sub-eyes, the bias currents for the VCSEL are $I_{TOP}$, $I_{MID}$, and $I_{BOT}$, respectively. For the electrical bottom sub-eye, VCSEL's E/O gain is the largest, as $I_{BOT}$ is the smallest compared with $I_{MID}$ and $I_{TOP}$. For the electrical top sub-eye, in contrast, VCSEL has the smallest E/O conversion gain. Consequently, the amplitude of the generated optical bottom sub-eye is the largest and that of the optical bottom sub-eye is the smallest.

Secondly, VCSEL's bandwidth is also nonlinear with respect to the bias current [15], as depicted in Fig. 14(b). The bandwidth of VCSEL increases with the increase of the bias current. For high-speed cases, the width of each PAM-4 sub eye is primarily determined by the bandwidth. If the bandwidth is inadequate, the data transitions will become slow, resulting in a small sub-eye width. Therefore, the bandwidth nonlinearity will induce the discrepancy between the widths of the three optical sub-eyes. As the top electrical sub-eye possesses the highest bandwidth, the width of the optical top sub-eye is the largest. On the contrary, since the electrical bottom sub-eye has the smallest bandwidth, the width of the optical bottom

sub-eye is the smallest.

The third non-ideality of the VCSEL is that its response to rising transitions is faster than that to falling transitions due to charge storage effect [16], as illustrated in Fig. 14(c). With the decrease of bias current and the increase of the signal data rate, this asymmetric response issue deteriorates further. Consequently, the optical eye diagram exhibits an obvious skew. The skew narrows the sampling window of the optical PAM-4 signal and complicates the implementation of the optical receiver.

To relieve the above three non-idealities, compensation circuits are highly demanded for VCSEL transmitters to enhance the optical signal integrity and increase the link speed. However, the compensations will be quite complicated, as both the E/O gain non-linearity and E/O bandwidth non-linearity are related to the bias condition of the VCSEL, while the asymmetric response issue is even relevant with not only the VCSEL bias but also the signal patterns. How to effectively compensate for those VCSEL non-idealities with low circuit complexity and low extra power overhead is one of the problems this thesis aims to solve.

### 1.1.3 Design Challenges for the Optical Modulator Transmitter

Different from VCSEL, optical modulators typical require voltage-mode driving signals. According to the working mechanism, optical modulators can be categorized into electro-absorption modulators and electro-refraction modulators [17].

In electro-absorption modulators (EAMs), the applied voltage signal will induce the variation of the absorption coefficient of the modulator. This effect enables the intensity modulation for the optical signal passing through the modulator. Fig. 1.5(a) shows the cross section of a surface-normal EAM as an example [18]. The light generated by the external optical source passes through the transparent substrate and arrives at the positive-intrinsic-negative (p-i-n) diode whose absorption coefficient changes with the applied

voltage signal. After being modulated, the light is then reflected and exits the EAM through the substrate. Fig. 1.5(b) shows the absorption characteristics of this EAM. Taking the wavelength of 1500 nm as an instance, with the applied electrical field increasing from 0 to 8.8 V/μm, the absorption coefficient of the modulator increases from around 250/cm to 1900/cm, resulting in a decreased optical intensity.

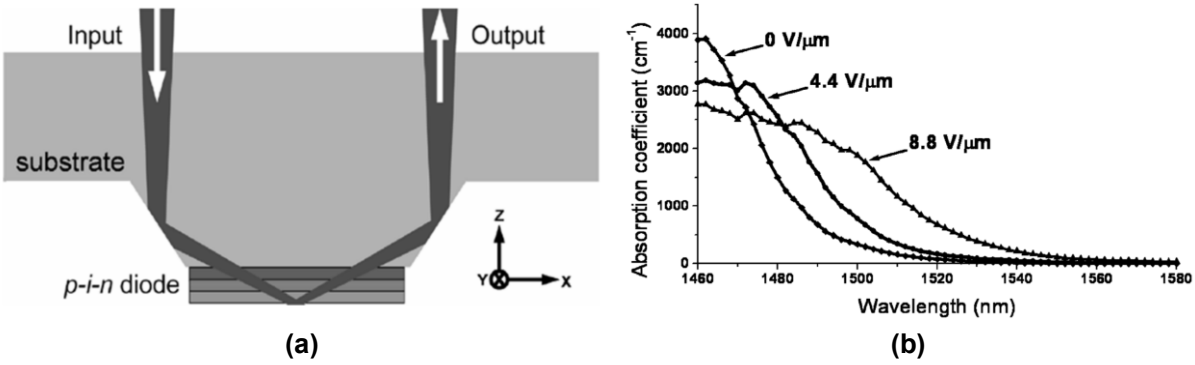


**Fig. 1.5 (a) Simplified cross section and (b) absorption characteristics versus wavelength and applied electrical field of a surface-normal EAM.**

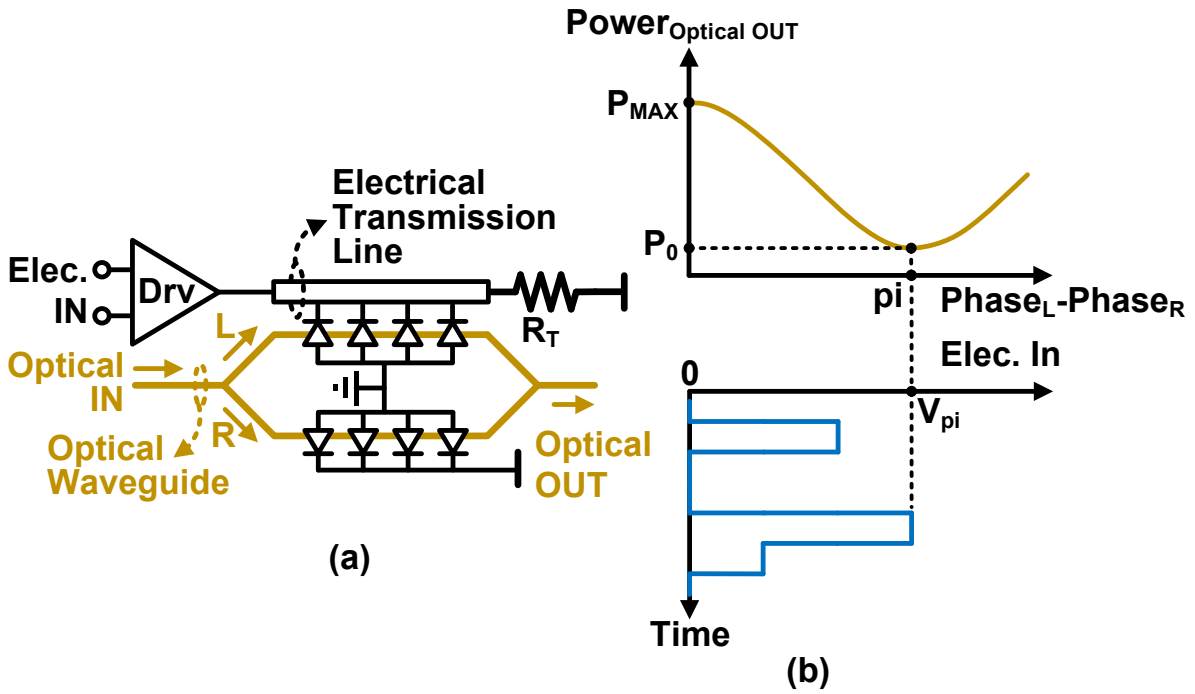


**Fig. 1.6 (a) Simplified structure and (b) E/O conversion characteristics of a single-drive traveling-wave MZM.**

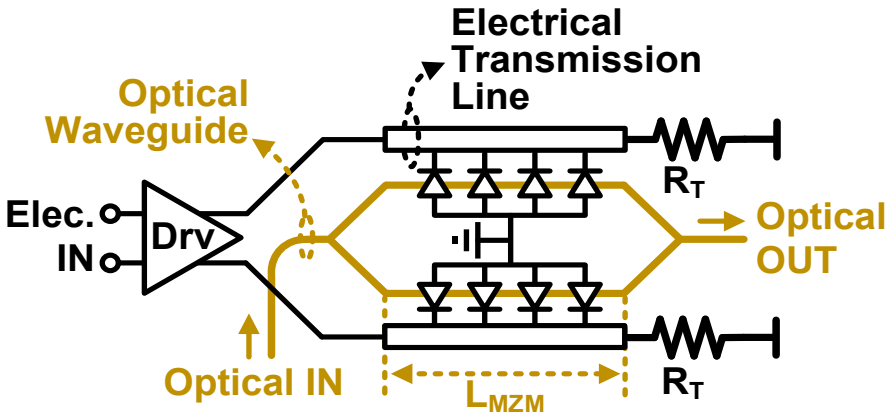


**Fig. 1.7 Simplified structure of a dual-drive traveling-wave MZM.**

In electro-refraction modulators such as MZM and micro-ring modulator (MRM), different from EAM, the E/O conversion relies on the variation of the refractive index. The application of the driving signal across the modulator will change the refractive index of the optical waveguide, and further inducing the phase shifting for the light passing through the modulator. To better illustrate how to use this phase shifting for optical intensity modulation, Fig. 1.6 presents the simplified structure and E/O conversion characteristics of a single-drive traveling-wave MZM. As depicted in Fig. 16(a), the MZM mainly consists of a pair of electrical transmission line made of metals, a terminated resistor ($R_T$), and optical waveguides which are typically made of lithium niobate [19], silicon [20], and indium phosphide [21]. The input light from the external optical source is split into two ways, which are sent to two arms of the MZM (L and R). The refractive index of the arm-L is modulated by the voltage signal from an electrical driver, while that of the arm-R remains static. Therefore, the phase of the light passing through arm-L denoted as $Phase_L$ will be different from that of the light passing through arm-R denoted as $Phase_R$. As illustrated in Fig. 1.6(b), when the applied voltage signal is zero, the power of the output light added by the two lights from the two arms will be the maximum ($P_{MAX}$), as the two lights are in-phase. $P_{MAX}$ will be a little bit smaller than the power of the input light due to the loss from the optical waveguide. On the other hand, when the applied voltage signal is as large as $V_{pi}$ which is the voltage value that shifts the phase of the light by $\pi$, the power of the output light will be the smallest ($P_0$), as the lights from the two arms are fully out-phase with each other. In this way, the E/O conversion is

achieved. In practice, the dual-drive traveling-wave MZM as shown in Fig. 1.7 is more widely adopted. Its two arms are driven by the differential outputs of the driver, and hence it can achieve a higher extinction ratio (ER). It is noted that the ER is defined as the ratio of the maximum and minimum optical powers. For example, the ER for the case of Fig. 1.6(b) is equal to $P_{MAX}/P_0$.

Although with different mechanisms, both electro-absorption and electro-refraction modulators demand transmitters capable of outputting large-swing voltage signal, to improve the ER of the modulated light and enhance the distance and quality of the communication. However, the requirement of large output swing leads to challenges of potential breakdown risks for the transistors and limited bandwidth due to large-size devices. Further, the ER can be improved by increasing the modulation length of the optical modulator, such as $L_{MZM}$ of the MZM shown in Fig. 1.7, which however will enlarge the size of the optical modulator with results of severe parasitics and then limit E/O conversion bandwidth further. Therefore, equalization is necessary inside the transmitter to boost the bandwidth of the E/O module. How to achieve a modulator transmitter simultaneously with large output swing, high bandwidth, equalization capability and without breakdown issue is another primary problem that this thesis focuses on.

## 1.2 Thesis Organization

This thesis is organized as follows:

Chapter I starts with a general introduction and comparison of the three mainstream wireline interconnects including electrical link, multi-mode optical link, and single mode link. Following that, non-idealities of the VCSEL and principles of the popular optical modulators including EAM and MZM are described. And design challenges of the VCSEL transmitter and the optical modulator transmitter, which are the primary motivations for the research work of this thesis, are illustrated.

Chapter II describes the first contribution of this thesis, which is a 56-Gb/s complementary metal-oxide semiconductor (CMOS) PAM-4 transmitter with a piecewise compensation scheme for VCSELs. This chapter begins with a comprehensive literature review on existing techniques for mitigating VCSELs' non-idealities. After that, the compensation mechanism, architecture design, circuit implementations of main building blocks, setups for electrical and optical measurements, as well as the electrical and optical measurement results of the proposed VCSEL are introduced.

Chapter III focuses on the second work of this thesis, which is a 56-Gbaud 7.3-$V_{ppd}$ linear modulator transmitter in 130-nm silicon-germanium (SiGe) BiCMOS process. This chapter covers the literature review on existing linear transmitters, architecture design of the proposed transmitter, circuit implementations of main building blocks including the analog multiplexer-feed-forward equalizer (AMUX-FFE) and dynamic triple-stacked driver, and measurement setups and results of the proposed transmitter.

Chapter IV introduces the third outcome of this thesis, which is a 100-Gbaud 4-$V_{ppd}$ distributed linear driver with 5-tap FFE in 130-nm SiGe BiCMOS also for optical modulators. Architecture design evolution, implementations of the proposed cross-folded transmission and cross-coupled Gm cell, frequency- and time-domain measurement setup and results are covered in this chapter.

Finally, Chapter V summarizes the outcomes of this thesis and gives prospects for future extended research.

# CHAPTER II

## 56-Gb/s PAM-4 CMOS VCSEL Transmitter Design

### 2.1 Introduction

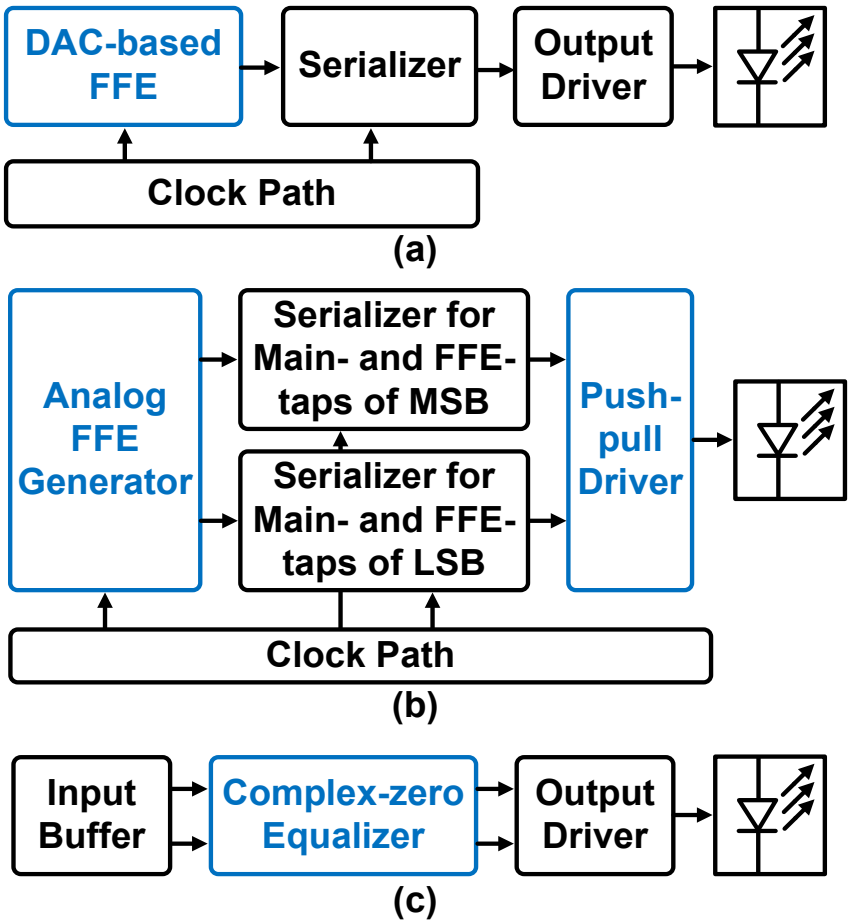


**Fig. 2.1 Simplified block diagrams of (a) VCSEL transmitter with DAC-based FFE, (b) VCSEL transmitter with push-pull driver-based asymmetric analog FFE, and (c) VCSEL transmitter with complex-zero equalizer.**

As illustrated in section 1.1.2, the non-idealities of VCSELs including E/O bandwidth nonlinearity, E/O gain nonlinearity, and asymmetric rising/falling responses are the main issues hindering the speed improvement of VCSEL-based multi-mode links, especially when PAM-4 emerges as the mainstream modulation scheme and the single-channel speed evolves to more than 50Gb/s.

To counteract those non-idealities, several compensation techniques have been proposed in recent years. [14] introduces a compressor into the VCSEL driver to pre-distort the PAM-4 electrical signal. By deliberately making the amplitudes of three electrical PAM-4 sub-eyes inequal, the compressor could well compensate for the E/O gain nonlinearity. But the E/O bandwidth nonlinearity and asymmetric response issue are not settled. [15] proposes a NRZ VCSEL driver with an edge detector-based asymmetric equalization scheme to separately equalize the rising and falling data transitions. [16] presents a pre-emphasis technique to speed up the falling data transition. Both [15] and [16] can handle the asymmetric response issue well. However, since they are all designed for NRZ signals, the E/O gain and bandwidth nonlinearities, which emerge as issues for PAM-4 VCSEL transmitters, are not resolved. [22] and [23] implement digital-to-analog converter (DAC)-based nonlinear feed-forward equalizers (FFEs), as shown in Fig. 2.1(a), to finely control the 16 possible transitions of PAM-4 signals, thereby compensating for VCSEL non-idealities. The effectiveness of this technique has been well verified by optical measurements. However, the digital method increases the link latency and power consumption and incurs significant die area overheads due to the required lookup tables and digital multiplexers (MUXs). Such method is more suitable for long-haul optical communications where multiple FFE taps are demanded to compensate for the imperfections of not only optical devices but also long optical fibers. [24] and [25] utilize a push-pull topology for the VCSEL driver to resolve non-idealities, as depicted in Fig. 2.1(b). By independently controlling the currents flowing through the push and pull transistors, an asymmetric pre-emphasis scheme is achieved. Nevertheless, these drivers are embedded in least-significant bit (LSB) and most-significant bit (MSB)-based transmitters. Since both the top and bottom PAM-4 sub-eyes are determined by the LSB data path, the E/O gain and bandwidth nonlinearities cannot be fully resolved. Some works compensate the VCSEL non-idealities from a frequency-domain perspective. Fig. 2.1(c) illustrates a complex-zero equalizer-based VCSEL transmitter proposed by [26]. A two-path filter is implemented to counteract the complex conjugate poles in the VCSEL frequency response. Building on this, [27] presents a complex-zero continuous-time linear equalizer

(CTLE) that introduces an inductor into the degenerated resistor-capacitor (R-C) network, further minimizing the in-band gain and group delay distortion and improving the overall bandwidth. However, both complex-zero equalizers have been demonstrated with NRZ cases. As the frequency characteristic of PAM-4 is much more complex than that of NRZ, extending the complex-zero method to PAM-4 can be complicated and costly.

To fully overcome the VCSEL non-idealities and relieve the overhead of compensation circuits, this work proposes a PAM-4 VCSEL transmitter with a piecewise compensation scheme [28]. The three PAM-4 sub eyes are decoupled by a binary-to-unary encoder and separately processed by three data slices with independently adjustable transconductance (Gm) cell, 2-tap FFE, CTLE and pre-emphasis. The data streams from the three slices are re-combined at the transmitter output into pre-distorted electrical PAM-4 signal, with which the VCSEL can generate low-distortion optical PAM-4 signals to improve the communication quality. As a mixed-signal method, the proposed piecewise compensation scheme could achieve full compensation for the VCSEL non-idealities, while posing small impacts on power consumption and die area.

This chapter is organized as follows. The compensation mechanism and architecture design of the proposed VCSEL transmitter is introduced in section 2.2. Section 2.3 presents circuit implementations of main building blocks including 4-to-1 MUX, clock tree, and output stage. Section 2.4 introduces the measurement setup and results. Finally, the conclusion of this article is drawn at Section 2.5.

## 2.2 Architecture Design

Figure 2.2 illustrates the conceptual block diagram of the proposed PAM-4 transmitter, which implements a piecewise compensation scheme for VCSEL non-idealities. A binary-to-unary encoder transforms input LSB and MSB data streams into three unary data streams $D_B$, $D_M$, and $D_T$, which are then processed by the top, middle, and bottom data slices,

respectively. The processed unary streams $D_{BP}$, $D_{MP}$, and $D_{TP}$ are 'stacked' at the transmitter output node into pre-distorted PAM-4 signals and then delivered to the off-chip VCSEL.

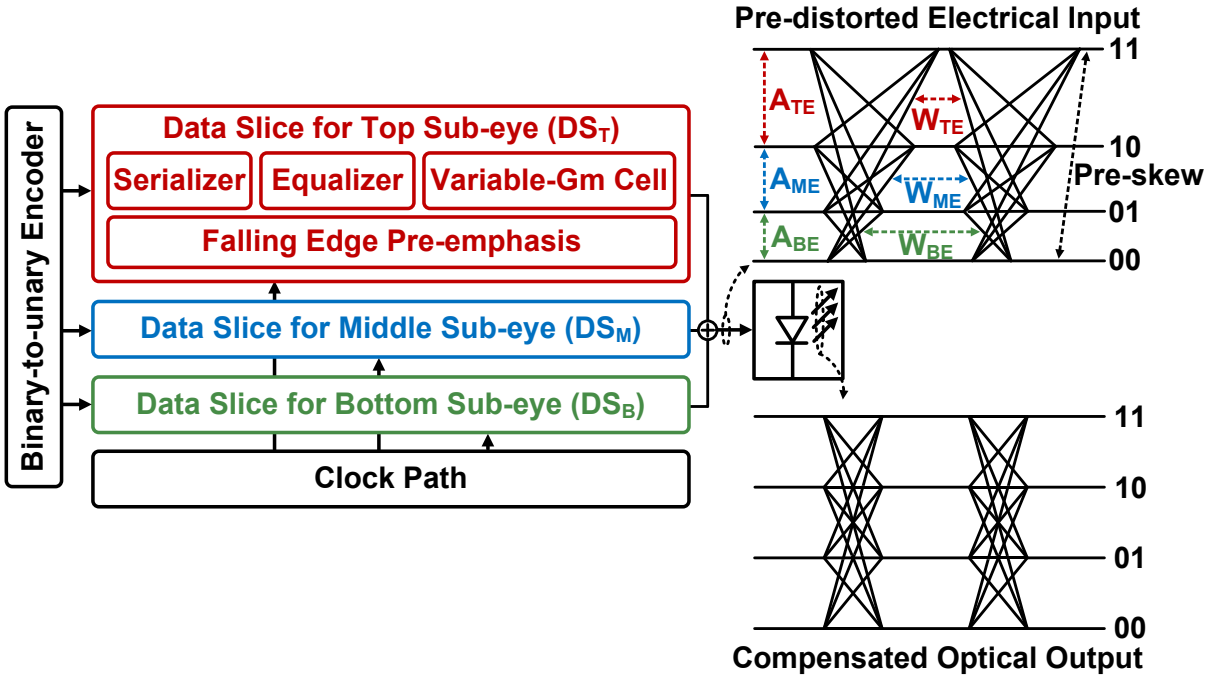


**Fig. 2.2 Conceptual block diagram of the proposed PAM-4 VCSEL Transmitter based on a piecewise compensation scheme.**

According to the relationship between binary and unary codes, the amplitudes of bottom, middle and top sub-eyes of the optical PAM-4 output are primarily determined by gains of bottom, middle, and top data slices, respectively. As introduced in section I, due to the gain nonlinearity, the E/O conversion gain of the middle sub-eye is smaller than that of bottom sub-eye and larger than that of top sub-eye. To compensate for this, the gain of middle slice should be adjusted to be larger than that of bottom slice and smaller than that of top slice.

The compensation of bandwidth nonlinearity adopts the same manner. The widths of bottom, middle and top sub-eyes of the optical PAM-4 output mostly depends on the bandwidth of bottom, middle, and top slices, respectively. By controlling the equalization characteristics of the three slices, their bandwidths can be tuned. As the E/O conversion bandwidth of middle sub-eye is larger than that of bottom sub-eye and smaller than that of top

sub-eye, the equalization strength of middle slice should be adjusted to be weaker than that of bottom sub-eye and stronger than that of top sub-eye, to compensate for the bandwidth nonlinearity.

Furthermore, a pre-emphasis circuit is implemented in the three data slices to boost the falling transitions of $D_{BP}$, $D_{MP}$, and $D_{TP}$. As described in section I, a low bias current will aggravate the asymmetric response issue. Therefore, the pre-emphasis strength for middle slice should be weaker than that of bottom slice and stronger than that of top slice. By this means, the electrical PAM-4 output can be pre-skewed also in a piecewise manner, and the asymmetric response issue can be counteracted.

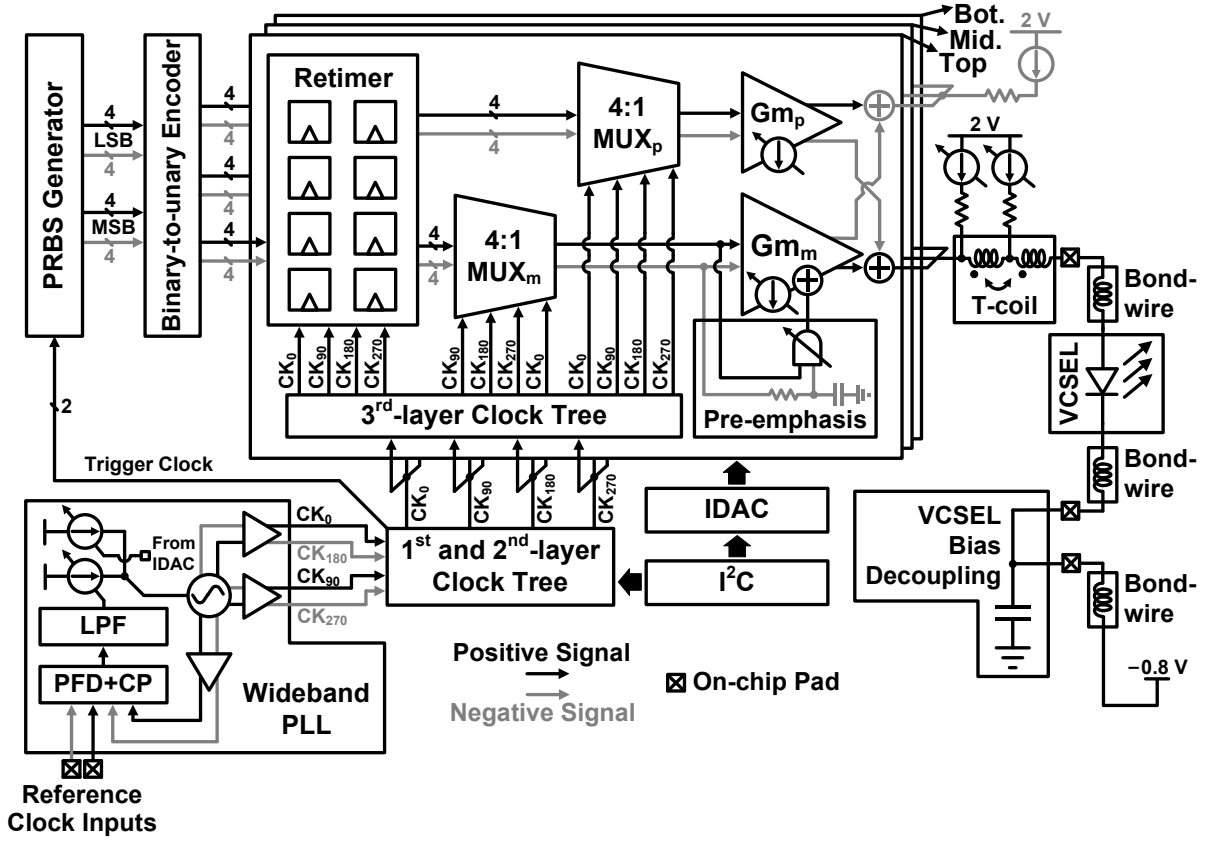


**Fig. 2.3 Detailed block diagram of the proposed PAM-4 VCSEL transmitter.**

To validate the above compensation techniques, a quarter-rate PAM-4 transmitter prototype is implemented. Fig. 2.3 depicts the block diagram of the transmitter, mainly

comprising a data path and a clock path.

At the data path, an on-chip pseudo-random binary sequence (PRBS) generator is implemented to facilitate measurements, producing 4 LSB and 4 MSB quarter-rate data streams. They are then transformed by a binary-to-unary encoder into 12 unary quarter-rate data streams, which are fed to top, middle, and bottom data slices. In each data slice, quarter-rate data inputs are re-timed by a latch-based re-timer. To implement a 2-tap analog FFE, the re-timer produces two data bundles. The timing of the data bundle for the pre-tap path is 1/4 UI ahead of that for the main-tap path. To guarantee correct serialization, the clocking for $MUX_p$ at the pre-tap path is 90 degrees ahead of that for $MUX_m$ at the main-tap path. Therefore, the full-rate data streams of the pre-tap path is 1 UI ahead of that of main-tap path. In this way, a 2-tap FFE with an initial tap spacing of 1 UI is achieved. The timing between these 2 taps can be further adjusted by controllable delay cells (CDCs) at the third-layer clock tree to tune the FFE peaking frequency [29]. The strength of the FFE is adjusted by tuning the transconductances of the Gm cells following 4-to-1 MUXs. Apart from functioning as a variable transconductance amplifier, the Gm cell at the main-tap path ($Gm_m$) integrates a degenerated R-C network to achieve the function of CTLE. Furthermore, a pre-emphasis circuit is integrated with $Gm_m$ to sense falling transitions of the data stream and generate boosting pulses which are added to the output of $Gm_m$. The data streams from top, middle, and bottom slices are combined at the transmitter output node into a pre-distorted PAM-4 current signal and applied to the VCSEL via an on-chip T-coil.

At the clock path, a wideband ring oscillator-based phase-locked loop (PLL) [30] is implemented on-chip to generate 4-phase clock signals. The clock signals are then duplicated and buffered by a 3-layer clock tree. Inside the clock tree, multiple CDCs are implemented to increase the driving capability of clock signals and the delays of clock signals to ensure correct timing of the whole transmitter. The outputs of the 3-layer clock tree are eventually delivered to re-timers and 4-to-1 MUXs for serialization operations.

Overall, in the proposed transmitter, the E/O bandwidths for each PAM-4 sub-eye are regulated by configuring characteristics of the 2-tap FFE and CTLE inside each data slice. The E/O gains for each PAM-4 sub-eye are adjusted through the main-tap Gm cells. And the falling transitions of each PAM-4 sub-eye are controlled by the pre-emphasis circuits. These adjustments are piecewise leveraging the unary code- based transmitter architecture, and thus the VCSEL non-idealities can be effectively mitigated.

## 2.3 Circuit Implementations

### 2.3.1 4-to-1 MUX

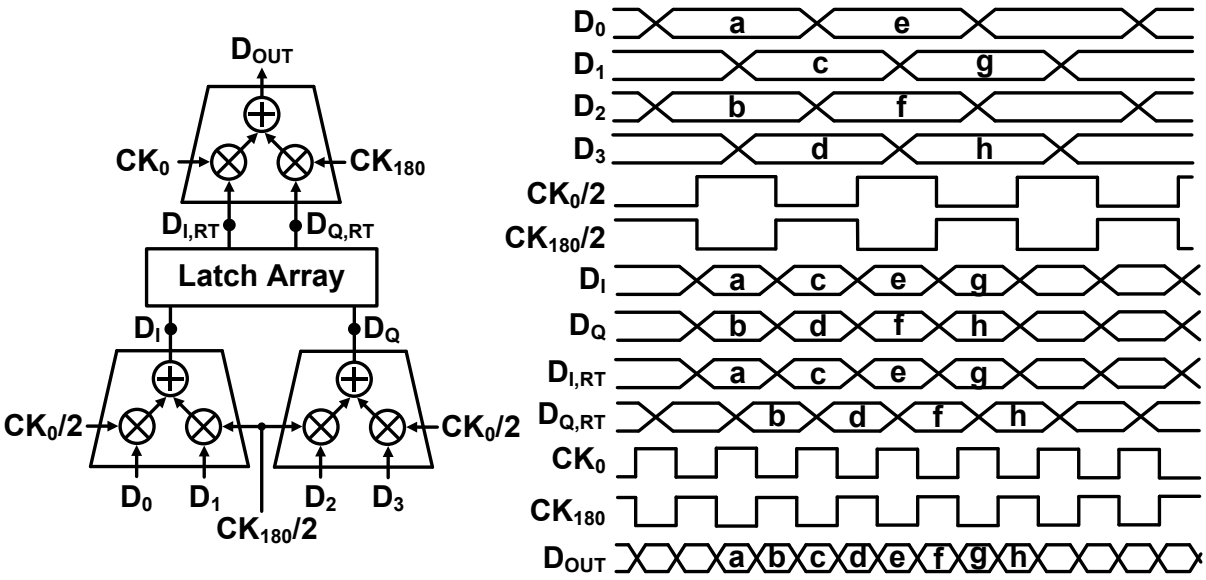


**Fig. 2.4 Structure and timing diagram of the conventional cascaded 2-to-1 MUXs-based 4-to-1 MUX.**

4-to-1 MUX is one of the most significant building blocks for quarter-rate transmitters to serialize the four quarter-rate data streams into one full-rate data stream. The design of the 4-to-1 MUX should be careful to reduce the signal distortion during serialization. Fig. 2.4 shows the structure and timing diagram of a conventional 4-to-1 MUX based on cascaded 2-to-1 MUXs [31], [32], [33]. After re-timed by the preceding re-timer, the input quarter-rate

data streams $D_0$~$D_3$ are serialized by the first-stage 2-to-1 MUX into half-rate data streams $D_I$ and $D_Q$, which are then re-timed by a latch array into $D_{I,RT}$ and $D_{Q,RT}$. The second stage further serializes $D_{I,RT}$ and $D_{Q,RT}$ into full-rate data stream $D_{OUT}$. However, in this implementation, the second-stage 2-to-1 MUX demands a clock frequency doubling that for the first-stage 2-to-1 MUX. And thus, for example, a clock frequency as high as 14 GHz is needed for the 28-Gbaud operation, burdening the design of the clock path.

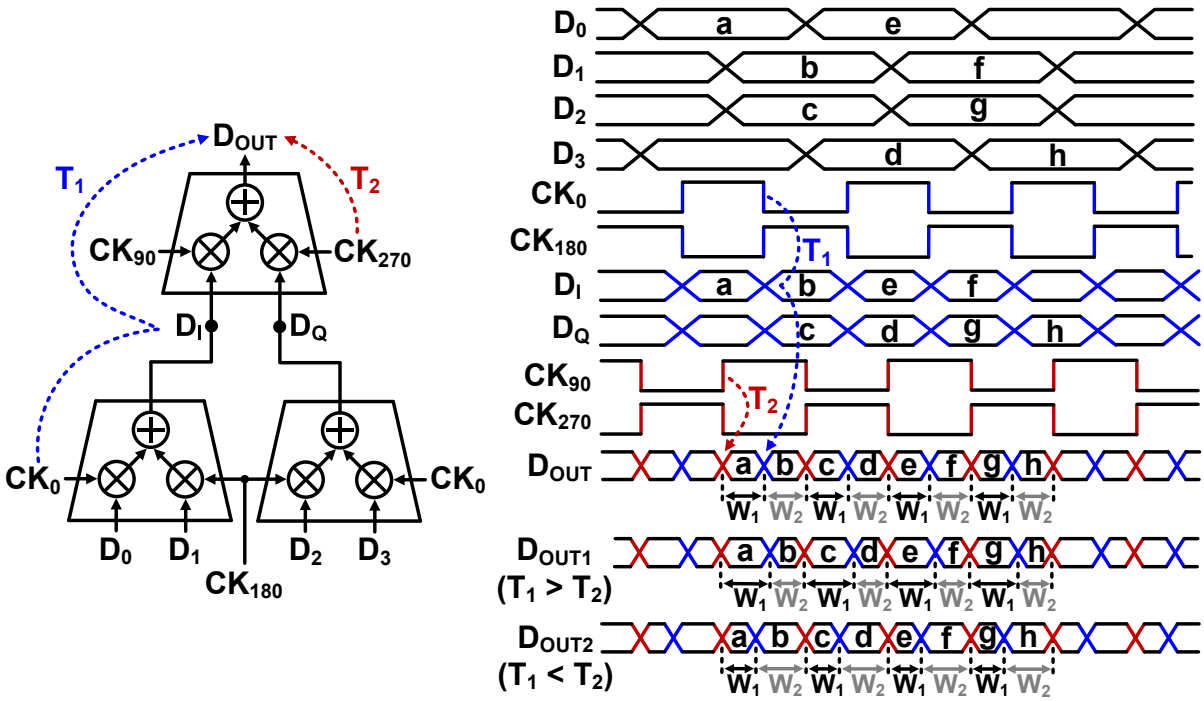


**Fig. 2.5 Structure and timing diagram of the proposed cascaded 2-to-1 MUXs-based 4-to-1 MUX.**

To reduce the highest clock frequency, this work proposes a 4-to-1 MUX with an optimized sampling scheme using four-phase clock signals $CK_0$, $CK_{90}$, $CK_{180}$, and $CK_{270}$. Fig. 2.5 presents the structure and timing diagram of the proposed MUX. During the first-stage serialization, high levels of $CK_0$ sample $D_0$ and $D_3$ to $D_I$ and $D_Q$, respectively, and high levels of $CK_{180}$ sample $D_1$ and $D_2$ to $D_I$ and $D_Q$, respectively. During the second-stage serialization, transition crossovers of $D_I$ and $D_Q$ are sampled to $D_{OUT}$ by high levels of $CK_{90}$ and $CK_{270}$, respectively. Leveraging the crossover sampling scheme during the second-stage serialization,

the proposed 4-to-1 MUX only needs single-frequency clock signals, with the highest clock frequency reduced by half compared to the conventional implementation. And thus, the bandwidth requirement for the clock path can be relieved.

However, in the transition crossover sampling scheme, there exists a duty-cycle distortion (DCD) issue for the full-rate data output, which relates to the difference between the delay $T_1$ from $CK_0$ ($CK_{180}$) to the output node and the delay $T_2$ from $CK_{90}$ ($CK_{270}$) to the output node. As illustrated by the timing diagram shown in Fig. 2.5, half of transitions (in red) of $D_{OUT}$ are determined by $CK_{90}$ and $CK_{270}$, while the rest half (in blue) are determined by $CK_0$ and $CK_{180}$. Ideally, as the phase difference between $CK_0$ ($CK_{180}$) and $CK_{90}$ ($CK_{270}$) is 90°, when $T_1$ is equal to $T_2$, $D_{OUT}$ would have a uniform bit width of 1 UI. However, in practical scenarios, $T_1$ can be different from $T_2$ owing to different clock-to-output paths. When $T_1$ is larger than $T_2$, $W_1$ will be larger than $W_2$, as illustrated by $D_{OUT1}$. Inversely, $W_1$ will be smaller than $W_2$ when $T_1$ is smaller than $T_2$, as illustrated by $D_{OUT2}$. This imperfection incurs severe DCD, resulting in degraded effective eye width which is determined by the narrowest eye.

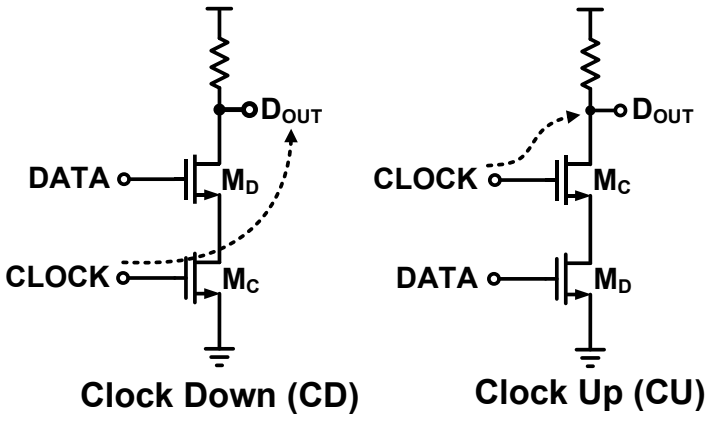


**Fig. 2.6 Two possible topologies for 2-to-1 MUX.**

To settle the DCD issue, transistor-level implementations for the MUX are investigated in this work. For the 2-to-1 MUX, there are two possible topologies shown in Fig. 2.6. The first topology named Clock Down (CD) stacks the data-controlled transistor $M_D$ above the clock-controlled transistor $M_C$, while the positions of $M_D$ and $M_C$ are reversed for the second

topology named Clock Up (CU). Further, when cascading two stages of 2-to-1 MUXs to form a 4-to-1 MUX, there will be four possible topologies, as listed in Fig. 2.7(a)~(d). For the CD-CU topology, $CK_0$ passes four transistors to reach the output node, while $CK_{90}$ only passes one transistor. As a result, $T_1$ is much longer than $T_2$. For the CU-CU topology, $T_1$ becomes closer to $T_2$, as $CK_0$ passes three transistors to the output node while $CK_{90}$ still passes one. For the CD-CD topology, the difference between $T_1$ and $T_2$ is further reduced, as $CK_0$ and $CK_{90}$ pass three and two transistors, respectively. Finally, for the CU-CD topology, both $CK_0$ and $CK_{90}$ pass two transistors to reach the output node, achieving the smallest difference between $T_1$ and $T_2$, and thus the DCD issue for this topology is slightest. The above analysis is verified by corresponding transient simulation results of those topologies, which demonstrate that $W_2$-$W_1$ ($\Delta W$) for the CU-CD topology is smallest among the four topologies. And thus CU-CD topology is selected in this work to achieve the 4-to-1 MUX. The residual $\Delta W$ can be mitigated by delaying $CK_{90}/CK_{270}$, to make the phase lagging of $CK_{90}/CK_{270}$ with respect to $CK_0/CK_{180}$ larger than 90°, as shown in Fig. 2.8. This can be achieved by controllable delay cells (CDCs) in the clock tree, which will be illustrated in section 2.2.2.

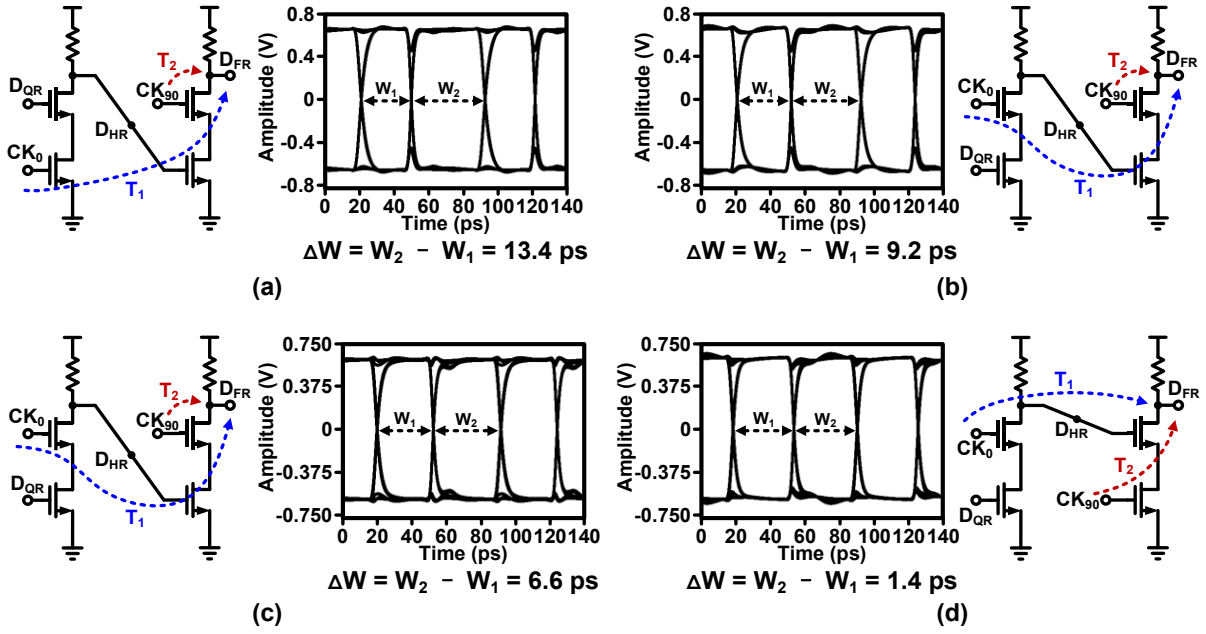


**Fig. 2.7 Simplified schematics and transient simulation results of (a) CD-CU topology, (b) CU-CU topology, (c) CD-CD topology, and (d) CU-CD topology.**

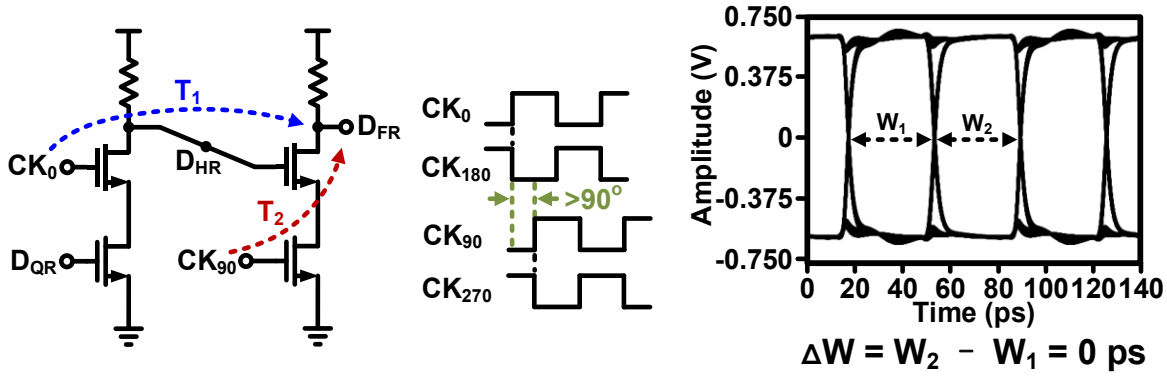


**Fig. 2.8 Enhanced CU-CD topology and its transient simulation result after clock calibration.**

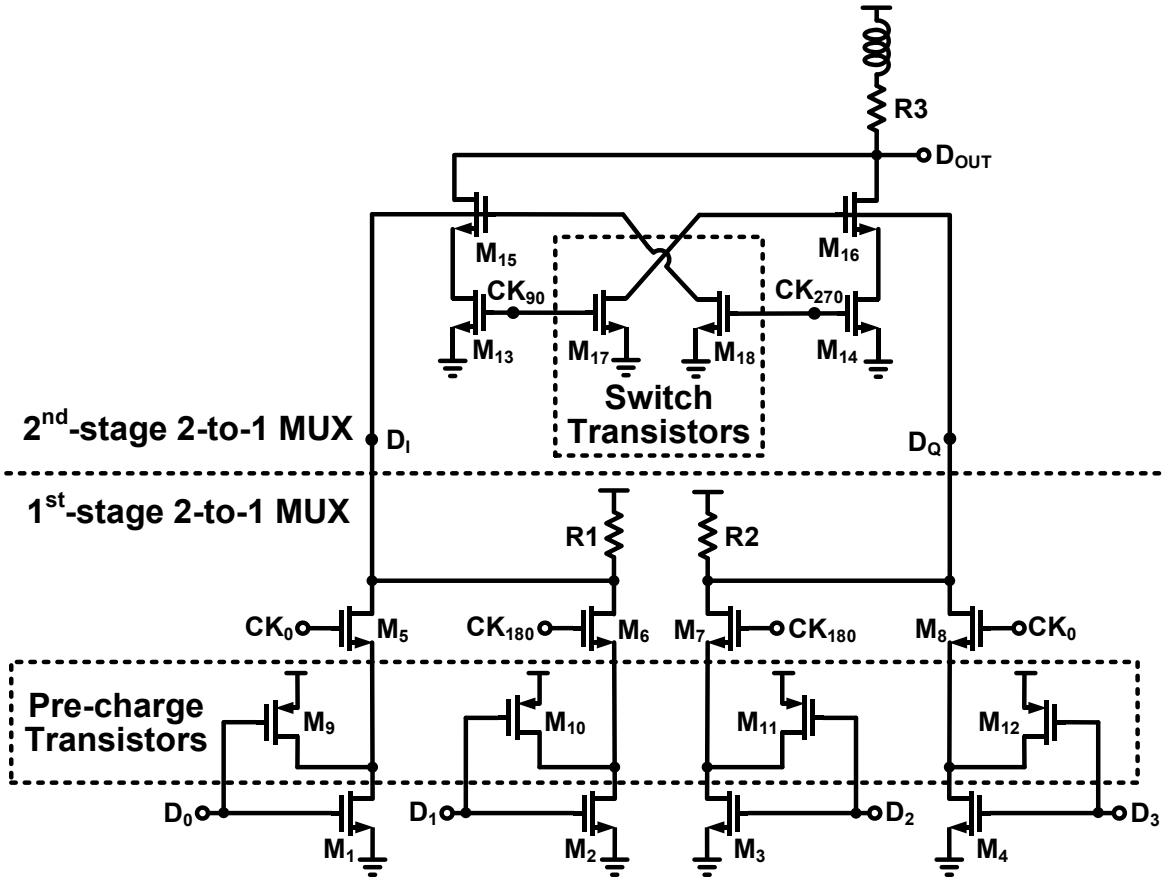


**Fig. 2.9 Half circuit of the proposed 4-to-1 MUX.**

The half circuit of the proposed CU-CD topology-based 4-to-1 MUX is shown in Fig. 2.9. In the first-stage 2-to-1 MUX, $M_1$~$M_4$ function as data-controlled transistors, and $M_5$~$M_8$ are controlled by clocks. $M_9$~$M_{12}$ are introduced as pre-charge transistors to relieve the charge-sharing effect of the CU topology [34]. In the second-stage 2-to-1 MUX, $M_{15}$ and $M_{16}$

are driven by the half-rate data streams $D_I$ and $D_Q$, respectively. However, as drains of $M_{15}$ and $M_{16}$ are directly connected to the output node, there is pattern-dependent jitter at $D_{OUT}$. For example, when $CK_{90}$ is low, the branch formed by $M_{15}$ and $M_{13}$ is turned off. At this time, the data transition of $D_I$ can still be coupled to $D_{OUT}$ through gate-drain parasitic capacitance of $M_{15}$. To relieve the issue, switch transistors $M_{17}$~$M_{18}$ are introduced. $M_{18}$ pulls down the gate of $M_{15}$ to ground when $CK_{90}$/$CK_{270}$ are low/high, and $M_{17}$ pulls down the gate of $M_{16}$ when $CK_{90}$/$CK_{270}$ are high/low. By this means, the pattern-dependent jitter can be suppressed. The sizes of $M_{17}$~$M_{18}$ should be small to reduce the extra power overhead.

### 2.3.2 Clock Tree

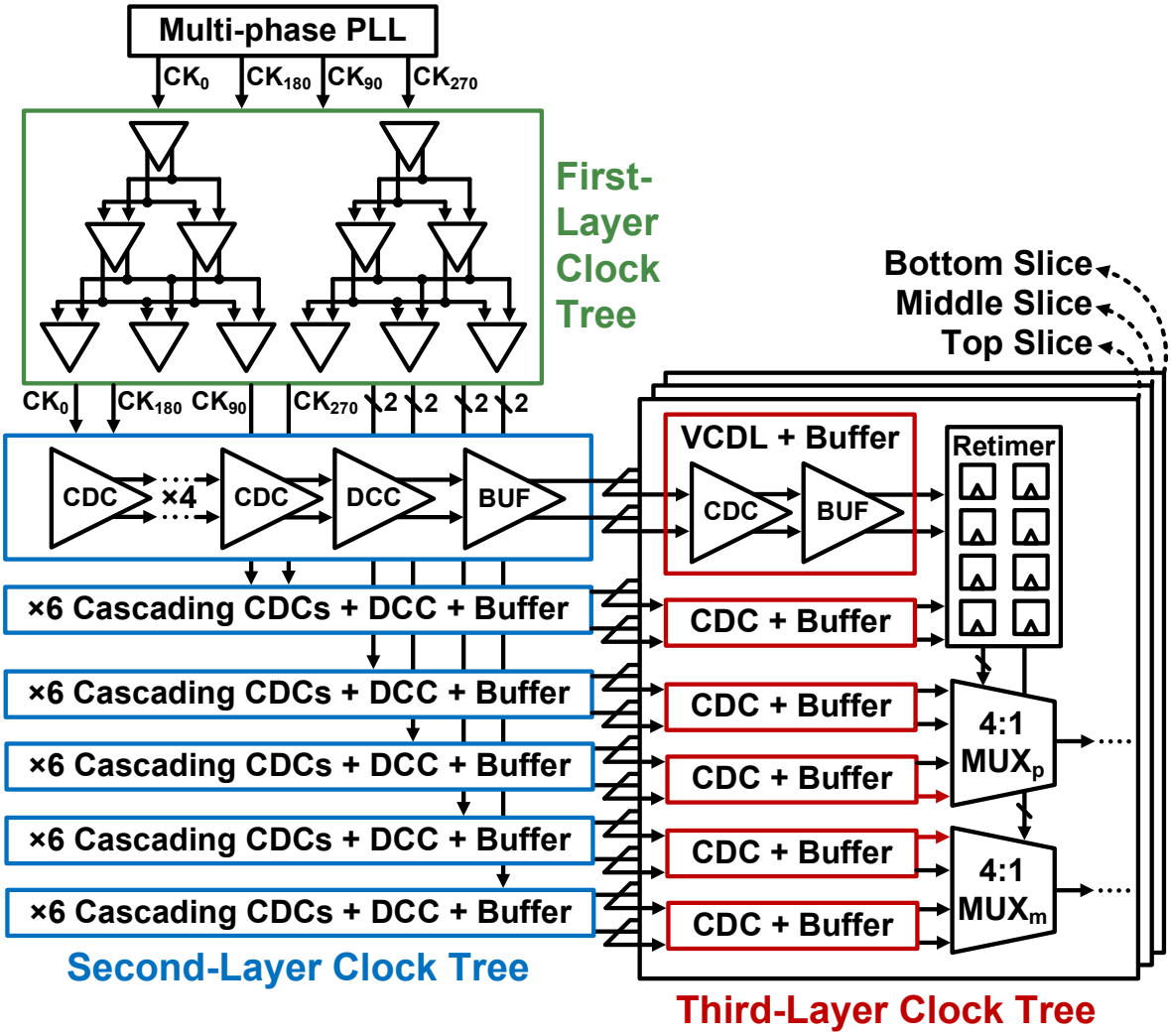


**Fig. 2.10 Architecture of the clock tree.**

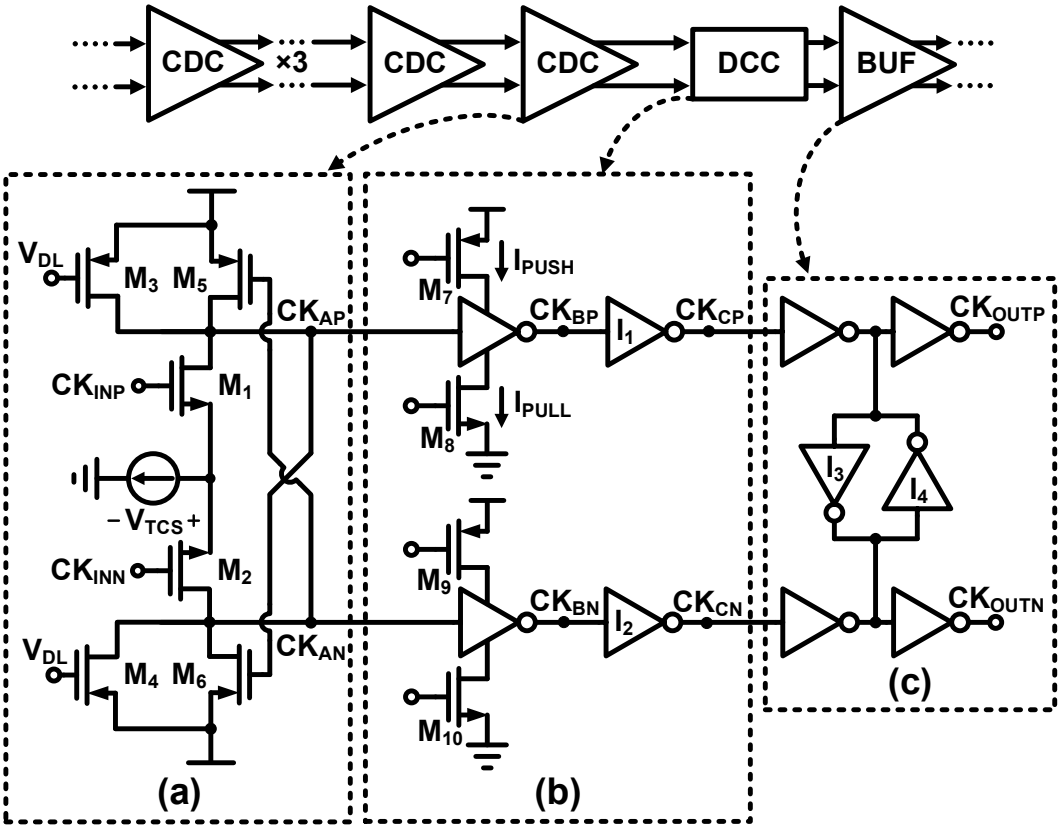


**Fig. 2.11 Circuits of the CDC, DCC and clock buffer.**

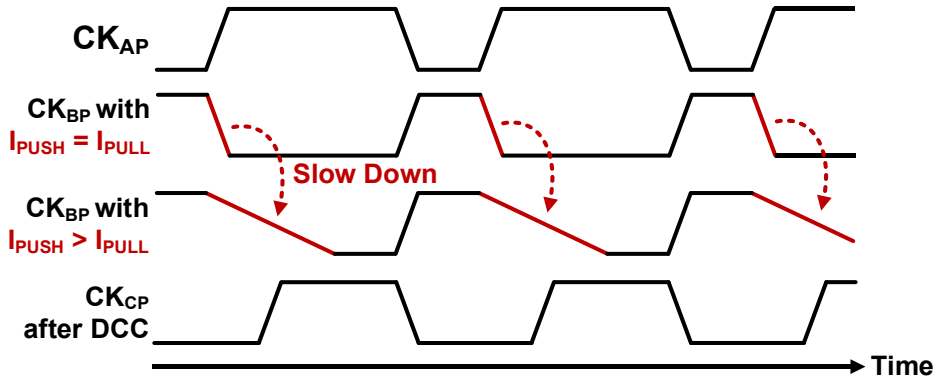


**Fig. 2.12 Principle of duty cycle correction.**

The clock tree is of high significance to distribute the clock signals from the on-chip PLL to clock-driven building blocks with high accuracy and low distortion. Fig. 2.9 describes the architecture of the proposed clock tree, which consists of three layers. The multi-phase PLL generates four-phase clock signals including $CK_0$, $CK_{90}$, $CK_{180}$, and $CK_{270}$. The phase discrepancies between the adjacent clock signals such as CK0 and CK90 are 90 degrees. Fed by the PLL, the first layer incorporating multiple inverter-based buffers is implemented to

duplicate this four-phase clock bundle into three same bundles. After that, the second layer adjusts the timing of the three clock bundles to synchronize the operations of the top, middle, and bottom data slices, as well as suppressing the signal distortions. The third layer mitigates residual timing skew between the three data slices owing to possible layout mismatch.

Among the three clock layers, the second layer plays the most important role in timing adjustment and clock quality enhancement. As depicted in Fig. 2.10, this layer includes 6 identical branches, among which 2 for retimers, 2 for pre-tap 4-to-1 MUXs ($MUX_p$) and 2 for main-tap 4-to-1 MUXs ($MUX_m$). To provide a large delay tuning range, each branch starts with 6 cascaded CDCs. Basically, the delay of CDC can be adjusted by changing the time constant of the signal path. [35] proposes a CDC which tunes delay by adjusting the varactor at the output node. However, a large varactor is needed to get a large delay tuning range, and thus the cell is not suitable for high-density implementation inside a clock tree. In this work, a compact CDC composed solely of transistors is utilized. The delay adjustment is provided by tuning the resistance at the signal path instead of capacitance. Fig. 2.11(a) shows the implementation of the proposed CDC. Differential transistors $M_1$ and $M_2$ receive the input clock signals. $M_3$ and $M_4$ function as variable loading resistors for $M_1$ and $M_2$, respectively. By controlling the gate voltage of $M_3$ and $M_4$, the time constant of the CDC output node varies, and the phase of output clock signal changes accordingly. However, the amplitude of the output clock signal will also change with different loading resistance. As a result, if the gain of the CDC is designed to be lower than 0 dB for low power consumption, the clock signal will diminish stage-by-stage along the long CDC link. To solve the issue, a cross-coupled transistor pair $M_5$ and $M_6$ are introduced to transform the CDC structure from a current-mode logic to a CMOS style. For example, when $CK_{INP}$ rises from low to high, $M_6$ is turned on to push up $CK_{AN}$ to $V_{DD}$-$V_{SD,6}$, where $V_{DD}$ is the power supply for the CDC and $V_{SD,6}$ is the source-drain voltage of $M_6$. At the same time, $CK_{INN}$ falls from high to low, resulting in that $CK_{AP}$ falls to $V_{TCS}+V_{DS,1}$, where $V_{TCS}$ is the voltage headroom for the tail current source and $V_{DS,1}$ is the drain-source voltage of $M_1$. And therefore, with $M_5$ and $M_6$, the

voltage swing of output clock signals of the CDC is fixed to $V_{DD}$-$V_{SD,6}$-$V_{TCS}$-$V_{DS,1}$ and will not change with the gate voltages of $M_3$ and $M_4$. In this way, the gain of CDC can be designed to be smaller to reduce the power dissipation.

Apart from the timing adjustment issue, clock signals suffer from quadrature error, duty-cycle error, and differential error during distribution, owing to the layout mismatch between the branches as well as parasitics of active devices and routing metals. For quadrature error, since differential clock pairs $CK_0$/$CK_{180}$ and $CK_{90}$/$CK_{270}$ are buffered by separate branches as described in Fig. 2.10, the error can be easily cancelled using CDCs. For example, if $CK_{90}$/$CK_{270}$ lag $CK_0$/$CK_{180}$ by more than 90 degrees, the error can be corrected by reducing the link delay for $CK_{90}$/$CK_{270}$ by tuning CDCs. The branch separation also makes it possible to finely correct the duty-cycle distortion issue of the 4-to-1 MUX as mentioned in part A of this section. To compensate for the duty-cycle error, a duty cycle corrector (DCC) is implemented following the CDC link, as shown in Fig. 2.11(b). The DCC adopts an inverter-based structure with adjustable push-up and pull-down current sources. The duty cycle of clock signals can be tuned by adjusting gate voltages of $M_7$~$M_{10}$. Fig. 2.12 presents an instance to illustrate the principle of the DCC, where the duty cycle of $CK_{AP}$ is larger than 50%. In this case, $I_{PULL}$ are supposed to be reduced by decreasing the gate voltage of $M_8$, and thus the falling transitions of $CK_{BP}$ can be slowed down. After passing through the inverter $I_1$ which is implemented for waveform shaping, a clock signal $CK_{CP}$ with corrected duty cycle can be obtained. Following the DCC, a clock buffer cascading two stages of inverters is implemented to increase the drive capability, as shown in Fig. 2.11(c). Between the two-stage inverters, a pair of cross-coupled inverters $I_3$ and $I_4$ are inserted, to suppress the differential error [36].

### 2.3.3 Output Stage

The first concern for output stage design is to select an appropriate VCSEL driven scheme. [15] and [22] use the common-anode scheme depicted by Fig. 2.13(a), in which the

anode of VCSEL is biased at a fixed voltage $V_{DD}$ and the high-speed electrical signal is applied to the cathode of VCSEL. However, VCSELs typically require an anode-to-cathode voltage of larger than 2 V for high-speed operations [37]. Hence a high $V_{DD}$ is demanded. As a result, the power consumption for the output stage increases and the dummy path has breakdown risks. Moreover, commercial VCSEL arrays typically share the same cathode, and thus the common-anode scheme can hardly be extended to multi-channel applications. In view of this, this work uses a common-cathode scheme as shown in Fig. 12(b), in which the cathode of VCSEL is biased at a fixed voltage and the electrical signal is applied to the anode of VCSEL. In this scheme, the anode-to-cathode voltage for the VCSEL is determined by $V_{DD}$-$V_B$. Since $V_B$ is independent of the power domain of output stage, a negative $V_B$ can be employed to reduce the required $V_{DD}$. This approach reduces the power overhead of the output stage and mitigates the breakdown issue.

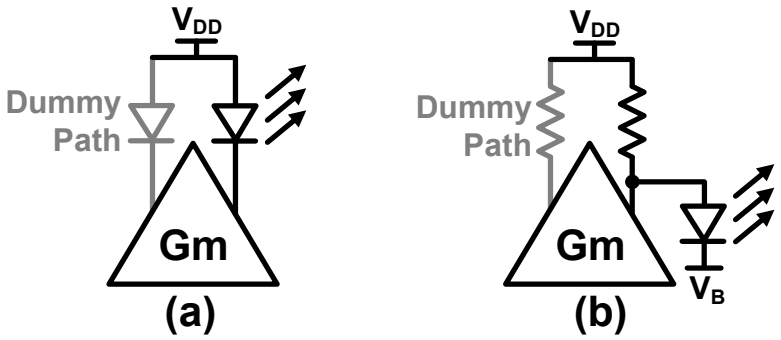


**Fig. 2.13 (a) Common-anode and (b) common-cathode schemes.**

The detailed implementation of the proposed output stage is shown in Fig. 2.14. It consists of three Gm slices, a dummy load, an output load, and a T-coil. Each Gm slice contains a pre-tap Gm cell ($Gm_p$) and a main-tap Gm cell ($Gm_m$). The polarities of the outputs of $Gm_p$ are reversed with those of $Gm_m$ to implement the FFE. The differential outputs from the three Gm slices are summed at the dummy and output loads. The output load, which consists of large-size PMOS-based current sources and resistors, is divided into two parts. These two parts are separated by a T-coil for bandwidth extension. The output node of the transmitter is wire-bonded to the anode of the VCSEL, and the cathode of the VCSEL is

wire-bonded back to the chip for AC de-coupling. The cathode of VCSEL is biased at a negative voltage of -0.8 V to reduce the required supply voltage of the output stage to 2 V.

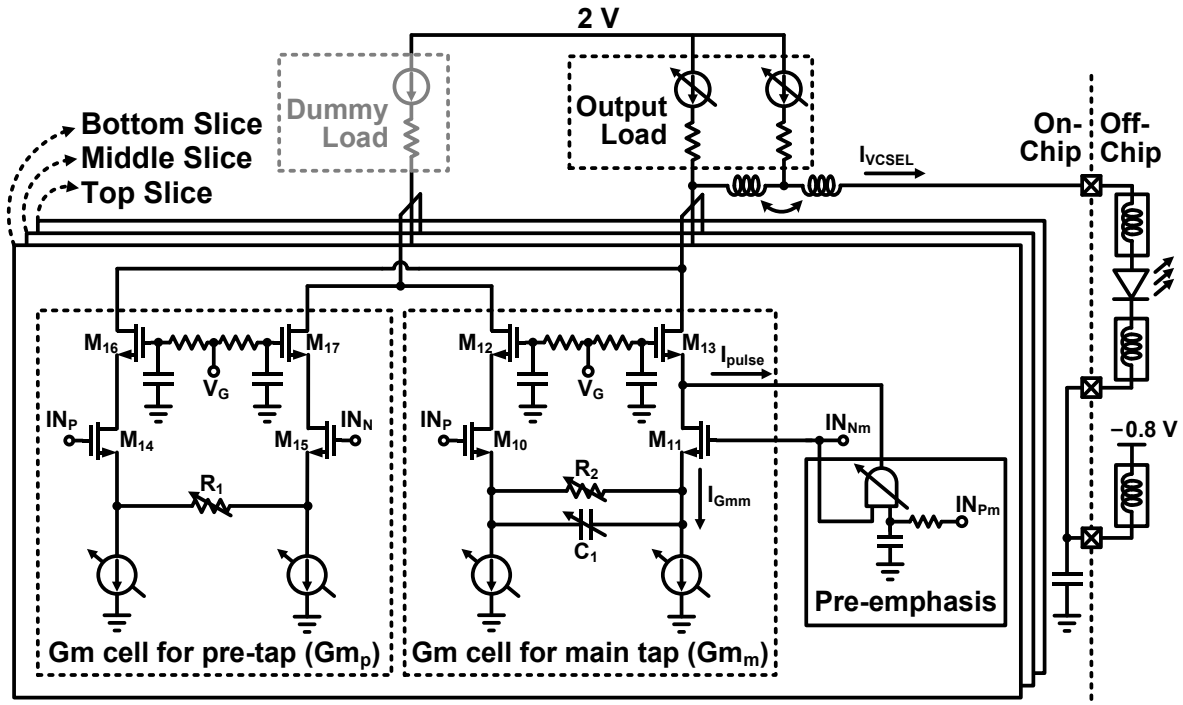


**Fig. 2.14. Implementation of the output stage.**

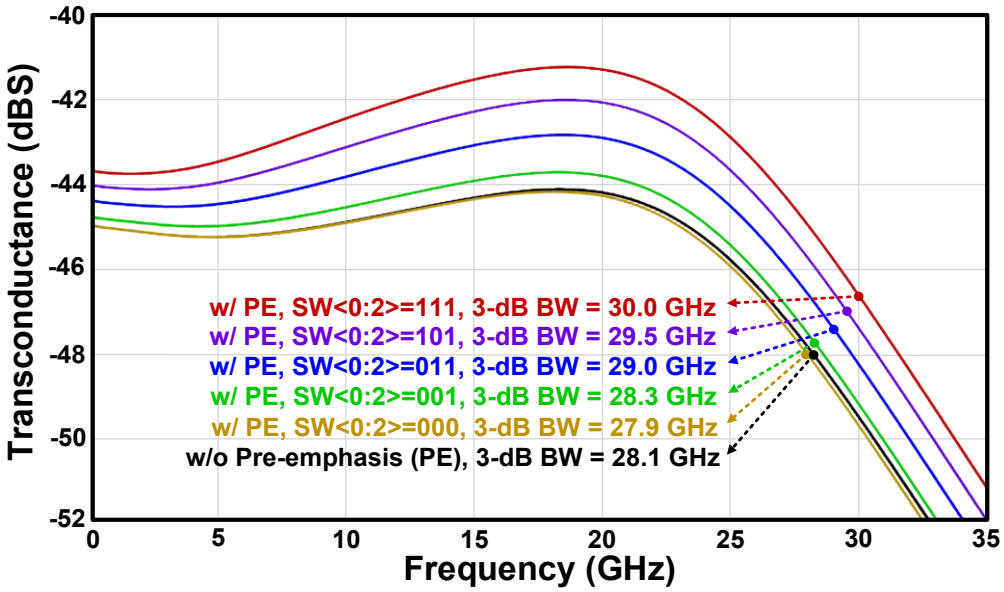


**Fig. 2.15. Simulated frequency responses of the main-tap Gm cell without and with the pre-emphasis circuit of different strengths.**

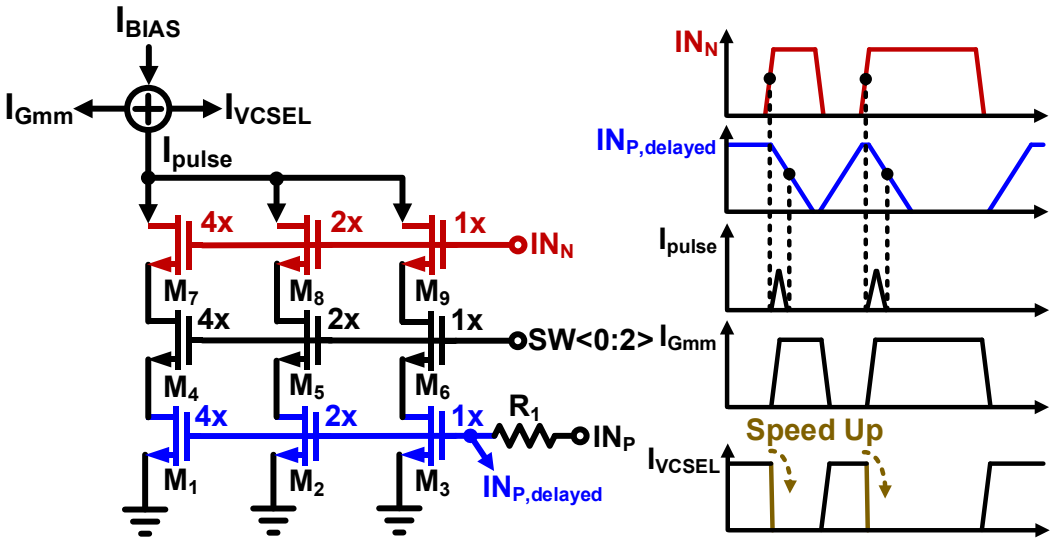


**Fig. 2.16. Principle of the proposed pre-emphasis circuit.**

To ensure safe operation with 2-V supply voltage, $Gm_p$ adopts a cascode structure. A degenerated variable resistor $R_1$ made of digitally controlled transistor-resistor array [38] is implemented to enable gain tuning. $Gm_m$ employs a similar topology but with two differences. Firstly, a degenerated capacitor bank [39] is added in parallel with the degenerated variable resistor to form a CTLE to boost the bandwidth. Secondly, a pre-emphasis circuit is integrated with $Gm_m$ to mitigate the asymmetric response issue of the VCSEL. The output of the pre-emphasis circuit is connected to the source of the cascode transistor $M_{13}$. As the dominant pole of $Gm_m$ locates at the drain of $M_{13}$ and the source of $M_{13}$ exhibits a low impedance, the impact from the parasitics of pre-emphasis circuit on bandwidth is small. It can be validated by the frequency-domain simulation results shown in Fig. 2.15. The 3-dB bandwidth of the Gm cell without pre-emphasis circuit is 28.1 GHz. When introducing pre-emphasis circuit and setting SW<0:2> as 000 to turn off the pre-emphasis function, the 3-dB bandwidth degrades to 27.9 GHz. The degradation is slight and acceptable for 28-Gbaud operation.

Fig. 2.16 describes the principle of the pre-emphasis circuit, which implements a current-mode AND operation between input data $IN_N$ and $IN_{P,delayed}$. $IN_{P,delayed}$ is the delayed version of $IN_P$. The delay is provided by a low-pass network composed of a poly resistor $R_1$ and parasitic capacitance of $M_1$~$M_3$. At the rising edge of $IN_N$, $IN_{P,delayed}$ falls. Due to the delay,

there is a period when both $IN_N$ and $IN_{P,delayed}$ are high, resulting in a narrow current pulse denoted as $I_{pulse}$. The relationship between the current signals flowing through the output node can be expressed as

$$I_{VCSEL} = I_{BIAS} - I_{Gmm} - I_{pulse} \tag{2.1}$$

where $I_{VCSEL}$, $I_{BIAS}$ and $I_{Gmm}$ are the current applied to the VCSEL, the bias current set by the output load and the current generated by the main-tap Gm cell, respectively. When $IN_N$ rises, $I_{Gmm}$ rises. Since $I_{BIAS}$ is fixed, rising of $I_{Gmm}$ results in the falling of $I_{VCSEL}$. At this moment, the generation of $I_{pulse}$ will boost the falling of $I_{VCSEL}$. In this way, the VCSEL's falling response can be accelerated, thereby relieving the asymmetric response issue. Besides, from the frequency-domain perspective, $I_{pulse}$ as a pulse signal will introduce a high-frequency component into the output of $Gm_m$, which is beneficial for the bandwidth of the transmitter. This effect can be confirmed by the simulation results in Fig. 2.15. With the increase of the pre-emphasis strength, the 3-dB bandwidth of the main-tap Gm cell gradually increases. Besides, the DC gain also increases slightly. This is because the proposed pre-emphasis circuit will contribute to the signal amplification when any of the branches is turned on. For instance, as the gate of $M_1$ is biased at the DC voltage of $IN_{P,delayed}$, when $M_4$ is switched on, $M_1$ will provide a small current to $M_7$. And then, $M_7$ will amplify $IN_N$ with a small transconductance.

## 2.4 Measurement Setups and Results

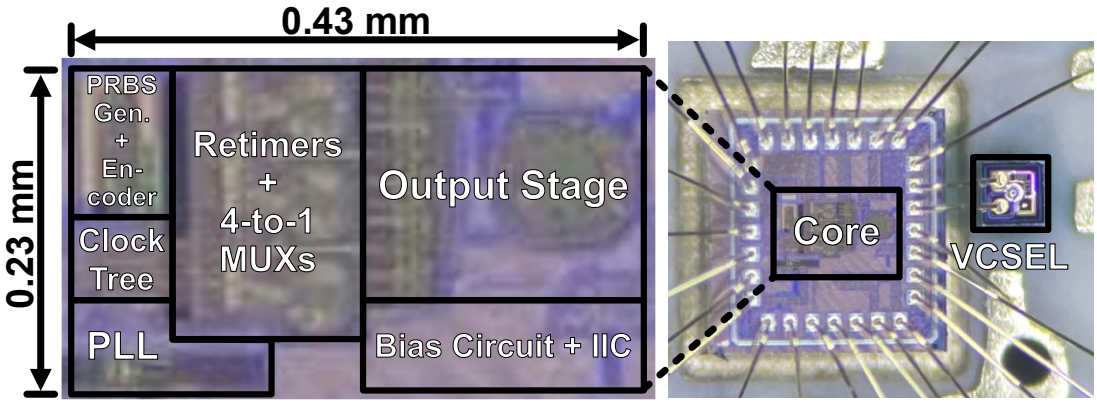


**Fig. 2.17. Die photo of the transmitter.**

The transmitter prototype is fabricated in 40-nm CMOS technology. The micrograph of the die is shown in Fig. 2.17. The core, which consists of the data path, clock path, and bias and control circuits, occupies an area of 0.01 $mm^2$. This section will introduce the electrical and optical measurement setups for the transmitter, as well as corresponding measurement results.

### 2.4.1 Electrical Measurement Setup and Results

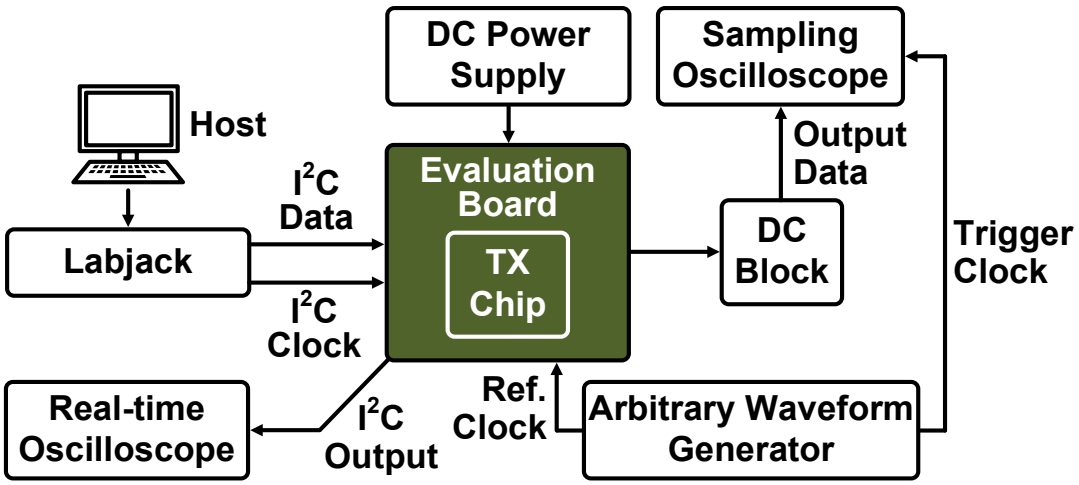


**Fig. 2.18. Electrical measurement setup for the transmitter.**

Although the proposed transmitter is designed for driving VCSELs, electrical measurement is necessary before the optical measurement to ensure functionality of the transmitter chip and facilitate debugging. Fig. 2.18 shows the electrical measurement setup for the transmitter. The transmitter chip is mounted on a high-frequency evaluation board by bond-wires. $I^2C$ is implemented on-chip to control the operations of the circuits. The serial data and clock for $I^2C$ are provided by a Labjack. And the output of $I^2C$ is delivered to a real-time oscilloscope to ensure that the serial data has been written to the on-chip $I^2C$ correctly. The electrical output of the transmitter chip is sent via a SMA connector and a DC block to the sampling oscilloscope for eye diagram observation. An arbitrary waveform generator (AWG) generates the reference clock for the on-chip PLL and the trigger clock for the sampling oscilloscope.

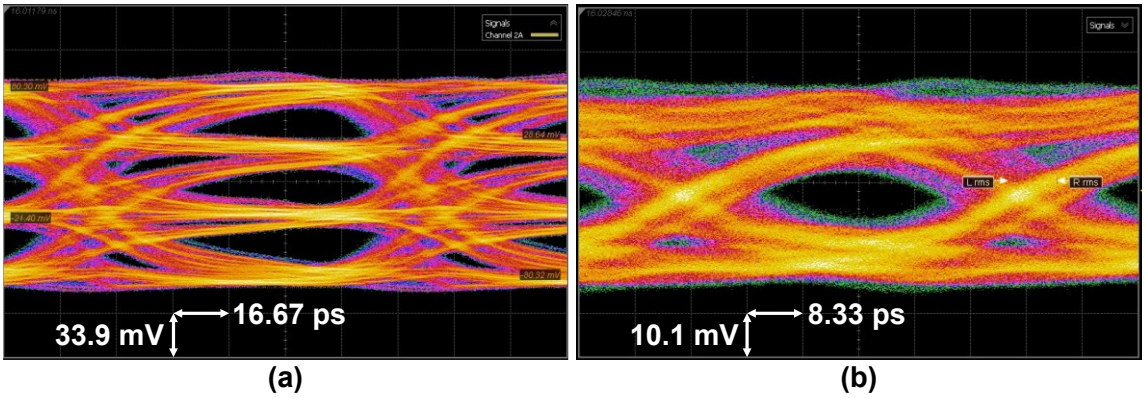


**Fig. 2.19. Measured (a) 10-Gbaud PAM-4 and (b) 20-Gbaud NRZ electrical eye diagrams of the transmitter.**

Fig. 2.19(a) shows the measured 10-Gbaud PAM-4 eye diagram with a single-ended voltage swing of 161 mV. The ratio-of-level mismatch (RLM) of the PAM-4 eye is 94.1%. Fig. 2.19(b) shows the measured 20-Gbaud NRZ eye diagram with a single-ended swing of 56 mV. It is noted that the output impedance of the transmitter is designed to be 110 Ω to match the 110-Ω input impedance of VCSEL. Thus, when the output port of the transmitter is connected to the 50-Ω input port of the sampling oscilloscope, there will be severe impedance mismatch between the two ports. This is why the quality of the measured electrical eye diagram is not good and the measured maximum data rate is not that high. But the measured electrical eye diagrams are still meaningful, as they indicate that the transmitter works normally.

### 2.4.2 Optical Measurement Setup and Results

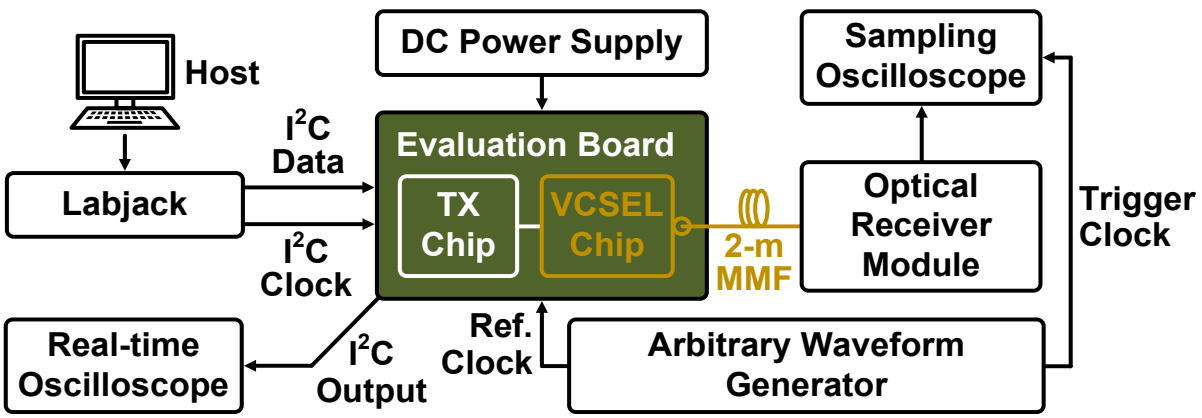


**Fig. 2.20. Optical measurement setup for the transmitter.**

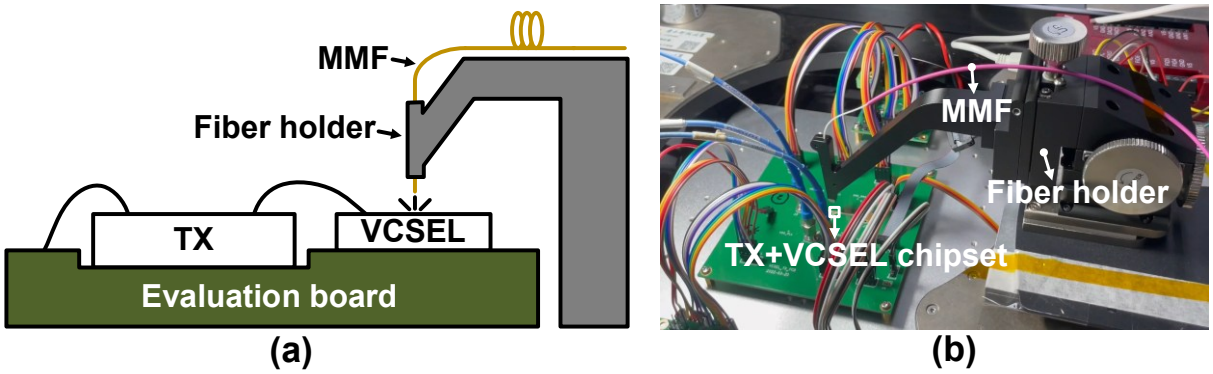


**Fig. 2.21. (a) Transmitter-VCSEL packaging and fiber holding scheme and (b) photo of the optical measurements.**

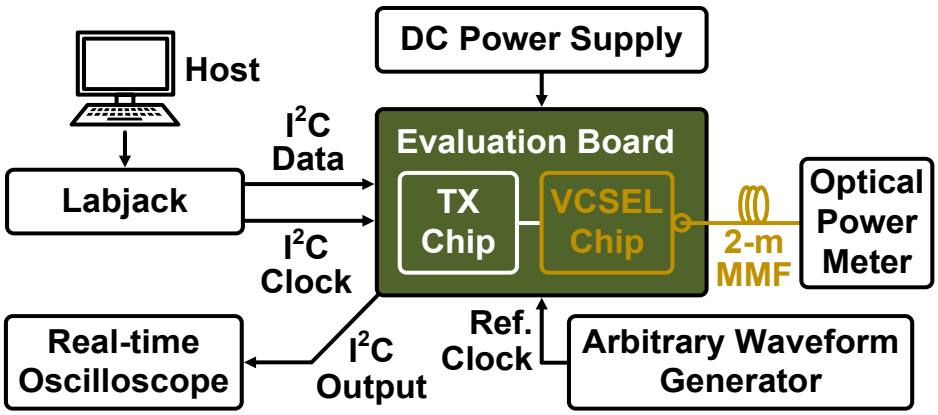


**Fig. 2.22. Setup for the fiber aligning operation.**

To fully verify the proposed piecewise compensation scheme, a commercial 19-GHz VCSEL is wire-bonded with the transmitter for optical measurement. The setup for the optical measurement is described in Fig. 2.20. The output of the TX is wire-bonded to a commercial VCSEL chip. The control part and the DC power supply part are the same as the electrical measurement setup described in 2.3.1. For the high-speed part, an AWG generates reference clock for the on-chip PLL inside the TX. With the clock, the TX outputs the high-speed electrical signal to the VCSEL. And the VCSEL performs E/O conversion. The optical signal emitted from the VCSEL is butt-coupled to a 2-meter OM2 multi-mode fiber (MMF) fixed by a customized fiber holder as shown in Fig. 2.21. The terminal of the fiber is tapered to reduce the coupling loss. The fiber holder can be tuned in X, Y, Z dimensions manually, to get the terminal of the fiber align with the emitting spot of the VCSEL. During fiber aligning process,

another terminal of the fiber is connected to an optical power meter instead of the optical receiver module to facilitate the aligning operation, as shown in Fig. 2.22. And after the aligned optical power is above 0 dBm which is the minimum required power level for eye diagram observation, the fiber terminal is connect back to the optical receiver module. In addition, as the transmitter chip is thicker than the VCSEL chip, the surfaces of the two chips are not at the same horizontal plane. Therefore, as shown in Fig. 2.21, the evaluation board is trenched to accommodate the transmitter die, so that the height difference between the two surfaces can be minimized. In this way, the length of the bondwire connecting the transmitter and VCSEL can be reduced to relieve the bandwidth degradation owing to bondwire parasitics.

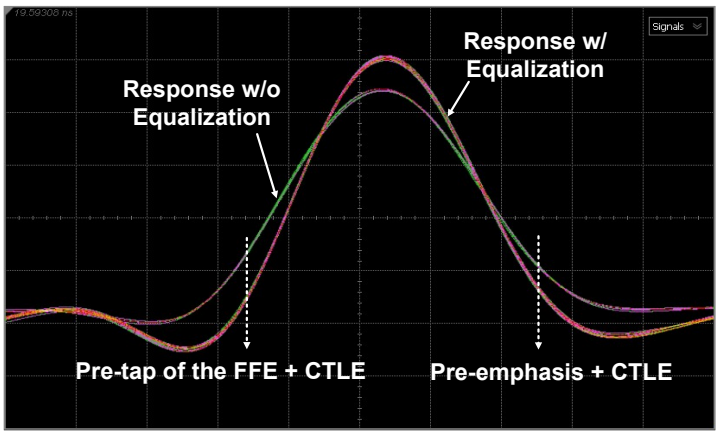


**Fig. 2.23. Setup for the fiber aligning operation.**

Fig. 2.23 presents the measured optical 50-ps single-pulse responses with the on-chip 2-tap FFE, CTLE and pre-emphasis circuit turned off and on. Due to inadequate bandwidth of the wire-bonded VCSEL, when the three circuits are turned off, the optical response shows long inter-symbol interference (ISI) tail. When the three circuits are turned on, since the bandwidth of the transmitter-VCSEL system is boosted, the tail is obviously reduced. Moreover, the optical pulse becomes higher when the three circuits are turned on. This is because the gain improvement from the pre-emphasis circuit could compensate for the gain loss from the 2-tap FFE, manifesting the advantage of the hybrid equalization scheme over single equalization method.

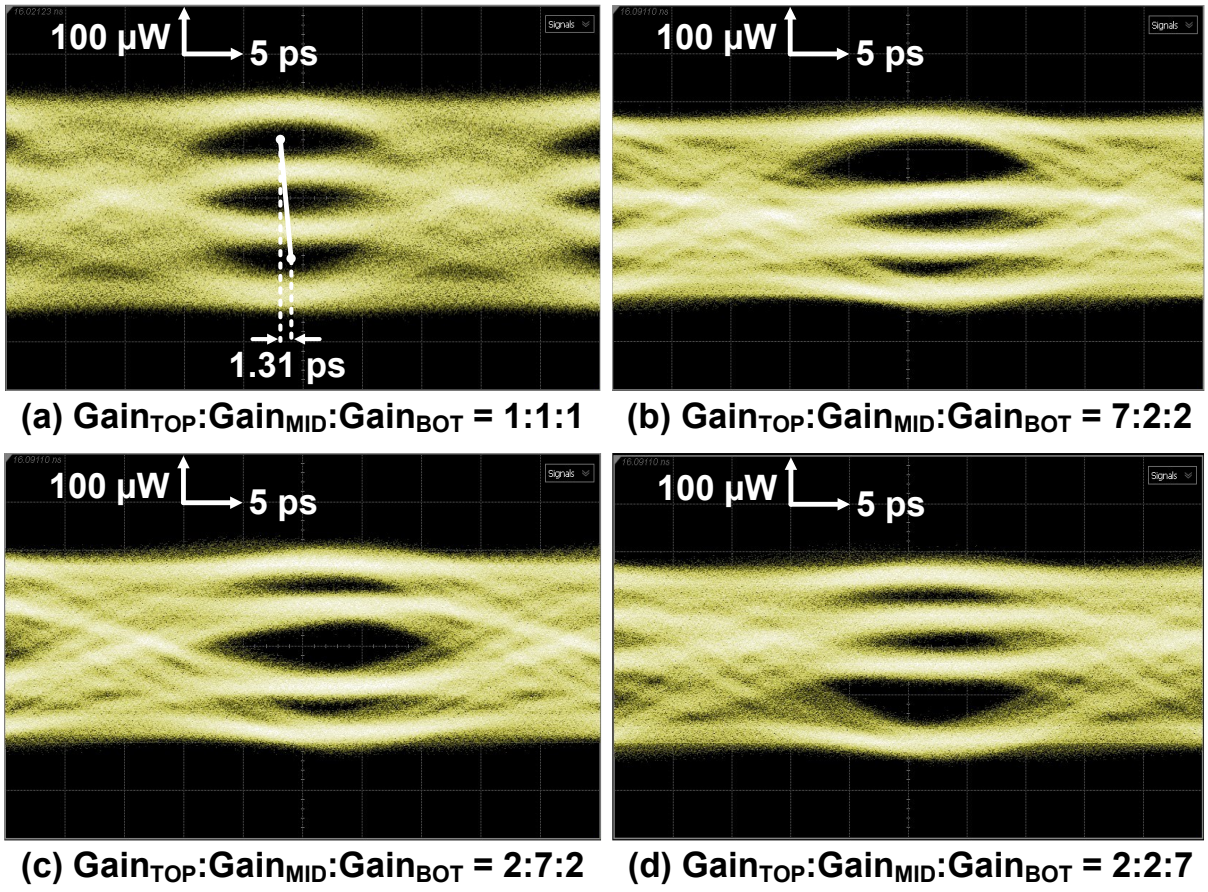


**Fig. 2.24. Measured optical eye diagrams at 28-Gb/s PAM-4 with different settings.**

Fig. 2.24(a) presents the measured 28-Gb/s optical PAM-4 eye diagram with the equalization circuits turned off and the gains of the top, middle, and bottom slices kept the same. The average sub-eye amplitude/width and RLM are 56.56 μW/26.75 ps and 88.4%, respectively. At this data rate, VCSEL's asymmetric response issue is not significant. And therefore, the horizontal skew, which is defined as the X-axis difference between the middle points of the top sub-eye and bottom sub-eye as described in Fig. 2.24(a), is as small as 1.31 ps. Fig. 2.24(b)~(c) show the optical eye diagrams also at 28-Gb/s PAM-4 but with different gain settings for the three data slices. For instance, in Fig. 2.24(b), the gain of the top slice is set to be 3.5 times those of the middle and bottom slices. As a result, the amplitudes of top, middle, and bottom sub-eyes are 103.2 μW, 31.5 μW, and 31.0 μW, respectively. In other words, the amplitude of the top sub-eye becomes about 3.27 and 3.33 times those of middle and bottom sub-eyes, respectively, which are close the ratio of the slice gain settings. Overall, Fig. 2.24(b)~(c) validate the piecewise gain tuning scheme.

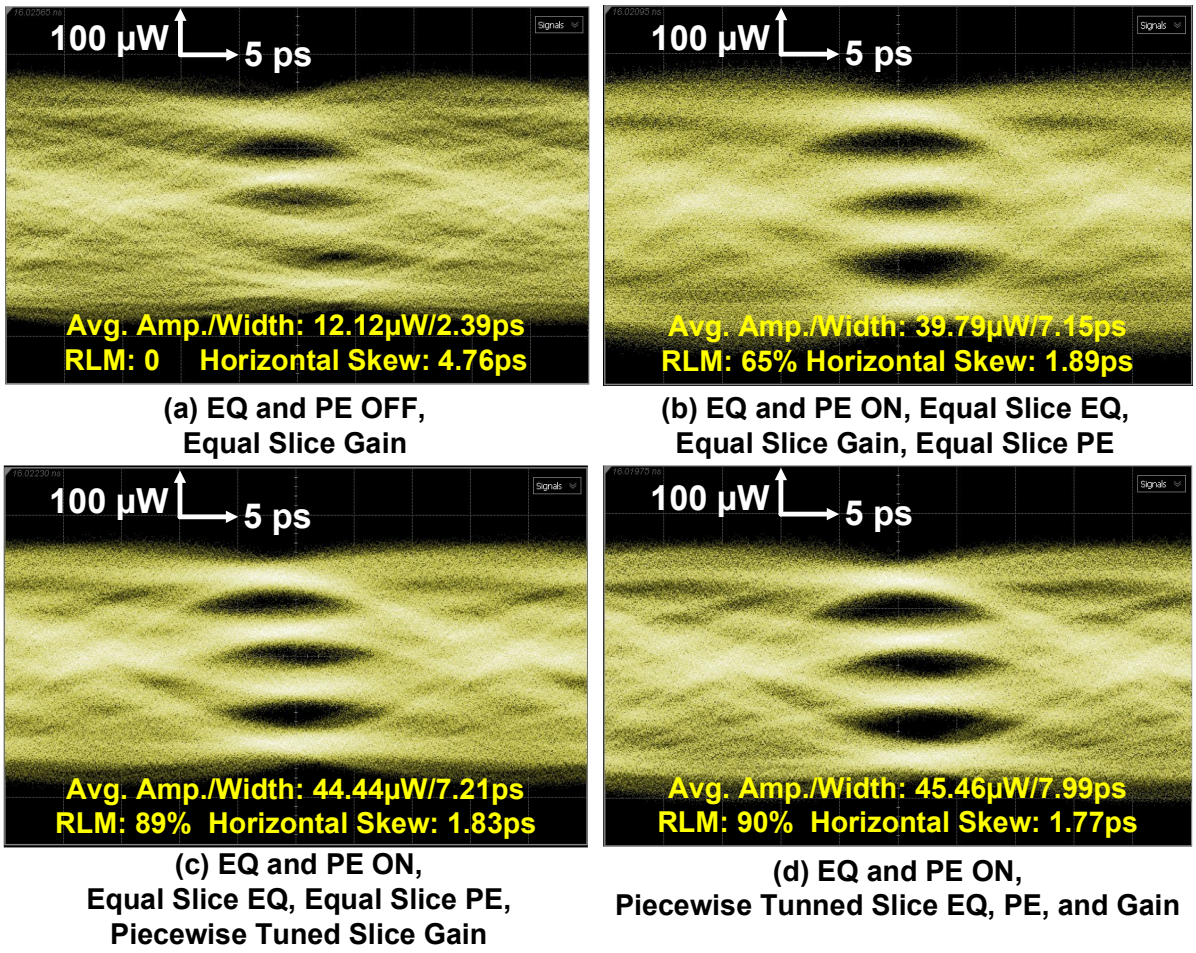


**Fig. 2.25. Measured optical eye diagrams at 56-Gb/s PAM-4 with different gain, equalization (EQ) and pre-emphasis (PE) settings for three data slices.**

When it goes to higher data rate, the bandwidth of the electro-optical system can be inadequate, and the VCSEL's asymmetric response issue also emerges. In this situation, piecewise tuning of equalizations and pre-emphasis becomes important. To demonstrate it, Fig. 2.25 shows measured optical eye diagrams at 56-Gb/s PAM-4 with different settings of gain, equalization, and pre-emphasis for the three data slices. Fig. 2.25(a) shows the eye diagram when turning off the equalization and pre-emphasis, with the gains of the three slices kept the same. It is shown that the optical eye diagram cannot be clearly opened owing to inadequate bandwidth. In addition, the optical eye exhibits a horizontal skew as large as 4.76 ps (~0.13 UI) because of VCSEL's asymmetric response. Fig. 2.25(b) presents the measured optical eye diagram which is clearly opened after turning on the equalizations and

pre-emphasis. The equalizations, pre-emphasis and gains of the three data slices are configured to be the same. The average sub-eye amplitude and width are improved noticeably from 12.12 μW and 2.39 ps to 39.79 μW and 7.15 ps, respectively. Leveraging the pre-emphasis circuit, the horizontal skew decreases from 4.76 ps to 1.89 ps. However, due to the nonlinearities of the VCSEL, the openings of the three sub-eyes still differ. The top sub-eye is the widest as the top sub-eye has the highest E/O bandwidth. The amplitude of the bottom sub-eye is the largest because the bottom sub-eye has the highest E/O gain. For the middle sub-eye, it has medium bandwidth and gain. Moreover, since the PAM-4 signal is 'stacked' by these three NRZ signals in the proposed transmitter, the overshooting of the NRZ signals from the top and bottom slices induced by the equalization circuits and T-coil will 'squeeze' the NRZ signal from the middle slice. The squeezing effect, medium bandwidth, and medium gain together result in the smallest middle sub-eye opening. And the RLM of the PAM-4 eye is as low as 65%. To even the amplitudes of the three sub-eyes, in Fig. 2.25(c), the gains of the three data slices are piecewise tunned. Specifically, the gain of the top slice is tuned to be smaller than that of the middle slice but larger than that of the bottom slice. In this way, the RLM is enhanced significantly to 89%. Based on Fig. 2.25(c), the equalization and pre-emphasis of the three slices can be further piecewise tuned. Eventually, as shown in Fig. 2.25(d), a PAM-4 optical eye diagram with the largest eye opening and RLM as well as the smallest horizontal skew is obtained. Compared with Fig. 2.25(b), the piecewise compensation scheme improves the average sub-eye amplitude/width and RLM by 14%/12% and 38%, respectively. It is also noted that the piecewise tuned pre-emphasis helps reduce the horizontal skew by 63% comparing Fig. 2.25(d) with Fig. 2.25(a). The OMA of the eye in Fig. 2.25(d) is about 1.18 mW after de-embedding 3-dB butt-coupling loss [15]. In summary, the step-by-step eye quality improvements from Fig. 2.25(a) to Fig. 2.25(d) demonstrate the effectiveness of the proposed piecewise compensation scheme for VCSEL non-idealities.

Fig. 2.26 presents the measured power breakdown for 56-Gb/s PAM-4 operation with the setting of Fig. 19(d). The transmitter consumes a power of 115 mW excluding that for VCSEL,

corresponding to an energy efficiency of 2.05 pJ/b. As shown, 70% of the power is consumed by the 4-to-1 MUXs and clock tree which mainly serve for the serialization and FFE, while the output stage burns only 20.9% of the power for VCSEL driving. Besides, the power overhead of the VCSEL is about 14 mW.

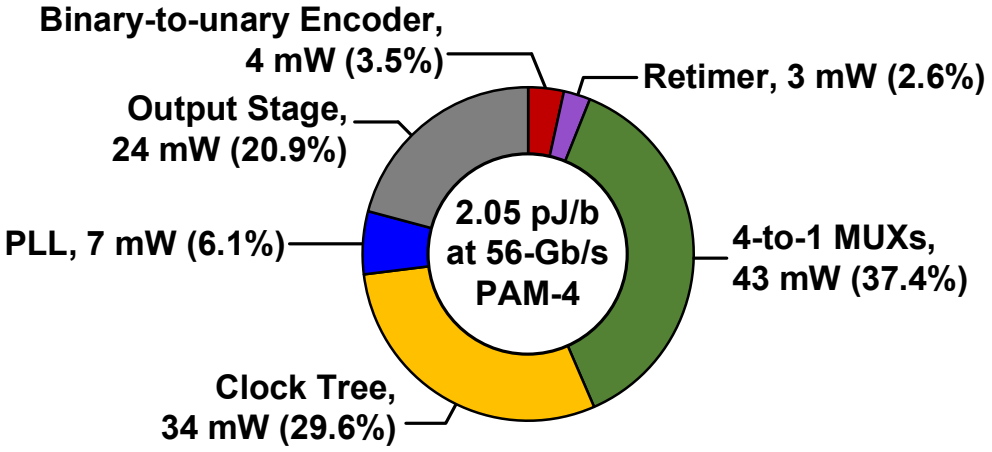


**Fig. 2.26. Power breakdown of the transmitter operated at 56-Gb/s PAM-4.**

### 2.4.3 Performance Summary

Table 2.1 summarizes the performance of the prototype and compares it with state-of-the-art PAM-4 VCSEL transmitters. Thanks to the compact mixed-signal implementation, the die area of the proposed transmitter is much smaller than those of [22] and [23] which use digital signal processing (DSP) to compensate for VCSEL non-idealities. Compared with [24], [25], and [40] which implement analog circuits to solve VCSEL non-idealities, the proposed transmitter achieves full compensation without any sacrifices on energy efficiency or die area. To the best of authors' knowledge, this work is the first design achieving full compensation for VCSELs' non-idealities without DSP techniques, bringing advantages of not only smaller die area but also lower link latency. The proposed piecewise compensation method can be further extended for higher-order modulated signals such as PAM-6 and PAM-8 to obtain higher data rate by modifying the implementation of the binary-to-unary encoder and the number of data slices. Taking PAM-8 as an instance, the binary-to-unary encoder is then supposed to be upgraded to convert the 3 binary inputs to 7

unary outputs, and 7 unary data slices should be implemented to separately control the amplitudes, widths as well as the rising/falling transitions of the 7 sub-eyes. The underlying compensation methodology remains unchanged.

**Table 2.1. Performance summary of the proposed VCSEL transmitter and comparison with state-of-the-art works.**

| | [22] | [23] | [24] | [25] | [40] | This work |
|---|---|---|---|---|---|---|
| CMOS technology | 65nm | 40nm | 65nm | 40nm | 12nm | 40nm |
| Architecture | Half-rate | Quarter-rate | Quarter-rate | Quarter-rate | Full-rate | Quarter-rate |
| Data rate [Gb/s] | 50 | 56 | 64 | 64 | 50 | 56 |
| OMA [mW] | 2.00 | 0.81* | 2.50* | 1.08* | 1.39 | 1.18* |
| Energy efficiency [pJ/b] | 5.12 | 1.73 | 2.69** | 2.09 | 0.82*** | **2.05**** |
| Core area [$mm^2$] | 0.31 | 0.47 | 0.28 | 0.16 | 0.09*** | **0.10** |
| Equalization | 2.5-tap Nonlinear FFE | 2-tap Nonlinear FFE | 3-tap Asym. FFE | 3-tap Asym. FFE | 3-tap Asym. FFE | **2-tap FFE+ CTLE + Pre-emphasis** |
| Full Compensation? | Yes | Yes | No | No | No | **Yes** |
| Method Type | Digital | Digital | Analog | Analog | Analog | **Mixed-signal** |

## 2.5 Conclusion

In this chapter, a piecewise compensation scheme addressing VCSELs' E/O gain nonlinearity, bandwidth nonlinearity and asymmetric rising/falling responses is proposed. Utilizing the scheme, a quarter-rate transmitter prototype comprised of improved 4-to-1

MUXs, 3-layer clock tree, 2-tap FFE, CTLE and pre-emphasis circuit is implemented. Optical measurements with a commercial VCSEL at 56-Gb/s PAM-4 operation demonstrate that, by piecewise configuring the equalizations, pre-emphasis and gains of three data slices, the average optical PAM-4 sub-eye amplitude/width, RLM and horizontal skew are enhanced by 14%/12%, 38% and 63%, respectively. The transmitter achieves a de-embedded OMA of 1.18 mW and delivers an energy efficiency of 2.05 pJ/b at 56-Gb/s PAM-4.

# CHAPTER III

## 56-Gbaud Half-rate Linear Modulator Transmitter Design

## 3.1 Introduction

As introduced in chapter I, optical modulators require electrical transmitters with large output swing and high bandwidth to generate high-ER and high-speed optical signals. Besides, equalization capability is a plus to allow the utilization of large-size optical modulators for further enhancement of the ER. Moreover, linearity is an important concern, as PAM-4 modulation scheme is widely deployed replacing traditional NRZ scheme nowadays to double the data rate using the same system bandwidth.

The above performances are mostly determined by the final stage of the electrical transmitter, i.e. driver. Several drivers for optical modulators are reported recently targeting simultaneously satisfy those specifications [41-49]. Most of them are implemented in compound semiconductor processes such as SiGe BiCMOS and InP, which outperform bulk CMOS process in terms of speed, power gain, and breakdown voltage. [45] presents a distributed modulator driver in 130-nm SiGe BiCMOS, in which transmission lines are utilized to counter the parasitics of Gm cells for bandwidth extension. A maximum swing of 4 $V_{ppd}$ is achieved with 50-Gb/s non-return-to-zero (NRZ) signals. [46] proposed a multi-mode driver also in a distributed manner using 130-nm SiGe BiCMOS. By modifying the gain and polarization of the Gm cell, the driver can be re-configured into an amplifier, a duobinary encoder and a 2-tap FFE. The functions are well demonstrated and a swing of 4 $V_{ppd}$ is achieved for 64-Gb/s duobinary signals. [47] proposes a modulator driver in 55-nm SiGe BiCMOS, achieving a data rate of 120-Gb/s NRZ with a swing of 2.8 $V_{ppd}$. The driver is implemented in a hybrid topology, where the output stage adopts a distributed topology while the preceding stages such as the input buffer and variable-gain amplifier (VGA) are all lumped, to achieve a good balance between the gain, bandwidth and die area. Similarly, [48] presents a 4-channel linear driver also with a hybrid topology using 55-nm SiGe BiCMOS, achieving a data rate of 256-Gb/s PAM-4 with a swing of 3.4 $V_{ppd}$. [49] reports a lumped

linear modulator driver in InP technology. With a superior process performance, the driver achieves a data rate of 180-Gb/s PAM-4 with a swing of 3 $V_{ppd}$.

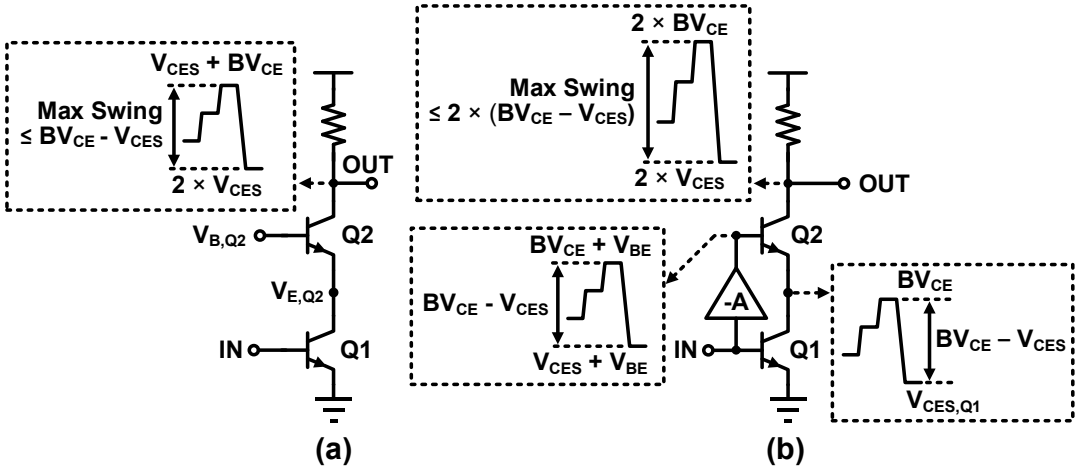


**Fig. 3.1 Illustrations of (a) the conventional cascode structure, and (b) BV doubler.**

However, the output stages of [46,48,47,45,49] are all implemented using cascode structure as illustrated in Fig. 3.1(a). With the input signal swinging, the current flowing through the emitter of Q2 denoted by $I_{E,Q2}$ changes. Since

$$V_{BE,Q2} = V_T \ln \frac{I_{E,Q2}}{I_S} \tag{3.1}$$

where $V_T$, $I_S$, and $V_{BE,Q2}$ are the thermal voltage, saturation current, and base-emitter voltage of Q2, respectively, the impact of the variation of $I_{E,Q2}$ on $V_{BE,Q2}$ is small. In other words, $V_{BE,Q2}$ is almost static. As the base voltage of the Q2 denoted by $V_{B,Q2}$ is fixed, the emitter voltage of Q2 denoted by $V_{E,Q2}$ can be seemed unchanged. Therefore, the maximum output swing of the conventional cascode structure denoted by $SW_{CAS}$ depends on the breakdown voltage of Q2. Assuming Q1 and Q2 adopt the same size, $SW_{CAS}$ can be expressed by

$$SW_{CAS} = BV_{CE} - V_{CES} \tag{3.2}$$

where $BV_{CE}$ is the collector-emitter breakdown voltage of Q1 and Q2, and $V_{CES}$ is the minimum collector-emitter voltage to prevent Q1 and Q2 from saturation region.

To improve the output swing without sacrificing reliability, [50] proposes a driver topology named breakdown voltage (BV) doubler, which is depicted in Fig. 3.1(b). In BV

doubler, an auxiliary amplifier is implemented to inversely amplify the input signal and deliver its output to the base of Q2. Therefore, $V_{B,Q2}$ changes with the input signal. As $V_{BE,Q2}$ stays almost unchanged, $V_{E,Q2}$ changes accordingly. $V_{E,Q2}$ should to be higher than $V_{CES}$ to prevent Q1 from saturation and smaller than $BV_{CE}$ to protect Q1 from breakdown. And therefore, the auxiliary amplifier should be designed to have an output swing of

$$SW_{AUX} = BV_{CE} - V_{CES} \tag{3.3}$$

In this way, $V_{E,Q2}$ swings in-phase with the collector voltage of Q2, i.e. the output of the driver. Therefore, the maximum output swing of the BV doubler denoted by $SW_{BVD}$ is enhanced to

$$SW_{BVD} = 2 \times (BV_{CE} - V_{CES}) \tag{3.4}$$

which is two times that of the conventional cascode structure shown in Fig. 3.1(a). With BV doubler, [50] achieves a maximum differential output swing of 6 $V_{ppd}$.

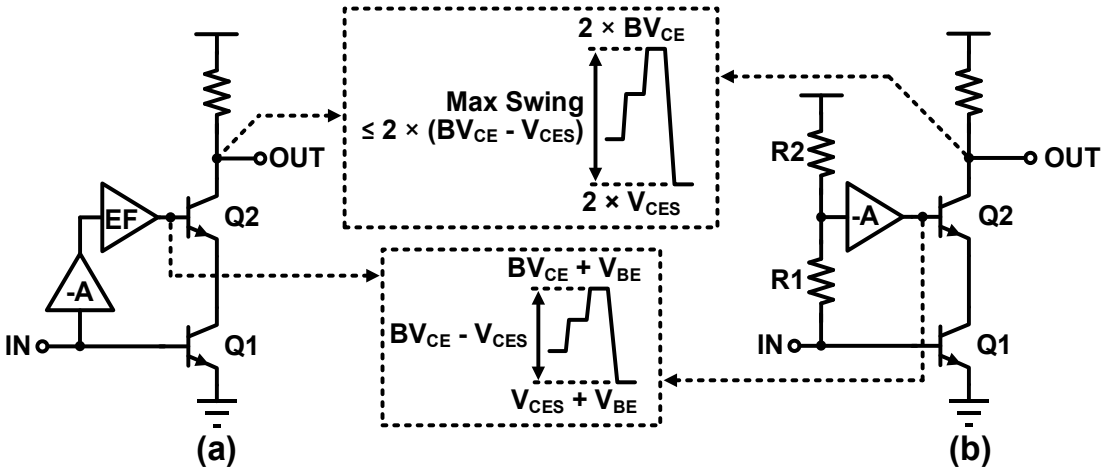


**Fig. 3.2 Illustrations of (a) BV doubler with enhanced dynamic bias stage, and (b) BV doubler with resistor-based capacitor splitter.**

Following [50], several techniques have been reported to optimize the performance of BV doubler. In Fig. 3.1(b), as the size of Q2 is typically large to deliver large current, the transistors inside auxiliary amplifier are supposed to be large to improve the bandwidth at the base of Q2, resulting in high power overhead. Therefore, to improve the power efficiency of the BV doubler, [51] inserts an emitter follower between the output of the auxiliary amplifier and the base of Q2, as shown in Fig. 3.2(a). The emitter follower functions as a signal buffer

to reduce the time constant at the base of Q2, and hence the auxiliary amplifier can be designed smaller to save power. In [52], a resistor-based capacitor splitting scheme is reported to enhance the bandwidth of BV doubler as depicted in Fig 3.2(b). The resistor R1 isolates the input of the auxiliary amplifier from the base of Q1. In this way, the impact of the large-size input transistors of the auxiliary amplifier on the bandwidth of BV doubler can be reduced. While both [50] and [51] demonstrate the designs using NRZ not demanding linearity, [52] stimulates the proposed driver using PAM-4 and PAM-8. And thus, emitter-degenerated resistors are introduced at the output stage of the BV doubler for linearity enhancement. Nevertheless, the linearity of the driver is still inadequate, as the swing decreases dramatically from 6-$V_{ppd}$ for NRZ case to 2.4 $V_{ppd}$ for high-speed PAM-4 and PAM-8 cases according to measurement results.

Therefore, in this work [53], an enhanced BV doubler named dynamic triple-stacked topology is proposed in 130-nm SiGe BiCMOS to improve the linearity as well as output swing of the driver. Furthermore, to boost the link bandwidth as well as broaden the application scenarios, the driver is integrated monolithically with an analog multiplexer-based feed-forward equalizer (AMUX-FFE) to implement a complete linear transmitter for optical modulators. The AMUX-FFE simultaneously achieves 2-to-1 analog serialization and 3-tap highly re-configurable feed-forward equalization without the need of extra tap generator.

This chapter is organized as follows. Section 3.2 introduces the architecture design of the proposed linear transmitter, followed by detailed description on the implementations of AMUX-FFE and linear driver in section 3.3. In section 3.4, measurement setups and results of the standalone linear driver chip as well as the whole transmitter chip are introduced. The conclusion of this chapter is drawn in section 3.5.

## 3.2 Architecture Design

In typical optical links such as those in Fig. 1.3(a) and Fig. 1.3(b), high-speed

digital-to-analog converters (DACs) are widely adopted at the transmitter side to modulate the digital signals from the preceding DSP into analog signals. As the connections between the DAC and DSP are quite complicated, the DAC and DSP are typically implemented monolithically using advanced CMOS nodes to avoid assembling loss. However, with the scaling of CMOS technologies slowing down, DACs meet bottleneck in further developing the bandwidth to satisfy the dramatically increased demand of data throughput. To relieve the issue, [54] proposes an analog-multiplexed DAC which consists of two sub-DACs and a 2-to-1 AMUX. The AMUX serializes the outputs of the two sub-DACs, thereby halving the bandwidth requirements for the sub-DACs. After that, several AMUXs have been presented with various features [55], [56], [57]. But they are all standalone blocks with limited output swings, and thus cannot be directly adopted for optical modulator-based communication links. [58] proposes an AMUX-driver IC which integrates a 2-to-1 AMUX with a linear driver. Implemented in 250-nm InP technology, the AMUX-driver achieves 168-Gbaud PAM-4 output with a swing of 1.5 $V_{ppd}$. The swing is still small for high-V$\pi$ optical modulators with high electrical-to-optical (E/O) bandwidth but low E/O conversion efficiency. Furthermore, lacking equalization limits the application of this chip.

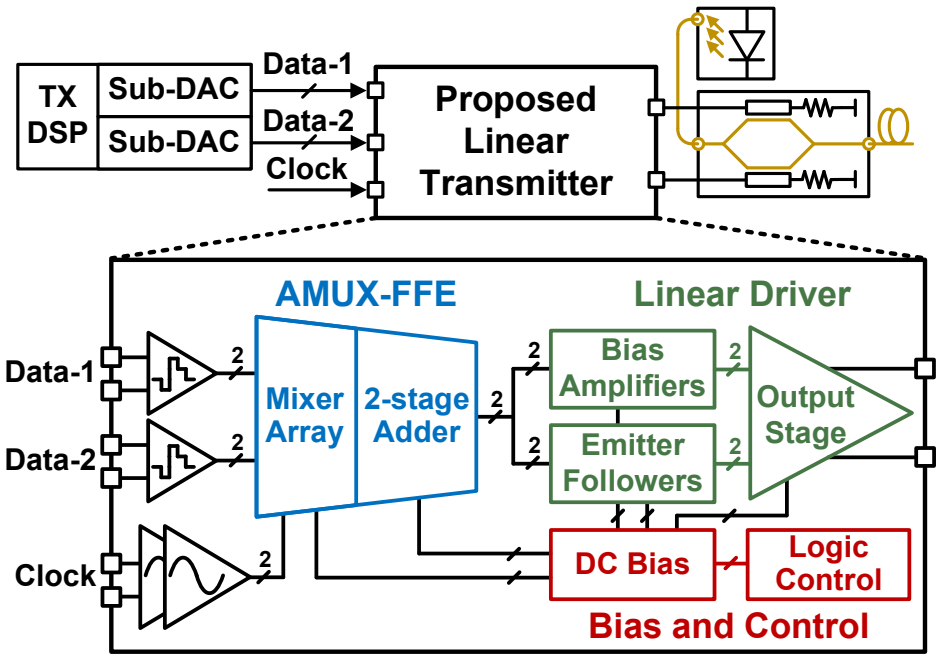


**Fig. 3.3 Architecture of the proposed linear modulator transmitter.**

Therefore, this work, for the first time, implements the AMUX, FFE and large-swing driver monolithically using SiGe BiCMOS. The FFE is achieved inherently by the AMUX during serializing process, and hence the proposed AMUX is named AMUX-FFE in the following description. The architecture of the proposed linear transmitter is depicted in Fig. 3.3. It mainly consists of a 2-to-1 AMUX-FFE, a linear driver and bias/control blocks. The two half-rate analog data inputs from the preceding two sub-DACs are separately buffered by two data buffers and delivered to the mixer array of the AMUX-FFE. An external clock signal is also applied to the mixer array via two-stages of clock buffers to support the serializing operation. The mixer array interleaves the input data and clock in current domain and at the same time generate equalization components. The outputs of the mixers are combined into an equalized full-rate data stream by a two-stage adder, which is then sent to the linear driver for amplification. In the linear driver, the input data stream is delivered to two paths. One of the paths includes cascading emitter followers, acting as a level shift to control the DC voltage of the signal as well as a buffer to isolate the large parasitics of the output stage of the linear driver from the AMUX-FFE. Another path consists of two bias amplifiers, which generate dynamic bias signals for the output stage according to the input data. 50-Ω termination resistors are implemented inside the output stage for broadband output impedance matching. After amplified by the output stage, the data is finally applied to the following optical modulator for electrical-to-optical conversion. The operations of the AMUX-FFE and driver are controlled by the bias/logic control block. With the architecture shown in Fig. 3.3, the proposed linear transmitter achieves analog serialization, large output swing and equalization simultaneously, and thus capable of not only extending the bandwidth of the DAC but also directly driving optical modulators.

## 3.3 Circuit Implementations

### 3.3.1 AMUX-FFE

Different from the digital multiplexers (MUX) widely employed in wireline transmitters

which can only be used for serializing NRZ signals, AMUX can directly serialize the analog signals such as PAM-4 without the help of decoder and encoder. And therefore, design considerations for AMUX include not only bandwidth and power consumption but also linearity. On the other hand, if using the same structure of typical digital MUX-based analog FFE [59-61] to implement the AMUX-based FFE inside the linear transmitter, the power consumption of the FFE will be quite high. This is because the latches inside the re-timer and tap generator for the AMUX-based FFE should also be capable of dealing with analog signals, and thus conventional energy-efficient CMOS logic-based latch implementation is not suitable anymore. Instead, current-mode logic (CML)-based latch implementation [62,63] becomes the only choice especially for heterojunction bipolar transistor (HBT)-based designs, resulting in high power consumption.

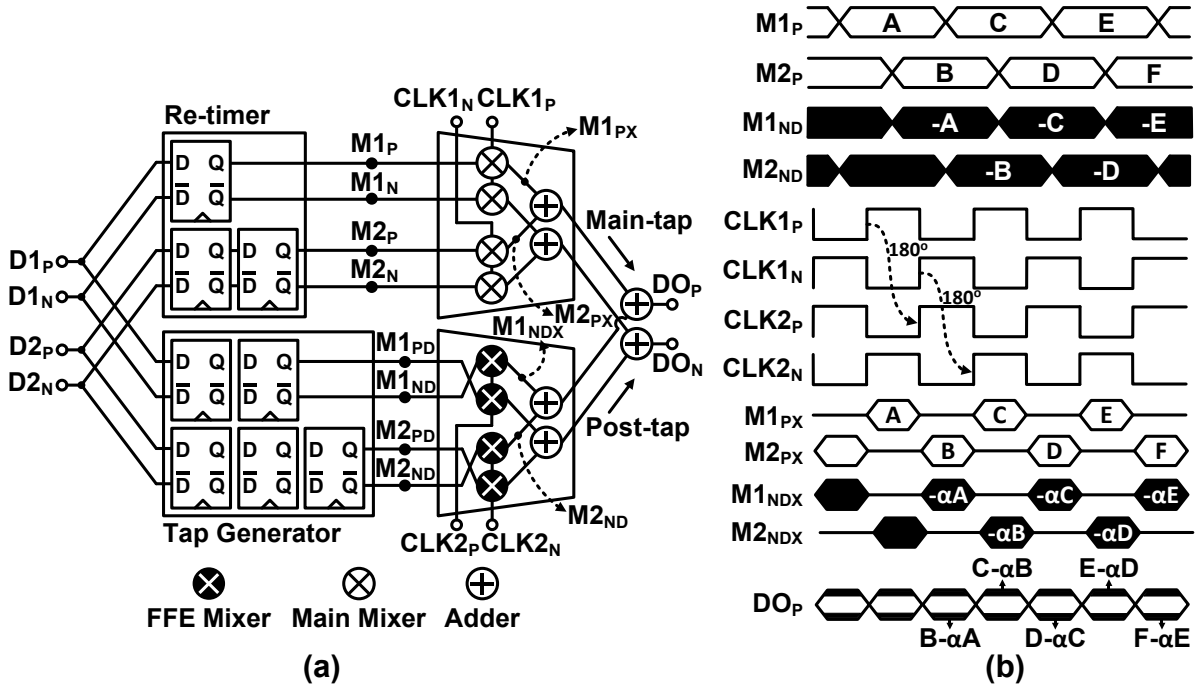


**Fig. 3.4 (a) Structure and (b) timing diagram of a conventional AMUX-based 2-tap FFE.**

To better illustrate the drawbacks of conventional AMUX-based FFE, Fig. 3.4(a) depicts an example. In addition to providing 2-to-1 analog serialization, it implements a main tap and a post-tap using one re-timer, one tap generator, and two 2-to-1 AMUXs. There are two paths inside the FFE. At the main tap path, two pairs of differential half-rate data streams denoted as

$D1_P/D1_N$ and $D2_P/D2_N$ are firstly processed by the re-timer to adjust their timing relationships. As shown in Fig. 3.4(b), re-timed $D1_P$ denoted by $M1_P$ advances re-timed $D2_P$ denoted by $M2_P$ by 1 UI. $M1_P$ and $M2_P$ are further interleaved by clock signals $CLK1_P$ and $CLK1_N$ into $M1_{PX}$ and $M2_{PX}$, respectively. At the post-tap path, $D1_P/D1_N$ and $D2_P/D2_N$ are sent to the tap generator instead of the re-timer. Compared with the re-timer, the tap generator has two more latches to provide additional delays to achieve the post-tap. Hence, $M1_{ND}$ and $M2_{ND}$ lag $M1_P$ and $M2_P$ by 1 UI, respectively. And then, $M1_{ND}$ and $M2_{ND}$ are interleaved by clock signals $CLK2_P$ and $CLK2_N$ into $M1_{NDX}$ and $M2_{NDX}$, respectively. To ensure correct interleaving, $CLK2_P$ and $CLK2_N$ lag $CLK1_P$ and $CLK1_N$ by 180° (1 UI), respectively. Thus, $M1_{NDX}$ and $M2_{NDX}$ also lag $M1_{PX}$ and $M2_{PX}$ by 1 UI, respectively. $M1_{NDX}$, $M2_{NDX}$, $M1_{PX}$ and $M2_{PX}$ are finally combined at the output of the FFE by two stages of adders into $DO_P$, which is an equalized full-rate data stream containing the information of $D1_P$ and $D2_P$. With the re-timer and tap generator made of multiple analog latches, the conventional AMUX-based FFE is power-hungry. The power overhead will scale up when more FFE taps are needed. Moreover, the re-configurability of this FFE implementation is poor. For example, the tap spacing between the main tap and post-tap are determined by the timing relationship between the re-timer and tap generator as well as that between $CLK1_P/CLK1_N$ and $CLK2_P/CLK2_N$, and hence can hardly be adjusted.

To reduce the power consumption of the AMUX-based FFE, [56] proposes a 4-to-1 AMUX with inherent equalization. The 4-to-1 AMUX consists of two stages of 2-to-1 AMUXs. In each 2-to-1 AMUX, two straight-through paths are introduced in addition to the two interleaving paths. The signals from the four paths are combined at the output of the 2-to-1 AMUX by a summer. By controlling the gain relationship between the interleaving and straight-through paths, the 2-to-1 AMUX can be configured to either emphasized mode, de-emphasized mode or emphasis-off mode. In the emphasized mode, the 2-to-1 AMUX achieves analog serialization and 2-tap FFE simultaneously. The 2-tap FFE includes one main tap and one post tap. As no tap generator is needed, the power and hardware cost of the FFE is

reduced compared to the conventional method. However, the re-configurability is still not good enough. For one thing, the spacings between the taps are fixed to 1 UI. For another thing, the conformation of the FFE cannot be changed. The application of the proposed design is thereby constrained.

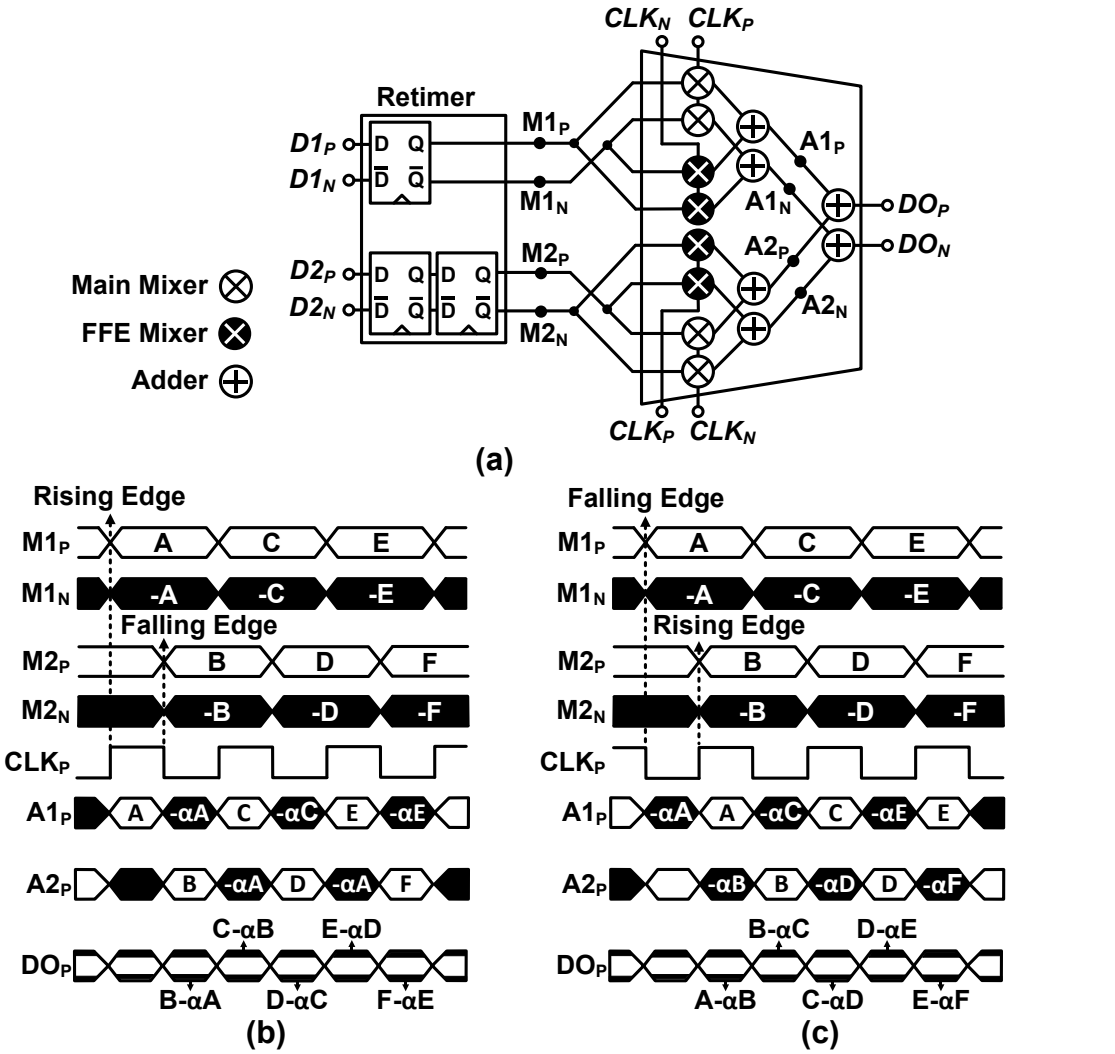


**Fig. 3.5 (a) Structure of the proposed AMUX-FFE, (b) timing diagram of the AMUX-FFE configured into one main tap and one post-tap with a $TS_{MPO}$ of 1 UI, and (c) timing diagram of the AMUX-FFE configured into one main tap and one pre-tap with a $TS_{PRM}$ of 1 UI.**

In view of the issues, this work proposes an AMUX-FFE. In addition to achieving 2-to-1 analog serialization, it can provide either a 2-tap UI-spaced FFE or a 3-tap fractional-spaced

FFE. For the 2-tap UI-spaced mode, the AMUX-FFE can be configured into one main tap and one pre-tap or one main tap and one post-tap, with 1-UI tap spacing. For the 3-tap fractional-spaced mode, the AMUX-FFE can be configured into one pre-tap, one main tap, and one post-tap. To simplify the description, the tap spacing between the pre-tap and main tap is denoted by $TS_{\mathrm{PRM}}$, and the tap spacing between the main tap and post-tap is denoted by $TS_{\mathrm{MPO}}$. In the 3-tap factional-spaced mode, the tap spacings $TS_{\mathrm{PRM}}$ and $TS_{\mathrm{POM}}$ can be adjusted by adjusting the timing relationship between the clock signals and input data streams. And the following equation always holds true.

$$TS_{\mathrm{PRM}} + TS_{\mathrm{MPO}} = 1 \text{ UI} \tag{3.5}$$

while $0 < TS_{\mathrm{PRM}} < 1$ UI and $0 < TS_{\mathrm{MPO}} < 1$ UI.

Fig. 3.5(a) depicts the structure of the proposed AMUX-FFE. Compared with the conventional implementation in Fig. 3.4(a), there is no tap generator, and hence the required latch number significantly decreases from eight to three to reduce the power consumption as well as the die area overhead.

Fig. 3.5(b) illustrates the timing diagram of the proposed AMUX-FFE when it is configured into one main tap and one post-tap with 1-UI tap spacing. In this configuration, the rising edges of the clock signal $CLK_{\mathrm{P}}$ are aligned with the starting transitions of the re-timed input differential data streams $M1_{\mathrm{P}}/M1_{\mathrm{N}}$, while the falling edges of $CLK_{\mathrm{P}}$ are aligned with the starting transitions of the re-timed input differential data stream $M2_{\mathrm{P}}/M2_{\mathrm{N}}$. Each of the four data streams is sent to both the main mixer and FFE mixer where it is interleaved with clock signals. When $CLK_{\mathrm{P}}$ is high, $M1_{\mathrm{P}}$ and $M2_{\mathrm{N}}$ are sampled by $CLK_{\mathrm{P}}$-controlled mixers to $A1_{\mathrm{P}}$ and $A2_{\mathrm{P}}$, respectively. When $CLK_{\mathrm{P}}$ is low, $M1_{\mathrm{N}}$ and $M2_{\mathrm{P}}$ are sampled by $CLK_{\mathrm{N}}$-controlled mixers to $A1_{\mathrm{P}}$ and $A2_{\mathrm{P}}$, respectively. Therefore, both $A1_{\mathrm{P}}$ and $A2_{\mathrm{P}}$ have one-bit positive and one-bit negative information for every sampled data, and the amplitudes of negative bits are weighted by a coefficient of α which is determined by the gain ratio of the FFE mixer over main mixer. And then, $A1_{\mathrm{P}}$ and $A2_{\mathrm{P}}$ are combined by the adder into $DO_{\mathrm{P}}$, which is the same as the one

generated by a UI-spaced FFE composed of one main tap and one post-tap, with α as the coefficient of the post-tap.

For the configuration with one pre-tap and one main tap and a tap spacing of 1 UI, as shown in Fig. 3.5(c), the falling edges of $CLK_P$ are aligned with the starting transitions of $M1_P/M1_N$, while the rising edges of $CLK_P$ are aligned with the starting transitions of $M1_P/M1_N$. The interleaving operations are the same with those of Fig. 3.5(b). After interleaving, $A1_P$ contains both positive and negative information of $M_1$, while $A2_P$ contains both positive and negative information of $M_2$. Still, all the negative bits are multiplied by a coefficient α which is determined by the gain ratio of the FFE mixer over main mixer. However, different from the configuration of Fig. 3.5(b), in this configuration, the negative bits advance their corresponding positive bits for both $A1_P$ and $A2_P$. And therefore, $DO_P$ is the same with the output of a UI-spaced FFE composed of one pre-tap and one main tap, with α as the coefficient of the pre-tap.

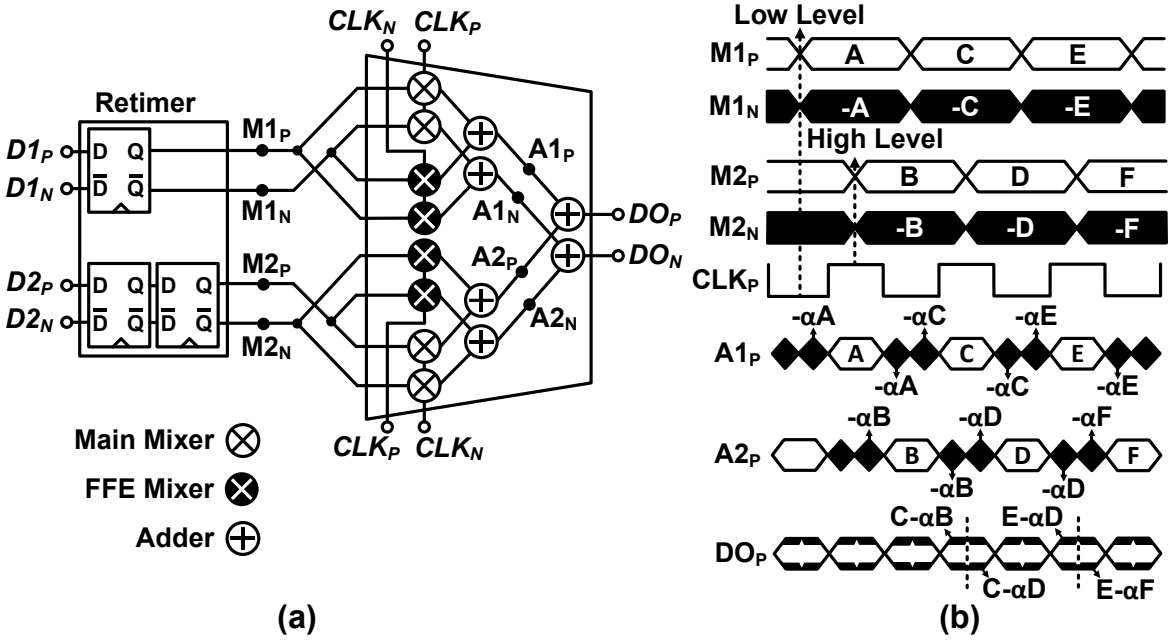


**Fig. 3.6 (a) Structure of the proposed AMUX-FFE, and (b) timing diagram of the AMUX-FFE configured into one pre-tap, one-main, and one pre-tap with both $TS_{PRM}$ and $TS_{MPO}$ equaling 0.5 UI.**

As mentioned above, the proposed AMUX-FFE can also be configured into fractional-spaced FFE with one pre-tap, one main tap, and one post-tap. Fig. 3.6 depicts an example where the tap spacings $TS_{PRM}$ and $TS_{MPO}$ are both equal to 0.5 UI. In this configuration, the middle points of the low levels of $CLK_P$ are aligned with the starting transitions of $M1_P/M1_N$, while the middle points of the high levels of $CLK_P$ are aligned with the starting transitions of $M2_P/M2_N$. Still, both $A1_P$ and $A2_P$ have one-bit positive and one-bit negative information for every sampled data, with the negative bits multiplied by a coefficient α which is determined by the gain ratio of the FFE mixer over main mixer. Nevertheless, as the timing relationship between the clock signals and data streams change, the components of $A1_P$ and $A2_P$ are different from those in Fig. 3.5(b) and Fig. 3.5(c). In this configuration, all the negative bits are separated in half by the positive bits. Therefore, $DO_P$ added by $A1_P$ and $A2_P$ is the same as the output provided by a 0.5 UI-spaced FFE composed of one pre-tap, one main-tap and one post-tap, with α as the coefficients of both the pre-tap and post-tap.

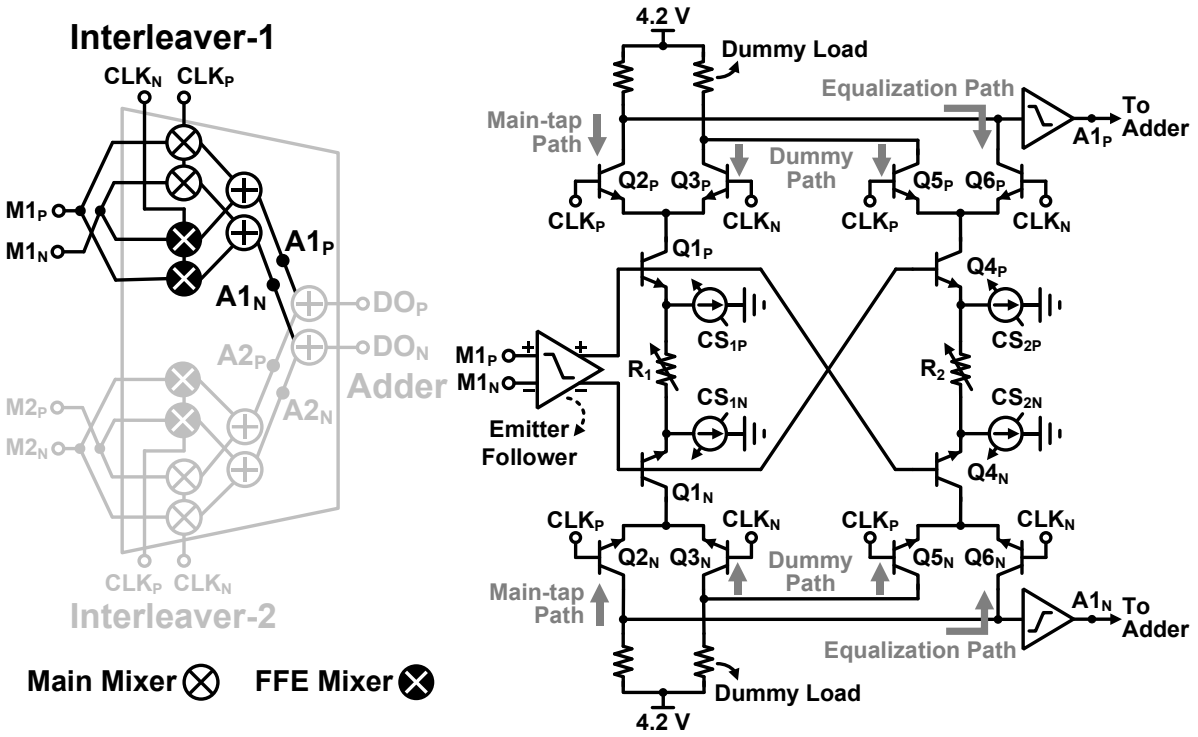


**Fig. 3.7 Half-schematic of the interleaver inside the AMUX-FFE.**

Regarding the transistor-level implementation of the proposed AMUX-FFE, it consists of

two interleavers and one adder. Fig. 3.7 shows the schematic of the interleaver. The re-timed differential data streams $M1_P/M1_N$ are firstly buffered by an emitter follower which is used for shielding the input ports of the AMUX-FFE from the input pads of the chip to enhance the bandwidth. Following the emitter follower, four mixers are implemented to interleave the data with clock signals. The mixers formed by $Q1_{P/N}$, $Q2_{P/N}$, and $Q3_{P/N}$ are the main mixers, while those formed by $Q4_{P/N}$, $Q5_{P/N}$, $Q6_{P/N}$ are FFE mixers. The mixing is performed in current domain. Dummy paths are implemented in each mixer to eliminate the charge sharing effect. To elaborate the principle of the dummy path, the main mixer formed by $Q_{1P}$, $Q_{2P}$ and $Q_{3P}$ is taken as an instance. When $CLK_P$ is high, $M1_P$ at the base of $Q1_P$ is sampled to the $A1_P$ through $Q2_P$, and the dummy path is turned off as $Q3_P$ is turned off by $CLK_N$ which is low. When $CLK_P$ is low, $Q2_P$ is turned off. Ideally, at this time, the data transition at the base of $Q1_P$ will not affect the signal at the collector of $Q_{2P}$. However, in practice, without the dummy path, if $M1_P$ transits from high to low, the charge stored at the collector of $Q_{1P}$ will be leaked to the ground, inducing voltage variation at the collector of $Q2_P$. With the dummy path, the collector of $Q_{1P}$ is charged by the $Q_{3P}$ and fixed to a certain DC voltage when $CLK_P/CLK_N$ are low/high, and thus the change of $M1_P$ will not affect the collector of $Q_{2P}$ anymore. During serialization operations, the main mixers and FFE mixers are switched on alternatively. The gain ratio of the two types of mixers determines the equalization strength of the FFE, i.e. the coefficient α mentioned above. The gain of each mixer can be tuned by its tail current source and degenerated variable resistor. Outputs from the main mixers and FFE mixers are eventually added at the resistor loads in current and then buffered by emitter followers to the adder.

The schematic of the adder is depicted in Fig. 3.8. The signals $A1_{P/N}$ and $A2_{P/N}$ from the preceding interleavers are firstly converted by $Q1_{P/N}$ and $Q2_{P/N}$ from voltage mode to current mode. The converted signals are added at the emitter of $Q3_{P/N}$. $Q3_{P/N}$ is implemented to improve the tolerant voltage of the adder as well as relieve the Miller effect. The outputs of the adder denoted by $DO_P$ and $DO_N$ are delivered to the linear driver for amplification.

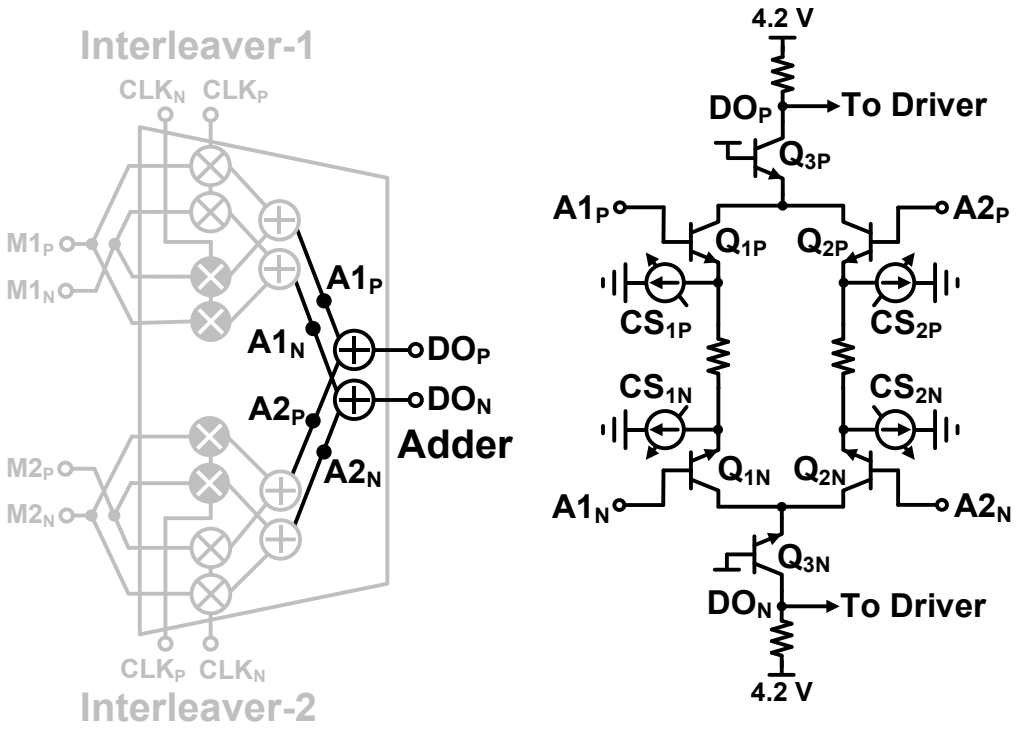


**Fig. 3.8 Schematic of the adder inside the AMUX-FFE.**

### 3.3.2 Linear Driver

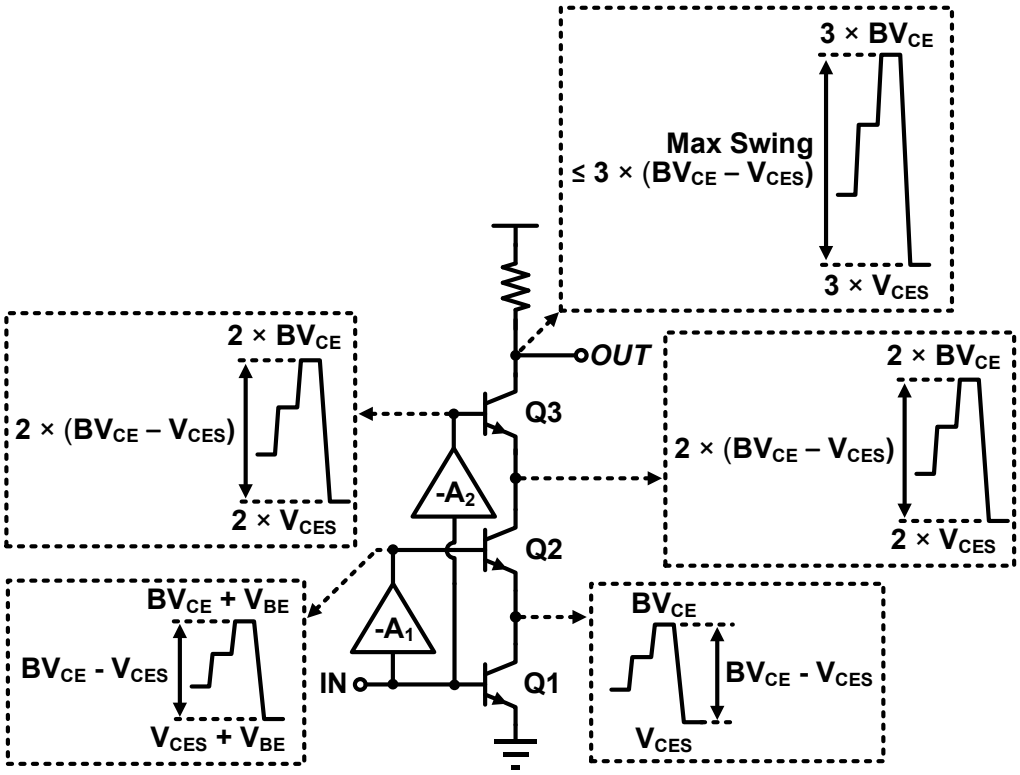


**Fig. 3.9 Illustration of the proposed dynamic triple-stacked driver topology.**

As described above, compared with the conventional cascode structure showin in Fig. 3.1(a), the BV doubler shown in Fig. 3.1(b) doubles the maximum output swing without incurring any breakdown issues. Based on the BV doubler, this work proposes a dynamic triple-stacked driver topology to further enhance the output swing. Fig 3.9 depicts the simplified schematic of the proposed driver topology. At the output stage, three transistors denoted by Q1, Q2, and Q3 are stacked. The main feature of this topology is that both the bases of Q2 and Q3 are dynamically biased. To simplify the following description, it is assumed the sizes, $BV_{CE}$, and $V_{CES}$ of Q1, Q2 and Q3 are the same. $BV_{CE}$ is the collector-emitter breakdown voltage of those HBTs, and $V_{CES}$ is the minimum collector-emitter voltage to prevent those HBTs from saturation region.

For Q2, an auxiliary amplifier denoted by $A_1$ is connected to its base to swing its base and emitter voltages. The gain of $A_1$ should be properly designed, so that

$$SW_{Q2B} = SW_{Q2E} = BV_{CE} - V_{CES} \tag{3.6}$$

where $SW_{Q2B}$ and $SW_{Q2E}$ denote the base and emitter voltage swings of Q2, respectively. Moreover, the output common-mode voltage of $A_1$ should also be properly set, such that the high level and low level of the emitter voltage of Q2 equal $BV_{CE}$ and $V_{CES}$, respectively, to protect Q1 from breakdown and saturation.

Different from BV doubler, in the proposed topology, as there is one more stacked transistor Q3, another auxiliary amplifier denoted by $A_2$ is introduced. The gain of $A_2$ should be twice that of $A_1$, to obtain

$$SW_{Q3B} = SW_{Q3E} = 2 \times (BV_{CE} - V_{CES}) \tag{3.7}$$

where $SW_{Q3B}$ and $SW_{Q3E}$ denote the base and emitter voltage swings of Q3, respectively. Furthermore, to prevent Q2 from breakdown and saturation, the high level and low level of the emitter voltage of Q3 should equal $2 \times BV_{CE}$ and $2 \times V_{CES}$, respectively.

With Q2, Q3, and two auxiliary amplifiers $A_1$ and $A_2$, the maximum output swing of the proposed driver topology denoted by $SW_{DTS}$ can be enhanced to

$$SW_{\mathrm{DTS}} = 3 \times (BV_{\mathrm{CE}} - V_{\mathrm{CES}}) \tag{3.8}$$

without breakdown issues. $SW_{\mathrm{DTS}}$ is 1.5 times the swing of BV doubler and 3 times the swing of cascode structure. Additionally, when operated for the same output swing, the collect-emitter voltage variation of every output-stage HBT of the proposed driver topology will be smaller than that of BV doubler and cascode structure, and hence a better linearity can be achieved.

However, in practical implementations, there are several issues for the proposed driver to be addressed. Firstly, the introductions of $A_1$ and $A_2$ will increase the parasitics at the input port of the driver, resulting in the degradation of the bandwidth. Secondly, $A_2$ should be properly designed to avoid breakdown, as its required output swing is already twice the swing of the cascode structure. Thirdly, there are multiple paths inside the proposed driver from the input port to output port. The delays of those paths are supposed to be the same to avoid distortion of the output signal. The solutions for those issues will be elaborated in the following.

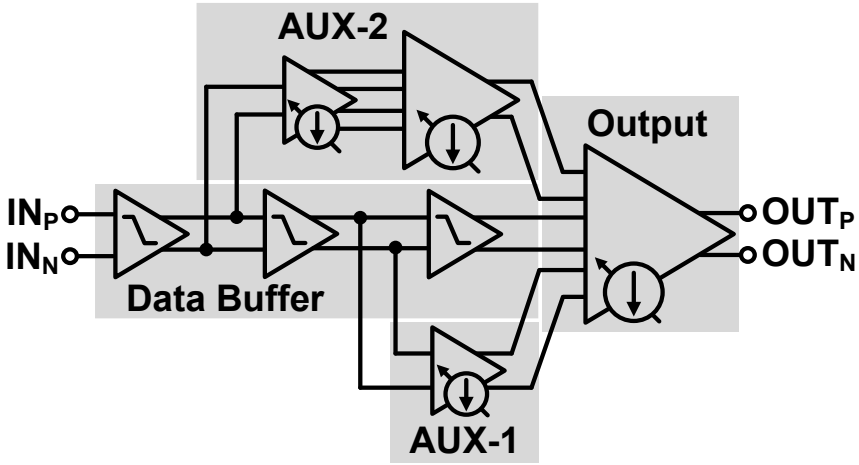


**Fig. 3.10 Block diagrams of the proposed dynamic triple-stacked driver.**

Fig. 3.10 depicts the block diagram of the proposed driver. To relieve the bandwidth degradation due to the two auxiliary amplifiers, a 3-stage data buffer is implemented to deliver the input differential signals to auxiliary amplifier-1 (AUX-1), auxiliary amplifier-2

(AUX-2) and output stage. The outputs of the first stage of the data buffer are fed to AUX-2, and those of the second stage of the data buffer are delivered to AUX. Finally, the output of the third stage of the data buffer is sent to the output stage. Each stage of the data buffer is simply a differential emitter follower composed of HBTs. As the output impedance of emitter follower is small, the time constant of the input ports of AUX-1, AUX-2, and output stage can be reduced. In this way, the impact from the two auxiliary amplifiers on the bandwidth of the driver can be effectively relieved. Moreover, with the data buffer, the common-mode voltages of the input signals for AUX-1, AUX-2, and output stage can be properly set.

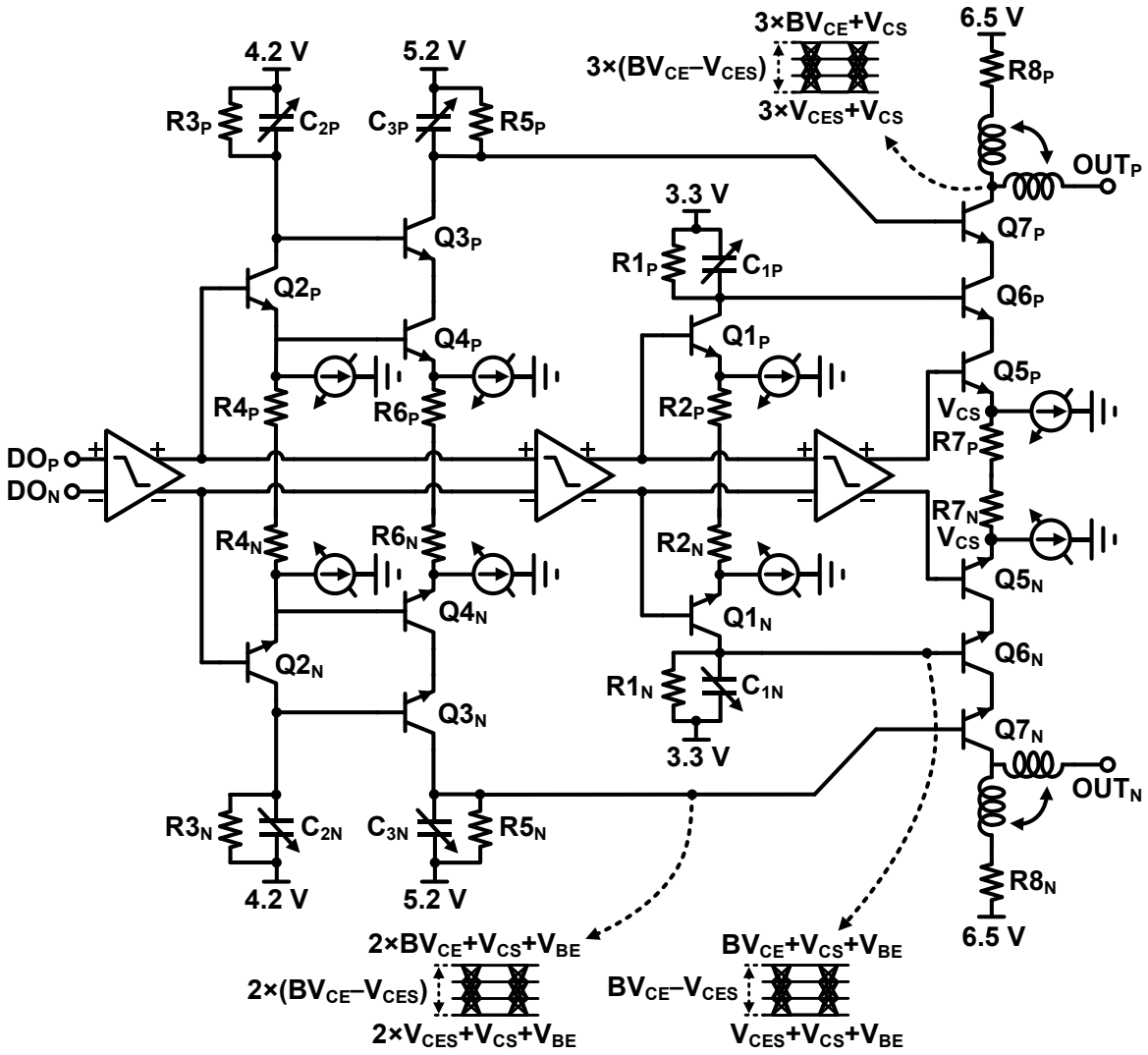


**Fig. 3.11 Schematic of the proposed linear driver.**

The detailed transistor-level implementation of the proposed driver is shown in Fig. 3.11.

AUX-1 mainly consists of a differential HBT pair $Q1_{P/N}$, load resistors $R1_{P/N}$, degenerated resistors $R2_{P/N}$, and varactors $C1_{P/N}$. AUX-1 adopts a common-emitter topology to achieve the swing requirement of $BV_{CE}$ - $V_{CES}$, with a supply voltage of 3.3 V. For AUX-2, since the required output swing is as high as 2 × ($BV_{CE}$ - $V_{CES}$), an optimized BV doubler structure is employed. It incorporates two stages. The first stage is formed by a differential HBT pair $Q2_{P/N}$, load resistors $R3_{P/N}$, degenerated resistors $R5_{P/N}$, and varactors $C2_{P/N}$, with a supply voltage of 4.2 V, while the second stage consists of $Q3_{P/N}$, $Q4_{P/N}$, load resistors $R5_{P/N}$, degenerated resistors $R6_{P/N}$, and varactors $C3_{P/N}$, with a supply voltage of 5.2 V. The emitters of $Q2_{P/N}$ are connected to the bases of $Q4_{P/N}$ to buffer the input signal, while the collectors of $Q2_{P/N}$ are connected to the bases of $Q3_{P/N}$ for dynamic biasing. Therefore, the first stage of AUX-2 functions not only as an emitter follower but also as an auxiliary amplifier. Compared with BV doubler [50] where the emitter follower and auxiliary amplifier are two separate stages, the enhanced BV doubler used in the proposed driver merges two stage and hence can achieve a better power efficiency. The output stage mainly incorporates $Q5_{P/N}$, $Q6_{P/N}$, $Q7_{P/N}$, degenerated resistors $R7_{P/N}$, load resistors $R8_{P/N}$, and two T-coils, with a supply voltage of 6.5 V. The values of $R8_{P/N}$ are 50 Ω for output impedance matching. The outputs of AUX-1 and AUX-2 are delivered to the bases of $Q6_{P/N}$ and $Q7_{P/N}$, respectively, to create demanded signal swings at the emitters of $Q6_{P/N}$ and $Q7_{P/N}$. Since the sizes of $R8_{P/N}$ are large to deliver the large amount of current, the T-coils are implemented at the output port of the driver to cancel the parasitics from $R8_{P/N}$ as well as $Q7_{P/N}$ for bandwidth extension.

An important concern for the proposed driver topology is that the introductions of the two auxiliary amplifiers create three more paths from the input port to output port in addition to the main path, as illustrated in Fig. 3.12. The delay of those four paths should be the same, otherwise, the output signal will be degraded with severe kinks [50]. Path-1 from node A via node B, node C, node I, and node J to the output node K is the main path of the driver. AUX-1 introduces path-2, which goes through node A, node B, node D and node J to the output node K. Obviously, the delay of path-2 is larger than that of path-1, as path-2 travels through one

more emitter follower, and Q5 acting as a degeneration component for Q6 further enlarges the discrepancy between path-1 and path-2. Therefore, a varactor denoted by C1 is inserted in paralleled with the load resistor of AUX-1 to slow down the signal traveling through path-2. Similarly, AUX-2 introduces path-3 and path-4 from the input port to output port. Therefore, varactors C2 and C3 are inserted in the loads of the first and the second stages of AUX-2, respectively. C2 is for matching the delays between path-3 and path-4, so that the bias signal generated by AUX-2 will not be distorted. And C3 is implemented to further mitigate the delay discrepancy between path-1, path-3 and path-4.

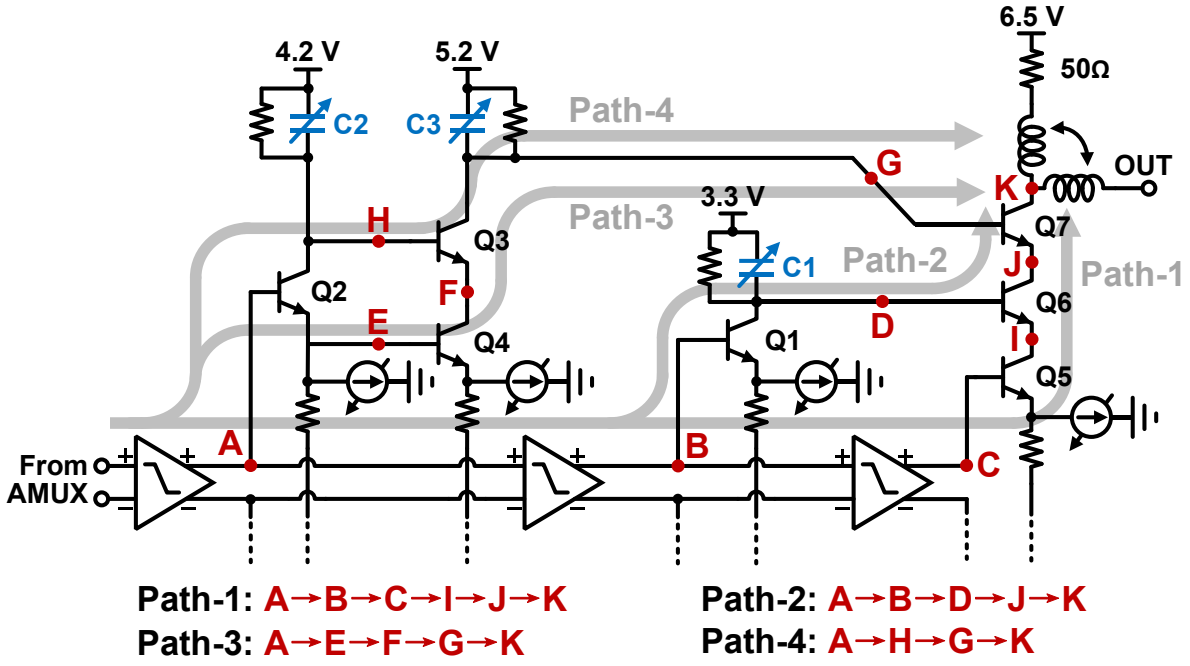


**Fig. 3.12 Illustration of the path delay mismatch issue.**

## 3.4 Measurement Setups and Results

The proposed transmitter is fabricated in 130-nm SiGe BiCMOS technology with $f_T$ and $f_{MAX}$ of 250 GHz and 340 GHz, respectively. Fig. 3.13(a) shows the die photo of the transmitter, where the core occupies a die area of 0.33 $mm^2$. To facilitate the characterization of the linear driver, a standalone linear driver chip has also been fabricated. Its die photo is shown in Fig. 3.13(b), with a core area of 0.22 $mm^2$.

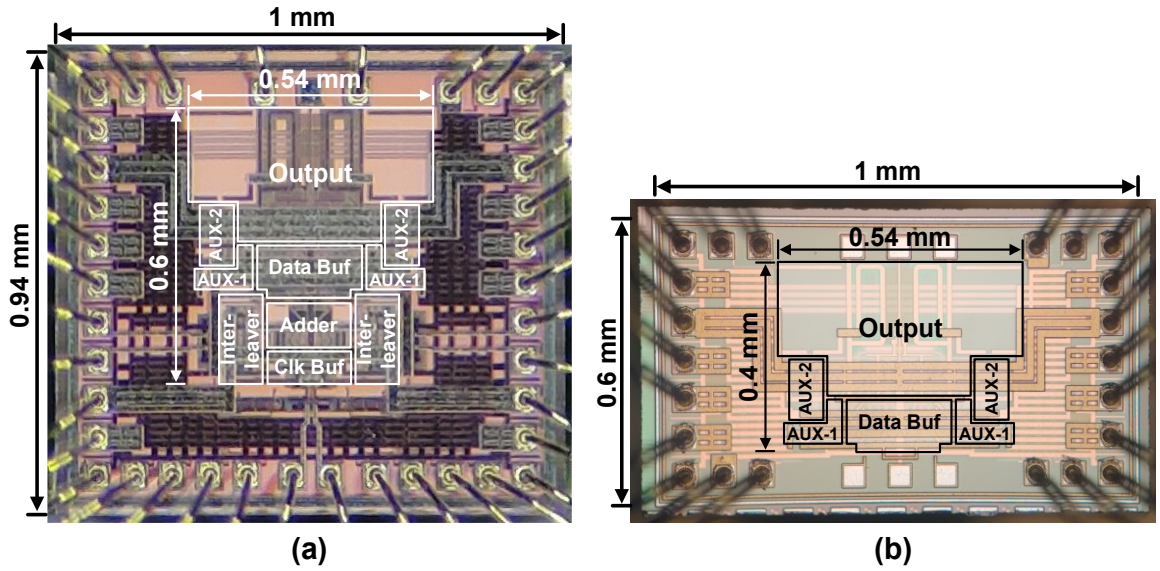


**Fig. 3.13 Die micrographs of (a) the whole modulator transmitter and (b) the standalone linear driver.**

### 3.4.1 Measurement Setups and Results for the Standalone Linear Driver

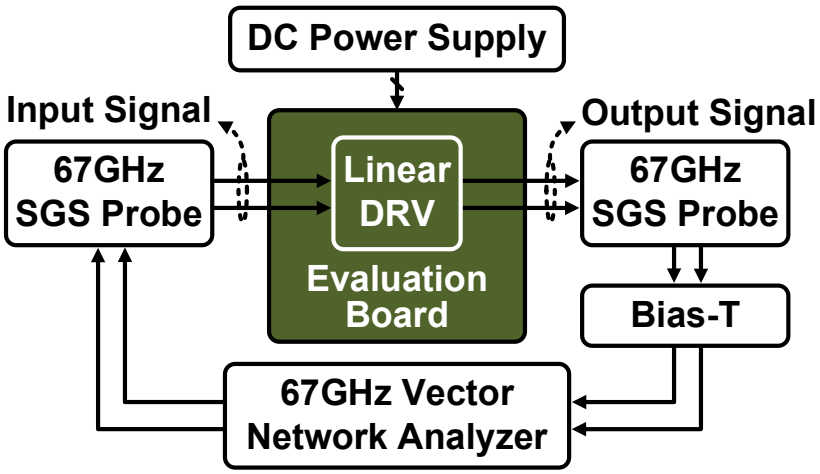


**Fig. 3.14 Frequency-domain measurement setup for the standalone linear driver chip.**

Fig. 3.14 shows the setup for frequency-domain measurements of the linear driver chip. The driver chip is mounted on a high-frequency evaluation board (EVB). DC pads of the chip, including those for power supply, controlling and biasing, are all wire-bonded to EVB. A 67-GHz vector network analyzer (VNA) is adopted to generate the input differential signals for the driver and analyze the output differential signals from the driver. The model of the

VNA is Keysight N5227B. To get rid of the parasitic effects from bond-wires, traces of evaluation boards, and SMA connectors for accurate performance characterization, the input signals are fed to the driver via a 67-GHz signal-ground-signal (SGS) probe. The output signals from the driver are sent to the VNA also through a 67-GHz SGS probe. A pair of bias-T are utilized to set the common-mode voltage for the output port of the driver.

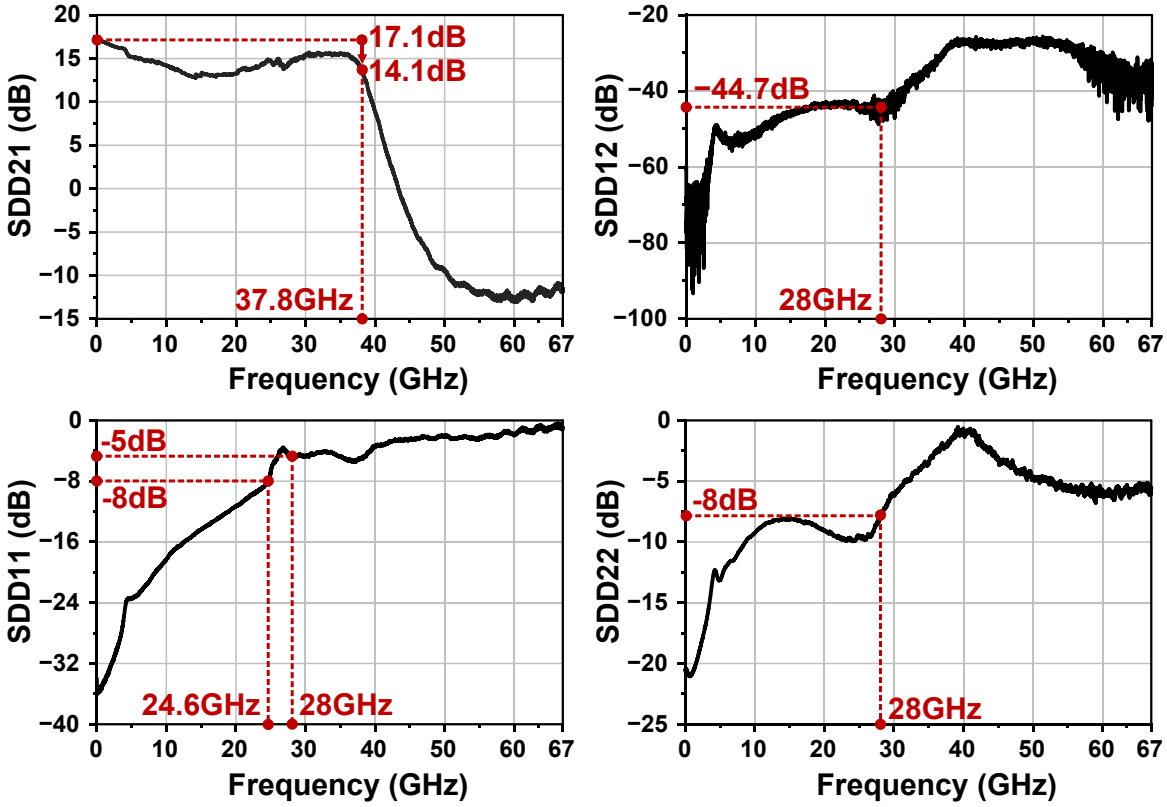


**Fig. 3.15 Measured S-parameters of the linear driver chip.**

Fig. 3.15 shows measured S-parameters of the linear driver. As demonstrated by the SDD21 curve which describes the forward gain characteristics, the linear driver achieves a DC gain of 17.1 dB. The DC gain rolls off to 14.1 dB at a frequency of 37.8 GHz, indicating that the 3-dB bandwidth of the driver is 37.8 GHz. For the reverse gain, the SDD12 of the driver is as low as -44.7 dB at the Nyquist frequency of 28 GHz, indicating a good reverse isolation performance. The input and output reflection performances are characterized by SDD11 and SDD22 curves, respectively. The driver achieves an input return loss smaller than -8 dB from DC to 24.6 GHz, and it achieves an output return loss smaller than -8 dB from DC

to 28 GHz. The input reflection performance is mainly degraded by the large-size input transistors of the driver which bring severe parasitic capacitance contributing to the sharp decrease of the input impedance with the increase of frequency. It is noted that this issue will be relieved for the whole transmitter chip. This is because the sizes of the input transistors of the AMUX are much smaller than those of the driver. Additionally, as described above, data buffers and clock buffers made of emitter followers are implemented to further isolate the input pads with the inputs of AMUX.

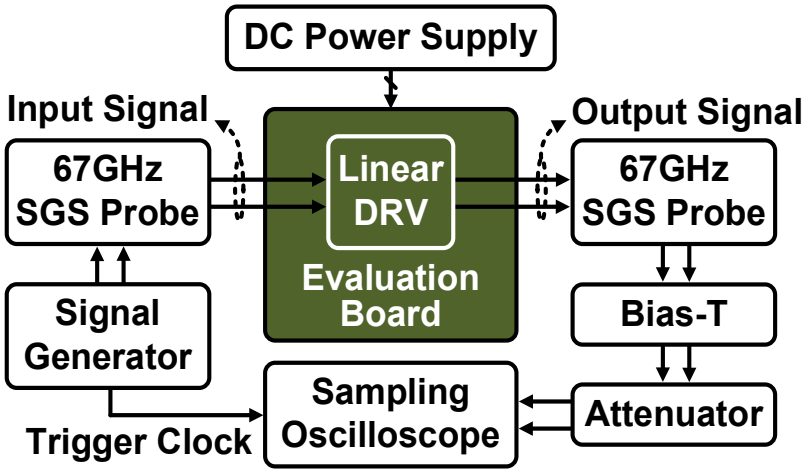


**Fig. 3.16 Time-domain measurement setup for the standalone linear driver chip.**

For time-domain measurement, as shown in Fig. 3.16, the driver chip is mounted on the EVB with all DC pads wire-bonded to the EVB. A signal generator (Keysight M8040) is used to generate pseudo-random binary sequence (PRBS) signal which is applied to the driver via a 67-GHz SGS probe. The large-swing output signal of the driver is sent off-chip through a 67-GHz SGS probe, and a pair of bias-T is deployed to define the common-mode voltage for the output port of the driver. A sampling oscilloscope (Keysight N1060A) is used to capture the output signal of the driver for eye diagram observations. To prevent the input ports of the oscilloscope from saturation, a pair of attenuators with forward gains of approximately -32 dB are inserted between the bias-T and oscilloscope to shrink the signal swing.

Fig. 3.17 shows measured eye diagrams of the differential output signal of the driver. As

demonstrated in Fig. 3.17(a) and Fig. 3.17(b), the driver supports amplifications of 50-Gbaud NRZ and PAM-4 signals with differential output swings of 7.6 $V_{ppd}$ and 6.9 $V_{ppd}$, respectively. Both eye diagrams are clearly opened. And their signal patterns are both PRBS-13. For higher-speed cases, the driver achieves 7.3-$V_{ppd}$ 60-Gbaud NRZ output and 6.7-$V_{ppd}$ 60-Gbaud PAM-4 output. For the 60-Gbaud PAM-4 output, the eye diagram is noisy, due to inadequate bandwidth of the driver.

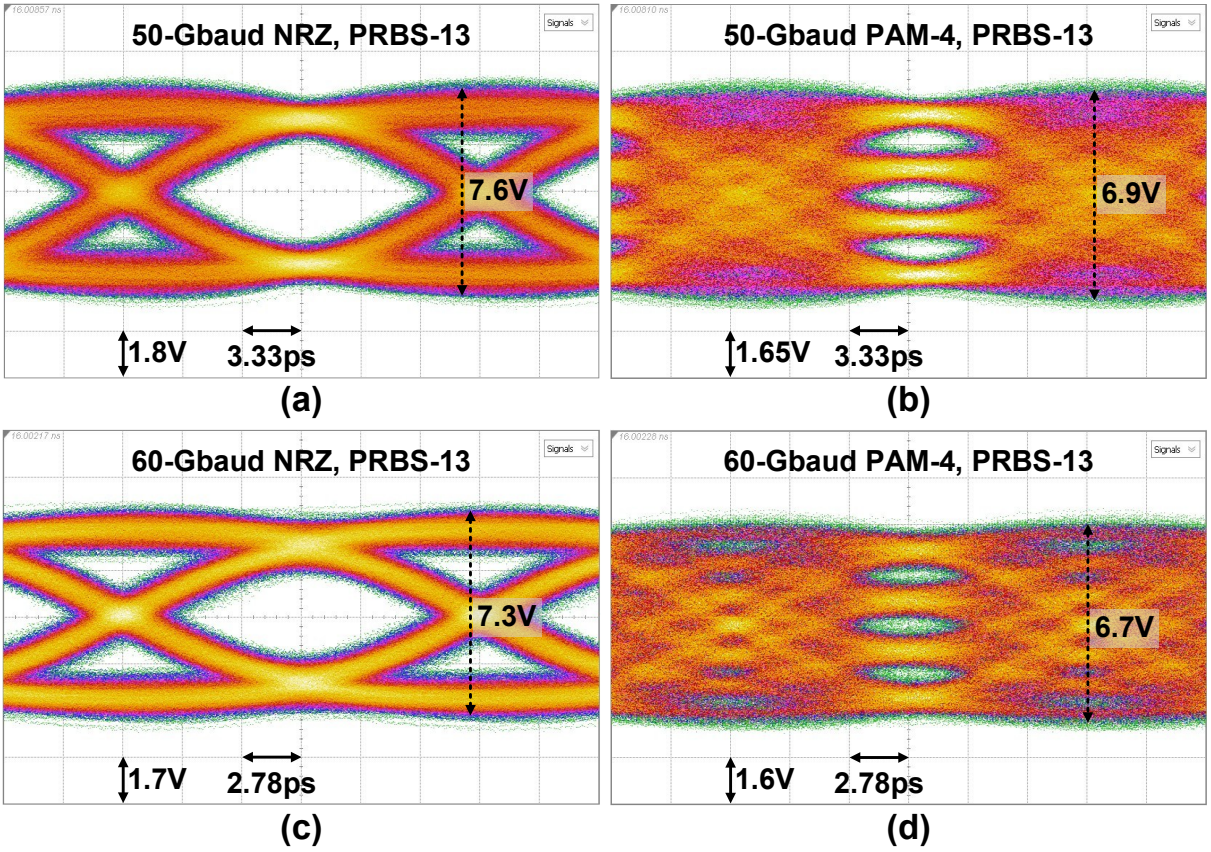


**Fig. 3.17 Measured eye diagrams of the output signal of the linear driver chip at (a) 50-Gbaud NRZ, (b) 50-Gbaud PAM-4, (c) 60-Gbaud NRZ, and (d) 60-Gbaud PAM-4.**

To evaluate the linearity of the driver, total harmonic distortion (THD) measurement has also been performed. The setup for the THD measurement is basically the same with that shown in Fig. 3.16, except that the signal generator replaced from Keysight M8040 to Keysight M8196A, as the former cannot generate sinusoidal signals. The frequency of the sinusoidal input is 1 GHz. The sinusoidal output from the driver is captured by the

oscilloscope, where Fourier transform is performed to obtain the harmonics of the signal. Fig. 3.18 shows the measured THDs with sinusoidal inputs of different swings. With the increase of the input swing, the output swing increases, and THD degrades due to non-linearity of the driver. When the swing of the output signal is 6 $V_{ppd}$, the THD is 1.6%, which can well satisfy the linearity requirement for 16 quadrature amplitude modulation (QAM) coherent optical communications [52].

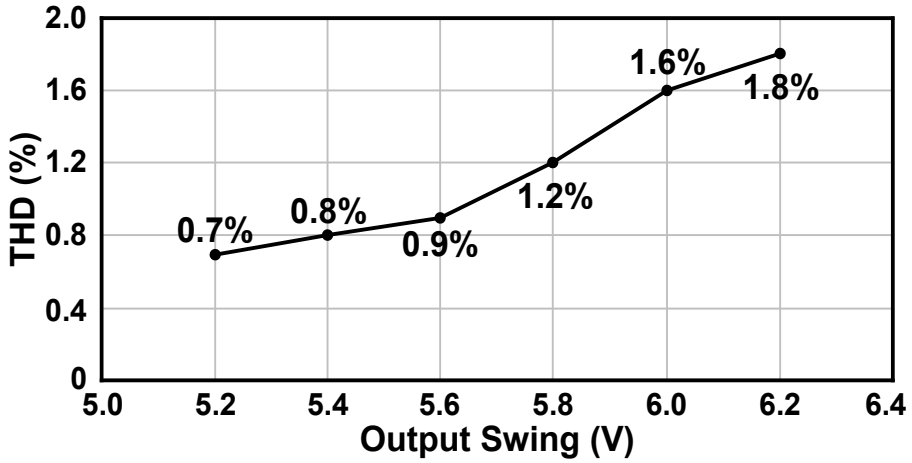


**Fig. 3.18 Measured THDs of the linear driver chip at different output swings.**

### 3.4.2 Measurement Setup and Results for the Whole Transmitter

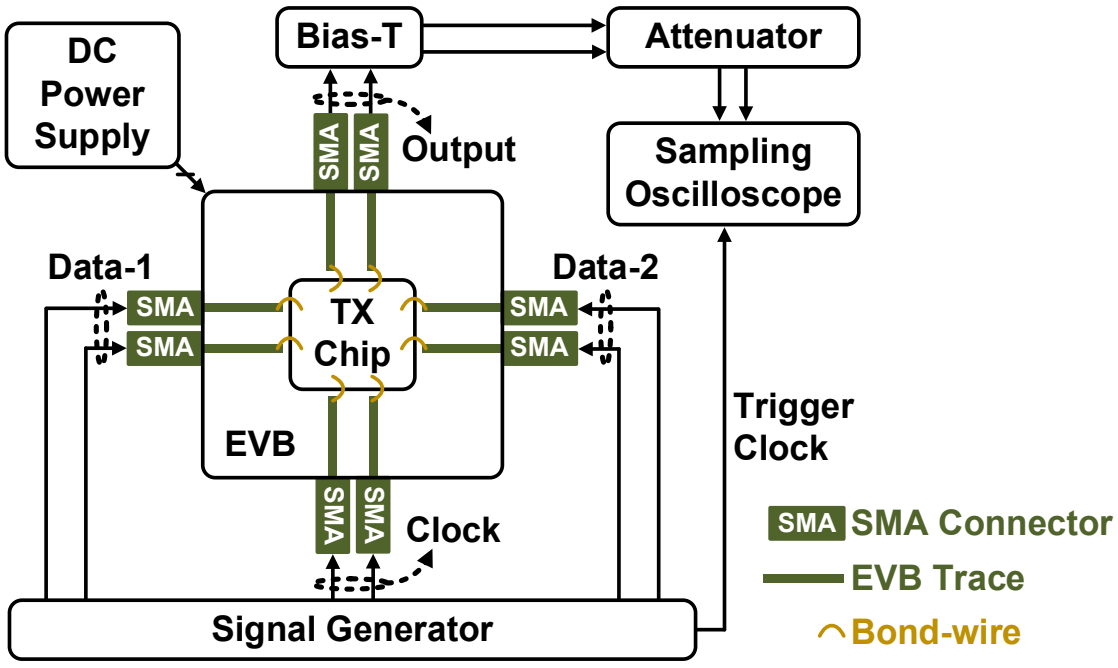


**Fig. 3.19 Measurement setup for the whole linear modulator transmitter.**

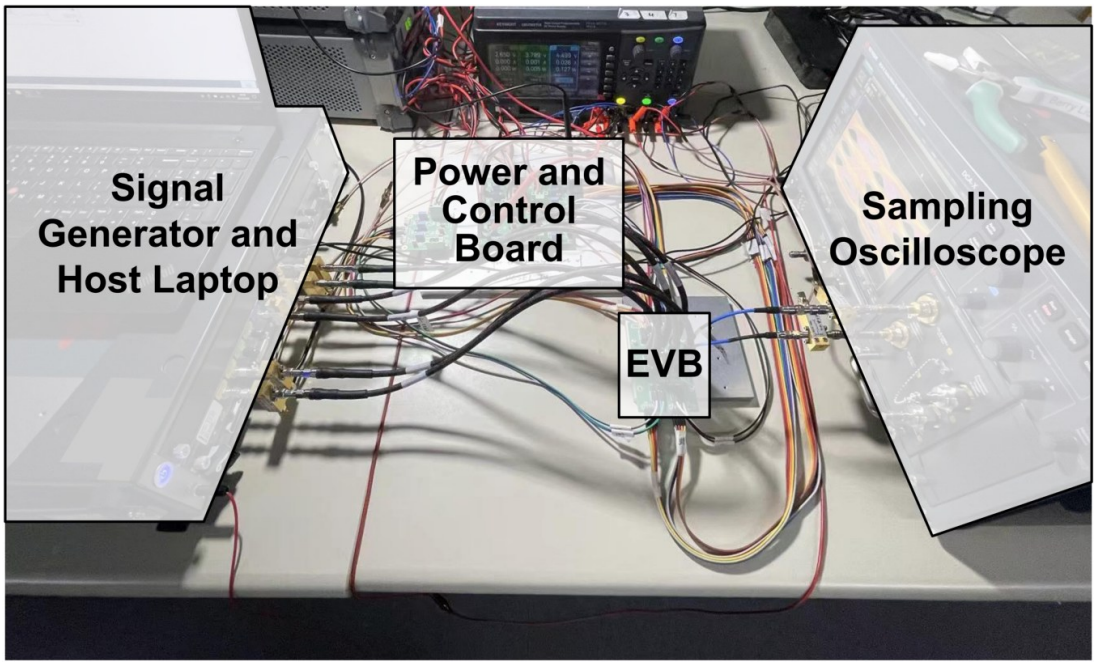


**Fig. 3.20 Photo of the measurement environment for the whole transmitter.**

Fig. 3.19 presents the measurement setup for the whole linear modulator transmitter chip. The transmitter chip is mounted on an evaluation board. All the DC pads, including those for power supplying, biasing and controlling, are wire-bonded to the EVB. Moreover, all the RF pads including those for input data, clock, and output data are also wire-bonded to the EVB, to get the measurement conditions close to practical application scenarios of the chip. An arbitrary signal generator (Keysight M8196A) is adopted to generate two half-rate data streams (Data-1 and Data-2) and clock signal for the transmitter. The timing relationships between Data-1, Data-2, and clock signal are set by the signal generator. The data and clock signals are fed to the transmitter chip through cables, 1.85-mm SMA (Sub-Miniature version A) connectors, PCB traces, and bond-wires. The losses of the cables are de-embedded before the measurement, while those of the assembly elements including SMA connectors, PCB traces and bond-wires are not. Therefore, the losses of those assembly elements will be reflected in the measurement results. The output signal of the transmitter chip is sent off-chip in the same way. A pair of bias-T is adopted to set the common-mode voltage for the output ports of the transmitter. A pair of -32-dB attenuator is utilized to shirk the signal swing to prevent the input ports of the sampling oscilloscope (Keysight N1060A) from saturation. The

photo of the measurement environment is presented in Fig. 3.20. In addition to the signal generator and sampling oscilloscope, a low-frequency board is utilized to feed the EVB with power supply, bias currents and control voltages.

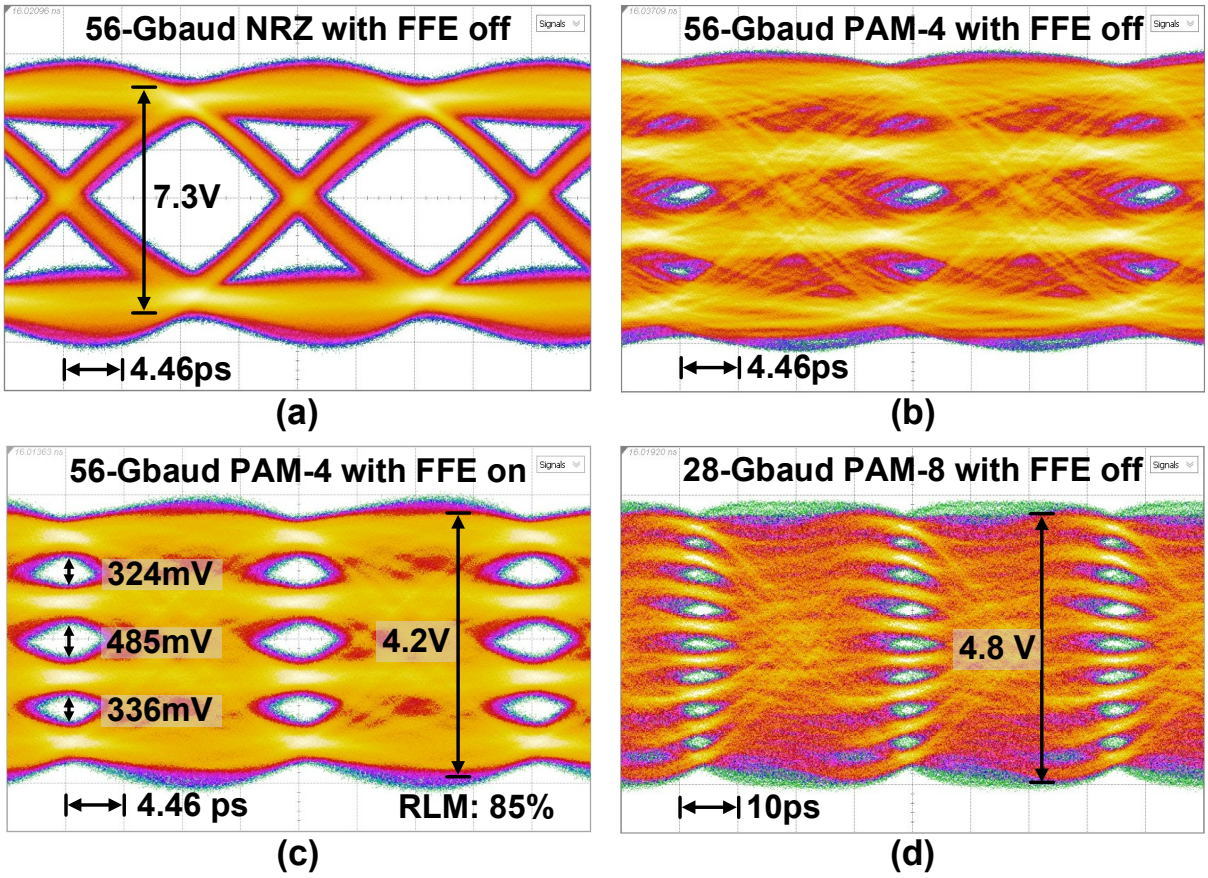


**Fig. 3.21 Measured eye diagrams of the outputs of the whole transmitter at (a) 56-Gbaud NRZ with FFE off, (b) 56-Gbaud PAM-4 with FFE off, (c) 56-Gbaud PAM-4 with FFE on, and (c) 28-Gbaud PAM-8 with FFE off.**

The measured eye diagrams of the whole transmitter are presented in Fig. 3.21. Fig. 3.21(a) shows the output of the transmitter with two 28-Gbaud NRZ inputs and the FFE turned off by powering down the equalization path of the AMUX-FFE. The two 28-Gbaud NRZ inputs are firstly serialized by the AMUX-FFE inside the transmitter into small-swing 56-Gbaud NRZ signal, which is then amplified by the following linear driver. As shown in Fig. 3.21, the eye diagram of the 56-Gbaud NRZ output can be clearly opened with a swing of 7.3 $V_{ppd}$. However, for the case with two 28-Gbaud PAM-4 inputs and the FFE turned off, as

shown in Fig. 3.21(b), the eye diagram of the 56-Gbaud PAM-4 output cannot be clearly opened, mainly due to limited bandwidth of the linear driver and the losses of assembly elements. And then, when the FFE is turned on, a clearly opened 56-Gbaud PAM-4 eye diagram with a swing of 4.2 $V_{ppd}$ is obtained, as shown in Fig. 3.21(c). The transmitter is further evaluated with PAM-8 signal capable of delivering 3-bit information per symbol. Fig. 3.21(d) presents the eye diagram of the 28-Gbaud PAM-8 output of the transmitter which is stimulated by two 14-Gbaud PAM-8 inputs, corresponding to a data rate of 84 Gb/s. The seven PAM-8 sub-eyes are clearly opened and a swing of 4.8 $V_{ppd}$ is achieved. PAM-8 measurements with higher data rates have not been performed due to insufficient bandwidth of the signal generator.

Fig. 3.22 illustrates the power breakdown of the proposed transmitter when dealing with two 28-Gbaud PAM-4 inputs and outputting 56-Gbaud 4.2-$V_{ppd}$ PAM-4 signal. The power consumed by the AMUX-FFE is 740 mW, occupying 41.5% of the total power consumption of the transmitter. The power overhead of the linear driver is 1040 mW, out of which the output stage burns 560 mW for high-speed large-swing output signals. The whole linear transmitter consumes a power of 1780 mW.

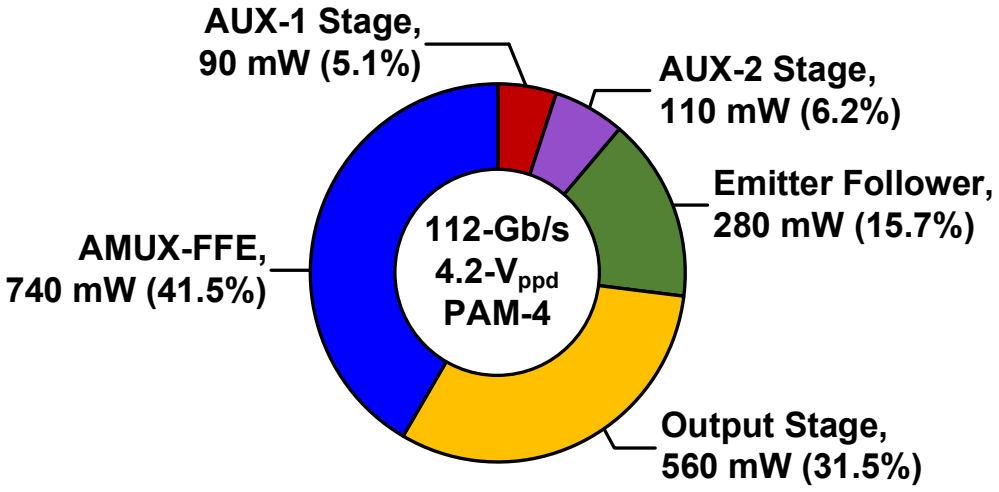


**Fig. 3.22 Power breakdown of the whole linear transmitter when delivering 112-Gb/s 4.2-$V_{ppd}$ PAM-4 signal.**

### 3.4.3 Performance Summary

**Table 3.1. Performance summary of the proposed linear modulator transmitter and comparison with state-of-the-art works.**

| | | [45] | [46] | [52] | [64] | This Work |
|---|---|---|---|---|---|---|
| SiGe Tech. Node | | 130nm | 130nm | 130nm | 130nm | 130nm |
| $f_T$ / $f_{MAX}$ [GHz] | | 300/500 | 300/500 | 250/NA | 380/520 | 250/340 |
| Type | | Distributed | Distributed | Lumped | Lumped | Lumped |
| $Z_O$* [Ω] | | 100 | 100 | 100 | 100 | 100 |
| Equalization | | NA | 2-tap FFE | NA | NA | Re-config. 3-tap FFE |
| Serialization | | NA | NA | NA | NA | 2:1 Analog |
| Maximum Ouput Swing [$V_{ppd}$] | | 4 @90-Gb/s PAM-4 | 4 @64-Gb/s Duobinary | 6 @64-Gb/s NRZ | 2 (estimated from P1dB) | **7.3 @56-Gb/s NRZ** |
| Maximum Data Rate [Gb/s] | | 120 @3-Vppd NRZ | 64 @4-$V_{ppd}$ Duobinary | 138 @2.4-$V_{ppd}$ PAM-4 | 128 @1.2-$V_{ppd}$ PAM-4 | **112 @4.2-$V_{ppd}$ PAM-4** |
| Data Rate*Output Swing [V·Gb/s] | | 360 | 256 | 384 | 256 | **470** |
| Driver THD | | 3.8% @1GHz, 3$V_{ppd}$ | 5.5% @1GHz, 4$V_{ppd}$ | 3.6% @1GHz, 6$V_{ppd}$ | 6% @5GHz, 2$V_{ppd}$ | **1.6% @1GHz, 6$V_{ppd}$** |
| Area [$mm^2$] | | 1.2 | 1.5 | 1.6 | 0.55 | 0.9 |
| Power [mW] | Driver | 1030 | 1000 | 550 | 280 | 1040 |
| | AMUX | NA | NA | NA | NA | 740 |
| FoM** [bit/s/Hz] | | 0.00818 | 0.00414 | 0.00397 | 0.00217 | **0.00867*** ** |

*Differential output impedance matching

$$**\text{FoM}=\frac{\text{Maximum Data Rate}}{f_T}\times\frac{(\text{Output Swing@Maximum Data Rate})^2}{8\times Z_O\times\text{Power Consumption}}$$

***Includes the power consumed by the driver and the equalization paths of the AMUX

Table 3.1 summarizes the performance of the proposed linear modulator transmitter and compares this work with state-of-the-art linear drivers also in SiGe BiCMOS [45][46][52][64]. This work is the first design integrating AMUX with linear driver monolithically in SiGe BiCMOS, while the other works are all merely linear driver front end. In addition to the function of analog serialization and re-configurable FFE, this transmitter achieves the largest data rate-output swing product at 4.2-$V_{ppd}$ 112-Gb/s PAM-4. Since performances of different SiGe technologies are different even if they are at the same node, a FoM taking account of data rate, frequency performance of the HBT, and power transfer efficiency is utilized to better compare these works. This transmitter achieves the highest FoM of 0.00867, thanks to the proposed AMUX-FFE and dynamic triple-stacked driver topology.

## 3.5 Conclusion

This chapter introduces a half-rate linear transmitter in 130-nm SiGe BiCMOS for optical modulator-based interconnects. The transmitter consists of an AMUX-FFE and a linear driver. The AMUX-FFE achieves 2-to-1 analog serialization as well as tap generator-less FFE which can be reconfigured into either 2-tap UI-spaced FFE or 3-tap fractional-spaced FFE. The linear driver adopts a triple-stacked topology with two common-base transistors dynamically biased by two auxiliary amplifiers. Measurements demonstrate that the linear driver achieves a DC gain of 17.1 dB, a 3-dB bandwidth of 37.8 GHz, and a THD of 1.6 GHz with 6-$V_{ppd}$ sinusoidal output. The performance of the proposed AMUX-FFE is verified by the time-domain measurement for the whole transmitter at 112-Gb/s PAM-4. With the FFE turned on, the linear transmitter is capable of outputting 4.2-$V_{ppd}$ 112-Gb/s PAM-4 signals with a power consumption of 1.78 W. Additionally, the transmitter achieves a maximum output swing of 7.3 $V_{ppd}$ with 56-Gb/s NRZ signal.

# CHAPTER IV

## 100-Gbaud Distributed Linear Modulator Driver Design

### 4.1 Introduction

In the last chapter, a linear driver with dynamic triple-stacked topology is proposed for optical modulators, achieving superior output swing and linearity. However, its data rate still cannot fully satisfy the requirements of the next-generation Ethernet standard which targets for a gross data rate of 800 Gb/s with configurations of 8 × 100 Gb/s or 4 × 200 Gb/s [65]. The major obstacle that limits the data rate is the parasitics of transistors. To provide adequate output swing, gain, and linearity simultaneously, the sizes of the transistors are supposed to be large, especially for the output stage where a large amount of current is delivered, resulting in severe parasitics alongside the critical signal path. Moreover, for broadband drivers, termination resistors are necessary to ensure good impedance matching from DC to high-frequency band. The sizes of output termination resistors should also be large enough to withstand the large current, further degrading the bandwidth of the driver.

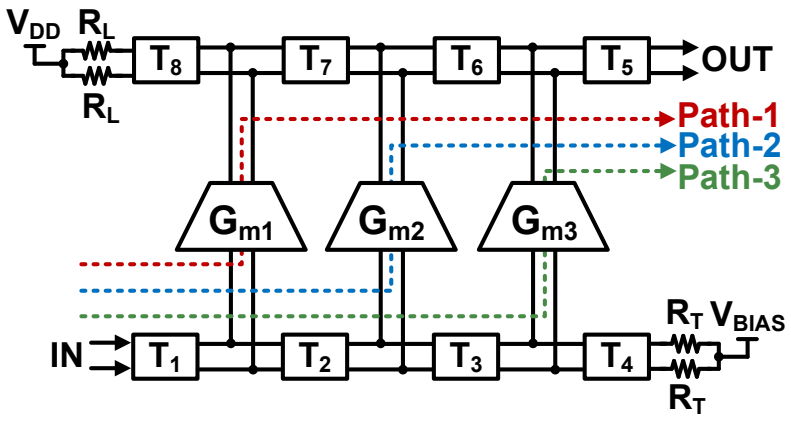


**Fig. 4.1 A typical distributed amplifier with three parallel Gm cells.**

One promising solution to counteract those parasitics is to use distributed amplifier topology. Fig. 4.1 depicts a typical distributed amplifier with three parallel Gm cells as an example. The three Gm cells denoted by $G_{m1}$, $G_{m2}$ and $G_{m3}$ are connected by eight

transmission line (TL) segments denoted by $T_1$~$T_8$. There are three paths from the input port to the output port. Path-1 denotes the path travelling through $T_1$, $G_{m1}$, $T_7$, $T_6$, and $T_5$. Path-2 denotes the paths going through $T_1$, $T_2$, $G_{m2}$, $T_6$, and $T_5$. And Path-3 denotes the path traveling through $T_1$, $T_2$, $T_3$, $G_{m3}$, and $T_5$. To ensure that the outputs of the three Gm cells can be combined in-phase at the output node, delays of Path-1, Path-2 and Path-3 should be equivalent. Therefore, $T_2$ should be the same with $T_7$, and $T_3$ should be the same with $T_6$. By properly designing the eight TL segments, the input and output parasitic capacitance of the three Gm cells can be significantly absorbed, and a high bandwidth can be achieved. This topology is initially extensively employed in power amplifiers for wireless communications to achieve wide operational frequency range [66-71]. Recently, it has emerged as a promising choice for broadband linear driver designs to boost the data rate of optical modulator-based interconnects [41,45,42-44,46-48]. Some of these drivers are fully implemented in distributed amplifier topology [41,45,42-44], while others adopt this topology only for their output stages to save the die area [46-48].

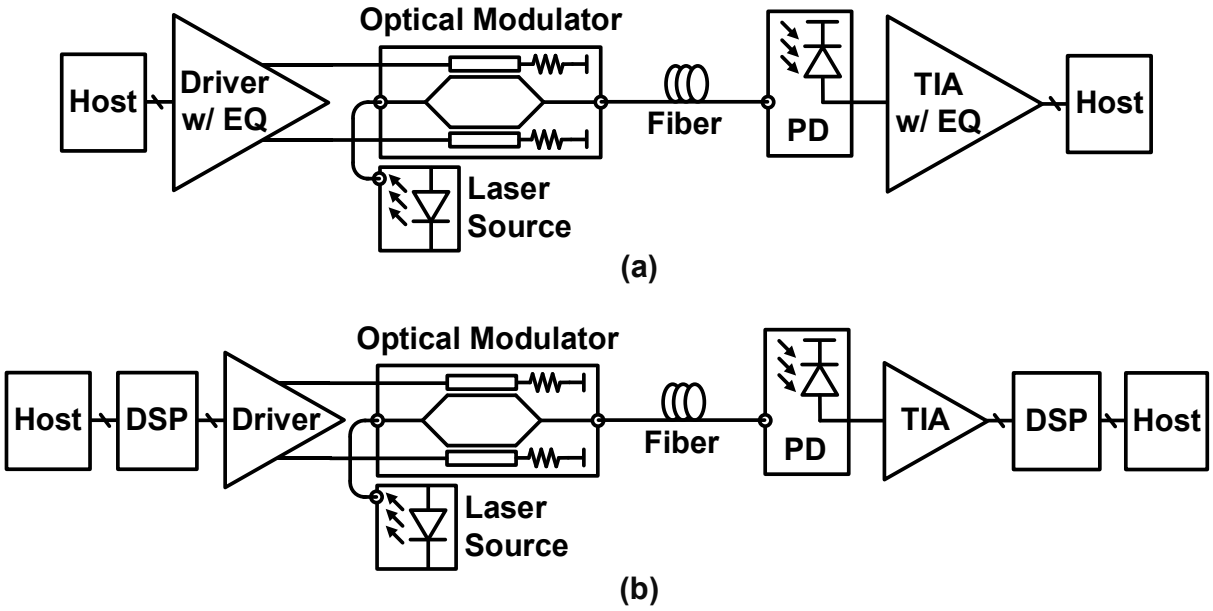


**Fig. 4.2 (a) A typical LPO interconnect, and (b) a typical DSP-based optical interconnect.**

To further extend the bandwidth of the whole system, capability of equalization is a plus for distributed linear drivers to compensate for losses from assembly components and

channels. For the linear drivers in some specific applications, the equalization function is even indispensable. Linear pluggable optics (LPO), which emerges as one of the hottest research topics recently, is a representative example. A typical LPO interconnect is shown in Fig. 4.2(a), and a conventional DSP-based optical interconnect is depicted in Fig 4.2(b) for comparison. By implementing equalization functions in driver and transimpedance amplifier (TIA), LPO interconnects remove DSP block at both TX and RX sides. Hence, the power consumption, latency, and hardware cost compared of LPO interconnects can be significantly reduced compared with the conventional DSP-based solution. However, most of distributed linear drivers mentioned above do not have equalization capabilities, and hence cannot be adopted for LPO applications. [46] and [48] are exceptions. In [46], a distributed driver with two parallel Gm cells is reported. Different from the conventional distributed amplifier topology, the delays of the two signal paths via the two Gm cells are different, to form a two-tap FFE. However, this topology is hard to get extended to multiple FFE taps. Because with the increase of the length of transmission line units, the corner frequency of related nodes will decrease, resulting in a limited overall bandwidth. In [48], the equalization is achieved by degenerated resistors inside the lumped VGA and pre-driver stages. Transistors with controllable gate voltages are implemented in parallel with those resistors to tune their effective resistance. The larger the resistance, the higher the peaking gain. However, the peaking frequency of this scheme cannot be adjusted and is mostly constrained by the parasitics of transistors and resistors, resulting in a limited equalization capability.

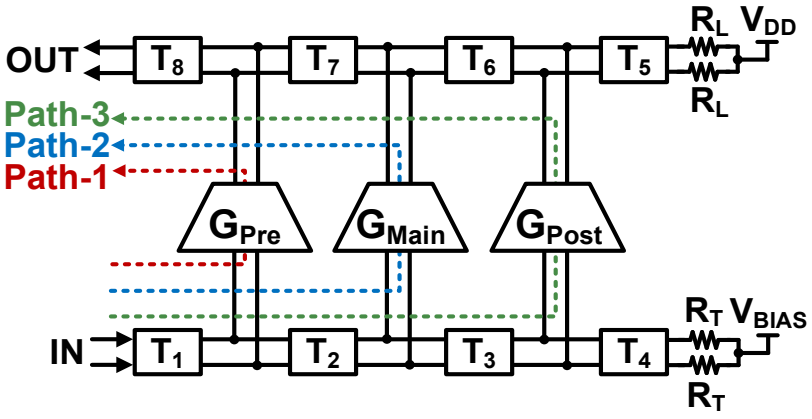


**Fig. 4.3 A typical TL-based FFE with three taps.**

To achieve equalization functions without degrading the bandwidth, some works adopt TL-based FFE topology [72-74]. Fig. 4.3 depicts a typical implementation of the TL-based FFE with three taps. Still, there are three paths from the input port to the output port, denoted by Path-1, Path-2, and Path-3. Different from the distributed amplifier topology shown in Fig. 4.1, the delays of the three paths are deliberately designed to be different, and the polarity of $G_{Main}$ is reversed with those of $G_{Pre}$ and $G_{Post}$. To simplify the analysis, the designs of the eight TL segments denoted by $T_1$~$T_8$ are assumed to be the same, and the designs of $G_{Pre}$, $G_{Main}$, and $G_{Post}$ are also assumed to be the same. Therefore, the delay of Path-2 is $2 \times D_{TL}$ longer than that of Path-1, $D_{TL}$ denoting the delay of a single TL segment. Similarly, the delay of Path-3 is $2 \times D_{TL}$ longer than that of Path-2. In this way, a three-tap FFE consisting of one pre-tap, one main tap and one post-tap is achieved, and both pre-to-main and main-to-post tap spacings are equal to $2 \times D_{TL}$. The TL-based FFE can provide superior equalization capability. Moreover, with the inductance of transmission lines, its inherent bandwidth is high. Nevertheless, this topology is not suitable for linear drivers, as its gain and output swing are quite small due to reversed polarities between the main-tap Gm cell and other equalization Gm cells.

To obtain superior performances in bandwidth and equalization capability while not sacrificing output swing, gain, and linearity, this work proposes a distributed amplifier topology with cross-folded transmission line and cross-coupled Gm cells to for built-in FFE. The proposed topology simultaneously utilizes transmission lines as inductance to absorb the parasitics of the Gm cells and as delay elements to achieve built-in FFE which is easily re-configurable and upgradable. To validate the topology, a linear distributed driver with 5-tap FFE is implemented in 130-nm SiGe BiCMOS as a prototype.

This chapter is organized as follows. Section 4.2 introduces the architecture design evolution of the proposed distributed amplifier topology. Section 4.3 describes the layout implementation of the cross-folded transmission line, as well as circuit implementations of the

Gm cell. The frequency- and time-domain measurement setups and measurement results of the implemented distributed linear driver prototype are presented in section 4.4. Finally, the conclusion of this chapter is drawn in section 4.5.

## 4.2 Architecture Design

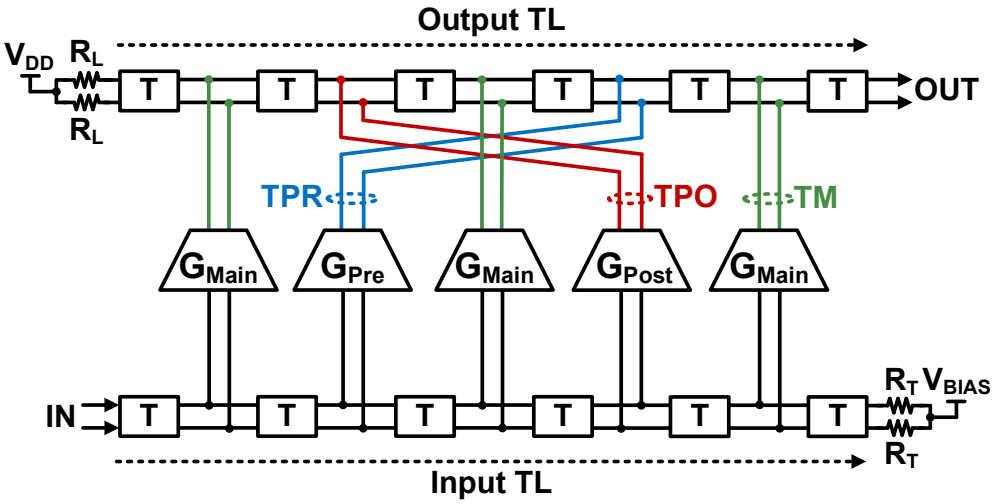


**Fig. 4.4 Architecture of the distributed amplifier with cross-coupled Gm cells.**

Fig. 4.4 depicts the first version of the proposed distributed linear driver. Based on conventional distributed amplifier shown in Fig. 4.1, two additional Gm cells denoted by $G_{Pre}$ and $G_{Post}$ are inserted between the three main-tap Gm cells denoted by $G_{Main}$. The polarities of $G_{Pre}$ and $G_{Post}$ are reversed with that of $G_{Main}$. There are three different paths from the input port denoted by IN to the output port denoted by OUT, including the pre-tap path, main-tap path and post-tap path. The pre-tap path travels through $G_{Pre}$ and four TL segments from IN to OUT. The main-tap path going through $G_{Main}$ and six TL segments from IN to OUT. And the post-tap path travels through $G_{Post}$ and eight TL segments from IN to OUT. In this way, a 3-tap FFE composed of one pre-tap, one main tap, and one post-tap is built inside the driver, where $G_{Main}$, $G_{Pre}$ and $G_{Post}$ are Gm cells for the pre-tap, main-tap, and post tap, respectively. The gain and output swing of this topology can be improved by increasing the number of $G_{Main}$ and related TL segment. In this way, superior performances in output swing, bandwidth, gain as well as equalization capability can be achieved simultaneously.

Regarding the tap spacing between the three paths, with an assumption that the circuits of $G_{Pre}$, $G_{Main}$ and $G_{Post}$ are the same, the tap spacing between the pre-tap and main tap can be expressed as

$$TS_{\text{Pre-to-Main}} = 2 \times Delay_{\text{T}} + Delay_{\text{TM}} - Delay_{\text{TPR}} \tag{4.1}$$

and that between the main tap and post-tap can be expressed as

$$TS_{\text{Main-to-Post}} = 2 \times Delay_{\text{T}} + Delay_{\text{TPO}} - Delay_{\text{TM}} \tag{4.2}$$

where $Delay_{\text{T}}$, $Delay_{\text{TM}}$, $Delay_{\text{TPR}}$, and $Delay_{\text{TPO}}$ denote the delay of a single TL segment, delay of the interconnection between the output of $G_{Main}$ and the output TL, delay of the interconnection between the output of $G_{Pre}$ and the output TL, and delay of the interconnection between the output of $G_{Post}$ and the output TL, respectively. However, there is a severe defect with this topology. Since

$$2 \times Delay_{\text{T}} + Delay_{\text{TM}} \approx Delay_{\text{TPR}} \tag{4.3}$$

the pre-to-main tap spacing is too small to cancel ISI cursors properly.

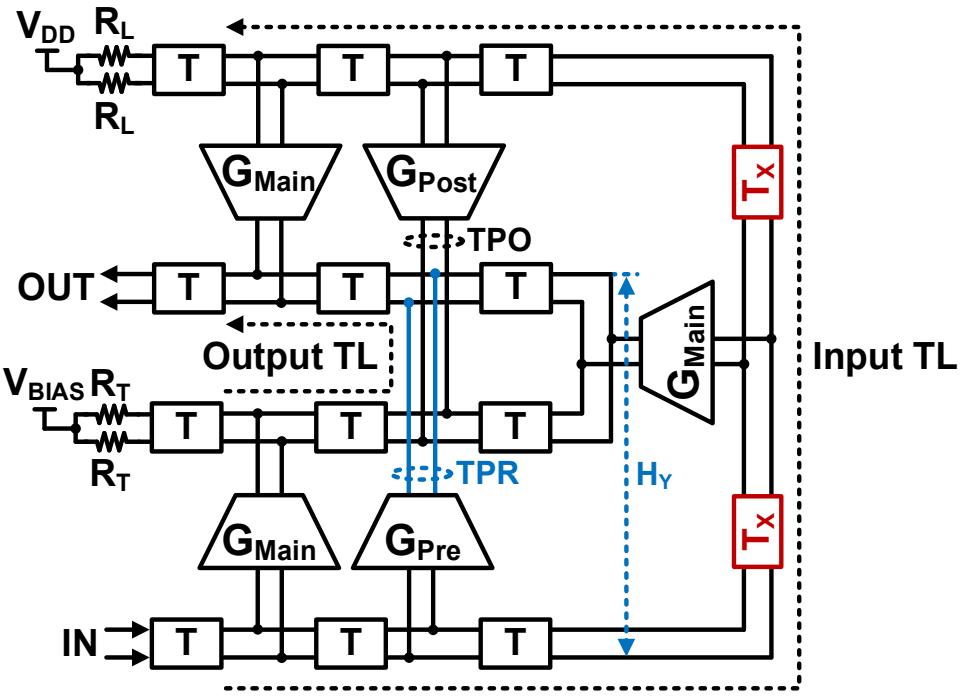


**Fig. 4.5 Architecture of the distributed amplifier with cross-coupled Gm cells and folded transmission line.**

To settle the issue, the second-version distributed amplifier is proposed, as depicted in Fig. 4.5. By folding the input TL and output TL, the interconnection between the output of $G_{Pre}$ and output TL, i.e. TPR, can be implemented vertically, so that its length can be minimized by decreasing $H_Y$ without affecting the length of TL segment. Hence, a reasonable pre-to-main tap spacing can be achieved.

However, this topology introduces a length discrepancy between the input and output TLs. As shown in Fig. 4.5, the length of the input TL is $2 \times T_X$ longer than that of the output TL. Consequently, the outputs of the three main-tap Gm cells cannot be combined in-phase at the output node of the driver, resulting in significant distortion for the output signal.

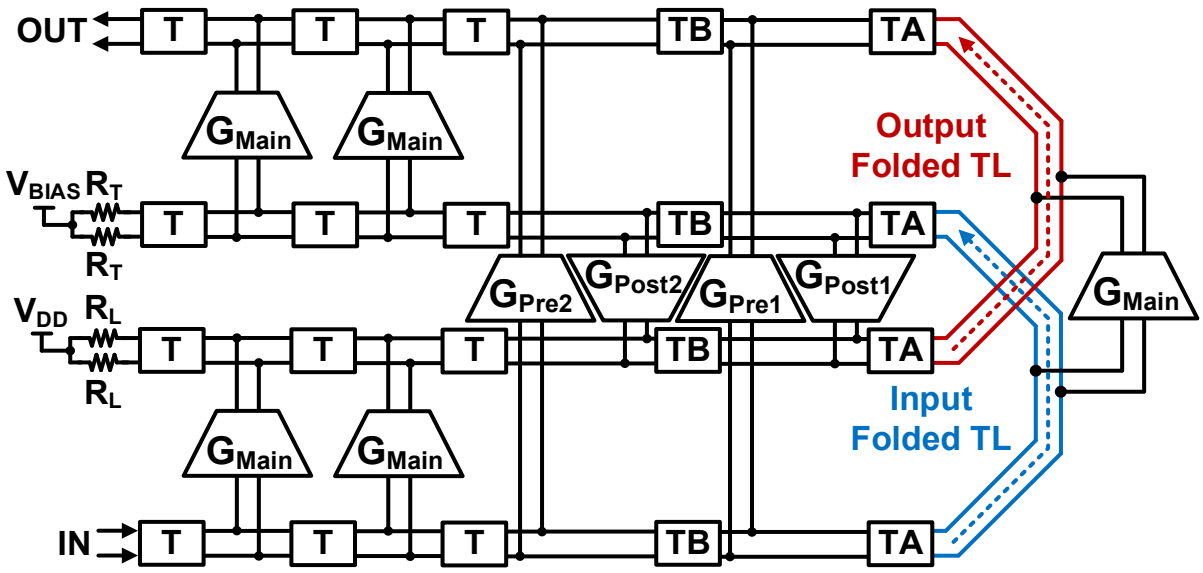


**Fig. 4.6 Architecture of the distributed amplifier with cross-coupled Gm cells and cross-folded transmission line.**

To equalize the lengths of the input and output TLs, the topology in Fig. 4.5 eventually evolves to the final version shown in Fig. 4.6. In this version, the input and output TLs are still folded. Different from the second version, a cross-folded TL scheme is introduced, where the input and output TLs are partially stacked to match their lengths. By this means, the length discrepancy issue is mitigated. Besides, to further enhance the equalization capability of the

driver, in this version, four cross-coupled Gm cells denoted as $G_{Pre2}$, $G_{Pre1}$, $G_{Post1}$, and $G_{Post2}$ are implemented to achieve 2nd pre-tap, 1st pre-tap, 1st post-tap, and 2nd post-tap, respectively. Moreover, five main-tap Gm cells denoted as $G_{Main}$ are deployed to provide large swing and high gain. The tap spacings between these five taps are expressed by equations (4.4) ~ (4.7), where $TS_{Pre2\text{-}to\text{-}Pre1}$, $TS_{Pre1\text{-}to\text{-}Main}$, $TS_{Main\text{-}to\text{-}Post1}$, and $TS_{Post1\text{-}to\text{-}Post2}$ denotes the tap spacings between 2nd pre-tap and 1st pre-tap, 1st pre-tap and main tap, main tap and 1st post-tap, and 1st post-tap and 2nd post-tap, respectively. $Delay_{Pre2}$, $Delay_{Pre1}$, $Delay_{Main}$, $Delay_{Post1}$, and $Delay_{Post2}$ are delays of 2nd pre-tap, 1st pre-tap, main-tap, 1st post-tap, and 2nd post-tap, respectively. And $Delay_{TA}$ and $Delay_{TB}$ denote the delays of the TL segment TA and TB, respectively. The four tap spacings can be adjusted by related transmission line segments. For example, the spacing between the 1st pre-tap and main tap can be tuned by changing the length of TA.

$$TS_{Pre2\text{-}to\text{-}Pre1} = 2 \times Delay_{TB} + Delay_{Pre1} - Delay_{Pre2} \tag{4.4}$$

$$TS_{Pre1\text{-}to\text{-}Main} = 2 \times Delay_{TA} + Delay_{Main} - Delay_{Pre1} \tag{4.5}$$

$$TS_{Main\text{-}to\text{-}Post1} = 2 \times Delay_{TA} + Delay_{Post1} - Delay_{Main} \tag{4.6}$$

$$TS_{Post1\text{-}to\text{-}Post2} = 2 \times Delay_{TB} + Delay_{Post2} - Delay_{Post1} \tag{4.7}$$

## 4.3 Implementations of Building Blocks

### 4.3.1 Transmission Line Segment

There are three different TL segments inside the proposed distributed linear driver, including T, TA, and TB as shown in Fig. 4.6. While TA is a part of the cross-folded TLs, T and TB share the same structure and only differ in the segment length. This section illustrates the design of the TL segment for T and TB, and the design of TA will be introduced in the next section which focuses on the cross-folded TL.

The first concern when designing the TL is the selection of metal. There are two criteria

for the metal determination. Firstly, it should be capable of delivering high-density current, and hence thick metals are preferable. Secondly, it should be far from the substrate to reduce the noise coupling and parasitic effect. The SiGe BiCMOS process design kit (PDK) used in this work provides six metal layers. While metal-1 (M1) to metal-4 (M4) are all thin layers, metal-5 (M5) and metal-6 (M6) are thick layers with current delivery capabilities much better than those of M1 to M4. Specifically, M5 is made of copper and supports a current density of approximately 16 mA/μm at 100 °C, while M6 is an aluminum-based layer supporting a current density of 6 mA/μm at 100 °C which is only 37.5% of that of M5. Although M6 is farther from the substrate than M5, to withstand the same amount of current, the width of M5 can be merely one third of that of M6, leading to benefits of slighter parasitic effect and smaller area overhead. Therefore, M5 is selected by this work to build the TL segment.

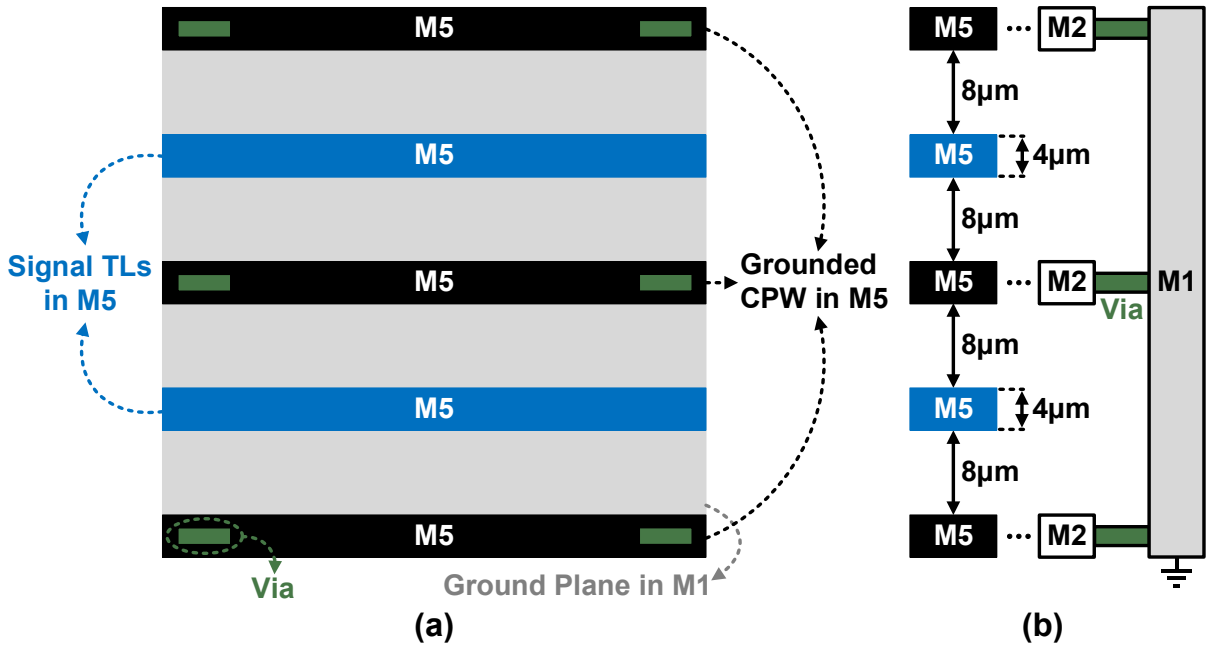


**Fig. 4.7 (a) Top and (b) cross-section views of the TL segment.**

The top and cross-section views of the designed TL segment are presented in Fig. 4.7(a) and Fig. 4.7(b), respectively. The differential signals are delivered by a pair of signal TLs which are implemented using M5 layer. Three grounded coplanar waveguides (CPWs) are deployed also in M5 shielding the two signal TLs to enhance the signal integrity. The widths of all signal TLs and grounded CPWs are 4 μm. And the separation between adjacent signal

TL and grounded CPW is 8 μm. A ground plane in M1 layer is designed beneath the signal TLs and grounded CPWs to shield the signal from the noise of the substrate. The three grounded CPWs are connected to the ground plane using vias to share the same ground voltage, which simplifies the power distribution for the whole driver chip.

### 4.3.2 Cross-coupled Transmission Line

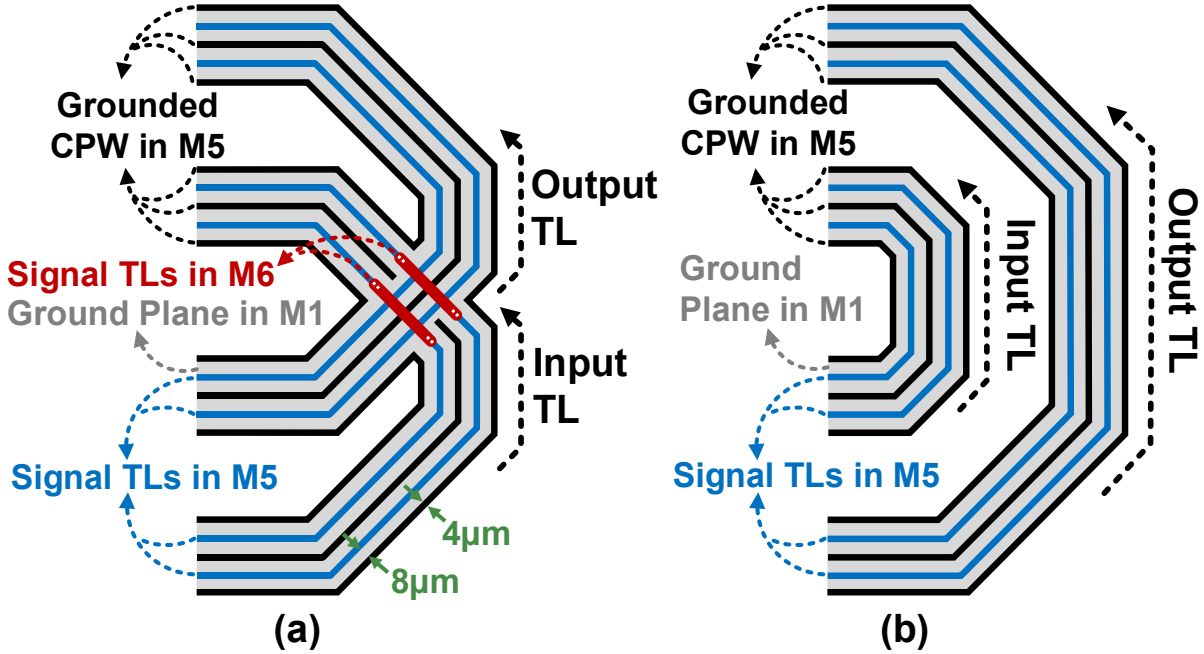


**Fig. 4.8 (a) Layout of the proposed cross-folded TL scheme, and (b) layout of the conventional folded TL scheme.**

As described above, to match the lengths of the input and output TLs, a cross-coupled TL scheme is implemented in the proposed distributed linear driver. Fig. 4.8(a) shows the layout of the cross-coupled TL, consisting of an input TL and an output TL. Except the overlapping part, both the input and output TLs adopt the same structure with the TL segment described in section 4.3.1, incorporating a pair of 4-μm signal TLs shielded by three 4-μm grounded CPWs. The separations of adjacent signal TL and grounded CPW are 8 μm. And all of signal TLs and grounded CPW are implemented in M5 and shielded by the ground plane in M1. For the overlapping part, the signal TLs of the input TL jump from M5 to M6 to avoid intersection

with the output TL. After passing the output TL, the signal TLs of the input TL drop from M6 back to M5. However, the overlapping between the input and output TLs may cause impedance discontinuity for the input signal, leading to bad input reflection of the driver. Moreover, the overlapping introduces parasitic capacitance between the input and output TLs which may degrade the reverse isolation of the driver. To evaluate these potential degradations, a conventional folded TL scheme is implemented for comparison as shown in Fig. 4.8(b), where the input TL and output TL are not overlapped. As a result, the length of the output TL is approximately three times that of the input TL. Still, structures of both input TL and output TL are the same with that of the TL segment described in section 4.3.1.

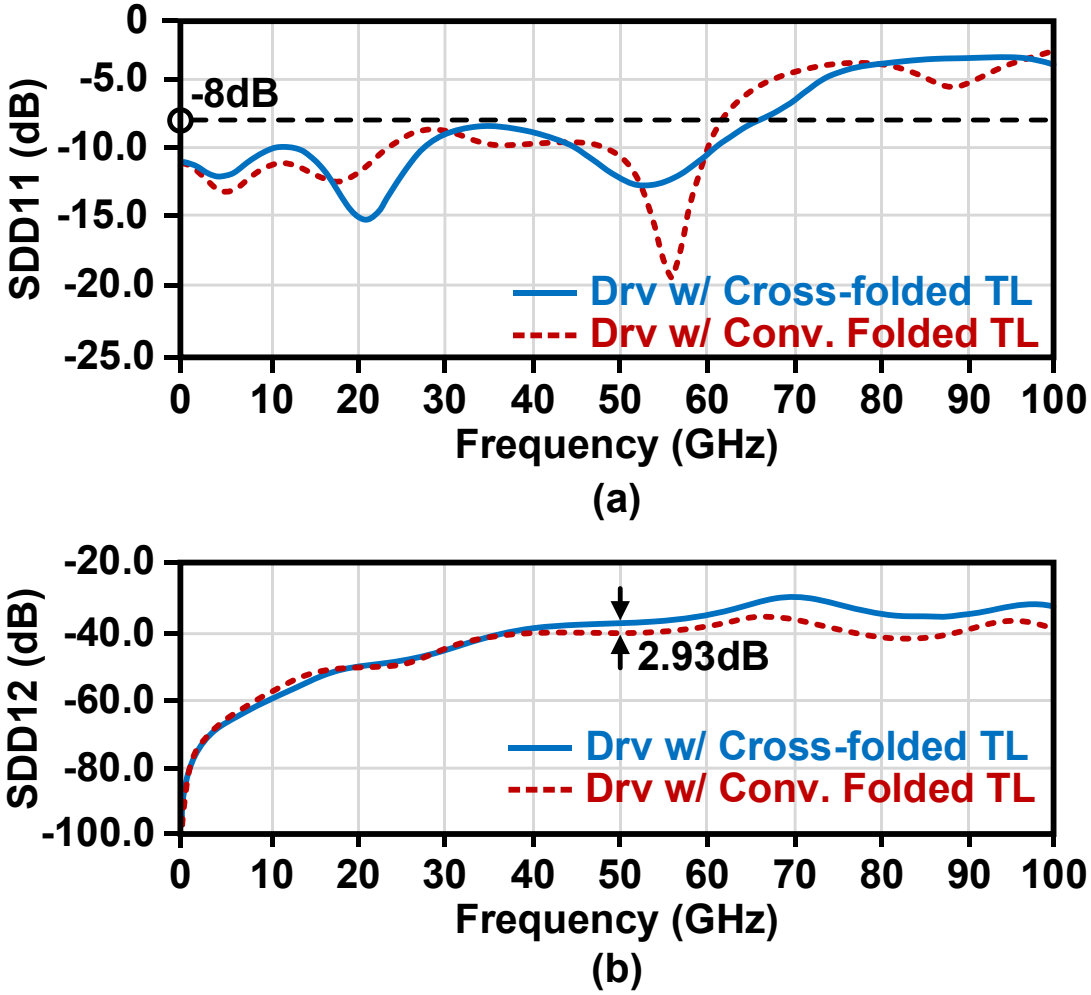


**Fig. 4.9 Simulated (a) input return losses and (b) reverse isolations of the linear drivers with cross-folded TL and conventional folded TL.**

Blue solid curve and red dashed curve in Fig. 4.9(a) illustrate the simulated input return losses of the driver with cross-folded TL and the driver with conventional folded TL, respectively. The two curves are close to each other and both smaller than -8 dB from DC to 50 GHz, indicating that the impact from the overlapping part in the cross-coupled TL scheme on the input reflection performance is negligible. Fig. 4.9(b) presents simulated reverse gains of the two drivers. The two SDD12 curves are still so close to each other with DC to 50 GHz. At 50 GHz, the reverse isolation of the driver with cross-folded TL is 2.93 dB worse than that of the driver with conventional TL. The degradation is negligible considering the absolute values of both SDD12 curves at 50 GHz are already much smaller than -30 dB.

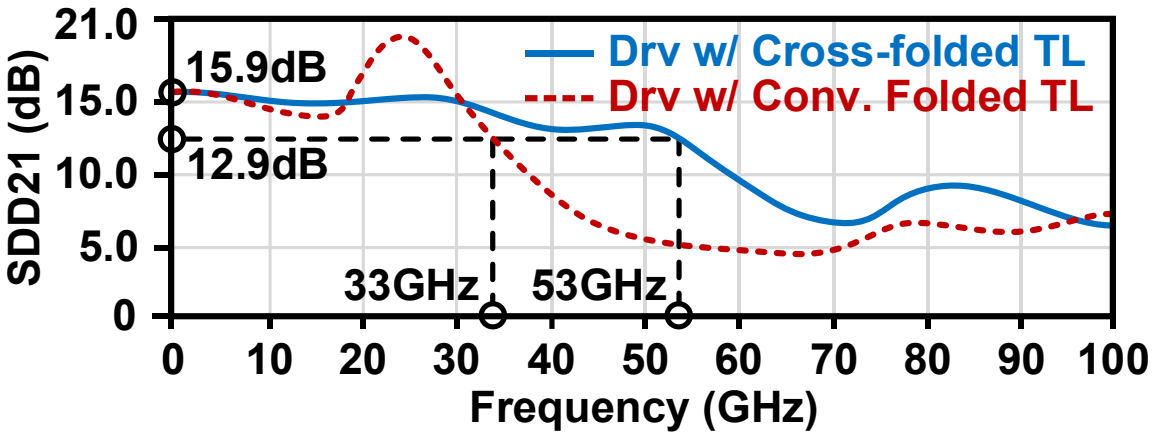


**Fig. 4.10 Simulated forward gain of the linear drivers with cross-folded TL and conventional folded TL.**

Blue solid curve and red dashed curve in Fig. 4.10 show the simulated forward gain of the driver with cross-folded TL and the driver with conventional folded TL, respectively. With the same active parts, both drivers achieve DC gains of 15.9 dB. However, due to the significant mismatch in the lengths of the input and output TLs, the driver with conventional folded TL only obtains a 3-dB bandwidth of 33 GHz with severe in-band gain variations. In contrast, with matched lengths of the input and output TLs, the driver with cross-folded TL achieves a 3-dB bandwidth of 53 GHz, which is about 1.6 times that of the driver with conventional folded TL, as well as a very flat in-band gain characteristic.

### 4.3.3 Gm Cell

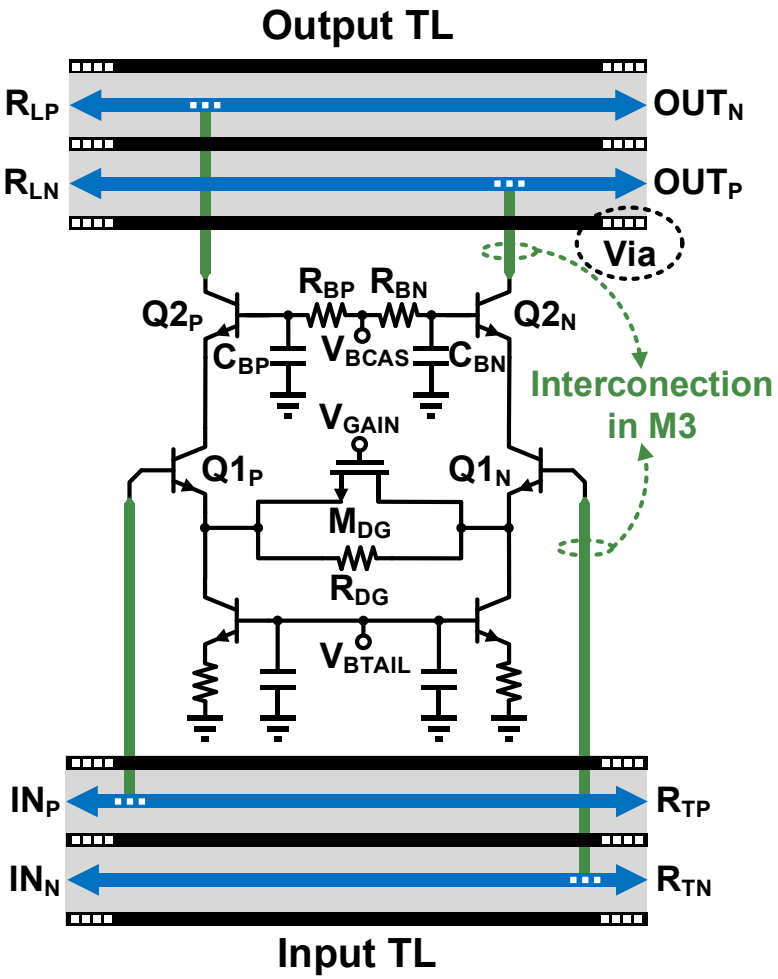


**Fig. 4.11 Schematic of the Gm cell and its interconnections with input and output TLs.**

Gm cells determine the gain, output swing, and linearity of a distributed amplifier. In the proposed distributed linear driver, all the main-tap, pre-tap, and post-tap Gm cells adopt the same structure and same transistor size. The schematic of the driver is depicted in Fig. 4.11. A cascode structure formed by $Q1_P/Q1_N$ and $Q2_P/Q2_N$ is adopted to enhance the breakdown voltage of the Gm cell and suppress the Miller effect. A degenerated resistor denoted by $R_{DG}$ is implemented to enhance the linearity of the Gm cell. To enable gain control for adjusting the coefficients of FFE taps, a MOSFET denoted by $M_{DG}$ is deployed in parallel with $R_{DG}$ to tune the effective degenerated resistance by tuning the gate voltage $V_{GAIN}$. The higher $V_{GAIN}$, the smaller degenerated resistance, and the higher gain of the Gm cell. The bias voltage

denoted by $V_{BCAS}$ is fed to the bases of $Q2_P/Q2_N$ through a biasing network composed of $C_{BP}/C_{BN}$ and $R_{BP}/R_{BN}$. As illustrated in [51], the breakdown voltage of a SiGe HBT is related to its base resistance. When the base of HBT is open, its base resistance is equivalent to infinite. At this time, the breakdown voltage of HBT is $BV_{CEO}$, which is 1.6 V for the used SiGe BiCMOS process. To obtain a breakdown voltage beyond $BV_{CEO}$, the base resistance of the HBT should be as low as possible. Therefore, the resistance of $R_{BP}/R_{BN}$ is supposed to be small. However, the small $R_{BP}/R_{BN}$ increases the corner frequency of the low-pass biasing network, degrading its filtering performance. Hence, a resistance of 350 Ω is selected for $R_{BP}/R_{BN}$ in this work for an optimal tradeoff between the breakdown voltage and bias stabilization.

Fig. 4.11 also illustrates the interconnections between the Gm cell and the input/output TLs. Metal-3 (M3) is selected for these interconnections as this layer located at the middle of M1 and M5, to reduce the couplings with substrate and signal TLs. The input differential signals are delivered to the bases of $Q1_P/Q1_N$ using M3 lines with widths of 4 μm, and the outputs of the Gm cells are sent to the output TL also using 4-μm-width M3 lines.

## 4.4 Measurement Setups and Results

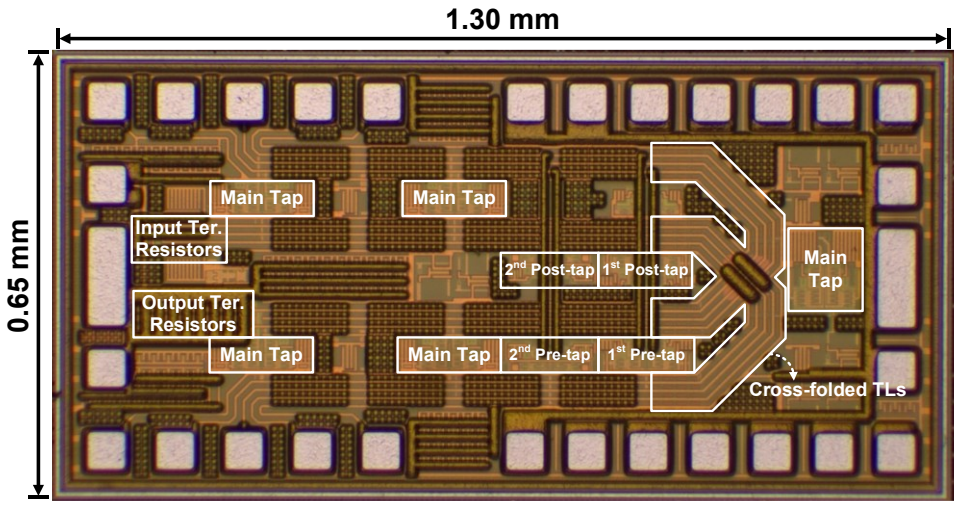


**Fig. 4.12 Die micrograph of the proposed distributed linear driver prototype.**

The proposed distributed linear driver is fabricated in 130-nm SiGe BiCMOS process with $f_T$ and $f_{MAX}$ of 250 GHz and 340 GHz, respectively. Fig. 4.12 presents the die micrograph of the driver, which occupies an area of approximately 0.85 $mm^2$.

### 4.4.1 Frequency-domain Measurement Setup and Results

Fig. 4.13 presents the frequency-domain measurement setup for the distributed linear driver, which is basically the same with the one used for characterizing the linear driver described in section 3.4.1. The driver chip is mounted in a high-frequency EVB. All of power pads, bias pads, and control pads of the driver are wire-bonded to the EVB, except the RF pads. A VNA is used for generating differential continuous-wave signals to stimulate the driver. The model of the VNA is Keysight N5227B. The signals are fed to the input ports of the driver using a 67-GHz SGS probe, and another 67-GHz SGS probe is employed to deliver the differential outputs of the driver to a pair of bias-T. The bias-T is used to set the common-mode voltage for the driver output. The outputs of the bias-T are eventually sent back to the VNA for signal analysis. Fig. 4.14 shows the photo of the frequency-domain measurement environment. In addition to the VNA and power source, a low-frequency auxiliary board is used to provide the supply voltage, bias currents, and control signals for the driver chip. The losses from the cables used for connecting the probes with the VNA/bias-T have been calibrated before the measurement using the calibration kit of the VNA.

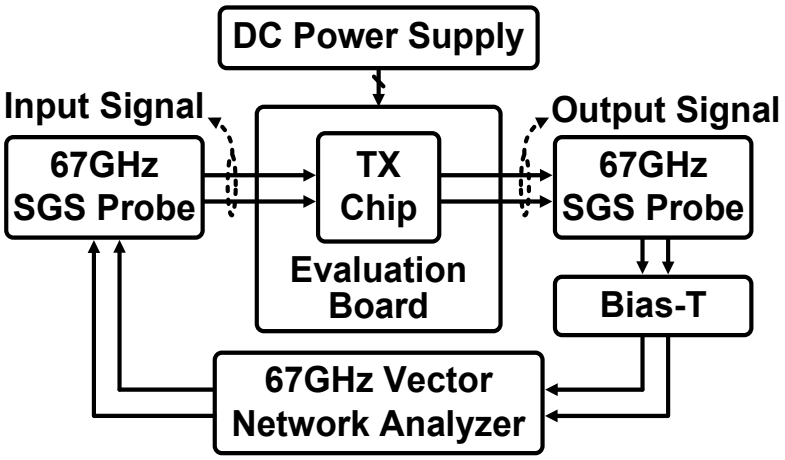


**Fig. 4.13 Frequency-domain measurement setup.**

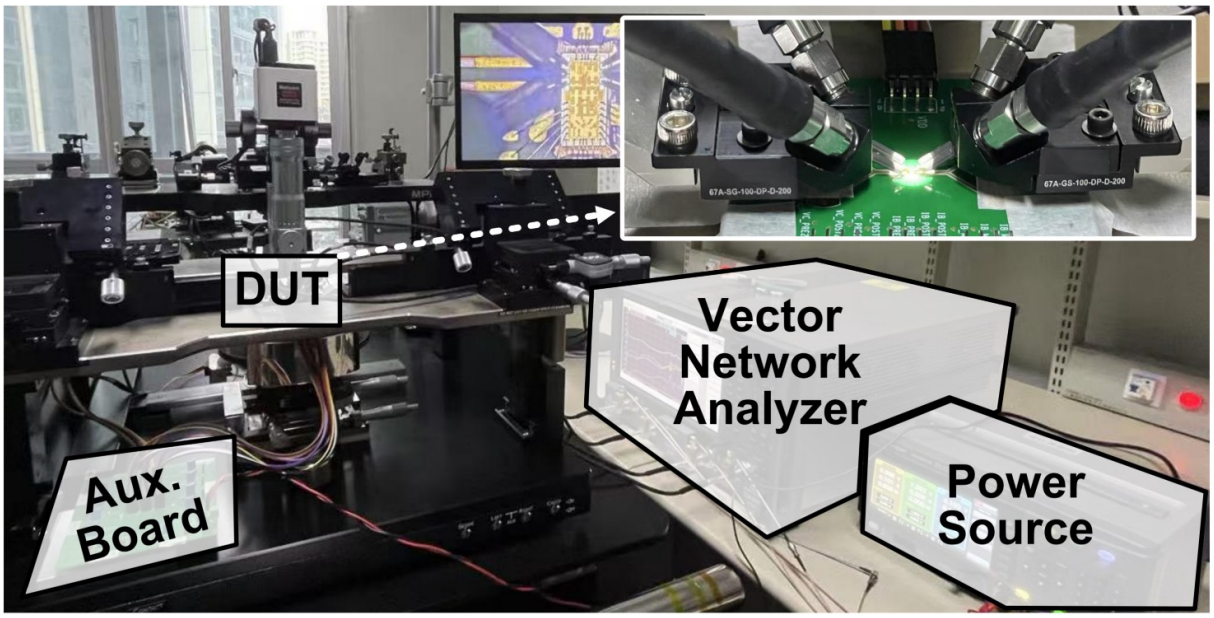


**Fig. 4.14 Photo of the frequency-domain measurement environment.**

Fig. 4.15(a)~(d) present the measured S-parameters with three different FFE settings. For the FFE off, the bias currents of the two pre-taps and two post-taps are switched off. For the middle FFE strength, the bias currents of the two pre-taps and two-post taps are switched on, with control voltages $V_{GAIN}$ for the four FFE taps all set to 1.5 V. For the maximum FFE strength, the bias currents of the two pre-taps and two-post taps are switched on, with control voltages $V_{GAIN}$ for the four FFE taps all increased to 3.3 V. As indicated by the measured forward gains shown in Fig. 4.15(a), when the FFE is turned off, the DC gain and 3-dB bandwidth (BW) of the driver are 15.8 dB and 24.5 GHz, respectively. Although the 3-dB is not that high, the gain roll-off is slow thanks to the distributed topology, achieving a 6-dB bandwidth of 53.4 GHz. When the FFE cells are switched on and their strengths are set to the middle, the DC gain degrades to 12.3 dB, but the 3-dB bandwidth is extended to more than 67 GHz. At the Nyquist frequency of 50 GHz, a gain peaking of 1.8 dB is achieved. When the FFE strength is set to the maximum, although the DC gain decreases to 10.0 dB, the peaking gain at the Nyquist frequency is further boosted to 6.9 dB. The transformations of the three SDD21 curves under different FFE settings verify the effectiveness of the proposed distributed driver topology.

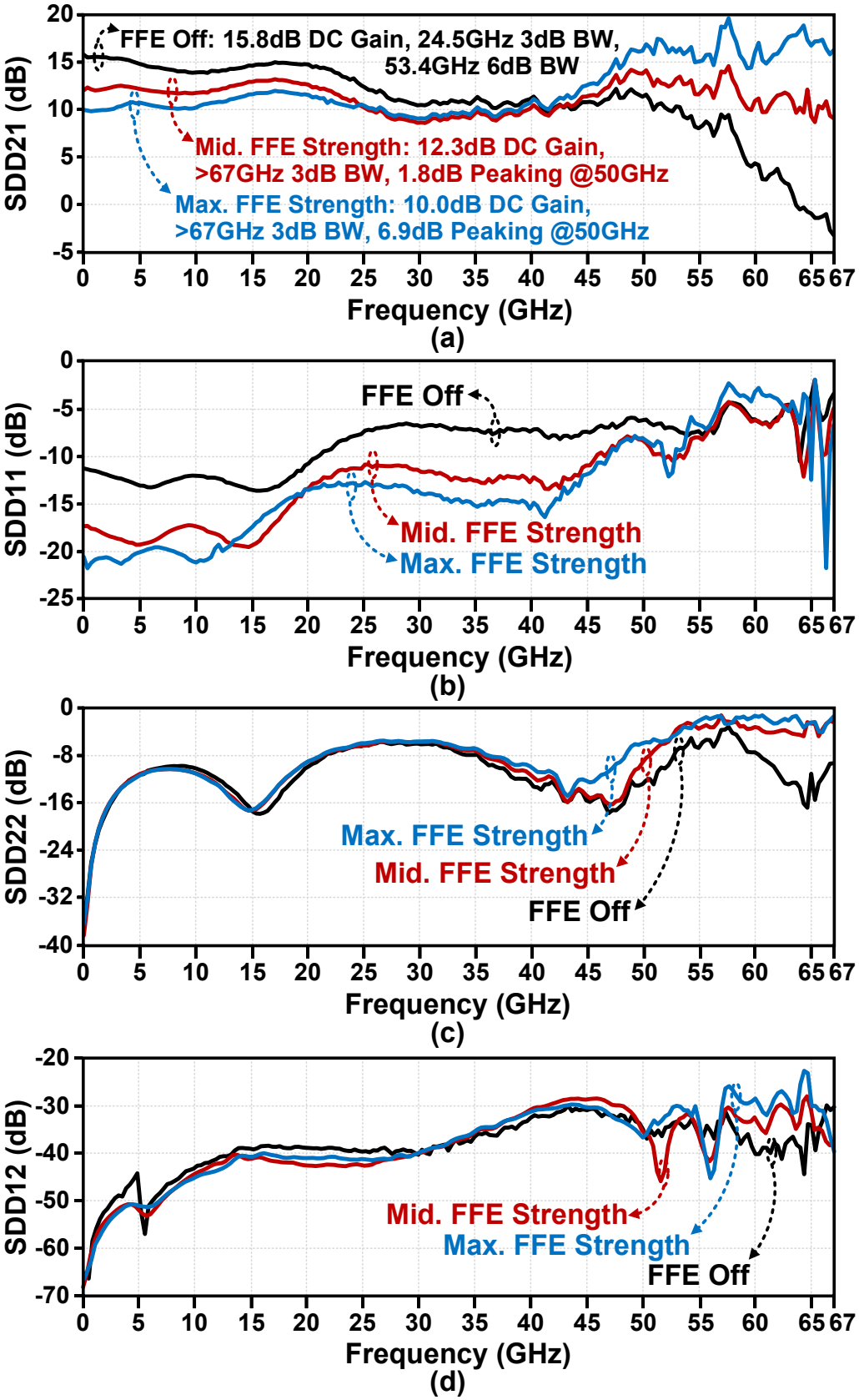


**Fig. 4.15 Measured (a) forward gain (SDD21), (b) input return loss (SDD11), (c) output return loss (SDD22), and (d) reverse gain (SDD12).**

Fig. 4.15(b) and Fig. 4.15(c) present the measured SDD11 and SDD22 curves, respectively. The SDD11 curves indicate that the input return loss of the driver is enhanced when the FFE is switched on. This is because when the FFE is switched off, the shunted resistance provided by the base resistance of FFE Gm cells are too large to impact the impedance alongside the input TL. At this time, the parasitic distribution alongside the input TL becomes less average, introducing the discontinuity of the input impedance which degrades the input return loss. For both middle FFE strength and maximum FFE strength, the input return losses are smaller than -10 dB from DC to 45 GHz. The SDD22 curves indicate that the output return losses for the three FFE settings are similar, as the change of the output impedance of the Gm cell with respect to the bias current is much slighter than that of the input impedance. For all of three FFE settings, the output reflections of the driver are smaller than -8 dB from DC to 21 GHz and 35 GHz to 45 GHz. Within 21 GHz to 35 GHz, the output reflections rise slightly but are still smaller than -6 dB. The measured reverse isolation performances under the three FFE settings are shown in Fig. 4.15(c). The three SDD12 curves are close to each other and below -28 dB from DC to 50GHz.

### 4.4.2 Time-domain Measurement Setup and Results

Fig. 4.16 presents the setup for the time-domain measurements. The assembly between the driver chip and EVB is the same as that for frequency-domain measurements illustrated in section 4.4.1. A signal generator (Keysight M8050A) is employed to provide high-speed NRZ/PAM-4 signals, which are sent to the differential input ports of the driver via a 67-GHz SGS probe. The differential outputs of the driver are delivered to a sampling oscilloscope (Keysight N1046A) through a pair of bias-T and a pair of attenuators for signal analysis and eye diagram observation. The bias-T is used for setting the common-mode voltage for the driver output, and the attenuators prevent the input ports of the sampling oscilloscope from saturation. Fig. 4.17 shows the time-domain measurement environment. Similar with the frequency-domain measurement, the power supply, bias currents and control voltages for the driver are provided by an auxiliary board. The losses from the input and output cables are

de-embedded by the pre-emphasis functions of the signal generator, which is performed before the measurements.

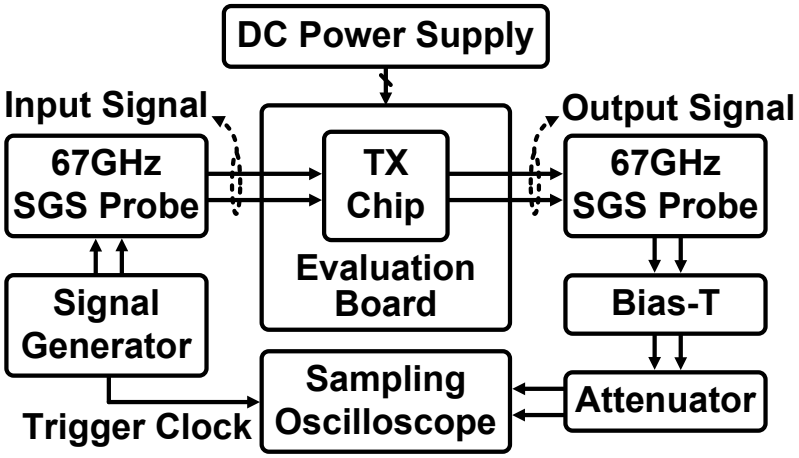


**Fig. 4.16 Time-domain measurement setup.**

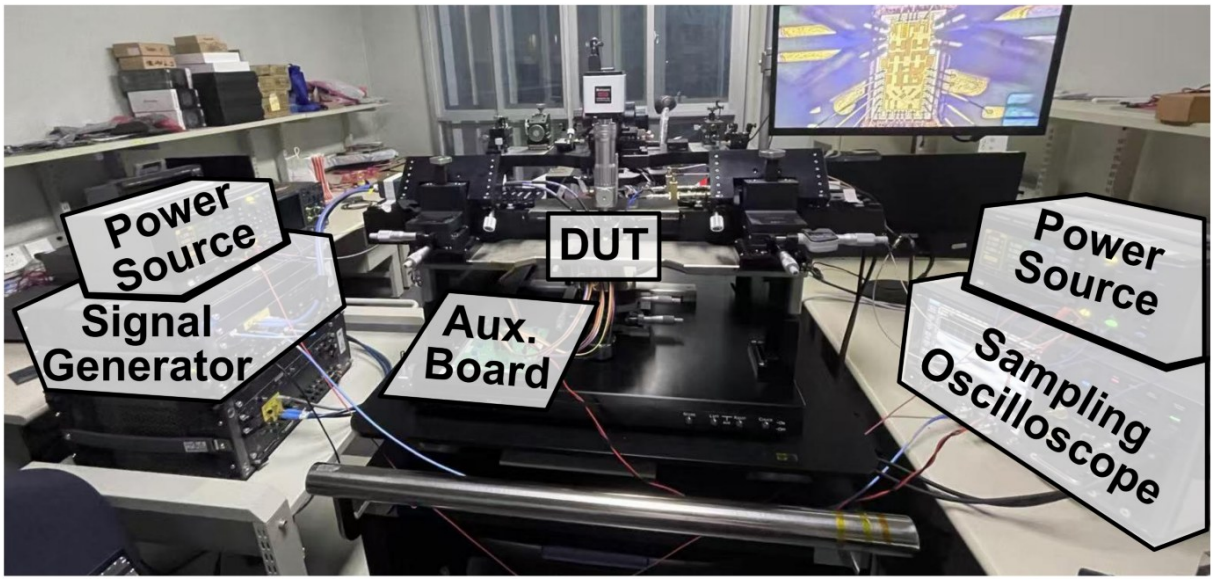


**Fig. 4.17 Photo of the time-domain measurement environment.**

Fig. 4.18 presents the measured NRZ and PAM-4 eye diagrams of the differential outputs of the driver at different data rates. As shown in the top row of Fig. 4.18, even without the help of FFE, the driver supports the amplification of both 56-Gbaud NRZ and 56-Gbaud PAM-4 signals with output swings of 4.8 $V_{ppd}$ and 4.3 $V_{ppd}$, respectively. For measurements with 80-Gbaud PAM-4 signals as shown in the middle row of Fig. 4.18, due to limited

bandwidth, the eye diagram of the driver output cannot be opened clearly. And then, with the FFE turned on, the eye diagram is clearly opened, with an output swing of 3.8 $V_{ppd}$ and an RLM of 95.8%. The FFE setting for the 80-Gbaud PAM-4 case is that the $V_{GAIN}$ for the 2nd pre-tap, 1st pre-tap, 1st post-tap, and 2nd post-tap Gm cells are set to 0, 1.2 V, 1.5 V, and 0.5 V, respectively. The measurements with 100-Gbaud NRZ signals exhibit a similar trend to those with 80-Gbaud PAM-4 signals, as shown in the bottom row of Fig. 4.18. The 100-Gbaud NRZ output cannot be clearly opened until the FFE is turned on. The FFE setting for 100-Gbaud NRZ case is that the $V_{GAIN}$ for the 2nd pre-tap, 1st pre-tap, 1st post-tap, and 2nd post-tap Gm cells are set to 0, 1.4 V, 1.9 V, and 0.5 V, respectively. For the six cases in Fig. 4.18, the signal patterns are all PRBS13.

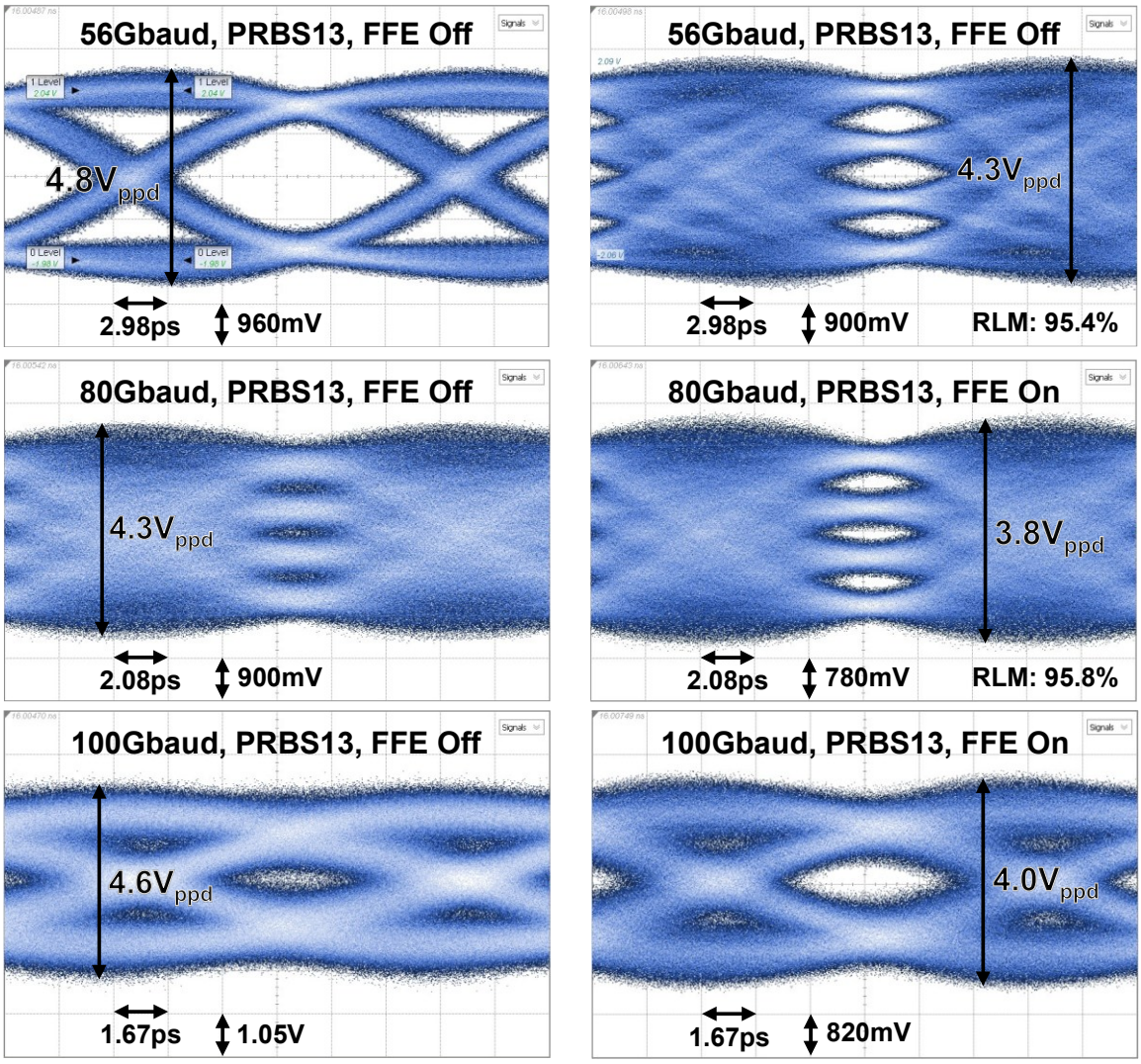


**Fig. 4.18 Measured NRZ and PAM-4 eye diagrams at different data rates.**

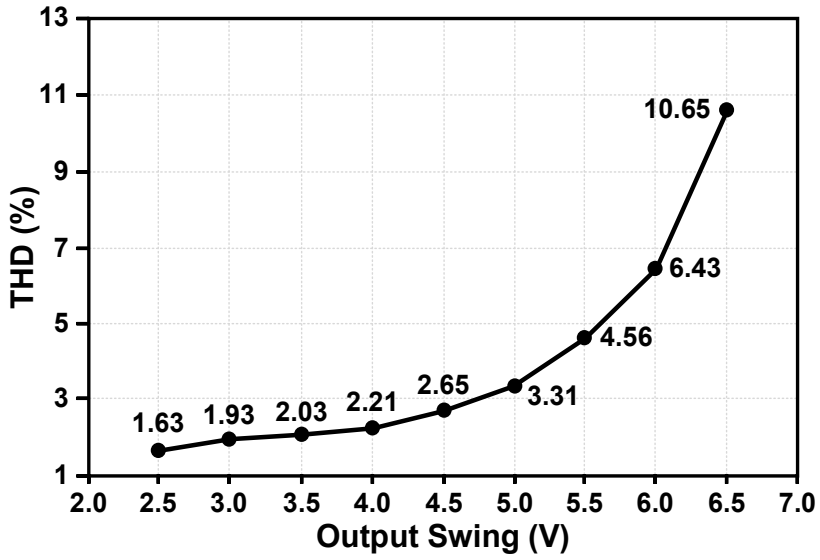


**Fig. 4.19 Measured THD at different output swings.**

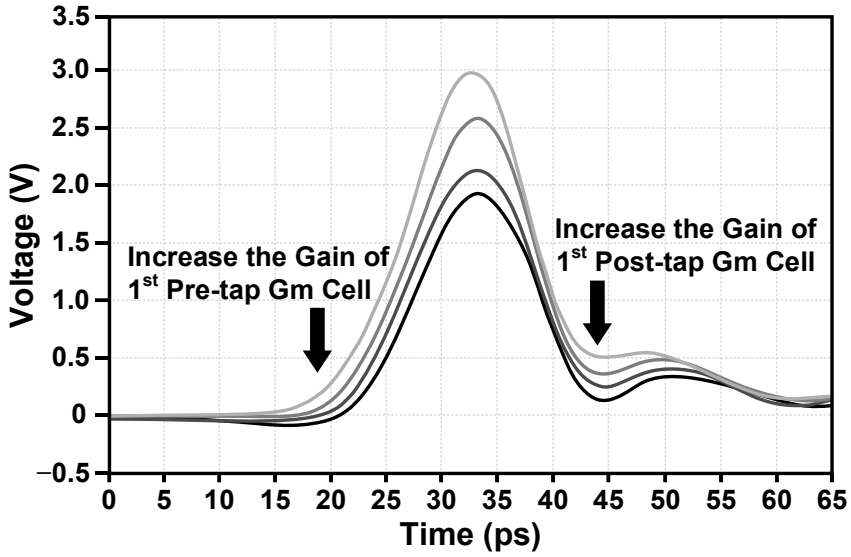


**Fig. 4.20 Measured pulse responses with different FFE settings.**

Fig. 4.19 presents the measured THDs of the differential outputs of the driver at different swings. The change of the output swing is obtained by varying the swing of the input signal. With the increase of the input swing, the output swing increases, and the THD deteriorates. This is because the increase of the input swing gradually saturates the bases of the common-emitter HBTs ($Q1_P/Q1_N$ in Fig. 4.11) and reduces the collector-emitter voltage headroom for both common-base HBTs ($Q2_P/Q2_N$ in Fig. 4.11) and common-emitter HBTs ($Q1_P/Q1_N$ in Fig. 4.11), resulting in the degradation of the linearity of the driver. When the

output swing of the driver reaches 4 $V_{ppd}$, a THD of 2.21% is achieved. And the THD is degraded dramatically when the output swing exceeds 6 $V_{ppd}$.

Fig. 4.20 shows the measured pulse responses of the driver with different settings for the 1st pre-tap and 1st post-tap Gm cells. When the two FFE Gm cells are switched off, the output pulse exhibits obvious pre- and post-cursors. With the $V_{GAIN}$ for the two FFE Gm cells increasing, the amplitude of the output pulse gradually decreases, and the pre- and post-cursors are mitigated significantly, demonstrating the effectiveness of the implemented built-in FFE.

### 4.4.3 Performance Summary

Table 4.1 summarizes the performance of the proposed linear distributed driver and compares this work with state-of-the-art linear drivers also in SiGe BiCMOS. Among linear drivers operating beyond 100 Gb/s, this work is the first design with built-in FFE using the proposed distributed amplifier topology which adopts TLs simultaneously as inductance and delay elements. Besides, the proposed distributed linear driver achieves the best FoM. The proposed topology allows easy extension of FFE tap number to satisfy the equalization requirements of LPO links with higher data rates and longer communication distances.

## 4.5 Conclusion

This chapter introduces a distributed amplifier topology with cross-folded transmission lines and cross-coupled Gm cells to simultaneously utilize transmission lines as inductance for parasitic mitigation and as delay elements for equalization. To verify the proposed topology, a distributed linear driver with 5-tap FFE is implemented. Frequency-domain measurement results show that the driver achieves a bandwidth of >67 GHz and a peaking gain of 6.9 dB at 50 GHz with the FFE turned on. The effectiveness of the proposed topology is further verified by time-domain measurement results. Clearly opened 3.8-$V_{ppd}$ 80-Gbaud PAM-4 and 4-$V_{ppd}$ 100-Gbaud NRZ eye diagrams are obtained with the FFE turned on. Moreover, the driver achieves a THD of 2.21% at 4-$V_{ppd}$ 5-GHz sinusoidal output.

**Table 4.1. Performance summary of the proposed linear driver and comparison with state-of-the-art works.**

| | [45] | [52] | [53] | [48] | This Work |
|---|---|---|---|---|---|
| SiGe Tech. Node | 130 | 130 | 130 | 55 | 130 |
| $f_T$ / $f_{MAX}$ [GHz] | 300/500 | 250/NA | 250/340 | 330/370 | 250/340 |
| Topology Type | Distributed, Linear | Lumped, Linear | Lumped, Linear | Hybrid, Linear | Distributed, Linear |
| Equalization in Driver | No | No | No | No | **5-tap FFE** |
| 3-dB Bandwidth (GHz) | 90 | >40 | 38 | >70 | >67 |
| Maximum Data Rate (Gb/s) | 120 @3$V_{ppd}$ NRZ | 138 @2.4$V_{ppd}$ PAM-4 | 112 @4.2$V_{ppd}$ PAM-4 | 256 @3.4$V_{ppd}$ PAM-4 | **160 @3.8$V_{ppd}$ PAM-4** |
| THD | <5.00% @1GHz, 3$V_{ppd}$ | 3.60% @1GHz, 6$V_{ppd}$ | 1.60% @1GHz, 6$V_{ppd}$ | <2.00% @1GHz, 3.6$V_{ppd}$ | **2.21% @5GHz, 4$V_{ppd}$** |
| DC Gain (dB) | 12.5 | 30.0 | 17.0 | 11.2~21.8 | 10.0~15.8 |
| Supply (V) | 5.5 | 5.5 | NA | 3.0/4.0 | 4.8 |
| Power (mW) | 550 | 1000 | 1040 | 725 | 612 |
| Area ($mm^2$) | 1.19 | 1.60 | 0.66 | 1.07* | 0.85 |
| $Z_O$** [Ω] | 100 | 100 | 100 | 100 | 100 |
| FoM***[bit/s/Hz] | 0.008 | 0.004 | 0.009 | 0.016 | **0.019** |

*Estimated single-channel area

**Differential output impedance matching

***$\text{FoM}=\frac{\text{Maximum Data Rate}}{f_T}\times\frac{(\text{Output Swing@Maximum Data Rate})^2}{8\times Z_O\times\text{Power Consumption}}$

# CHAPTER V

## Conclusions and Future Work

This thesis focuses on silicon-based transmitter integrated circuits design techniques to improve signal integrity and data rate for optical fiber communications. Three transmitter designs, including a 56-Gb/s quarter-rate PAM-4 VCSEL transmitter in 40-nm CMOS for short-reach optical communications, a 56-Gbaud half-rate linear modulator transmitter in 130-nm SiGe BiCMOS for long-haul optical communications, and a 100-Gbaud 4-$V_{ppd}$ distributed linear driver in 130-nm SiGe BiCMOS for linear pluggable optical links, have been presented.

For the 56-Gb/s PAM-4 VCSEL transmitter introduced in Chapter II, a piecewise compensation scheme is proposed to mitigate three imperfections of VCSELs including E/O gain nonlinearity, E/O bandwidth nonlinearity, and asymmetric response to rising/falling transitions. To implement the proposed compensation scheme, the transmitter prototype adopts a unary code-based structure, where three data slices with variable-Gm cells, 2-tap FFE, CTLE, and pre-emphasis circuit are deployed to independently control the widths, amplitudes, and skews of the three optical PAM-4 sub-eyes. The piecewise compensation scheme has been well verified by optical measurements with a commercial VCSEL, improving the average optical PAM-4 sub-eye amplitude/width, RLM and horizontal skew by 14%/12%, 38% and 63%, respectively.

For the 56-Gbaud linear modulator transmitter described in Chapter III, to extend the bandwidth of optical modulator-based links and enhance the OMA of generated optical signals, a 2-to-1 tap generator-less AMUX-FFE scheme and a dynamic triple-stacked linear driver topology are proposed. The AMUX-FFE utilizes the timing relationship between the half-rate data streams to achieve a 2/3-tap re-configurable FFE without the need for tap generator. The linear driver stacks three HBTs at the output stage and dynamically biases the bases of the top two HBT, to achieve a large output voltage swing without breakdown issues.

Fabricated in 130-nm SiGe BiCMOS, the transmitter supports the serialization and amplification for 56-Gbaud NRZ signal with an output swing of 7.3 $V_{ppd}$ and 56-Gbaud PAM-4 signal with an output swing of 4.2 $V_{ppd}$ according to the measurement results.

For the 100-Gbaud distributed linear driver introduced in Chapter IV, to further enhance the data rate of optical modulator-based links, a distributed amplifier topology with cross-folded transmission line and cross-coupled Gm cells is proposed. This topology simultaneously adopts transmission lines as inductance to cancel the parasitic capacitance from Gm cells and as delay elements to achieve built-in FFE. A distributed linear driver prototype with 5-tap built-in FFE is fabricated in 130-nm SiGe BiCMOS to verify the proposed topology. Measurement results show that, with the help of the FFE, the driver prototype supports the amplifications of 80-Gbaud PAM-4 and 100-Gbaud NRZ signals with output swings of 3.8 $V_{ppd}$ and 4.0 $V_{ppd}$, respectively.

In the future, the transmitters presented in this thesis can be further optimized from three aspects listed below.

1. In addition to the asymmetric response issue and nonlinearities in E/O gain and bandwidth, VCSEL is sensitive to temperature variation. When the VCSEL operates for a long time, its temperature will rise, resulting in the variation of E/O conversion characteristics and degrade the quality of the generated optical signal. The heat from surrounding transmitters further exacerbates the temperature rise. Therefore, the compensation techniques for VCSEL's temperature sensitivity are to be explored.
2. The equalization capabilities of the proposed linear modulator transmitter and distributed linear driver can be enhanced to boost the link speed further. For the linear modulator transmitter, the 2-to-1 AMUX-FFE can be upgraded to 4-to-1 or even 8-to-1 AMUX-FFE to achieve a FFE with more taps. For example, a 4-to-1 AMUX-FFE can be implemented by cascading two stages of the 2-to-1 AMUX-FFE presented in this thesis to achieve a FFE with a tap number of five, as depicted in Fig. 5.1. Moreover, the current version

AMUX-FFE relies on the re-timer inside the signal generator equipment to control the timing relationship between the half-rate data inputs, which is however not accurate and becomes one of bottlenecks for the data rate. In the future, the re-timer can be implemented on-chip using flip flops to solve the issue. For the distributed linear driver, more FFE Gm cells can be implemented to extend the FFE tap number. Additionally, the FFE Gm cells can be designed to be controllable delay cells to enable the adjustments of not only FFE coefficients but also FFE tap spacings.

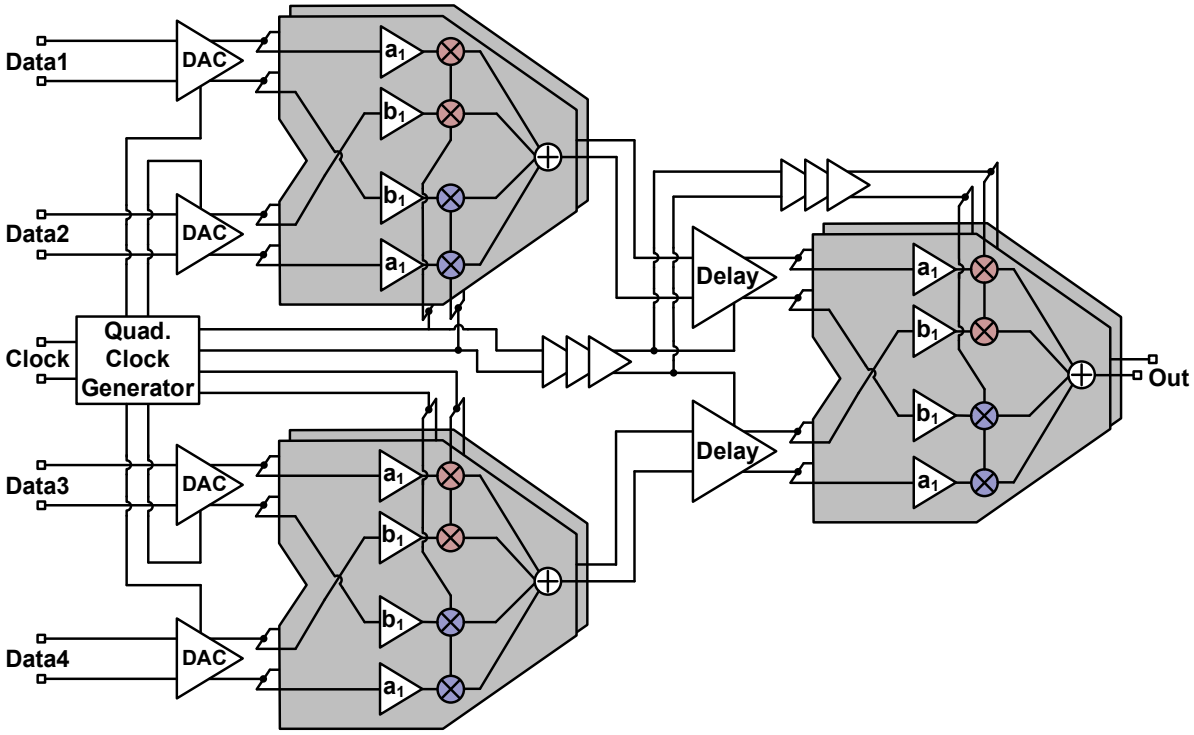


**Fig. 5.1 Architecture of a 4-to-1 tap generator-less AMUX-FFE with 5-tap inherent FFE.**

3. The power efficiency of the transmitters for optical modulators can be enhanced by adopting heterogeneous architecture. For example, the AMUX-FFE of the linear transmitter in Chapter III which merely performs signal processing, i.e. serialization, can be implemented in bulk CMOS technology to save power, while the linear driver which provides signal amplification can be designed in SiGe BiCMOS or compound semiconductor process such as GaN to enhance the gain and output swing. In this way, an optimal balance between energy efficiency and power output capability can be achieved.

The major issue of heterogeneous architecture is the impact of packaging components such as bond-wire on signal integrity. This degradation can be compensated by implementing equalization circuits such as FFE inside the signal processing chip. Additionally, with the advance of packaging technology, this issue can be further relieved.

# References


[1] IDC and Statista, "Volume of data/information created, captured, copied, and consumed worldwide from 2010 to 2020, with forecasts from 2021 to 2025," in *https://www.statista.com/statistics/871513/worldwide-data-created/*, June 7, 2021.

[2] Vincent Houtsma and Dora van Veen, "Higher-speed PONs based on data center technology and optics," *Journal of Optical Communications and Networking*, vol. 16, no. 2, pp. A98–A104, Feb. 2024.

[3] A.V. Krishnamoorthy, K.W. Goossen, W. Jan, X. Zheng, R. Ho, G. Li, R. Rozier, F. Liu, D. Patil, J. Lexau, H. Schwetman, D. Feng, M. Asghari, T. Pinguet, and J.E. Cunningham, "Progress in low-power switched optical interconnects," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 17, no. 2, pp. 357–376, March 2011.

[4] Gholami, D. Molin, and P. Sillard, "Compensation of chromatic dispersion by modal dispersion in MMF- and VCSEL-based gigabit Ethernet transmissions," *IEEE Photonics Technology Letters*, vol. 21, no. 10, pp. 645–647, May 15, 2009.

[5] A. Korichi, M. Hiekkamäki, and R. Fickler, "High-efficiency interface between multi-mode and single-mode fibers," *Optics Letters*, vol. 48, no. 4, pp. 1000–1003, Feb. 15, 2023.

[6] R. Puerta, M. Agustin, L. Chorchos, J. Tonski, J.R. Kropp, N. Ledentsov, V.A. Shchukin, N.N. Ledentsov, R. Henker, I.T. Monroy, J.J.V. Olmos, and J.P. Turkiewicz, "Effective 100 Gb/s IM/DD 850-nm multi- and single-mode VCSEL transmission through OM4 MMF," *Journal of Lightwave Technology*, vol. 35, no. 3, pp. 423–429, Feb. 2017.

[7] U. Hecht, N. Ledentsov, L. Chorchos, P. Scholz, P. Schulz, J.P. Turkiewicz, N.N. Ledentsov, and F. Gerfers, "120Gbit/s multi-mode fiber transmission realized with feed forward equalization using 28GHz 850nm VCSELs," in *45th European Conference on Optical Communication (ECOC 2019)*, Dublin, Ireland, Sep. 2019, pp. 85.

[8] J. Lavrencik, S. Varughese, N. Ledentsov, L. Chorchos, N.N. Ledentsov, and S.E. Ralph, "168Gbps PAM-4 multimode fiber transmission through 50m using 28GHz 850nm multimode VCSELs," in *2020 Optical Fiber Communications Conference and Exhibition (OFC)*, San Diego, CA, USA, March 2020, pp. 1–3.

[9] N.N. Ledentsov, O.Y. Makarov, V.A. Shchukin, V.P. Kalosha, N. Ledentsov, L. Chrochos, M.B. Sanayeh, and J.P. Turkiewicz, "High speed VCSEL technology and applications," *Journal of Lightwave Technology*, vol. 40, no. 6, pp. 1749–1763, March 2022.

[10] M. Morsy-Osman, M. Chagnon, M. Poulin, S. Lessard, and D.V. Plant, "224-Gb/s 10-km transmission of PDM PAM-4 at 1.3 μm using a single intensity-modulated laser and a direct-detection MIMO DSP-based receiver," *Journal of lightwave technology*, vol. 33, no. 7, pp. 1417–1424, April 2015.

[11] An Li, Zhihong Li, Yangjing Wen, Wei-Ren Peng, Yan Cui, and Yusheng Bai, "192-Gb/s 160-km transmission of carrier-assisted dual- polarization signal with Stokes vector direct detection," in *2016 Optical Fiber Communications Conference and Exhibition (OFC)*, Anaheim, CA, USA, March 2016, pp. 1–3.

[12] T.M. Hoang, Q. Zhuge, Z. Xing, M. Sowailem, M. Morsy-Osman, and D.V. Plant, "Single wavelength 480 Gb/s direct detection transmission over 80 km SSMF enabled by stokes vector receiver and reduced-complexity SSBI cancellation," in *2018 Optical Fiber Communications Conference and Exposition (OFC)*, San Diego, CA, USA, March 2018, pp. 1–3.

[13] E. Säckinger, *Broadband circuits for optical fiber communication*. New York, NY, USA: Wiley, 2005.

[14] G. Belfiore, R. Henker, and F. Ellinger, "40 Gbit/s 4-PAM VCSEL driver circuit with power roll-off compensation," in *2018 IEEE 61st International Midwest Symposium on Circuits and Systems (MWSCAS)*, Windsor, ON, Canada, Aug. 2018, pp. 747–750.

[15] M. Raj, M. Monge, and A. Emami, "A modelling and nonlinear equalization technique for a 20 Gb/s 0.77 pJ/b VCSEL transmitter in 32 nm SOI CMOS," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 8, pp. 1734–1743, Aug 2016.

[16] D. Kucharski, Y. Kwark, D. Kuchta, D. Guckenberger, K. Kornegay, M. Tan, Chao-Kun Lin, and A. Tandon, "A 20 Gb/s VCSEL driver with pre-emphasis and regulated output impedance in 0.13 μm CMOS," in *2005 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, Feb. 2005, pp. 222–594.

[17] L. Vivien and L. Pavesi, *Handbook of Silicon Photonics*. Boca Raton, FL, USA: CRC Press, 2013.

[18] N.C. Helman, J.E. Roth, D.P. Bour, H. Altug, and D.A.B. Miller, "Misalignment-tolerant surface-normal low-voltage modulator for optical interconnects," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 11, no. 2, pp. 338–342, March 2005.

[19] F. Yang, X. Fang, X. Chen, Y. Li, and F. Zhang, "Up to 360 Gb/s optical interconnects with ultra-high bandwidth thin film lithium niobate modulator," in *2022 Optical Fiber Communications Conference and Exhibition (OFC)*, San Diego, CA, USA, March 2022, pp. 1–3.

[20] M.S. Alam, X. Li, M. Jacques, Z. Xing, A. Samani, E. El-Fiky, P. Koh, and D. Plant, "Net 220 Gbps/λ IM/DD transmssion in O-band and C-band with silicon photonic traveling-wave MZM," *Journal of lightwave technology*, vol. 39, no. 13, pp. 4270–4278, July 2021.

[21] M.U. Sadiq, M.R. Gleeson, N. Ye, J. O'Callaghan, P. Morrissey, H.Y. Zhang, K. Thomas, A. Gocalinska, E. Pelucchi, F.C.G. Gunning, B. Roycroft, F.H. Peters, and B. Corbett, "10 Gb/s InP-based Mach-Zehnder modulator for operation at 2 μm wavelengths," *Optics Express*, vol. 23, no. 9, pp. 10905–10913, May 2015.

[22] A. Tyagi, T. Iwai, K. Yu, B. Wang, W. Sorin, S. Mathai, M. Tan, and S. Palermo, "A 50 Gb/s PAM-4 VCSEL transmitter with 2.5-tap nonlinear equalization in 65-nm CMOS," *IEEE Photonics Technology Letter*, vol. 30, no. 13, pp. 1246–1249, July 2018.

[23] P. Peng, P. Lee, H. Huang, W. Huang, M. Lin, Y. Juang, and S. Tseng, "A 56-Gb/s PAM-4 transmitter/receiver chipset with nonlinear FFE for VCSEL-based optical links in 40-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 57, no. 10, pp. 3025–3035, Oct. 2022.

[24] J. Hwang, H. Choi, H. Do, G. Jeong, D. Koh, K. Park, S. Kim, and D. Jeong, "A 64Gb/s 2.29pJ/b PAM-4 VCSEL transmitter with 3-tap asymmetric FFE in 65nm CMOS," in *2019 Symposium on VLSI Circuits (VLSI-C)*, Kyoto, Japan, 2019, pp. C268–C269.

[25] H. Do, J. Sull, S. Lee, K. Lee, and D. Jeong, "A 64 Gb/s 2.09 pJ/b PAM-4 VCSEL transmitter with bandwidth extension techniques in 40 nm CMOS," in *2021 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, Busan, Korea, 2021, pp. 1–3.

[26] A. Sharif-Bakhtiar, M.G. Lee, and A.C. Carusone, "A 40-Gbps 0.5-pJ/bit VCSEL driver in 28nm CMOS with complex zero equalizer," in *2017 IEEE Custom Integrated Circuits Conference (CICC)*, Austin, TX, USA, 2017, pp. 1–4.

[27] S. Mondal, J. Qiu, S. Krishnamurthy, J. Kennedy, S. Bose, T. Acikalin, S. Yamada, J. Jaussi, and M. Mansuri, "A 4×64Gb/s NRZ 1.3pJ/b co-packaged and fiber-terminated 4-ch VCSEL-based optical transmitter," in *2024 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2024, pp. 1–3.

[28] F. Chen, C. Zhang, L. Wang, Q. Pan, and C.P. Yue, "A 2.05-pJ/b 56-Gb/s PAM-4 VCSEL transmitter with piecewise nonlinearity compensation and asymmetric equalization in 40-nm CMOS," in *2023 IEEE 49th European Solid State Circuits Conference (ESSCIRC)*, Lisbon, Portugal, Sep. 2023, pp. 373–376.

[29] X. Zheng, H. Ding, F. Zhao, D. Wu, L. Zhou, J. Wu, F. Lv, J. Wang, and X. Liu, "A 50–112-Gb/s PAM-4 transmitter with a fractional-spaced FFE in 65-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 7, pp. 1864–1876, July 2020.

[30] Z. Zhang, G. Zhu, C. Wang, L. Wang, and C.P. Yue, "A 32-Gb/s 0.46-pJ/bit PAM4 CDR using a quarter-rate linear phase detector and a self-biased PLL-based multiphase clock generator," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 10, pp. 2734–2746, Oct. 2020.

[31] K. Kanda, D. Yamazaki, T. Yamamoto, M. Horinaka, J. Ogawa, H. Tamura, and H. Onodera, "40Gb/s 4:1 MUX/1:4 DEMUX in 90nm standard CMOS," in *2005 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2005, pp. 152–590.

[32] J. Lee, P. Chiang, P. Peng, L. Chen, and C. Weng, "Design of 56 Gb/s NRZ and PAM4 SerDes transceivers in CMOS technologies," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 9, pp. 2061–2073, Sep. 2015.

[33] M. Verplaetse, H. Ramon, N. Singh, B. Moeneclaey, P. Ossieur, and G. Torfs, "A 4-to-1 240 Gb/s PAM-4 MUX with a 7-tap mixed-signal FFE in 55nm BiCMOS," in *2021 IEEE Custom Integrated Circuits Conference (CICC)*, Austin, TX, USA, 2021, pp. 1–2.

[34] X. Zheng, C. Zhang, F. Lv, F. Zhao, S. Yuan, S. Yue, Z. Wang, F. Li, Z. Wang, and H. Jiang, "A 40-Gb/s quarter-rate SerDes transmitter and receiver chipset in 65-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 11, pp. 2963–2978, Nov. 2017.

[35] A. Momtaz and M.M. Green, "An 80 mW 40 Gb/s 7-Tap T/2-spaced feed-forward equalizer in 65 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 3, pp. 629–639, March 2010.

[36] B. Razavi, "Design techniques for high-speed wireline transmitters," *IEEE Open Journal of Solid-State Circuits*, vol. 1, pp. 53–66, Sep. 2021.

[37] N.N. Ledentsov, O.Y. Makarov, V.A. Shchukin, V.P. Kalosha, N. Ledentsov, L. Chrochos, M.B. Sanayeh, and J.P. Turkiewicz, "High speed VCSEL technology and applications," *Journal of Lightwave Technology*, vol. 40, no. 6, pp. 1749–1763, March 2022.

[38] J. Han, Y. Lu, N. Sutardja, K. Jung, and E. Alon, "Design techniques for a 60 Gb/s 173 mW wireline receiver frontend in 65 nm CMOS technology," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 4, pp. 871–880, April 2016.

[39] S. Kiran, S. Cai, Y. Luo, S. Hoyos, and S. Palermo, "A 52-Gb/s ADC-based PAM-4 receiver with comparator-assisted 2-bit/stage SAR ADC and partially unrolled DFE in 65-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 3, pp. 659–671, March 2019.

[40] M.H. Kashani, H. Shakiba, and A. Sheikholeslami, "A low-power high-BW PAM4 VCSEL driver with three-tap FFE in 12-nm CMOS FinFET process," *IEEE Journal of Solid-State Circuits*, vol. 59, no. 7, pp. 1995–2004, July 2024.

[41] H. Wakita, M. Nagatani, K. Kurishima, M. Ida, and H. Nosaka, "An over-67-GHz-bandwidth 2 Vppd linear differential amplifier with gain control in 0.25-um InP DHBT technology," in *2016 IEEE MTT-S International Microwave Symposium (IMS)*, San Francisco, CA, USA, May 2016, pp. 1–3.

[42] R.J.A. Baker, J. Hoffman, P. Schvan, and S.P. Voinigescu, "SiGe BiCMOS linear modulator drivers with 4.8-Vpp differential output swing for 120-GBaud applications," in *2017 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Honolulu, HI, USA, June 2017, pp. 260–263.

[43] A. El-Aassar and G.M. Rebeiz, "A DC-to-108-GHz CMOS SOI distributed power amplifier and modulator driver leveraging multi-drive complementary stacked cells," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 12, pp. 3437–3451, Dec. 2019.

[44] T. Lee, J. Zhang, S. Hong, C. Hsu, S. Li, S. Chen, S. Shyh-Shyuan, C. Wu, and S.S.H. Hsu, "A low power CMOS driver integrated with Mach-Zehnder modulator for PAM4 optical transmissions," in *2020 50th European Microwave Conference (EuMC)*, Utrecht, Netherlands, Jan. 2021, pp. 328–331.

[45] P. Rito, I.G. Liopez, A. Awny, A.C. Ulusoy, and D. Kissinger, "A DC-90 GHz 4-Vpp differential linear driver in a 0.13 μm SiGe:C BiCMOS technology for optical modulators," in *2017 IEEE MTT-S International Microwave Symposium (IMS)*, Honololu, HI, USA, June 2017, pp. 439–442.

[46] A. Fatemi, G. Kahmen, and A. Malignaggi, "A multi-mode linear optical modulator driver circuit in 130 nm SiGe BiCMOS technology," in *2021 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, Monterey, CA, USA, Dec. 2021, pp. 1–4.

[47] J.H. Choi and N. Nijanandi, "120 GBd 2.8 Vpp,diff low-power differential driver for InP Mach–Zehnder modulator using 55-nm SiGe HBTs," *IEEE Microwave and Wireless Technology Letters*, vol. 33, no. 6, pp. 871–874, June 2023.

[48] S. Niu, R. Ahmed, J. Lambrecht, J. Declercq, M. Verbeke, M. Verplaetse, B. Moeneclaey, C. Wang, J.V. Kerrebrouck, N. Singh, J. Bauwelinck, and X. Yin, "A linear modulator driver with over 70-GHz bandwidth 21.8-dB gain and 3.4-Vppd output swing for beyond 120-GBd optical links," *IEEE Transactions on Microwave Theory and Techniques*, vol. 72, no. 7, pp. 4080–4091, July 2024.

[49] R. Hersent, T.K. Johansen, V. Nodjiadjim, F. Jorge, B. Duval, F. Blache, M. Riet, C. Mismer, J. Renaudier, and A. Konczykowska, "InP DHBT linear modulator driver with a 3-Vppd PAM-4 output swing at 90 GBaud: from enhanced transistor modeling to integrated circuit design," *IEEE Transactions on Microwave Theory and Techniques*, vol. 72, no. 3, pp. 1618–1633, March 2024.

[50] S. Mandegaran and A. Hajimiri, "A breakdown voltage multiplier for high voltage swing drivers," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 2, pp. 302–312, Feb. 2007.

[51] Knochenhauer, J.C. Scheytt, and F. Ellinger, "A compact, low-power 40-GBit/s modulator driver with 6-V differential output swing in 0.25-µm SiGe BiCMOS," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 5, pp. 1137–1146, May 2011.

[52] A.H. Ahmed, A.E. Moznine, D. Lim, Y. Ma, A. Rylyakov, and S. Shekhar, "A dual-polarization silicon-photonic coherent transmitter supporting 552 Gb/s/wavelength," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 9, pp. 2597–2608, Sep. 2020.

[53] F. Chen, C.P. Yue, and Q. Pan, "A 56-Gbaud 7.3-Vppd linear modulator transmitter with AMUX-based reconfigurable FFE and dynamic triple-stacked driver in 130-nm SiGe BiCMOS," in *2024 IEEE Custom Integrated Circuits Conference (CICC)*, Denver, CO, USA, Apr. 2024, pp. 1–2.

[54] H. Yamazaki, M. Nagatani, S. Kanazawa, H. Nosaka, T. Hashimoto, A. Sano, and Y. Miyamoto, "Digital-preprocessed analog-multiplexed DAC for ultrawideband multilevel transmitter," *Journal of Lightwave Technology*, vol. 34, no. 7, pp. 1579–1584, Apr. 2016.

[55] T. Tannert, Xuan-Quang Du, D. Widmann, M. Grozing, M. Berroth, C. Schmidt, C. Caspar, Jung Han Choi, V. Jungnickel, and R. Freund, "A SiGe-HBT 2:1 analog multiplexer with more than 67 GHz bandwidth," in *2017 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, Miami, FL, USA, Oct. 2017, pp. 146–149.

[56] H. Ramon, M. Verplaetse, M. Vanhoecke, H. Li, J. Bauwelinck, P. Ossieur, X. Yin, and G. Torfs, "A 700mW 4-to-1 SiGe BiCMOS 100GS/s analog time-interleaver," in *2020 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, Feb. 2020, pp. 214–216.

[57] M. Collisi and M. Moller, "Resolution-related design considerations for a 120-GS/s 8-bit 2:1 analog multiplexer in SiGe-BiCMOS technology," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 9, pp. 2624–2634, Sep. 2021.

[58] M. Nagatani, H. Wakita, H. Yamazaki, Y. Ogiso, M. Mutoh, M. Ida, F. Hamaoka, M. Nakamura, T. Kobayashi, Y. Miyamoto, and H. Nosaka, "A beyond-1-Tb/s coherent optical transmitter front-end based on 110-GHz-bandwidth 2:1 analog multiplexer in 250-nm InP DHBT," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 9, pp. 2301–2315, Sep. 2020.

[59] Jihwan Kim, A. Balankutty, R. Dokania, A. Elshazly, Hyung Seok Kim, S. Kundu, S. Weaver, Kai Yu, and F. O'Mahony, "A 112Gb/s PAM-4 transmitter with 3-Tap FFE in 10nm CMOS," in *2018 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, Feb. 2018, pp. 102–104.

[60] P. Peng, Y. Chen, S. Lai, and H. Huang, "A 112-Gb/s PAM-4 voltage-mode transmitter with four-tap two-step FFE and automatic phase alignment techniques in 40-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 7, pp. 2123–2131, July 2021.

[61] Z. Wang, M. Choi, K. Lee, K. Park, Z. Liu, A. Biswas, J. Han, S. Du, and E. Alon, "An output bandwidth optimized 200-Gb/s PAM-4 100-Gb/s NRZ transmitter with 5-Tap FFE in 28-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 57, no. 1, pp. 21–31, Jan. 2022.

[62] G. Scotti, D. Bellizia, A. Trifiletti, and G. Palumbo, "Design of low-voltage high-speed CML D-latches in nanometer CMOS technologies," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 25, no. 12, pp. 3509–3520, Dec. 2017.

[63] P. Heydari and R. Mohanavelu, "Design of ultrahigh-speed low-voltage CMOS CML buffers and latches," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 12, no. 10, pp. 1081–1093, Oct. 2004.

[64] F. Iseini, A. Malignaggi, F. Korndorfer, M. Inac, and G. Kahmen, "Lumped ultra-broadband linear driver in 130 nm SiGe SG13G3 technology," in *2022 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, Phoenix, AZ, USA, Oct. 2022, pp. 136–139.

[65] X. Wang, X. He, and H. Ren, "Advanced FEC for 200 Gb/s transceiver in 800 GbE and 1.6 TbE standard," *IEEE Communications Standards Magazine*, vol. 7, no. 3, pp. 56–62, Sep. 2023.

[66] Y. Ayasli, S.W. Miller, R. Mozzi, and L.K. Hanes, "Capacitively coupled traveling-wave power amplifier," *IEEE Transactions on Microwave Theory and Techniques*, vol. 32, no. 12, pp. 1704–1709, Dec. 1984.

[67] Hongjong Park, Sangho Lee, Kwangseok Choi, Jihoon Kim, Hyosung Nam, Jaeduk Kim, Wangyong Lee, Changhoon Lee, Junghyun Kim, and Youngwoo Kwon, "A 6-18 GHz GaN distributed power amplifier using reactive matching technique and simplified bias network," in *2017 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Honolulu, HI, USA, June 2017, pp. 394–397.

[68] Y. Zhang and K. Ma, "A 2–22 GHz CMOS distributed power amplifier with combined artificial transmission lines," *IEEE Microwave and Wireless Components Letters*, vol. 27, no. 12, pp. 1122–1124, Dec. 2017.

[69] P.V. Testa, C. Carta, U. Jorges, and F. Ellinger, "Analysis and design of a 30- to 220-GHz balanced cascaded single-stage distributed amplifier in 130-nm SiGe BiCMOS," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 5, pp. 1457–1467, May 2018.

[70] H.T. Nguyen, D. Jung, and H. Wang, "A 60GHz CMOS power amplifier with cascaded asymmetric distributed-active-transformer achieving watt-level peak output power with 20.8% PAE and supporting 2Gsym/s 64-QAM modulation," in *2019 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, Feb. 2019, pp. 90–92.

[71] A. Kazan and G.M. Rebeiz, "A 10-130 GHz distributed power amplifier achieving 2.6 THz GBW with peak 13.1 dBm output P1dB for ultra-wideband applications in 90nm SiGe HBT technology," in *2021 IEEE BiCMOS and Compound Semiconductor*

*Integrated Circuits and Technology Symposium (BCICTS)*, Monterey, CA, USA, Dec. 2021, pp. 1–4.

[72] A. Momtaz and M.M. Green, "An 80 mW 40 Gb/s 7-Tap T/2-spaced feed-forward equalizer in 65 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 3, pp. 629–639, March 2010.

[73] Ming-Shuan Chen and C.K. Yang, "A 50–64 Gb/s serializing transmitter with a 4-tap, LC-ladder-filter-based FFE in 65 nm CMOS technology," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 8, pp. 1903–1916, Aug. 2015.

[74] Ye, G. Wu, W. Gai, K. Sheng, and Y. He, "A 0.43pJ/b 200Gb/s 5-Tap delay-line-based receiver FFE with low-frequency equalization in 28nm CMOS," in *2023 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, Feb. 2023, pp. 112–114.

# List of Publications and Patents

## Publications

[1] **F. Chen**, C. P. Yue and Q. Pan, "A 100Gbaud 4$V_{ppd}$ distributed linear driver with cross-folded transmission lines and cross-coupled Gm cells for built-in 5-tap FFE in 130nm SiGe BiCMOS," in *2025 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, Feb. 2025. (Accepted)

[2] **F. Chen**, C. P. Yue and Q. Pan, "A 56-Gbaud 7.3-$V_{ppd}$ linear modulator transmitter with AMUX-based reconfigurable FFE and dynamic triple-stacked driver in 130-nm SiGe BiCMOS," in *2024 IEEE Custom Integrated Circuits Conference (CICC)*, Denver, CO, USA, April 2024, pp. 1-2.

[3] **F. Chen**, C. Zhang, L. Wang, Q. Pan and C. P. Yue, "A 2.05-pJ/b 56-Gb/s PAM-4 VCSEL transmitter with piecewise nonlinearity compensation and asymmetric equalization in 40-nm CMOS," in *2023 IEEE 49th European Solid State Circuits Conference (ESSCIRC)*, Lisbon, Portugal, Sep. 2023, pp. 373-376.

[4] **F. Chen**, C. Zhang, T. Min, B. Xu, Q. Pan and C. P. Yue, "Design and co-simulation of QPSK and NRZ/PAM-4/PAM-8 VCSEL-based optical links utilizing an integrated system evaluation engine," in *2021 IEEE 14th International Conference on ASIC (ASICON)*, Kunming, China, Oct. 2021, pp. 1-4.

[5] **F. Chen**, C. Zhang, L. Wang, Q. Pan and C. P. Yue, " A 56-Gb/s PAM-4 VCSEL transmitter with piecewise compensation scheme in 40-nm CMOS," submitted to *IEEE Journal of Solid-State Circuits*. (Under Review)

[6] C. Zhang, **F. Chen** and C. P. Yue, "A 56-Gb/s PAM-4 transmitter using silicon photonic micro-ring modulator in 40nm CMOS," in *2022 IEEE 65th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Fukuoka, Japan, Aug. 2022, pp. 1-4.

[7] S. Feng, **F. Chen**, Z. Li, W. Zhou, D. Xu, C.-Z. Chen, X. Liu, H. Wu and Q. Pan, "A 4-$V_{ppd}$ 160-Gb/s PAM-4 optical modulator driver with all-pass filter-based dynamic bias and 2-Tap FFE in 130-nm BiCMOS," in *2022 IEEE Asia Pacific Conference on Circuits*

*and Systems (APCCAS)*, Shenzhen, China, Nov. 2022, pp. 1-5.

[8] W. Shi, **F. Chen**, X. Liu, C. Zhang, Z. Liu, T. Min, B. Xu, L. Wang, J. Kang and C. P. Yue, "An Integrated System Evaluation Engine for Cross-Domain Simulation and Design Optimization of High-Speed 5G Millimeter-Wave Wireless SoCs," in *2021 IEEE 14th International Conference on ASIC (ASICON)*, Kunming, China, Oct. 2021, pp. 1-4.

[9] C. Zhang, L. Wang, Z. Liu, **F. Chen**, Q. Pan, X. Li and C. P. Yue, "A 48-Gb/s half-rate PAM4 optical receiver with 0.27-pJ/bit TIA efficiency, 1.28-pJ/bit RX efficiency, and 0.06-mm$^2$ area in 28-nm CMOS," in *2024 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, Honolulu, HI, USA, June 2024, pp. 1-2.

[10] Q. Pan, X. Luo, Z. Li, Z. Jia, **F. Chen**, X. Ding and C. Patrick Yue, "A 26-Gb/s CMOS optical receiver with a reference-less CDR in 65-nm CMOS," *Journal of Semiconductors*, vol. 43, no. 7, pp. 072401, 2022.

## Patents

[1] C. P. Yue, **F. Chen**, X. Liu. A Low-distortion PAM-4 Optical Transmitter. US Patent. (Provisional)

[2] **F. Chen**, C. P. Yue. A Low-distortion PAM-4 Optical Transmitter. China Invention Patent, Patent No.: CN116192268A.

[3] Q. Pan, **F. Chen**, C. Wang, S. Feng, Z. Jia. A High Output Swing Driver. China Invention Patent, Patent No.: CN115021694A.