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EMI Related Common-Mode Noise Analysis in High-Speed Backplane Links

by

Duona LUO

A Thesis Submitted to

The Hong Kong University of Science and Technology

in Partial Fulfillment of the Requirements for

the Degree of Doctor of Philosophy

in the Department of Electronic and Computer Engineering

January 2018, Hong Kong

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This is to certify that I have examined the above Ph.D. thesis
and have found that it is complete and satisfactory in all respects,
and that any and all revisions required by
the thesis examination committee has been made.

Prof. C. Patrick YUE, ECE Department (Thesis Supervisor)

Prof. Bert SHI, Head of ECE Department

Thesis Examination Committee

1. Prof. C. Patrick YUE (Supervisor)	Department of Electronic and Computer Engineering
2. Prof. Pak Wo LEUNG	Department of Physics
3. Prof. Man Sun CHAN	Department of Electronic and Computer Engineering
4. Prof. Volkan KURSUN	Department of Electronic and Computer Engineering
5. Prof. Jinglei YANG	Department of Mechanical and Aerospace Engineering
6. Prof. Jri LEE (External Examiner)	Department of Electrical Engineering, National Taiwan University

Department of Electronic and Computer Engineering,
The Hong Kong University of Science and Technology
January 2018

To my parents

To Zhao Min

R.I.P.

Abstract

Due to the rapid growth of the data traffic and the integration density of systems, the electromagnetic compatibility (EMC) of communication circuits is increasingly challenging to accomplish. In modern data centers, thousands of paralleled backplane communication links enable the tremendous volume of data throughput. However, these backplane links also generate undesired electromagnetic interference (EMI), which can potentially cause system malfunction.

In a typical backplane communication link, differential non-return-to-zero (NRZ) signaling has been widely used for years. However, non-linear distortion of differential NRZ signals leads to a large common-mode (CM) noise at the double Nyquist frequency, which is a primary source of EMI. Therefore, the first half of the thesis focuses on investigating the CM noise of NRZ signals to understand the EMI issue in high-speed backplane links. Similar to the NRZ signaling, 4-level pulse amplitude modulation (PAM-4), which is the key solution for the next generation of 200/400 GbE communications, also suffers from the similar EMI problems. Hence, the second half of the thesis focuses on the EMI-related CM noise of PAM-4 signals.

In the first half, the analysis of EMI-related CM noise of differential NRZ signals is presented from a circuit design perspective. A current-mode logic (CML) driver circuit is used for analysis and simulations. It is observed that the CM noise is correlated with the data rate, amplitude, and mismatch of rising and falling edges. Accordingly, a method for EMI reduction is proposed by optimizing the signal swing and the biasing voltage of the circuit. The proposed method is experimentally verified on a test chip fabricated in a 65 nm CMOS process.

In the second half, the analysis of PAM-4 signals is presented, showing a correlation between the EMI-related CM noise and the system architecture. It is observed that the CM noise of a PAM-4 transmitter with a thermometer-coded architecture is intrinsically lower than the CM noise of a

transmitter with a typical binary-scaled architecture. Hence, a mathematical expression is derived to estimate the CM noise of the PAM-4/8/16 signals, and transistor-level simulations in a 65 nm CMOS process are performed to further evaluate the correlation between the CM noise and the system architecture.

Acknowledgement

Time flies, and it is finally to say goodbye and embrace the new commencement.

It is still reminding me the moment when four years ago, I nervously walked towards the end of the corridor on the 2nd floor of ECE department, opened the office door, and had my ever first talk with my supervisor, Prof. Patrick Yue. Then, my UST story began there.

He is the definitely the first person I would like to thank for going through all these years and experiencing all these joys, pains, and gains. His industrial insights and his passionate about emerging technologies motivate me and inspire me to find my future direction. His strong academic background guide and support me through all the hard research works. It is just wordless to describe or summarize the Ph.D. career within a few sentences, but everything is more than worthy to be memorized, and for sure, I will remember.

There is an old Chinese saying that “when walking along with two others, you must be able to learn from them”. I truly appreciate having all those friends, mentors, and even haters during my Ph.D. career.

I still remember two years ago, when we fought together against the tape-out deadline in the old Rm. 3112 lab until the late midnight. Blair supported us with some homemade delicious food, Yipeng was taking the lead for the whole project, Robin was busy with his huge PA, and I was just eating the cookies and cakes there, and talking to them on some funny jokes and keeping them awake. It is truly the old memorable glorious days. I profoundly hope the guys and girl all doing smoothly these days.

First, to my best lab mates, Yipeng Wang, Babar, Blair Liwen Jing, Robin Zhenxiong Hou, Lucas Zhixin Li, Guang Zhu, Liusheng Sun, Haikun Jia, Raju, Milad, George Fengyu Che, Alex Quan Pan, Liang Wu, Xianbo Li, Qasim, Li Wang, Zhao Zhang, Xiangyu Meng, Sam Can Wang,

Kanghui Zhao, Xuan Wu, Mr. Luk, Mr. KW Chan, Leon Ziang Chen, Feng Zhang, and all those people who helped me before, I sincerely appreciate your support and wish you all a pleasant life and a good health.

Subsequently, I am also so grateful to my thesis committee, Prof. Kursun Volkan, Prof. Mansun Chan, Prof. Kai Tang, and Prof. Jri Lee. Thank you all for your valuable support and guidance. It is really a great honor to have you all witness the milestone moment of my career.

Besides the academic life, I have had several years of great experience serving the mainland society in UST, which is called the Mainland Students and Scholars Society (MSSS). I have met great people in the society, who inspired me so much and influence me so much, like the "global vision local commitment" from our president Tony, as well as the "being generally generous" from the most beloved vice-president Eden Woon. In addition, I truly treasure the brotherhood and the purest friendship with Weiguang Ye, David Wei Yang, Jie Liu, Yuchen Wang, Yuanhao Huang, Meng Lang, Xiaoyuan Zhang, Tianyi Tan, Weiqi Huang, Jiaqi Wei and all the other brothers and sisters in the society. Serving a community is not about gaining research papers or professional knowledge, but it rewards me with much more valuable satisfactions and social skills.

Last, but obviously not the least, I would like to express my grateful appreciation to my mother, Qunhua Chen, and my father, Ningping Luo. They have supported me in the background for over 27 years. To be honest, I have to apologize that during the past eight years since my college, I barely have time being together with them and look after them. I do not need to say too much dedication to them, but just wish I could slow down the aging on them, and could always be there when they need me, just like during my childhood, I could always find them when I needed them.

All the best to all the life passengers I have met.

Again, thank you all.

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Chapter 1 Introduction

1.1 Background Introduction and Research Motivation

"Bigger data, smaller world."

It is a brief but precise description of the current information technology industry.

People are so optimistic about our future technologies for the true "big data" era. By that time, everything, everyone, and every event will be connected, and tons of data will be generated and collected with a second. Emerging technologies, like 5G, big data, cloud computing, and the internet of things (IoT), empower all these final fantasies into our daily true lives. However, the static data, generated by every entity in the huge network, has no meaning until the intercommunication channels are built for data collection and exchange. As the increasingly larger amount of entities are accessing the internet, the data volume is booming, and the background engineers, who are the actual technology enablers, are really facing new challenge and trouble.

The trouble comes from the not only the need of more interactive, reliable, and easily accessible data platform from end users and data consumers, but also from the necessary implementation of big data tunnels with tremendous throughput. In terms of constructing the data tunnels, data center applications are inevitably involved. It is the fundamental infrastructure used to house computing systems, associated storage systems, and the communication components [1]. In general, it is the most required fundamental elements for future communications, like 5G, IoT, and cloud services. Fig. 1.1 shows part of a data center of Cisco. It occupies several floors of the entire building, and it is equipped with advanced power and cooling systems. Most of the inner devices are in the form of server racks mounted in large cabinets or containers. Each server rack consists of the computing elements, storage elements, and the communication modules.

Fig. 1.1 Cisco data center [2].

Fig. 1.2 shows the forecast of the communication transceiver modules for global web-scale intra-data center applications. The infrastructures for 40 GbE standards will be totally replaced by the 100 GbE infrastructures within the next 5 years, or even less, which means the intercommunication speed will be doubled by the time when all the 40 GbE module are replaced by 100 GbE modules.

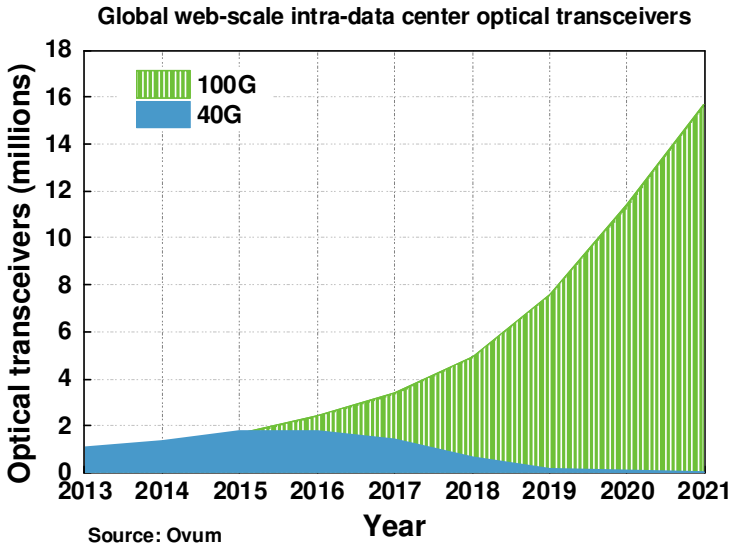


Fig. 1.2 40/100 GbE transceiver forecast of global data center applications [3]

However, it is to be clearly noted that, upgrades of the communication speed is not just building more data centers, but squeeze more communication modules into a limited space. It means, the data centers will have a higher density of unit cells, and the distance of each communication unit

is shortened. Higher communication data rate of 100 GbE, or even 200/400 GbE [4], [5], means higher density of unit cells, and it makes the reliability requirement of the system integration much more strict than the previous case in 40/100 GbE infrastructures.

Inevitably, the shortened distance between the communication cells increases the risk of electromagnetic interference (EMI). EMI is a disturbance generated by an external source that affects an electrical circuit by electromagnetic induction, electrostatic coupling, or conduction. The disturbance may degrade the performance of the circuit or even stop it from functioning. In the case of a data path, these effects can range from an increase in error rate to a total loss of the data. Both man-made and natural sources generate changing electrical currents and voltages that can cause EMI: automobile ignition systems, mobile phones, thunderstorms, the Sun, and the Northern Lights [6]. Electromagnetic interference can be categorized as narrowband EMI and broadband EMI. Narrowband EMI typically emanates from intended transmissions, such as radio and TV stations or mobile phones. While the broadband EMI is unintentional radiation from sources such as electric power transmission lines.

Switching loads (inductive, capacitive, and resistive), such as electric motors, transformers, power supplies, etc., all cause electromagnetic interference, especially at large power consumption. However, the switched-mode power supplies can be a source of EMI but have become less of a problem as design techniques have improved, such as integrated power factor correction.

In the data center, obviously, the potential EMI inside the data center mainly comes from the unintentional radiations from the unit communication cells. There are hundreds of communication units on one server rack, which make the electromagnetic environment inside the rack is extremely complicated. In order to keep the server functional, international standards and regulations are developed to constrain the electromagnetic radiation intensity.

Most countries have legal requirements that mandate electromagnetic compatibility (EMC): electronic and electrical devices should work correctly when exposed to a certain amount of EMI, and should not emit a too large amount of EMI, which could interfere with other electrical systems. In the United States, the 1982 Public Law 97-259 allowed the Federal Communications Commission (FCC) to regulate the susceptibility of consumer electronic equipment [7]. For the unintentional radiations from the electrical devices inside the data center, Code of Federal Regulations, Title 47, Part 15 (47 CFR 15) is one part of FCC rules that can be applied [8].

It regulations regarding unlicensed transmissions, and it regulates everything from spurious emissions to unlicensed low-power broadcasting. Nearly every electronics device radiates unintentional emissions and must comply with Part 15 before it gets into the US market. According to the FCC regulations, the radiated electric field strength at a 3-meter distance from the device should not exceed the limitations in Table I [9].

Table I FCC 3-meter measurement regulation

Frequency of Emission (MHz)	**Field Strength (uV/m)**	**Field Strength (dBuV/m)**
30 – 88	100	40
88 – 216	150	43.5
216 – 960	200	46
Above 960	500	54

Besides the FCC regulations, CISPR 22 is the analog standard to European standard EN 55022, which is often referenced in all European EMC standards, defining measurement methods, measurement equipment, limit lines and interpretation of the applicability of limit lines, starting from household appliances to medical devices. According to the CISPR 22, the limitation for the radiated emission from 30 MHz to 6 GHz is shown in Fig. 1.3. When compared to the FCC regulations mentioned above, the CISPR 22 extended the specified frequency range up to 6 GHz,

and the limit values in both standards are quite similar. The comparison of Title 47 CFR 15, FCC and EM 55022, CISPR 22 are plotted in Fig. 1.4.

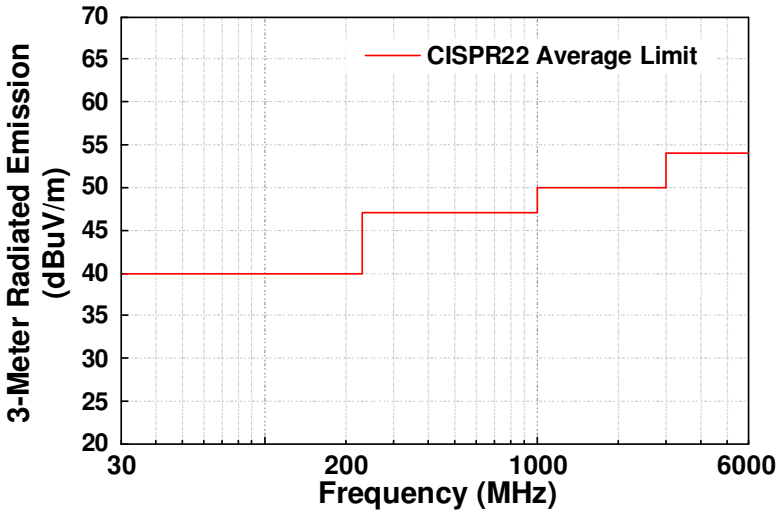


Fig. 1.3 CISPR 22 radiated emission limit line

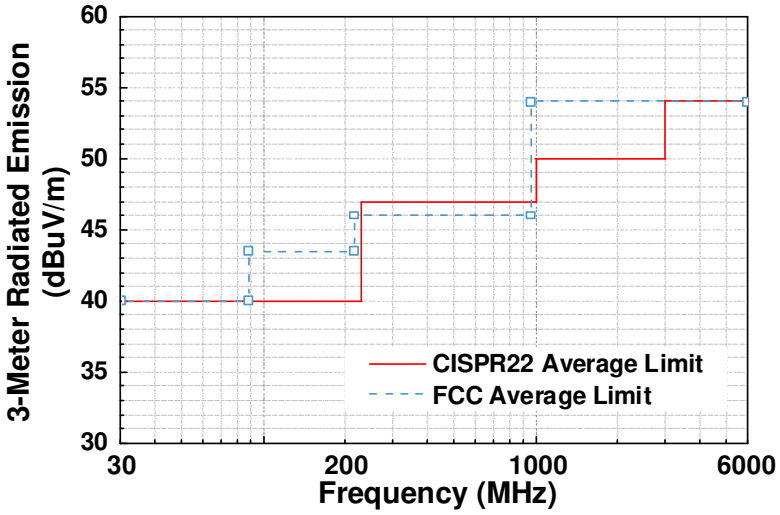


Fig. 1.4 Comparison of FCC and CISPR 22

As mentioned before, basically, every electronic system generates unwanted and unintentional electromagnetic radiations and it needs to fulfill certain EMC regulations to be advertised or sold in particular market, e.g., FCC regulations for US market and CISPR 22 for Europe. Therefore,

for product development, EMC design becomes one of the most critical considerations, and in fact, it is exactly the most complicated and mysterious part, previously known as “black magic”. In order to unveil the EMI inside the data center, we will first start with the architecture of each unit communication module.

To boost the communication speed, engineers intuitively choose the parallel architectures to implement the data link. Intrinsically, increasing the number of channels directly increases the number of symbols sent in parallel per unit period, e.g., two channels doubles the symbol rate. Thus, parallel architectures are widely adopted for the ultra-high-speed interconnections between chip to chip, or the internal buses of each module. Notwithstanding the communication speed, a parallel communication architecture is problematic due to the synchronization, latency, and crosstalk between channels. Contradicting to the superficial instinct about increasing the number of paralleled channels, a high-speed serial communication architecture is a more appealing choice for engineers. These links include chip-to-chip communications on backplanes, computer networks, computer peripheral buses, long-haul communications, etc.. Due to the consideration of cost, serial link requires much fewer data channels than the parallel link, e.g. copper cables, optical fibers, etc., and thus, reducing the number of interconnections saves a lot of expenditures, especially when the communication distance is long enough. Furthermore, the multi-channel design also requires paralleled transceivers (TRX), or at least, the number of paralleled I/O pins, and it will increase the cost of communication integrated circuit (IC), or the package cost of each IC. Additionally, according to [10], the IC package costs more than 25% of the total budget in some advanced electronic systems, which is really a huge amount of money. Finally, yet importantly, the most challenging and critical parts in parallel data link are the clock skew, data skew, and crosstalk. Skew basically describes the difference of arrival time of the data symbols transmitted at the same time. The time for a signal to travel the interconnection channel is

determined by the length and the material of the interconnection, and the group velocity of the signal. When the communication speed is getting higher, e.g., larger than 10 Gbps, even a small amount of skew can cause a serious issue in parallel links. In addition, the capacitive coupling, circuit delay, and process, voltage, temperature (PVT) variation will further deteriorate clock skew and data skew between different channels. When data rate and the number of links increase, crosstalk between adjacent channels also tends to increase. The connectors, vias, and even heat sinks break the continuity of electromagnetic fields and increase the chance of crosstalk [11].

Therefore, high-speed serial communications are replacing parallel communications rapidly. Common high-speed serial data links include backplane links such as PCI Express, Ethernet, USB, HDMI, etc., and particularly in the data center, backplane links are the most fundamental communication units as shown in Fig. 1.5. The backplane link consists of a transmitter (TX), a receiver (RX), and passive the interconnections. The data signal goes from the TX, through the IC package, PCB traces, vias, backplane connectors and finally reaches the RX I/O pin. In the procedure of data communication, unintentional EMI happens.

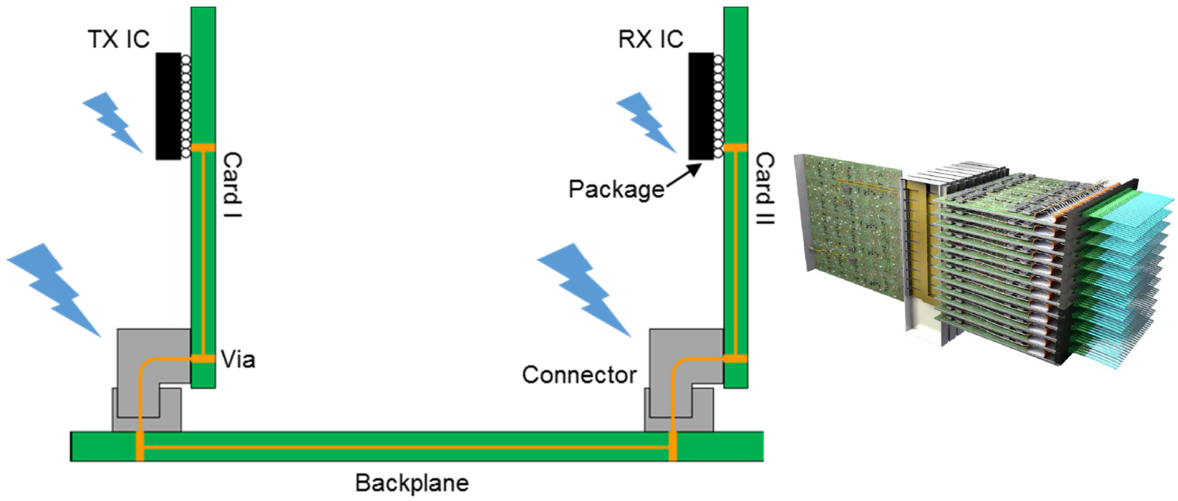


Fig. 1.5 A typical backplane SERDES link [12]

Fig. 1.6 is a practical case study from a joint project of Cisco and Molex, which are the world-leading communication service and infrastructure providers. This research work can give us a

quick glimpse of the EMI behavior of a typical backplane module, but no detailed analysis provided.

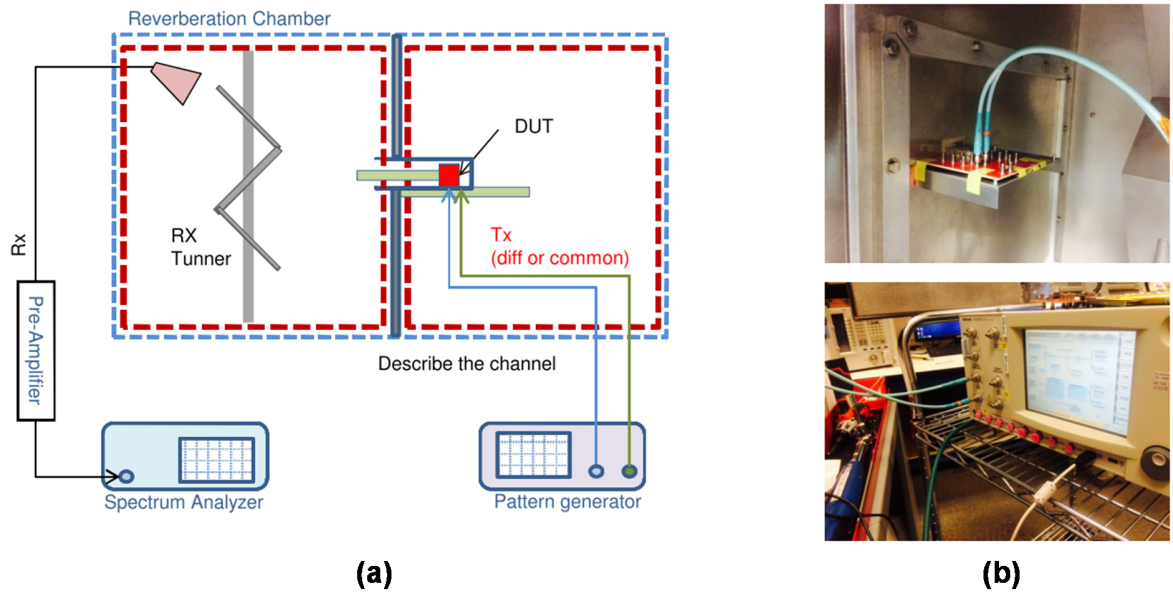


Fig. 1.6 (a) The EMI measurement setup, and (b) photos of the measurement site [13].

The measurement is done in a reverberation chamber, where the backplane module is fixed at the middle of the chamber and several dual-ridge antennas are placed to receive the radiated emissions from 3 GHz to 40 GHz. A pattern generator is placed outside the chamber to generate the differential pseudo-random bit sequence (PRBS) excitations to the backplane module and a spectrum analyzer is used to monitor the received signal spectrum from antennas. In the measurement, the PRBS data rate is 10.3125 Gbps and the corresponding measured signal spectrum of total radiated emission is shown in Fig. 1.7.

Observations are summarized as follows:

The noise floor of the radiated emission is below -80 dBm, except a few points at particular frequencies, which are 10.3 GHz, 20.6 GHz, and 31.9 GHz. The result shows the radiated power of signal backplane module, but when the number of modules increases to be over thousand, like the practical case in a data center, the accumulated radiation at those frequencies will be most

likely to fail the system electromagnetic compatibility. Furthermore, it is noted that the largest EMI noise tone appears at 10.3 GHz.

The well-known spectrum of ideal PRBS contains no energy at the double Nyquist frequency and the harmonics [14]. In this case, for a 10.3 Gbps PRBS, the double Nyquist frequency is exactly 10.3 GHz. Thus, ideally, there should be spectrum nulls, instead of large spikes, at the frequencies of 10.3, 20.6, and 30.9 GHz. However, the practical measured data is contradicting to the superficial instinct. Though there are plenty of FCC regulations, CISPR 22 standards, and even the Generic IC EM emission testing specifications [15], [16], talking about the EMI in general electronic systems, there is no detailed analysis or description about this contradictory phenomena yet.

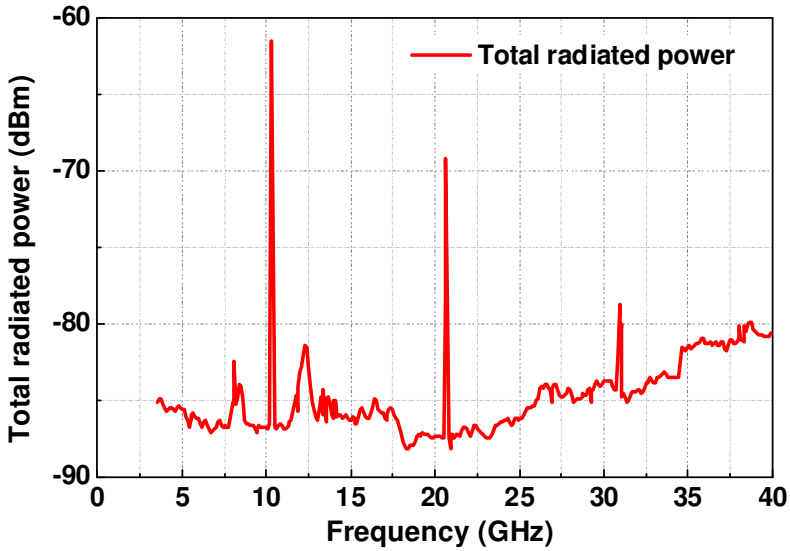


Fig. 1.7 Measured total radiated emission [13].

Based on all the observations above, we have to ask several questions:

Why are the measured EMI peaks located at the double Nyquist frequency and the harmonics?

What is the EMI noise source?

How to simulate the EMI noise?

How to reduce the EMI noise?

Therefore, baring all the uncertainties of the EMI behavior in the backplane link, the dissertation work aims to provide the fundamental analysis and verifications to answer these questions.

1.2 Thesis Organization

This dissertation mainly discusses the EMI-related common mode (CM) noise issue in high-speed differential SERDES links, from circuit-design perspectives.

First, a non-return to zero (NRZ) wireline link is analyzed to unveil the characteristics of the EMI-related CM noise in the high-speed wireline link. The work starts from the behavior-level simplification of the CM noise of the differential NRZ signals and provides the fundamental mathematic analysis for the differential NRZ signals.

Based on the mathematic expression of the CM noise of differential NRZ signals, several noise behaviors are analyzed with simulations and experiments. Chapter 3 talks about the simulation details and the corresponding experiment procedures for differential NRZ signals.

Similar to the NRZ signals, differential 4-level pulse amplitude modulation (PAM-4) signals also suffer from the EMI-related CM noise issue. Thus, Chapter 4 mainly discusses the CM noise in differential PAM-4 signals. A systematic methodology is proposed to describe the CM noise behavior in PAM-4, or even PAM-8/16, signals. In addition to the theoretical analysis, both behavior-level and transistor-level simulations are conducted to further consolidate the proposed methodology.

Chapter 2 Anatomy of EMI Issue in Typical SERDES Links

Differential signaling has been widely used for high-speed SERDES links due to its outstanding noise tolerance and signal integrity. To analyze the EMI issue in typical SERDES links, we need to first find out the exact source of EMI radiation and then the generation mechanism of the EMI source. Fig. 2.1 shows the typical differential non-return-to-zero (NRZ) signals and the related signal characteristics, e.g., skew, rising and falling time, data period and the definition of the common mode (CM) and differential mode (DM) parts. As depicted in Fig. 2.1, the DM spectrum for ideal differential signals has an envelope of the rectified *sinc* function with a sharp notch for every $1/T_b$ frequency, while the CM spectrum only contains a DC component.

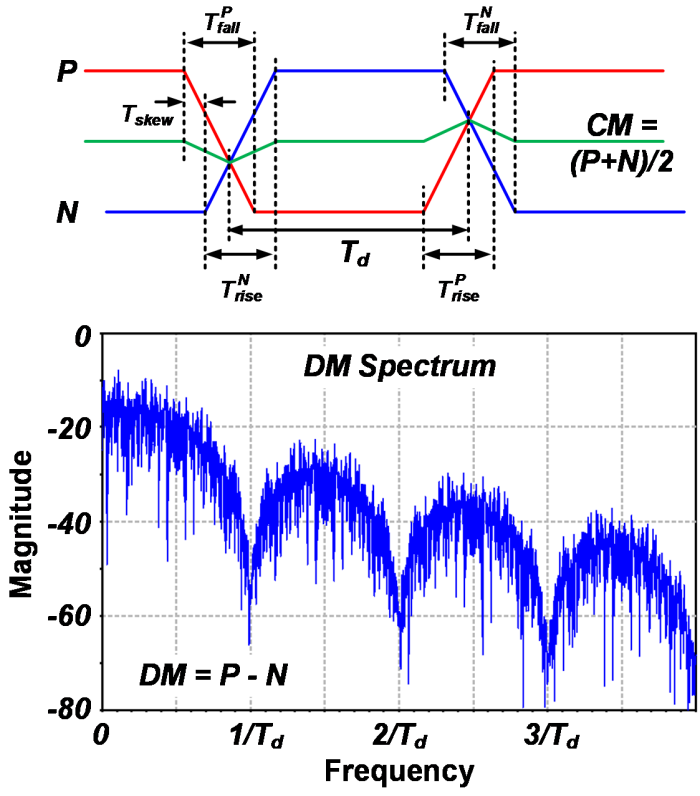


Fig. 2.1 Typical differential data signals and the corresponding spectrum

However, in practical cases, a certain signal distortion introduces unwanted noise at the double Nyquist frequency and the subsequent harmonics, which are n/T_d frequencies in Fig. 2.1. In the following section, a simplified model for typical SERDES links is presented and several simulations are conducted with the model to locate the EMI radiation source, explain the radiation mechanism, and comprehensively analyze the EMI issue.

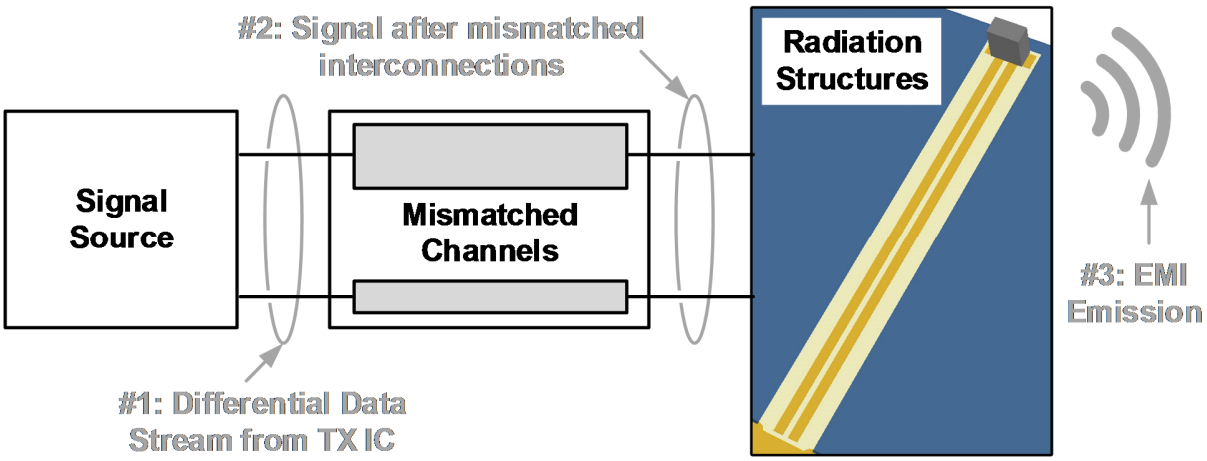


Fig. 2.2 Simplified backplane link for behavior-level simulations.

2.1 EMI Radiation in Differential Data Links

In order to radiate and generate EMI, the SERDES link has to have an EMI source and a radiation structure, e.g. PCB trace, via and connector. A typical SERDES link can be simplified and divided into three major parts, as shown in Fig. 2.2, for behavior-level simulation and analysis. The simplified SERDES link consists of a signal source, which is typically the SERDES transmitter (TX), interconnection data channels, and a radiation structure for the EMI noise to radiate. Since the receiver in a typical SERDES link passively receives the signal and generates no active signals, it can be modeled to a termination resistor (differential 100-Ω) as part of the data interconnection.

The signal source in Fig. 2.2 is a Verilog-A-based differential pseudo-random bit stream (PRBS) generator and it generates 10 Gbps of differential data with a data pattern length of 2^7-1. The subsequent data interconnection model is a pair of differential PCB traces. The differential PCB traces are intentionally mismatched to analyze the effects of channel mismatch on EMI. In the end, a simplified pair of unshielded differential PCB traces with a 100-Ω far-end termination resistor are added to provide the radiation structure for EMI emissions.

In the simplified link, three observation points are set, as shown in Fig. 2.2, which are the output of the signal source (point 1), the output of the data channels (point 2) and the emission 1 meter away from the radiation structure. Point 3 is to observe the maximum electric field strength in the surrounding space at a given distance of 1 meter away from the radiation structure.

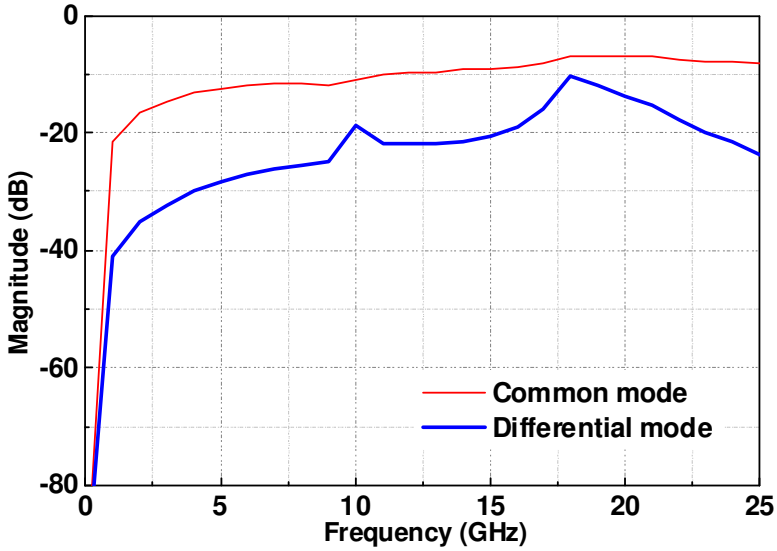


Fig. 2.3 CM radiation efficiency vs. DM radiation efficiency [17]

Fig. 2.3 shows the measured radiation efficiency, which equals the radiated power over the total input power, for a typical backplane connector. In the figure, CM radiation has much higher efficiency than DM radiation. Thus, in the following sections, differential signals are taken into analysis with separated CM and DM signal components.

2.2 EMI Related Common-Mode Noise

As the signal source for the entire SERDES link, the TX output signal affects the link EMI performance intrinsically. The ideal differential data stream from the TX has fully symmetrical positive and negative signals and thus, the CM signal component, which is the sum of the positive and negative signals, has only a constant DC component. However, signal distortions caused by impedance inconsistency, reflection, fabrication variation, etc., are inevitable in a practical TX. In addition to generating 2^7-1 PRBS, the Verilog-A-based signal generator in Fig. 2.2 also has built-in functions to generate different types of distorted differential data signals. The signal distortions are classified into linear and non-linear distortions according to the conclusions in [18]–[21].

2.2.I Linear Distortions in Differential Signals

In Fig. 2.4 to Fig. 2.7, the differential channels are named the positive (P) channel and negative (N) channel separately for the following analysis. In Fig. 2.4, the amplitude of P is 20% smaller than the amplitude of N and the amplitude mismatch generates the non-ideal CM signal transient waveform as shown. In this case, when the data is “1” (a high potential in the P channel and a low potential in the N channel), the CM signal goes down, while when the data is “0” (a low potential in the P channel and a high potential in the N channel) the CM signal goes up. The observation above indicates that the CM signal follows the data pattern; in other words, it is data-dependent. Due to the data-dependency of the CM signal, the corresponding CM spectrum is similar to the DM spectrum, which has a similar PRBS spectrum envelope, as shown at the right side of Fig. 2.4.

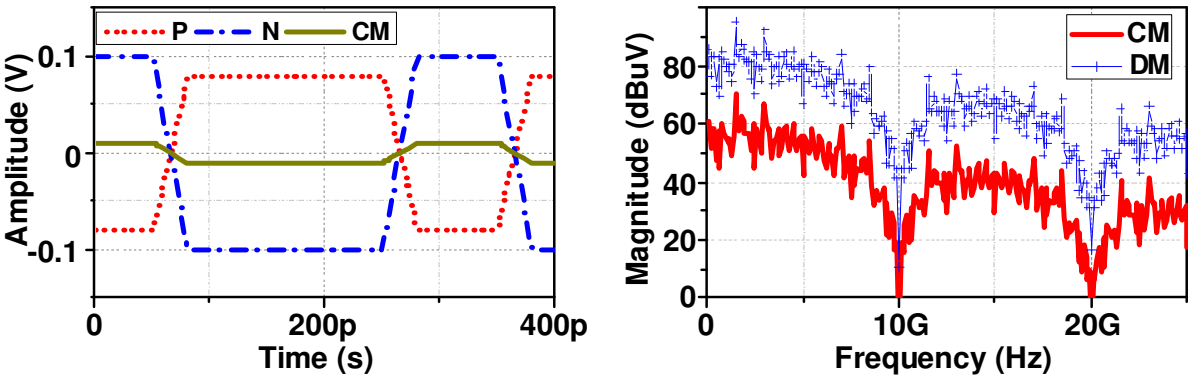


Fig. 2.4 Transient waveforms and corresponding spectrums of differential data with amplitude mismatch

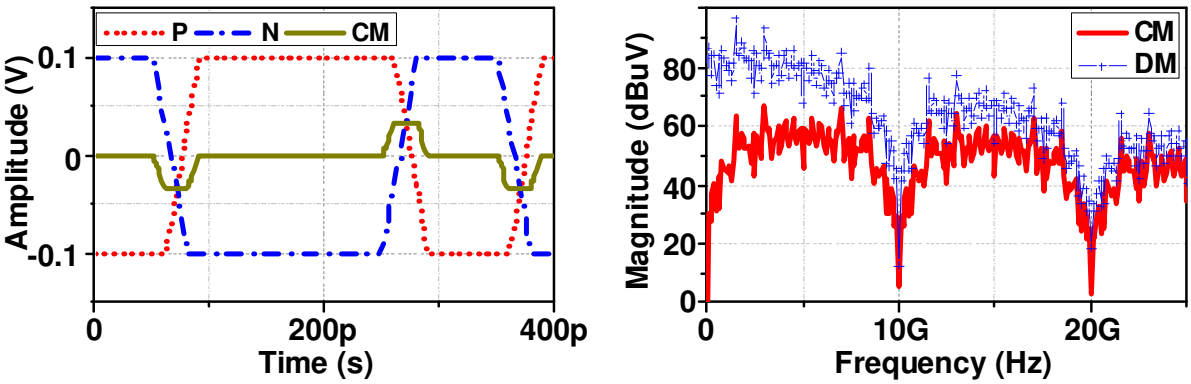


Fig. 2.5 Transient waveforms and corresponding spectrums of differential data with channel skew

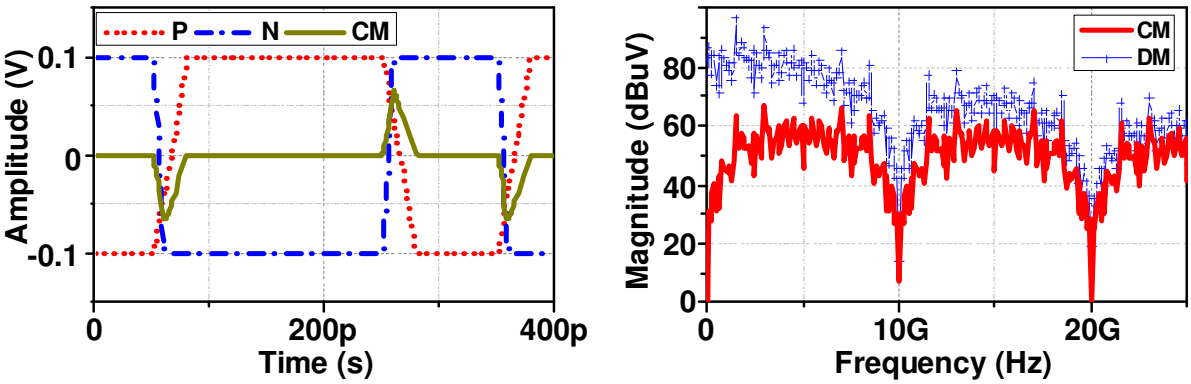


Fig. 2.6 Transient waveforms and corresponding spectrums of differential data with bandwidth/slew rate mismatch

In Fig. 2.5, where the channel skew exists, the P channel signal is 10 ps lagging behind the N channel signal. Then, in Fig. 2.6, the slew rate mismatch introduced by the channel bandwidth mismatch is simulated. In the P channel, the rising and falling edges for full signal swing are 10-

ps, while the rising and falling edges, for the full swing of the N channel signal, are 25 ps respectively. The simulation settings for Fig. 2.4, Fig. 2.5 and Fig. 2.6 are described in (2.1), (2.2) and (2.3), respectively.

$$Amp_{P} = 0.8\,Amp_{N} \tag{2.1}$$

$$T_{skew} = 10\ ps \tag{2.2}$$

$$T_{rise}^{P} = T_{fall}^{P} = 25\ ps > T_{rise}^{N} = T_{fall}^{N} = 10\ ps\ . \tag{2.3}$$

Applying the spectrum analysis to both the channel skew and the slew rate mismatch, similar conclusions are observed. In the three cases of Fig. 2.4, Fig. 2.5 and Fig. 2.6, the CM signals are data-dependent and the corresponding CM spectrums are similar to the DM spectrums with a rectified *sinc* spectrum envelope. These distortions with similar characteristics are categorized as "linear distortions" [19].

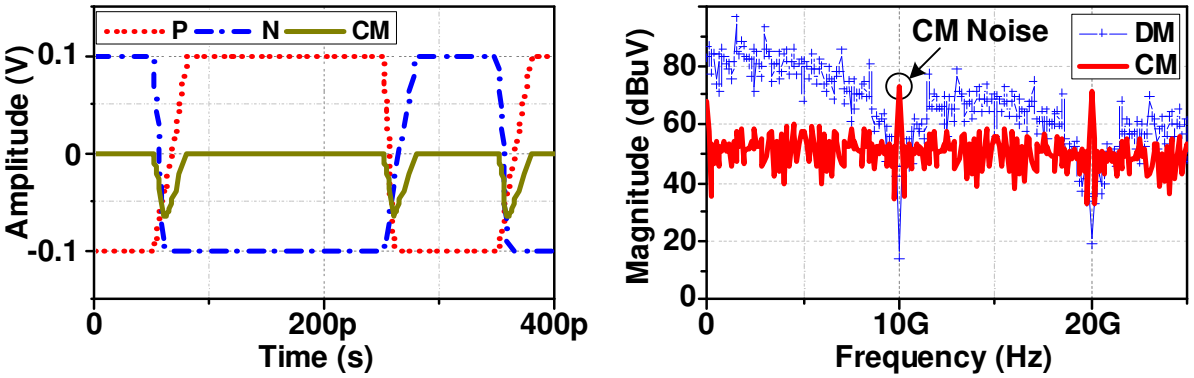


Fig. 2.7 Transient waveforms and corresponding spectrums of differential data with rising/falling edge mismatch

2.2.II Non-linear Distortion in Differential Signals

However, the case in Fig. 2.7 is different from all three distortions analyzed above, where the signal rising edge time is always longer than the falling edge time during the data transition periods. Unlike the slew rate mismatch in Fig. 2.6, where the mismatch exists between the P and N channels,

the rising and falling edge mismatch exists internally in both the P and N channels, as described in (2.9):

$$T_{rise}^{P} = T_{rise}^{N} = 25\ ps > T_{fall}^{P} = T_{fall}^{N} = 10\ ps\ . \tag{2.4}$$

As depicted in the transient waveforms in Fig. 2.7, the voltage spikes on the transient CM waveform are identically going down towards the low potential, which indicates the data-independency feature of the CM noise in this particular case. According to the simulated frequency domain spectrums, the DM spectrum has a typical rectified *sinc* envelope but the CM spectrum only shows large power tone at every data frequency and the corresponding harmonics. The frequency of $1/T_b$ is also known as the double Nyquist frequency ($2F_{Nyquist}$) in wireline communication, e.g., $F_{Nyquist}$ is 5 GHz for a 10 Gbps NRZ data link. Instead of generating a broadly dispersed CM spectrum like the cases in Fig. 2.4, Fig. 2.5 and Fig. 2.6, the distortion in Fig. 2.7 behaves so differently and creates a large CM power tone at $2F_{Nyquist}$; therefore, it is categorized as "non-linear distortion" [19].

Referring to the analysis above, **only the non-linear distortion introduces the signal tone at $2F_{Nyquist}$**, and it can be associated with the previous case from MOLEX in [13]. In the following sections, we specify the discussed CM noise to be the non-linear distortion introduced signal tone at $2F_{Nyquist}$, and analysis of the generation mechanism and behavior of the non-linear distortion will be conducted.

2.2.III Locating the CM Noise Source

To tackle the EMI issue in typical SERDES links, the noise source needs to be identified and located first. For the following analysis, a simulation setup is built referring to Fig. 2.2, where the Verilog-A-based TX generates a 20 Gbps PRBS and the subsequent interconnection channels are

modeled by several blocks based on measured S-parameters of different PCB traces (3 cm and 4 cm PCB traces with a grounded coplanar waveguide structure).

The simulation setup in Fig. 2.8 has an ideal signal source (ISS) with a 50-Ω output impedance to generate ideal differential PRBS signals. The subsequent data channels are non-ideal and intentionally mismatched with the P channel going through a 4 cm PCB trace, and the N channel going through a 3 cm PCB trace. We name it as 'ISS-non-ideal channels (NICH)'. Fig. 2.8 shows the simulated transient waveforms and spectrums, at the position of point 2 in Fig. 2.2.

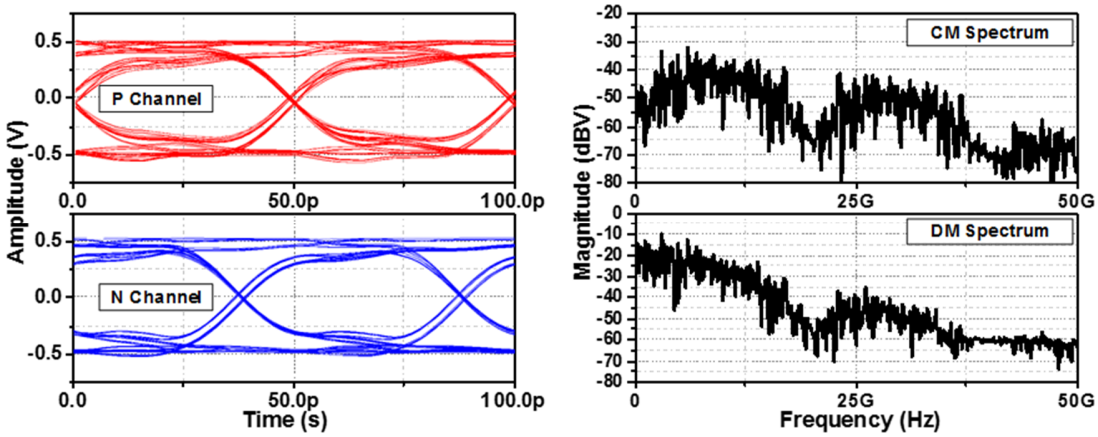


Fig. 2.8 Waveforms and corresponding spectrums of simulated results of "ISS and NICH"

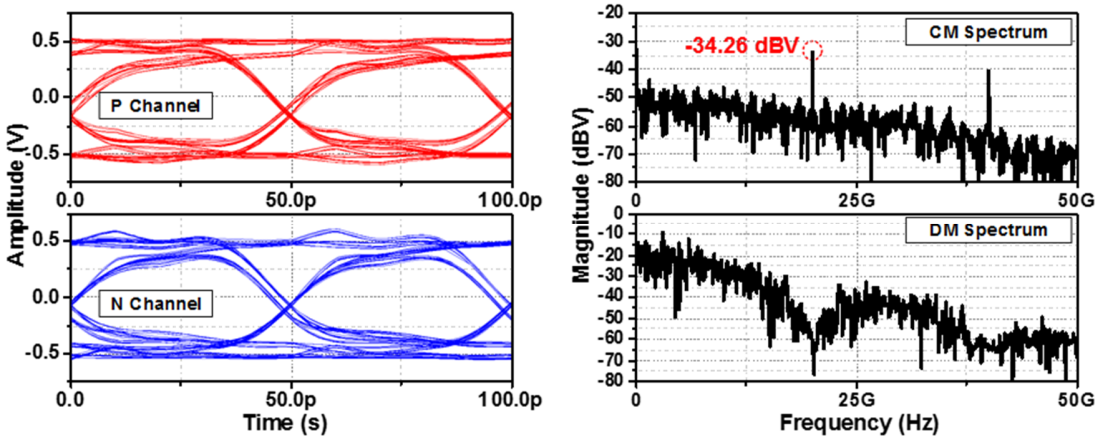


Fig. 2.9 Waveforms and corresponding spectrums of simulated results of "NISS and ICH"

The simulation setup in Fig. 2.9 has a non-ideal signal source (NISS) with a 50-Ω output impedance to generate differential PRBS signals with non-linear distortions. The subsequent data

channels are fully matched with the P and N channels both go through a 4 cm PCB trace. We name this setup as 'NISS-ideal channels (ICH)'. Fig. 2.9 shows the corresponding simulated transient waveforms and spectrums.

Similarly, the simulation setup in Fig. 2.10 has a non-ideal signal source (NISS) and the mismatched data channels with the P channel goes through a 4 cm PCB trace and the N channel goes through a 3 cm PCB trace. This setup is named 'NISS-NICH' and the corresponding simulation results are shown in Fig. 2.10.

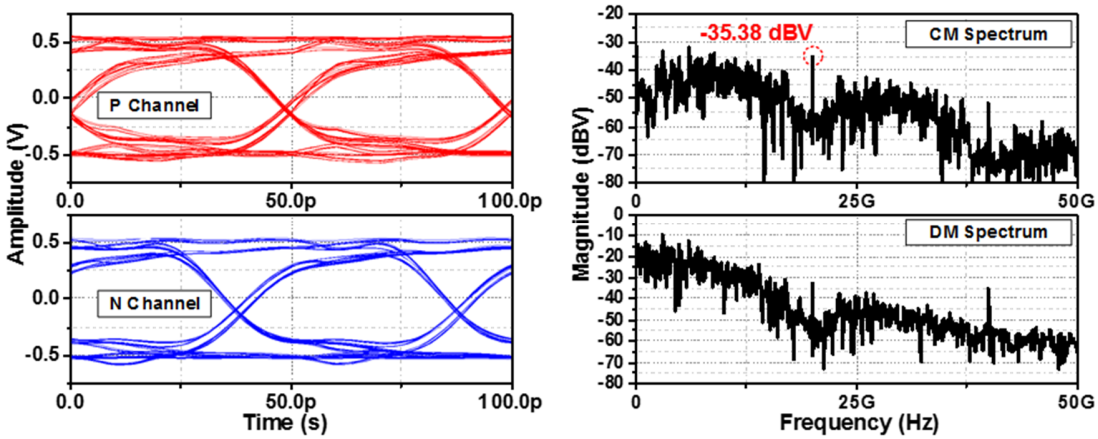


Fig. 2.10 Waveforms and corresponding spectrums of the simulated results of "NISS-NICH"

Comparing the simulated CM spectrums in these three setups, the CM noise tone at $2F_{Nyquist}$ only appears in the 'NISS-ICH' and 'NISS-NICH' cases, which indicates that **the CM noise is intrinsically generated from the non-ideal single source and the mismatched interconnection channels cannot generate the CM noise**.

Comparing the simulated CM spectrums in Fig. 2.9 and Fig. 2.10, the CM noise tones at $2F_{Nyquist}$ are slightly different, with about a 1 dB gap. However, the DM spectrums of these two cases are completely different at $2F_{Nyquist}$, where the 'NISS-ICH' case has only a spectrum notch at $2F_{Nyquist}$ but the 'NISS-NICH' case has a noise tone at the same frequency. The comparison above shows the migration from the CM signal to the DM signal, which is discussed in the following section.

2.3 Mode Conversion in Mismatched Differential Channels

The distorted signals from the signal source go through the data channels first. However, in practical engineering cases, differential signal channels cannot be fully matched. Thus, a pair of mismatched PCB traces is used for the simulation, as shown in Fig. 2.11.

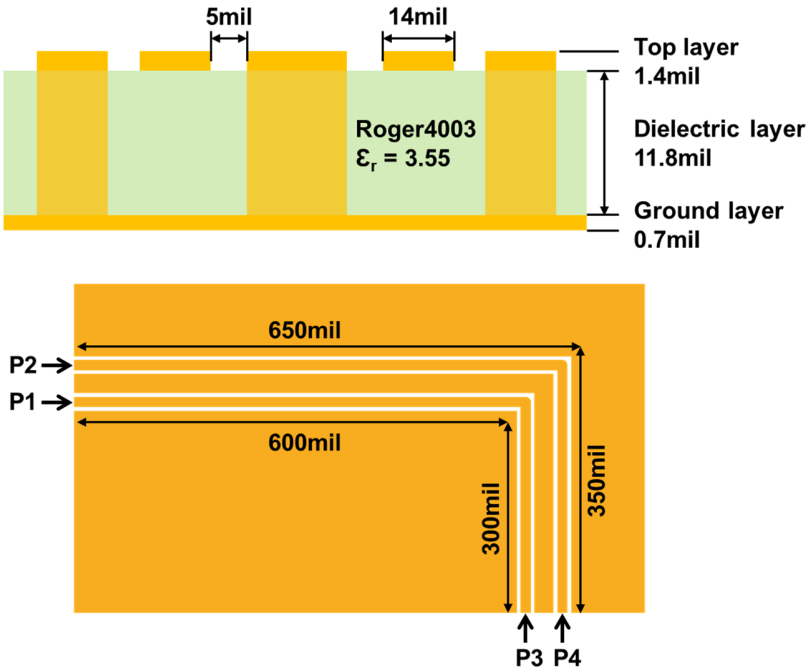


Fig. 2.11 Intersection and top views of the mismatched data channels

The PCB traces have basically grounded coplanar waveguide structure and lie on a Roger4003 dielectric layer of 11.8 mil thickness and a dielectric constant of 3.55. The trace width and the distance gap between the adjacent ground are carefully designed as 14 mil and 5 mil, respectively, to have a 50-Ω characteristic impedance. One of the traces has a 1000 mil length and the other one has a 900 mil length, which creates the 10% channel mismatch. It is to be noted that the 10% mismatch is actually over-exaggerated to magnify and demonstrate the channel mismatch effects in this case.

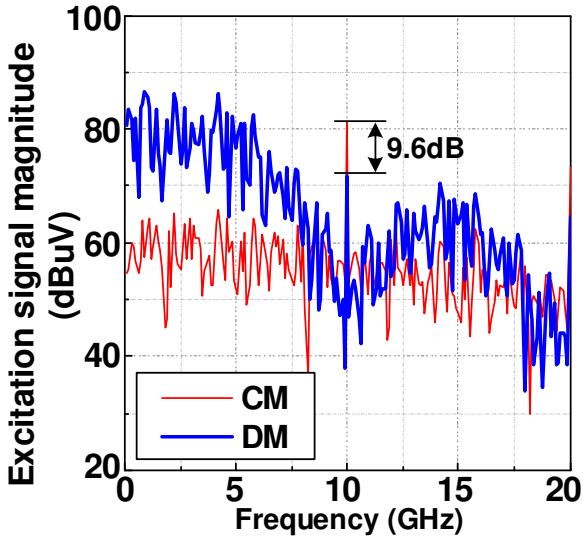


Fig. 2.12 Spectrums of the data after the mismatched data channels

Wes use the High-Frequency Structure Simulator (HFSS) to characterize and generate the 4-port s-parameter (s4p) file of the mismatched PCB traces, and we plug the s4p block into the simulation setup in Fig. 2.2. Then the differential signals with non-linear distortion, as described in Fig. 2.7, are fed to the input ports of the 4-port block, and the differential data streams at the output ports are observed. Fig. 2.12 shows the CM and DM spectrums of the output differential signals after the mismatched PCB channels. Comparing the spectrums in Fig. 2.12 to the source signal spectrums in Fig. 2.7, a large power tone at $2F_{Nyquist}$ exists not only in the CM spectrum but also in the DM spectrum, which indicates the mode conversion between CM and DM during data propagation through the mismatched channels [22]–[24].

From the observations, we conclude that **the TX initially provides CM noise as the signal source, and the mismatched data channels provide mode conversion between the CM and DM, which makes the $2F_{Nyquist}$ power tone appear in both the signal CM and DM components.**

2.4 Crosstalk and CM Noise

In practical applications, paralleled I/Os are widely used in high-speed communication systems. When paralleled data signals simultaneously pass through the paralleled channels, crosstalk inevitably happens. In addition to evaluating CM noise, crosstalk is also discussed in this section.

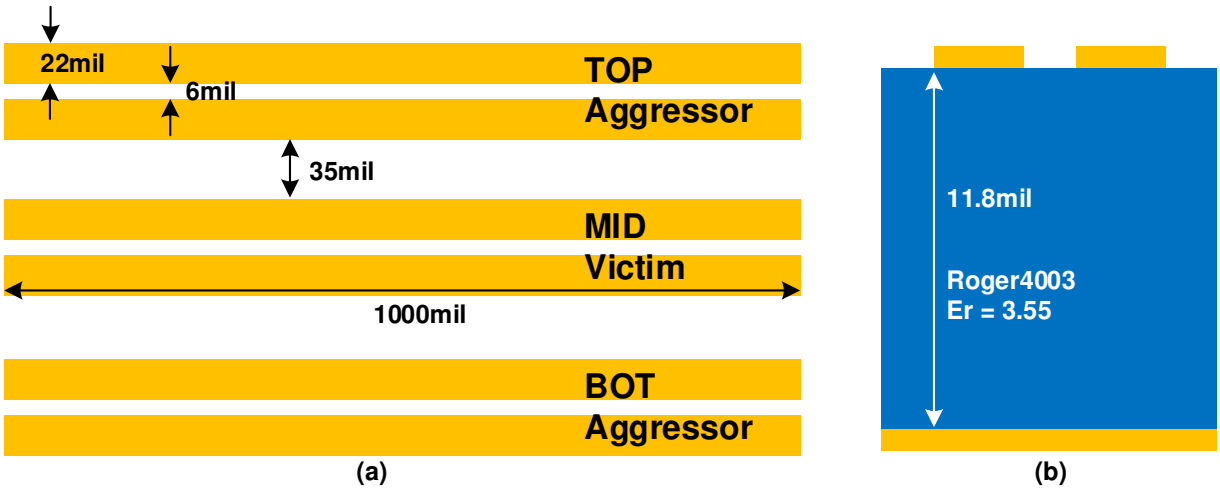


Fig. 2.13 Parallel PCB traces. (a) Top-view; (b) cross-section view.

In order to mimic the crosstalk between adjacent channels, three pairs of differential PCB traces are used in the simulation-based evaluation, as depicted in Fig. 2.13. Top and bottom traces are used as aggressors and the middle traces are the victims. The whole structure is built on a dielectric layer with Roger4003 material and other copper metal layers. The physical dimensions and the simulated characteristics of these PCB traces are shown in Fig. 2.14.

In the simulation, differential data signals are generated by a Verilog-A-based generator and the signals go through PCB traces from the left side to the right side. The generated 10Gbps NRZ signals have a rise and fall time mismatch (20ps and 12ps for rise and fall time respectively) to intentionally add the CM noise in the signals. A 100-Ohm resistor is placed at the right side of each PCB trace pair as a differential termination.

When the top and bottom aggressors are disabled (no signals inside the top and bottom traces) and only the NRZ signals in middle victim traces are enabled, the corresponding simulation results are shown in Fig. 2.15 and Fig. 2.16. When the NRZ data signals in all three pairs of differential traces are enabled, the corresponding simulated results are shown in Fig. 2.17 and Fig. 2.18.

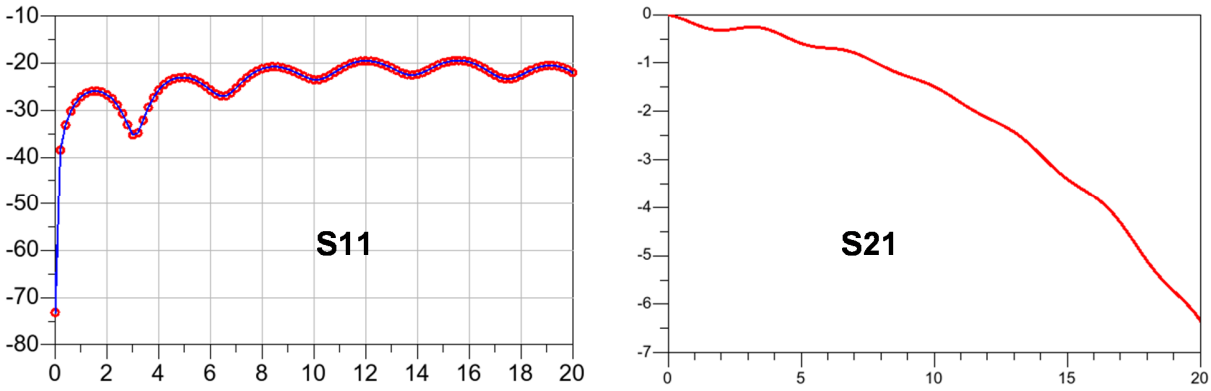


Fig. 2.14 Simulated characteristics of differential PCB traces.

In Fig. 2.15, due to the coupling between adjacent channels, the disturbances in the top and bottom signals are generated during the switching period of the middle channels signals.

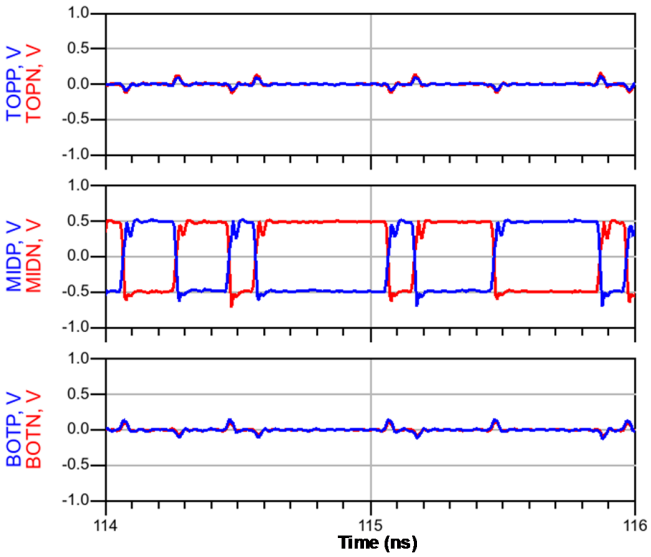


Fig. 2.15 Transient NRZ waveforms without aggressor.

When separate the middle channels signals in DM and CM components, the corresponding DM and Cm transient waveforms and the spectrums are plotted in Fig. 2.16. Due the rise and fall time

mismatch, the CM noise is generated during each switching period and the CM noise tone can be found in the CM spectrums.

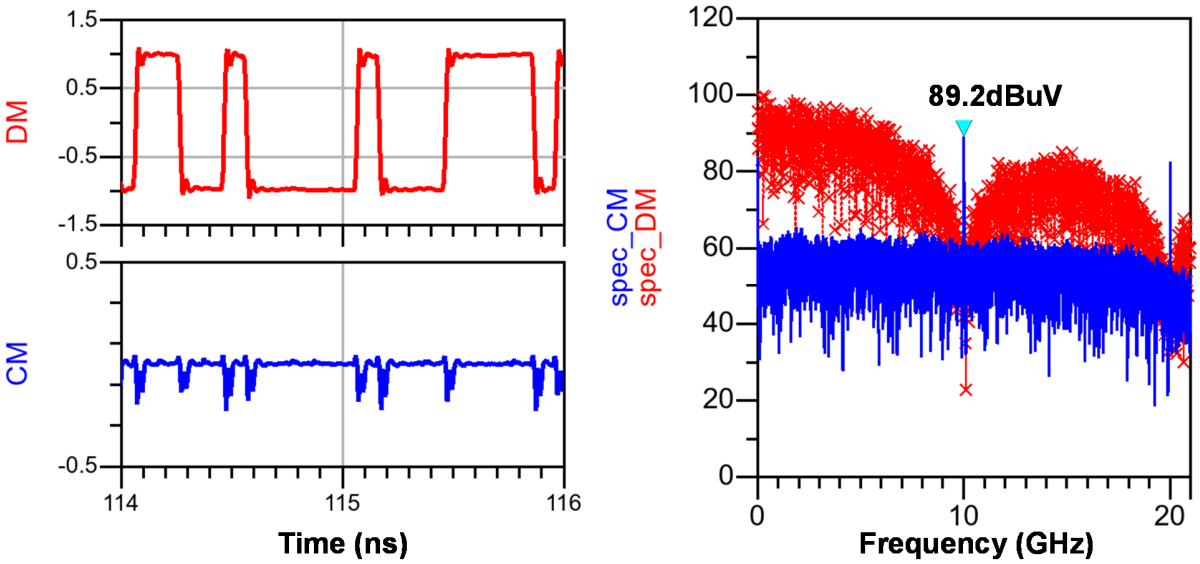


Fig. 2.16 Transient NRZ waveforms of DM and CM signals without aggressor and the corresponding spectrums.

Similarly, when all the signals in three channels are enabled, the simulation results with relatively significant crosstalk are shown in Fig. 2.17. And the transient waveforms of the DM and CM signals in the middle victim channel are shown in Fig. 2.18.

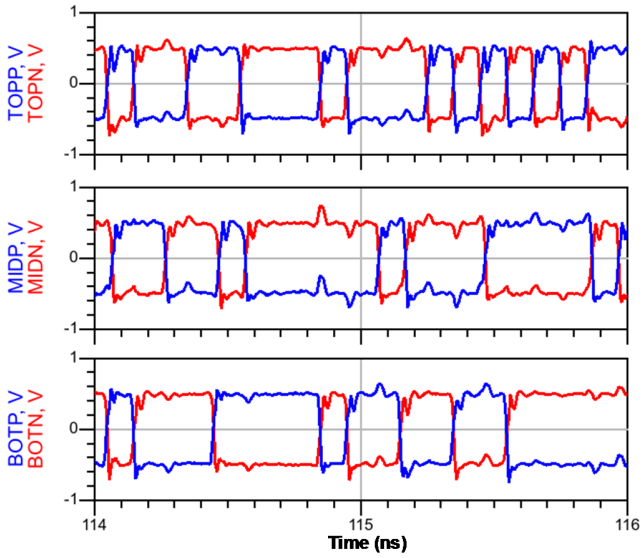


Fig. 2.17 Transient NRZ waveforms with top and bottom aggressors.

By comparing the simulated results in the case without crosstalk and the case with crosstalk, several observations are found as below.

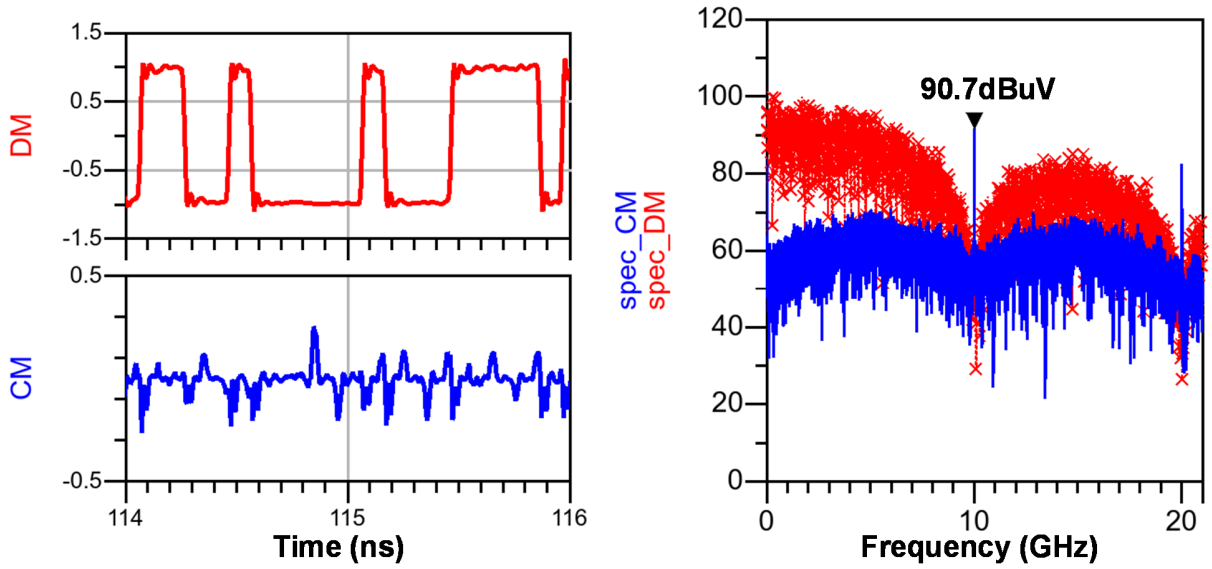


Fig. 2.18 Transient NRZ waveforms of DM and CM signals with aggressors and the corresponding spectrums.

From the comparison between Fig. 2.15 and Fig. 2.17, crosstalk deteriorates the signal quality. However, due to the intrinsic immunity of differential signaling, the DM signals in both cases (Fig. 2.16 and Fig. 2.18) are almost similar. Because the CM noise from adjacent channels is coupled to the victim channel, the final CM noise at 10GHz is slightly enlarged when the aggressor channels are enabled.

Similar analysis is conducted with PAM-4 signaling. Fig. 2.19 shows the simulated PAM-4 victim signals in the case without aggressor signal and the case with aggressor signals.

Similar to the results in previous analysis on NRZ signals, the signal integrity deteriorates due to the crosstalk. However, because of the intrinsic characteristics of differential signaling, the DM signals in both cases (with/without aggressor signals) are almost the same.

Because the CM noise coupled from adjacent aggressor signals are added to the CM noise of the victim signal, the CM noise at 10GHz is slightly enlarged when the aggressors are enabled. This observation is consistent to the situation in NRZ signaling.

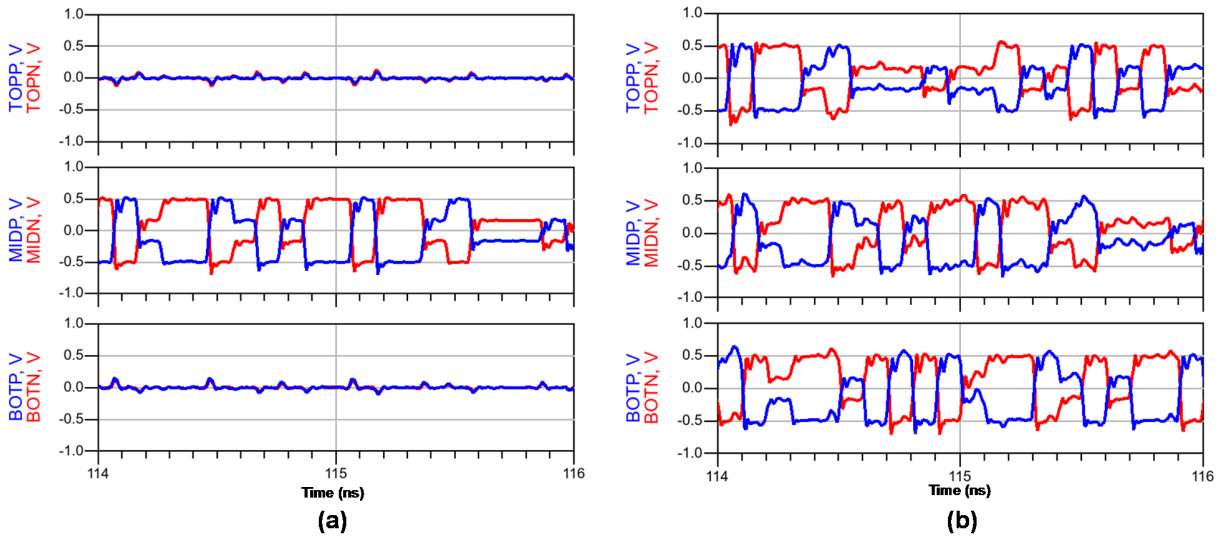


Fig. 2.19 Transient PAM-4 waveforms. (a) Without aggressor and (b) with top and bottom aggressors.

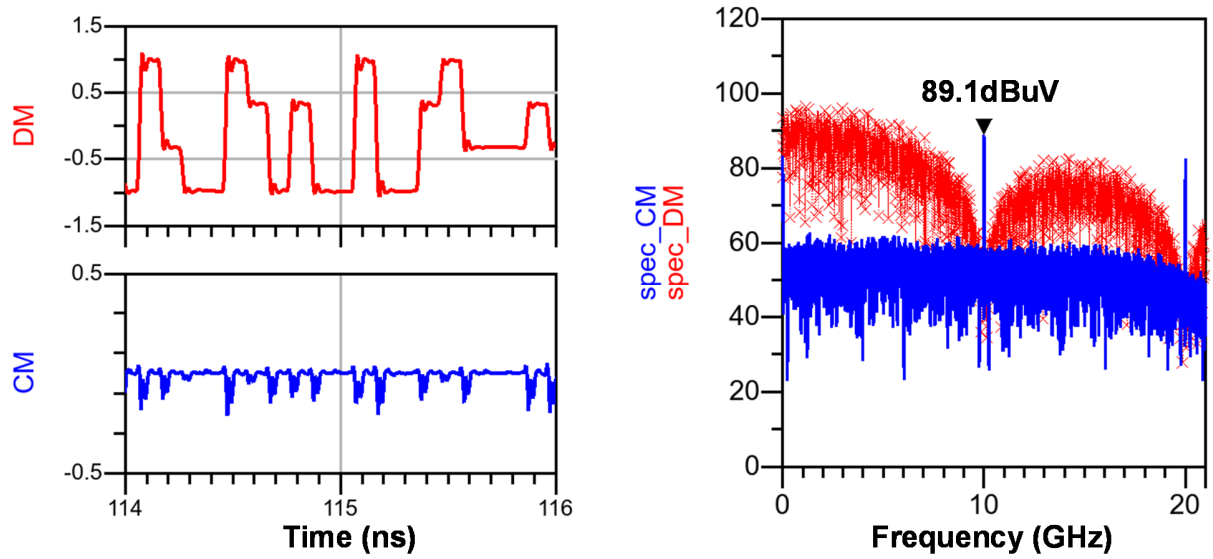


Fig. 2.20 16 Transient PAM-4 waveforms of DM and CM signals without aggressor and corresponding spectrums.

In summary, crosstalk does affect the signal integrity, especially in single-ended mode. However, due to the advantage of differential signaling, the CM noise coupled from adjacent

channels barely affects the communication quality (DM signals) but the coupled CM noise from adjacent channels slightly enlarges the final CM noise level of the victim signal.

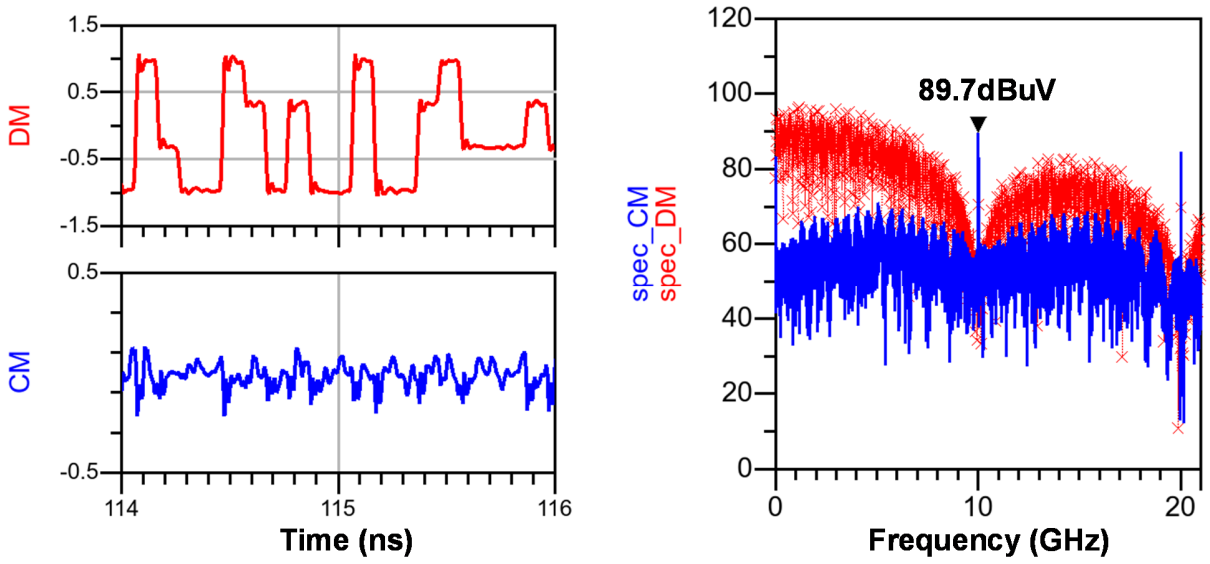


Fig. 2.21 16 Transient PAM-4 waveforms of DM and CM signals without aggressor and corresponding spectrums.

2.5 Radiation of CM Noise

In a typical backplane SERDES link, the CM and DM signals of the differential data streams radiate through certain antenna structures, such as PCB traces, vias, connectors or integrated circuit (IC) packages. In the simplified SERDES link setup in Fig. 2.2, a pair of 2-cm differential PCB traces with a 100-Ω termination resistor is used as the antenna structure, as shown in Fig. 2.22, for EMI radiation simulation.

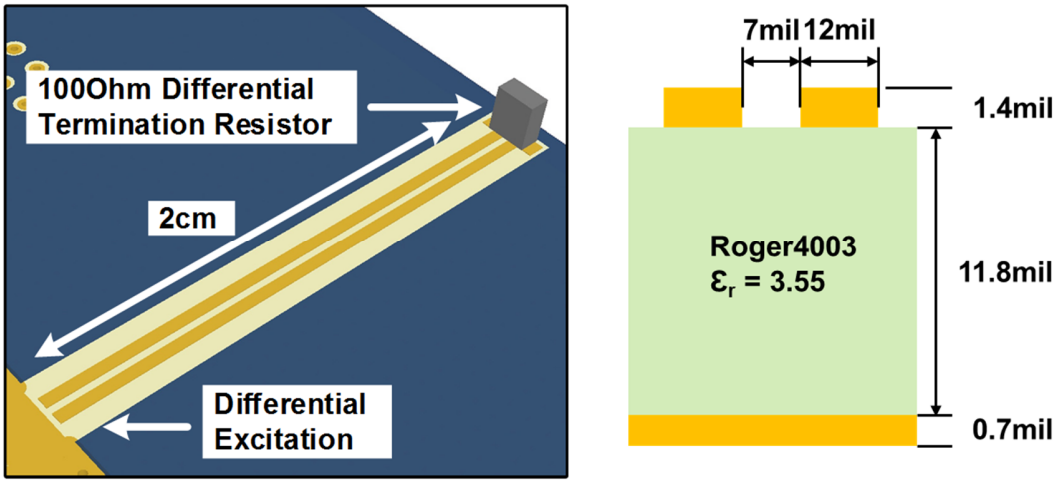


Fig. 2.22 Layout of the differential PCB microstrip traces with a 100-Ω rumination resistor

The layer information is basically same as the case in Fig. 2.11 and the differential PCB traces are based on the microstrip structure, and the trace width and gap are designed to be 12 mil and 7-mil, respectively, to have the characteristic impedance of 50-Ω. The end 100-Ω resistor represents the input impedance of the receiver (RX).

HFSS is also used for the EMI emission simulation. The input excitation is a differential high-frequency sinusoidal signal with a constant 1-V amplitude. The 1-V excitation signal is fed to the PCB input in the common mode or differential mode separately. The simulated maximum CM and DM emission in the surrounding space, at a given distance of 1 meter away from the PCB, are plotted in Fig. 2.23. When the excitation signals are in the differential mode, the electromagnetic fields, generated by the current flows inside the differential PCB traces, are strongly coupled to each other and barely radiate. However, the case of CM excitation exhibits much higher radiation power than the case with DM excitation, e.g. 29.4 dB higher at 10 GHz. In addition, similar simulation results on high-speed backplane connectors also indicate the large difference between CM and DM radiation in [13], [17], [25]. Thus, for the emission of passive components in typical backplane SERDES links, the CM radiation is typically more significant than the DM radiation[26].

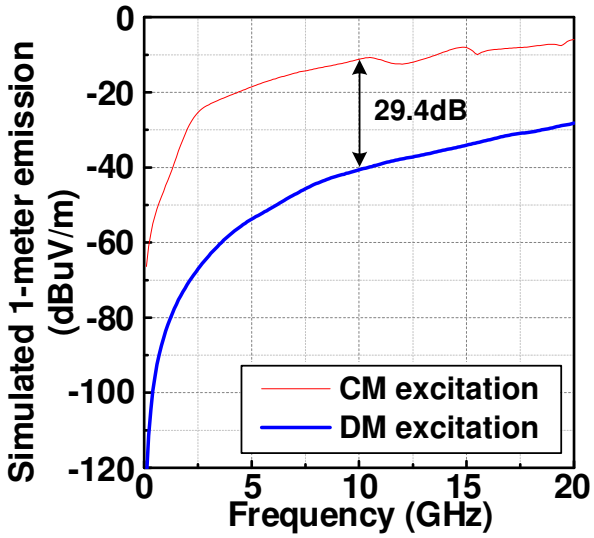


Fig. 2.23 Simulated 1-meter CM and DM radiations of the differential PCB microstrip traces

Because the input excitation has a constant 1-V amplitude, the emission simulation result in Fig. 2.23 is actually the normalized maximum electric field in the surrounding space at 1-meter distance away from the radiation structure. In Fig. 2.2, the signal after mismatched data channels at point-2 goes directly into the cascaded PCB radiation structures. Thus, by exciting the unshielded PCB traces with the signals after the data channels in Fig. 2.12, the final radiated CM and DM electric fields at point-3 in Fig. 2.2 are calculated by multiplying the CM and DM spectrums in Fig. 2.12 and Fig. 2.23, respectively, as shown in Fig. 2.24. Due to the huge difference between CM and DM radiations of the PCB trace in Fig. 2.22 and the intrinsic difference in the excitation signals in Fig. 2.12, the final calculated difference between the final CM and DM emission becomes even larger at $2F_{Nyquist}$. The DM emission at $2F_{Nyquist}$, which is sourced from the mode conversion by mismatched data channels at point-2, is 39 dB lower than the CM emission, which is mainly generated from the distorted signal source (point-1).

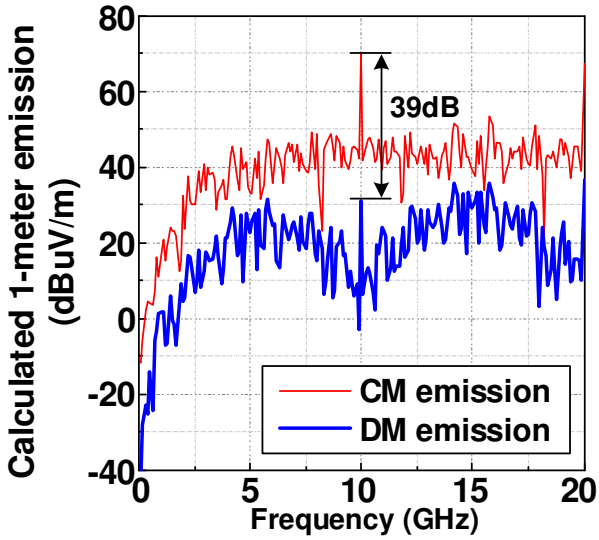


Fig. 2.24 Calculated 1-meter radiation with the differential PRBS excitation

Observations are summarized and we note that the CM noise at $2F_{Nyquist}$ in the SERDES link dominates the EMI emission, which is also most likely to fail the system EMC, while the DM emission at $2F_{Nyquist}$ generated by mode conversion is relatively ignorable. Given this analysis, **the key solution for the EMI issue in the high-speed SERDES link is to control the CM noise at $2F_{Nyquist}$, or, in other words, to control the non-linear distortion** (Fig. 2.7) **in the signal source.**

2.6 Mathematical Expression of CM Noise

The transient waveforms of the non-linear distortion can be quantitatively described in Fig. 2.25. T_d is the period for one bit of data, t_{rise} and t_{fall} are the rising and falling edge time, and T_{tr} is the data transition time, which is defined as the maximum value between rising and falling edge periods, $max(t_{rise}, t_{fall})$. *Amp* is the signal swing of the differential signals. To obtain the CM noise at $2F_{Nyquist}$, the Fourier transform of the CM signal needs to be calculated first. However, the CM noise is randomly generated by the random data sequences, and the Fourier transform cannot be

directly applied on the random signals. Thus, we will estimate the CM signal spectrum by the autocorrelation function and the corresponding power spectral density [27].

During each data transition, there is a spike on the CM signal and it can be modeled as a triangle shape with height A and transition width of T_{tr}. Assuming the rising and falling edges are linear, the height A of each CM spike is calculated as shown in (2.5).

$$A = \frac{\left|t_{rise} - t_{fall}\right|}{T_{tr}} \cdot \frac{Amp}{2} = \frac{Amp}{2} \cdot \frac{\left|t_{rise} - t_{fall}\right|}{\max(t_{rise}, t_{fall})} \tag{2.5}$$

The amplitude of the CM spike is determined by the data transition time (T_{tr}) and the mismatch between the rising and falling edges.

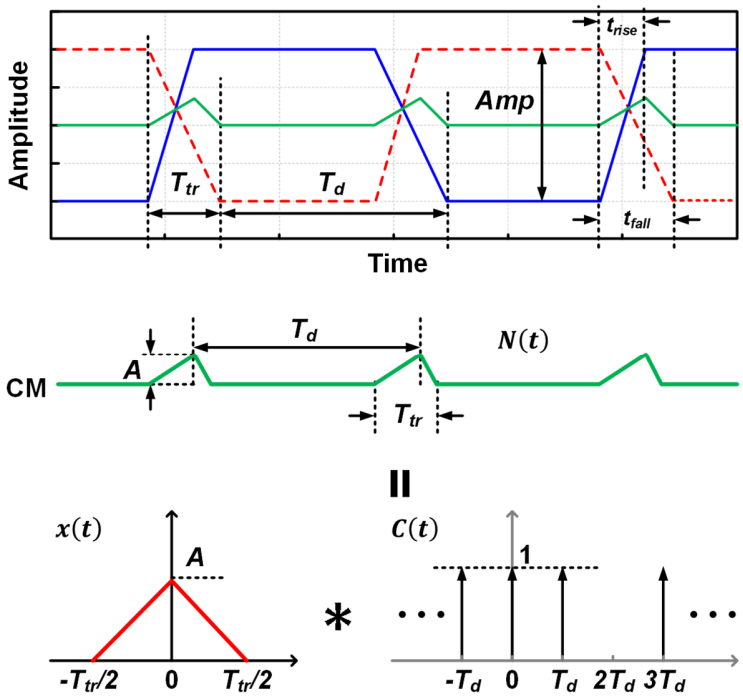


Fig. 2.25 Simplification and calculation of CM noise

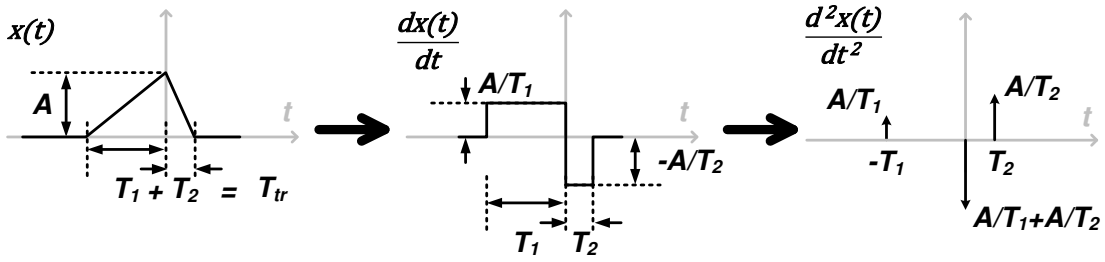


Fig. 2.26 Calculation of single voltage spike, *x(t)*. [18]

According to Fig. 2.26, the Fourier transform of *x(t)* is calculated as

$$\begin{aligned} F(x(t)) &= \frac{1}{-\omega^2} \cdot F[\frac{d^2x(t)}{dt^2}] \\ &= -j\frac{A}{\omega} e^{\frac{1}{2}j\omega T_1} \sin c(\frac{1}{2}\omega T_1) + j\frac{A}{\omega} e^{-\frac{1}{2}j\omega T_2} \sin c(\frac{1}{2}\omega T_2) \end{aligned} \quad . \tag{2.6}$$

When T1 and T2 are equal, each single spike, *x(t)*, with an irregular triangle shape, is further simplified to the shape of an isosceles triangle with height *A* and the bottom width of T_{tr}, as the *x(t)*, shown in Fig. 2.25 and (2.7).

$$x(t) = \begin{cases} -\frac{2}{T_{tr}} A \cdot |t| + A, & -\frac{T_{tr}}{2} \le t \le \frac{T_{tr}}{2} \\ 0, & |t| > \frac{T_{tr}}{2} \end{cases} \tag{2.7}$$

In the SERDES communication link, since the data transitions randomly happen and CM spikes are generated by these data transitions, the CM signal *N(t)* can be described as the convolution of *X(t)* and an infinite random sequence *C(t)* [28], as shown in Fig. 2.25. The function *C(t)* is composed of an infinite number of random delta functions (with the area of unit 1) at uniform time interval T_b and it is defined with its statistic expectation, $E\{C(t)\}$, as (2.8). *C(t)* is described such that at every time interval of T_b, there is a 50% probability of being a delta function with an area of 1, thus the expectation of *C(t)* is a comb function with the 1/2 delta functions equally spaced with an interval of T_b.

$$E\{C(t)\} = \sum_x \sum_n p(x) \cdot \delta(t - nT_b) = \frac{1}{2} \sum_n \delta(t - nT_b), x \in \{0,1\},$$
$$p(0) = P(C(nT_b) = 0) = p(1) = P(C(nT_b) = 1) = \frac{1}{2} \tag{2.8}$$

Because the random signal is stationary and it is time-independent, *C(t)* can be statistically analyzed by the autocorrelation function $\Re_C(\tau)$:

$$\Re_C(\tau) = E\{C(t) \cdot C^*(t - \tau)\}. \tag{2.9}$$

Because $C(t)$ is a real function, $C(t)$ equals $C^*(t)$. The autocorrelation $\Re_C(\tau)$ is further calculated as shown in (2.10). As depicted in Fig. 2.27, the autocorrelation can be expressed as the sum of a comb function $\Re_1(\tau)$ and a delta function $\Re_2(\tau)$ with an area of $\frac{1}{4T_b}$.

$$\Re_C(\tau) = \begin{cases} \frac{1}{2NT_b} \lim_{N\to\infty} \sum_{k=-N}^{N} \frac{1}{4} C(kT_b) C(kT_b - \tau) = \frac{1}{4T_b} \sum_n \delta(\tau - nT_b), & \tau \neq 0 \\ \frac{1}{2NT_b} \lim_{N\to\infty} \sum_{k=-N}^{N} \frac{1}{2} C^2(kT_b) = \frac{1}{2T_b}, & \tau = 0 \end{cases} \tag{2.10}$$

It has been proved that the Fourier transform of the autocorrelation of a finite power signal is the power spectral density (PSD) function. Thus, the PSD function $S_C(f)$ of *C(t)* is calculated in (2.11):

$$S_C(f) = F(\Re_C) = F(\Re_1 + \Re_2) = F(\Re_1) + F(\Re_2). \tag{2.11}$$

The Fourier transforms of the comb function $\Re_1(\tau)$ and the delta function $\Re_2(\tau)$ are easily obtained, and the calculated $S_C(f)$ is depicted in (2.12):

$$S_C(f) = \frac{1}{4T_b} + \frac{1}{4T_b^2} \sum_n \delta(f - n\frac{1}{T_b}) = F_C(f) F_C^*(f) = \left\| F_C(f) \right\|^2. \tag{2.12}$$

According to the PSD function above, the amplitude of Fourier transfer of the random sequence $\left\| F_C(f) \right\|$ can be estimated as

$$\left\|F_C(f)\right\| = \begin{cases} \sqrt{\frac{1}{4T_b} + \frac{1}{4T_b^2}\sum_n \delta(f - n\frac{1}{T_b})} \approx \frac{1}{2T_b}, & f = n\frac{1}{T_b} \\ \sqrt{\frac{1}{4T_b}}, & f \neq n\frac{1}{T_b} \end{cases}. \tag{2.13}$$

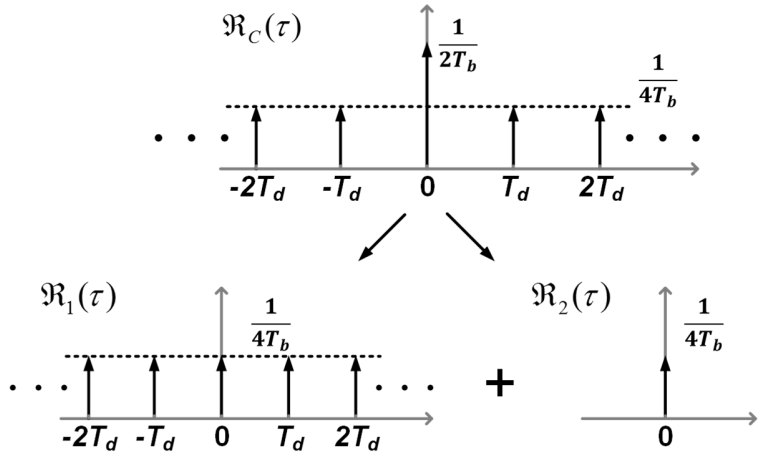


Fig. 2.27 Calculated autocorrelation for *C(t)*

CM noise signal *N(t)* is the convolution of the triangle function *x(t)* and the random function *C(t)*. And the convolution in the time domain is equivalent to multiplication in the frequency domain. Thus, the Fourier transform of *N(t)* equals the multiplication of *F(x(t))* and $F_C(f)$.

According to the results in (2.6) and the simplification of the single CM voltage spike, when $T_1=T_2=T_{tr}/2$, the Fourier transform of the triangle function *x(t)* is calculated in (2.14):

$$X(f) = F(x(t)) = \frac{1}{2} AT_{tr} \cdot \sin c^2(\pi \frac{T_{tr}}{2} f). \tag{2.14}$$

The Fourier transform *X(f)* is a real function since *x(t)* is a real, even function. Thus, the amplitude of N(t) can be calculated as

$$\left\|N(f)\right\| = \left\|X(f) \cdot F_C(f)\right\| = X(f) \cdot \left\|F_C(f)\right\|. \tag{2.15}$$

By substituting (2.13) and (2.14) into (2.15), the magnitude of the CM signal spectrum, $\left\|N(f)\right\|$, is calculated as (2.16), where $T_b << 1$ (for high-speed SERDES link, T_b is on the scale of a

nanosecond or even picosecond). The behavior-level simulation results are shown in Fig. 2.28, where the *sinc* function providing the spectrum envelope and the noise tone at $1/T_b$ is the largest one among all the harmonics.

$$\left\|N(f)\right\| \approx \begin{cases} \frac{1}{4} A T_{tr} \frac{1}{T_b} \cdot \sin c^2(\pi \frac{T_{tr}}{2} f), & f = \frac{n}{T_b} \\ \frac{1}{4} A T_{tr} \sqrt{\frac{1}{T_b}} \cdot \sin c^2(\pi \frac{T_{tr}}{2} f), & f \neq \frac{n}{T_b} \end{cases}, n \in Z . \tag{2.16}$$

It is to be noted that the double Nyquist frequency, $2F_{Nyquist}$, in an NRZ SERDES link is exactly $1/T_b$, and the CM noise at $2F_{Nyuist}$ is calculated in (2.17) by substituting (2.5).

$$N(2F_{Nyquist}) = N(\frac{1}{T_b}) = \frac{1}{4} A \frac{T_{tr}}{T_b} \cdot \sin c^2(\frac{\pi}{2} \cdot \frac{T_{tr}}{T_b}) = \frac{1}{8} Amp \frac{\left|t_{rise} - t_{fall}\right|}{T_b} \cdot \sin c^2(\frac{\pi}{2} \cdot \frac{T_{tr}}{T_b}). \tag{2.17}$$

From the results in (2.17), the CM noise is basically determined by the ratio of the data transition time over the data period $\frac{T_{tr}}{T_b}$, and the amplitude A of each CM spike because A is also positively correlated to the full signal swing *Amp* as shown in (2.5). The above relationships are summarized in (2.18). When optimizing the CM noise for a SERDES link with a certain data rate ($1/T_b$), the signal swing, data transition period and the mismatch between rising and falling edges are the key factors.

$$N(2F_{Nyquist}) \propto A \cdot T_{tr} \cdot \frac{1}{T_b} \propto Amp \cdot \left|t_{rise} - t_{fall}\right| \cdot \frac{1}{T_b} \tag{2.18}$$

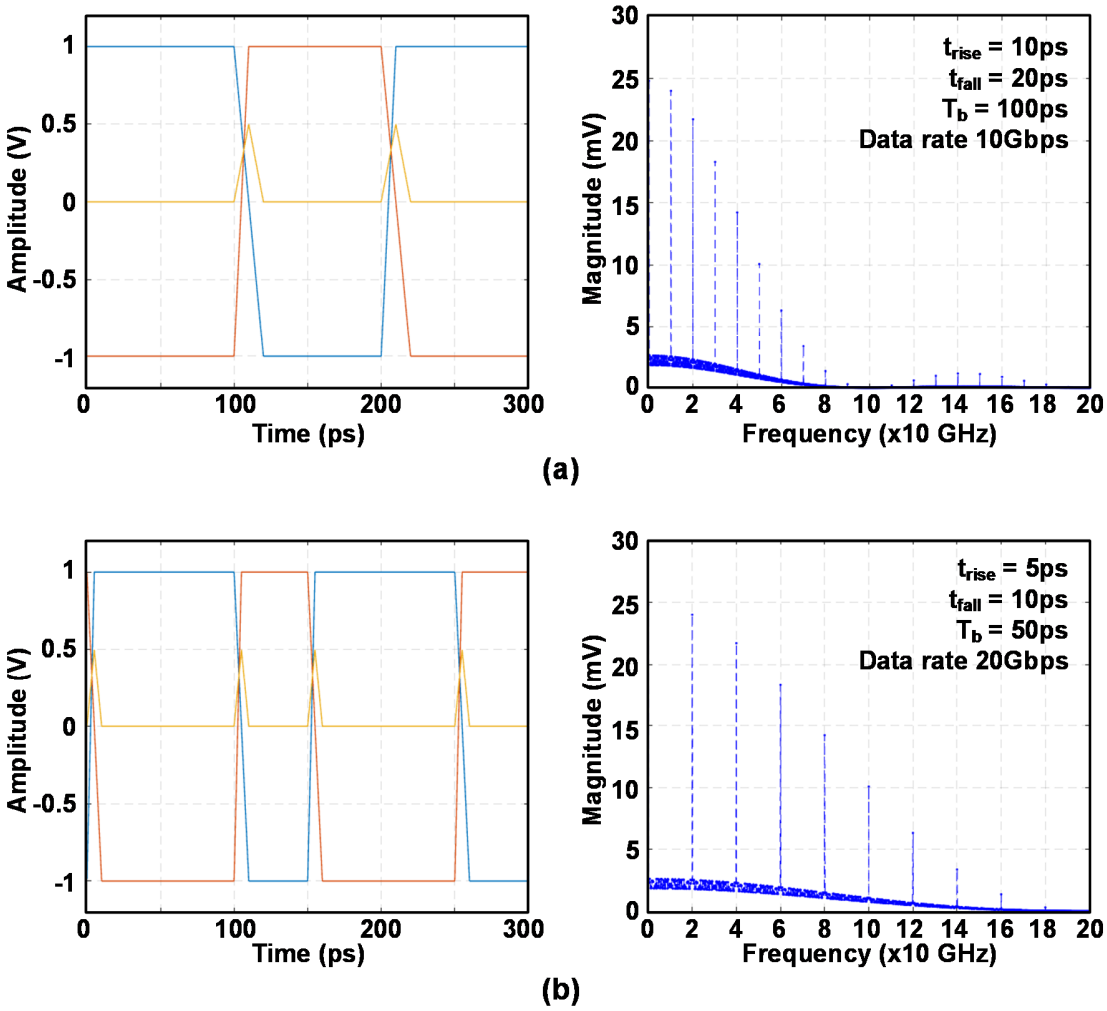


Fig. 2.28 Simulated CM noise waveforms and the corresponding spectrums. (a) 10 Gbps and (b) 20 Gbps.

Chapter 3 Circuit Analysis of a NRZ SERDES Link

3.1 Simulation-Based Analysis on High-Speed CML Drivers

According to the analysis in Chapter 2, the non-linear distortion, caused by the mismatch of rising and falling edges of the TX output signals, actually generates the original CM noise at $2f_{Nyquist}$, and this CM noise dominates the EMC of entire SERDES link EMC.

For the high-speed communication in the backplane link, the current mode logic (CML) circuit is widely used for the I/O driver in the TX and RX [29]. Thus, in this section, a transistor-level CML-based driver circuit in a 65 nm CMOS process is simulated and analyzed to further unveil the reasons of the mismatch of rising and falling edges, and the mechanism of CM noise generation.

3.1.I Theoretical Calculation on Ideal CML Drivers

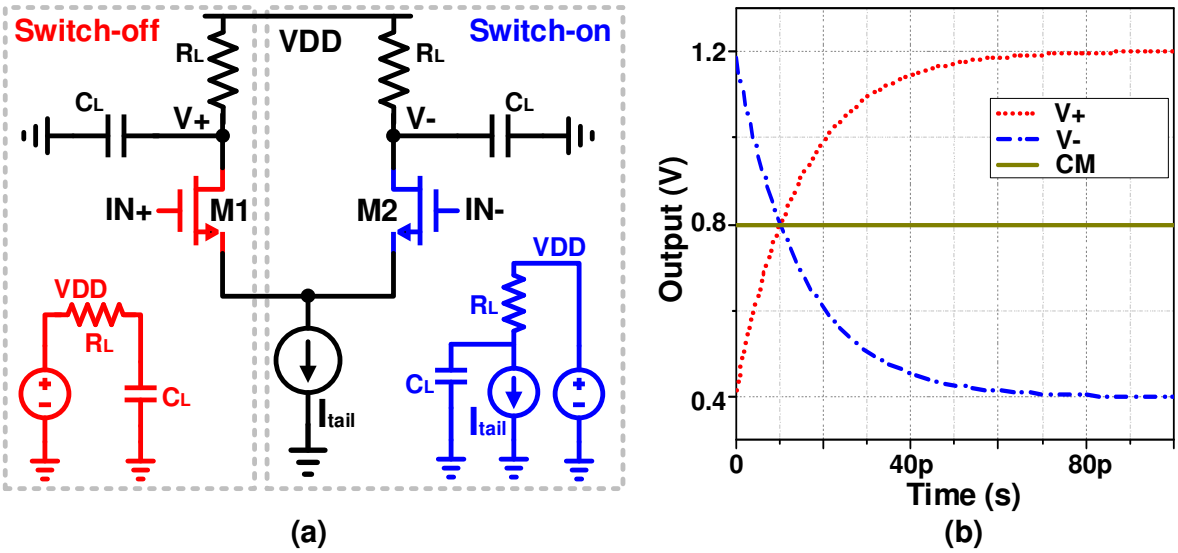


Fig. 3.1 (a) Schematic of a CML driver; (b) transient output waveforms of an ideal CML driver.

A CML-based driver circuit with resistor and capacitor loading is shown in Fig. 3.1(a). The input differential transistors M1 and M2 are biased and operated by the input signals, IN+ and IN-,

to steer the current through the loading resistors, R_L. The AC currents flow through the differential resistive loading and subsequently creates the differential output signals.

When ideal switches with zero on-resistance and infinite off-resistance are used for the input differential transistors (M1 and M2), only the loading resistor, R_L, and the capacitor, C_L, determine the rising and falling edges during data transitions. To describe the rising edge at output node *V*+, the differential equation and initial value V_{+0} are written as in (3.1):

$$\frac{V_{dd} - V_+}{R_L} = C_L \cdot \frac{dV_+}{dt}, \qquad V_{+0} = V_{dd} - I \cdot R_L . \tag{3.1}$$

The calculated rising edge is (3.2):

$$V_+ = (V_{dd} - I \cdot R_L) + I \cdot R_L (1 - e^{-\frac{1}{R_L \cdot C_L} t}) . \tag{3.2}$$

Similarly, to describe the falling edge at output node *V*-, the differential equation and initial value V_{-0} are written as in (3.3):

$$\frac{V_{dd} - V_-}{R_L} = I + C_L \cdot \frac{dV_-}{dt}, \qquad V_{-0} = V_{dd} . \tag{3.3}$$

The corresponding calculated result is (3.4):

$$V_- = V_{dd} - I \cdot R_L (1 - e^{-\frac{1}{R_L \cdot C_L} t}) . \tag{3.4}$$

Comparing the calculation results in (3.2) and (3.4), the exponentials in both equations, which describe the charging and discharging procedures, they have same expression with variables of R_L and C_L. Thus, as shown in Fig. 3.1(b), the corresponding simulated rising and falling edges are fully symmetrical and there is no CM noise or voltage spike generated when the input transistors operate as ideal switches.

3.1.II Non-Linear Parasitic Effects in CML Driver Circuit

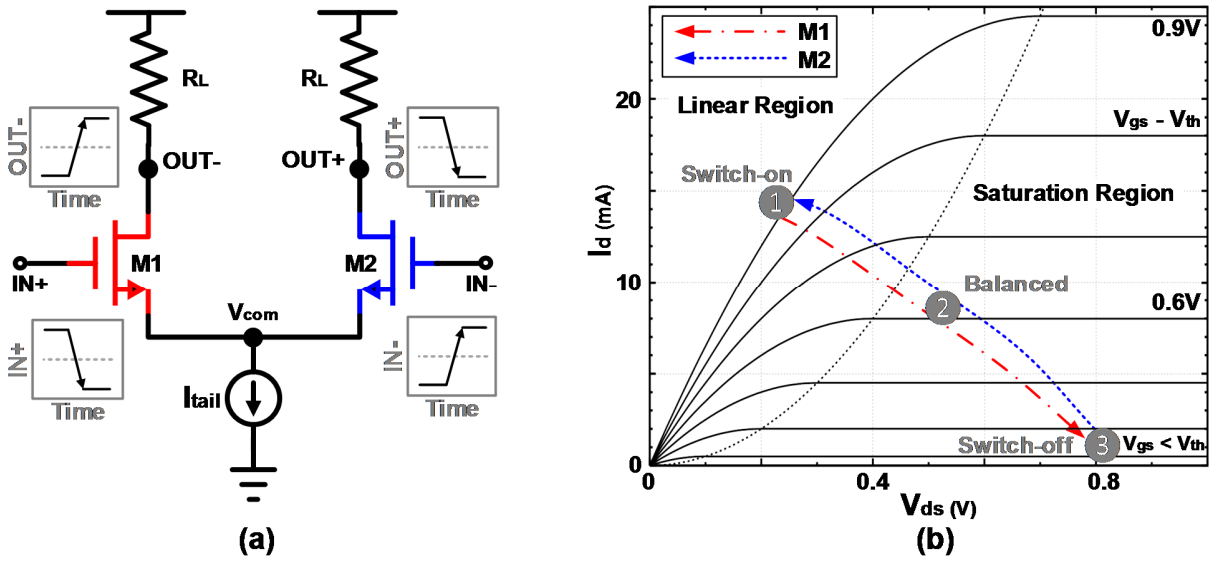


Fig. 3.2 (a) Schematic of a CML driver; (b) operation condition changes of the switching transistors.

However, in transistor-level analysis, the parasitic impedance at the metal-oxide semiconductor field-effect transistor (MOSFET) output nodes should be included into the simulation, i.e. the stray capacitors at drain node and the on-resistance of the transistor. All the parasitic capacitors and resistors are part of the loading of the CML driver, and this parasitic impedance varies with the migration of the transistor operation region during each data transition.

In the CML driver in Fig. 3.2(a), the W/L ratio of M1 and M2 is 60 um/60 nm, the tail current, I_{tail}, is 18.1 mA, and the loading resistor R_L equals 50 Ω. According to the simulation results, the Norton equivalent circuits at output node *V*+ for switch-off transistor M1, and node *V*- for switch-on transistor M2, are presented in Fig. 3.3(a). The calculated results show the significant difference of output impedance, including the equivalent on-resistance and the parasitic capacitance, between the "switch-off" transistor M1 and "switch-on" transistor M2.

In the transistor I-V curve plotted in Fig. 3.2(b), the "switch-off" status is corresponding to the "off" region (region 3) and the "switch-on" status corresponds to the linear region (region 1).

During the data rising edge, M1 in Fig. 3.2(a) is experiencing the data rising edge and its corresponding operation region migrates from the linear region to the "off" region (1 → 2 → 3), as the M1 curve in Fig. 3.2(b).

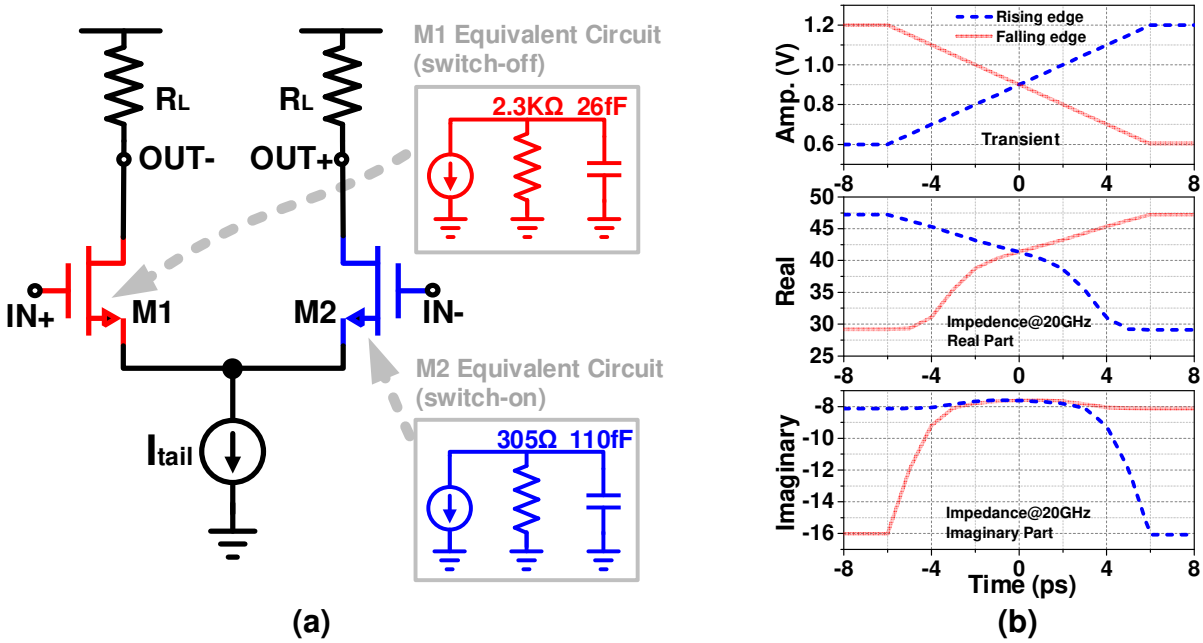


Fig. 3.3 (a) CML driver and the corresponding Norton equivalent circuits for switching transistors; (b) simulated impedance variations during rising and falling edges.

At meanwhile, during the data falling edge, transistor M2 on the other side, is switching on and going through a reverse procedure from the "off" region to the linear region (3 → 2 → 1), as presented by the M2 curve in Fig. 3.2(b).

Fig. 3.3(b) also shows the simulated impedance variation during data rising and falling edges. During the 10 ps of data transition period, as shown in the top figure of Fig. 3.3(b), the corresponding real and imaginary parts of the output impedances of both M1 and M2 are separately shown in the middle and bottom plots.

Thus, from the analysis above, the differential transistors are going through two different procedures during rising and falling edges, and this difference generates the asymmetric rising and

falling edges [12]. Eventually, the asymmetry and mismatch of rising and falling edges, known as the non-linear distortion in the last chapter, generates the CM noise at $2f_{Nyquist}$. Because the impedance variation at the transistor output node directly contributes to the CM noise at $2f_{Nyuist}$, several circuit design factors, which affect transistor parasitic impedance, need to be investigated for CM noise behavior characterization in the following section, including the temperature, process corner, signal swing, and the biasing voltage for input differential transistors [12], [30].

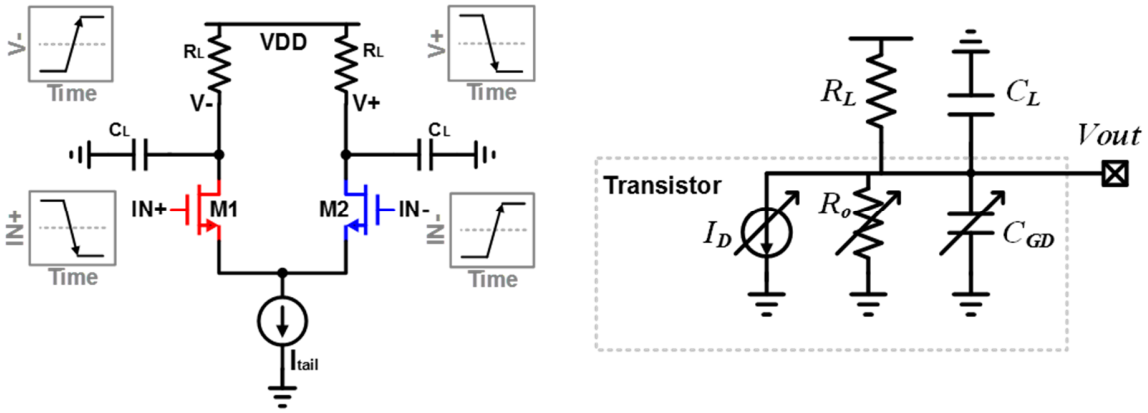


Fig. 3.4 Equivalent circuit of simplified CML driver

In other words, the equivalent circuit in Fig. 3.4 also gives a hint about the rising and falling edge mismatch. During the data transition period, the differential transistors (M1 and M2) are working under different operation regions, thus, the parasitic capacitance and output resistance vary with the transistor status. Because the varying parasitic capacitance and output resistance are part of the loading network, rising and falling edge are intrinsically unbalanced. It also implies that optimize the ratio of parasitic impedance and off-chip loading impedance helps balancing the rising and falling edges.

In advanced technology nodes, e.g. 28nm and 16nm, transistor with smaller size can provide same amount of driving capability (g_m, current), and the parasitic capacitance is proportionally reduced which seems helps balancing the rising and falling edges. However, when the transistor size is fabricated with a more advanced technology, it becomes sensitive to the change of operating

condition. It means that when applying same signal swing, the variation of parasitic impedance becomes more significant in advanced technology. On one hand, the advanced technology helps proportionally reducing the parasitic influence. On the other hand, the advanced technology makes the devices more sensitive to the change of operation conditions, which potentially causes more significant mismatch between rise and fall time. Therefore, it is still hard to predict the trend of EMI related CM noise under different technologies. At this stage, it is still highly recommended to use accurate transistor-level models to evaluate and simulate the CM noise.

3.1.III CM Noise under Different Process Corners

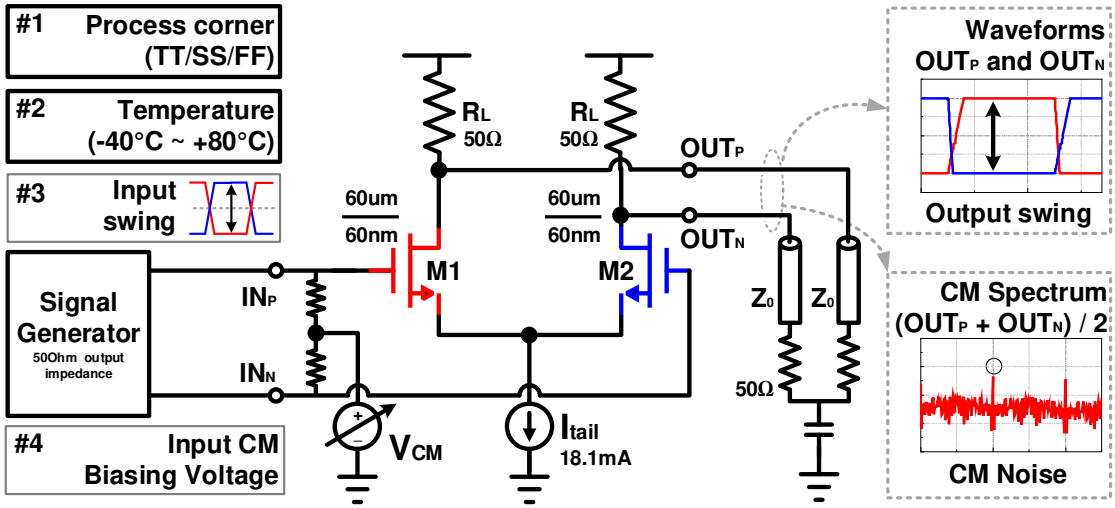


Fig. 3.5 Corner simulation setup.

In order to investigate the design factors mentioned in last section, a simulation setup of the CML based driver is described in Fig. 3.5. A Verilog-A-based signal generator drives the CML driver with non-distorted differential 20 Gbps PRBS signals, and the differential signals are AC coupled to the input of the CML driver for the adjustability of input CM biasing voltage. The CML

driver outputs (OUT_P and OUT_N) are connected to an s-parameter-based PCB-trace models with a characteristic impedance Z_0 of 50 Ω.

Within the simulation setup, four different design factors, including process corner, temperature, input signal swing (IN_P and IN_N) and input CM biasing voltage (V_{CM}), are modified and the signals at output nodes (OUT_P and OUT_N) are observed. Both the transient waveforms and the output CM spectrum are monitored to evaluate the output signal swing and CM noise. In the simulation setup, evaluating the CM noise is for the EMI concern, and monitoring the output signal swing is for the data quality consideration.

During IC manufacturing, the process corner indicates the extreme conditions of the global variation of fabrication parameters and the performance of semiconductor devices [31]. Since the CML driver circuit in Fig. 3.5 consists of only N-type transistors, only typical-typical (TT), fast-fast (FF) and slow-slow (SS) corners are considered to evaluate the CM noise behaviors under different process corners. The schematic-level simulation results under different process corners are shown in Table II.

Table II Simulation results under different process corners

	Schematic-level Simulation		
Process Corner	**FF**	**TT**	**SS**
Simulated CM Noise	0.277mV	3.0mV	10.9mV

A comparison between the results under TT, FF and SS corners shows that fast transistors under a FF corner lead to a relatively small CM noise because transistors under a FF corner with maximum carrier mobility behaves most similarly to ideal switches and the transistors under a FF corner have a shorter data transient period. In Chapter 2, it has been proved that the signal CM noise is positively correlated to the data transition period, T_{tr}, thus, the parasitic impedance

variation of the transistors under a FF corner has a relatively weaker influence to the CM noise during each data transition.

Another alternative simulation to further verify the conclusion mentioned above is to intentionally change the transistor switching speed by adjusting the rising and falling edges of input signals, as shown in Fig. 3.6. It is to be noted that the process corner is given as FF in this simulation and the simulated output CM noise result is plotted in Fig. 3.7.

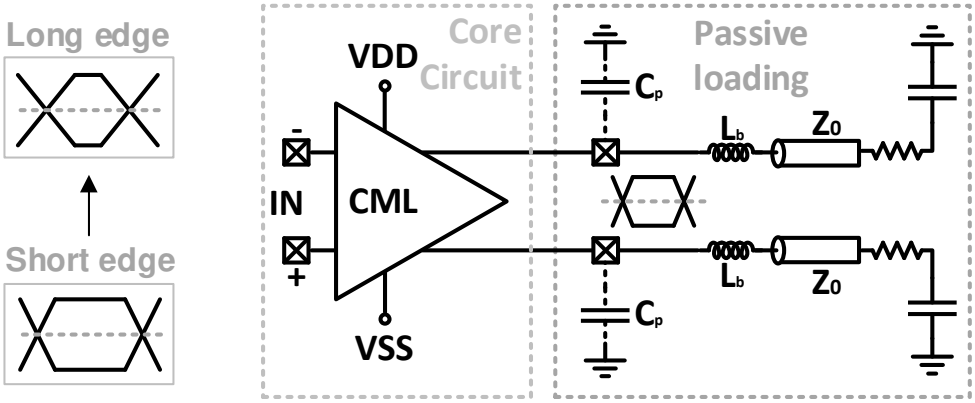


Fig. 3.6 Edge time simulation setup.

Short edge time leads to short data transition T_{tr}, and consequentially small CM noise, because when the data transition time is short, the non-linearity effect during the switching procedure has less impact on the CM noise. Obviously, the conclusion matches with the previous simulation results in Table II.

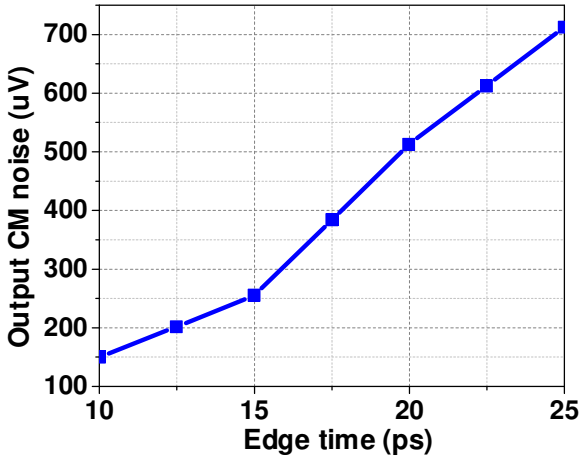


Fig. 3.7 Simulated edge time vs. output CM noise @ FF corner

3.1.IV Temperature Effects on CM Noise

To analyze the temperature influence on CM noise, the simulation setup is built as Fig. 3.8. All the simulation environments are kept as same as the setup in Fig. 3.5, and only the simulation temperature is swept from -40 Celsius to 80 Celsius. In the simulation, the process corner is set to be TT.

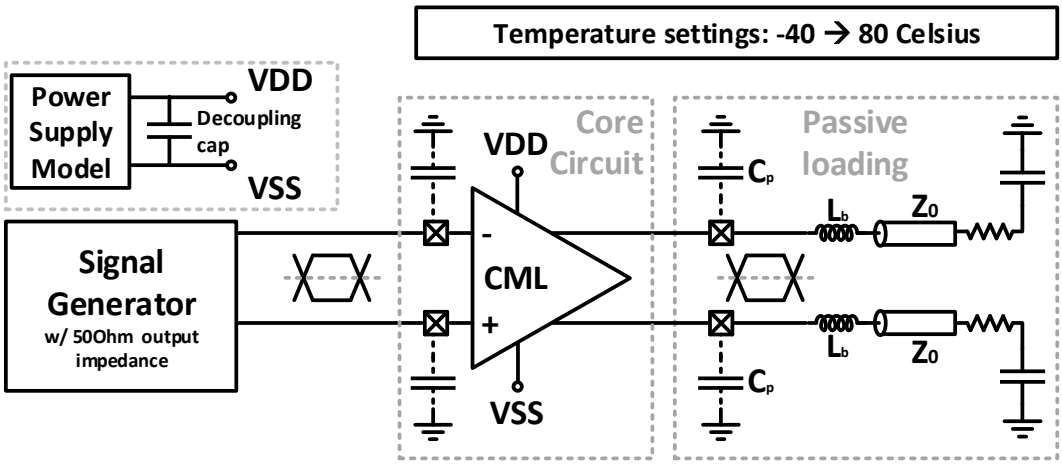


Fig. 3.8 Temperature simulation setup.

In a typical IC design flow, temperature is one of the key factors for circuit evaluation because the semiconductor performance has large temperature dependency. Fig. 3.9 depicts the simulated plot of the correlation between temperature and CM noise under the TT process corner.

Taking the CM noise at 20 °C for the reference, the CM noise under different temperatures are normalized to the CM noise at 20 °C, and the slope of the simulated temperature plot is calculated. The CM noise plot has been divided into two sections by the data point at 20 °C. When the circuit operating temperature is below 20°C, the CM noise changes 0.43% per Celsius, and when the operating temperature is above 20°C, CM noise changes 0.27% per Celsius, respectively.

The simulation results in Fig. 3.9 is concluded that, when the operating temperature of the core circuit varies positively or natively 20°C different from the typical room temperature (about 27°C), the temperature variation will introduces a 5 – 9% variation on CM noise, which is actually ignorable. However, when the circuit is operated under extreme temperatures, e.g. -40 °C or 80 °C, the CM noise can be over 20% different from the CM noise under typical room temperature.

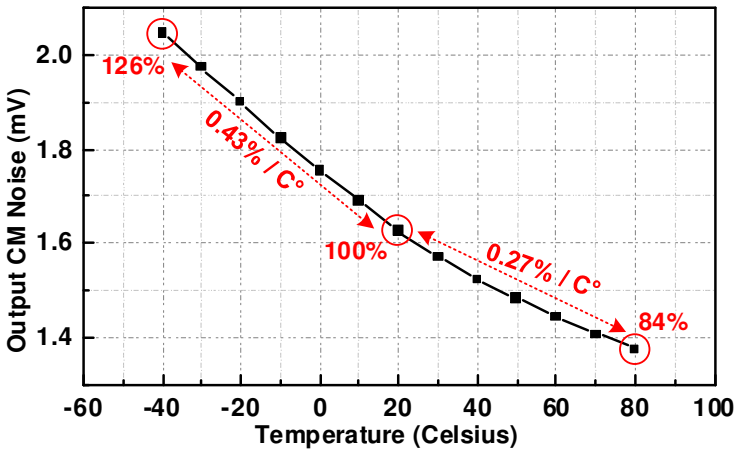


Fig. 3.9 Simulated temperature vs. output CM noise.

3.1.V Correlation between CM noise and input swing

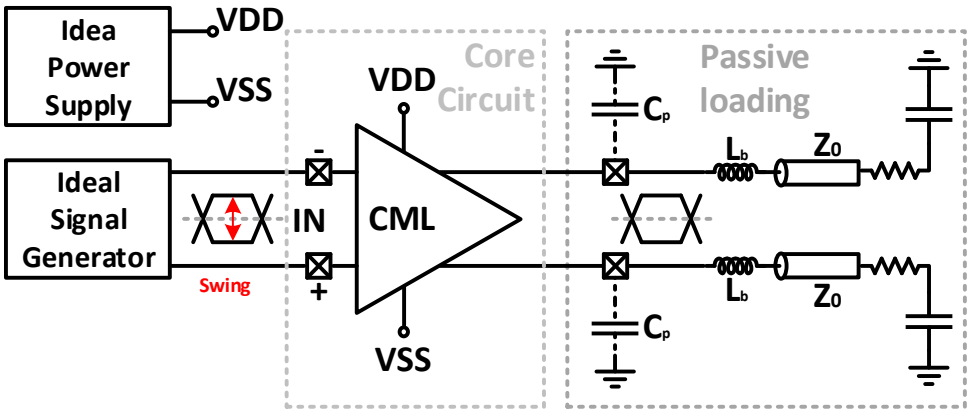


Fig. 3.10 Simulation setup for the signal swing vs. CM noise.

Referring to the analysis in Chapter 2, the CM noise is proportional to the input signal swing. Thus, in this section, a transistor-level simulation is performed to verify the correlation between signal swing and CM noise, as depicted in Fig. 3.10. Because the temperature and process corner affect the CM noise, the entire setup is simulated under a temperature of 27 °C and a TT process corner. By changing the input signal swing, the CM noise behavior at the driver output is obtained as the plots in Fig. 3.11. The output CM noise at $2f_{Nyquist}$ and the input signal swing are normalized to the corresponding max values. When the input signal swing increases, both the output signal swing and output CM noise are increasing, which is consistent with the analysis in Chapter 2.

However, the saturation of the output signal swing happens before the saturation of CM noise. For example, in this case, when the input signal swing reduces from 400mV to 250mV, the CM noise is reduced about 30% from the maximum, while the output signal swing is only reduced by 10% from the maximum signal swing.

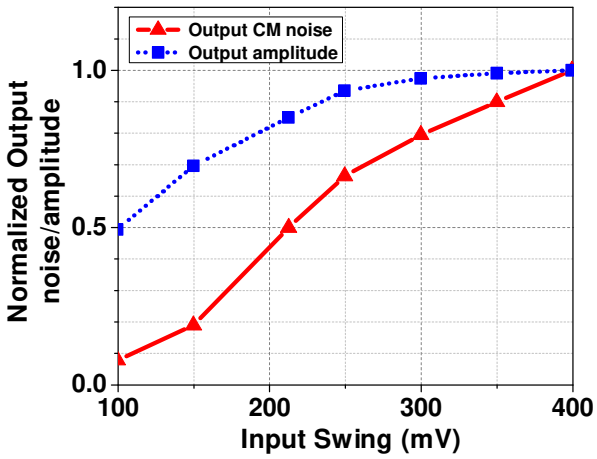


Fig. 3.11 Plot of input signal swing vs. output CM noise and output signal amplitude.

Because the CM noise saturates faster than the signal swing, this observation actually provides a trade-off between signal swing and CM noise when optimizing the circuit CM noise performance. No like the circuit bandwidth or the driving capability, CM noise is not the first prior consideration for circuit design. However, when the circuit design is physically fixed, is there still any method to optimize CM noise performance?

Recalling from the previous analysis in Chapter 2, the ways to reduce CM noise, in a high-speed wireline link, are reducing the data transition, T_{tr}, minimizing the edge mismatch, $\left|t_{rise}-t_{fall}\right|$, and reducing the signal swing. It is to be noted that, in Fig. 3.5, after the physical design of CML driver is fixed, the input biasing voltage and input signal swing are still free to control. Thus, in the following section, we will discuss the CM noise reduction techniques based on controlling the input biasing voltage, V_{CM}, and the input signal swing, Amp.

3.1.VI Preliminary Optimization of CM Noise

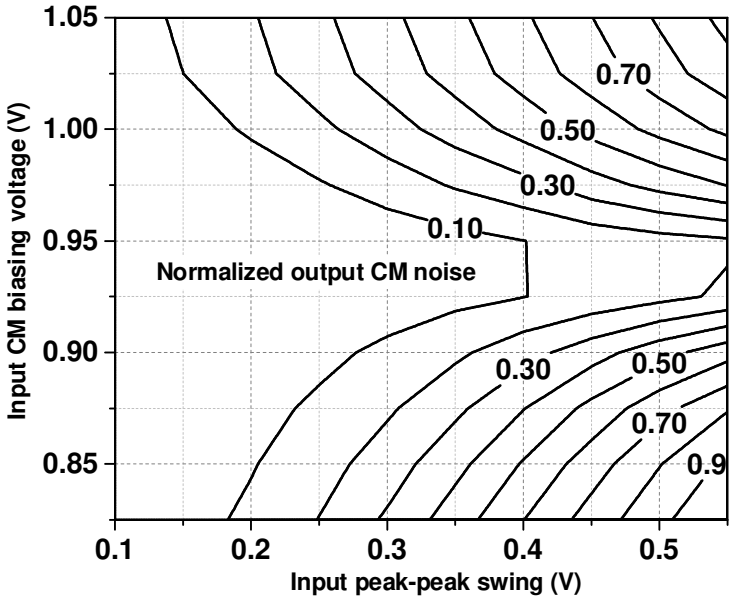


Fig. 3.12 Contour plot of the input swing, input CM biasing voltage and normalized output CM noise.

Because the CM radiation dominates the EMI emission in the high-speed SERDES link, previous research works have proposed different optimization methods for CM noise reduction. A general review of previous CM noise reduction techniques is summarized in [32]. The CM reduction techniques include the optimization of data interconnection and channel layout [33]–[36], passive filtering techniques for differential signals [23], [37], [38], [19], [18], and improving the EMI immunity at the RX side [39], [40]. In[21], and [20], several circuit-level methods for CM noise reduction is proposed, and the proposed methods are in the perspective of system-level signaling. In [30], [41], similar CM noise issue is discussed. However, only simulation-based CM noise observations and corresponding CM noise suppression techniques are provided, and there is no detailed circuit-level analysis of CM noise generation or any experimental verification in these two works. Therefore, with the fundamental analysis in previous chapters, the possible methods are proposed to reduce CM noise at transistor-level in the TX side in the following sections.

With the same simulation setup shown in Fig. 3.5, we sweep both the input signal swing and the CM biasing voltage (V_{CM}) simultaneously and observe the corresponding CM noise at the driver output. The simulated contour plot is shown in Fig. 3.12. The CM noise is further reduced by tuning the biasing voltage, V_{CM}, at a given input swing, i.e., in this case, the relatively small CM noise (10% of maximum value) appears when the signal swing is set to be 0.4 V and the optimal input CM biasing voltage is about 0.92 to 0.95 V. However, the prior consideration for high-speed wireline communication is not CM noise, but the communication data quality. In another word, to maintain a reasonable communication quality, we need to have a reasonable signal quality, which is the signal to noise ratio (SNR). Referring to the observation in Fig. 3.12, changing both the signal swing and CM biasing voltage can significantly reduce CM noise. However, insufficient signal swing will reduce the eye-diagram opening of the output data and degrades communication quality.

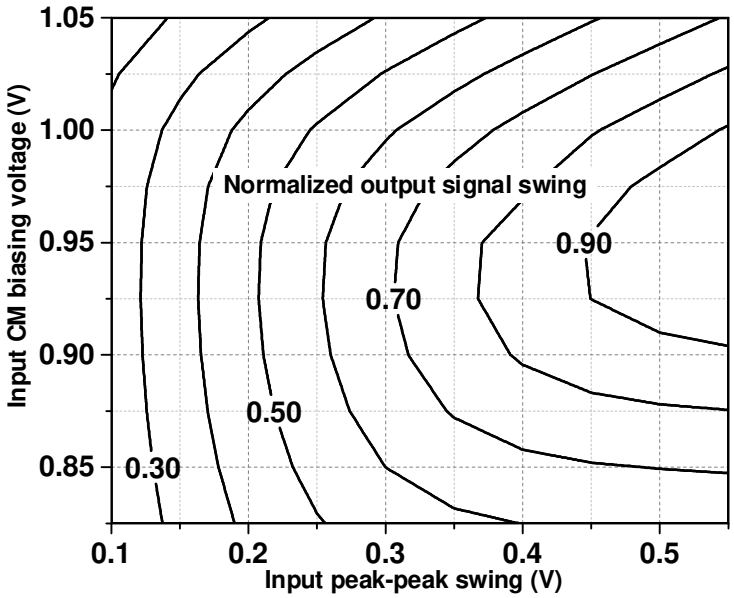


Fig. 3.13 Contour plot of the input swing, input CM biasing voltage and normalized output signal swing.

Instead of showing the output CM noise, Fig. 3.13 shows the simulated contour plots of the output signal swing when sweeping the input biasing voltage and the input signal swing

simultaneously. All the simulated data are normalized to the maximum in the plot. In this case, with a given input signal swing of 0.4 V, and the maximum output signal swing appears when the input CM biasing voltage is about 0.92 to 0.95 V.

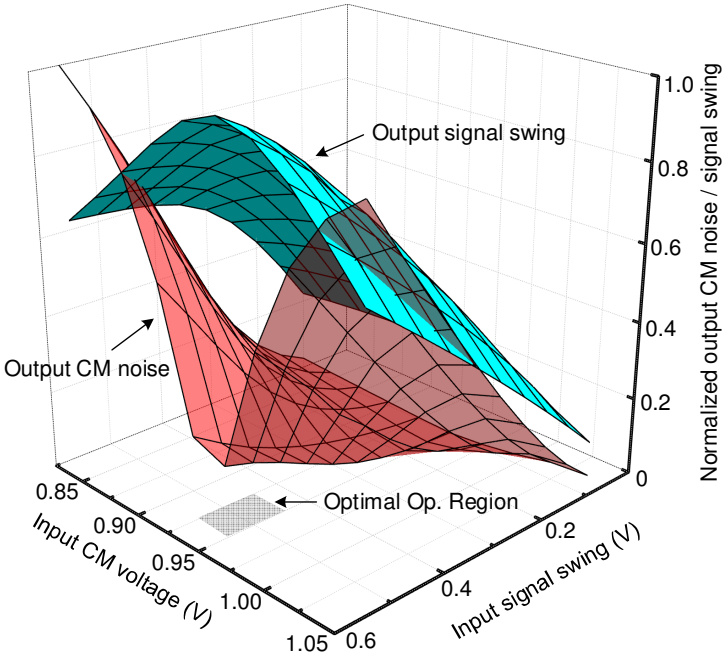


Fig. 3.14 Optimization for the CM noise in a CML driver.

Overlapping the results in Fig. 3.12 and Fig. 3.13 to make a 3-D contour plot in Fig. 3.14, it is such a coincidence that the large output swing and the relatively small CM noise happen at the same simulation condition. The normalized result shows that the optimal operating region for the output signal swing and CM noise actually overlap at the shadowed area, where the CML driver achieves sufficient output signal swing (>90%) and relatively small CM noise (<20%) simultaneously.

Thus, based on the observation in Fig. 3.14, an optimization method is proposed that, by optimizing the signal swing and the input biasing voltage of the CML driver, the EMI-related CM noise at $2F_{Nyquist}$ is significantly reduced by 80% when compared to the worst case.

3.2 Experiment and Verification

To validate the analysis in previous chapters, a CML driver test chip is designed, and fabricated in a 65 nm CMOS process. In the following section, the experimental results, including simulation and measurement, will be analyzed and compared with the previous conclusions.

3.2.I Test Driver Chip Design

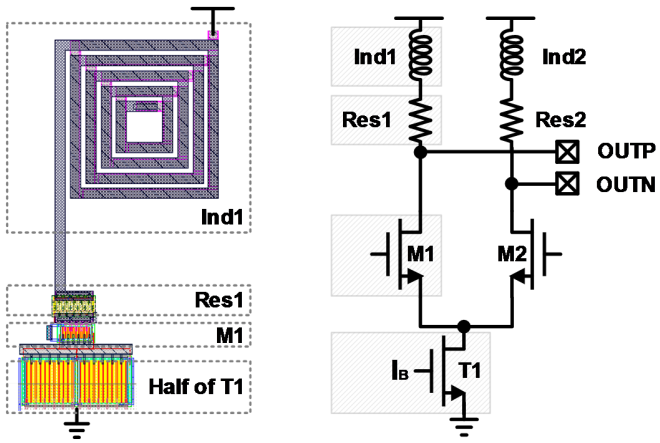


Fig. 3.15 Single stage of CML driver with inductive peaking

Fig. 3.16 and Fig. 3.17 show the circuit schematic and corresponding die photos, respectively. The total driver array consists of three identical paralleled CML drivers and each CML driver occupies a 0.3 mm×0.3 mm of area. The DC biasing pads and power pads are allocated at the top and bottom, and the high-speed differential input signals are fed into the circuit from the left-side ground-signal-ground (GSG) pads. The output signals come out from the right side GSG pads.

Each CML driver has three cascaded CML stages with identical topologies. The schematic and the corresponding layout of single CML stage is shown in Fig. 3.15. In order to support a data rate of 10 Gbps and above, each CML stage adopts an inductive shunt peaking technique for bandwidth extension [42], [43].

When the DC power supply is 1.2 V, the total DC biasing current for the all three paralleled CML drivers is 52 mA, which gives a total power consumption of 62.4 mW correspondingly.

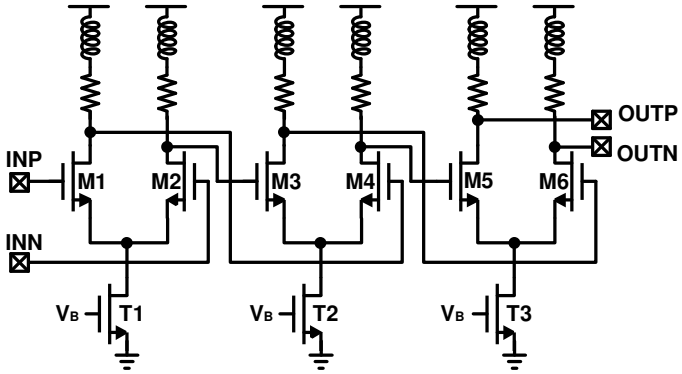


Fig. 3.16 Schematic of the CML driver test chip.

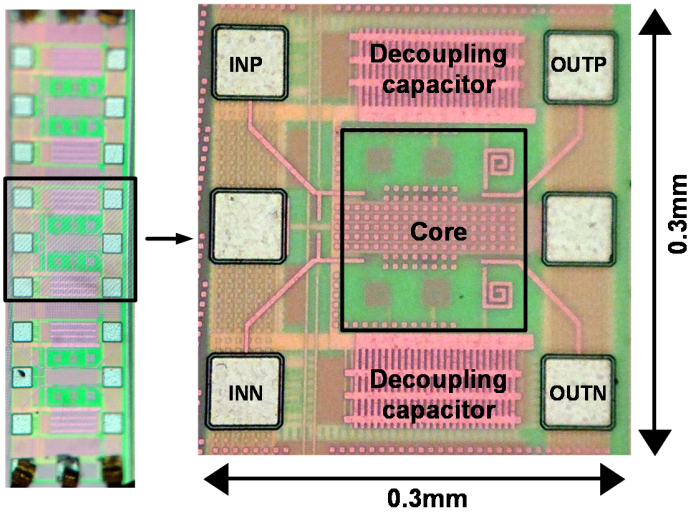


Fig. 3.17 Layout of the CML driver test chip

3.2.II Experimental Environment and Methods

The measurement setup for the test chip is depicted in Fig. 3.18 and Fig. 3.19. A high-speed pattern generator is used to generate a 10 Gbps differential PRBS as the input signal for the device under test (DUT). The generated differential signals are fed into the test chip through a broadband RF probe, and the output signals from the test chip are also led out through a broadband RF probe.

The passive interconnections, including the cables and connectors at both the input and output sides, have a DC-40 GHz bandwidth and a 50-Ω characteristic impedance.

In the first setup for monitoring the output signal swing in Fig. 3.18, one of the differential output signals from DUT goes into the Agilent 86100D sampling scope, and the other output is terminated with a broadband 50-Ω termination resistor for impedance balancing.

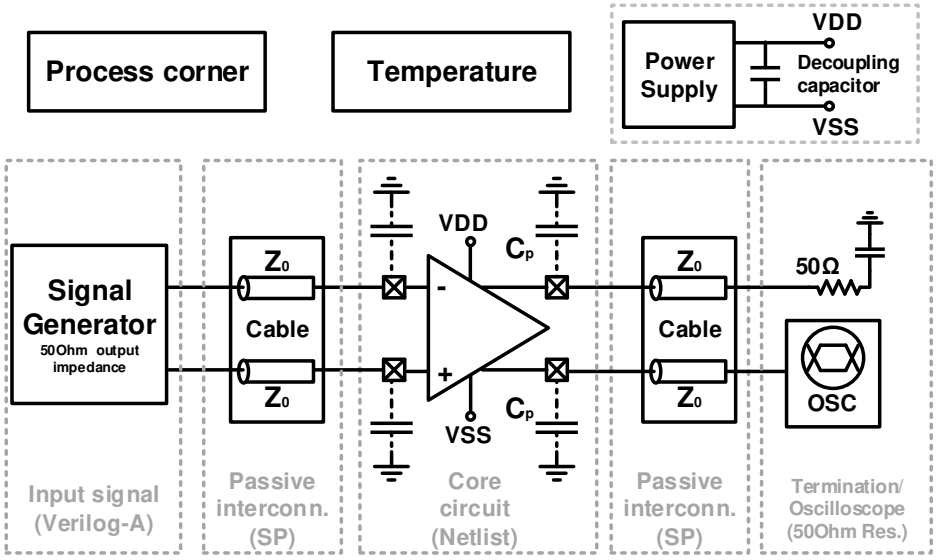


Fig. 3.18 Experimental setup for observing output transient waveform.

Fig. 3.19 shows the second setup for the output CM noise measurement. Different from the first measurement setup, a broadband passive power combiner is used to combine the differential output signals from the DUT, and to extract the CM signal in the output. The CM signal, from the power combiner output, goes into a broadband (DC-40 GHz) spectrum analyzer for the frequency domain analysis. The CM noise at $2f_{Nyquist}$ is displayed on the spectrum analyzer.

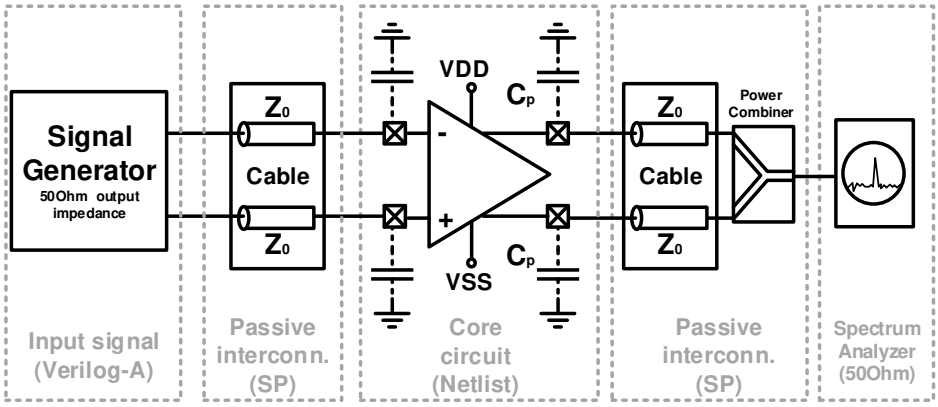


Fig. 3.19 Experimental setup for evaluating output CM noise.

To compare with the measured results, a corresponding reference simulation environment is built. A Verilog-A-based high-speed pattern generator with a 50-Ω output impedance generates the input differential PRBSs in the measurement setup. All the passive interconnections, including cables, connectors and the power combiner, are modeled with measured s-parameters, which are measured by a 0-40 GHz 4-port vector network analyzer (VNA). A post-layout model of the test chip, where all the chip-level parasitic capacitance and resistance are included, is used in the simulation.

However, as mentioned in previous sections, the temperature and process corner information should be also considered to perform a precise simulation, because these two factors affects the CM noise simulation results directly.

3.2.III Thermal Analysis and Process Corner Screening

In order to simulate the CM noise for verification, the chip operating temperature is simulated and estimated in this section. A 3-D modeling software is used to build a simplified 3-D model for the test chip and surrounding bond-wires and the PCB layers, as shown in Fig. 3.20. As described in the cross-section view of the DUT in Fig. 3.20, the test chip is modeled as a silicon cuboid, and

the height of the cuboid, also known as the chip thickness, is 300 um. The chip is surface-mounted on the PCB top layer, and the top layer has a 1.4 mil thickness with copper material. A very thin silver layer of the conductive silver epoxy is added between the silicon chip and the copper layer in the thermo-analysis setup. The PCB top layer lies on a dielectric layer with a Roger 4003 material, and the thickness of the Roger 4003 layer is 11.8 mil. The ground copper layer of the PCB is underneath the Roger 4003 layer, and it is also set to be the thermal boundary with a constant temperature of 300 K (room temperature). Three heat sources are added in the positions where the three paralleled CML drivers are located, referring to the test chip layout in Fig. 3.17. The heat power for each heat source is 21 mW, which is estimated according to the DC power consumption of each CML driver, as mentioned in last section.

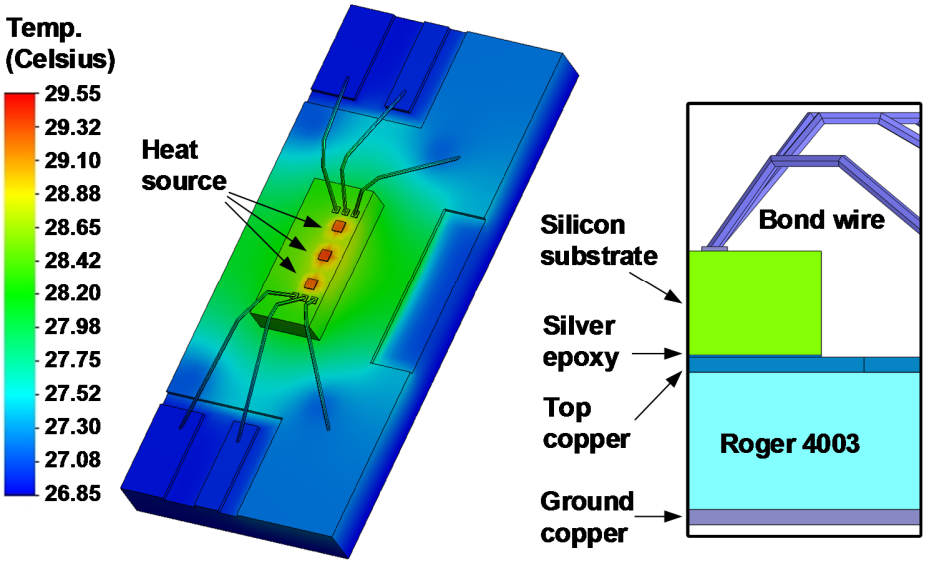


Fig. 3.20 Thermal simulation results and cross-section view of the PCB and the test chip.

The simulated heat transfer result in Fig. 3.20 shows that the locations of highest temperature (29.5°C) are at the three heat sources, and most of the heat goes through the silicon substrate and gets absorbed by the PCB ground plane. In this simulation, the total temperature rises less than 3°C during chip operation, which barely affects the CM noise performance (less than 1%)

according to the conclusions Fig. 3.9. **Thus, the simulation temperature is set to be 29°C for the following discussions.**

Besides the temperature, the process corner setting significantly affects the CM noise performance according to the previous simulation results in Table II. In order to obtain the process corner information of the measured chip samples and only consider the case in TT corner, we need to have a measurement method to screen out those unwanted chip samples in FF or SS corners.

In the simulation and measurement results in Fig. 3.21, when the DC power supply voltage varies from 0.9 to 1.3 V, the total DC current of the test chip exhibits distinctive behaviors under different process corner settings. The simulated DC current varies from 36 mA to 57 mA under TT corner, while it goes from 63 mA to 112 mA under FF corner as shown in Fig. 3.21. Thus, the DC current is used for chip samples screening in the measurement.

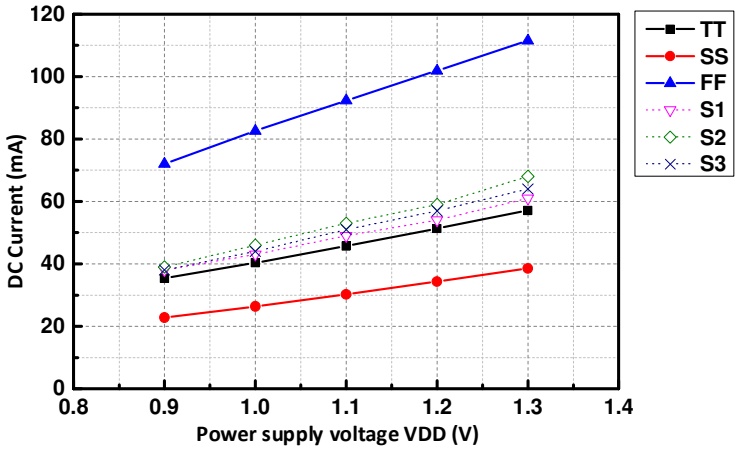


Fig. 3.21 Corner simulation and measurement result of DC currents.

The dotted plots in Fig. 3.21 are the measured DC currents from three different chip samples (S1, S2, and S3), which are fabricated and located within the TT corner. The measured DC currents are close to the simulated results in TT corner but far different from the results in FF or SS corner. All the chip samples are screened by the DC current and only those samples with a typical DC

power consumption (similar like S1, S2, and S3) are kept for the subsequent CM noise measurement.

3.2.IV Results of the Experiment

So far, the effects of temperature and process corner have been comprehensively considered through simulations and measurements. Thirteen chip samples, in TT corner, are screened by the DC power consumption measurement for the next CM noise measurement. In order to perform a fair comparison between the simulation and measurement, process corner settings is used to cover the global variation of the integrated circuit fabrication, besides, a Monte-Carlo simulation method is used to cover the local mismatch during fabrication.

All measured results from the 13 sample chips are plotted from Fig. 3.22 to Fig. 3.25. In the simulation, the Monte-Carlo simulation generates a range of confidence interval of the simulated CM noise, e.g., 95% of the measured CM noise data should locate within the interval of $\mu \pm \sigma$, where is μ the simulated average, and σ is the standard deviation.

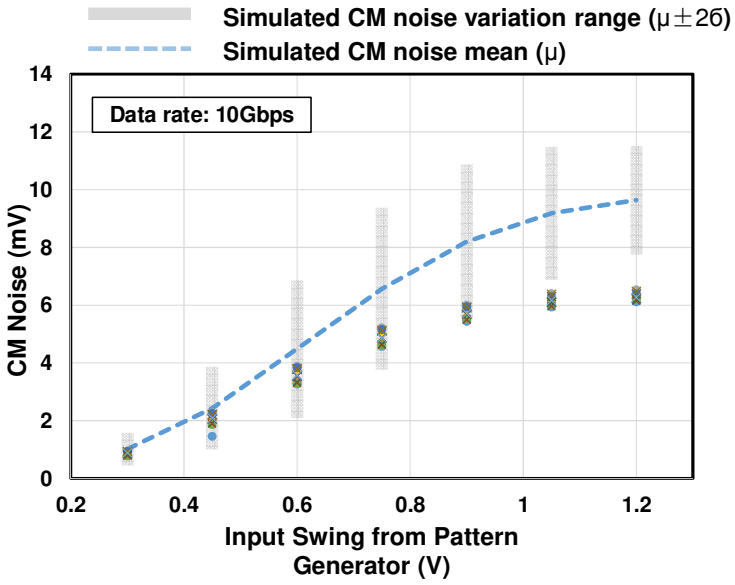


Fig. 3.22 Input Swing vs CM noise: simulation and measurement @ 10Gbps (left) /20Gbps (right)

Fig. 3.22 shows both the measured and simulated results of the input signal swing and output CM noise. The measured data proves the previous conclusions in Fig. 3.11, that the CM noise is positively correlated to the signal swing. During small signal operation region, e.g., the input swing is below 0.7 V, the correlation of CM noise and signal swing is almost linear as calculated in Chapter 2, and the measurement results all settle inside the confidence interval from the Monte-Carlo simulation.

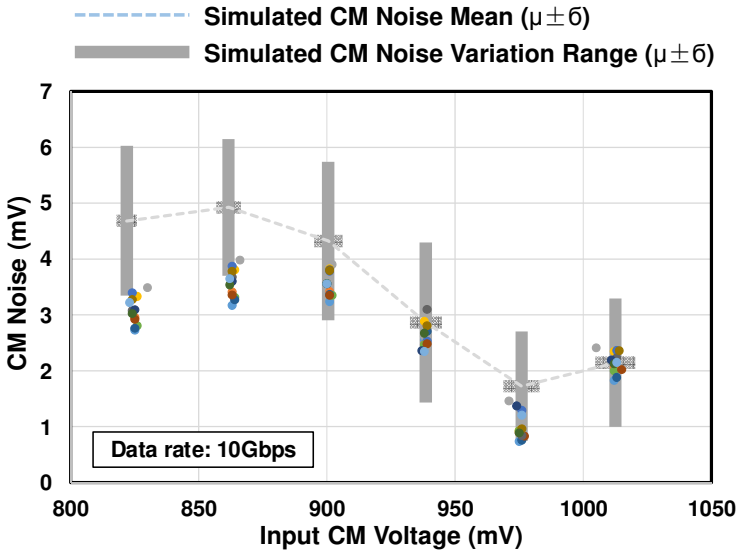


Fig. 3.23 Input CM Voltage vs. Simulated and Measured CM Noise @ 10Gbps (left) / 20Gbps (right)

Fig. 3.23 shows the simulated and measured CM noise plots when changing the input CM biasing voltage. The results are consistent with the previous analysis in Fig. 3.12. By comparing the simulated and measured results, the CM noise behavior qualitatively matches the well-modeled simulated setup. The measured data from 13 chip samples are located within the simulated interval of the Monte-Carlo simulation, and only several measured data points are located outside the simulated interval with acceptable difference when the input CM voltage is set as 820 mV. It is to be noted that, changing the input CM voltage is to balance the rising and falling edges when the transistors are switching, or, in other words, to minimize the mismatch of the rising and falling

edges, $\left|t_{rise}-t_{fall}\right|$, as analyzed in Chapter 2. Thus, there is only one optimal biasing point where the rising and falling edges are most balanced and the CM noise is also minimized.

The combined measurement results of both the output signal swing and the output CM noise are shown in Fig. 3.24, when the input CM biasing voltage is set to be 900 mV, and the input signal swing is swept. The measured results from 13 chip samples are plotted, and the average of 13 data in each measurement are linked to show the data trend. When the input signal swing increases, the output signal swing, and the CM noise increase, but the output swing saturates faster than the CM noise, which is consistent with the previous conclusion in Fig. 3.11. Therefore, to achieve a trade-off between the signal swing and the CM noise performance, the test CML driver can be operated in the shadowed region, as shown in Fig. 3.24, to reduce 30% of the CM noise and maintain 90% of output swing simultaneously.

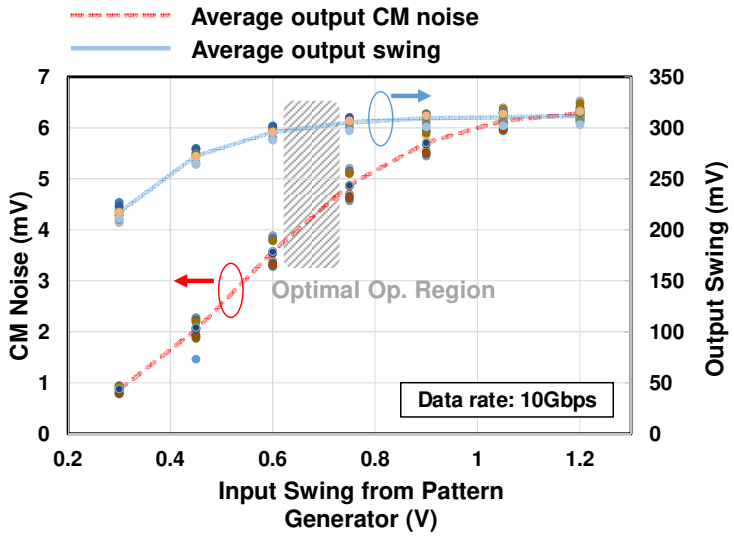


Fig. 3.24 Input Swing vs. Normalized Measured Output Swing & CM Noise

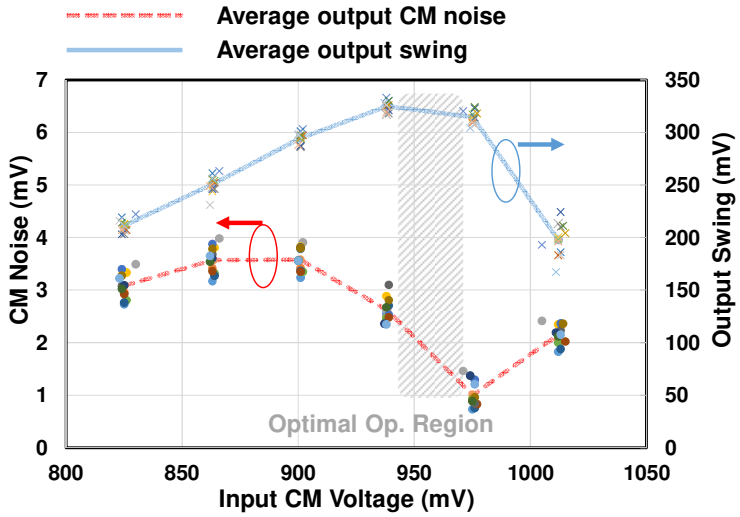


Fig. 3.25 Input CM Voltage vs. Normalized Measured Output Swing & CM Noise.

Moreover, the combined measurement results of both the output signal swing and the output CM noise are shown in Fig. 3.25, when the input signal swing is set to be 600 mV, and the input CM biasing voltage is swept. The measured results from 13 chip samples are plotted, and the average of 13 data in each measurement are linked to show the data trend. The CM noise is optimized to achieve a large output signal swing and a relatively small CM noise simultaneously when the test chip is operated at the shadowed region, as shown in Fig. 3.25. In the optimal operation region, the mismatch between rising and falling edge, $\left|t_{rise}-t_{fall}\right|$, is minimized to reduce the CM noise. At meanwhile, the large transconductance, G_m, of the transistors provides sufficient output swing, shortens the data transition period, T_{tr}, and finally reduces the CM noise.

$$N(2F_{Nyquist}) \propto A \cdot T_{tr} \cdot \frac{1}{T_b} \propto Amp \cdot \left|t_{rise}-t_{fall}\right| \cdot \frac{1}{T_b} \tag{3.5}$$

Recalling the conclusions on CM noise at 2FNyquist in Chapter 2, as shown in (3.5), the measurement results of the test chip consistently matches the previous calculation and conclusions. The comparisons in Fig. 3.22 and Fig. 3.23 between the Monte-Carlo simulation results and measurement results also indicate the consistency.

3.2.V EMI Field Measurement Results

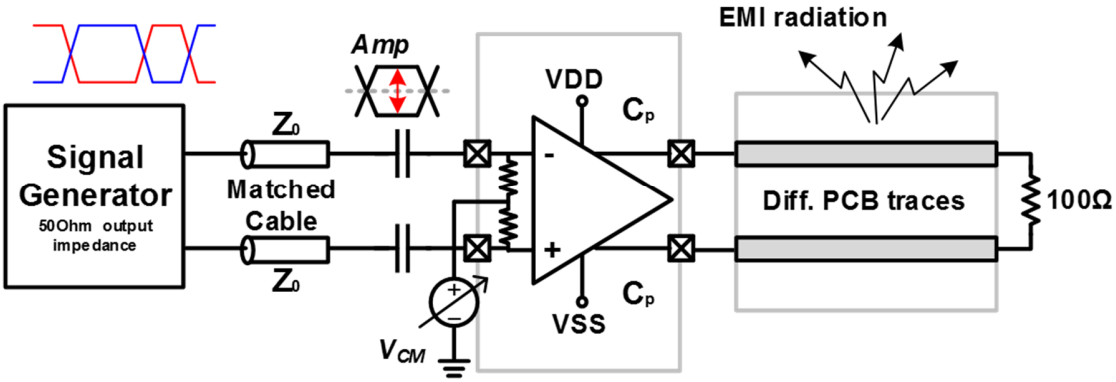


Fig. 3.26 System diagram of EMI testing

An EMI-related CM noise reduction method is proposed in previous section by reducing the signal swing and optimizing the input CM voltage. In order to justify the effectiveness of the optimization, an EMI radiation measurement of the test chip is conducted in this section, as depicted in Fig. 3.26.

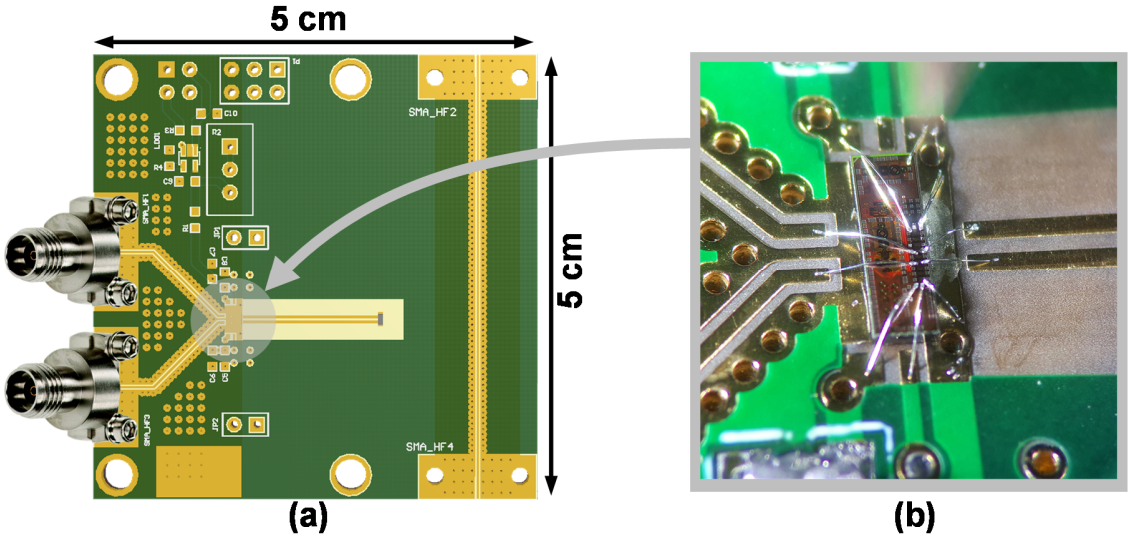


Fig. 3.27 EMI testing PCB

First, a PCB is designed to provide DC supply voltages and radiation structures for the test chip as shown in Fig. 3.27. On one hand, the test chip inputs are wire-bonded to the differential input coplanar waveguides (CPW), which is connected to the pattern generator through high-speed end

launch connectors. On the other hand, the test chip outputs are wire-bonded to differential microstrip traces to radiate the output CM noise. The differential microstrip traces are designed referring to the structure in Fig. 8, and a 100-Ω resistor is placed at the other end of these traces for differential termination. It is to be noted that according to electromagnetic simulations, the radiation of the input CPWs is weak, but the radiation of output microstrip traces are much stronger (28dB gain difference). Hence, most of the radiated EMI is from the outputs of the test chip.

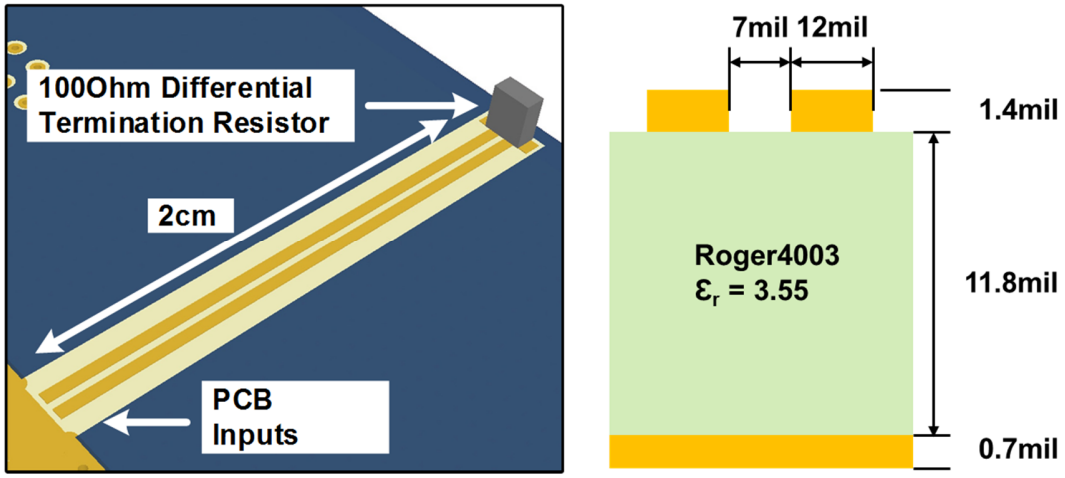


Fig. 3.28 Cross section view of output PCB traces

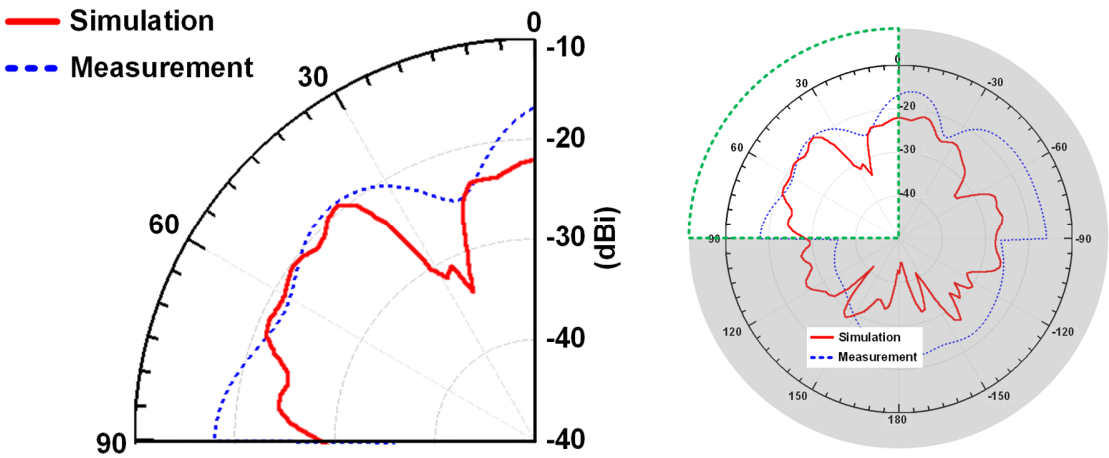


Fig. 3.29 The simulated and measured radiation pattern of testing PCB

Second, in order to get the maximum far-field 10 GHz radiation of the test chip, the 10 GHz radiation pattern of the PCB should be measured to provide the direction. By using 10 GHz CM signals to excite the PCB (without test chip), the radiation pattern is measured with a StarLab antenna measurement system. The PCB is placed horizontally in the x-y plane and the z-axis is perpendicular to the PCB surface. The measured 10-GHz gain pattern at $\varphi = 0°$ is shown in Fig. 3.29, where the maximum value appears at the direction of $\theta = 40°$.

Then, a measurement setup is built in the anechoic chamber to measure the EMI radiation of the test chip, as shown in Fig. 3.30. The whole PCB with the wire-bonded test chip is placed in the center of the chamber, a pattern generator generates 10 Gbps differential PRBS signals for the test chip and a polarized dual-ridge horn antenna (2 – 32 GHz bandwidth, 10.48 dB gain at 10 GHz) is used to collect the far-field EMI emission. For EMI measurement requirements, the antenna should be placed in a position in the far-field region where the EMI radiation is relatively large.

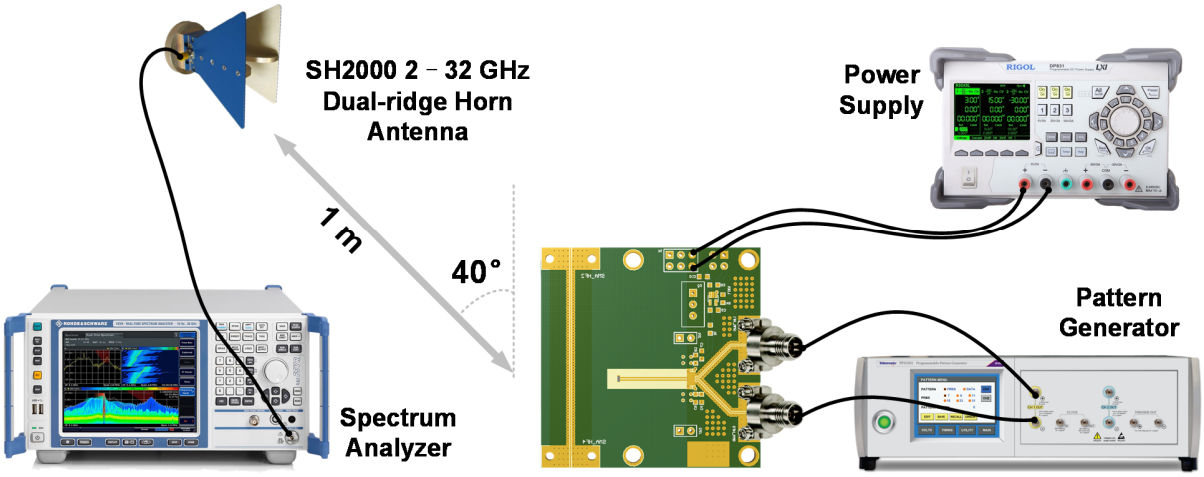


Fig. 3.30 EM radiation testing setup

For antennas shorter than half of the wavelength of the radiation they emit (i.e., "electromagnetically short" antennas), the far and near regional boundaries are measured in terms of a simple ratio of the distance r from the radiating source to the wavelength λ of the radiation.

For such an antenna, the near field is the region within a radius ($r \ll \lambda$), while the far-field is the region for which $r \gg 2\lambda$. The transition zone is the region between $r = \lambda$ and $r = 2\lambda$.

In this case, the wavelength of a 10 GHz radio wave is 3 cm and the antenna is physically larger than the half-wavelength of the 10 GHz radiation. Therefore, the far field is defined in terms of the Fraunhofer distance. The Fraunhofer distance, named after Joseph von Fraunhofer, is given by the following:

$$r \geq \frac{2d^2}{\lambda}, \tag{3.6}$$

where d is the largest dimension of the radiator (or the diameter of the antenna) and λ is the wavelength of the radio wave.

Obviously, in this case, the largest dimension of the dual ridge horn antenna is 105mm, and it is larger than the half wavelength of 10 GHz microwave. Thus, according to the calculated Fraunhofer distance of 0.7 m, the dual-ridge horn antenna is placed 1 meter away from the PCB to collect the radiated emissions in the measurement setup.

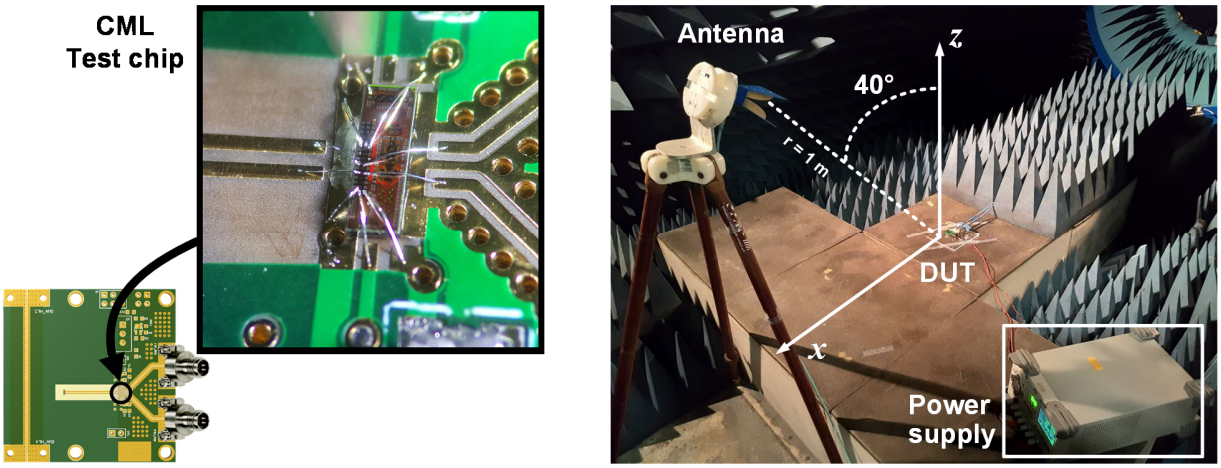


Fig. 3.31 (a) Photo of the test chip on PCB and (b) the EMI measurement site

Moreover, according to the measured radiation pattern in Fig. 3.29, the antenna is placed in the direction of $\theta = 40°$ and $\varphi = 0°$ to get the maximum EMI radiation. It is to be noted that the actual θ in the setup is slightly adjusted onsite to get the maximum received power. Fig. 3.31 shows the

photos of the wire-bonded test chip and the EMI measurement site in the anechoic chamber. Additionally, in order to consider the polarization effect of the receiving antenna, the measurement has been done twice with the antenna rotated 90° orthogonally to get the vertical and horizontal EMI radiations separately. The total received power is calculated by adding the measured vertical and horizontal power together.

Now, the strength of an electromagnetic wave can be expressed in terms of electric field strength E (measured in V/m), of magnetic field strength H (measured in A/m) or of power density S (measured in W/m^2).

$$S = E \times H = \frac{P_r}{A_e} \tag{3.7}$$

The characteristic impedance of free space, also called the Zo of free space, is an expression of the relationship between the electric-field and magnetic-field intensities in an electromagnetic field (EM field) propagating through a vacuum . The Z_0 of free space, like characteristic impedance in general, is expressed in ohm and is theoretically independent of wavelength. It is considered a physical constant. Mathematically, the Z_0 of free space is equal to the square root of the ratio of the permeability of free space (μ o) in henrys per meter (H/m) to the permittivity of free space (o) in farads per meter (F/m):

$$Z_0 = \sqrt{\frac{\mu_0}{\varepsilon_0}} \approx 120\,\pi \approx 377\,\Omega \tag{3.8}$$

And,

$$E = Z_0 \cdot H \tag{3.9}$$

Calculate the antenna effective aperture:

$$A_e = \frac{\lambda^2}{4\pi} \cdot G \tag{3.10}$$

The effective electric field strength:

$$S = \frac{E^2}{Z_0} = \frac{P_r}{A_e} \tag{3.11}$$

Thus,

$$E = \sqrt{Z_0 \cdot P_r \cdot \frac{4\pi}{\lambda^2 \cdot G}} \approx 68.8 \frac{c}{f} \sqrt{\frac{P_r}{G}} \tag{3.12}$$

In the equation, c is the speed of light, f is the frequency of received signal, P_r is the corresponding received power, and G is the gain of receiver antenna.

Similar to the measurement in the last section, the input signal swing is changed and the total received power at 10 GHz is recorded and plotted in Fig. 3.32(a). When the input signal swing increases, the measured EMI radiation power increases as well, because the EMI-related CM noise is positively correlated to the signal swing.

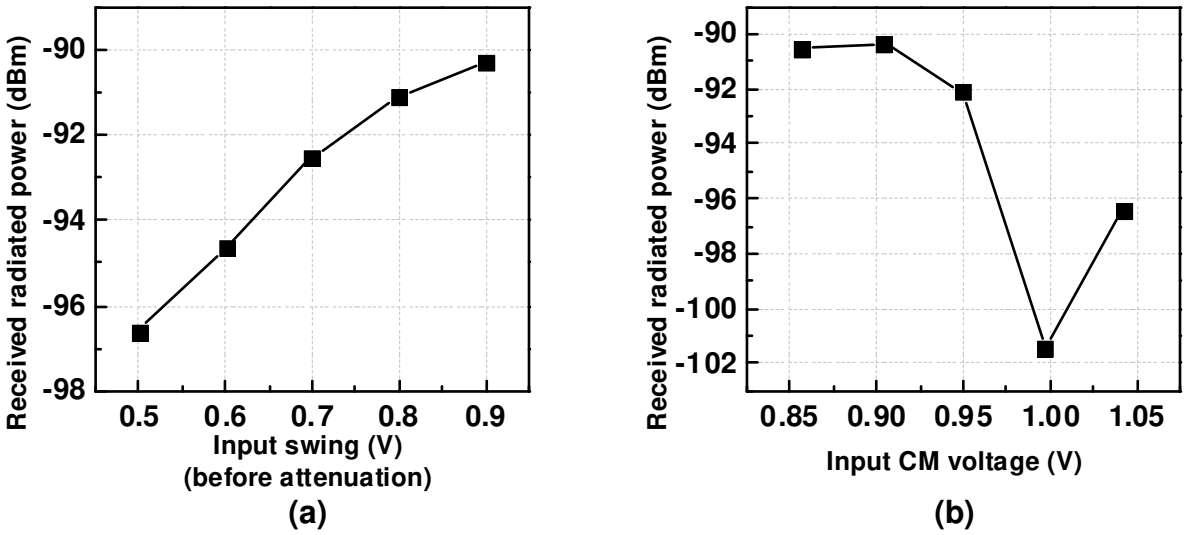


Fig. 3.32 (a) CM noise vs. input swing. (b) CM noise vs. input CM voltage.

Furthermore, similar to the electrical measurement in the last section, by changing the input CM voltage under a fixed 0.6 V input swing, the total radiated power is measured and shown in Fig. 3.32(b). As expected, the optimal input CM voltage leads to a significant reduction of the EMI

radiation by 11dB, due to a considerable reduction of the EMI-related CM noise. observations are consistent with the previous analysis.

In summary, in this chapter, we start from the system-level and walk down to the transistor-level inside the TX to investigate the EMI related circuit design methodology, in the perspective of EMC considerations for a typical high-speed wireline link. The fundamental mechanism for EMI problems in the SERDES communication link is discussed and verified. The analysis bridges the transistor-level IC designers and the system-level engineers with the solutions for the EMI issue. In the development of a high-speed wireline link, the EMI issue is typically addressed at the system-level with the costly shielding, filtering, and packaging techniques. However, with the analytic results and the optimization methodology, engineers are able to tackle the EMI issue, and improve the performance of the entire link, in the early design stage.

Chapter 4 Circuit Analysis of a PAM-4 SERDES Link

The tremendous growth of the data volume has driven the development of high-speed communication technologies to rapidly increase the data rate in the “big data” era. Powered by the huge market demanding of data center applications, communication infrastructures of 40/100 GbE are gradually being replaced by the next generation of 200/400 GbE communication systems, which makes the development of high-performance and high-speed wireline interconnection strategically significant and necessary.

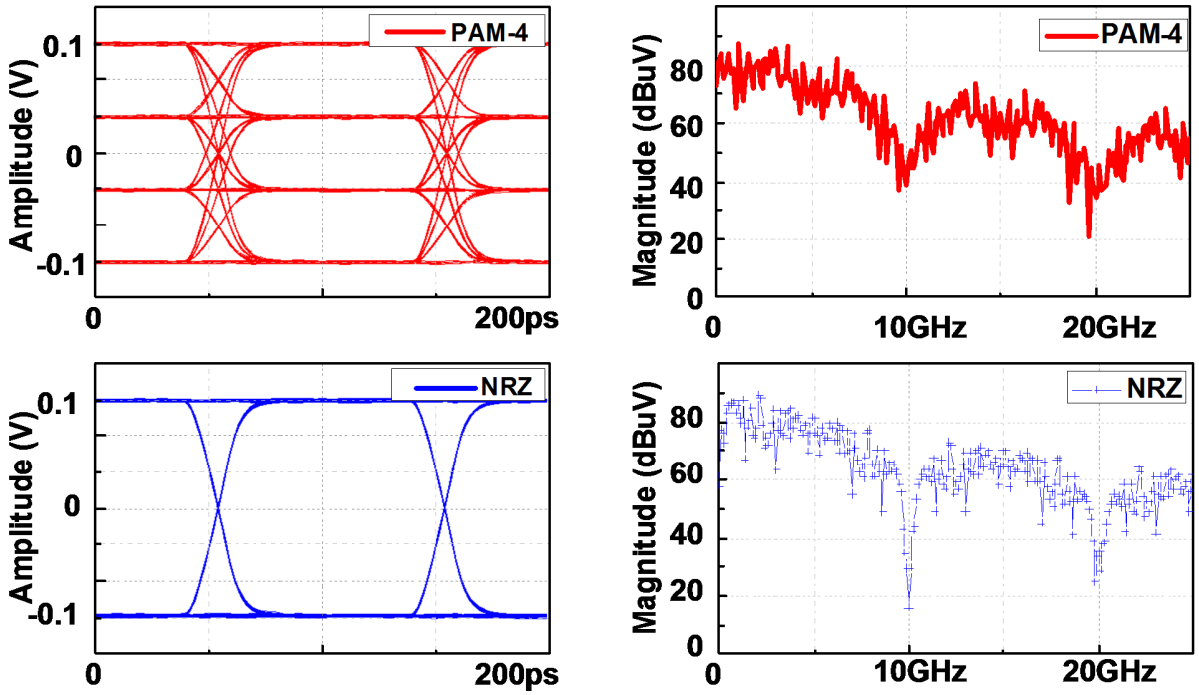


Fig. 4.1 Comparison of ideal eye-diagrams and corresponding spectrums of 20Gbps PAM-4 and 10Gbps NRZ signals.

For the next generation of 200/400 GbE communication, 4-level pulse amplitude modulation (PAM-4) signaling is one of the most promising key solutions [44] because of its high bandwidth efficiency. With the same bandwidth limitation, PAM-4 signaling can double the data rate, when compared to the widely adopted NRZ solutions, while maintaining the same Nyquist bandwidth,

as depicted in Fig. 4.1. The spectrums of each signal in the plots of both the 10 GBaud NRZ and 10 GBaud PAM-4 signals show the Nyquist frequency to be 5 GHz, but every PAM-4 symbol consists of 2 bits of information while NRZ signaling only contains 1 bit. Researchers from National Taiwan University reported high-speed backplane communication links based on PAM-4 signaling back in 2014 [45], [46]. Besides this, several applications on electrical to optical interface applications based on PAM-4 signaling have also been reported in recent years [47], [48].

Differential PAM-4 signals suffer from a similar EMI-related CM noise issue due to the non-linear signal distortions, as shown in Fig. 4.2. In the behavior level simulation, the rising and falling edges of the 10 GBaud NRZ and PAM-4 signals are intentionally set to be 25 ps and 10 ps, respectively. The mismatched rising and falling edges introduce the voltage spikes on the CM signal during each data transition period. In both the NRZ and PAM-4 cases, the CM spectrum exhibits a large noise tone at the double Nyquist frequency ($2f_{Nyquist}$ equals 10 GHz in 10 GBaud data link).

However, the PAM-4 signal is more complicated than the NRZ signal because it has four data levels, three data eyes, and twelve different data transitions. All these unique signaling features of PAM-4 signals eventually result in the different CM noise behaviors other than the CM noise behaviors of NRZ signaling discussed previous chapters. This chapter presents an analysis for the EMI-related CM noise in the high-speed wireline link, based on PAM-4 signaling, in the perspective of different signal distortions. Based on the analysis results, a PAM-4 signaling method based on thermometer encoding is analyzed. Both behavior-level and transistor-level simulations are performed to verify the proposed methodology. The thermometer encoding method is proved to suppress the CM noise while maintaining the same power consumption and communication speed.

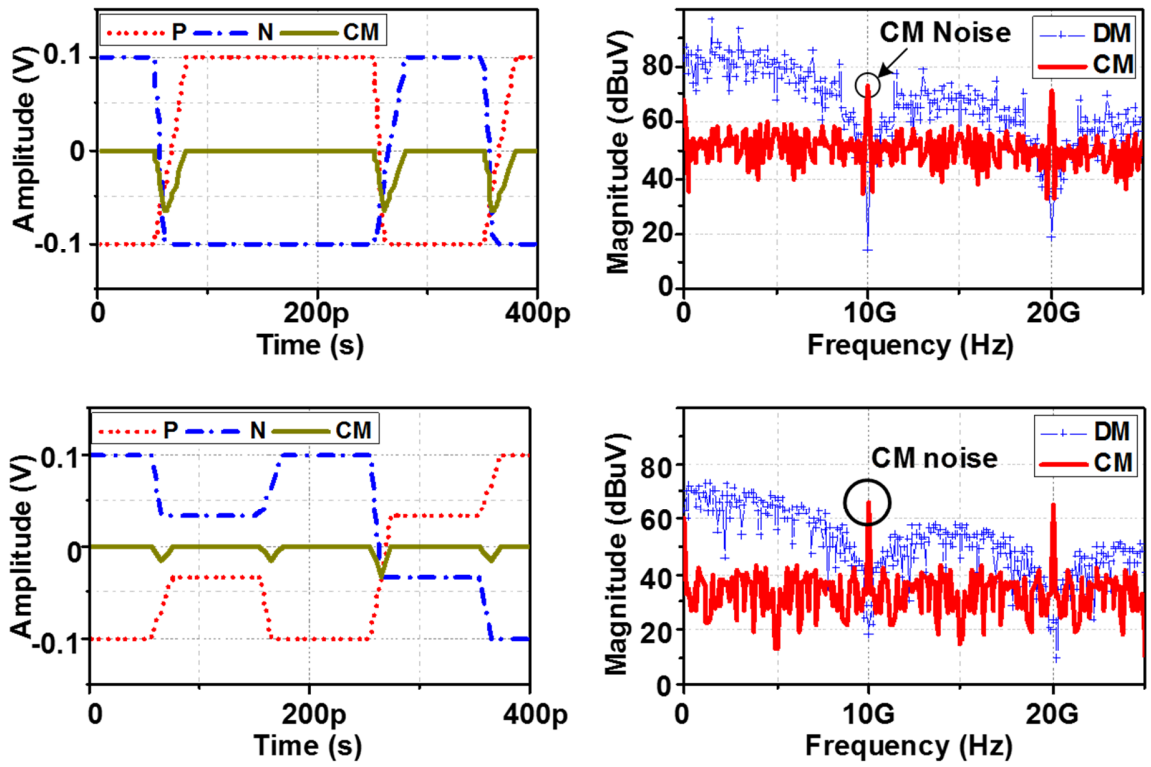


Fig. 4.2 Top: behavior-level simulated waveforms and corresponding spectrums for rising/falling edge mismatch in 10 Gbps NRZ signals; bottom: behavior simulation results of transient waveforms and corresponding spectrums for rising/falling edge mismatch in 20 Gbps PAM-4 signals.

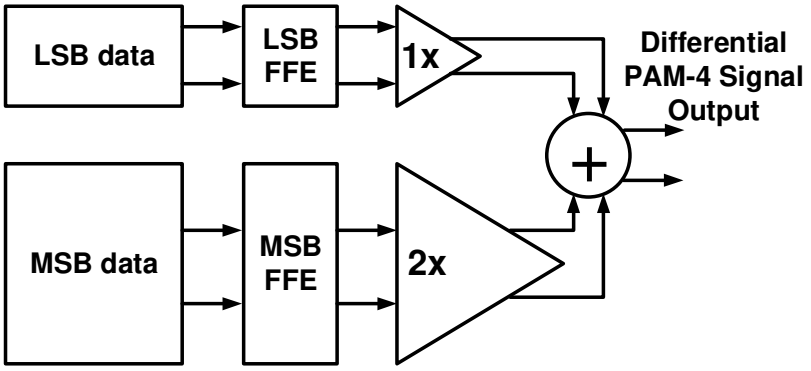
4.1 Briefing on System Architectures

The transmitter (TX) in the entire SERDES link acts as the CM noise source according to the analysis in previous chapters. Thus, before discussing the EMI-related CM noise in PAM-4 communication systems, a briefing on common PAM-4 TX architectures is conducted as follows.

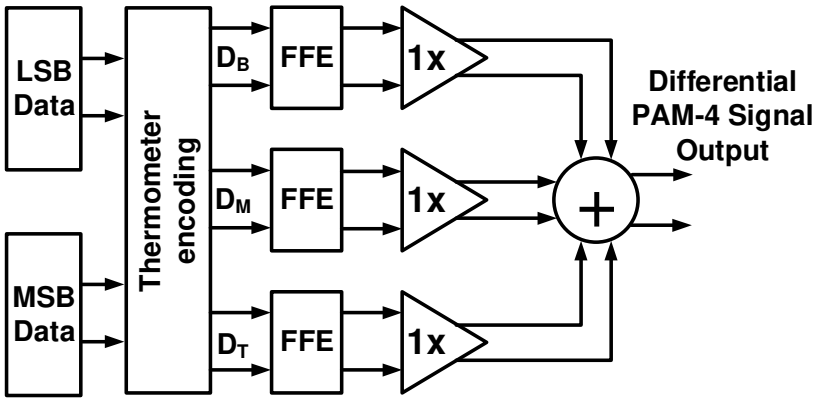
Fig. 4.3 illustrates two different architectures to generate PAM-4 signals, which are the binary-scaled topology and the thermometer-coded topology. In the binary-scaled topology, the baseband circuit provides two data streams for the most significant bit (MSB) and least significant bit (LSB) respectively. In the last driver stage, the MSB and LSB are combined through the binary-weighted circuit to generate PAM-4 signals [45], [49].

Table III Truth table: binary-scaled topology vs. thermometer-coded topology

MSB	LSB		D_B	D_M	D_T
0	0		0	0	0
0	1		1	0	0
1	0		1	1	0
1	1		1	1	1



(a)



(b)

Fig. 4.3 PAM-4 TX system architecture: (a) binary-scaled topology; and (b) thermometer-coded topology.

The other approach for PAM-4 signal generation is based on thermometer code, as described in Table III, where the MSB and LSB data are coded into the 3-bit thermometer code format. D_B stands for the bottom eye and it equals "MSB || LSB". D_M is the middle eye and it equals the MSB. D_T is the top eye and its value is "MSB && LSB". After the thermometer encoding, each symbol

is represented by the linear summation of D_B, D_M, and D_T, instead of the binary-weighted summation of MSB and LSB. The corresponding TX architecture is depicted in Fig. 4.3(b), where the 3 bits of coded data go through the cascaded feed-forward equalization (FFE) and finally are combined in the last driver stage [50]–[52]. This architecture is named thermometer-coded topology [52].

The last driver stage of TX directly contributes to the CM noise directly. Since the last stages of both binary-scaled topology and thermometer-coded topology are quite different in terms of data combination method, the PAM-4 data distortion in each topology also differ from each other. Fig. 4.4 illustrates the amplitude distortions and skew-introduced distortions in both binary-scaled and thermometer-coded topologies.

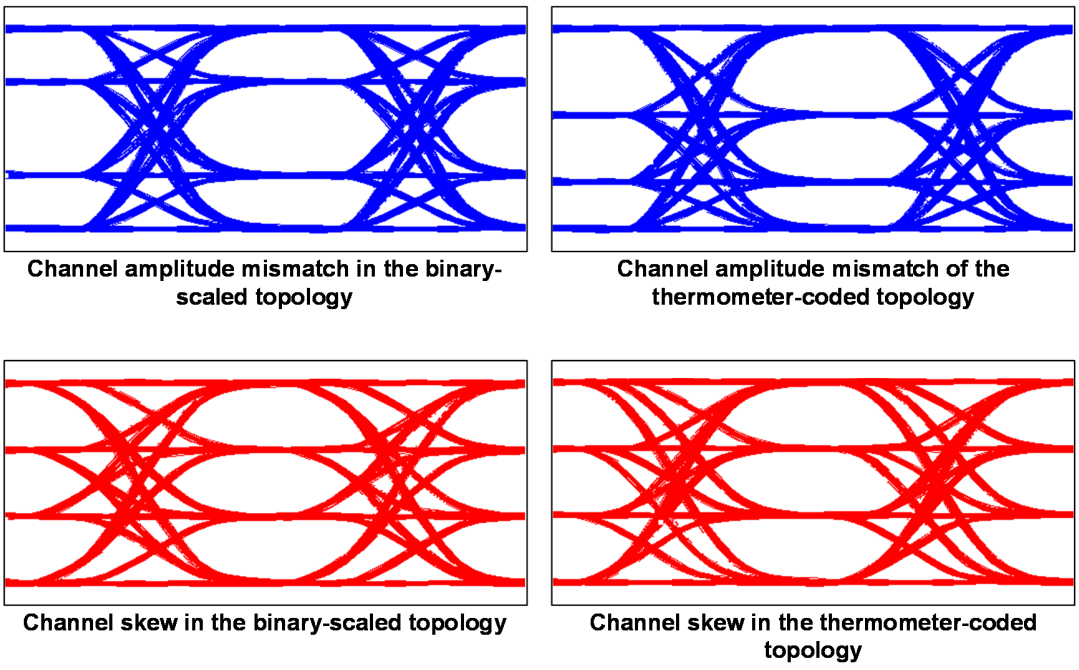


Fig. 4.4 Different types of distortions of differential PAM-4 signals

For the binary-scaled topology, the top and bottom data eyes are bonded, and they all have the same amplitude distortion and time skew, which is different from the middle data eye, as shown in the left two plots in Fig. 4.4. In the simulation, the amplitude ratio of MSB and LSB is

intentionally set to be 2.5:1, instead of the 2:1 in an ideal no distorted case, and the time skew between LSB and MSB is set to be the 1/10 of a unit interval (UI).

However, in the thermometer-coded topology, since the three data channels are independent, the amplitude distortions and the time skews for these three channels are also independent, as illustrated in the right-side plots in Fig. 4.4. In the simulation, the amplitude ratio between the top (D_T), middle (D_M) and bottom (D_B) data eyes is 1.3:1:0.7 and the time skews of three channels are 0.1 UI, 0.05 UI, and zero UI respectively.

4.2 Evaluation of PAM-4 Data Generation Methods

For all the simulations to evaluate the CM noise behaviors in PAM-4 signals, the author needs to provide the truly random data for a reasonable approximation for the high-speed physical-layer communication.

To provide random PAM-4 data, which consists of 2-bit of information per symbol, the MSB and LSB data streams can be obtained by using separated two pseudo-random bit sequence (PRBS) generators. As shown in Fig. 4.5(a), the MSB data is a PRBS with a length of 2^{15}-1, while the LSB data is a PRBS with a length of 2^7-1.

Another approach, which is called PRBSQ [53] and shown in Fig. 4.5(b), is to generate the random PAM-4 data with only one PRBS. The core generator generates a PRBS of a length 2^{13}-1 in this case. Then, the generated data is de-multiplexed into the MSB and LSB data streams. Intuitively, the combination of the two different PRBSs in the first approach is more irregular, complicated and unpredictable. While the PRBS13Q in the second approach seems more regular in terms of the data generation method. However, does the first irregular approach really beat the

second PRBS13Q method in terms of the randomness? In other words, which approach provides better data estimation to the practical physical-layer communication?

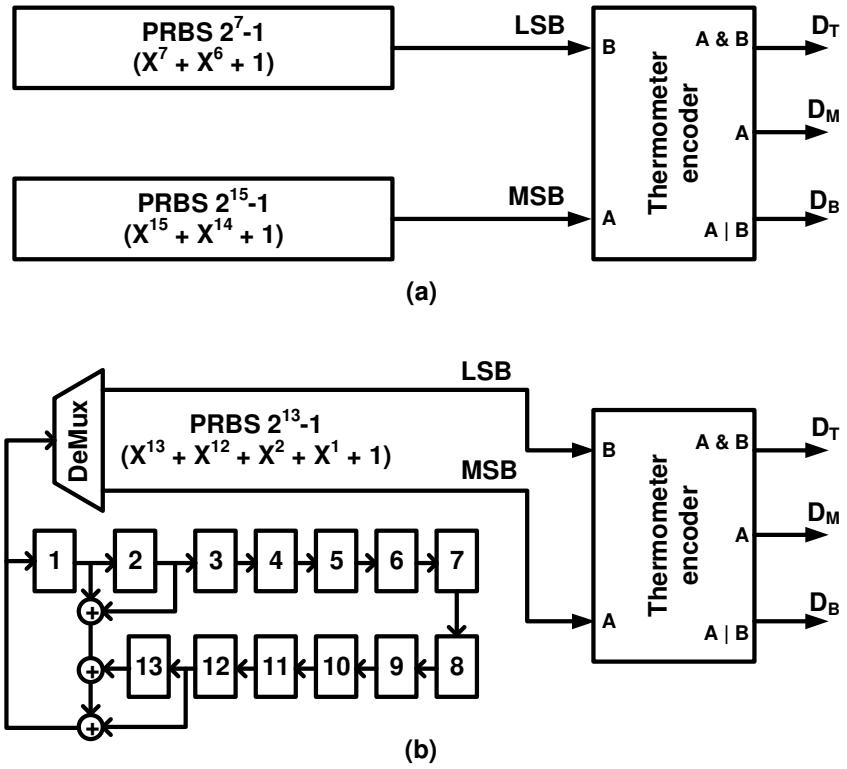


Fig. 4.5 PAM-4 signal generation: (a) a combination of two different PRBSs; (b) PRBS13Q

Before evaluating these two approaches, we would like to bring up the criteria for the comparison. The randomness of PAM-4 data means (1) all four data levels in the PAM-4 signal appears with the same probability of 25%, and (2) all 16 data transitions of the PAM-4 signals appear with the same possibilities of 1/16.

With the definition of randomness, simulation and comparisons are made as follows. The comparison is to simulate and count the statistics of 4 data levels and 16 data transitions with a given scale of the data set, which is 26,000 data symbols in this case.

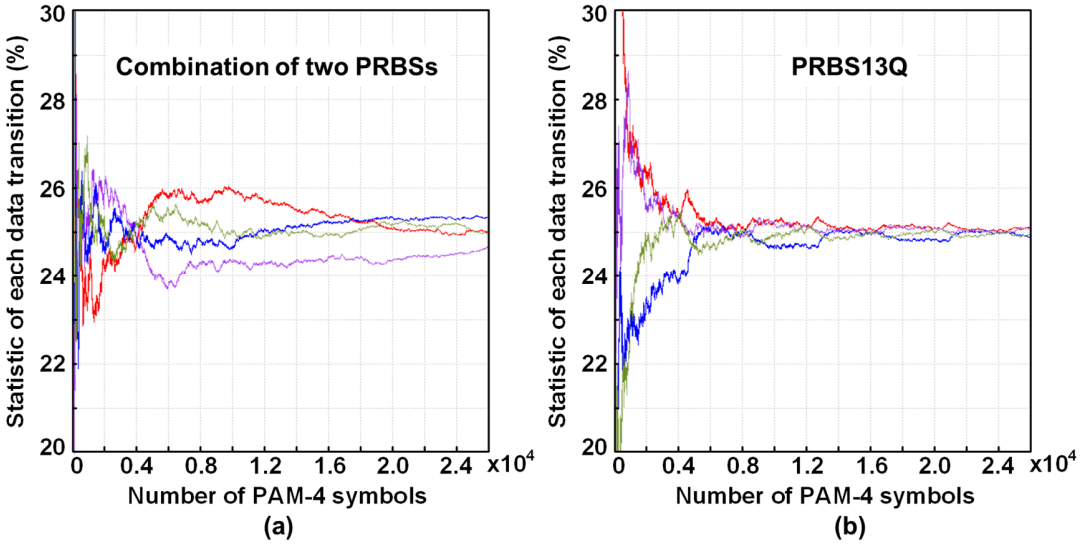


Fig. 4.6 Data level randomness

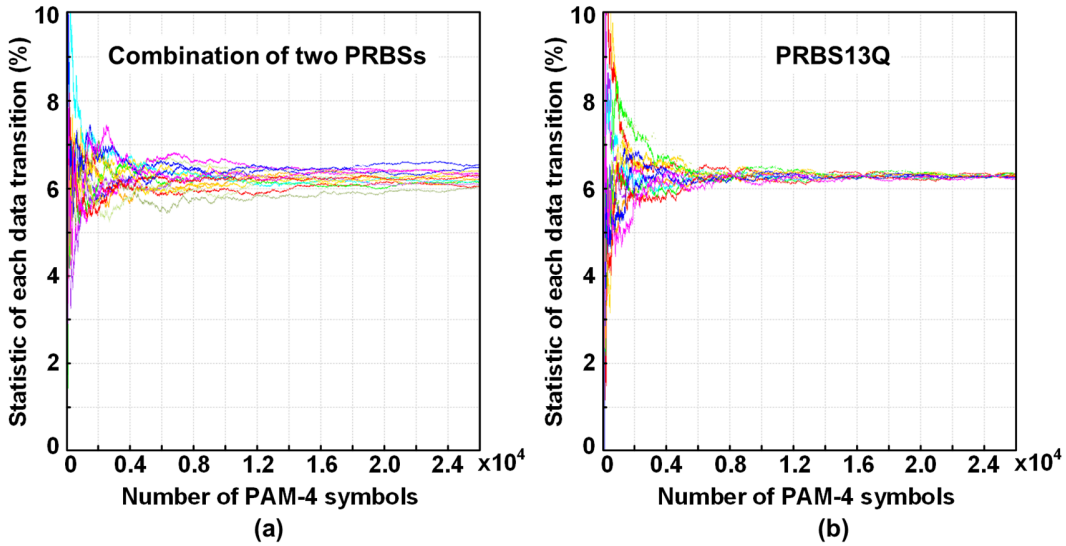


Fig. 4.7 Data transition randomness

As shown in Fig. 4.6, when the number of generated data samples gets larger, the probabilities of the occurrences of all four data levels converge towards 25% in both cases, but the PRBS13Q approach has obviously better and quicker convergence. In Fig. 4.7, the probability of the occurrence of each data transition gets closer to 1/16, along with the increasing number of the data samples; however, the PRBS13Q also has obviously better convergence.

In summary, the PRBS13Q approach is statistically more random in terms of the equal occurrences of data levels and data transitions. Thus, the PRBS13Q method will be used for all the following PAM-4 simulations and evaluations in the following parts of this chapter.

4.3 Amplitude Distortion Effects on CM Noise

This section discusses the CM noise behavior in both binary-scaled and thermometer-coded systems when the amplitude of each data eye is distorted.

In the binary-scaled topology as shown in Fig. 4.8(a), the amplitude distortion normally happens between the middle eye and top or bottom eyes, but the amplitudes of the top and bottom eyes are bonded. In Fig. 4.8, the middle-eye amplitude ratio (MEAR) is defined as the ratio of the middle eye amplitude over the total signal amplitude, as shown in (4.1). Ideally, it equals 1/3 when the amplitudes of the bottom, middle and top eyes are the same.

$$MEAR = \frac{Amp_{mid}}{Amp_{top} + Amp_{mid} + Amp_{bottom}}. \tag{4.1}$$

Before the further analysis, two assumptions have to be set in advance.

First, in the signaling-wise consideration, the top, middle, and bottom eyes are linearly added to form a PAM-4 signal, and the transition edges are also linearly added, e.g. $T_{rise}^{0,3}$ describes the rising edge from level-0 to level-3, and it can be decomposed into the summation of three rising edges of the bottom, middle and top eyes. All 16 rising and falling edges are decomposed and described from (4.2) to (4.8), as follows:

$$\begin{aligned} T_{rise}^{0,3} &= T_{rise}^{top} + T_{rise}^{mid} + T_{rise}^{bottom}, \\ T_{fall}^{3,0} &= T_{fall}^{top} + T_{fall}^{mid} + T_{fall}^{bottom}, \end{aligned} \tag{4.2}$$

$$T_{rise}^{0,2} = T_{rise}^{mid} + T_{rise}^{bottom} ,$$
$$T_{fall}^{2,0} = T_{fall}^{mid} + T_{fall}^{bottom} , \quad (4.3)$$

$$T_{rise}^{0,1} = T_{rise}^{bottom} ,$$
$$T_{fall}^{1,0} = T_{fall}^{bottom} , \quad (4.4)$$

$$T_{rise}^{1,3} = T_{rise}^{top} + T_{rise}^{mid} ,$$
$$T_{fall}^{3,1} = T_{fall}^{top} + T_{fall}^{mid} , \quad (4.5)$$

$$T_{rise}^{1,2} = T_{rise}^{mid} ,$$
$$T_{fall}^{2,1} = T_{fall}^{mid} , \quad (4.6)$$

$$T_{rise}^{2,3} = T_{rise}^{top} ,$$
$$T_{fall}^{3,2} = T_{fall}^{top} , \quad (4.7)$$

$$T_{fall}^{1,1} = T_{fall}^{2,2} = T_{fall}^{3,3} = T_{rise}^{1,1} = T_{rise}^{2,2} = T_{rise}^{3,3} = 0 . \quad (4.8)$$

Second, at the physical layer of Ethernet, fiber channel, and high-speed video applications, the encoded data streams can be estimated as random sequences. Thus, for a PAM-4 data stream, the statistics of the occurrence of all four data levels are equal, as well as the statistics of all 16 different data transitions, as mentioned in last section.

Therefore, according to the evaluation in last section, PRBS13Q approach is used to perform the analysis in this section due to its better randomness, when compared to the PAM-4 generation approach of combining two different PRBSs.

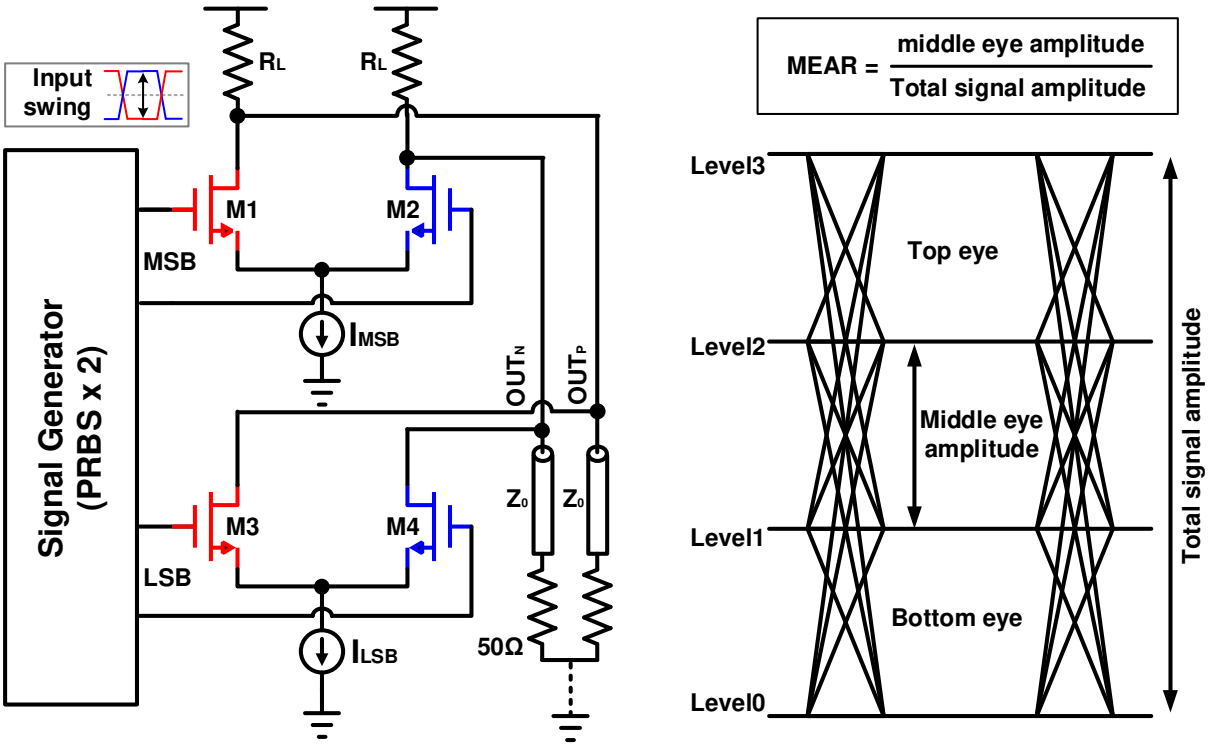


Fig. 4.8 (a) PAM-4 driver simulation setup; (b) simplified PAM-4 eye diagram.

Based on the two assumptions above, among all the 16 different data transitions, only 12 data transitions contains amplitude changes, as shown from (4.1) to (4.7). Among all these 12 data transitions, both the rising and falling edges of the middle data eye, appear 4 times out of 10, while the edges of the top and bottom eyes only appear 3 times out of 10.

Since each data edge introduces CM noise, the higher probability of the occurrence of the middle eye edge suggests that the mismatch of the rising and falling edges in the middle eye would contribute more to the final CM noise of the PAM-4 data stream, when compared to the top and bottom eyes. If there is any amplitude mismatch between the top and bottom eyes, the larger

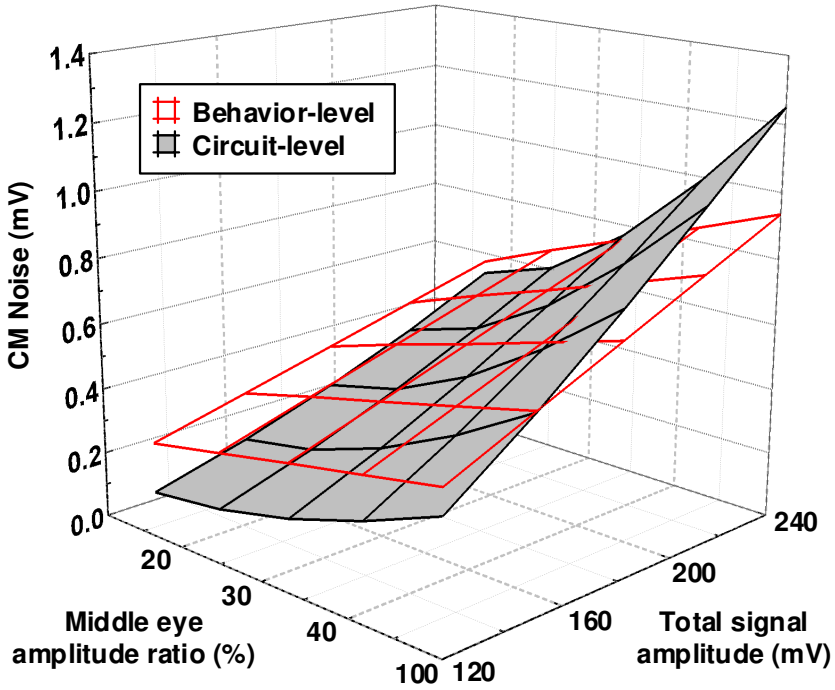


Fig. 4.9 Circuit-level simulated 3-D contour of CM noise for PAM-4 differential signals.

The signal amplitude was changed from 120 mV to 180 mV and the MEAR was swept from 16% to 50% in the behavior-level signals in Fig. 4.8(b), and the simulated behavior-level results are shown in Fig. 4.9. Meanwhile, a PAM-4 driver circuit in a 65 nm CMOS process, as shown in Fig. 4.8(a), is also simulated and the corresponding simulation results are also shown in Fig. 4.9.

In the circuit simulation setup in Fig. 4.8(a), the input data is generated by a Verilog-A-based PRBS13Q generator. The generated MSB and LSB data streams are fed into the subsequent MSB and LSB drivers, respectively. The size of M_1 and M_2 in the MSB driver is double the size of M_3 and M_4 in the LSB driver. Comparisons are concluded from the behavior-level and circuit-level simulations as below.

(a) Similar to the results of the previous analysis of NRZ signals, the CM noise in PAM-4 signals is positively correlated to the signal swing.

(b) With a given total signal swing, the CM noise increases with the increase of MEAR. This observation indicates that among the three data eyes, the unmatched rising and falling edges of the middle eye contribute more to the total CM noise of differential PAM-4 signals than the mismatched edges of the top and bottom data eyes.

(c) The circuit-level simulation result qualitatively matches the behavior-level prediction. The non-linearity effects in the transistors, as discussed in previous chapters, mainly cause the difference in these two simulations.

4.4 Non-ideal Data Transitions Effects on CM Noise

Besides the amplitude distortions discussed in the last section, the system architecture will also affect the CM noise behavior. Behavior-level simulations for both the binary-scaled topology and thermometer-coded topology are conducted and are discussed following.

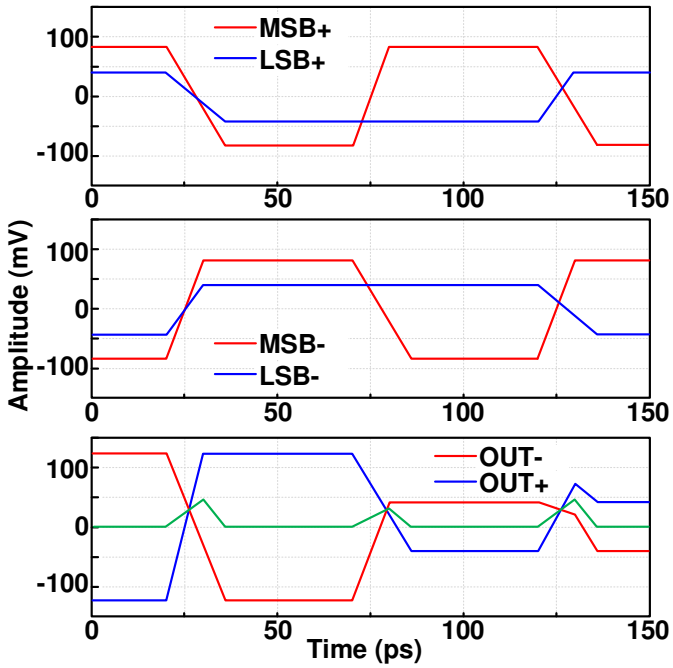


Fig. 4.10 Behavior-level transient waveforms in binary-scaled topology

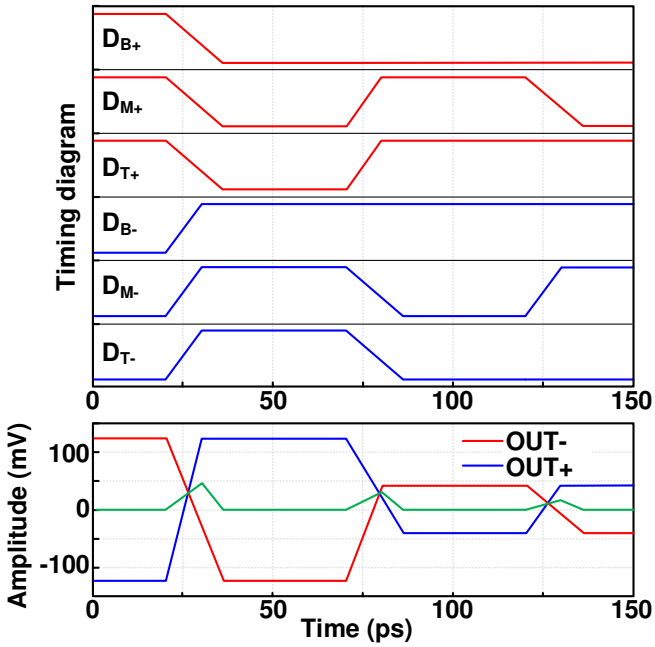


Fig. 4.11 Behavior-level transient waveforms in thermometer-coded topology

In Fig. 4.10, differential MSB and LSB signals are shown in the top and middle figures, while the combined PAM-4 signals are shown at the bottom. In the simulation, the rising and falling edge time are set to be 10 ps and 16 ps, respectively, and the amplitude of MSB is 80 mV, which is double the amplitude of LSB. Due to the asymmetrical rising and falling edges, CM noise spikes are introduced in each data transition period. Besides this, a significant waveform distortion appears together with a large CM noise spike at 120 ps during the data transition from level-1 to level-2. By comparing the CM noise at 120 ps of the data transition from level-1 to level-2, to the CM noise at 70 ps during the data transition from level-0 to level-2, much controversy is raised over the smaller amplitude change leading to an even larger CM noise spike. This observation seems to go against the conclusion drawn in the previous chapter, that a larger amplitude variation should lead to larger CM noise.

Before explaining the hidden reason, we would like to conduct similar behavior-level simulation on the thermometer-coded PAM-4 topology. Fig. 4.11 illustrates the simulated results,

where the rising and falling edges are set as 10 ps and 16 ps, respectively. The amplitude for the top, middle and bottom data streams (D_T, D_M, and D_B) are equal at 40 mV, which makes the total PAM-4 amplitude the same as the situation in Fig. 4.10. Instead of generating large CM noise or significant signal distortion at 120 ps, when the data is changing from level-1 to level-2, the thermometer-coded topology shows a better signal quality as well as smaller CM noise at that moment.

Based on the observation and comparison between Fig. 4.10 and Fig. 4.11, an intuitive and preliminary conclusion can be drawn that the thermometer-coded topology is inherently better than the binary-scaled topology in the perspective of signal quality and CM noise performance. However, is this superficial instinct correct?

4.4.I Introduction of Switching Distance in PAM Systems

Simulation results in Fig. 4.10 and Fig. 4.11 reveal the different behaviors between binary-scaled and thermometer-coded topologies. Since CM noise is intrinsically introduced by the mismatched rising and falling edges, the data edges can be represented in the format of CM and differential mode (DM) parts as described from (4.9) to (4.11), where T_{CM} represent the CM components in the differential falling and rising transitions and T_{DM} represents the DM part of the differential data transitions.

$$T_{fall} = T_{CM} - T_{DM} \ , \tag{4.9}$$

$$T_{rise} = T_{CM} + T_{DM} \ , \tag{4.10}$$

$$T_{CM} = (T_{rise} + T_{fall}) / 2 \ . \tag{4.11}$$

Based on the definition above, and assuming the data transitions are linearly proportional to the amplitude, the CM noise is then determined by the amount of T_{CM} in each data transition. Thus,

$T_{rise}^{1,2}$ and $T_{fall}^{2,1}$, the data transitions of level-1 to level-2 at the 120 ps position in Fig. 4.10, are redefined in (4.12) and (4.13):

$$T_{rise}^{1,2} = T_{rise}^{MSB} + T_{fall}^{LSB} = (T_{CM}^{MSB} + T_{DM}^{MSB}) + (T_{CM}^{LSB} - T_{DM}^{LSB}), \quad (4.12)$$

$$T_{fall}^{2,1} = T_{fall}^{MSB} + T_{rise}^{LSB} = (T_{CM}^{MSB} - T_{DM}^{MSB}) + (T_{CM}^{LSB} + T_{DM}^{LSB}). \quad (4.13)$$

According to above expressions, the CM component of the data transition from level-1 to level-2 can be calculated as (4.14)

$$T_{CM}^{1,2} = T_{CM}^{2,1} = (T_{rise}^{1,2} + T_{fall}^{2,1}) / 2 = T_{CM}^{MSB} + T_{CM}^{LSB}. \quad (4.14)$$

Similar calculations of the data transitions between level-0 and level-2, at the 70ps position in Fig. 4.10, can be obtained, as shown in (4.15), (4.16) and (4.17):

$$T_{rise}^{0,2} = T_{rise}^{MSB} = T_{CM}^{MSB} + T_{DM}^{MSB}, \quad (4.15)$$

$$T_{fall}^{2,0} = T_{fall}^{MSB} = T_{CM}^{MSB} - T_{DM}^{MSB}, \quad (4.16)$$

$$T_{CM}^{0,2} = T_{CM}^{2,0} = (T_{rise}^{0,2} + T_{fall}^{2,0}) / 2 = T_{CM}^{MSB}. \quad (4.17)$$

$T_{CM}^{0,2}$ in (4.17) is smaller than the $T_{CM}^{1,2}$ in (4.14), even though the signal amplitude gap between level-0 and level-2 is double the amplitude gap between level-1 and level-2.

The amplitude of time-domain CM noise spikes (Amp_{CM}) determines the final EMI-related CM noise (N_{CM}), as discussed in the chapter 2. However, Amp_{CM} is only positively correlated to the CM component (T_{CM}) of each data transition, instead of the total signal transition amplitude. Thus, the summarized derivation and correlations are written as

$$N_{CM} \propto Amp_{CM} \propto T_{CM}. \quad (4.18)$$

In order to explain the quantitative difference between the CM components during data transitions in both the binary-scaled and thermometer-coded topologies, a technical term of

switching distance (SD) of two binary data, A and B, is introduced for the following discussion, as defined by

$$SD(A,B) = \sum_k W_k \cdot (A[k] \oplus B[k]),$$
$$W_k = 2^{k-1}. \tag{4.19}$$

In the definition above, *A* and *B* are two binary strings, and the switching distance is the sum of $A[k] \oplus B[k]$, the exclusive or (*XOR*) between the k_{th} bit of *A* and *B*, multiplies the binary weight for the corresponding k_{th} bit. Basically, the weight of the k_{th} bit equals 2^{k-1}. For example, the switching distance of *"101"* and *"110"*, is calculated as following

$$SD(101,110) = 4 \cdot (1 \oplus 1) + 2 \cdot (0 \oplus 1) + 1 \cdot (1 \oplus 0) = 3.$$

The concept of switching distance is extended and applied to the data transitions in differential PAM-4 signals, as the formula in (4.20)

$$SD(S_x, S_y) = \sum_k A_k \cdot (S_x[k] \oplus S_y[k]). \tag{4.20}$$

In the definition above, S_x and S_y are two different data levels of the PAM-4 signal, and the switching distance of two data levels is the summation of $(S_x[k] \oplus S_y[k])$, the exclusive or (*XOR*) of the k_{th} bit of S_x and S_y, multiplies the signal amplitude for the k_{th} bit. For example, the switching distance of PAM-4 levels, *"10"* and *"01"*, is calculated as follows

$$SD(10,01) = A_{MSB} \cdot (1 \oplus 0) + A_{LSB} \cdot (1 \oplus 0) = A_{MSB} + A_{LSB}.$$

In an ideal binary-scaled topology, the amplitude of *MSB* (A_{MSB}) is the double the *LSB* amplitude (A_{LSB}), and it equals 2/3 of total PAM-4 signal amplitude (A_{total}). Thus the switching distance of symbol *"10"* and symbol *"01"* is further calculated as (4.21)

$$SD(10,01) = A_{MSB} + A_{LSB} = \frac{2}{3}A_{total} + \frac{1}{3}A_{total} = A_{total} \tag{4.21}$$

According to the definition in (4.20), all the switching distances of all the data transitions in a binary-scaled PAM-4 signal can be derived, as shown in Table IV. Results in the table clearly reveal the positive correlation between the CM component in each data transition, T_{CM} , and the switching distance, *SD*, as described in (4.22), where eventually, the CM noise and the switching distance are linearly associated together:

$$N_{CM} \propto Amp_{CM} \propto T_{CM} \propto SD \ . \tag{4.22}$$

In a typical SERDES communication link, each symbol (00, 01 10 and 11) in the transmitted PAM-4 data stream randomly occurs among each data period. Thus, the EMI-related CM noise is an average representation for the noise energy at the double Nyquist frequency ($2f_{Nyquist}$).

Table IV Switching distance for all 16 PAM-4 data transitions in the binary-scaled topology

SD: S_y / S_x	S_0 00	S_1 01	S_2 10	S_3 11
S_0 00	0	$\frac{1}{3}A_{total}$	$\frac{2}{3}A_{total}$	A_{total}
S_1 01	$\frac{1}{3}A_{total}$	0	A_{total}	$\frac{2}{3}A_{total}$
S_2 10	$\frac{2}{3}A_{total}$	A_{total}	0	$\frac{1}{3}A_{total}$
S_3 11	A_{total}	$\frac{2}{3}A_{total}$	$\frac{1}{3}A_{total}$	0

Instead of considering only a single data transition, as in the previous case of a NRZ-based link, statistical analysis for all the data transitions is scientifically appropriate to describe the data transition behavior in a PAM-4 communication link. As shown in (4.23), the statistical average of switching distance (SD^{B}_{PAM4}), of all 16 different data transitions in a binary-scaled system, is defined with the probability of the occurrence, *p*, and the switching distance, *SD*, of each data transition:

$$SD^{B}_{PAM\ 4} = \sum_{n=0}^{3}\sum_{m=0}^{3} p_{n,m} \cdot SD(S_n, S_m)\ . \tag{4.23}$$

For a random data stream, the probabilities of the occurrence of all 16 data transitions are equal to 1/16, meaning that each data transition occurs evenly and randomly. Thus, the final calculated result is (4.24), where A_{total} is the total PAM-4 signal amplitude.

$$SD^{B}_{PAM\ 4} = \frac{1}{16} \cdot \sum_{n=0}^{3}\sum_{m=0}^{3} SD(S_n, S_m) = \frac{1}{2} A_{total} \tag{4.24}$$

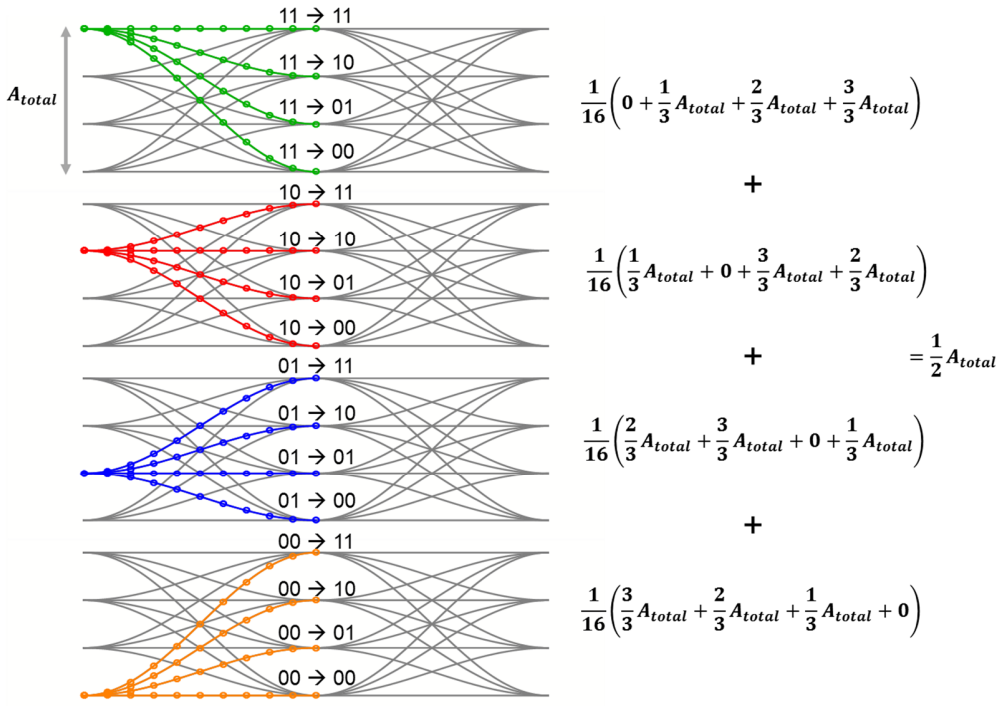


Fig. 4.12 Switching distance calculation in the binary-scaled PAM-4 signaling

Fig. 4.12 shows the calculation for the binary-scaled PAM-4 system. Based on the calculation of the statistically average switching distance, and the analysis of the T_{CM} of the data transitions, above, the PAM-4 CM noise in the binary-scaled topology is positively proportional to the average switching distance SD^{B}_{PAM4} and is then correlated to the signal amplitude, as shown in (4.25).

$$N_{CM}^{B} \propto Amp_{CM} \propto T_{CM}^{B} \propto SD_{PAM\,4}^{B} \propto \frac{1}{2} A_{total} \tag{4.25}$$

Similar calculation and analysis are applied to the thermometer-coded topology, and the derivation procedure is shown in the following section. In the calculation, the total signal amplitude is A_{total}, which is same as the amplitude in the previous binary-scaled topology. (4.26) shows the formula of the switching distance in the thermometer-coded topology. Instead of using the amplitudes of MSB and LSB in the previous binary-scaled case, A_0, A_1, and A_2 are used as the amplitude of the top, middle, and bottom eyes, respectively. All three values are equal to one-third of the total amplitude.

$$SD(S_x, S_y) = \sum_k A_k \cdot (S_x[k] \oplus S_y[k]),$$
$$A_0 = A_1 = A_2 = \frac{1}{3} A_{total}. \tag{4.26}$$

Table V Switching distance for all 16 PAM-4 data transitions in the thermometer-coded topology

SD (S_y / S_x)	S_0 000	S_1 001	S_2 011	S_3 111
S_0 000	0	$\frac{1}{3}A_{total}$	$\frac{2}{3}A_{total}$	A_{total}
S_1 001	$\frac{1}{3}A_{total}$	0	$\frac{1}{3}A_{total}$	$\frac{2}{3}A_{total}$
S_2 011	$\frac{2}{3}A_{total}$	$\frac{1}{3}A_{total}$	0	$\frac{1}{3}A_{total}$
S_3 111	A_{total}	$\frac{2}{3}A_{total}$	$\frac{1}{3}A_{total}$	0

Fig. 4.13 and Table V show the calculation procedure and the calculated switching distances for all 16 data transitions in the thermometer-coded topology.

The only two different numbers, when compared with the corresponding results in Table IV, are highlighted in the table, which are the switching distances of the data transitions between level-1 and level-2.

In the data transitions from level-1 to level-2, both MSB and LSB are switching simultaneously in the binary-scaled topology, while in the thermometer-coded topology, only the middle data, D_M in Fig. 4.11, is switching. Thus, the average switching distance in the thermometer-coded case is smaller than the average switching distance in the binary-scaled system.

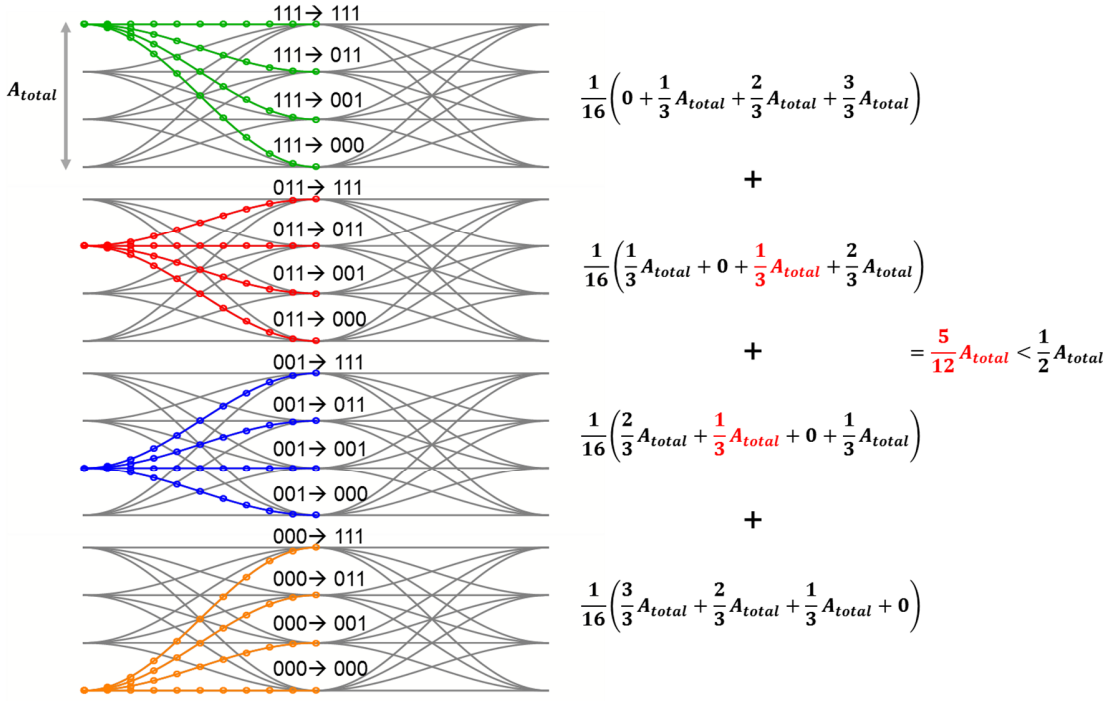


Fig. 4.13 Switching distance calculation in the thermometer-coded PAM-4 signaling

With the results in Table V and (4.23), the statistical average of the switching distance in the thermometer-coded topology is derived as follows:

$$SD^{T}_{PAM\ 4} = \sum_{n=0}^{3}\sum_{m=0}^{3} p_{n,m} \cdot SD(S_n, S_m) = \frac{5}{12} A_{total} \ . \tag{4.27}$$

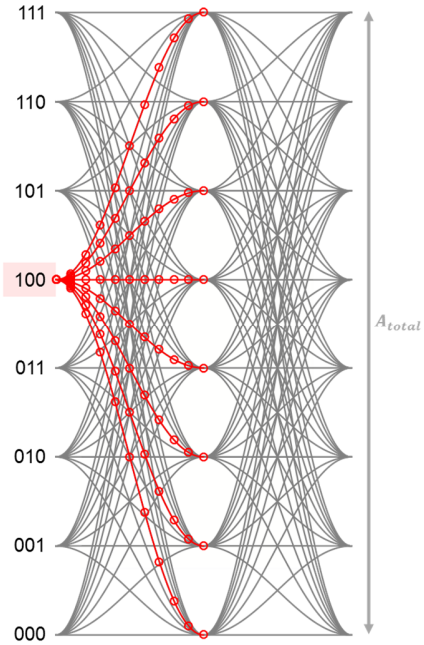
Thus, the CM noise in the ideal thermometer-coded topology is also proportional to the amplitude, but with a different coefficient, as shown below:

$$N_{CM}^{T} \propto T_{CM}^{T} \propto SD_{PAM\,4}^{T} \propto \frac{5}{12} A_{total} \,. \tag{4.28}$$

By comparing the results in (4.25) and (4.28), the CM noise of a thermometer-coded system is intrinsically 17% smaller than the CM noise of a binary-scaled system, when the total PAM-4 signal amplitudes of both systems are equal.

Even though 8-level pulse amplitude modulation (PAM-8) and 16-level pulse amplitude modulation (PAM-16) still sound impossible for high-speed wireline communication, due to the trade-off between the signal noise margin and the channel bandwidth, all the mathematic derivations and analyze on the PAM-4 signals are extendable and applicable to both PAM-8 and PAM-16 systems. The calculation procedures for binary-scaled PAM-8 system and thermometer-coded PAM-8 system are depicted in Fig. 4.14 and Fig. 4.15, respectively, and the calculated results for PAM-8 signals are summarized in Table VI.

Due to the complexity of illustrating the calculation procedure for PAM-16 signals, only the calculated results are summarized in Table VI.



	111	110	101	100	011	010	001	000
111	0	$\frac{1}{7}$	$\frac{2}{7}$	$\frac{3}{7}$	$\frac{4}{7}$	$\frac{5}{7}$	$\frac{6}{7}$	$\frac{7}{7}$
110	$\frac{1}{7}$	0	$\frac{3}{7}$	$\frac{2}{7}$	$\frac{5}{7}$	$\frac{4}{7}$	$\frac{7}{7}$	$\frac{6}{7}$
101	$\frac{2}{7}$	$\frac{3}{7}$	0	$\frac{1}{7}$	$\frac{6}{7}$	$\frac{7}{7}$	$\frac{4}{7}$	$\frac{5}{7}$
100	$\frac{3}{7}$	$\frac{2}{7}$	$\frac{1}{7}$	0	$\frac{7}{7}$	$\frac{6}{7}$	$\frac{5}{7}$	$\frac{4}{7}$
011	$\frac{4}{7}$	$\frac{5}{7}$	$\frac{6}{7}$	$\frac{7}{7}$	0	$\frac{1}{7}$	$\frac{2}{7}$	$\frac{3}{7}$
010	$\frac{5}{7}$	$\frac{4}{7}$	$\frac{7}{7}$	$\frac{6}{7}$	$\frac{1}{7}$	0	$\frac{3}{7}$	$\frac{2}{7}$
001	$\frac{6}{7}$	$\frac{7}{7}$	$\frac{4}{7}$	$\frac{5}{7}$	$\frac{2}{7}$	$\frac{3}{7}$	0	$\frac{1}{7}$
000	$\frac{7}{7}$	$\frac{6}{7}$	$\frac{5}{7}$	$\frac{4}{7}$	$\frac{3}{7}$	$\frac{2}{7}$	$\frac{1}{7}$	0

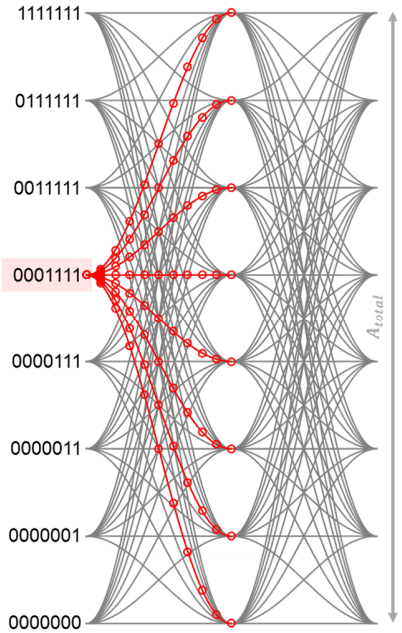
$$SD = \sum_{n=0}^{7}\sum_{m=0}^{7} p_{n,m} \cdot SD(S_n, S_m) = \frac{1}{64}\sum_{n=0}^{7}\sum_{m=0}^{7} \frac{m}{7} A_{total} = \frac{1}{2} A_{total}$$

Fig. 4.14 Switching distance calculation in the binary-scaled PAM-8 signaling

The generic calculation method of the switching distance in all thermometer-coded 2^k-level pulse amplitude modulation (PAM-2^k) signals is (4.29):

$$SD^{T}_{PAM-2^k} = \sum_{n=0}^{2^k-1}\sum_{m=0}^{2^k-1} p_{n,m} \cdot SD(S_n, S_m) = \frac{1}{2^{2k}}\sum_{n=0}^{2^k-1}\left(\sum_{x=0}^{n} \frac{x}{2^k-1} + \sum_{y=n}^{2^k-1} \frac{y-n}{2^k-1}\right) A_{total} \quad . \qquad (4.29)$$

It is to be noted that there is assumed no amplitude distortion, and each data eye in the PAM-2^k signal has same opening amplitude in the calculation above. Similar as previous cases, A_{total} is the total signal amplitude of the PAM-2^k signal.



	1111111	0111111	0011111	0001111	0000111	0000011	0000001	0000000
1111111	0	$\frac{1}{7}$	$\frac{2}{7}$	$\frac{3}{7}$	$\frac{4}{7}$	$\frac{5}{7}$	$\frac{6}{7}$	$\frac{7}{7}$
0111111	$\frac{1}{7}$	0	$\frac{1}{7}$	$\frac{2}{7}$	$\frac{3}{7}$	$\frac{4}{7}$	$\frac{5}{7}$	$\frac{6}{7}$
0011111	$\frac{1}{7}$	$\frac{2}{7}$	0	$\frac{1}{7}$	$\frac{2}{7}$	$\frac{3}{7}$	$\frac{4}{7}$	$\frac{5}{7}$
0001111	$\frac{1}{7}$	$\frac{2}{7}$	$\frac{3}{7}$	0	$\frac{1}{7}$	$\frac{2}{7}$	$\frac{3}{7}$	$\frac{4}{7}$
0000111	$\frac{1}{7}$	$\frac{2}{7}$	$\frac{3}{7}$	$\frac{4}{7}$	0	$\frac{1}{7}$	$\frac{2}{7}$	$\frac{3}{7}$
0000011	$\frac{1}{7}$	$\frac{2}{7}$	$\frac{3}{7}$	$\frac{4}{7}$	$\frac{5}{7}$	0	$\frac{1}{7}$	$\frac{2}{7}$
0000001	$\frac{1}{7}$	$\frac{2}{7}$	$\frac{3}{7}$	$\frac{4}{7}$	$\frac{5}{7}$	$\frac{6}{7}$	0	$\frac{1}{7}$
0000000	$\frac{1}{7}$	$\frac{2}{7}$	$\frac{3}{7}$	$\frac{4}{7}$	$\frac{5}{7}$	$\frac{6}{7}$	$\frac{7}{7}$	0

$$SD = \sum_{n=0}^{7}\sum_{m=0}^{7} p_{n,m} \cdot SD(S_n, S_m) = \frac{1}{64}\sum_{k=0}^{7}\left(\sum_{x=0}^{k}\frac{x}{7}A_{total} + \sum_{y=k}^{7}\frac{y-k}{7}A_{total}\right) = \frac{3}{8}A_{total}$$

Fig. 4.15 Switching distance calculation in the thermometer-coded PAM-8 signaling

Table VI summarizes the calculation results for all the PAM-4/8/16 binary-scaled and thermometer-coded signals. Because in the previous calculation in Chapter 2 the higher baud rate directly increases the CM noise power, the baud rates of three modulation schemes are kept as 10 GBaud for all the calculations to perform a fair comparison at the same Nyquist frequency (5 GHz). Furthermore, for all calculations, the total signal amplitude, which is also positively correlated to the signal CM noise, remains the same as A_{total}.

Based on the observations and comparisons in Table VI, the following conclusions are drawn.

(a) When the data baud rate is fixed, e.g. 10 GBaud, the binary-scaled systems with PAM-4, PAM-8, and PAM-16 signaling have exactly the same average switching distance. Thus, they also have same CM noise performance.

(b) Within a certain modulation scheme, e.g. PAM-4, because the switching distance of the thermometer-coded topology is theoretically smaller than the switching distance of the binary-scaled topology, the thermometer-coded topology intrinsically performs better in terms of CM noise reduction.

Table VI Calculation results summary of PAM-4/8/16 systems

	PAM-4		PAM-8		PAM-16	
Topology	**BS***	**TC#**	**BS**	**TC**	**BS**	**TC**
Baud rate (GB)	10	10	10	10	10	10
Data rate (Gbps)	20	20	30	30	40	40
Double Nyquist frequency (GHz)	10	10	10	10	10	10
Total Signal Amplitude	A_{total}	A_{total}	A_{total}	A_{total}	A_{total}	A_{total}
Average SD	$\frac{1}{2}A_{total}$	$\frac{5}{12}A_{total}$	$\frac{1}{2}A_{total}$	$\frac{3}{8}A_{total}$	$\frac{1}{2}A_{total}$	$\frac{17}{48}A_{total}$
Normalized CM Noise	1	0.83	1	0.75	1	0.71

* BS stands for binary-scaled

TC stands for thermometer-coded

In order to further verify the calculated results and conclusions in Table VI, behavior-level and transistor-level simulations are both conducted. Because PAM-16 signaling is nearly impossible to implement at the transistor-level in the near future for high-speed wireline communication applications, it is excluded from the following simulation, and only the binary-scaled and thermometer-scaled systems with PAM-4 and PAM-8 signaling are verified with both behavior-level and transistor-level simulations.

4.4.II Behavior-Level Simulation and Verification

The general simulation setup is depicted in Fig. 4.16. In the setup, the incoming data is generated by a Verilog-A-based generator, which has a 50-Ω output impedance and a finite output bandwidth of 30 GHz. The generation of the random data is based on the PRBS13Q method to

guarantee the data randomness, which has been discussed in section 4.2 . To combine the incoming data into the PAM-4 or PAM-8 format, an output driver circuit is either implemented with idea components or is built with the transistors in a 65 nm CMOS process. The output driver circuits are loaded with a differential 100-Ω resistor.

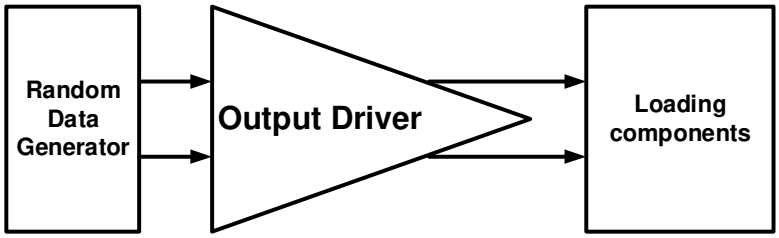
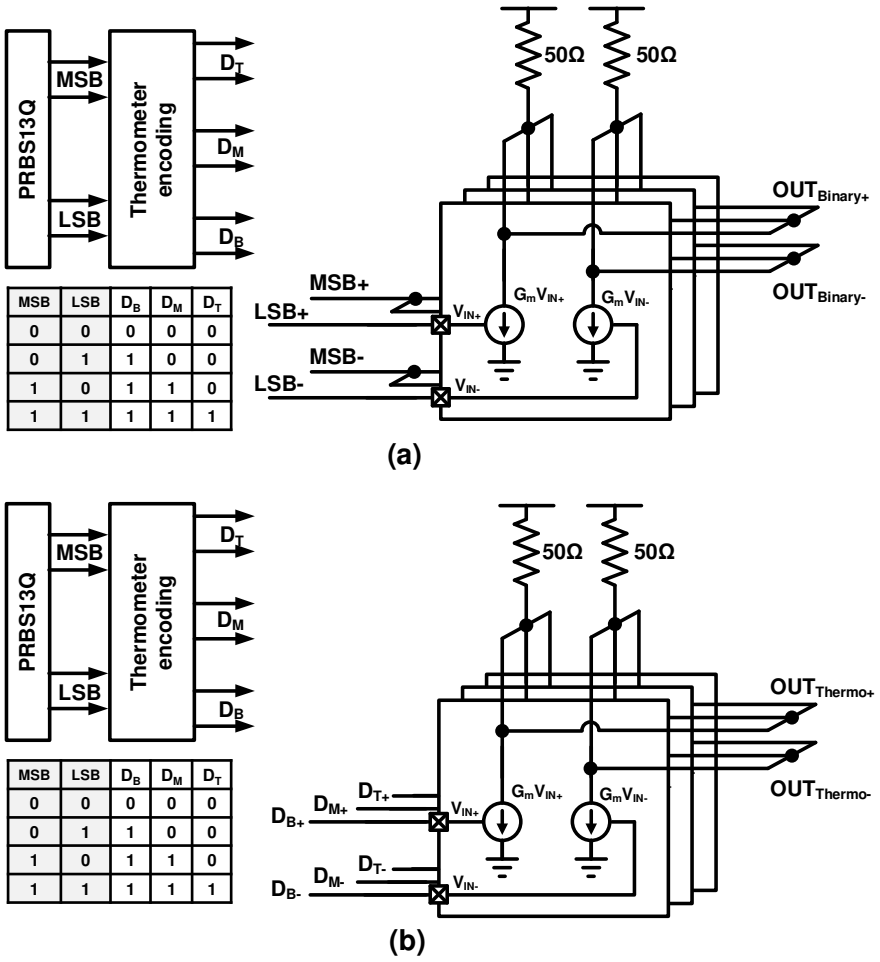


Fig. 4.16 Simulation setup, including data generation, output driver, and loading components

Fig. 4.17 shows the behavior-level simulation setups for both binary-scaled and thermometer-coded PAM-4 topologies. The baseband random data is generated and de-multiplexed into MSB and LSB data sequences. In the thermometer-coded system in Fig. 4.17(b), the MSB and LSB data are further converted into 3-bit thermometer code – D_T, D_M, and D_B.

The output driver stage, which consists of the ideal differential G_m cells and a pair of 50-Ω pull-up resistors, converts the incoming data into current and combines them on the 50-Ω loading resistors. The total driver is segmented into three parallel stages with identical structures. The only difference between the binary-scaled and thermometer-coded systems is the configuration of these three output-driver segments. In the binary-scaled system simulation, two of the segments are parallel-connected to form the MSB driver while the rest one segment is for LSB use; while, in the thermometer-coded system, three driver segments are individually used for D_T, D_M, and D_B. To intentionally generate CM noise, the rising and falling edges are set to be 11 ps and 10 ps, respectively, and the total signal amplitude is 252 mV.



MSB	LSB	D_B	D_M	D_T
0	0	0	0	0
0	1	1	0	0
1	0	1	1	0
1	1	1	1	1

Fig. 4.17 Behavior-level simulation setup for PAM-4. (a) Binary-scaled topology; (b) thermometer-coded topology.

By slightly modifying the simulation setup in Fig. 4.17, a similar simulation setup can be used to evaluate the binary-scaled and thermometer-coded PAM-8 systems as well. The behavior-level simulation results are summarized in Table VII. When compared with the results in Table VI, the behavior-level simulations show general consistency with the mathematical calculation and analysis in previous sections.

Table VII Behavior-level simulation results of PAM-4/8 systems

	PAM-4		**PAM-8**	
Topology	**BS***	**TC#**	**BS**	**TC**

Baud rate (GB)	10	10	10	10
Data rate (Gbps)	20	20	30	30
Double Nyquist frequency (GHz)	10	10	10	10
Simulation time (nS)	800	800	800	800
Total amplitude (mV)	252	252	252	252
Rising/falling edge (ps)	11/10	11/10	11/10	11/10
Simulated CM noise @ 20GHz (mV)	2.41	1.99	2.41	1.81
Normalized CM noise	1	0.826	1	0.751

* BS stands for binary-scaled

TC stands for thermometer-coded

4.4.III Transistor-Level Simulation and Verification

In the last section, the behavior-level simulation results quantitatively match the previous calculations in section 4.4.I . In order to verify the conclusions at the transistor level, a TSMC 65nm CMOS process is used to build an output driver circuit, as shown in Fig. 4.16.

In the simulation setup, the incoming data is generated by a Verilog-A-based generator, with a PRBS13Q structure shown in Fig. 4.5(b). The generated MSB and LSB data streams are further encoded to the 3-bit thermometer code for the thermometer-coded system simulation as shown in Fig. 4.19. Each output port of the generator has a 50Ohm output impedance and finite output bandwidth of 30GHz.

Fig. 4.18 illustrates the simulation setup for a binary-scaled PAM-4 driver. The CML-based driver consists of MSB and LSB sub-drivers with a shared pair of 50-Ω resistors. The size of the MSB driver is twice the size of the LSB driver, and the biasing current (I_{tail}) is also distributed with the ratio of 2:1 according to the driver size. The loading of the driver consists of a pair of

transmission lines (based on measured data of PCB traces) cascaded with two differentially terminated 50-Ω resistors.

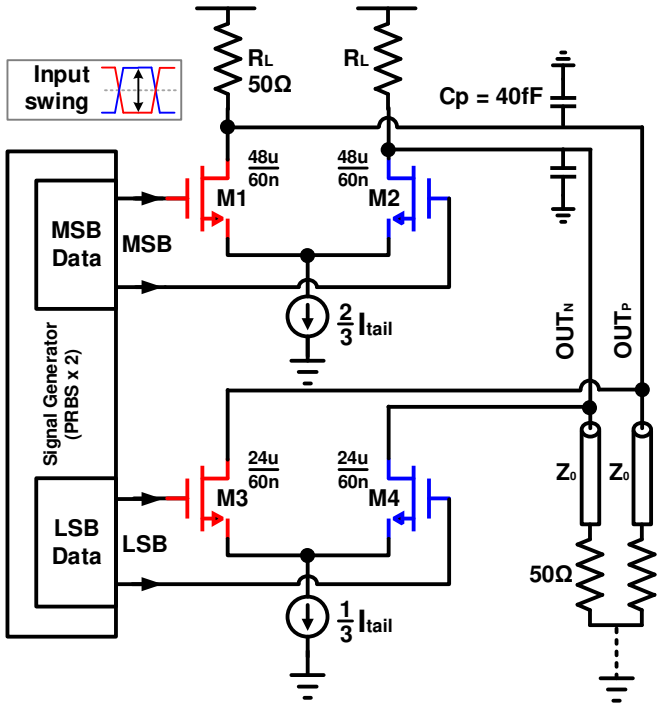
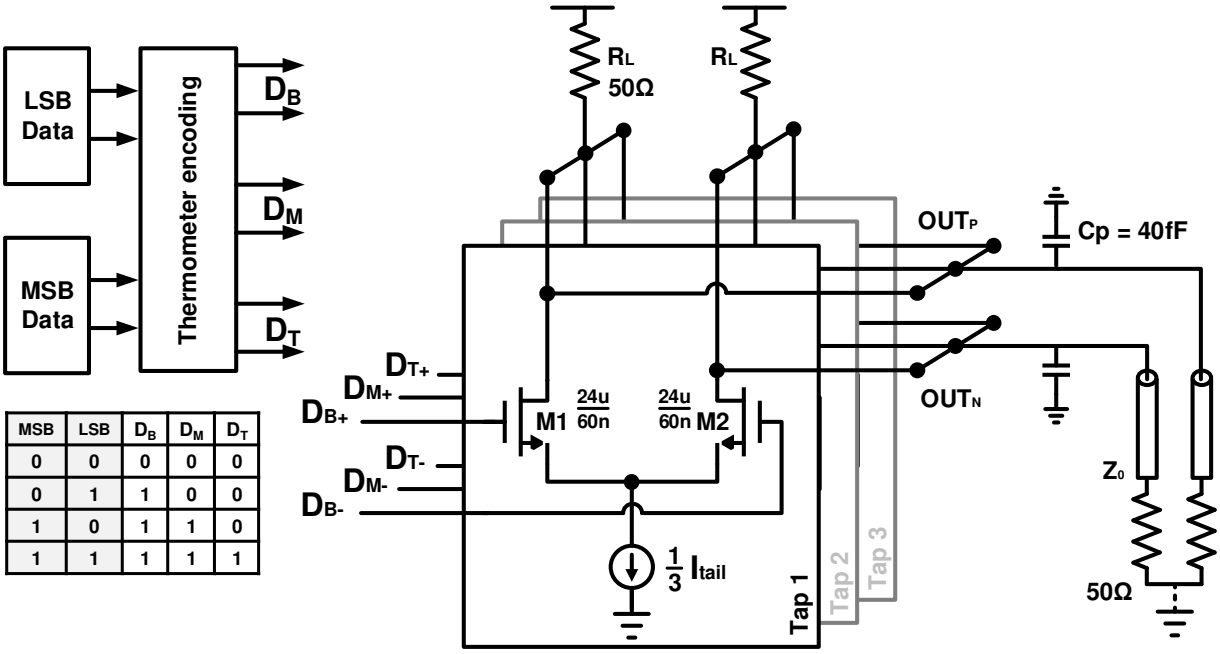


Fig. 4.18 Transistor-level simulation setup for the binary-scaled PAM-4 driver

Fig. 4.19 describes the simulation setup for a thermometer-coded PAM-4 driver. The baseband data streams are generated by a Verilog-A-based generator. The generator uses the PRBS13Q method to generate 10 GBaud data, and each of the output ports has a 50-Ω output impedance and a finite output 3 dB bandwidth of 30 GHz. The driver consists of three identical CML-based segments with a shared pair of 50-Ω resistors. The total size of the driver is the same as the binary-scaled driver in Fig. 4.18, and the biasing current (I_{tail}) is evenly distributed among all three drivers. The loading of this driver also consists of a pair of transmission lines (based on measured data of PCB traces), cascaded with two differentially terminated 50-Ω resistors.

Comprehensively analysis of the circuit behavior on CM noise performance is carried out. Simulations with different process corner settings (FF, TT, and SS) are performed to evaluate the

CM noise behavior under different process corners. The simulated details and results are summarized in Table VIII.



MSB	LSB	D_B	D_M	D_T
0	0	0	0	0
0	1	1	0	0
1	0	1	1	0
1	1	1	1	1

Fig. 4.19 Transistor-level simulation setup for the thermometer-coded PAM-4 driver

Based on the simulation setup in Fig. 4.18 and Fig. 4.19, the simulation setups for both binary-scaled and thermometer-coded PAM-8 systems are built and are shown in Fig. 4.20 and Fig. 4.21, respectively.

In Fig. 4.20, the 10 GBaud data streams are generated by a Verilog-A-based generator and the subsequent driver consists of three similar CML-based differential sub-drivers with binary-scaled sizing. The total tail current I_{tail} is same as the current of the previous PAM-4 drivers in Fig. 4.18, but it has been distributed to three drivers with the ratio of 4:2:1 respectively. The circuit loading is consistently the same as the cases in Fig. 4.18 and Fig. 4.19, which consists of a pair of 40fF capacitors for the output parasitic capacitances from bond-pads, a pair of differential microstrip lines on the PCB and two 50-Ω differential termination resistors.

In the thermometer-coded simulation of Fig. 4.21, the Verilog-A-based generator generates 10 GBaud data streams with a 7-bit output for the subsequent thermometer-coded PAM-8 driver. The

driver has seven segments with identical structures and combines the 7-bit thermometer codes into the differential PAM-8 output. The total biasing current for the driver, I_{tail}, is divided evenly for the seven CML-based sub-drivers. The circuit loading is the same as all previous transistor-level simulation setups in Fig. 4.18, Fig. 4.19 and Fig. 4.20.

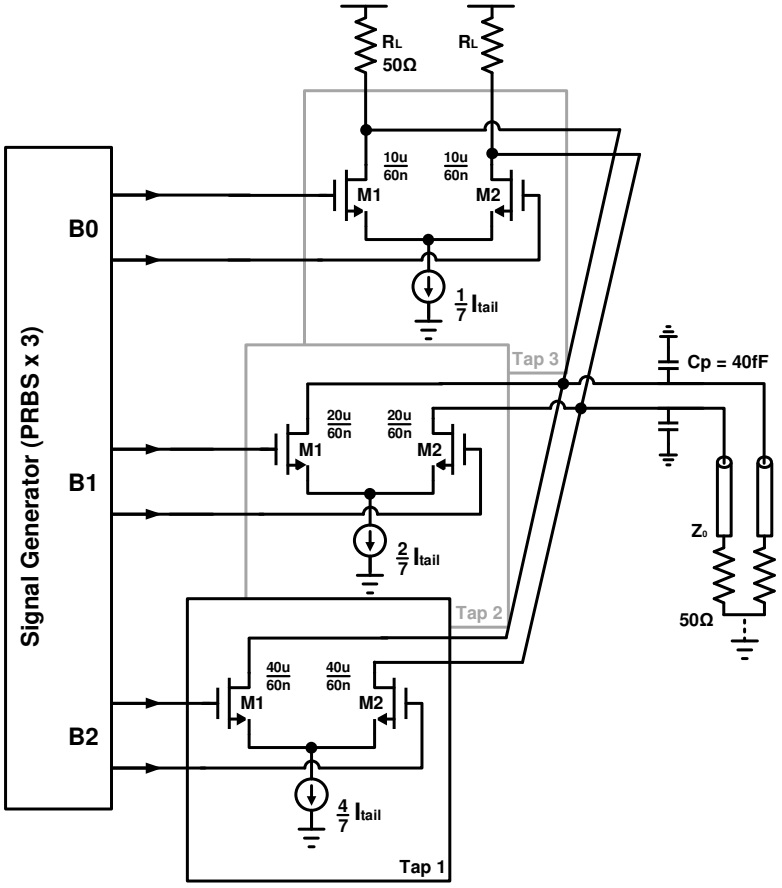
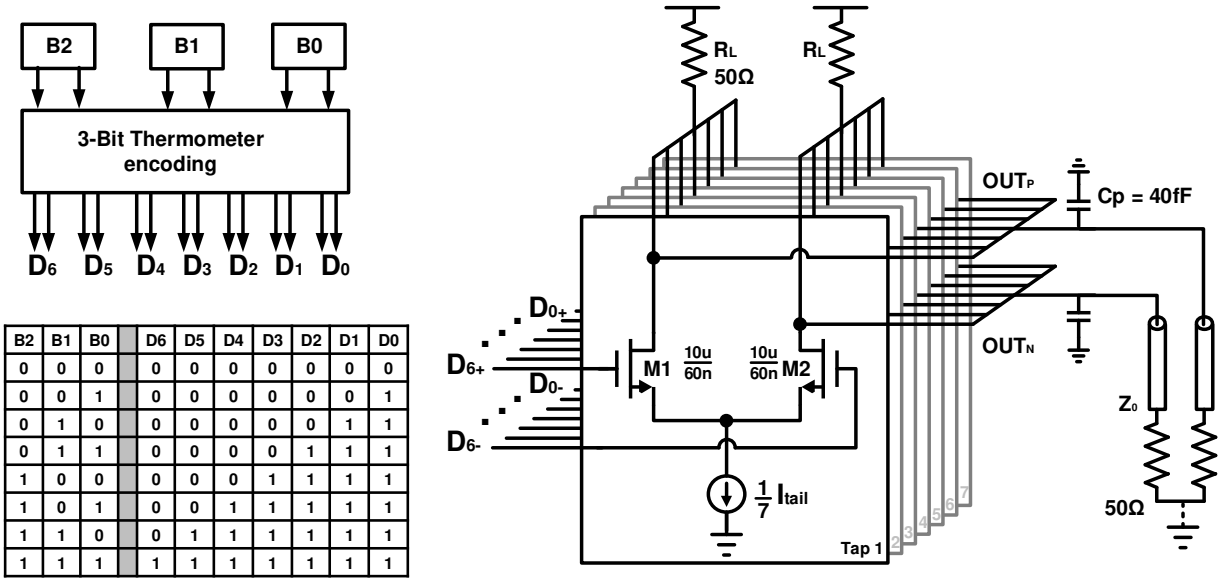


Fig. 4.20 Transistor-level simulation setup for the binary-scaled PAM-8 driver



B2	B1	B0	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	1	1
0	1	1	0	0	0	0	1	1	1
1	0	0	0	0	0	1	1	1	1
1	0	1	0	0	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1

Fig. 4.21 Transistor-level simulation setup for the thermometer-coded PAM-8 driver

All the simulation results of the binary-scaled and thermometer-coded in PAM-4 and PAM-8 topologies are summarized in Table VIII. By comparing the results in four different simulation setups under three different process corner settings, the following conclusions are drawn as the main takeaway keynotes for this chapter.

(a) Within same system topology, the process corner affects the CM noise performance in a way that the SS corner produces the worst CM noise while the FF corner provides the lowest. The reason has been revealed in Chapter 3 on the NRZ-based system, where transistors under the FF corner have better conductivity and they switch more like ideal switches, thus, the CM noise in the FF corner is significantly reduced.

(b) Under a certain process corner, the overall system power consumption remains the same, as long as the total output signal swing and the total driver sizing remain the same.

(c) Under a certain process corner, the CM noise performance of the binary-scaled topologies in both the PAM-4 and PAM-8 topologies are quite similar (1.34 mV for PAM-4 and 1.41 mV for PAM-8). The observation exactly matches the theoretical calculation in Table VI, because, in the

binary-scaled topologies, the statistical average switching distance is not correlated with the modulation scheme.

(d) Under a certain process corner, the simulated CM noises in the thermometer-coded topologies are better than the simulated CM noises in the binary-scaled topologies. This observation is qualitatively consistent with the previous conclusion in Table VI and Table VII.

(e) Due to the non-ideal effects in the circuit-level simulation, e.g. the parasitic effect and the non-linear G_m variation, the simulated differences between thermometer-coded topologies and binary-scaled topologies, at the behavior–level (Table VI) and the transistor-level (Table VIII) are not quantitatively matching.

Table VIII Summary table of transistor-level simulation results

	PAM4 BS*			PAM4 TC#			PAM8 BS			PAM8 TC		
Baud rate (GB)	**10**			**10**			**10**			**10**		
Data rate (Gbps)	**20**			**20**			**30**			**30**		
Double Nyquist frequency	**10 GHz**			**10 GHz**			**10 GHz**			**10 GHz**		
Transistor sizing	**48u+24u**			**24u × 3**			**40u+20u+10u**			**10u × 7**		
Process corner	**FF**	**TT**	**SS**	**FF**	**TT**	**SS**	**FF**	**TT**	**SS**	**FF**	**TT**	**SS**
DC current (mA)	**18.5**	**17.7**	**16.8**	**18.5**	**17.7**	**16.8**	**18.5**	**17.7**	**16.8**	**18.5**	**17.7**	**16.8**
Input swing (V)	**0.2**	**0.2**	**0.2**	**0.2**	**0.2**	**0.2**	**0.2**	**0.2**	**0.2**	**0.2**	**0.2**	**0.2**
Input biasing voltage (V)	**0.85**	**0.85**	**0.85**	**0.85**	**0.85**	**0.85**	**0.85**	**0.85**	**0.85**	**0.85**	**0.85**	**0.85**
Output swing (mV)	**214.9**	**234.7**	**253.7**	**214.8**	**234.7**	**253.6**	**212.1**	**231.7**	**250.7**	**212.1**	**231.7**	**250.7**
CM Noise @ 10GHz (mV)	**1.34**	**1.86**	**3.01**	**0.92**	**1.39**	**2.13**	**1.41**	**1.93**	**3.04**	**0.96**	**1.32**	**2.11**

* BS stands for binary-scaled

TC stands for thermometer-coded

4.5 Summary

In summary, the thermometer-code topology provides several advantages over the traditional binary-scaled topologies other than the CM noise performance. Table IX lists a brief comparison between the binary-scaled and thermometer-coded topologies.

Table IX Comparison between binary-scaled PAM-4 and thermometer-coded PAM-4

Topology	**Binary-scaled**	**Thermometer-coded**
Power	Same	Same
BW	Same	Same
Data rate	Same	Same
Output swing	Same	Same
Amplitude adjustment	Top and bottom eyes are bonded	3 data eyes are independent
Waveform distortion	Inevitable distortion	Small distortion
CM Noise @ $2F_{Nyuist}$	Larger	Smaller

On one hand, the difference of implementations of binary-scaled and thermometer-coded PAM-4 drivers is only to split the MSB driver in binary-scaled topology into two halves, and to encode the binary data into 3-bit thermometer-coded data in the baseband. Thus, in the driver stage, which is normally a power-hungry block in a wireline transmitter, the power consumption and the driver bandwidth all remain the same because, in terms of circuit implementation, there is no significant modification.

On the other hand, in a PAM-4 based optical communication system, the driver circuit, which acts as the electrical to the optical interface, is also designed to compensate the nonlinearity of the subsequent optical components [51]. Moreover, the nonlinearity of the subsequent optical

components also introduces the time skews between three data eyes [54]. In the traditional binary-scaled topology, the top and bottom data eyes are bonded, meaning that the time skew or amplitude mismatch between the top and bottom eyes are difficult to compensate. However, thermometer-coded topology has intrinsic flexibility for the amplitude and channel skew compensation, because the bottom, middle and top data eyes are independently tunable.

Thus, with all the analyze above, in a PAM-4 based wireline link, the thermometer-coded topology is more appealing and promising when compared to the traditional binary-scaled one due to the better CM noise performance, the better flexibility to compensate amplitude and skew distortions, and, last but not least, the minimum requirement for power overhead.

According to the mathematical derivations in Chapter 2, the similar calculation can be extended to PAM-4 or even PAM-8 signals. The final expression of CM noise in PAM-4/PAM-8 is:

$$N(2f_{Nyquist}) = \frac{1}{8}\beta_S \cdot Amp \frac{\left|t_{rise} - t_{fall}\right|}{T_s} \cdot \sin c^2(\frac{\pi}{2} \cdot \frac{T_{tr}}{T_s}). \tag{4.30}$$

In the equation, Amp is the signal amplitude, t_{rise} and t_{fall} are the rise and fall time in data transitions, T_{tr} is the total data transition time, and T_s is the period of each data symbol. All the variables are defined as same as the previous equation except a newly introduced coefficient β_S, which describe the impact of system topology.

According the analysis of the average switching distance in Table VI, all binary-scaled topologies in PAM-4/8/16 have same average switching distance $\frac{1}{2}A_{total}$, and the thermometer-scaled topologies have smaller switching distance, thus, the corresponding coefficient β_S in a PAM-2k thermometer topology is calculated as:

$$\beta_S = \frac{SD^{T}_{PAM-2^k}}{SD^{B}_{PAM-2^k}} = \frac{\frac{1}{2^{2k}}\sum_{n=0}^{2^k-1}(\sum_{x=0}^{n}\frac{x}{2^k-1}+\sum_{y=n}^{2^k-1}\frac{y-n}{2^k-1})A_{total}}{\frac{1}{2}A_{total}}. \quad (4.31)$$

β_S is defined as the ratio of the average switching distance of PAM-2k thermometer-coded topology over the average switching distance of PAM-*2k* binary-scaled topology. The different calculated coefficient of different topologies are summarized in Table X.

Table X Calculated β_S for different topologies

β_S	PAM-4	PAM-8	PAM-16
Binary-scaled	1	1	1
Thermometer-coded	0.83	0.75	0.71

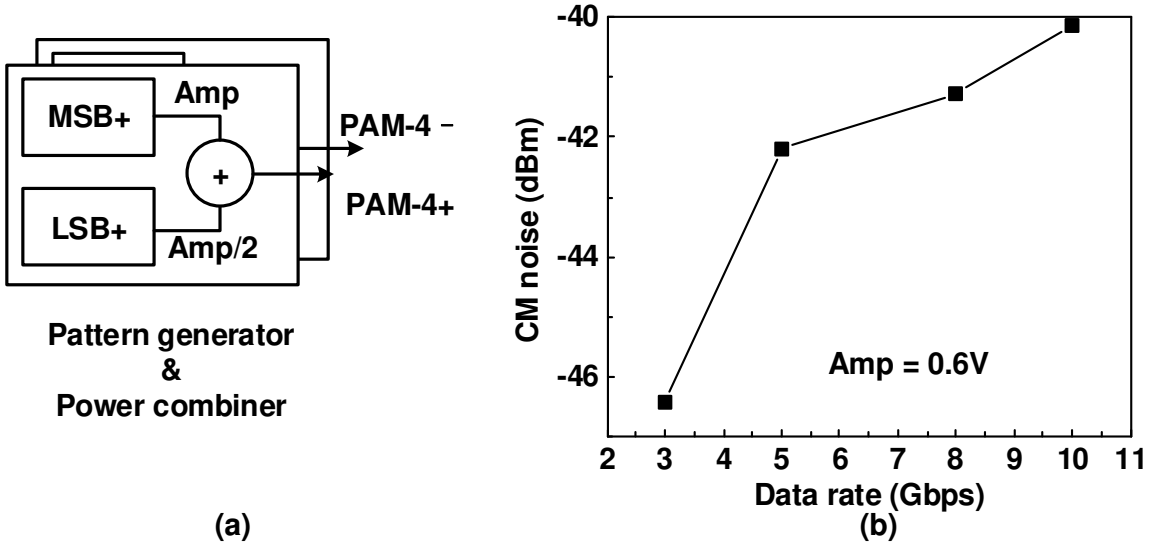


Fig. 4.22 PAM-4 measurement result: CM noise vs. data rate.

By using the measurement instrument (Tektronix PPG3202), differential PAM-4 signals are obtained by combining two channels of NRZ data sequences, as depicted in Fig. 4.22(a). The amplitude of MSB channel is the double of the LSB amplitude. And the final PAM-4 output (PAM-

4– and PAM-4+) are combined by another power combiner to extract the CM signal. After all the combining, the extracted CM signal goes into a spectrum analyzer to get the CM noise at $2f_{Nyquist}$. When the signal amplitude is fixed, the output CM noise is positively correlated to the data rate according to the description in (4.30). The measurement results in Fig. 4.22(b) support the argument.

In summary, (4.30) gives a generic description of CM noise in different PAM-2/4/8/16 systems, and the CM noise is directly associated with several critical factors, including the period of each data symbol T_s, the total signal amplitude Amp, the mismatch between rising and falling edges $\left|t_{rise} - t_{fall}\right|$, and the system topology indicated by the coefficient β_S.

Chapter 5 Summary and Future Work

5.1 Summary

This work studies the EMI-related CM noise issue in typical high-speed backplane links. Both the NRZ and PAM-4 signals are discussed and analyzed.

Chapter 2 starts with the basic concepts in the EMI issue in high-speed communication, and gradually unveils the characteristics of the CM noise. Among all the conclusions in Chapter 2, the most important takeaway one is that only the mismatch between rising and falling edges generates the CM noise tone at $2f_{Nyquist}$ and its mathematic expression is shown below:

$$N(2f_{Nyquist}) = \frac{1}{4} A \frac{T_{tr}}{T_b} \cdot \sin c^2(\frac{\pi}{2} \cdot \frac{T_{tr}}{T_b}) = \frac{1}{8} Amp \frac{\left| t_{rise} - t_{fall} \right|}{T_b} \cdot \sin c^2(\frac{\pi}{2} \cdot \frac{T_{tr}}{T_b}) . \quad (5.1)$$

(5.1) shows the critical factors of the EMI-related CM noise, where T_b is the period for each symbol, T_{tr} is the total data transition time, A is the amplitude of voltage spike during each data transition, Amp is the signal swing and $\left| t_{rise} - t_{fall} \right|$ is the quantitative difference between rising and falling edge. The equation concludes the ways to suppress CM noise, e.g. reducing the signal amplitude, minimizing the difference between rising and falling time and shorten the data transition.

In Chapter 3, we have verified the CM noise with the simulation and the measurement results of a CML-based test chip. First, the process corner settings in the simulation setup are proved to dramatically affect the circuit CM noise, thus, during the measurement, only 13 chip samples in the TT corner are screened out for the later on CM noise measurements. Second, the circuit CM noise is positively correlated to the signal swing as predicted in Chapter 2. Last but not least, optimizing the circuit biasing condition can balance the rising and falling edges, provide sufficient gain simultaneously, and dramatically reduce the CM noise.

In Chapter 4, we extend the methodologies of analyzing NRZ signals to PAM-4 signals. A technical term of 'switching distance' is created to describe the data transitions in the PAM-4 system or even PAM-8/16 systems. According to the results from the behavior-level simulation and the circuit-level simulation, the thermometer-coded system architecture is proposed to reduce the CM noise, up to 20%, when compared with the traditional binary-scaled topologies.

However, the EMI noise in a wireline communication link is still not easy to predict or simulate because it requires the mixed simulation environment with both the electric domain simulator and electromagnetic field simulator simultaneously. Instead of precisely simulating the EMI emission, engineers can either reduce the EMI-related noise as much as possible by using particular circuit design techniques or providing efficient simulation tools or noise models for the system-level design.

5.2 Future work

Based on the current work, it is worthy to develop the prediction and reduction techniques of EMI noise. Since either the technique of CM noise prediction or the technique of CM noise reduction is mature enough to be generic commercialized. We offer two development directions in the following discussion as the guideline and inspiration for other researchers. One is the CM noise reduction technique at circuit-level for circuit designers, and the other one is the system-level methodology for EMI-related CM noise prediction for system engineers.

5.2.I Circuit-level CM Noise Reduction

The method of CM noise reduction is straightforward and intuitive. It is based on the previously proposed optimization techniques in Chapter 3, which are reducing signal swing and optimizing

biasing voltage. As depicted in Fig. 5.1, the proposed adaptive CM noise reduction circuit contains two basic adaptive loops. One is used to limit the signal swing, as loop 1 in the figure, and the other one, loop 2, is used to optimize the input signal biasing voltage.

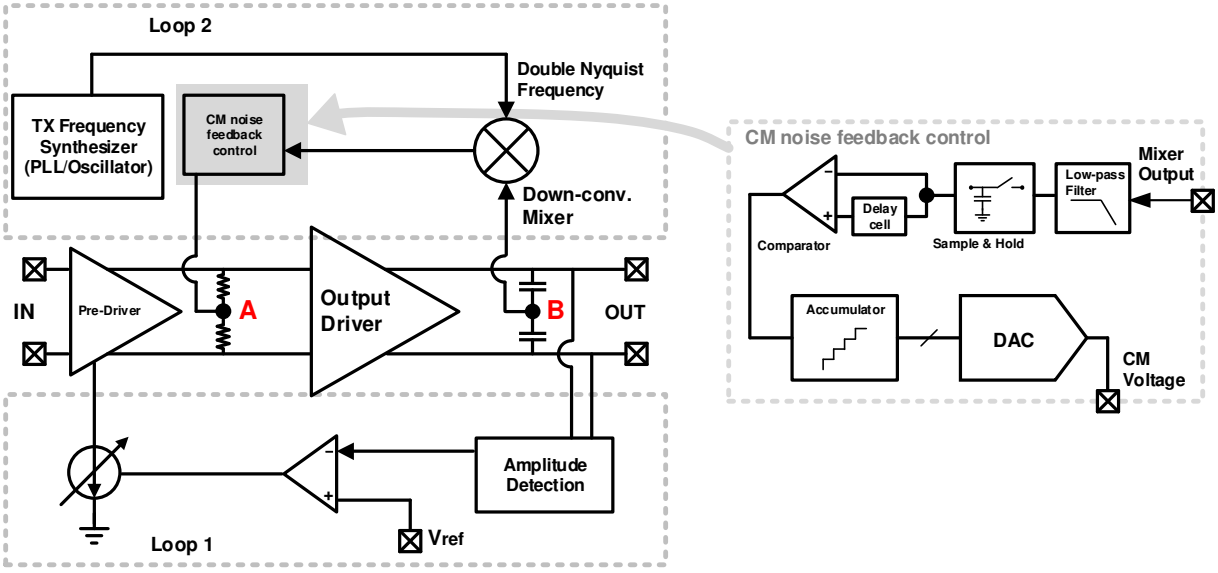


Fig. 5.1 Adaptive CM noise reduction loop

In loop 1, an amplitude detection circuit detects the output signal swing and send the amplitude information to the subsequent comparator. The comparator compares the amplitude with a predefined reference voltage, and adjust the current biasing for the pre-driver stage to limit the signal swing at position A, as shown in Fig. 5.1.

Loop 2 optimizes the biasing voltage at position A with the following control logic. The output CM signal is sensed with a pair of weakly coupled capacitors, as shown in the position B. The sensed CM signal is fed into the down-conversion mixer, which mixes the CM signal with the local oscillation frequency of the double Nyquist frequency, $2f_{Nyquist}$. After the mixer, the CM noise at is mixed down to DC or mixed up to $4f_{Nyquist}$. The mixer output signal goes through a low-pass filter to filter out only the DC component. The subsequent sample and hold circuit samples the DC

component for the cascaded comparator and control logic circuits. The adaptive CM noise reduction loop is currently proposed, with no simulation or experimental data available yet.

5.2.II System-level CM Noise Simulation

As mentioned above, the other way to help diagnose the EMI issue in the high-speed wireline link is to provide efficient and accurate models for system designers. Obviously, the circuit models used in Chapter 3 and 4 are the transistor-level net-lists. The transistor-level models do provide better accuracy than the I/O buffer information specification (IBIS) model [55], which is normally used by system-level signal integrity investigation.

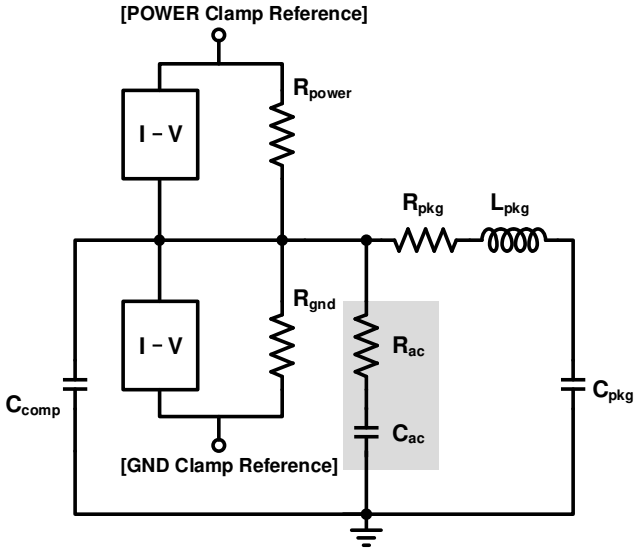


Fig. 5.2 IBIS model for output buffers

Fig. 5.2 shows the generic output buffer model in IBIS library. Basically, the pull-down and pull-up DC characteristics are represented by two I-V tables, the pull-up resistor (R_{power}), and pull-down resistor (R_{gnd}). The AC small-signal model consists of the R-C network of R_{ac} and C_{ac}. R_{pkg}, L_{pkg}, and C_{pkg} are used to model the package parasitic resistance, inductance, and capacitance, respectively. The IBIS buffer model is obviously much simpler, and the model accuracy is

correspondingly worse when compared to the transistor-level buffer models used in all previous chapters. However, also due to the simplicity, the IBIS model can provide an extremely fast system-level evaluation. Thus, the trade-off between simulation accuracy and speed is worthy to be optimized.

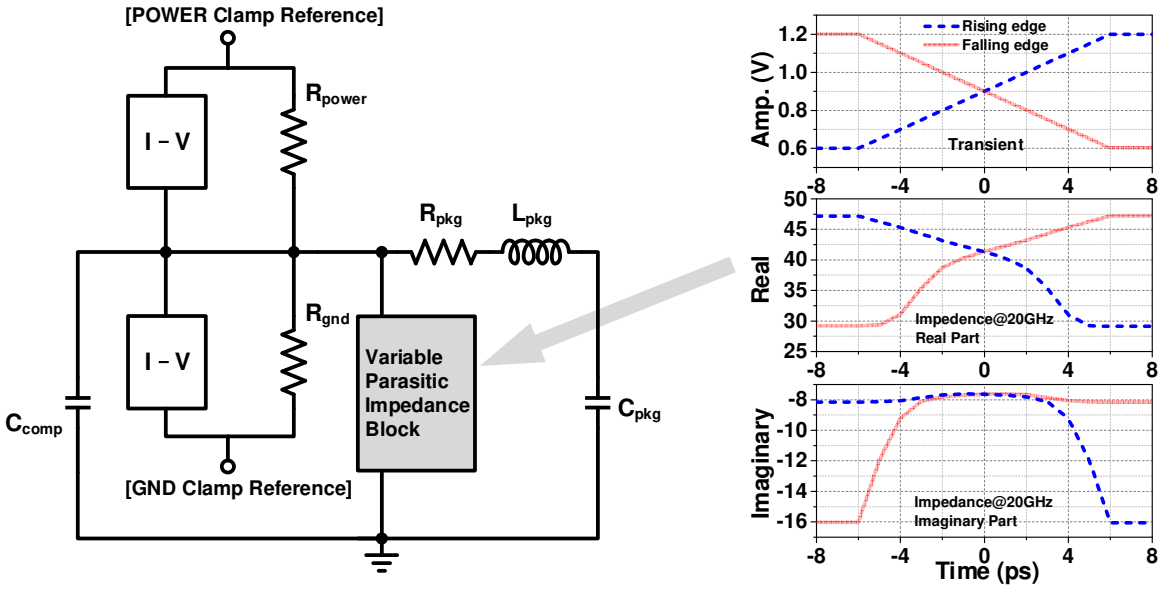


Fig. 5.3 Modified IBIS model for high-speed output buffers

As discussed in Chapter 3, the ultimate reason for CM noise is the equivalent impedance variation during each data transition, saying the differential transistors are experiencing different impedance variations during the data rising and falling edges. However, according to the description in Fig. 5.2, the AC small-signal network is fixed and there is no specification for the impedance variation. Thus, CM noise is difficult to be evaluated at the system-level with the existing IBIS models.

Fig. 5.3 shows a possible solution for the system-level CM noise evaluation. Instead of using only the AC resistor and capacitors to represent the AC small signal characteristics, we use a variable parasitic impedance block to model the impedance variation. The impedance variation will be calculated based on the measurement results, or, at least the transistor-level simulation

results. Once the measurement, or the transistor-level simulation, has been done and the impedance variation information is obtained. The corresponding impedance block will be inserted into the IBIS model to perform the system level evaluation. Comparing to the transistor-level simulation, this approach greatly simplifies the actual circuit topology but maintains the key information for CM noise evaluation at meanwhile. Nevertheless, the accurate measurement of the equivalent impedance variation is definitely difficult, and the accuracy of the modeling directly associates with the final CM noise evaluation. Therefore, future measurement and modeling are required to evaluate the feasibility of this approach.

Bibliography

[1] J. Glanz, "Power, Pollution and the Internet," *New York Times*, Sep. 2012.

[2] "Cisco UCS - Data Center." [Online]. Available: https://www.cisco.com/c/r/en/us/internet-of-everything-ioe/data-center/vision/index.html. [Accessed: 12-Oct-2017].

[3] Omar Hassen, "True 100G: The End Game for 100GE | OFC." [Online]. Available: http://www.ofcconference.org/zh-cn/home/about/ofc-blog/2016/march-1026/true-100g-the-end-game-for-100ge/. [Accessed: 12-Oct-2017].

[4] *IEEE 802.3 NGOATH SG Adopted Changes to 802.3bs Project Objectives*.

[5] *High-Speed Transmission Update: 200G/400G*.

[6] Wikipedia, "Electromagnetic interference." [Online]. Available: https://en.wikipedia.org/wiki/Electromagnetic_interference.

[7] M. D. Paglin, J. R. Hobson, and J. Rosenbloom, *The Communications Act: A Legislative History of the Major Amendments, 1934-1996*. Pike & Fischer - A BNA Company, 1999.

[8] FCC, *UNDERSTANDING THE FCC REGULATIONS FOR COMPUTERS AND OTHER DIGITAL DEVICES*. 1993.

[9] Daniel Hoolihan, "Radiated Emission Measurements at 1/3/5/10/30 Meters." [Online]. Available: https://interferencetechnology.com/radiated-emission-measurements-at-1351030-meters/. [Accessed: 22-Oct-2017].

[10] J. Adam, Chi Shih Chang, J. J. Stankus, M. K. Iyer, and W. T. Chen, "Addressing packaging challenges," *IEEE Circuits Devices Mag.*, vol. 18, no. 4, pp. 40–49, Jul. 2002.

[11] C. Ben, R. Kollipara, O. Dan, Y. Chuck, and L. S. Boluna, "Study of PCB trace crosstalk in backplane connector pin field," in *Electrical Performance of Electronic Packaging, EPEP*, 2006, pp. 281–284.

[12] D. Luo, X. Luo, K. Qasim Maqbool, Y. Huang, H. Yu, and C. P. Yue, "Analysis on EMI Related Common-mode Noise of SERDES Transmitter," in *DesignCon*, 2017.

[13] M. Rowlands, X. Li, and A. Bhobe, "EMI Analysis of High-Speed I / O Connector in an Active System," in *DesignCon*, 2015.

[14] Daniel Chow, "The basics of digital signal spectra," 2013. [Online]. Available: https://www.edn.com/design/test-and-measurement/4422710/The-basics-of-digital-signal-spectra. [Accessed: 23-Oct-2017].

[15] T. Steinecke *et al.*, "Generic IC EMC Test Specification," in *2012 Asia-Pacific Symposium on Electromagnetic Compatibility*, 2012, pp. 5–8.

[16] W. Pfaff *et al.*, "Generic IC EMC Test Specification Version 2.1." 2017.

[17] M. W. Fogg, "Understanding the Effects of Channel Generated Skew on Chassis EMI," in *DesignCon*, 2015.

[18] P. Acimovic, "Novel Band-Stop Common Mode Filter For High-Speed Digital Data Transmission," in *DesignCon*, 2007.

[19] P. Acimovic, "Loaded Parallel Stub Common Mode Filter," in *DesignCon*, 2008, vol. 1, pp. 5–8.

[20] P. Acimovic, "Transformer based circuit for reducing EMI radiation in high-speed CMOS SERDES transmitters," US9130650 B1, 2013.

[21] P. Acimovic, P. Mishra, and R. W. Hernandez, "Reduction of electromagnetic interference for differential signals," US8004330 B1, 2009.

[22] S. Wang and F. C. Lee, "Investigation of the Transformation Between Differential-Mode and Common-Mode Noises in an EMI Filter Due to Unbalance," *IEEE Trans. Electromagn. Compat.*, vol. 52, no. 3, pp. 578–587, Aug. 2010.

[23] Hao-Hsiang Chuang and Tzong-Lin Wu, "Suppression of Common-Mode Radiation and

Mode Conversion for Slot-Crossing GHz Differential Signals Using Novel Grounded Resonators," *IEEE Trans. Electromagn. Compat.*, vol. 53, no. 2, pp. 429–436, May 2011.

[24] F. Grassi, Y. Yang, X. Wu, G. Spadacini, and S. A. Pignari, "On Mode Conversion in Geometrically Unbalanced Differential Lines and Its Analogy With Crosstalk," *IEEE Trans. Electromagn. Compat.*, vol. 57, no. 2, pp. 283–291, Apr. 2015.

[25] M. Rowlands, A. Bhobe, C. Systems, P. Casher, and X. Li, "Quantitative EMI Analysis of Electrical connectors Using Simulation Models," in *DesignCon*, 2014.

[26] D. M. Hockanson, J. L. Drewniak, T. H. Hubing, T. P. Van Doren, F. Sha, and M. J. Wilhelm, "Investigation of fundamental EMI source mechanisms driving common-mode radiation from printed circuit boards with attached cables," *IEEE Trans. Electromagn. Compat.*, vol. 38, no. 4, pp. 557–566, 1996.

[27] "Autocorrelation & Power Spectral Density." [Online]. Available: http://www.navipedia.net/index.php/Autocorrelation_%26_Power_Spectral_Density. [Accessed: 05-Oct-2017].

[28] J. Redd and C. Lyon, "Spectral content of NRZ test patterns," *EDN*, vol. 49, no. 18. pp. 67–72, 2004.

[29] J. K. Kim and T. S. Kalkur, "High-speed current-mode logic amplifier using positive feedback and feed-forward source-follower techniques for high-speed CMOS I/O buffer," *IEEE J. Solid-State Circuits*, vol. 40, no. 3, pp. 796–802, Mar. 2005.

[30] K. Q. Maqbool, D. Luo, X. Luo, H. Yu, and C. P. Yue, "EMI-Related Common-Mode (CM) Noise Analysis and Prediction of High-Speed Source-Series Terminated (SST) I/O Driver in System-on-Package (SOP)," *IEEE Trans. Circuits Syst. II Express Briefs*, pp. 1–1, 2017.

[31] B. Razavi, *Design of Analog CMOS Integrated Circuits*, 1st ed. Tata McGraw-Hill, 2001.

[32] Tzong-Lin Wu, F. Buesink, and F. Canavero, "Overview of Signal Integrity and EMC

Design Technologies on PCB: Fundamentals and Latest Progress," *IEEE Trans. Electromagn. Compat.*, vol. 55, no. 4, pp. 624–638, Aug. 2013.

[33] G. H. Shiue, J. H. Shiu, Y. C. Tsai, and C. M. Hsu, "Analysis of common-mode noise for weakly coupled differential serpentine delay microstrip line in high-speed digital circuits," *IEEE Trans. Electromagn. Compat.*, vol. 54, no. 3, pp. 655–666, Jun. 2012.

[34] J. Li and J. Fan, "Radiation Physics and Design Guidelines of High-Speed Connectors," *IEEE Trans. Electromagn. Compat.*, vol. 58, no. 4, pp. 1331–1338, Aug. 2016.

[35] C.-C. Yeh, K.-C. Chen, and C.-L. Wang, "Common-Mode Noise Suppression of Differential Serpentine Delay Line Using Timing-Offset Differential Signal," *IEEE Trans. Electromagn. Compat.*, vol. 57, no. 6, pp. 1457–1465, Dec. 2015.

[36] Wei-Tzong Liu, Chung-Hao Tsai, Tzu-Wei Han, and Tzong-Lin Wu, "An Embedded Common-Mode Suppression Filter for GHz Differential Signals Using Periodic Defected Ground Plane," *IEEE Microw. Wirel. Components Lett.*, vol. 18, no. 4, pp. 248–250, Apr. 2008.

[37] Q. Liu *et al.*, "Reduction of EMI Due to Common-Mode Currents Using a Surface-Mount EBG-Based Filter," *IEEE Trans. Electromagn. Compat.*, vol. 58, no. 5, pp. 1440–1447, Oct. 2016.

[38] M. Kim, "Periodically Corrugated Reference Planes for Common-Mode Noise Suppression in High-Speed Differential Signals," *IEEE Trans. Electromagn. Compat.*, vol. 58, no. 2, pp. 619–622, Apr. 2016.

[39] G. A. Matig-a, M. R. Yuce, and J. M. Redouté, "An integrated LVDS transmitter in 0.18-μm CMOS technology with high immunity to EMI," *IEEE Trans. Electromagn. Compat.*, vol. 57, no. 1, pp. 128–134, Feb. 2015.

[40] G. E. Matig-A, M. R. Yuce, and J. M. Redoute, "Design of a CML Transceiver with Self-

Immunity to EMI in 0.18-?? m CMOS," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 64, no. 4, pp. 981–991, Apr. 2017.

[41] K. Q. Maqbool, D. Luo, G. Zhu, X. Luo, H. Yu, and C. P. Yue, "EMI common-mode (CM) noise suppression from self-calibration of high-speed SST driver using on-chip process monitoring circuit," in *2017 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2017, pp. 1–4.

[42] B. Razavi, *Design of integrated circuits for optical communications*, 2nd ed. Wiley, 2012.

[43] S. S. Mohan, M. D. M. Hershenson, S. P. Boyd, and T. H. Lee, "Bandwidth extension in CMOS with optimized on-chip inductors," *IEEE J. Solid-State Circuits*, vol. 35, no. 3, pp. 346–355, Mar. 2000.

[44] W. Way, "PAM-4: A Key Solution For Next-Generation Short-Haul Optical Fiber Links," 2015. [Online]. Available: https://www.neophotonics.com/pam-4-key-solution-next-generation-short-haul-optical-fiber-links/. [Accessed: 27-Sep-2017].

[45] J. Lee, P. C. Chiang, P. J. Peng, L. Y. Chen, and C. C. Weng, "Design of 56 Gb/s NRZ and PAM4 SerDes transceivers in CMOS technologies," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 9. pp. 2061–2073, Sep-2015.

[46] P. C. Chiang, H. W. Hung, H. Y. Chu, G. S. Chen, and J. Lee, "60Gb/s NRZ and PAM4 transmitters for 400GbE in 65nm CMOS," in *Digest of Technical Papers - IEEE International Solid-State Circuits Conference*, 2014, vol. 57, pp. 42–43.

[47] T. Zuo, L. Zhang, J. Zhou, Q. Zhang, E. Zhou, and G. N. Liu, "Single Lane 150-Gb/s , 100-Gb/s and 70-Gb/s 4-PAM Transmission over 100-m , 300-m and 500-m MMF Using 25-G Class 850nm VCSEL," in *2016 European Conference and Exhibition on Optical Communications (ECOC)*, 2016, pp. 974–976.

[48] F. Karinou, N. Stojanovic, C. Prodaniuc, Z. Qiang, and T. Dippon, "112 Gb/s PAM-4

Optical Signal Transmission over 100-m OM4 Multimode Fiber for High-Capacity Data-Center Interconnects," in *2016 European Conference on Optical Communication, ECOC*, 2016, pp. 124–126.

[49] P. J. Peng, J. F. Li, L. Y. Chen, and J. Lee, "A 56Gb/s PAM-4/NRZ transceiver in 40nm CMOS," in *Digest of Technical Papers - IEEE International Solid-State Circuits Conference*, 2017, vol. 60, pp. 110–111.

[50] P. D. Townsend, P. Ossieur, and N. Quadir, "A 56Gb/s PAM-4 VCSEL driver circuit," in *IET Irish Signals and Systems Conference (ISSC 2012)*, 2012, pp. 59–59.

[51] T. Kishi *et al.*, "56-Gb/s Optical Transmission Performance of an InP HBT PAM4 Driver Compensating for Nonlinearity of Extinction Curve of EAM," *J. Light. Technol.*, vol. 35, no. 1, pp. 75–81, Jan. 2017.

[52] J. L. Zerbe *et al.*, "Equalization and clock recovery for a 2.5-10-Gb/s 2-PAM/4-PAM backplane transceiver cell," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2121–2130, Dec. 2003.

[53] A. Healey and J. Slavick, "PAM4 transmitter training protocol," 2016. [Online]. Available: http://www.ieee802.org/3/cd/public/July16/healey_3cd_01a_0716.pdf. [Accessed: 29-Sep-2017].

[54] W. Soenen *et al.*, "40 Gb/s PAM-4 Transmitter IC for Long-Wavelength VCSEL Links," *IEEE Photonics Technol. Lett.*, vol. 27, no. 4, pp. 344–347, Feb. 2015.

[55] "IBIS (I/O Buffer Information Specification)." 2015.