Energy-Efficient CMOS Optical Receiver for Short-Reach Data Center Application

by

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Abstract

Optical interconnects have been deployed in data centers to replace electrical interconnects, offering enhanced traffic capacity and reduced power consumption. As data center networks scale in bandwidth (BW) and physical size, the cost and power consumption of optical transceivers have risen significantly. Further scaling of energy efficiency and BW density remains challenging due to limited integration in optical modules. This thesis focuses on the design of energy-efficient CMOS four-level pulse amplitude modulation (PAM-4) optical receivers (ORXs) for short-reach data center applications.

Based on a simplified shunt feedback (SF) transimpedance amplifier (TIA) model, noise-BW relationship is first analyzed and derived. ORX sensitivity enhancement by the continuous-time linear equalizer (CTLE), the feed-forward equalizer (FFE), and the decision feedback equalizer (DFE) are analyzed and simulated. The derivations indicate that the CTLE reduces the thermal noise from the SF resistor, but it leaves the color noise unaffected. System-level simulations demonstrate sensitivity improvement through post-TIA equalizations.

A 48-Gb/s PAM-4 ORX data path, integrating a linear TIA and a sampler, is introduced. The TIA employs a transadmittance-stage transimpedance-stage (TAS-TIS) topology, replacing conventional variable gain amplifiers (VGA) and post-amplifiers based on current-mode logic, avoiding CTLEs and passive inductors while preserving the linearity and gain-BW product for PAM-4 operation. The sampler exploits a 2-tap FFE and a 2-tap DFE to improve sensitivity and ensure correct data recovery. Fabricated in a 28-nm CMOS process, the ORX demonstrates a -5.1-dBm sensitivity and 1.28-pJ/bit (0.27 pJ/bit for TIA alone) efficiency at 48-Gb/s PAM-4.

A 100-Gb/s PAM-4 TIA is designed to relax the tradeoffs between BW, noise, and power without compromising linearity. Inverter-based circuits are predominantly used across stages. A current reuse VGA employing a TAS-TIS topology with high linearity is proposed, offering a large tuning range with fine step size. Multi-layer stacked network, T-coils and inductors are employed to achieve high inductance density, expanding the overall BW despite the presence of ESD diodes at both input and output. Implemented in a 28-nm CMOS process, the TIA achieves a BW of 28 GHz, a dc transimpedance gain of 65 dBΩ, an input referred noise density of 16 pA/√Hz, a THD of less than 5% up to 640 μA_{pp} input current, and 0.32-pJ/bit efficiency.

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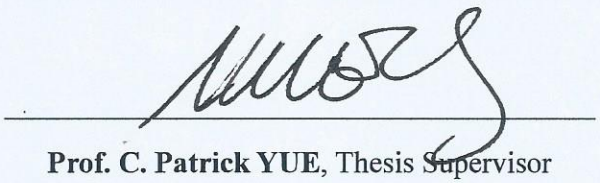

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Tempus Fugit

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Chapter 1

Introduction

1.1 Motivation

Data centers are crucial for storing, managing, analyzing and distributing data and information to the operation of online systems, applications, and services. The ever-increasing demand on the data centers with higher-bandwidth (BW), lower-cost and more energy-efficient solutions keeps increasing bolstered by the proliferation of data intensive applications, such as 5G, internet video, cloud-enabled services, and machine learning [1], [2]. The rise of big data and Internet of things (IoT) fuels data center market growth. As shown in Figure 1.1 [3], the size of data center market was valued at USD 312.3 billion in 2022 and is projected to grow from USD 372.78 billion in 2023 to USD 624.07 billion by 2030, exhibiting a compound annual growth rate (CAGR) of 7.6% during the forecast period (2023 - 2029). Of particular note is that network infrastructure accounts for more than 50% of the market share, and the revenue is forecast to exhibit strong growth in all segments in 2029.

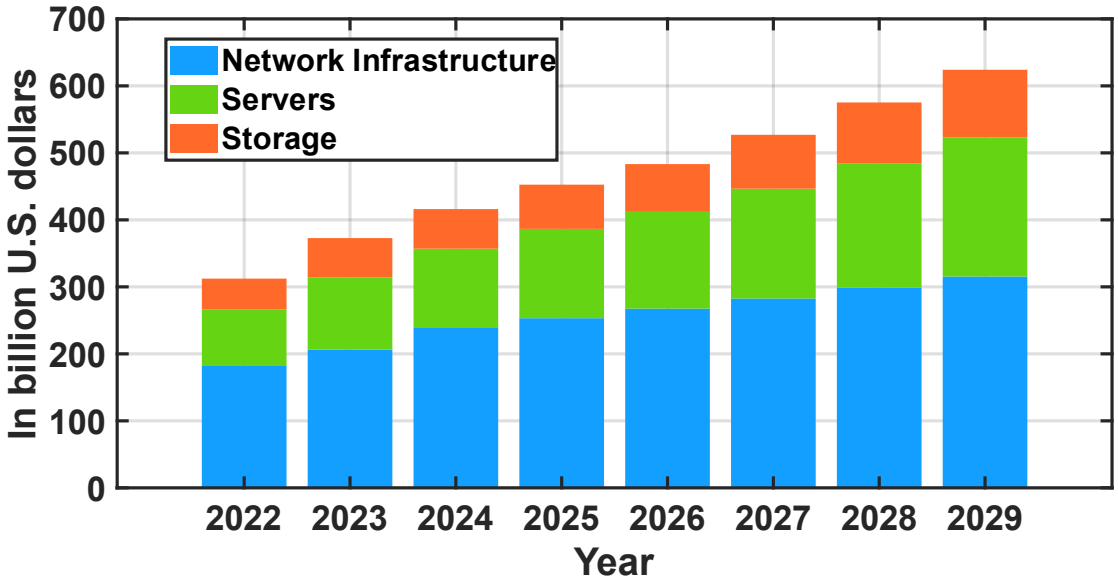


Figure 1.1. Revenue in the data center market for different segments worldwide from 2022 to 2029 (in billion U.S. dollars) [3].

Scaling data centers to support higher traffic capacity poses significant challenges of providing higher data rate per area while managing power consumption and attendant heat dissipation. As the data rate continues to increase, traditional electrical interconnects within data centers have been pushed to their limits. Electrical I/Os have reached a bottleneck where it is impossible to overcome the BW limitation without sacrificing other performance metrics like power, reach or cost. Thus, the trend towards optical links has continued to grow due to the benefits provided by the optical channels and the development of electrical-to-optical (E/O) and optical-to-electrical (O/E) conversion technologies [4]. Optical scaling also continues to further support ultra-short-reach (USR) links and high-density interconnects, facilitating the increases in computational demands and performance of high-performance computing (HPC) modules [5]. In such cases, a high-BW, high-density, power-efficient and low-latency optical interface is therefore required.

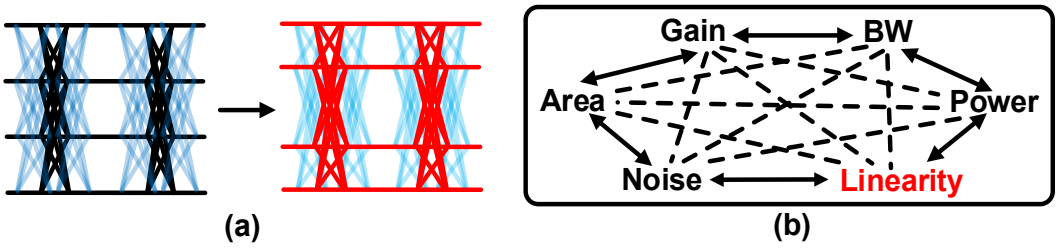


Figure 1.2. (a) Illustration of the effect of linearity on PAM-4 eye diagrams. (b) Design tradeoffs with linearity taken into consideration.

The modulation format is migrating towards four-level pulse amplitude modulation (PAM-4) format to provide higher spectral efficiency compared to non-return-to-zero (NRZ) modulation. However, as illustrated in Figure 1.2 (a), adapting to PAM-4 comes at the expense of enforced linearity constraints in both optical and electrical components, and the signal integrity becomes more vulnerable to both noise and linearity, presenting lower tolerance for signal-to-noise ratio (SNR). Compared with NRZ designs, besides the well-known BW-noise trade-off, PAM-4 systems place more emphasis on minimizing power consumption. Additionally, linearity has become a critical factor in design trade-offs, as highlighted in Figure 1.2 (b), which urges the development of optical interconnects featuring low noise, high-density, high power-efficiency, and high linearity.

1.2 Background

Intensity-modulation direct-detection (IMDD) optical system is the most straightforward implementation in short-reach interconnects due to its simplicity and low cost. In such systems, the transmitted data modulates the light intensity of a laser or an optical modulator, whereas a direct-detection receiver (RX) connected with a photodiode (PD) recovers the information at the RX side. Figure 1.3 provides a high-level overview of a typical IMDD optical interconnect, which consists of three main components: optical modules for electrical-to-optical (E/O) and optical-to-electrical (O/E) conversion, an electrical transceiver (front end + SerDes) for signal amplification and serialization/deserialization, and a digital signal processor (DSP) for data processing. On the RX side, the light from the optical fiber is detected by a PD, which generates a small output current in proportion to the light intensity. This current is then amplified and converted to a voltage by a transimpedance amplifier (TIA). A demultiplexer (DMUX) then converts the high-speed serial data stream into multiple parallel data streams for further digital processing. On the transmitter (TX) side, the data is processed reversely. Parallel lower-speed data from the DSP is combined into a single stream using a multiplexer (MUX). A laser/modulator driver drives the corresponding optoelectronic devices. The laser driver modulates the laser current, while the modulator driver drives the voltage across an optical modulator, which in turn modulates the light intensity from a continuous wave laser.

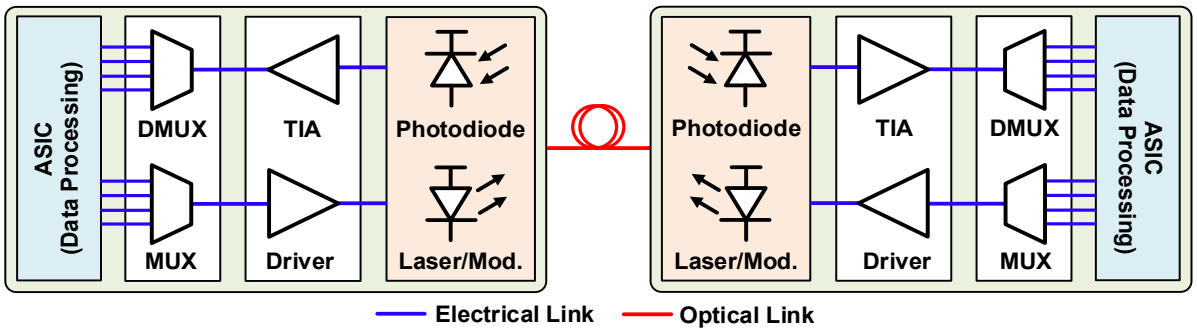


Figure 1.3. System diagram of an IMDD optical interconnect.

A conventional optical link from an application-specific integrated circuit (ASIC) on a host PCB to a pluggable optical engine (OE) with a re-timer or DSP chip is illustrated in Figure 1.4 (a). The host ASIC and the pluggable optical module are connected through electrical traces on

PCB. Inside the pluggable module, it usually includes a DSP chip to convert the interface on the host side, such as 8×50 Gb/s signaling, into an optical interface, such as 4×100 Gb/s signaling, or to convert them in a reverse order [6]. Crucially, the DSP also provides retiming and equalization, as it is too hard to directly connect the link from the ASIC to the optics [7]. During high-speed data transmission, this approach often leads to significant power consumption caused by the DSP and signal loss due to electrical traces on PCB. Generally, the shorter the electrical channel and the fewer the intermediate conversions, the easier it is to manage signal integrity issues. This has driven the trend of integrating optical modules closer to the ASIC, which can effectively reduce power consumption. Two main solutions have emerged based on this principle: co-packaged optics (CPO) and linear pluggable optics (LPO), as shown in Figure 1.4 (b) and (c), respectively. By co-packaging the optical module and the ASIC closely together, CPO technology greatly reduces the distance for signal conversion between electrical and optical domains, as well as the transmission distance. LPO technology places the optical module in a package near the ASIC and replaces DSPs with TIAs and drivers with high linearity and equalization capabilities. Both methods can significantly reduce power consumption, improve signal integrity, and reduce latency.

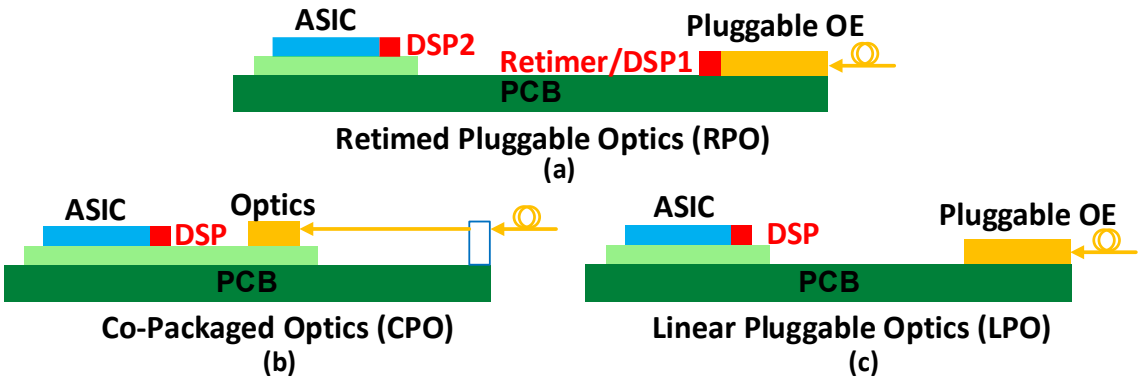


Figure 1.4. (a) Retimed pluggable optics in which an ASIC is placed to a pluggable OE with a re-timer or DSP chip. (b) Co-packaged optics where the optical module is on the same substrate as the ASIC. (c) Linear pluggable optics in which the OE is placed in a package near the ASIC, and the re-timer/DSP is removed.

Furthermore, pluggable front-panel transceivers are often implemented in SiGe BiCMOS circuits, which necessitate separate dies for the front-end blocks and high-speed CMOS ASICs

[8]. Although scaling up with the speed and channels count to meet the throughput demand, these front-panel modules are soon becoming a bottleneck due to heavy cost and power associated with frequency-dependent losses in PCB traces and multiple discrete components in re-timer and buffer circuitry [9], [10]. Integration of front-end modulation driver and TIA and SerDes integrated circuits (ICs) in a single CMOS IC becomes desirable to reduce the length of electrical connections and the number of components as shown in Figure 1.5, hence improving power efficiency and BW density. On the optical receiver (ORX) side, CMOS implementation of linear TIA has already been demonstrated in prior works [11], [12], [13], [14], [15], and the integration of TIA with subsequent SerDes circuits provides additional design choices and flexibility to break design tradeoffs and enhance design capability of the front end by leveraging the characteristics and performance of post-TIA circuits [8], [16], [17], [18], [19], [20].

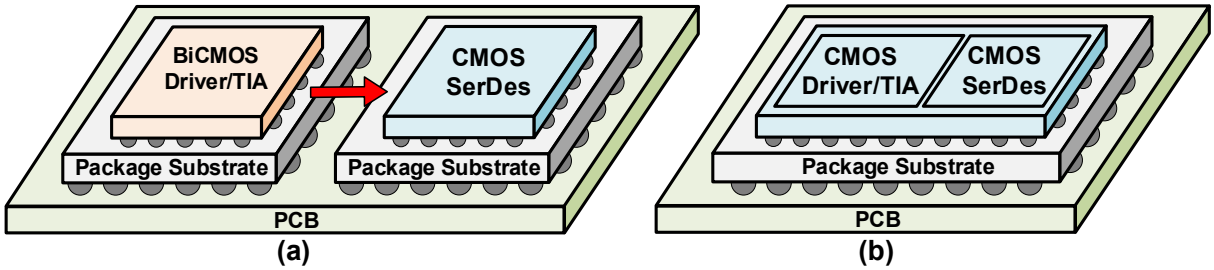


Figure 1.5. (a) Front-panel transceivers implemented in SiGe BiCMOS and (b) integration of CMOS front-end transceivers with SerDes IC.

1.3 Thesis Organization

This thesis focuses on the design of energy-efficient CMOS PAM-4 ORXs for short-reach data center applications, targeting both CPO and LPO scenarios. In Chapter 2, equalization techniques are first introduced, followed by noise analysis and modelling of shunt-feedback (SF) TIAs. ORX sensitivity enhancement using continuous-time linear equalizers (CTLEs), feed-forward equalizers (FFEs), and decision feedback equalizers (DFEs) are further analyzed and simulated. Chapter 3 presents a 1.28-pJ/bit 48-Gb/s inductorless PAM-4 ORX implemented in a 28-nm CMOS technology, featuring a linear TIA integrated with a sampler. The proposed TIA avoids CTLEs and passive inductors, achieving a compact and energy-efficient design. A

FFE and a DFE are implemented at the sampler to compensate for TIA BW, ensuring reliable data recovery. Chapter 4 introduces a 0.32-pJ/bit 100-Gb/s PAM-4 TIA in a 28-nm CMOS technology. The design leverages multi-layer stacked networks, T-coils, and inductors for BW extension and electrostatic discharge (ESD) compensation. By exploiting CMOS scaling and complementary design techniques, the tradeoff between BW, noise, and power is effectively relaxed. Finally, Chapter 5 summarizes the work presented in Chapters 2–4 and discusses potential directions for future research.

Chapter 2

Optical Receiver Sensitivity Enhancement by Equalization

Equalizers are essential in high-speed communication to mitigate signal degradation and imperfections caused by BW limitations and channel nonidealities. In optical interconnect design, equalization techniques not only address BW constraints but also enhance ORX sensitivity. This chapter begins by discussing various equalization schemes on the RX side. Noise analysis is then conducted based on a simplified SF TIA model, and ORX sensitivity enhancement by different equalization techniques are analyzed and demonstrated.

2.1 Optical Receiver Equalization Techniques

2.1.1 Continuous-Time Linear Equalizer (CTLE)

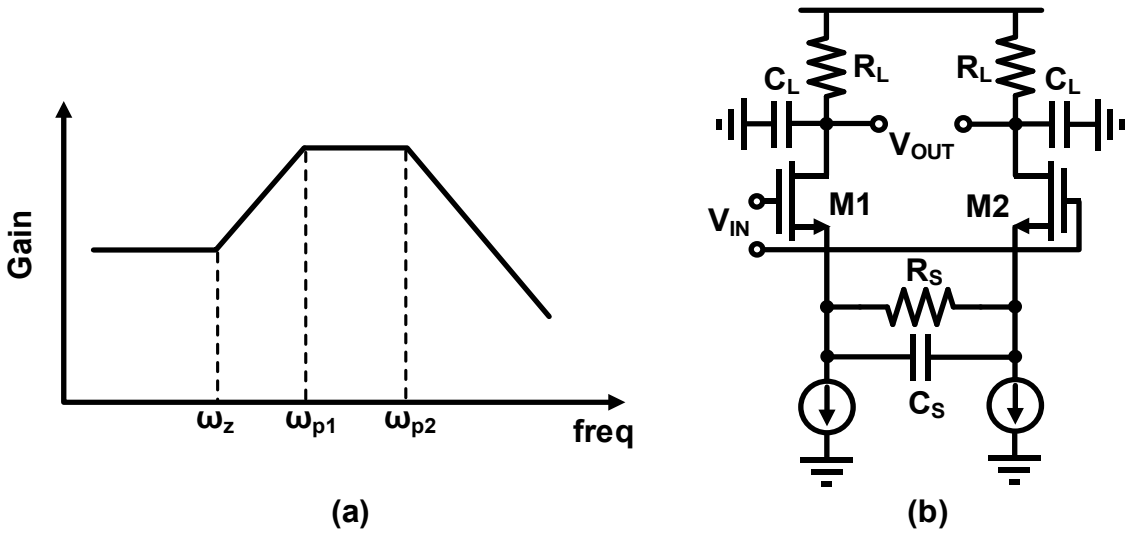


Figure 2.1. (a) Bode plot of a CTLE with one zero. (b) A CTLE circuit using resistive and capacitive degeneration in a differential pair.

CTLE is an analog equalizer that provides gain peaking in order to boost high frequencies. CTLEs are commonly designed in the frequency domain with a transfer function described as,

$$H_{CTLE}(s) = \frac{k(s+z_1)}{(s+p_1)(s+p_2)} \tag{2.1}$$

where z_1, p_1 and p_2 are the zero and poles of the CTLE. Figure 2.1 (a) shows the Bode plot

of a CLTE, where one zero produces a +20 dB/decade rise and two poles produce -20 dB/decade falls in the frequency response. The poles locate the peaking frequency and determine the roll-off of the high frequency response. Filter design techniques using passive or active components can be adopted to design CTLEs. Using resistive and capacitive degeneration in an active differential pair to create high-frequency boosting is one of the most common methods as depicted in Figure 2.1(b), where high-frequency boosting is achieved by introducing real zero using the parallel resistor and capacitor network [21]. The transfer function of the CTLE in Figure 2.1 (b) can be expressed as,

$$H(s) = \frac{g_m}{C_L} \frac{s + \frac{1}{R_S C_S}}{\left(s + \frac{1 + g_m R_S/2}{R_S C_S}\right)\left(S + \frac{1}{R_L C_L}\right)} \tag{2.2}$$

where g_m denotes the transconductance of input transistors M1 and M2. The real zero and poles are given by:

$$\omega_z = \frac{1}{R_S C_S}, \omega_{p1} = \frac{1}{R_L C_L}, \omega_{p2} = \frac{1 + g_m R_S/2}{R_S C_S} \tag{2.3}$$

The dominant pole ω_{p1} is designed to be higher than the zero frequency to realize high-frequency peaking gain, and the peaking gain is controlled by the ratio of the dominant pole and zero frequencies.

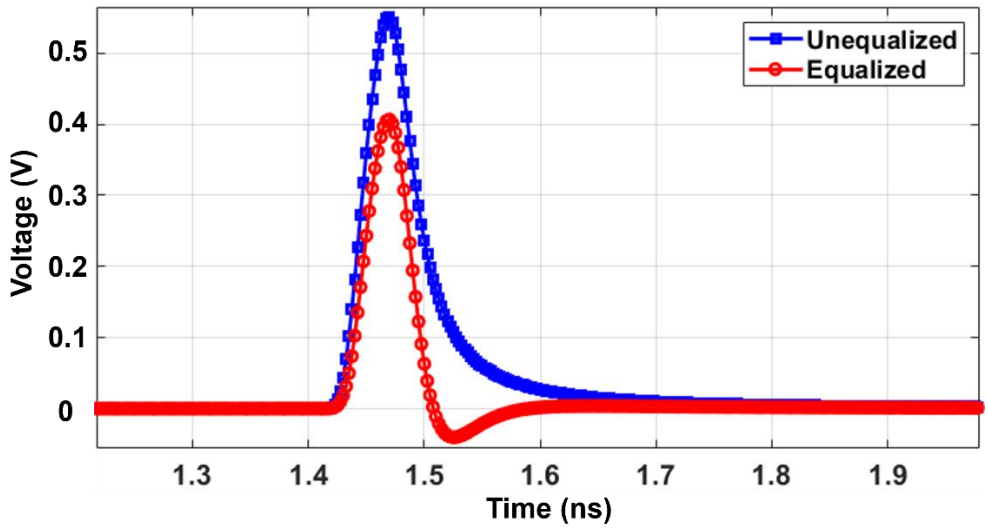


Figure 2.2. Pulse responses of a BW-limited signal and the CTLE-equalized signal.

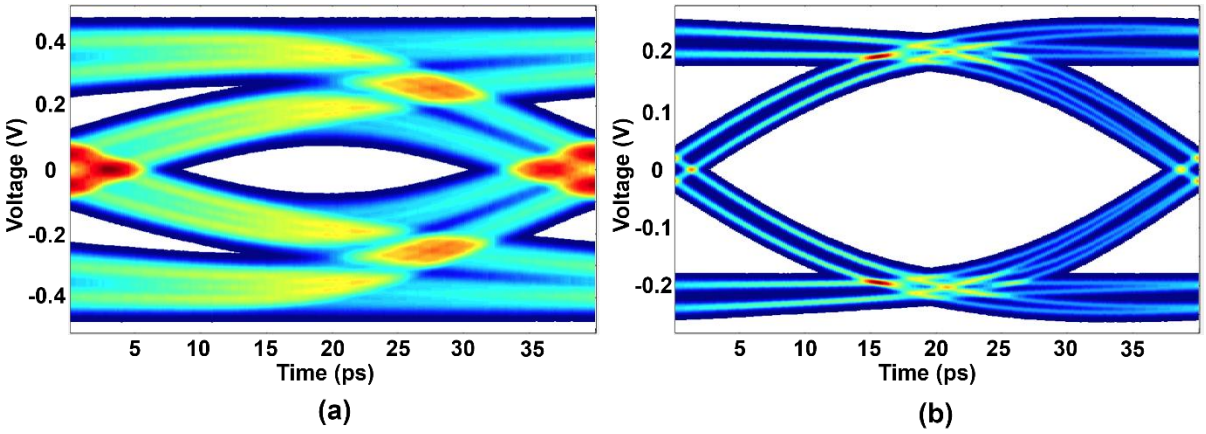


Figure 2.3. Eye diagrams of the signal (a) before and (b) after equalized by the CTLE.

To illustrate the effect of the CTLE, a 25-Gb/s NRZ signal through a channel with 8-dB loss at 10 GHz without and with CTLE is simulated and compared. The CTLE has a peaking frequency of 12.5 GHz, a dc gain of -6 dB, and a peaking gain of 6 dB. The time domain pulse responses (pulse width = 40 ps) of the BW-limited signal and the equalized signal are given in Figure 2.2, where the postcursor of the original pulse is cancelled by the CTLE. The corresponding 1-unity interval (UI) eye diagrams of these two signals are given in Figure 2.3 (a) and (b), respectively, demonstrating a significant improvement in the eye opening.

2.1.2 Feed-Forward Equalizer (FFE)

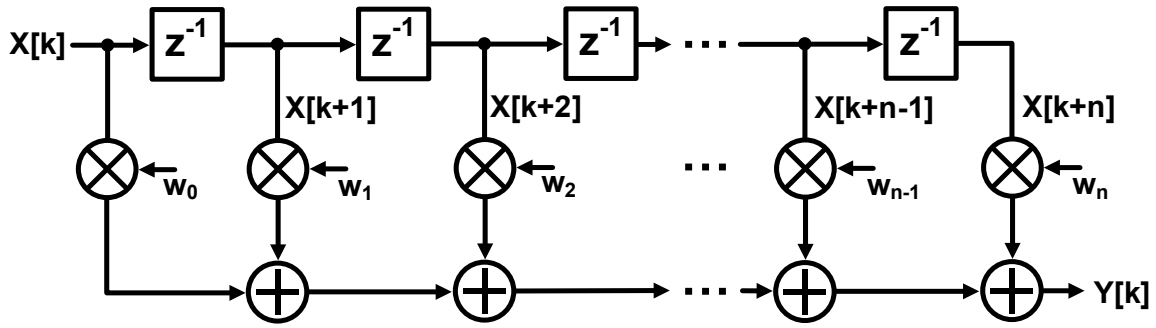


Figure 2.4. Block diagram of a linear n-tap FFE.

A FFE compensates for the signal degradation by amplifying or attenuating specific frequency components of the signal. This technique employs a finite impulse response (FIR) filter with a series of tap weights programmed to adjust the impulse and the frequency response with taps being both precursor and postcursor. The number of taps determines the complexity and

compensation ability of the FIR filter. The block diagram for a linear n-tap FFE is illustrated in Fig. 2.4, and the corresponding transfer function can be given as:

$$Y[k] = \sum_{j=0}^{n} X[k+j] \cdot w[j] \tag{2.4}$$

A FFE is configured to have high-pass characteristics and emphasizes the high-frequency signal components and hence ameliorates the inter-symbol interference (ISI). However, as a linear equalizer, the noise and crosstalk are also high-pass-filtered and amplified by the FFE. For analog implementations on the RX side, a number of delayed versions of input signal are generated using delay lines or multi-phase sampling and are added back at an analog summer with proper weights for summing or subtracting operations.

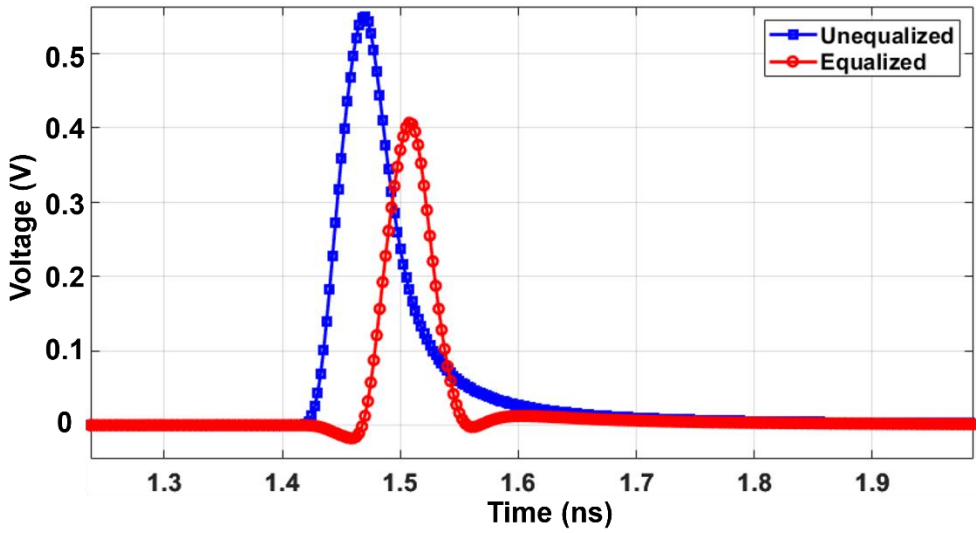


Figure 2.5. Pulse responses of a BW-limited signal and the FFE-equalized signal.

The 25-Gb/s NRZ signal described in 2.1.2 is also simulated and compared here to illustrate the effect of the FFE. A 3-tap FFE is used with a precursor of -0.05, main cursor of 1, and postcursor of -0.26. The time domain pulse responses of the BW-limited signal and the equalized signal are given in Figure 2.5, where both the precursor and the postcursor of the original pulse are cancelled by the FFE. The corresponding 1-UI eye diagrams of these two signals are given in Figure 2.6 (a) and (b), respectively, demonstrating a significant improvement in the eye opening.

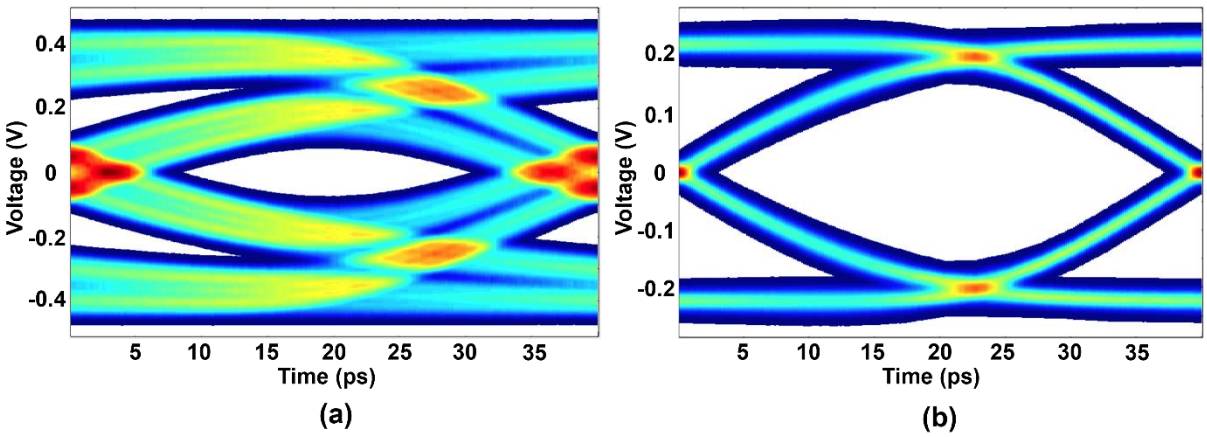


Figure 2.6. Eye diagrams of the signal (a) before and (b) after equalized by the FFE.

2.1.3 Decision Feedback Equalizer (DFE)

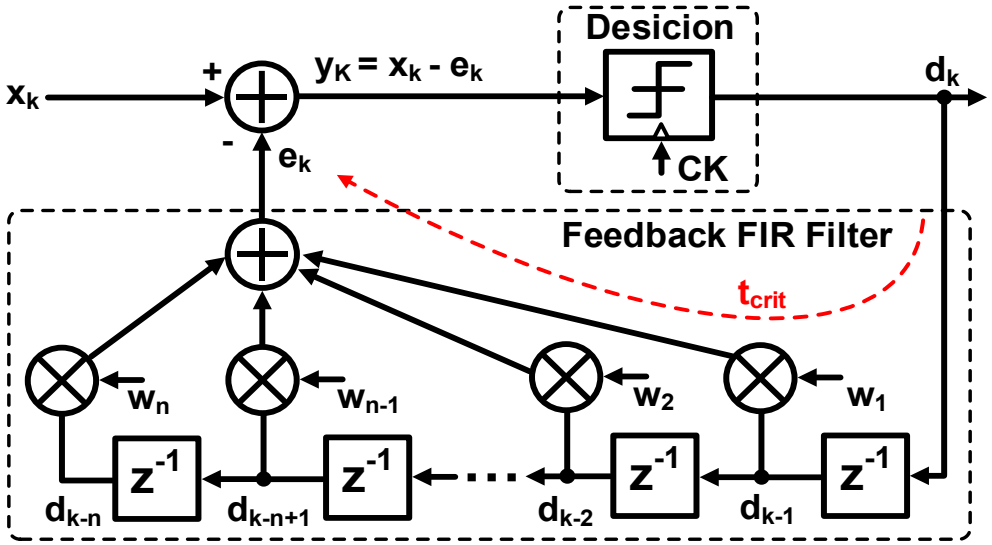


Figure 2.7. Block diagram of a n-tap direct DFE.

A DFE is a kind of nonlinear equalizer that uses a weighted sum of past decision(s) to cancel the ISI caused by previously detected symbols on the current symbol [22]. In effect, the distortion caused by previous pulses on the current pulse is subtracted. The block diagram of a n-tap DFE is depicted in Fig. 2.7, in which the decision function is also realized by a comparator, and postcursor ISI appearing in the uncompensated pulse response can be mitigated by the feedback signal. With an n-tap feedback FIR filter incorporated, an n-tap DFE can be built, enabling the compensation for n-tap post-cursor ISI. The corresponding transfer function can be expressed as

$$y_k = x_k - \sum_{j=0}^{n} d_k \cdot w_k \tag{2.5}$$

The key advantage of a DFE is that the feedback signal is a quantized symbol level, which prevents the amplification of noise and crosstalk that occurs in the CTLE and FFE topologies [23]. Nevertheless, unlike a FFE, the DFE can only cancel postcursor ISI because the subtraction is performed on the arriving symbols after the decision. In addition to clock phase alignment and proper setting of feedback taps, a major difficulty faced in DFE implementations is dealing with the total loop delay to meet the critical timing associated with feeding back the previous symbol decisions, which is denoted as t_{crit} in Figure 2.7 with the red dashed line. The DFE architecture in Figure 2.7 falls into the category of direct DFE, and the timing constraint in such a direct DFE design can be expressed as:

$$T_{CKQ} + T_{settle} + T_{setup} < 1\ UI \tag{2.6}$$

where T_{CKQ} is the clock-to-Q delay of the slicer, T_{settle} is the settling time of the summer, and T_{setup} is the setup time of the slicer. Similar speed limitations exist in other variants of this architecture as well. Another drawback of the DFE is that decision errors tend to propagate at future decisions due to residual ISI and a reduced margin against noise [24].

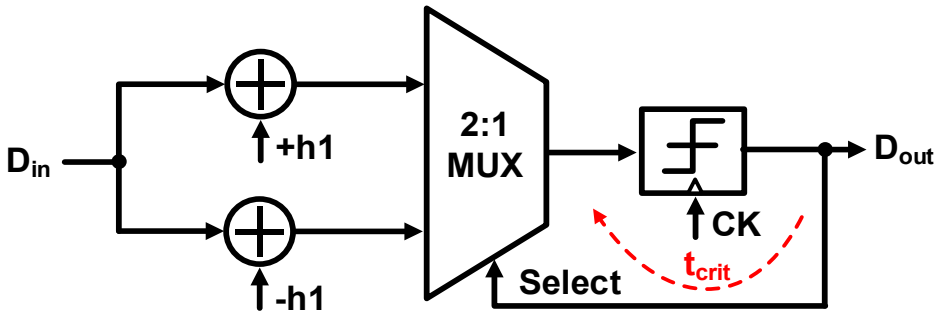


Figure 2.8. Block diagram of a 1-tap loop-unrolled DFE.

By transforming the feedback loop of Figure 2.7 to a predictive or “unrolled” topology, an alternative loop-unrolled (speculative) DFE architecture can be obtained as shown in Figure 2.8, which slightly relaxes the timing constraint of the first DFE tap to:

$$T_{CKQ} + T_{setup} + T_{MUX} < 1\ UI \tag{2.7}$$

where T_{MUX} denotes the delay from the select input of the MUX to its output and is usually smaller than T_{settle} in Eq. (2.6). However, for loop-unrolled DFE, the number of required slicers increases exponentially with the number of taps unrolled. If DFE is designed with n taps loop-unrolled in NRZ systems, the demand for 2^n slicers is required. Such hardware cost and power consumption are much more severe for a system with high-order modulation formats. For example, realizing an n-tap loop-unrolled DFE in PAM-4 systems leads to the required number of slicers to be proportional to 4^n.

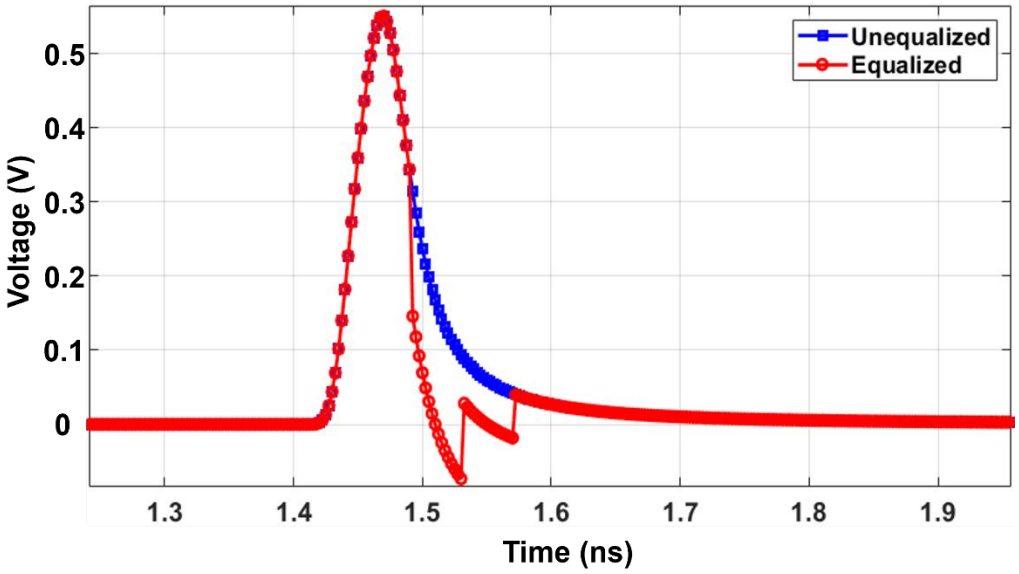


Figure 2.9. Pulse responses of a BW-limited signal and the DFE-equalized signal.

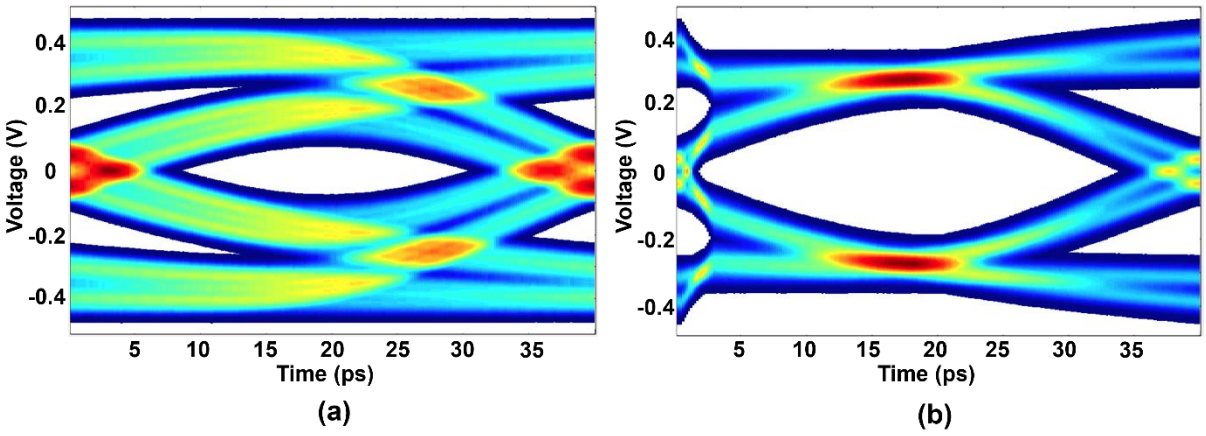


Figure 2.10. Eye diagrams of the signal (a) before and (b) after equalized by the DFE.

To demonstrate the impact of the DFE, a 25-Gb/s NRZ signal is simulated using a 2-tap DFE with postcursor coefficients of -0.17 (first tap) and -0.06 (second tap). Figure 2.9 compares the time-domain pulse responses of the BW-limited signal and the equalized signal, showing the effective cancellation of postcursor interference by the DFE. The nonlinear behavior of the DFE is also evident in the pulse responses. The corresponding 1-UI eye diagrams are presented in Figure 2.10 (a) and (b), respectively, demonstrating a significant improvement in the eye opening.

2.2 SF TIA Noise Analysis

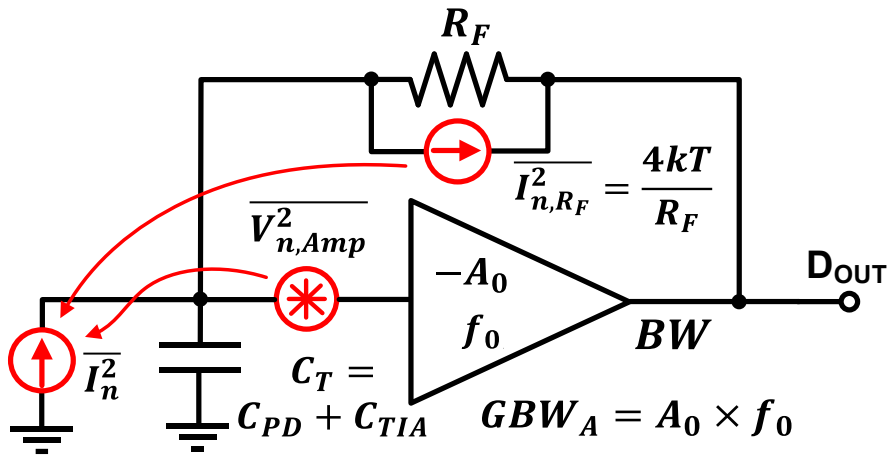


Figure 2.11. Illustration of noise contributions in SF TIA.

The overall achievable sensitivity in high-speed ORXs is usually limited by the noise performance of the TIA. Considering SF TIA which is the most common TIA circuit topology in deep sub-micron CMOS technology [14], [25], [26], a simplified SF TIA model is depicted in Figure 2.11, which consists of a feedback resistor R_F and a feed-forward amplifier with a gain and BW of A_0 and f_0 respectively. When accounting for the impact of finite BW of the feed-forward amplifier at high data rate, the transimpedance of TIA has a second-order response given by [27]

$$Z_T(s) = \frac{R_F A}{1+A} \times \frac{1}{1 + s/(\omega_0 Q) + s^2/\omega_0^2} \approx \frac{R_F}{1 + s/(\omega_0 Q) + s^2/\omega_0^2} \qquad (2.8a)$$

$$\omega_0 = \sqrt{\frac{(1+A)\omega_A}{R_F C_T}} \tag{2.8b}$$

$$Q = \frac{\sqrt{(1+A)\omega_A R_F C_T}}{1 + R_F C_T \omega_A} \tag{2.8c}$$

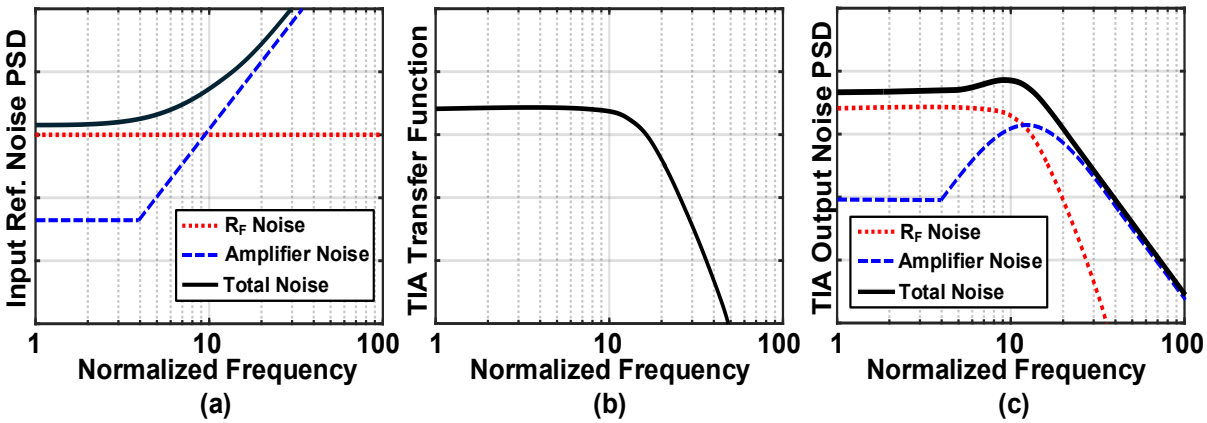


Figure 2.12. SF TIA (a) input referred current noise PSD, (b) magnitude frequency response, and (c) output voltage noise PSD.

For maximally flat TIA magnitude (Butterworth) response, $Q = 1/\sqrt{2}$, and the TIA BW (BW_{3dB}) can be expressed using Eq. (2.8b) and (2.8c) as [27]

$$BW_{3dB} = \frac{\sqrt{2A(A+1)}}{2\pi R_F C_T} \approx \frac{\sqrt{2}A}{2\pi R_F C_T} \tag{2.9}$$

The feedback resistance, R_F, needed to achieve the Butterworth response can be calculated as

$$R_F = \frac{(A+1)\omega_A}{C_T BW_{3dB}^2} \approx \frac{GBW_A}{2\pi C_T BW_{3dB}^2} \tag{2.10}$$

where C_T is the total capacitance at TIA input node consisting of the PD capacitance (C_{PD}) and TIA input capacitance (C_{TIA}), and GBW_A is the gain-BW product of the feed-forward amplifier. As shown in Eq. (2.10), R_F decreases quadratically with BW_{3dB}. If GBW_A and C_T keep constant and BW_{3dB} becomes n time smaller, then R_F becomes n^2 time larger, Eq. (2.9) shows A_0 is n

time larger, and f_0 is n time smaller. The main noise contributors of SF-TIA are R_F and the feed-forward amplifier as illustrated in Figure 2.12 (a). When referred to the TIA input, noise from R_F appears as white noise while the feed-forward amplifier voltage noise has both f^2 noise and white noise. The input-referred current noise power spectral density (PSD) can be expresses as [18]

$$\overline{i_{n,in,SF}^2}(f) = \overline{i_{n,RF}^2}(f) + \overline{i_{n,amp}^2}(f) = \frac{4kT}{R_F} + \frac{4kT\gamma}{g_m R_F^2} + 4kT\gamma \times \frac{(2\pi C_T)^2}{g_m} \times f^2$$

$$\approx \frac{4kT}{R_F} + 4kT\gamma \times \frac{(2\pi C_T)^2}{g_m} \times f^2 \tag{2.11}$$

where g_m is the transconductance of input MOSFETs of the feed-forward amplifier. The output voltage noise PSD of the TIA can be calculated by multiplying $\overline{i_{n,in,SF}^2}(f)$ by the squared magnitude of TIA transfer function as illustrated in Figure 2.12 (b) and (c). The total input referred current noise power can be expressed as [27]

$$\overline{i_n^2} = \frac{4kT}{R_F} \times I_1 BW_{3dB} + 4kT\gamma \times \frac{(2\pi C_T)^2}{g_m} \times \frac{I_2^3}{3} BW_{3dB}^3 \tag{2.12}$$

where γ is the channel-noise factor, and two Personick integral numbers $I_1 = 1.11$ and $I_2 = 1.49$ are for Butterworth response. The first term in Eq. (2.12) is due to R_F and the second term is due to feed-forward amplifier which is minimized when $C_{PD} = C_{TIA} = 0.5C_T$. In such case, $\overline{i_n^2}$ can be expressed as [27]

$$\overline{i_n^2} = 4kT \frac{2\pi C_T}{f_T} BW_{3dB}^3 \times \left(I_1 \times \frac{f_T}{GBW_A} + \frac{I_2^3}{3} \times 2\gamma \right) \tag{2.13}$$

Eq. (2.13) shows that the noise increases cubically with BW_{3dB}. If GBW_A is fixed to be $f_T/3$, and $C_{PD} = C_{TIA} = 80\,fF$, then using Eq. (2.9) (2.10) and (2.13), the TIA second order frequency response can be determined by BW_{3dB}/n and f_0/n, and the noise at different BW_{3dB} can be calculated and modelled. In Chapter 3, the SF TIA noise-BW relationship here will be extended to the ORX link to further evaluate the sensitivity enhancement of different post-TIA equalizations.

2.3 Sensitivity Enhancement by Equalization

2.3.1 CTLE-Equalized SF TIA

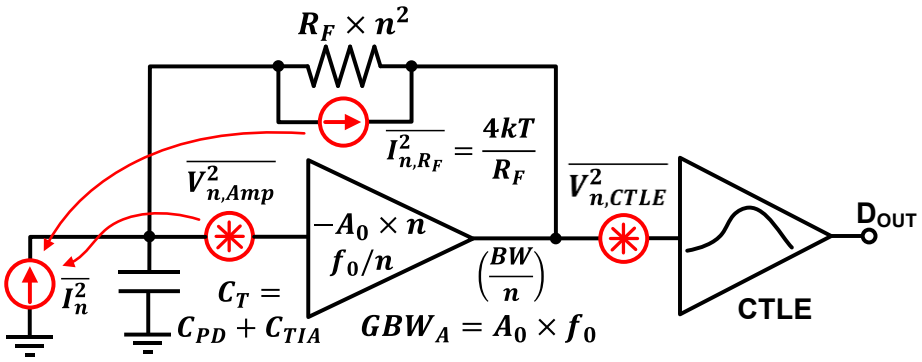


Figure 2.13. CTLE-equalized SF TIA design where a low-BW TIS is followed by a BW recovering CTLE.

A low-noise design approach is illustrated in Figure 2.13, where the first stage is a low-BW transimpedance stage (TIS) followed by a CTLE to recover the required BW and reduce the ISI of the first stage [28]. The noise reduction insight with the approach considered can be explained as follows. Assuming $R_F n^2$ as feedback resistor now and the overall BW remains the same as the single SF TIA with a feedback resistor R_F, then the input-referred noise PSD of the CTLE-equalized SF-TIS $\overline{i^2_{n,in,SF}|_{CTLE}}(f)$ can be calculated as:

$$\overline{i^2_{n,in,SF}|_{CTLE}}(f) = \frac{4kT}{R_F n^2} + \frac{4kT\gamma}{g_m R_F^2 n^4} + 4kT\gamma \times \frac{(2\pi C_T)^2}{g_m} \times f^2 + \frac{4kT\gamma}{g_{m.eq}|Z_T|^2}$$

$$= \frac{4kT}{R_F n^2} + \frac{4kT\gamma}{g_m R_F^2 n^4} + 4kT\gamma \times \frac{(2\pi C_T)^2}{g_m} \times f^2 + \frac{4kT\gamma}{g_{m.eq} R_F^2 n^4} + \frac{4kT\gamma}{g_{m.eq} R_F^2 n^4}\left(\frac{f}{BW_{3dB}/n}\right)^4$$

$$= \frac{4kT}{R_F n^2} + \frac{4kT\gamma}{g_m R_F^2 n^4} + 4kT\gamma \times \frac{(2\pi C_T)^2}{g_m} \times f^2 + \frac{4kT\gamma}{g_{m.eq} R_F^2 n^4} + \frac{4kT\gamma}{g_{m.eq} R_F^2}\left(\frac{f}{BW_{3dB}}\right)^4$$

$$\approx \frac{4kT}{R_F n^2} + 4kT\gamma \times \frac{(2\pi C_T)^2}{g_m} \times f^2 \qquad (2.14)$$

where $g_{m.eq}$ stands for the transconductance of input transistors of CTLE. Eq. (2.10) and (2.14) indicate that if the factor n is increased, then all the white noise terms can be reduced, while the f^2 and f^4 color noise terms remain unchanged. As a result, such a low noise design

approach boils down to a trade-off between the choice of the increasing factor n and equalization capability of the CTLE. A large n resulting in reduced TIS BW necessitates a higher peaking from the CTLE to recover overall targeted BW, imposing more stringent demand on the design of CTLEs. Figure 2.14 further illustrates the noise contributions and reduction of the two equations in logarithmic scale. As long as the equalizer can recover a given BW, this approach significantly reduces the white noise, and the colored noise almost remains the same. Input referred noise of a SF-TIA with its BW well equalized and restored by a CTLE can be calculated as

$$\overline{i_{n,in,SF}^2|_{CTLE}} = 4kT\frac{2\pi C_T}{f_T}BW_{3dB}^3 \times \left(\frac{I_1}{n^3} \times \frac{f_T}{GBW_A} + \frac{I_2^3}{3} \times 2\gamma\right) \tag{2.15}$$

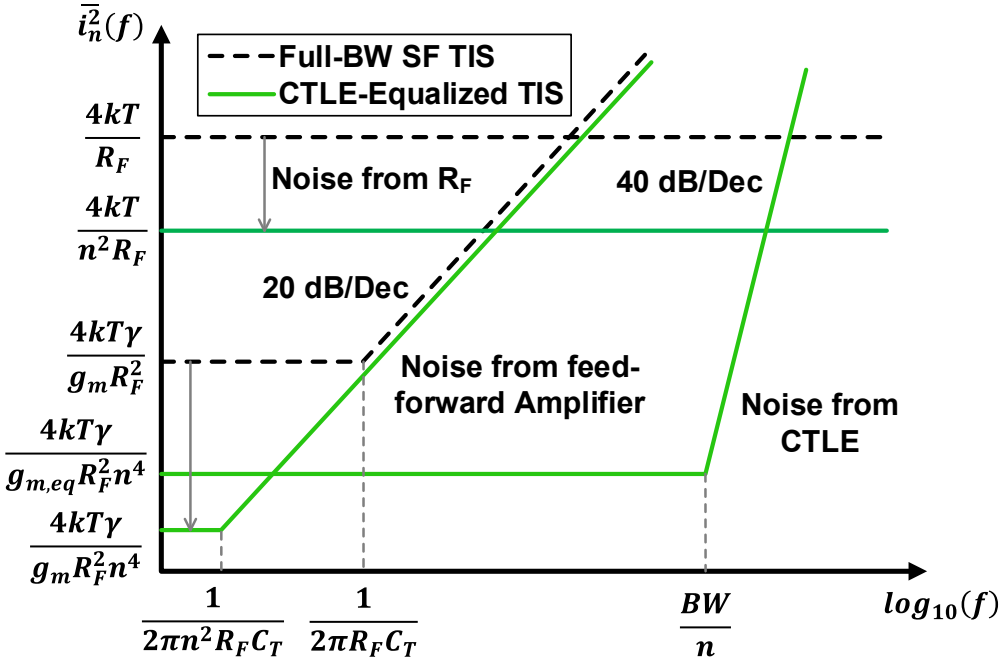


Figure 2.14. Illustration of input-referred noise of a CTLE-equalized SF TIA.

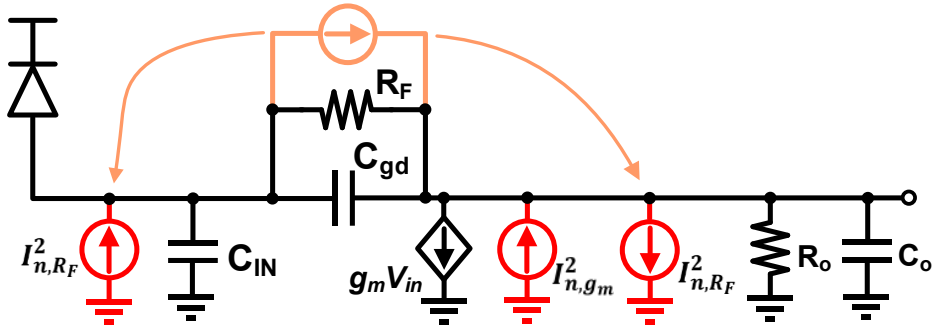


Figure 2.15. Small-signal model of TIS for calculating the output noise.

Again, compared with Eq. (2.13), Eq. (2.15) reveals that CTLE helps reduce R_F noise contribution by n^2 but does not affect the noise from the feed-forward amplifier. The transfer functions of TIS and CTLE are further derived to calculate the output RMS noise for simulation and analysis. The TIS transfer function is first derived using the small-signal model as shown in Figure 2.15, where the thermal noise from R_F is split at input and output [29]. The second-order TIS transfer function Z_{TIS} and its output impedance Z_o can be derived as

$$Z_{TIS}(s) = \frac{-R_o(g_m nR_F - 1 - sC_{gd}nR_F)}{1 + g_m nR_F + sK_1 + s^2K_2} \tag{2.16}$$

$$Z_o(s) = \frac{R_o[1 + snR_F(C_{gd} + C_{IN})]}{1 + g_m nR_F + sK_1 + s^2K_2} \tag{2.17}$$

where $K_1 = C_{IN}(R_o + nR_F) + C_oR_o + C_{gd}nR_F(1 + g_mR_o)$, and $K_2 = nR_FR_o(C_{IN}C_o + C_{IN}C_{gd} + C_{gd}C_o)$. The transfer function of an ideal unity-gain CTLE stage that recovers the full BW is given as

$$H_{CTLE}(s) = \frac{1 + g_mR_F + sK_1 + s^2K_2}{(1 + g_mR_a)\left(1 + \frac{s}{nQ2\pi f_{TIS}} + \frac{s^2}{(n2\pi f_{TIS})^2}\right)} \tag{2.18}$$

Eq. (2.18) is written as a second-order system with a quality factor of Q. Zeros of the CTLE cancels poles of the TIS. The noise PSD at CTLE output can be obtained by multiplying the R_F thermal noise term $I^2_{n,R_F} = 4kT/nR_F$ and channel thermal noise term $I^2_{n,g_m} = 4kT\gamma g_m$ with the corresponding transfer functions

$$S_{CTLE,out}(s) = I^2_{n,R_F}|(Z_{TIS} - Z_o) \times H_{CTLE}|^2 + I^2_{n,g_m}|Z_o \times H_{CTLE}|^2 \tag{2.19}$$

And the RMS noise at CTLE output can be calculated as square root of the integrated PSD

$$V_{noise,out} = \sqrt{\int_0^\infty S_{CTLE,out}(s)df} \tag{2.20}$$

The SNR at CTLE-equalized TIA output is defined as the ratio of the worst PAM-4 eye opening V_{ISI} to the RMS noise $V_{noise,out}$

$$SNR = 20log_{10}\left(\frac{V_{ISI}}{V_{noise,out}}\right) \tag{2.21}$$

V_{ISI} is calculated using peak distortion analysis modified for PAM-4 format [29]

$$V_{ISI} = |V_0| - 3\sum_{i\neq 0}|V_i| \tag{2.22}$$

Where V_0 is the main cursor and V_i is the i_{th} pre/post cursors. After that, the SNR as a function of R_F scaling factor n is plotted as Figure 2.16. The quality factor Q is kept $1/\sqrt{2}$. The signal to R_F noise ratio and signal to channel noise ratio are also plotted for comparison. Figure 2.16 reveals that SNR improves as n increases, but when n is larger than 3, channel noise becomes dominated, and the SNR improvement is not pronounced.

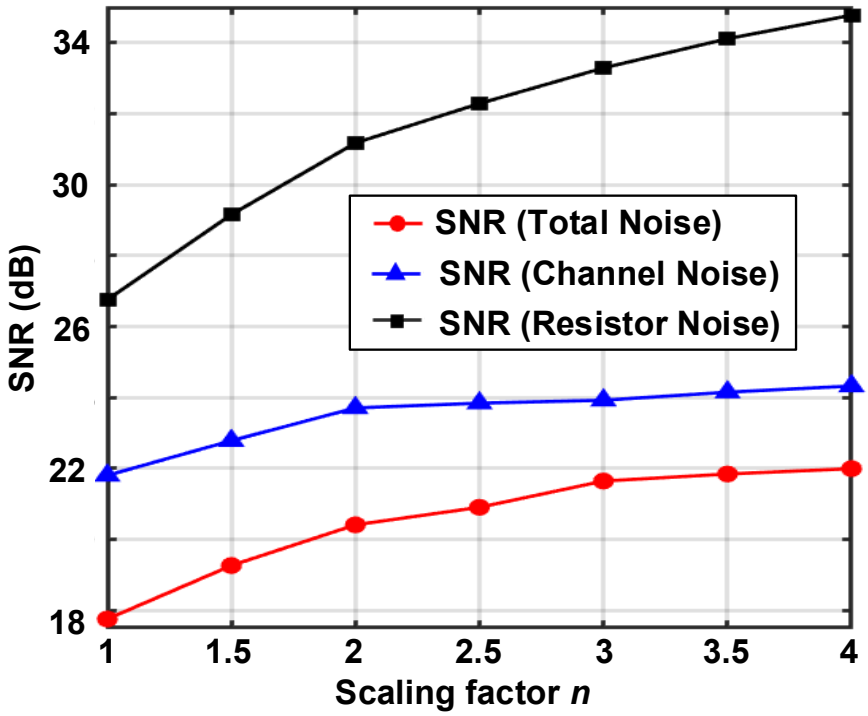


Figure 2.16. Simulated SNR with different scaling factor n.

If the CTLE is not well-designed, over or under peaking would happen which also affects the TIA noise. Figure 2.17 depicts the simulated CTLE-equalized TIA responses with scaling factor n kept 3 under different Q values to demonstrate the under/over peaking. The SNR as a function of quality factor Q is also simulated and plotted as Figure 2.18. The over or under peaking degrades the SNR, but if the variation of Q is less than 15%, the SNR degradation is less than 2 dB. As a result, peaking tunability is also required for CTLE design.

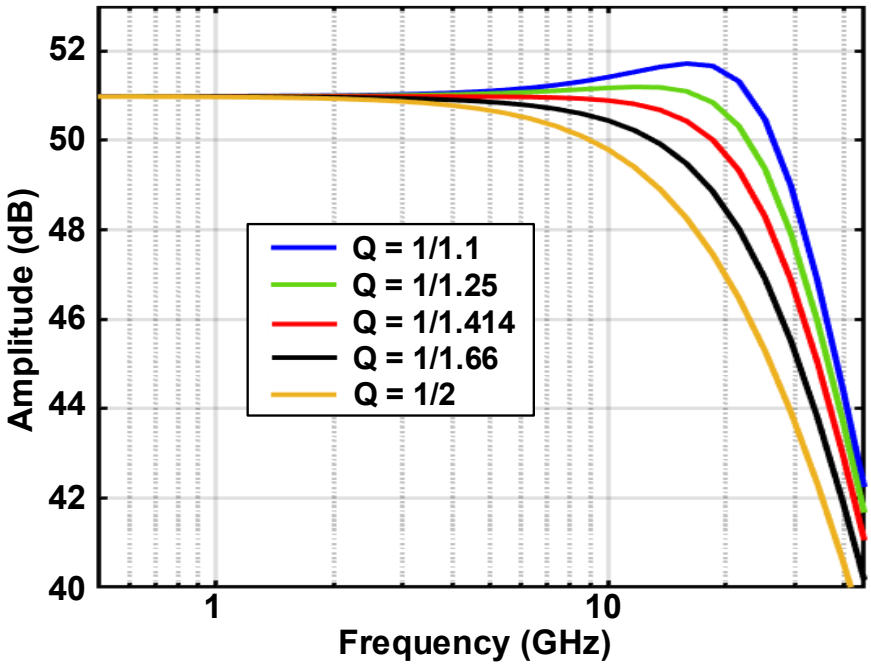


Figure 2.17. Simulated CTLE-equalized TIA responses under different Q values.

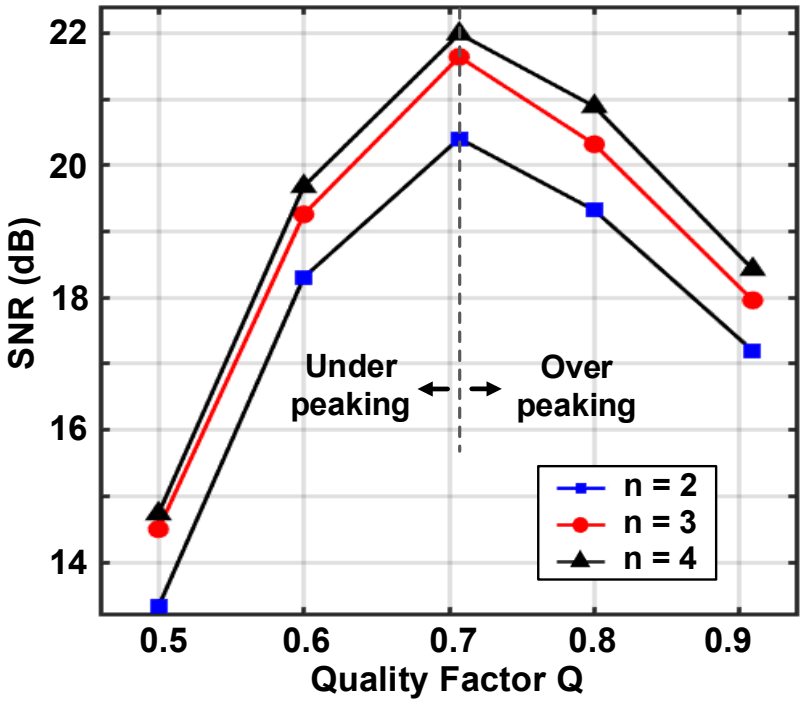


Figure 2.18. Simulated SNR with different Q values.

Increasing R_F results in a reduced $BW_{3dB,TIS}$, which in turn implies that higher peaking from CTLEs is required to recover overall targeted BW. Nevertheless, CTLE with its first-order peaking response (one zero and two poles) cannot adequately compensate for loss introduced by the second-order TIS response profile without introducing in-band peaking. Any such

peaking, however, results in TIA noise enhancement and degrades receiver sensitivity [18]. Therefore, design iterations and optimizations are required to find the right balance between R_F value and the extent to which CTLE is capable of recovering the desired BW.

2.3.2 SF TIA with Post-TIA Equalization

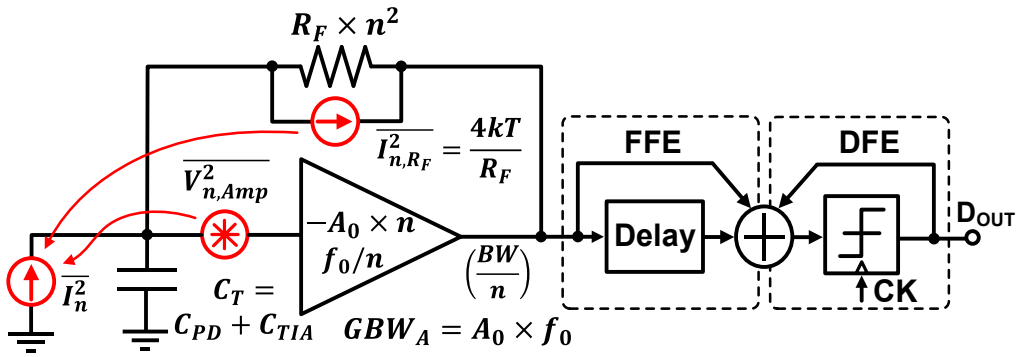


Figure 2.19. ORX design with post-TIA equalizers.

Conventionally, higher data rates in ORXs are achieved by extending the front-end TIA BW using techniques like CTLEs or passive inductive peaking. On the other hand, as an alternative approach, low-noise, high-gain, and low power CMOS ORXs can be designed by reducing the BW of entire TIA, followed by equalization techniques such as FFEs and DFEs as illustrated in Figure 2.19. Reducing TIA BW can help lower its input-referred noise, albeit at the cost of increased ISI. If the ISI penalty can be compensated at the subsequent equalizer with minimal noise penalty, the overall ORX sensitivity can be improved [16]. This approach is particularly attractive and advantageous for ORXs where the TIA and SerDes circuits are integrated into a single CMOS IC.

For NRZ ORX, the sensitivity is limited by TIA noise for BWs larger than 0.5x data rate and by ISI for smaller BWs, demonstrating a fundamental tradeoff between noise and ISI [18]. For PAM-4 ORX, the bit error rate (BER) using a BW-limited TIA with post-TIA equalization can be determined by evaluating the combined impact of noise and ISI. The model in Figure 2.20 is used to explore the effectiveness of post-TIA equalization at 50-Gb/s PAM-4 data rate. A 25-GHz E/O modulator and a 25-GHz PD with a sensitivity of 0.75 A/W are included in the signal path as additional BW-constrained elements. The SF TIA is modelled with a second-order

response, and the noise is calculated based on the BW-noise relationship in section 2.2, followed by the FFE and DFE. Parasitic capacitance of 160 fF and 20 fF are added at input and output of the TIA, respectively. Since it is known that high-frequency jitter is amplified in BW-limited systems, it is important to comprehend this effect when computing the optimal TIA BW. 1-ps random jitter (RJ) and 1.5-ps-pp duty cycle error (DJ) are added at the input of E/O modulator. Latch noise and offset (7 mV in total) are also considered and included in the model.

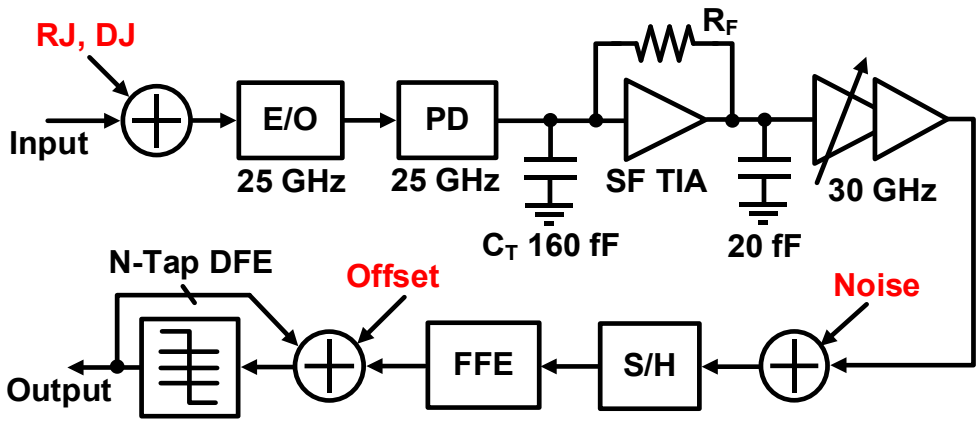


Figure 2.20. ORX model used to evaluate post-TIA equalizations.

Figure 2.21 illustrates the simulated PAM-4 ORX sensitivity across various post-TIA equalization configurations using a comprehensive model, with TIA BWs normalized to the data rate. For the 3-tap FFE, both a 1-tap precursor and a 1-tap postcursor are used, while in other cases, only a 1-tap precursor is employed. For TIA BWs smaller than 0.45x Baud rate, the sensitivity is primarily limited by ISI, thus both FFEs and DFEs help improve sensitivity, but a combination of a FFE and a DFE shows better improvement than the FFE only. Conversely, for TIA BWs exceeding 0.45x baud rate, noise becomes the dominant limiting factor. Here, the nonlinear DFE demonstrates superior performance compared to the linear FFE, with the combination of a 2-tap FFE and a 2-tap DFE achieving the best results. Although the sensitivity improvement at high TIA BWs is not markedly pronounced compared to using the DFE alone as shown in Figure 2.17, the 2-tap FFE + 2-tap DFE configuration is still preferred in this design because the ISI in both precursor and postcursor can be cancelled, and it leaves more flexibility and margin for TIA design. Besides, adding one-tap FFE and a second-tap DFE to a time-

interleaved ORX does not impose significant overhead.

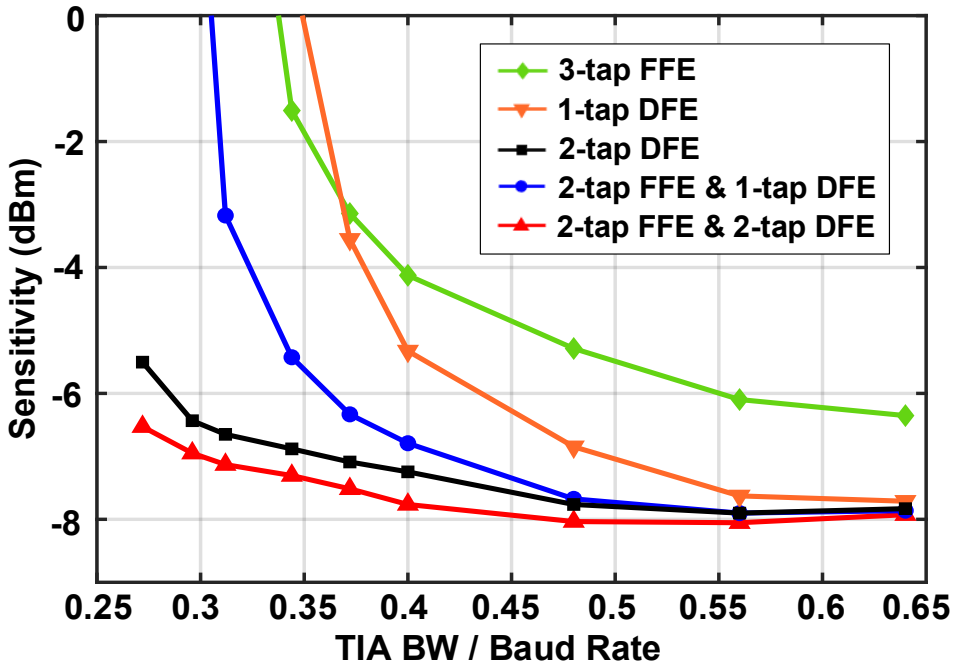


Figure 2.21. Simulated PAM-4 ORX sensitivity with different configurations of post-TIA equalizations.

Chapter 3

A 1.28-pJ/bit 48-Gb/s Inductorless PAM-4 Optical Receiver

3.1 Overview

The growing demand for high-bandwidth memory (HBM) and silicon photonics-based interconnects drives the need for power-efficient, low-latency, and high-density multi-channel optical interfaces. As introduced in Chapter 1, integrating CMOS serializers and samplers with optical interface electronics enhances BW density and power efficiency, making it particularly suitable for short-reach data center applications, as illustrated in Figure 3.1. Prior works have demonstrated the feasibility of integrating TIAs with subsequent SerDes circuits, which provides additional design choices and flexibility to break design tradeoffs and enhance design capability of the front end by leveraging the characteristics and performance of the subsequent circuits.

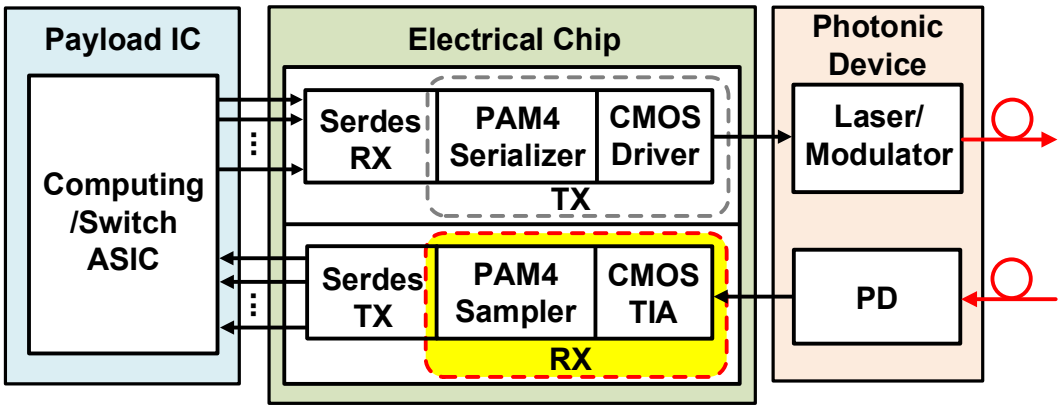


Figure 3.1. Integration of front-panel transceivers with SerDes circuits in a single CMOS IC.

The inherent tradeoffs between gain, noise, BW, and linearity make the power-efficient, low-latency, and high-density PAM4 ORX design highly challenging. As illustrated in Figure 3.2, to break the tradeoffs, a two-stage front-end design method using the CTLE in the TIA to compensate for low-BW TIS is proposed in [28]. At 25-Gb/s, this approach achieves significant noise reduction compared to a single-stage TIA. However, the CTLE has limited ability to

compensate for multiple TIA poles, as excessive compensation can cause in-band peaking and introduce high-frequency noise. Additionally, CTLEs become increasingly power-hungry at higher data rates. For instance, [15] employs a 2-stage CTLE to boost the TIA BW up to 32-GHz in 16-nm CMOS, while resulting in a power efficiency of 0.69-pJ/bit. Inductive multi-peaking scheme is another common technique in TIA design [30], [31], but its use of passive inductors poses challenges for compact and high-density implementations due to their large area and limited tunability. For example, [11] demonstrates an impressive BW of 60 GHz in 28-nm CMOS using various inductive peaking techniques, but at the cost of ~0.25 mm^2 area and 0.96-pJ/bit power efficiency.

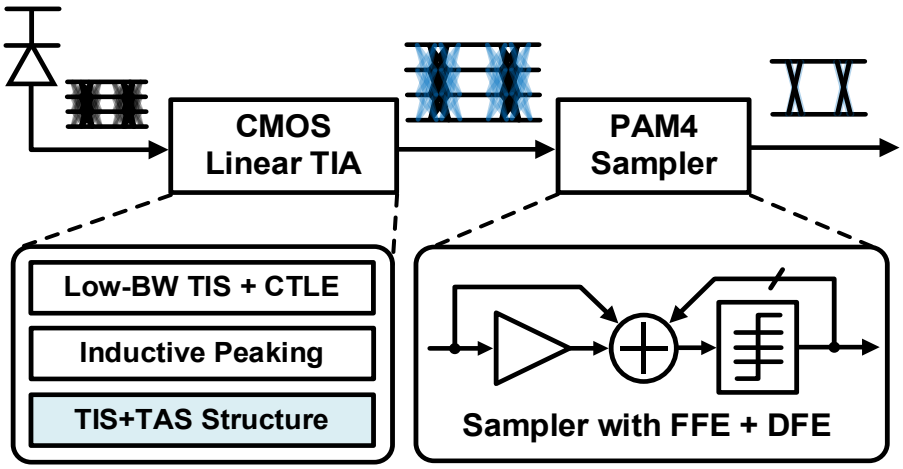


Figure 3.2. Integrated CMOS linear TIA and PAM-4 sampler with the FFE and the DFE.

Integrating the equalizer into the sampler, rather than the TIA, provides an alternative approach for ORX design, as depicted in Figure 3.2. Previous works, such as [8], [17] and [18], have demonstrated the integration of TIA and sampler with DFEs to address the noise-BW tradeoff, though these designs are limited to NRZ signaling. For instance, [8] combines a low-BW TIA with a 4-tap DFE in 65-nm CMOS, and a very good sensitivity of –16.8 dBm is achieved, but the data rate is limited to 12 Gb/s and the 1.9-pJ/bit energy efficiency is still too high. To support PAM-4 modulation, [16], [19], and [20] further extend this approach by integrating linear TIAs with post-TIA equalizers. However, all these PAM-4 designs suffer from high power consumption and area inefficiency, making them unsuitable for high-density multi-channel optical links. For example, [20] implements a 32-Gb/s PAM-4 ORX in 40-nm CMOS

by combining a TIA with a 2-tap DFE. However, the use of a three-stage cascaded amplifier-based TIA, a three-stage cascaded variable gain amplifier (VGA), and a CTLE with inductive peaking results in a high energy efficiency of 4.59-pJ/bit and a rather large area of 0.029 mm^2. Similarly, [16] achieves the first 100-Gb/s PAM-4 ORX in 28-nm CMOS by designing a low-BW TIA followed by a PAM-4 sampler including a 2-tap FFE and a 2-tap DFE. While the ORX achieves high data rate and good sensitivity, and a distributed current-integrating summer helps close the DFE loop. Nevertheless, the four-stage pre-amplifier and the three-stage post-amplifier (post-amp) with series and shunt peaking in the TIA design and the current-integrating summer contribute a 3.9-pJ/bit power efficiency and an area of 0.45 mm^2, highlighting the challenges in balancing speed, power, and area.

In this chapter, a CMOS linear TIA is integrated with a PAM-4 sampler into a single CMOS IC as illustrated in Figure 3.2. The TIA employs a transadmittance-stage transimpedance-stage (TAS-TIS) topology to replace conventional current-mode logic (CML)-based VGA and post-amp, avoiding CTLE and inductors while preserving linearity and a high gain-BW product for PAM-4 operation. The sampler incorporates a 2-tap FFE and a 2-tap DFE to relieve ISI from the TIA, ensuring correct data recovery, providing favorable data-rate density, and achieving superior energy efficiency among TIA and ORX designs. Timing criteria of DFE loop is achieved up to 30 GBaud by optimizing the clock-to-Q delay of slicers. The proposed ORX is implemented in a 28-nm CMOS technology and is wire-bonded to a commercial PD. Optical measurement results at 48-Gb/s PAM-4 show the ORX achieves -5.1-dBm sensitivity at 2.4e-4 BER consuming 61.4 mW, with only 13.1 mW contributed from the TIA, resulting in 1.28-pJ/bit (0.27 pJ/bit for TIA only) efficiency.

3.2 System Architecture

Based on the analysis results in Chapter 2, an ORX composed of a TIA with a BW of 0.5x Baud rate followed by a 2-tap FFE and a 2-tap DFE is designed. The block diagram of the proposed PAM-4 ORX is depicted in Fig. 3.3, which consists of a CMOS linear TIA, PAM-4 samplers, and a clock path. The CMOS linear TIA includes a TIS, a VGA, and a post-amp to accommodate a large input dynamic range with negligible BW variation. The common-mode photocurrent

and input referred offset voltage are subtracted by the dc offset cancellation (DCOC) loop. After two half-rate sample/hold (S/H) circuits and summers, three slicers in odd/even path and a voltage digital to analog converter (DAC) are employed with a 2-tap precursor FFE and a 2-tap DFE to recover the PAM-4 output of TIA to 3-bit digital thermometer codes. The recovered thermometer codes are then converted into 2-bit binary codes, including a most significant bit (MSB) and a least significant bit (LSB) output, which are deserialized and sent to off-chip bit BER testing. The clock path takes external half-rate differential clock signals and amplifies them to rail-to-rail. Voltage-controlled delay lines (VCDL) and dividers are included for data decoding and deserializing.

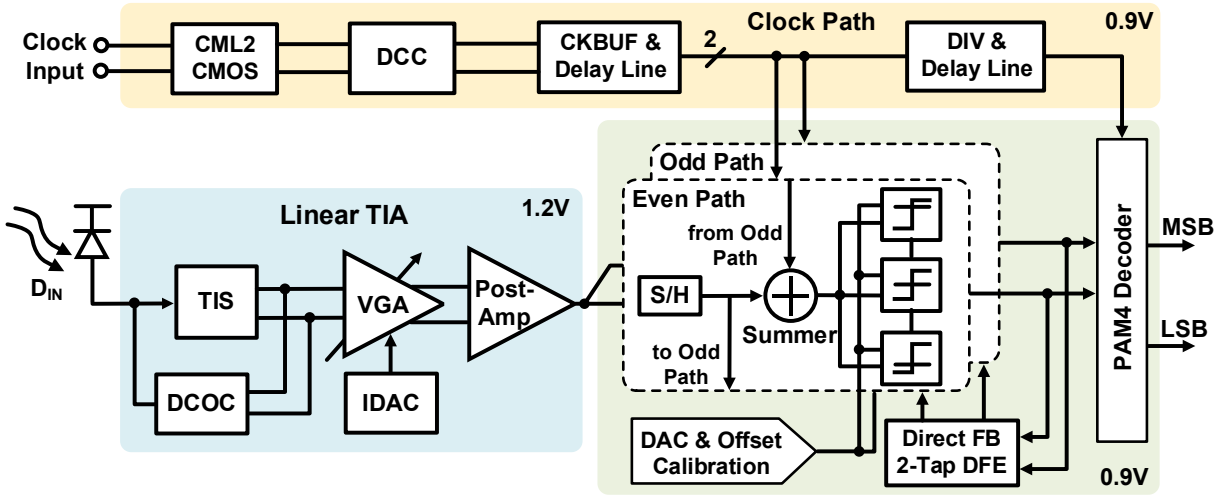


Figure 3.3. Block diagram of the proposed PAM-4 ORX architecture.

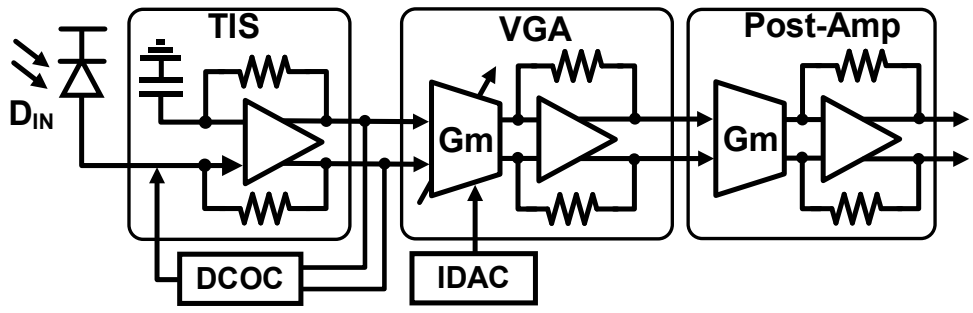


Figure 3.4. Block diagram of the proposed CMOS linear TIA.

Figure 3.4 shows the block diagram of the CMOS linear TIA. A pseudo-differential TIS is used as the first stage, and therefore the single-ended to differential (S2D) circuit is not needed.

The VGA with the gain controlled by a current DAC (IDAC) provides over 20 dB dynamic range, and the post-amp provides over 10 dB gain. Both the VGA and the post-amp adopt a TAS-TIS topology and use active inductors instead of passive inductors to save area. Passive inductors and CTLE are avoided here, which makes the TIA compact and energy efficient.

3.3 Building Blocks

3.3.1 PD Interface and TIS

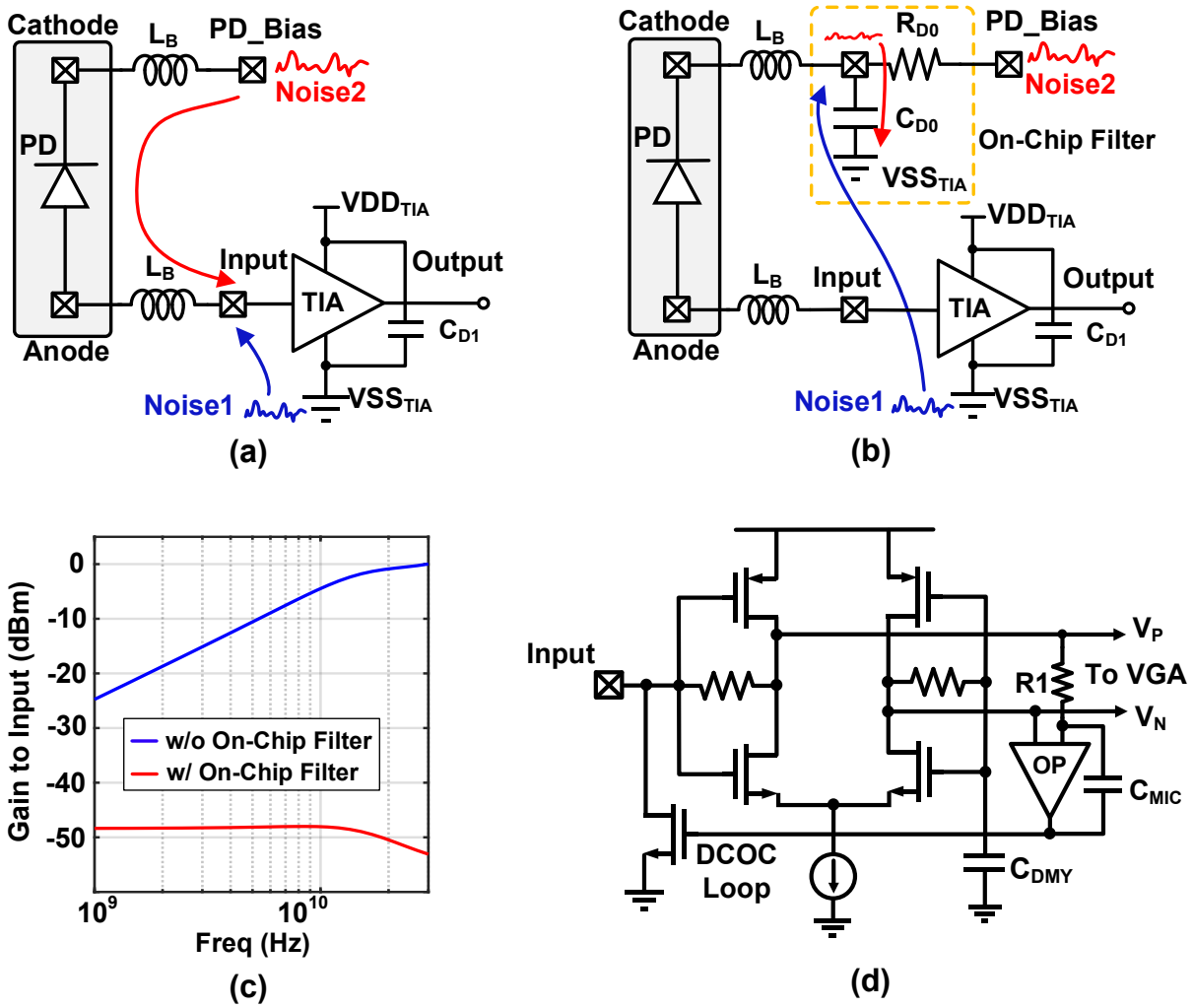


Figure 3.5. (a) Direct connection scheme where noise modulates the input signal. (b) On-chip connection scheme where noise is filtered and ac-coupled to VSS_{TIA}. (c) Simulated conversion gain from PD bias to TIA input. (d) Schematic of TIS and DCOC circuits.

The ORX is designed to interface with an external high-speed PD. At the ORX input, the single-

ended signal amplitude can be as low as 10 mV, which is particularly sensitive to noise. Therefore, the interface between the PD and ORX input should be treated carefully. Either a direct connection scheme or an on-chip connection scheme can be used to provide the bias voltage to the PD. The former one directly connects the bias voltage to the cathode of PD through a bonding wire L_B as shown in Figure 3.5 (a), and the other one first connects the PD cathode to ORX chip and makes the cathode ac-coupled to TIA ground VSS_{TIA} before it is connected to the bias voltage, as illustrated in Figure 3.5 (b). While the direct connection scheme is simple and saves chip pads, it has significant drawbacks. As noted in [8], due to the single-ended nature of the TIA input, noise at the VSS_{TIA} (referred to as noise1) affects the input signal since the PD signal is referred to VSS_{TIA} rather than the PD cathode at TIA input, and thus only PD anode is modulated by the noise1. Furthermore, the noise at the PD bias voltage (noise2) only modulates the PD cathode and would directly affect the TIA input, severely degrading sensitivity.

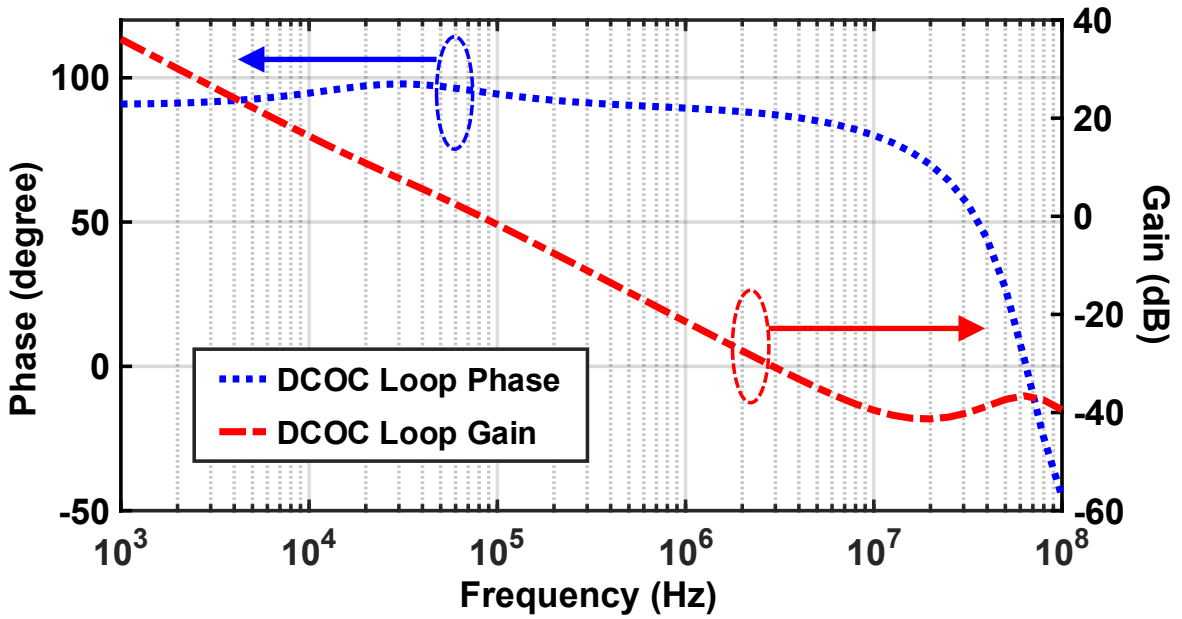


Figure 3.6. Simulated gain and phase of the DCOC loop.

In the on-chip connection scheme, PD cathode and VSS_{TIA} are ac-coupled through a capacitor, ensuring both are modulated by the same noise and improving ground noise rejection. R_{D0} and C_{D0} also provide on-chip filtering to attenuate noise2 before it is ac-coupled to VSS_{TIA}. As shown in Figure 3.5 (c), the on-chip filter effectively reduces the gain from the PD bias to the

TIA input compared to the unfiltered case. Figure 3.5 (d) illustrates the schematic of the TIS and DCOC circuits. The pseudo-differential push-pull TIS performs single-ended to differential conversion and incorporates a current tail for enhanced supply noise rejection [32]. The DCOC loop, formed by R1, C_{MIC}, OP, and M1, uses R1 and Miller capacitance C_{MIC} to create a low-pass filter. This feedback loop removes the DC component from the input signal before it enters the TIS, preventing a dc drop across R_F. Cutoff frequency of DCOC loop f_C must be much smaller than the data rate of the received signal to avoid baseline wander or data-dependent jitter, especially in the presence of long sequence of consecutive identical bits. As shown in Figure 3.6, the implemented DCOC loop has a cutoff frequency of 80 kHz with a phase margin of 85°.

3.3.2 VGA and Post-Amp

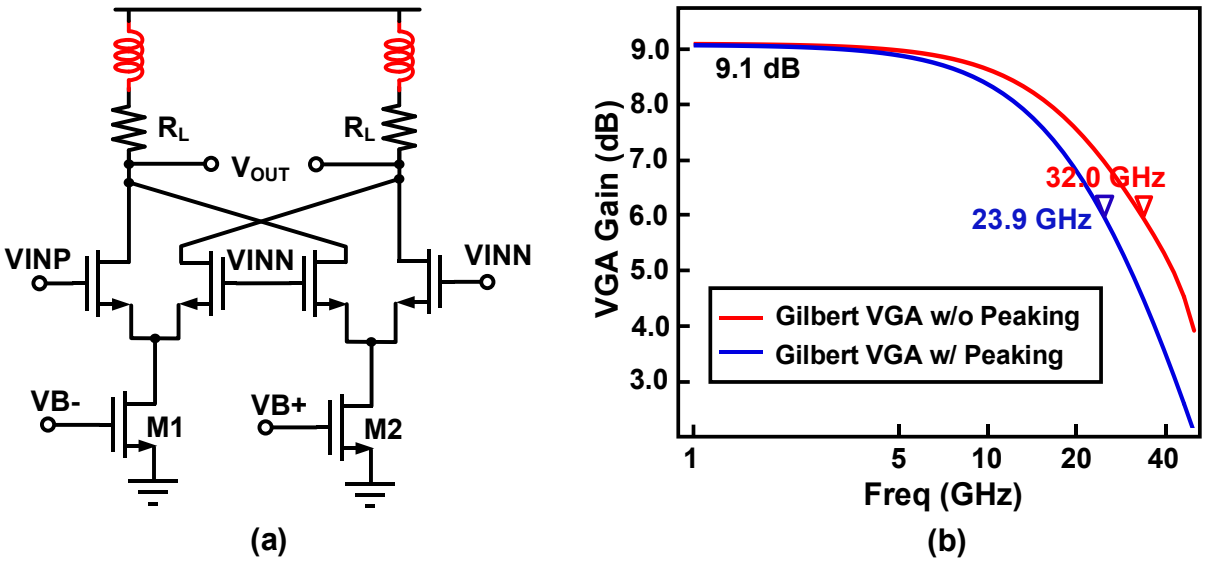


Figure 3.7. (a) Schematic of a conventional Gilbert-cell-based VGA. (b) Simulated frequency responses of VGA with and without inductive shunt peaking.

The VGA and the post-amp are designed to provide over 20 dB of dynamic range, and 10 dB gain, respectively. The Gilbert-cell-based VGA shown in Figure 3.7 (a) is widely used in linear TIAs to achieve a large input dynamic range while maintaining a constant frequency response [11], [33]. Nevertheless, limited by the gain-BW product of the structure, shunt inductive peaking is usually required to expand the VGA BW as shown in Figure 3.7 (b), where two 580-

pH inductors are used to achieve a BW of 32 GHz.

Another type of VGA comprised of a TAS and a TIS is shown in Figure 3.8, which in essence is a modified Cherry-Hooper amplifier [17]. The TAS provides transconductance Gm_{TAS}, and the TIS with feedback resistor R_F provides relatively low input resistance as described in Eq. (2.8a). Therefore, the dc gain of the VGA is

$$Gain_{TAS-TIS} = Gm_{TAS} \times \frac{A_{TIS}}{A_{TIS}+1} R_F \tag{3.1}$$

where A_{TIS} is the gain of feed-forward amplifier of TIS. The VGA changes the gain by tuning the value of feedback resistor R_F. Compared to the Gilbert-cell-based VGA, TAS-TIS topology provides much smaller load impedance of TAS which is R_F/A_{TIS} now, and also provides a smaller load impedance of TIS which is only $1/Gm_{TIS}$, resulting a larger capacity for driving the post-amp and a much higher gain-BW product, where Gm_{TIS} is the transconductance of TIS [34], [35].

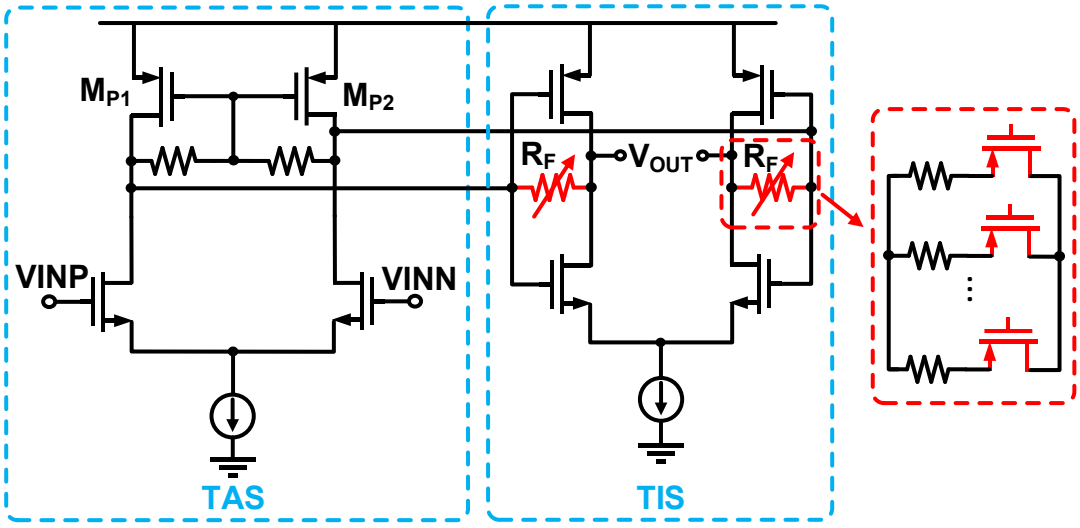


Figure 3.8. Schematic of a TAS-TIS topology-based VGA with its gain controlled by the feedback resistor R_F.

However, the variable resistor R_F causes BW variations over gain variations. For instance, with a design target of 20-dB tuning range and a constant Gm_{TAS}, R_F needs to have a tuning range of 10 times, so does the load impedance of TAS, and the overall BW of VGA is therefore affected. In addition, the switches for feedback resistor control would bring extra parasitic

capacitance reducing the BW, which becomes particularly serious when multi-bit control is required to support fine tuning of overall gain. A 3-bit TAS-TIS VGA with a tuning range of 8-dB is designed for evaluation as shown in Figure 3.9. Simulations show that the VGA provides a max. dc gain of 9.1 dB with a corresponding BW of 27.6 GHz, but the BW is over 50 GHz at 1.1 dB gain, resulting in a 25 GHz BW variation across 8 dB gain variation. When the TIA is set to have a low gain, the severe BW variation would cause high-frequency ripples and degrade the signal quality and noise performance.

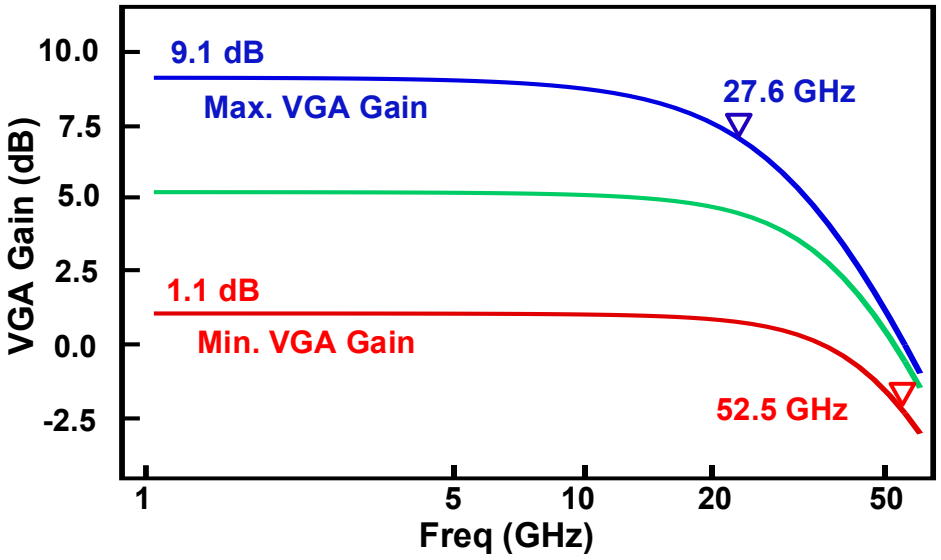


Figure 3.9. Simulated frequency responses of the TAS-TIS VGA with different gain settings.

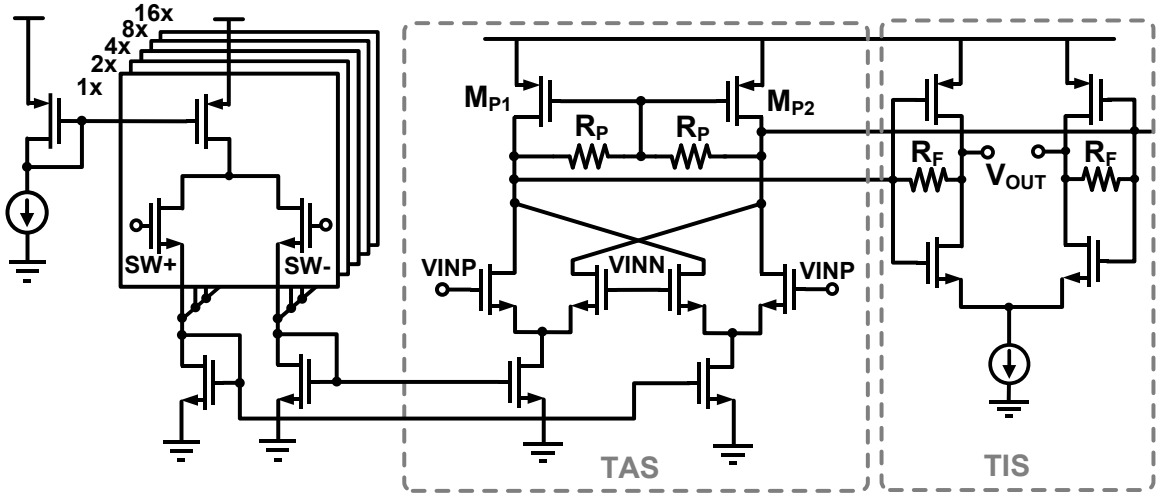


Figure 3.10. Schematic of the proposed Gilbert-TIS VGA.

The proposed VGA adopts a TAS-TIS topology, but the gain is controlled by changing the Gm_{TAS} instead of the feedback resistor R_F as shown in Figure 3.10. The TAS uses a Gilbert cell controlled by a 5-bit current DAC, and the resistor R_F is fixed to maintain a constant BW across gain variations, thus combining the advantages of both Gilbert-cell-based VGAs and conventional TAS-TIS VGAs. The fully differential input of the first stage also helps convert pseudo-differential signals from TIS into fully differential ones. Simulation results in Figure 3.11 show that under the same low-frequency gain of 9.1 dB, the proposed VGA achieves the same gain-BW product as the Gilbert-cell-based VGA with two 580-pH inductors, and its BW variation is less than 0.2 GHz over 19 dB gain variation. From another perspective, by splitting the transconductance and loading of the Gilbert cell and replacing the load resistors R_L in Figure 3.7 (a) with a TIS, the proposed VGA achieves a much higher gain-BW product and is able to remove inductors, with only an additional power consumption 2.7 mW.

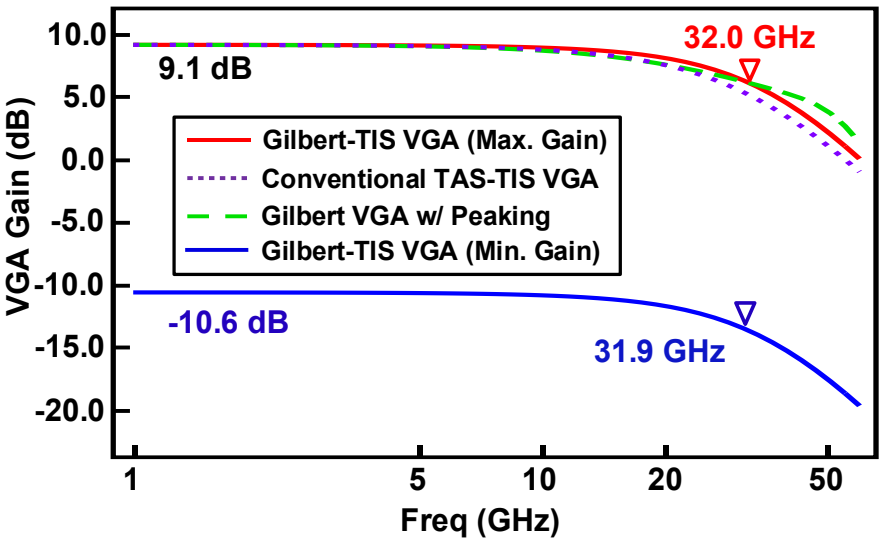


Figure 3.11. Simulation results and comparison of frequency responses for three types of VGAs.

The post-amp also adopts a TAS-TIS topology as shown in Figure 3.12, where the TAS consists of two differential pairs so that the output of M_{P1} and M_{P2} at inner pair can be further amplified by M_{P3} and M_{P4} at outer pair to achieve higher transconductance [14]. Besides, M_{P1}, M_{P2} with a transconductance of g_m, parasitic capacitance C_{gs} and resistor R_P form active inductors to further extend the BW [36], with inductance given by

$$L_{act} = \frac{R_P C_{gs}}{g_m} \tag{3.2}$$

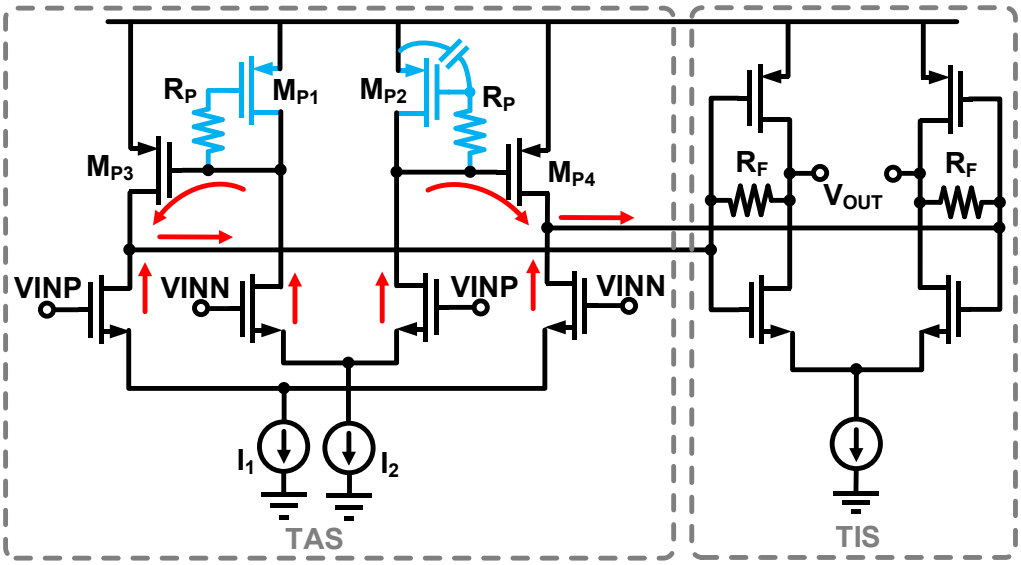


Figure 3.12. Schematic of the post-amp.

Post-layout simulations in Figure 3.13 show that the entire linear TIA achieves a gain up to 73.6 dBΩ with a BW of 14 GHz and provides a gain tuning range up to ~23 dBΩ, with a BW variation of around 0.1 GHz. The layout of the entire TIA, including DCOC circuits and IDAC is given in Figure 3.14 with a compact area of only 0.17 × 0.08 mm^2 thanks to the adoption of TAS-TIS topologies and active inductors. Capacitors used in DCOC circuits occupy almost half of the TIA area.

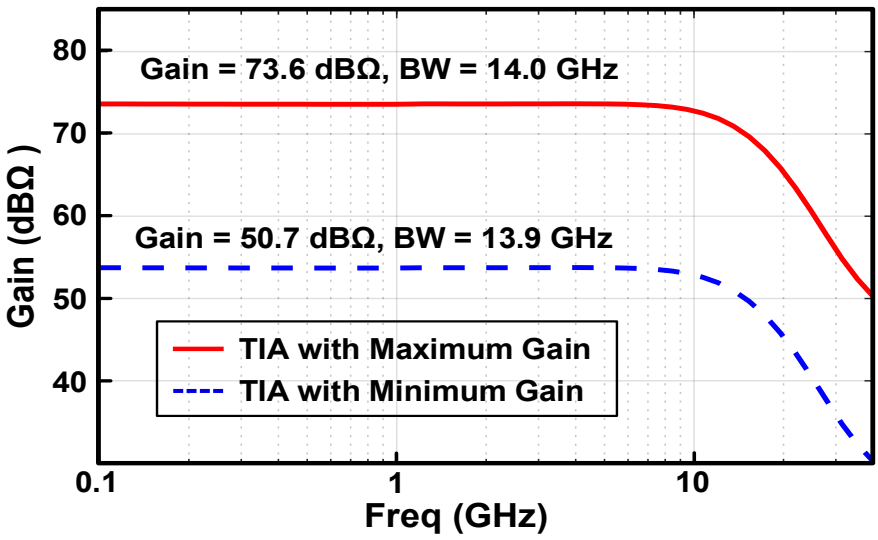


Figure 3.13. Simulated responses of the entire linear TIA with max. and min. gain settings.

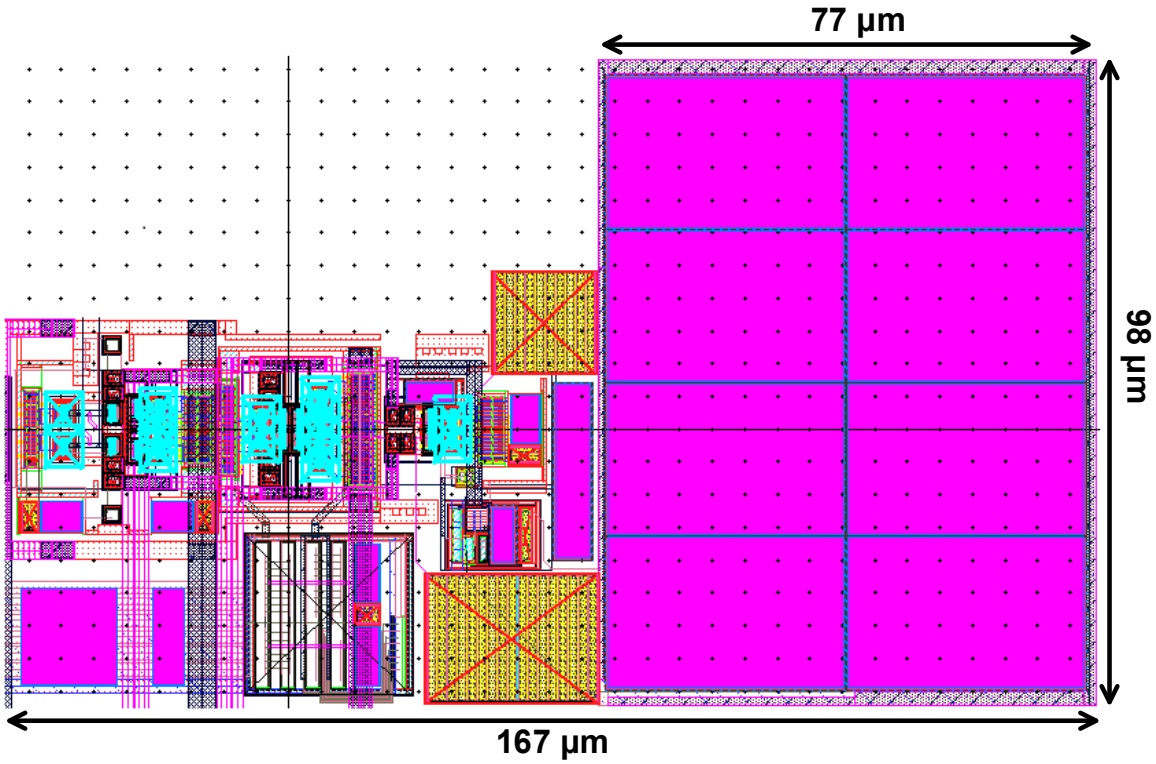


Figure 3.14. Layout of the TIA with DCOC circuits.

3.3.3 Sampler with Integrated Equalizer

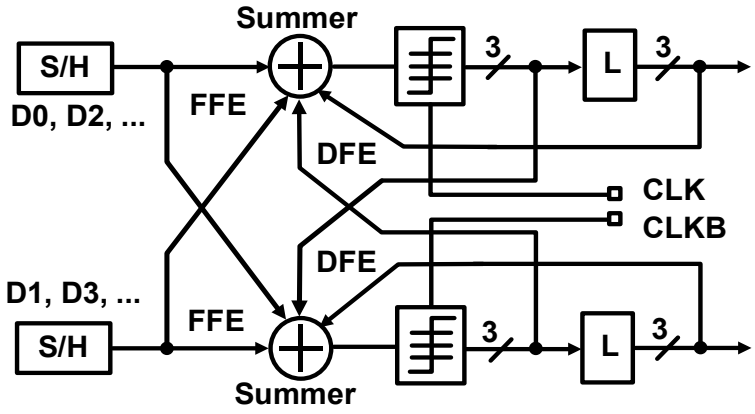


Figure 3.15. Block diagram of the half-rate FFE and DFE.

The full-rate input data is converted into two half-rate data streams at TIA output. The block diagram of half-rate PAM-4 sampler with FFE and DFE is shown in Figure 3.15. The precursor FFE is embedded with S/H circuits by a summer that performs summation of consecutive data samples. The 3-bit thermometer outputs, both before and after a set-reset (SR) latch, are fed

back to the summer to implement the first and the second tap DFE. Figure 3.16 shows the schematic of the S/H circuit and the summer with FFE and DFE taps. A current-mode summer with resistive load and adjustable degeneration resistor is used. Equalization coefficients are adjusted by changing tail current sources manually using current DACs. PMOS dummy M_{P3} and M_{P4} in the S/H help mitigate the clock through from M_{P1} and M_{P2}. NMOS dummy M_{N3} and M_{N4} in the summer help reduce the signal feedback from the output of summer to the output of S/H circuits [37].

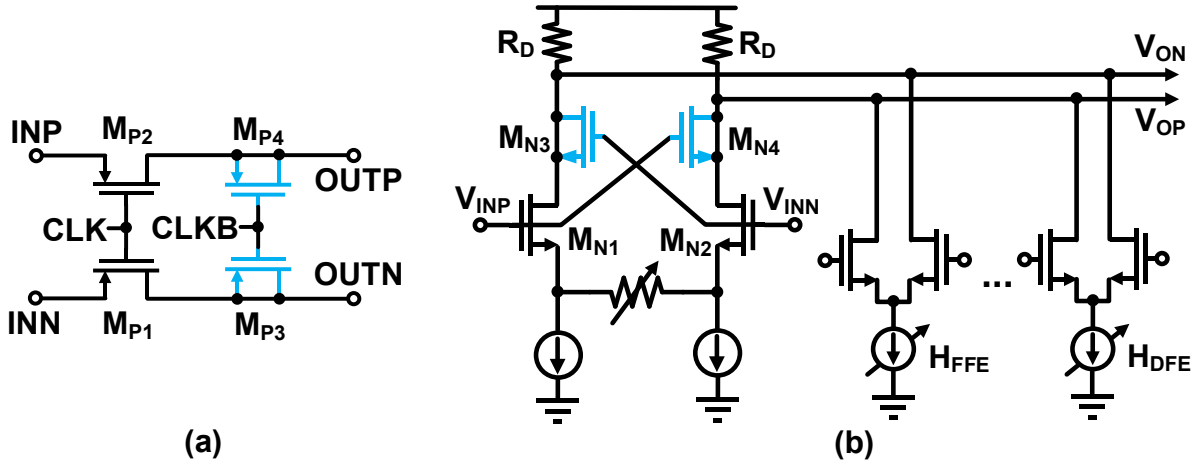


Figure 3.16. Schematic of (a) the S/H circuit and (b) the summer with FFE and DFE taps.

The timing diagram for pre-tap FFE and the first tap DFE in a half-rate design is illustrated in Fig. 11, where D_n represents the analog value of nth PAM-4 symbol and solid red arrows represent digitizing action of the slicer. The data is first sampled and held for 1 UI at S/H circuits by CK_SH and CKB_SH alternatively, and the data in the even path bears a 1-UI delay with respect to that in odd path. For the FFE, take D_1 in the even path for example, by subtracting D_2 from D_1, the 0.5-UI 1st precursor of D_1 can be cancelled. For the direct DFE, at the output of summer, D_2 in the odd path is sliced by the rising edge of slicer clock CK_CMP. Before D_1 is sliced at the rising edge of CKB_CMP, D_0 needs to be regenerated so that it is subtracted from D_1 to cancel the 1st postcursor of D_1. Therefore, to close the decision feedback loop for the first tap DFE, the sum of clock to Q delay T_{CKQ} of the slicer, setup time T_{setup} of the slicer, and settling time T_{settle} of the summer, should be less than 1 UI which is 42 ps for 48 Gb/s PAM-4 operation.

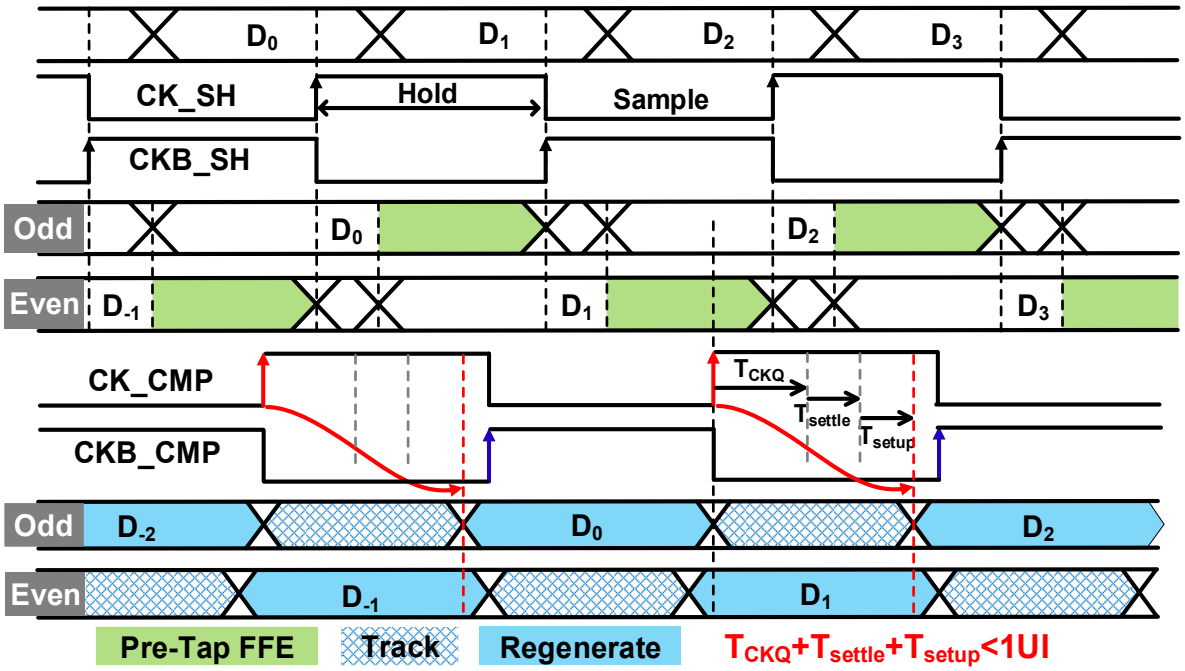


Figure 3.17. Timing diagram for the pre-tap FFE and the first tap DFE in a half-rate design.

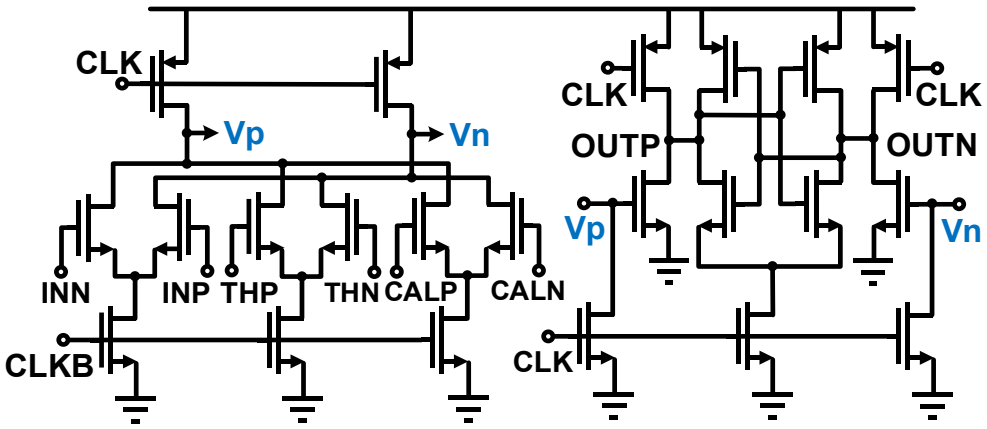


Figure 3.18. Schematic of the track-and-regenerate slicer.

The T_{CKQ} of a commonly used Strong-Arm latch-based comparator is around 19.5 ps, and it can be ~30 ps at the worst case (ss corner, 65 °C), which makes it not suitable for this design. To meet the stringent timing constraint of direct DFE at a speed higher than 24 GBaud, a track-and-regenerate slicer is adopted to reduce T_{CKQ} while maintaining a large output swing [38], as shown in Figure 3.18. When CLK is low and CLKB is high, the first stage tracks input signals, and the latch at the second stage is charged to V_{DD}. When CLK is high and CLKB is low, Vp and Vn are discharged to V_{SS}, and the latch regenerates the amplified signals to digital levels.

Post-layout simulation result at 15 GHz in Figure 3.19 shows that the optimized T_{CKQ} is reduced to less than 17 ps. To further verify the performance of the slicer, periodic steady-state (PSS) and periodic noise (Pnoise) simulations are conducted at 32 GBaud, resulting in an input-referred noise of 1.6 mV. Monte Carlo simulation is also conducted at tt corner with 400 simulations showing an offset standard differential of 23.5 mV, as shown in Figure 3.20.

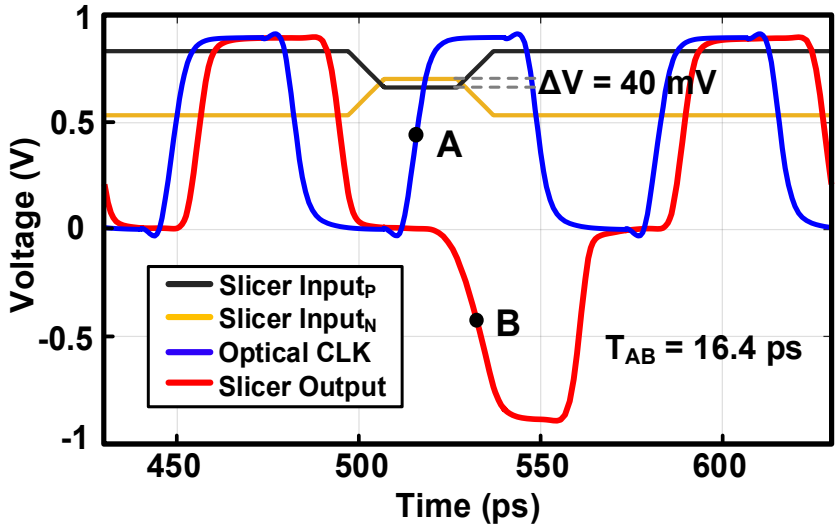


Figure 3.19. Simulated large signal performance of the slicer at 15 GHz.

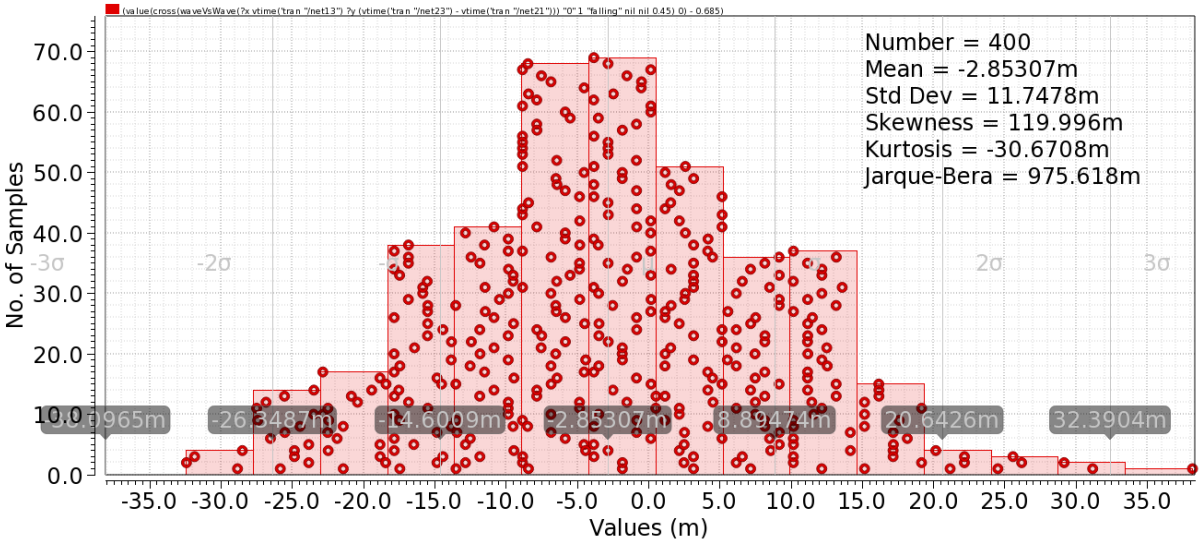


Figure 3.20. Monte Carlo simulation results of the slicer input offset.

Calibration logic is used to reduce the input offset of slicers, and the block diagram of the calibration scheme is shown in Figure 3.21. A 6-bit reference DAC, DAC_ref, provides

reference voltage to slicers to decode the top and bottom eyes of PAM-4 signals. The thermometer-to-binary (T2B) decoder converts the 3-bit output of slicers to 2-bit MSB and LSB outputs. The calibration circuits include three 6-bit calibration DACs, DAC_cal, and a calibration logic. During the calibration, the input of ORX is set to zero. Initially, the output of calibration logic is 0 and DAC_cal output is therefore set to be minimum, resulting in an output of '1'. If the comparator does not generate '0' within 8 clock cycles, the output of calibration logic increases by one and the DAC_cal increases by 1 LSB of DAC. The process continues until a transition from '1' to '0' happens at slicer output and then the calibration ends. Figure 3.22 shows the transient simulation results of the calibration output with a zero ORX input, which increases from 0 to 32 when the transition of the slicer output occurs. When the calibration is completed, the DAC_cal output is just higher than the inherent offset and fixed, but the excess is less than 1 LSB, as depicted in Figure 3.23. The calibration logic is designed to cover differential offset of slicers.

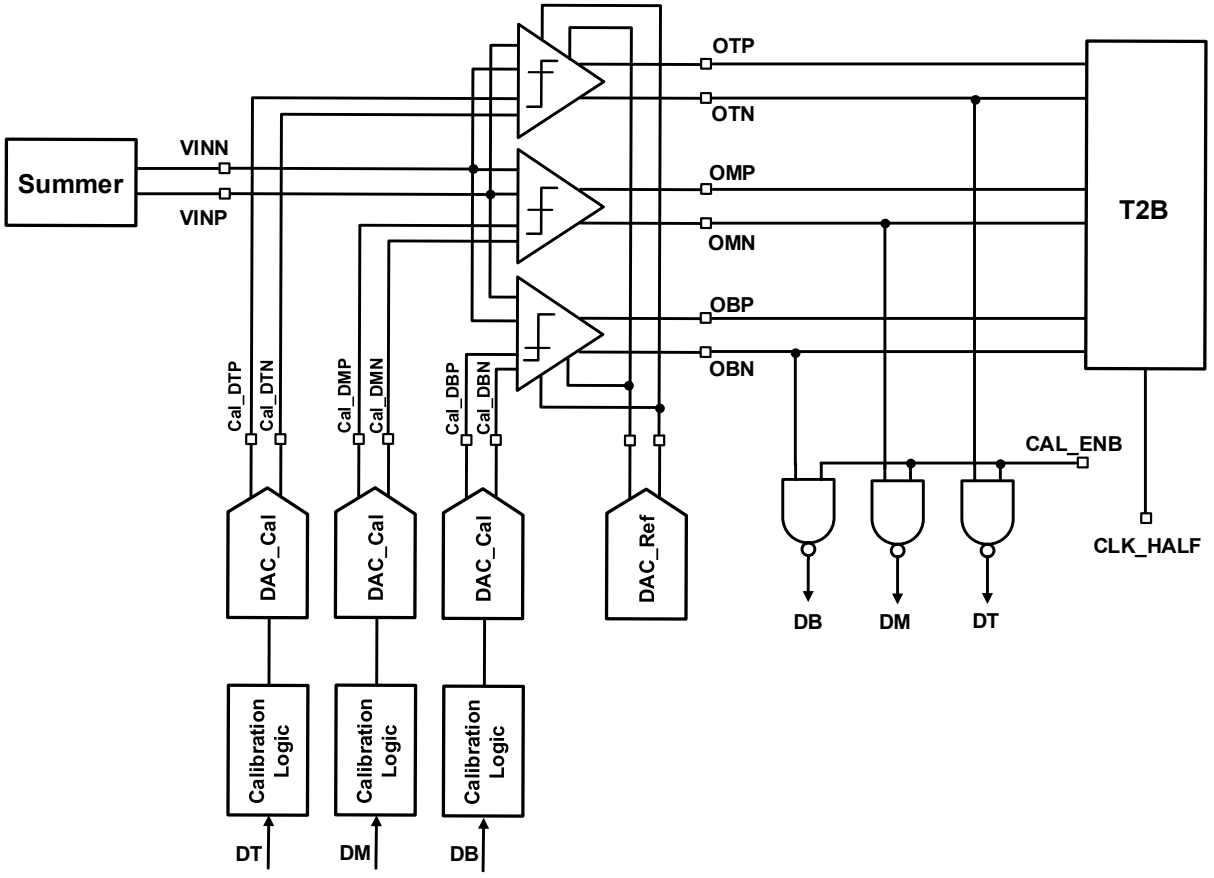


Figure 3.21. Block diagram of slicers with the calibration logic.

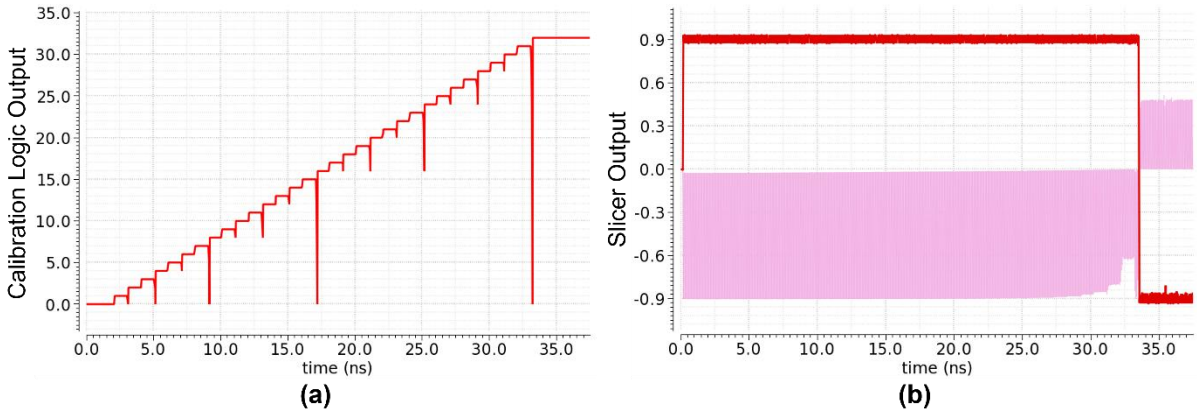


Figure 3.22. Simulation result of (a) the calibration logic output and (b) the slicer output.

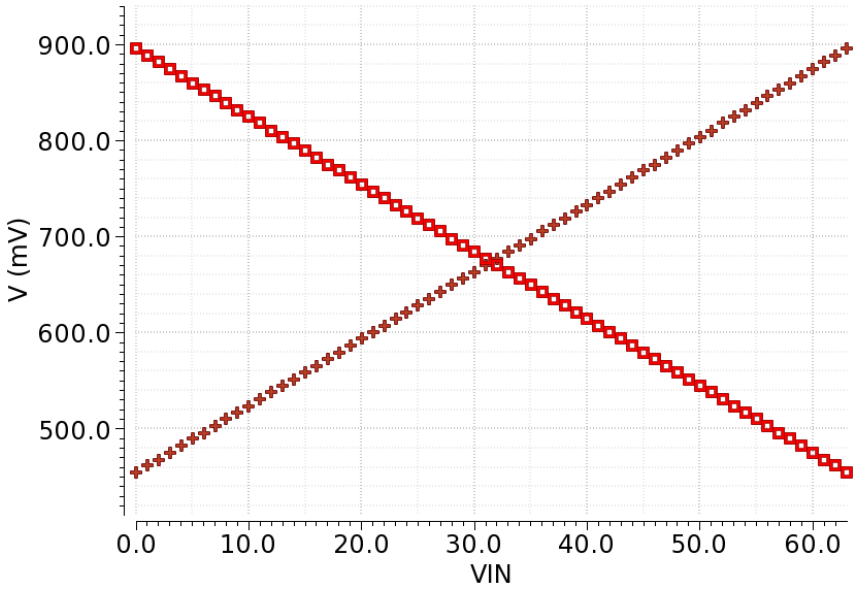


Figure 3.23. DAC_cal output with different input control words.

The layout symmetry of PAM-4 sampler directly affects its offset and final performance, and thus its layout should be carefully planned. Figure 3.24 depicts the layout of the half-rate PAM-4 sampler including S/H circuits, summers, DACs, and comparators. Symmetric and compact routines are planned and conducted to reduce parasitics from wires without introducing mismatches. Simulations with and without equalization have also been carried out to demonstrate a closed decision feedback loop and to evaluate the effectiveness of FFE and DFE for expanding the eye-opening. A 25-GHz BW constraint and 1.5-ps RJ are added to the input signal, and a PD model with 70 fF capacitance and a 300-pH wire-bond inductance are included. With 48-Gb/s PAM-4 input with an amplitude of 220 μA, the simulated half-rate 24-Gb/s PAM-

4 eye diagrams at summer output without and with equalizations are shown in Figure 3.25 (a) and (b) respectively. The coefficients of the pre-tap FFE, the first-tap DFE and the second tap DFE are 0.07, 0.08, and 0.01. With FFE and DFE, the PAM-4 eye diagram is successfully recovered at summer output.

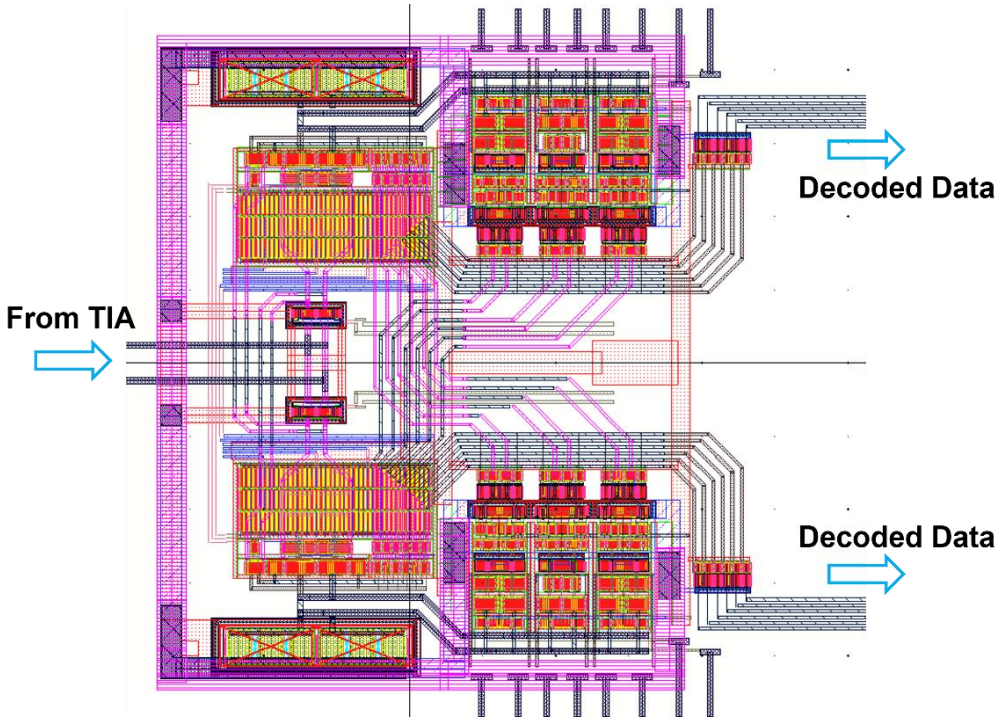


Figure 3.24. Layout of the PAM-4 sampler.

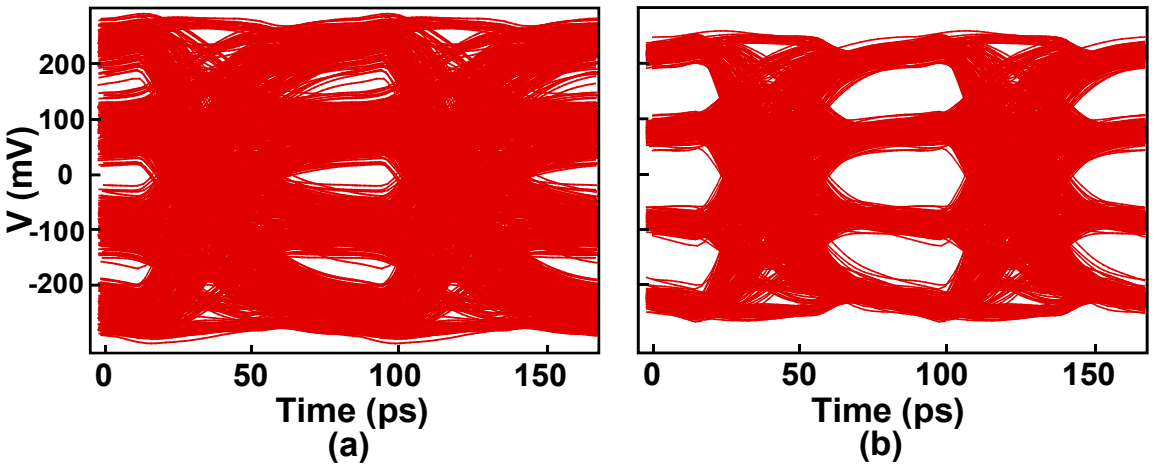


Figure 3.25. Simulated differential output at the summer (a) without equalization and (b) with a 2-tap FFE and a 2-tap DFE.

3.3.4 Clock Buffer

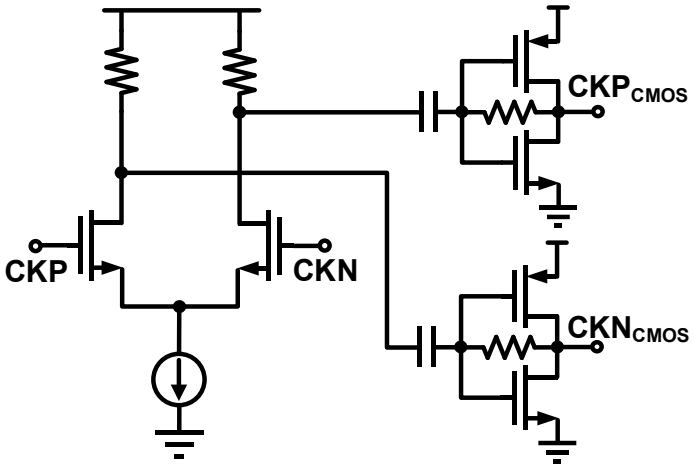


Figure 3.26. Schematic of the CML-to-CMOS input clock buffer.

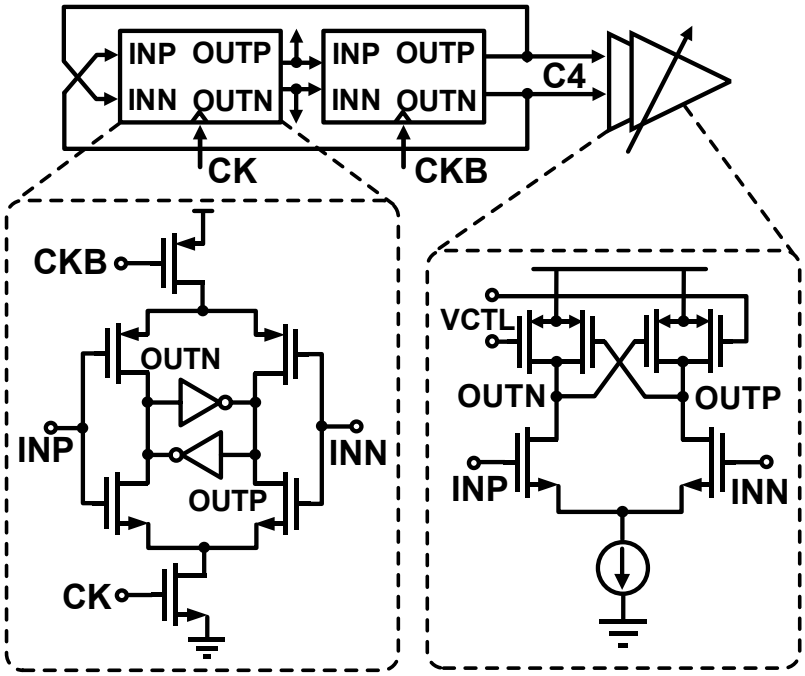


Figure 3.27. Block diagram of the clock divider and the voltage-controlled delay line.

The external differential clock is received through a CML-to-CMOS clock buffer shown in Figure 3.26 which amplifies incoming sinusoidal clock signals to rail-to-rail at various clock frequencies. It consists of a differential amplifier and ac-coupled inverter-based clock amplifiers. Self-biased inverter and ac coupling capacitor ensure that the dc level of clock signals is biased to around half of the supply voltage.

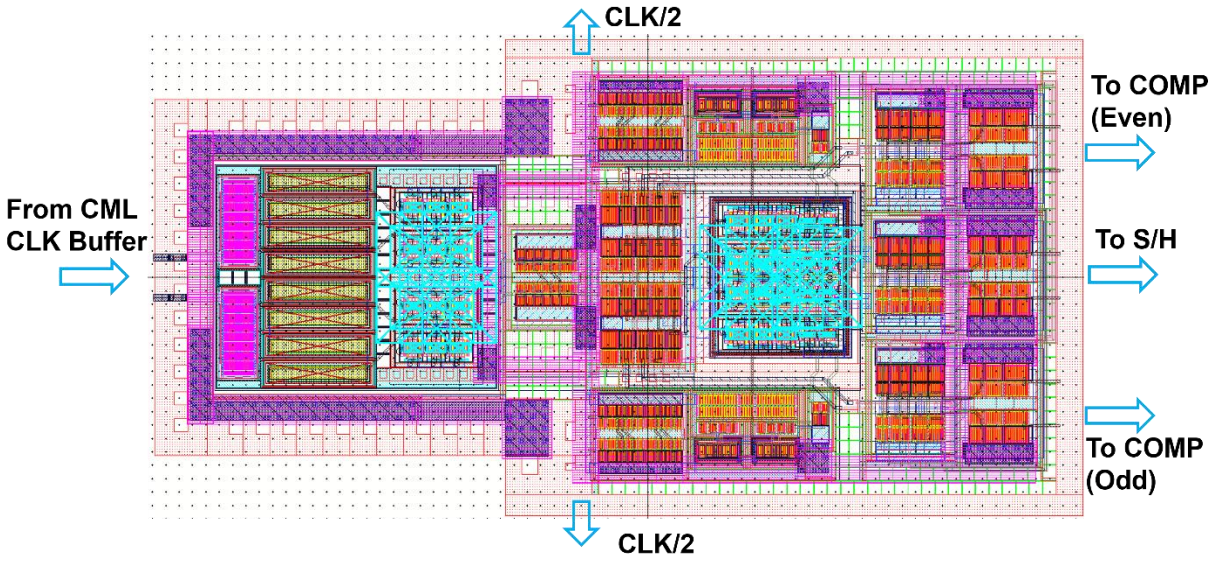


Figure 3.28. Layout of the entire clock buffer.

A divider is required to generate divided clock signals from half-rate differential clock for decoding and deserializing. To work at a frequency higher than 14 GHz, a C^2MOS frequency divider is designed as shown in Figure 3.27, which can provide a large output swing up to 16 GHz and avoid the use of CML divider and an extra CML-to-CMOS circuit [39]. To accommodate the delay variation, a VCDL controlled by a 6-bit R2R ladder is used. As shown in Figure 3.26, the cross-coupled PMOS of the delay cell exhibits negative resistance, and the PMOS controlled by voltage VCTL has positive resistance [40]. By tuning loading resistance of the delay cell, the delay can be controlled. The control voltage is generated by the R2R ladder with a step size ranging from 10.8 mV to 14.8 mV. With a control voltage range from 200 mV to 700 mV, the VCDL has a tuning range of 30 ps with a resolution of 1.3 ps. The layout of the entire clock buffer is given in Figure 3.28.

3.4 Measurement Results

The proposed ORX is fabricated in a 28-nm CMOS process and its die photo is shown in Figure 3.29. The ORX occupies an area of 1 x 0.53 mm^2 defined by the pad frame, and an active area of only 0.06 mm^2 thanks to the inductorless design. As shown in Figure 3.30, a low frequency power and control PCB is used for setting V_{DD}, bias point and control bits. Another high frequency PCB is employed for chip mounting and transmission lines routing. Before wire-

bonding ORX chip to a PD, time-domain electrical measurements are performed using a BER tester (BERT) as the data source with a 20-dB 67-GHz attenuator. Figure 3.31 shows the electrical measurement setup for the PAM-4 ORX. The BERT also generates half-rate differential clock signals for the ORX chip, and the chip sends out a divided clock to the sampling oscilloscope as a trigger clock. The electrical output of the ORX chip is sent via an SMA connector and a DC block to the sampling oscilloscope for eye diagram observation, and to the BERT for BER testing.

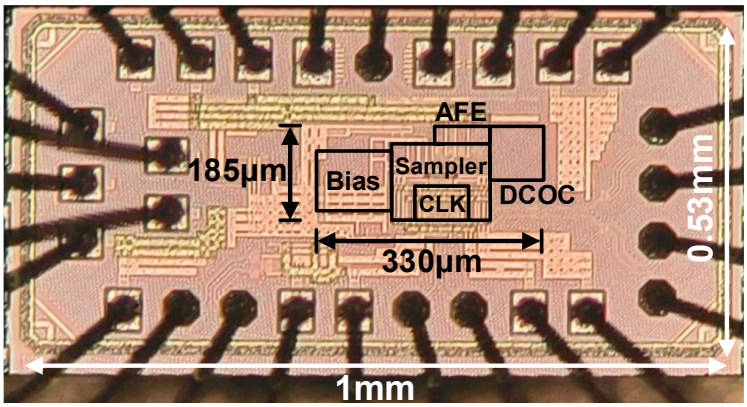


Figure 3.29. Micrograph of the ORX.

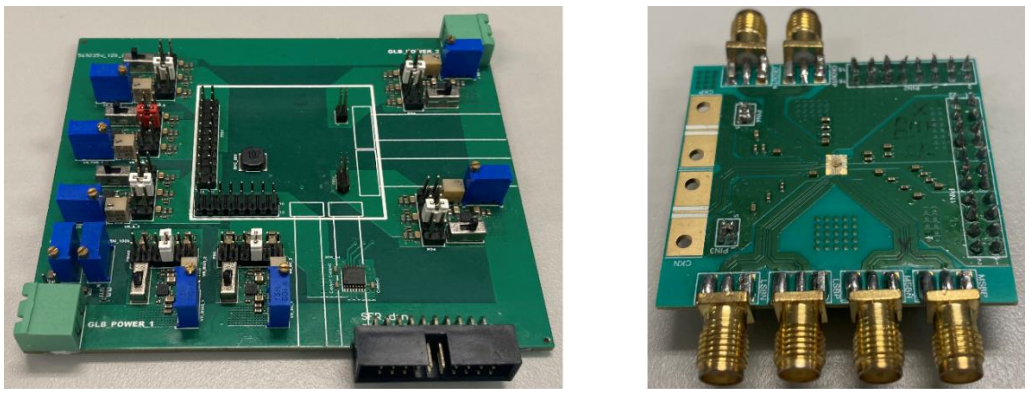


Figure 3.30. (a) Power and control low-frequency PCB module. (b) Chip mounting high-frequency PCB module.

The measured bathtub curves of 30-Gb/s NRZ with 18-mV input amplitude and 42-Gb/s PAM-4 with 40-mV input amplitude are shown in Figure 3.32 and 3.33, respectively. At 30

Gb/s, only 1e-4 BER is achieved when only ORX FFE is enabled and ORX DFE is disabled, while an error-free eye opening of 0.13 UI is achieved when both FFE and DFE are enabled. At 42 Gb/s, the BER is still higher than 2.4e-4 pre-FEC BER limit when ORX FFE is enabled. After enabling both FFE and DFE, the BER can be improved to < 1e-4. It should be noted that the electrical measurement is used to verify the function of the ORX design before the optical measurement, and the characteristic of single-ended electrical input signal through the 50-Ω PCB trace is different from the signal from PD output.

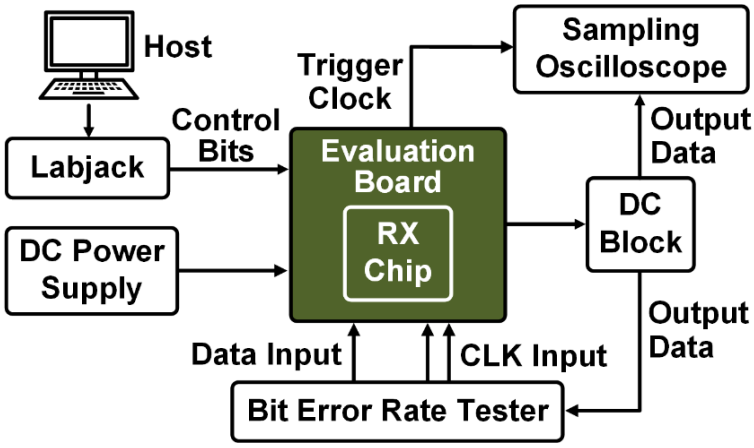


Figure 3.31. Electrical measurement setup for the ORX.

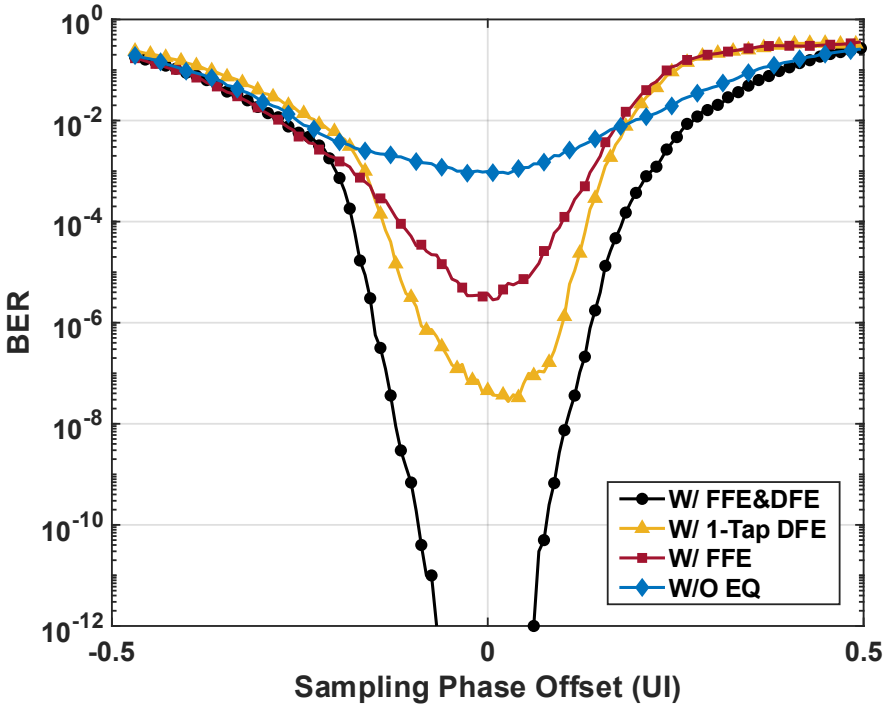


Figure 3.32. Measured bathtub curves at 30-Gb/s NRZ with a 18-mV input amplitude.

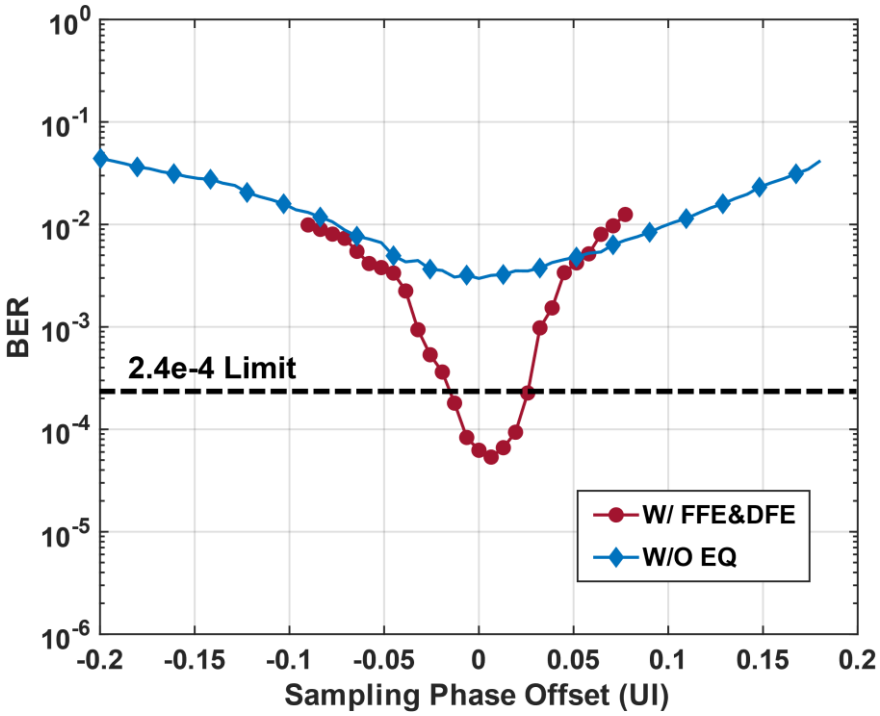


Figure 3.33. Measured bathtub curves at 42-Gb/s PAM-4 input with a 40-mV input amplitude.

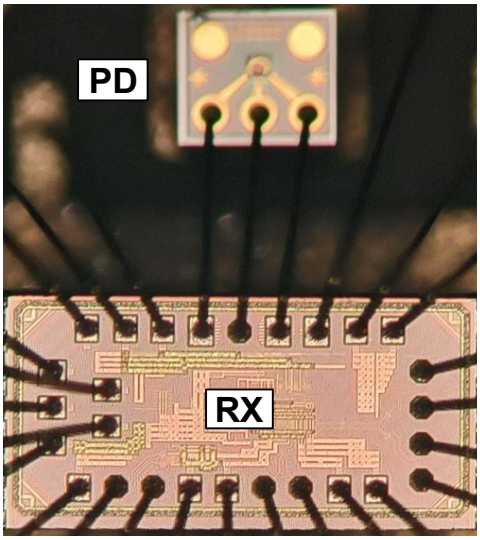


Figure 3.34. Micrograph of the ORX wire-bonded to a PD.

Figure 3.34 shows the ORX wire-bonded with a commercial O-band back-illuminated PD for optical testing. The PD has an O/E BW of 27-GHz, junction capacitance of 60 fF, and a responsivity of 0.75-A/W. The optical measurement setup is given in Figure 3.35 (a). The optical signal input is generated from an optical reference transmitter, Keysight M81491A, driven by a pattern generator, Keysight M8045A, and the optical power level is adjusted by an

internal optical attenuator of M81491A. A BERT, Keysight M8046A, provides a differential input clock for ORX, and the decoded output of ORX is connected back to BERT for BER testing. Both input and output signals are also connected to a sampling oscilloscope, Keysight DAC-X N1000A, for eye diagram observation. A PC interface controls the ORX to perform slicer offset calibration, FFE/DFE coefficient tuning, and BER measurement. A 1308-nm light source is coupled to PD via a 1-m single-mode fiber (SMF) as illustrated in Figure 3.35 (b).

The ORX was first characterized with 28- and 30-Gb/s PRBS9 NRZ inputs. In NRZ mode, all data slicers are enabled without PAM-4 thresholds. Bathtub curves are measured for 28-Gb/s NRZ with -8.0-dBm input OMA as shown in Figure 3.36. At 28 Gb/s, only 1e-4 BER is achieved when ORX FFE is enabled and DFE is disabled, while the BER can be significantly improved to achieve an 1e-12 eye opening of 0.13 UI when both FFE and DFE are enabled. The 1e-12 BER at 30-Gb/s NRZ indicates the operation of direct DFE and verifies the slicer design in the previous section.

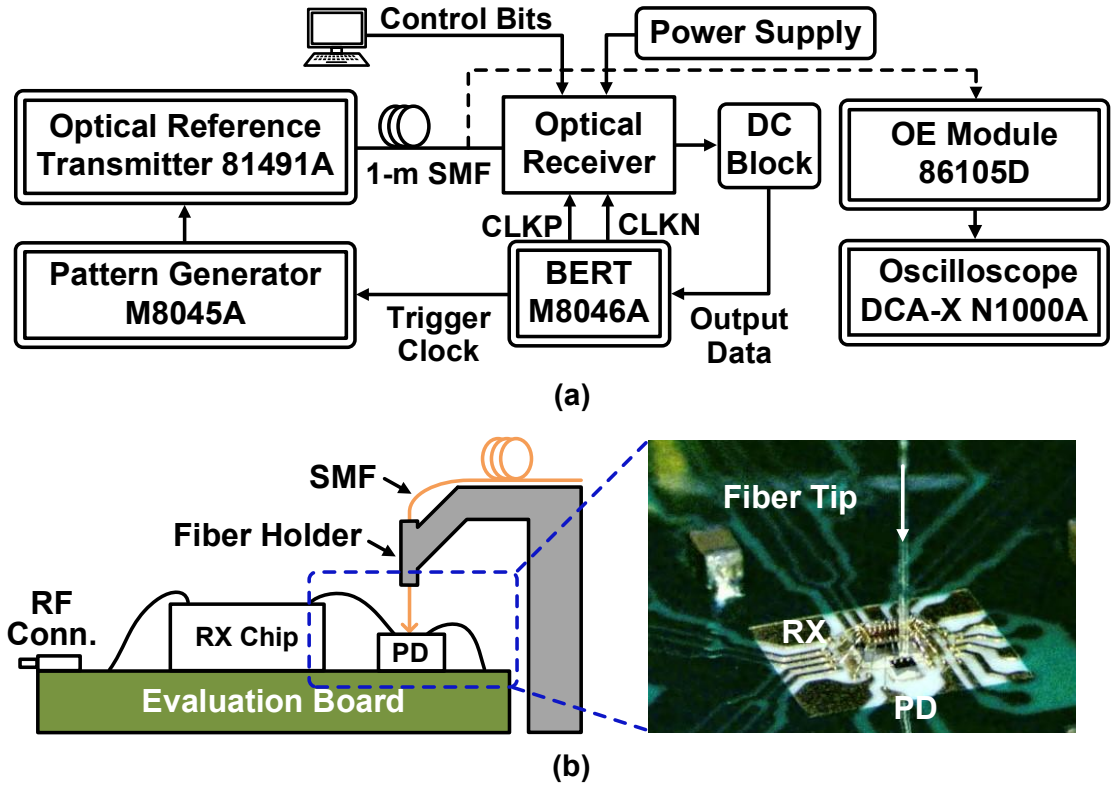


Figure 3.35. (a) ORX optical measurement setup. (b) Block diagram and photo of the fiber coupling scheme.

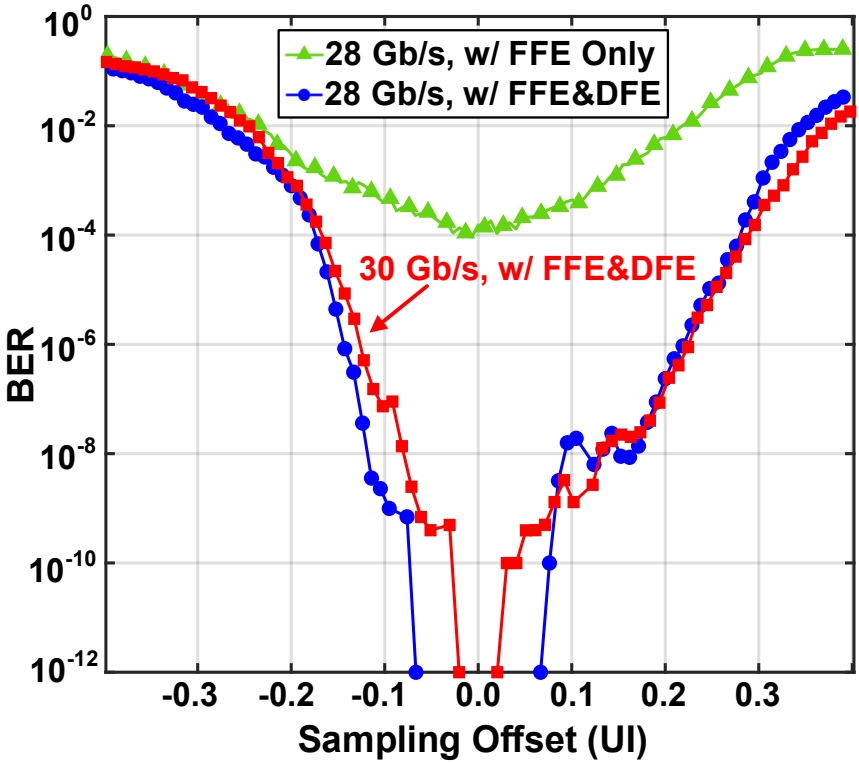


Figure 3.36. Measured 28-Gb/s and 30-Gb/s NRZ bathtub curves.

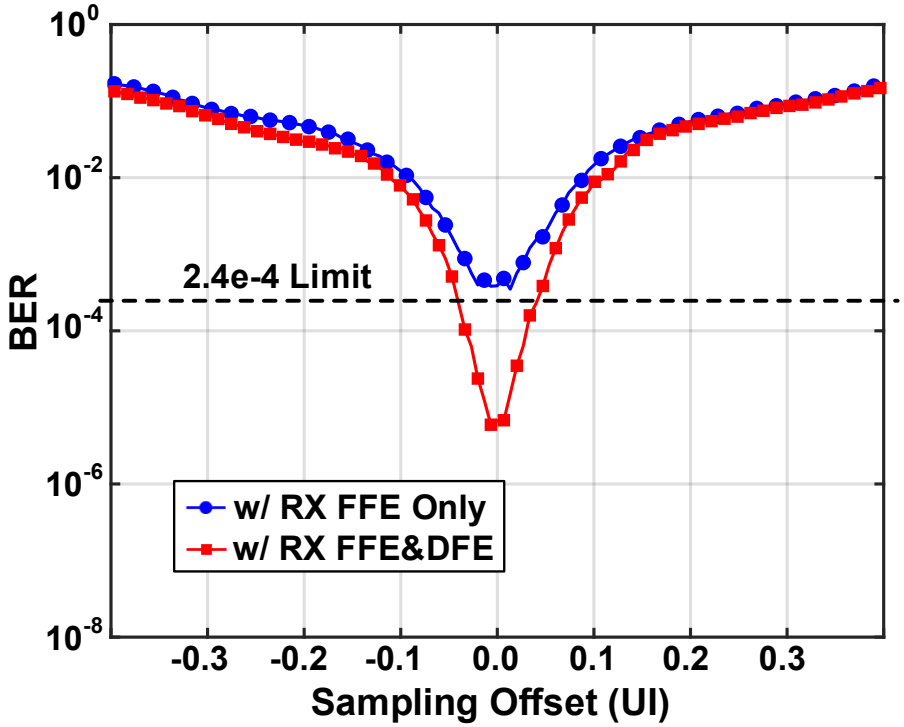


Figure 3.37. Measured 48-Gb/s PAM-4 bathtub curves.

In PAM-4 mode, bathtub curves are measured for 48-Gb/s PAM-4 with -4.6-dBm input OMA

as shown in Figure 3.37. At 48 Gb/s, the BER is still higher than 2.4e-4 pre-FEC BER limit even after enabling ORX FFE. The BER can be improved to < 1e-5 after enabling both FFE and DFE. Figure 3.38 shows the optical input eye diagrams of 30-Gb/s NRZ signal and 48-Gb/s PAM-4 signal with an extinction ratio (ER) of 4.8 dB. Figure 3.39 shows the decoded eye diagrams of 7.5-Gb/s with 30-Gb/s NRZ optical input, and 6-Gb/s with 48-Gb/s PAM-4 optical input. The input sensitivity vs. BER performance at 28, 30, and 48 Gb/s with FFE and DFE is summarized in Figure 3.40. The input OMA is controlled by adjusting the output power of optical reference transmitter. The measured NRZ sensitivity for 1e-12 target BER at 28 and 30 Gb/s are -8.2 and -7.9 dBm, respectively. The measured 48-Gb/s PAM-4 sensitivity is -5.1 dBm under 2.4e-4 BER target.

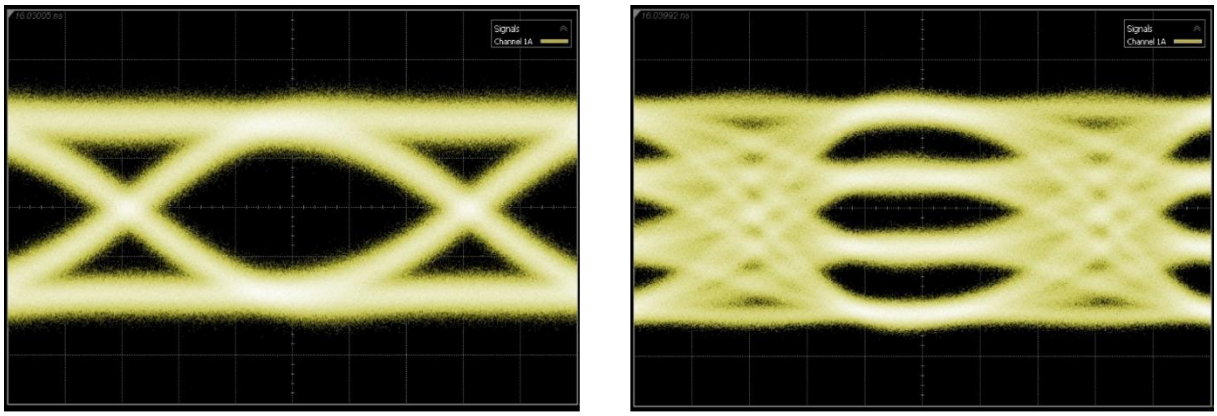


Figure 3.38. Optical input eye diagrams of (a) a 30-Gb/s NRZ signal and (b) a 48-Gb/s PAM-4 signal.

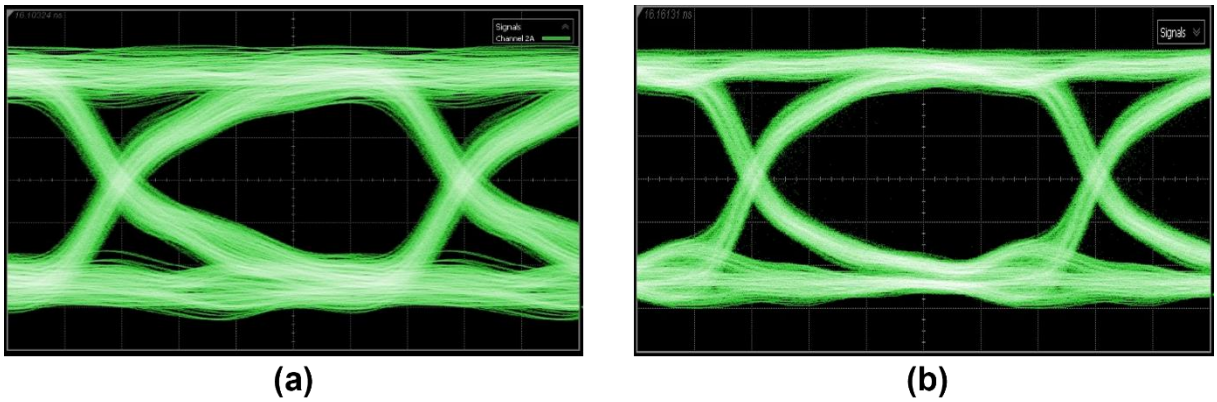


Figure 3.39. Decoded output eye diagrams of (a) a 7.5 Gb/s with a 30-Gb/s NRZ optical input, and (b) a 6 Gb/s with a 48-Gb/s PAM-4 optical input.

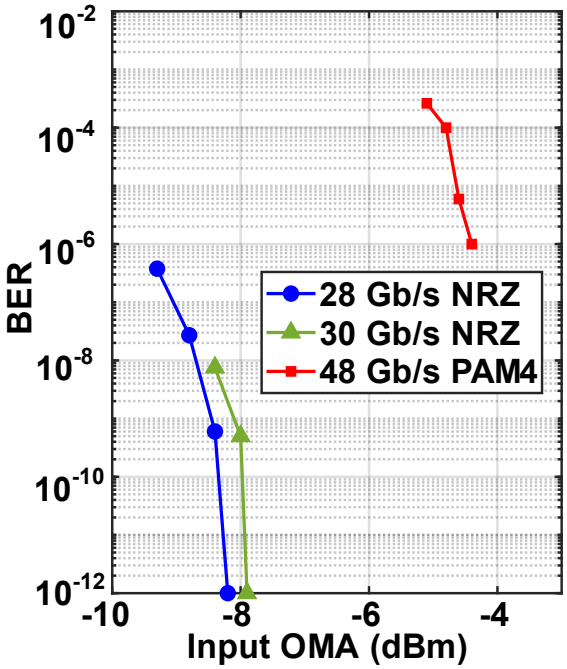


Figure 3.40. Measured BER vs. input OMA sensitivity at 28, 30, and 48 Gb/s with the FFE and DFE.

Figure 3.41 shows the measured ORX power breakdown at 48 Gb/s. The linear TIA dissipates 13.1 mW from a 1.2-V analog supply. The PAM-4 sampler and equalizer consume 17.4 mW from a 0.9-V digital supply. The clock path consumes 27.9 mW from a 0.9-V clock supply. In total, the ORX consumes 61.4 mW resulting in 1.28-pJ/bit (0.27 pJ/bit for TIA only) efficiency at 48 Gb/s.

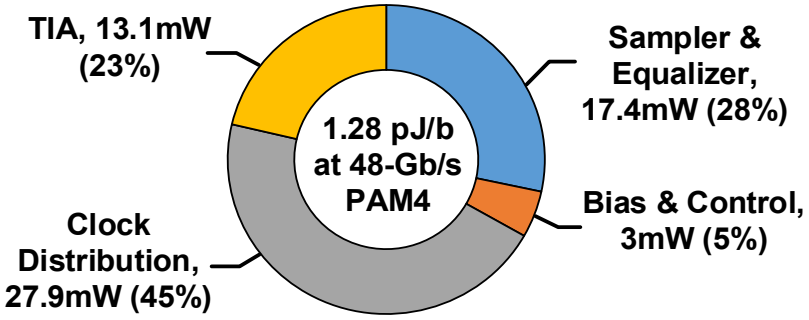


Figure 3.41. ORX power breakdown.

The performance summary and comparison with other high-speed CMOS ORXs are shown in Table 3.1. So far most of the previous works are NRZ ORXs, and only design [16] and [20]

achieved integration of linear TIA and PAM-4 sampler with optical measurement. Compared to previous designs, this work achieves a compact area and favorable energy efficiency at a competitive data rate.

TABLE 3.1

PERFORMANCE SUMMARY AND COMPARISON OF CMOS ORX

Reference	JSSC'21 [41]		OJCAS'21 [20]	JSSC'22 [16]		RFIC'23 [25]	VLSI'24 [42]		This Work	
Technology	65nm CMOS		40nm CMOS	28nm CMOS		28nm CMOS	22nm FinFET		28nm CMOS	
Speed (Gb/s)	16		36	100		42.7	50		48	
Signaling	Duobinary		PAM-4	PAM-4		NRZ	NRZ		PAM-4	
PD Cap. (fF)	180		100	70		N/A	100		60	
PD Responsivity (A/W)	0.8		0.8	1		0.8	0.48		0.75	
NRZ OMA Sens. at BER 1e-12 (dBm)	-11.6		N/A	-11.1 @56Gb/s		-3.6	-6		-8.2 @28Gb/s	
PAM-4 OMA Sens. at BER 2.4e-4 (dBm)	N/A		-4.8*	-8.9		N/A	N/A		-5.1	
RX EQ Capabilities	N/A		2-tap DFE	2-tap FFE + 2-tap DFE		CTLE	CTLE + 2-tap FFE		2-Tap FFE + 2-tap DFE	
Area (mm^2)	0.09		0.23	0.45		0.11**	0.32		0.06	
Power (mW)	4.0 (TIA)	11.2 (ORX)	128.8 (ORX)	117 (TIA)	381 (ORX)	145.2** (ORX)	15.8 (TIA)	75.9 (ORX)	13.1 (TIA)	61.4 (ORX)
Efficiency (pJ/bit)	0.25	0.7	4.0	1.17	3.9	3.4	0.38	1.5	0.27	1.28
FoM	2570		473	1725		889	622		2589	

*Estimated from reported sensitivity curves **CDR included

FOM = Data Rate / Area / Input OMA

3.5 Conclusion

Design techniques to implement compact and power-efficient PAM-4 ORXs are presented in this paper. The relationship between ORX sensitivity and TIA BW under different configurations of post-TIA equalization is studied. A PAM-4 ORX with CMOS linear TIA and PAM-4 samplers integrated using 28-nm CMOS technology is proposed and characterized up to 48 Gb/s. To achieve the design target, a TAS-TIS topology is employed in the TIA design to replace conventional CML-based VGA and post-amp, avoiding CTLE and inductors while preserving the linearity and gain-BW product for PAM-4 operation. As a result, the proposed TIA achieves max. 73.6-dBΩ gain, 14-GHz BW, and over 20-dB gain tuning range with less than 0.2-GHz BW variation. Second, a 2-tap FFE and a 2-tap DFE are integrated at PAM-4 sampler to cancel the precursor and postcursors of TIA differential output, ensuring correct data recovery. By optimizing the clock-to-Q delay of slicers, decision feedback loop is closed up to 30 GBaud. A prototype of the proposed ORX is fabricated in a 28-nm CMOS technology and is wire-bonded to a commercial PD. The ORX achieves -5.1-dBm sensitivity at 48 Gb/s consuming 61.4 mW, with only 13.1 mW contributed from TIA, resulting in 1.28-pJ/bit (0.27 pJ/bit for TIA only) efficiency, while occupying only 0.06 mm2. The presented ORX demonstrates strong potential for future high-density, low-power, and low-cost optical modules.

Chapter 4

A 0.32-pJ/b 100-Gb/s PAM-4 Linear TIA

4.1 Overview

As data center networks scale in BW and physical size, the cost and power consumption of pluggable optical transceivers have risen significantly [43]. Over the past two decades, data rates in pluggable optical modules have increased by three orders of magnitude, yet energy efficiency has improved by only two orders of magnitude [44]. Further scaling of energy efficiency and BW density remains challenging due to limited integration in conventional pluggable optical modules [45]. To address this, recent works explore compact, highly integrated optical transceivers assembled near the host, which is a departure from the traditional pluggable module approach. Compared to optical transceivers with integrated retimers or digital signal processers (DSPs), recent advancements in linear drive optics have enabled 100G/lane performance in both LPO and CPO form factors [46], [47]. Fig. 4.1 (a) and (b) illustrates the building blocks of transmission links employing retimed and linear drive optics, respectively. By replacing the DSP with the highly integrated linear transceiver front-end, linear optics eliminate the need for signal regeneration between link segments, resulting in significant reductions in power, cost, and latency.

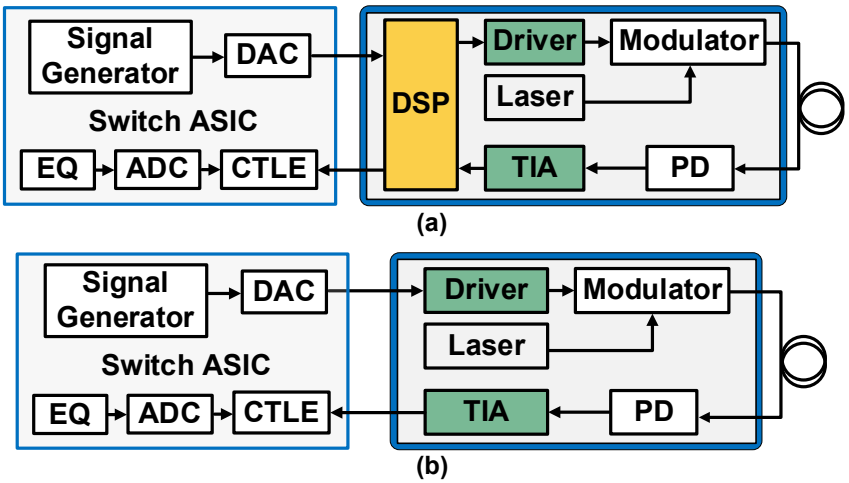


Figure 4.1. Block diagrams of transmission links with (a) retimed and (b) linear drive optics.

On the ORX side, the front-end TIA plays a critical role in determining the noise, BW, linearity, and power consumption of optical links used in data centers. Recent preferences from industry for LPO show the trend to substitute power-intensive DSP with a linear TIA incorporating equalization function to mitigate the channel loss, resulting in reduced cost, area, power consumption, and latency. CMOS TIA also brings the advantage of higher-level CMOS integration and shows severely reduced power consumption compared to SiGe BiCMOS counterparts. Although the design of CMOS linear TIA for a 100 Gb/s per lane link is drawing more attention, meeting requirements of PAM-4 signals in scaled CMOS process is challenging due to smaller transconductance per unit current, lower intrinsic gain, and limited supply voltage compared to SiGe BiCMOS process. Figure 4.2 shows the simulated intrinsic gain (g_m/g_{ds}) for transistors with low threshold voltage (LVT) of both 22-nm and 28-nm technologies, in which the gain is lower than 10 in most cases. The maximum intrinsic gain for 28-nm NMOS is 9.78 at 59 µA/µm, and it is only 7.82 for PMOS at 58 µA/µm. Such a low intrinsic gain makes design of analog building blocks such as operational amplifier and CML-based circuits difficult and less effective.

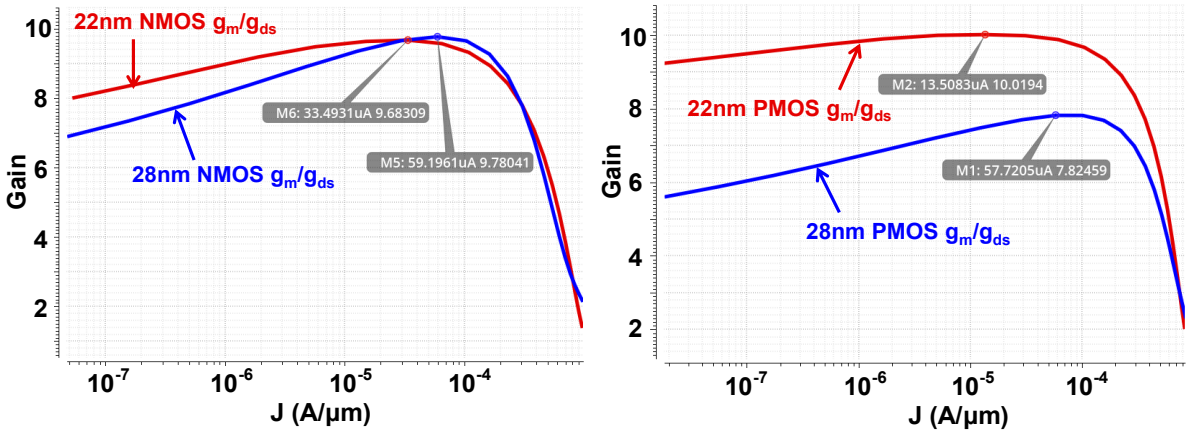


Figure 4.2. Simulated intrinsic gain of 22-nm and 28-nm CMOS.

Inverter-based design becomes more and more suitable in deep sub-micron CMOS technologies taking advantage of high f_T of PMOS. As shown in Figure 4.3, f_T of NMOS and PMOS in a 28-nm CMOS process is up to 332 GHz at 400 µA/µm and 287 GHz at 310 µA/µm, respectively, which is much higher than the one in 40-nm CMOS process (lower than 260 GHz

for NMOS and 210 GHz for PMOS). The improvement of PMOS speed due to technology scaling gradually replaces NMOS only designs.

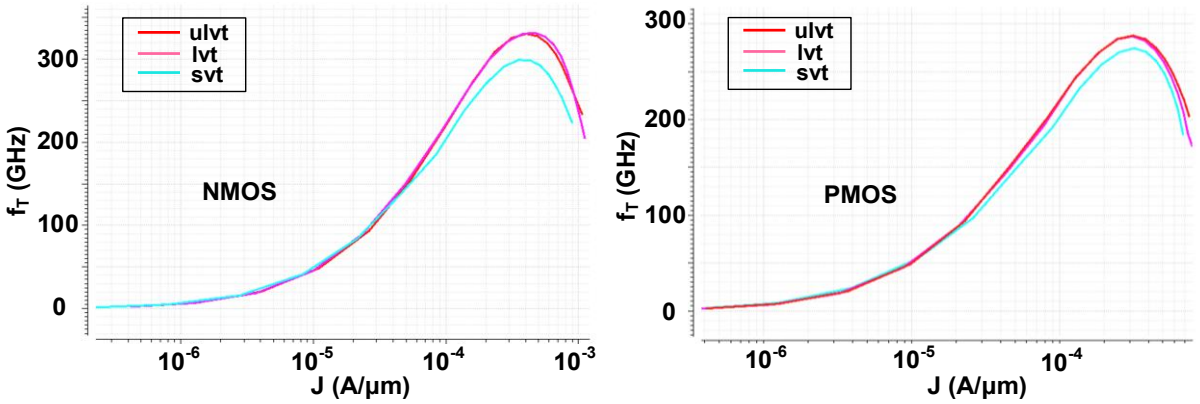


Figure 4.3. Simulated f_T of NMOS and PMOS in a 28-nm CMOS process.

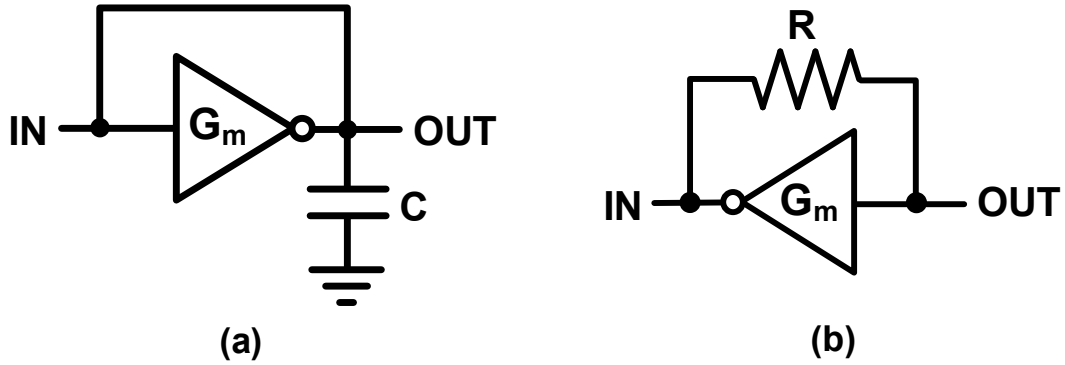


Figure 4.4. (a) Inverter-based G_m-C filter. (b) Inverter-based active inductor.

SF inverter-based topology has already been commonly used in designing the first TIS of CMOS TIA [14], [48]. Furthermore, inverter-based filters have shown potential for area reduction while maintaining low power, which are adopted in both electrical and optical links to replace conventional CML-based CTLEs [15], [49]. Figure 4.4 shows two inverter-based building blocks: a G_m-C filter and an active inductor. The former one provides a pole located at G_m/C, and the latter one as the load provides an impedance derived in Appendix A to be

$$Z_L = \frac{1}{G_m}\frac{1+sRC_{gs}}{1+s\frac{C_{gs}}{G_m}} \approx \frac{1}{G_m} + s\frac{RC_{gs}}{G_m} \tag{4.1}$$

which is a resistance of $1/G_m$ in series with an inductance of RC_{gs}/G_m, where C_{gs} is the

total gate capacitance of the inverter. Two kinds of buffers using diode connected load and active inductor load are also compared and shown in Figure 4.5. The first stage can be programmable resulting in a gain of kG_m, and considering load capacitance C_L, the transfer function of these two buffers can be expressed as

$$H_{diode}(s) = \frac{k}{1 + s\frac{C_L + C_{gs}}{G_m}} \tag{4.2}$$

$$H_{ind}(s) = k\frac{1 + sRC_{gs}}{1 + s\frac{C_{gs}C_L}{G_m} + s^2\frac{RC_LC_{gs}}{G_m}} \tag{4.3}$$

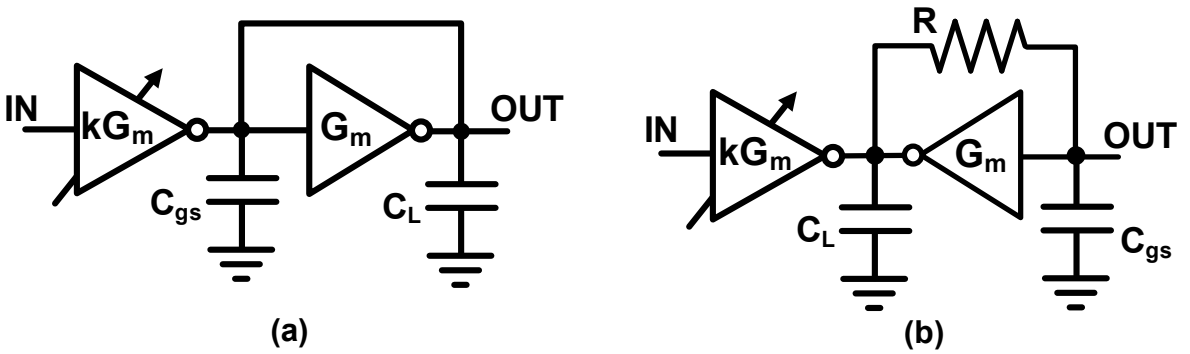


Figure 4.5. Buffers with (a) diode connected load and (b) active inductor load.

Scaling and complementarity of CMOS technology also bring benefits to some classic circuit topologies, e.g., the Cherry-Hooper amplifier shown in Figure 4.6. The original Cherry-Hooper amplifier which incorporates local feedback in the drain network to improve speed has been extensively used in broad applications [50]. The low-frequency voltage gain is given by

$$\frac{V_{out}}{V_{in}} = g_{m1}R_F - \frac{g_{m1}}{g_{m2}} \tag{4.4}$$

If $R_F \gg 1/g_{m2}$, then the gain is equal to that of a simple common source stage having a load resistance of R_F [50]. The key advantage of the circuit lies in the small-signal resistance seen at nodes X and Y. As derived in Appendix B, the resistance for both nodes is equal to $1/g_{m2}$. Thus, pole frequencies are on the order of $\omega_{p,X} \approx g_{m2}/C_X$, $\omega_{p,Y} \approx g_{m2}/C_Y$, yielding only high-frequency poles.

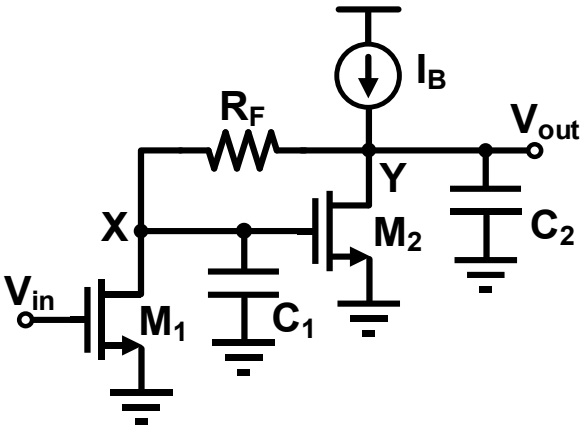


Figure 4.6. Schematic of a Cherry-Hooper amplifier.

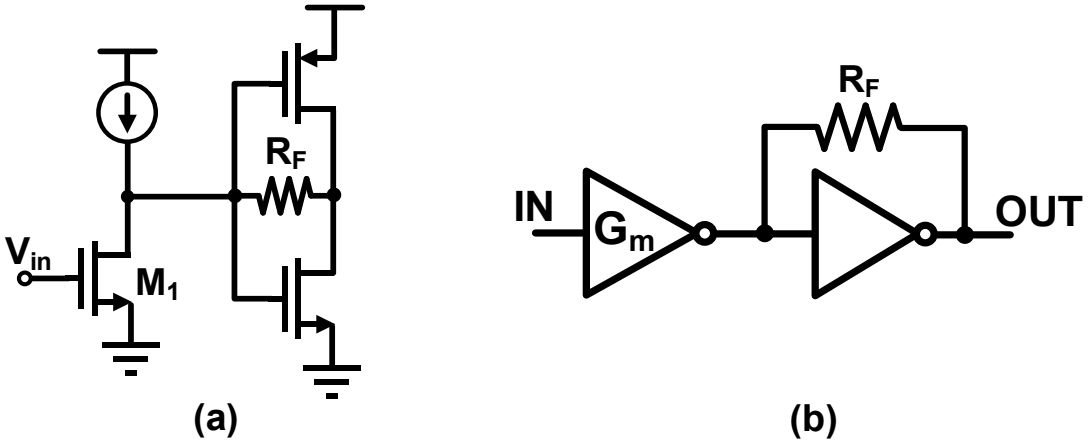


Figure 4.7. Modified Cherry-Hooper amplifiers. (a) Its second stage is replaced by an inverter-based TIA. (b) Inverter-based Cherry-Hooper amplifier.

The NMOS-only circuit in Figure 4.6 now can be modified to the circuit shown in Figure 4.7 (a), keeping the first input stage with NMOS but incorporating PMOS at the second stage to form an inverter-based SF TIA, which has been used in prior deep sub-micron designs [17], [34], known as the TAS-TIS topology as introduced in Chapter 3. By incorporating PMOS at the first stage, the inverter-based TAS provides larger transconductance and better linearity compared to the NMOS-only input stage. In this way, an inverter-based TAS-TIS topology is formed suitable for advanced CMOS process.

Under the scenario of LPO, equalizers should be incorporated into a TIA, and a CTLE becomes a good choice for 100-Gb/s+ TIA design to extend the BW. The stringent BW requirements also make passive inductors and T-coil loads a must. High inductance density and

self-resonance frequency (SRF) are imperative to minimize circuit size and increase BW in broadband applications, such as CML with a shunt-peaking load. Standard inductors included in the process design kit (PDK) of foundries do not meet these requirements. These standard inductors usually use a single metal layer to wind inductors, which results in low inductance density. Therefore, innovative techniques are necessary to design inductors with high inductance density and SRF for broadband applications. Nevertheless, multi-stage peaking provided by either CTLEs or passive inductors in high-speed CMOS TIA design mainly focuses on the optimization of BW and noise, ending up with large area, high power or poor linearity. In this work, BW-noise-power tradeoff is further relaxed by taking advantage of scaling and complementarity of CMOS technology in TIA design without sacrificing linearity performance and total area, and the design achieves the best energy efficiency among similar bulk CMOS designs.

4.2 System Architecture

Fewer components in the TIA help achieve high BW and low power consumption. Nevertheless, the following key blocks should be retained to meet basic requirements: a TIS at the first stage to convert current to voltage, a CTLE to expand the BW, a VGA to accommodate a large input dynamic range, and an output buffer for off-chip measurements. S2D circuit may also be added, depending on where the signal is converted to differential, as shown in Figure 4.7. The signal can be converted to differential right after the TIS as the one in Chapter 3 [12], or after the CTLE, or before the output buffer [15]. Alternatively, the signal can be kept single-ended through the TIA [31], but a S2D circuit is still needed at the subsequent SerDes IC [42]. At high data rates, CTLE itself consumes increasingly high power, typically accounting for over 25% of TIA power consumption [51]. The CTLE and VGA in configuration of Figure 4.8 (a) almost doubles the power consumption compared to the configuration in Figure 4.8 (d), while the signal in Figure 4.8 (c) is too sensitive to supply variations with poor common-mode rejection, which is not preferrable. As a compromise, a single-ended CTLE can significantly reduce the overall power consumption of the TIA while the TIA is not too sensitive to supply and common-mode votlages. Therefore, in this design, a single-ended CTLE followed by a S2D conversion

amplifier is chosen.

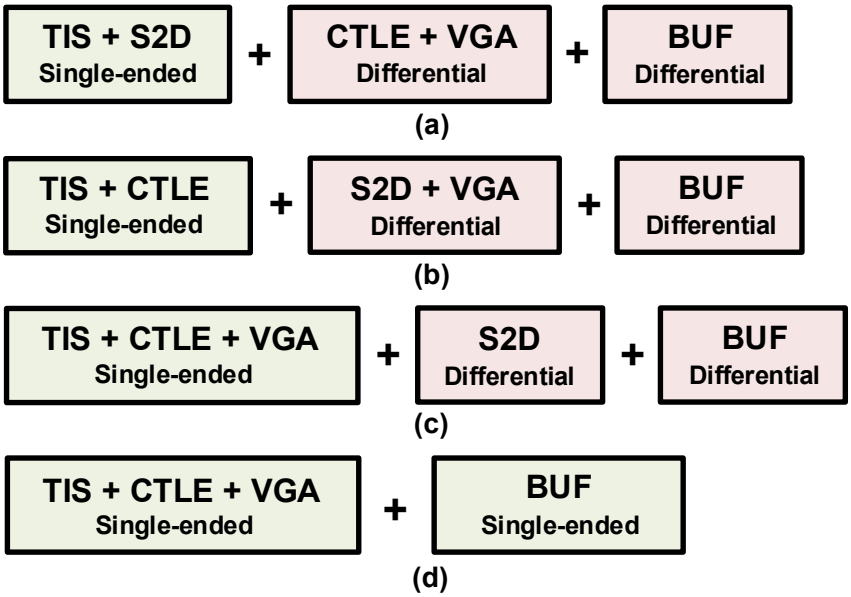


Figure 4.8. TIA system design choices. Convert the signal to differential (a) right after the TIS, or (b) after the CTLE, or (c) before the output buffer. (c) Keep the signal flow to be single ended through the TIA.

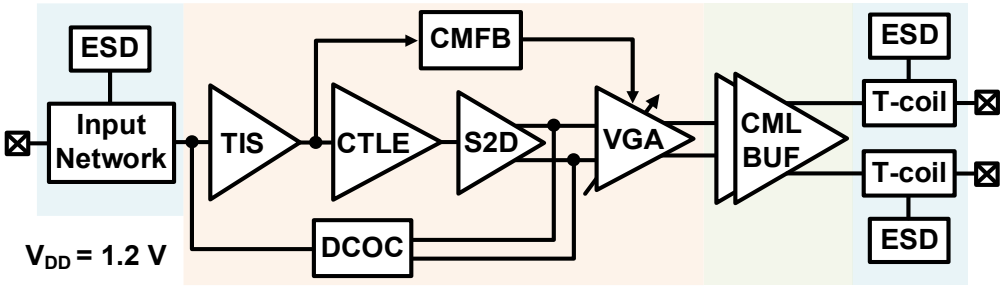


Figure 4.9. Block diagram of the proposed TIA.

Figure 4.9 shows the overall block diagram of the proposed TIA. The signal path is composed of a TIS, followed by a CTLE and a S2D conversion amplifier. Once the signal is differential at the S2D output, a VGA accommodates the required dynamic range, and a two-stage CML buffer with 0-dB gain drives outputs for off-chip measurements. A common-mode feedback (CMFB) loop guarantees the common-mode voltage of the VGA is the same as the output of the TIS. T-coils at input and output of TIA with the center-tap connected to ESD diodes are inserted to accommodate parasitics and extend the BW. A DCOC loop subtracts the input-

referred offset voltage, and a common-mode feedback loop provides the common-mode voltage to the VGA.

4.3 Building Blocks

4.3.1 TIS with Multi-peaking Network

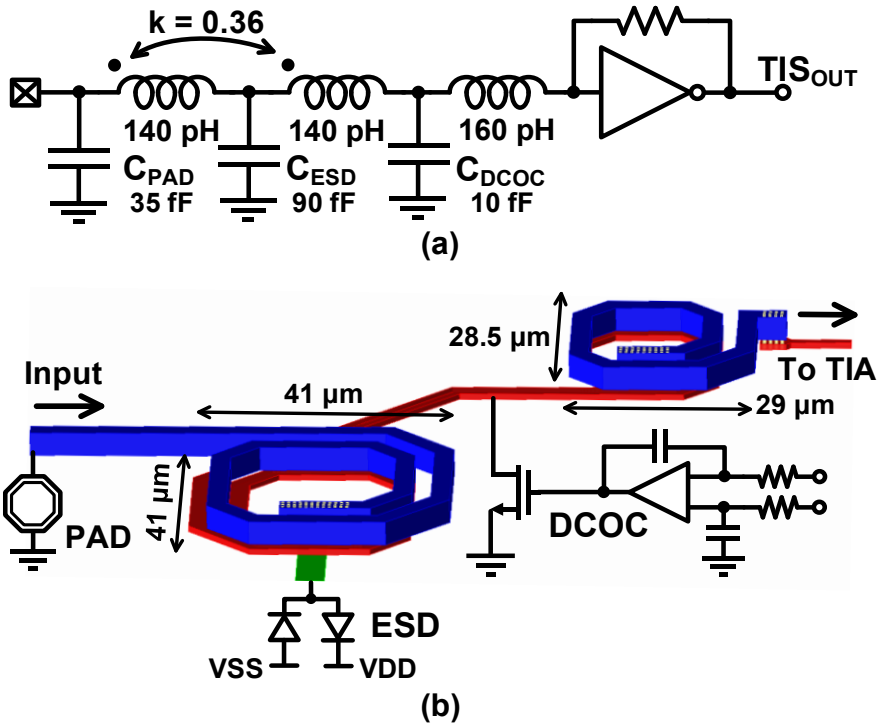


Figure 4.10. (a) Schematic of the SF TIS with multi-peaking input network. (b) 3D layout of the proposed network.

An inverter-based SF TIS is used as the first stage of TIA. To counteract the degradation of BW from the parasitics of input pad, ESD diodes and DCOC circuit, a multi-peaking input network comprised of a T-coil in series with an inductor is implemented as shown in Figure 4.10 (a). Parasitic capacitance C_{PAD}, C_{ESD}, C_{DCOC}, and input capacitance of TIS are distributed by the network. Multi-layer T-coil and inductor are custom-designed in the network to achieve a compact layout as shown in Figure 4.10 (b). T-coils can create a constant, resistive input impedance suitable for ESD protection circuits [52]. The T-coil consists of two coupled inductors with ESD protection devices connected to the center tap. The top two relatively thick metal layers (M9, M8) are used to prevent significant reduction in Q and SRF, and a thin layer

M7 is used as the center tap of the T-coil to connect with ESD diodes. Suitable selection of inductor width (3 µm) and number of vias ensures reliable handling of input current. The multi-peaking network provides a good broadband impedance matching in the presence of a heavy load capacitance. As shown in Figure 4.11, without the input network, S11 is worse than -5 dB at frequencies above 16 GHz, while it is better than -10 dB at frequencies up to 60 GHz. Since thermal noise caused by shunt resistor scales cubically with the BW [27], a large shunt resistor is chosen to reduce the BW and allows for lower input referred noise. The TIS with input network provides a gain of 53.6 dBΩ and BW of 7.1 GHz.

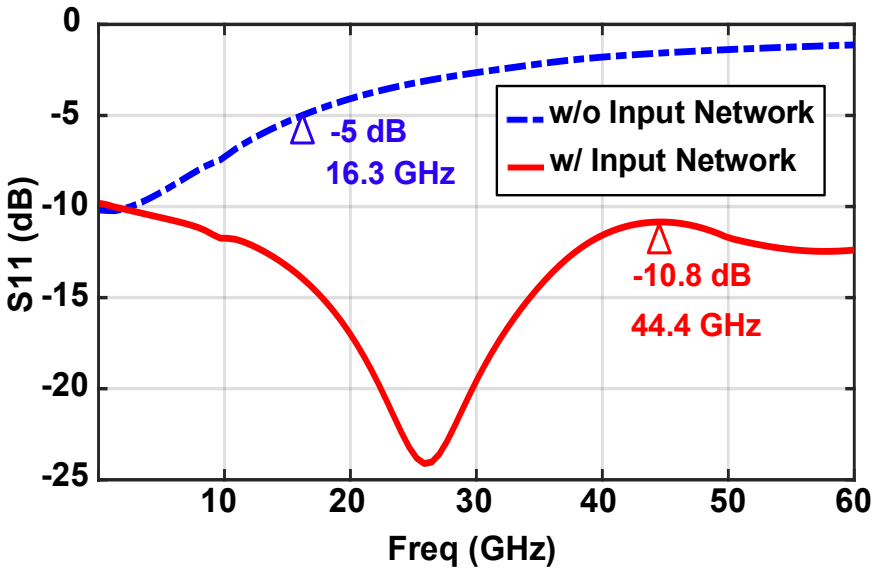


Figure 4.11. Simulated S11 without and with the multi-peaking input network.

4.3.2 CTLE and S2D

Subsequent CTLE restores the overall BW up to 34 GHz. Instead of using CML-based structures, a single-ended inverter-based CTLE is adopted with a peaking frequency of 31.4 GHz, and only one inductor is involved. The CTLE engages two parallel paths, where one path contains a pole at $g_{m1}/(C_{H1}+C_{H2})$ generated by a G_m-C filter, as shown in Figure 4.12 (a). The CTLE creates peaking by subtracting the low-pass path from the main path [43]. 3-bit dc gain control and 2-bit middle-frequency (MF) tuning are implemented by programmable g_m and a capacitor bank C_{H2}. An inverter-based active inductor load as introduced in Section 4.1 followed by a passive series-peaking inductor further expands the BW. Multi-layer layout using

M9 and M8 is also implemented to achieve a compact inductor as shown in Figure 4.12 (b).

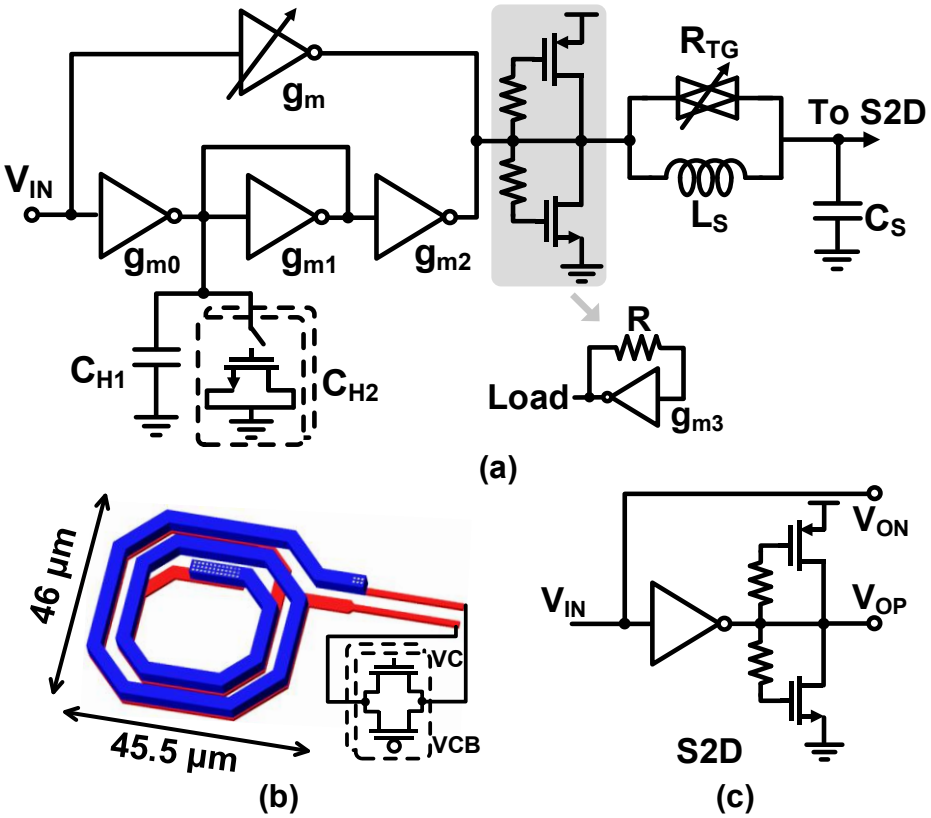


Figure 4.12. (a) Schematic of the inverter-based CTLE with series peaking. (b) 3D layout of the series peaking inductor. (c) Schematic of the inverter-based S2D amplifier.

The transfer function of the CTLE with an active inductor can be given by

$$H(s) = [H_M(s) - H_L(s)] \cdot L_{Active}$$
$$= \left[g_m - \frac{g_{m0}g_{m2}}{g_{m1}} \cdot \frac{1}{1 + s\,(C_{H1} + C_{H2})/g_{m1}}\right] \cdot \frac{sRC_{gs}}{2g_{m3}} \quad (4.5)$$

where $H_M(s)$ and $H_L(s)$ are transfer functions of main and low-pass paths respectively, and C_{gs} is the capacitance between gate and source of the active inductor. The load capacitance of the active inductor is ignored here for simplicity. By tuning g_m and C_{H2} in Eq. (4.5), both the peaking gain and profile can be tuned. To accommodate BW variation of TIA caused by the variation of bond wires and input capacitance, inductor Q-shaping is implemented [53] where programmable transmission gates R_{TG} in parallel with a 670-pH inductor L_S are used to tune the quality factor of series peaking, realizing high-frequency (HF) tuning. Assume parasitic

capacitance C_S and L_S resonate and cause a high-frequency peaking at ω_{PK}, the relationship between the quality factor of the resonator Q_tank and resonant BW is given by

$$\frac{1}{Q_{tank}} = \frac{1}{Q_{ind}} + \frac{\omega_{PK} L_S}{R_{TG}} + \frac{1}{Q_C} = \frac{BW_{3dB}}{\omega_{PK}} \tag{4.6}$$

Q_{ind} and Q_C of Eq. (4.6) represent the quality factor of L_S and C_S. By changing the value of R_{TG}, resonant BW is changed and thus the high-frequency peaking strength can be changed. The S2D amplifier in Figure 4.12 (c) is implemented by a unity gain buffer with active inductor load as introduced in Section 4.1. Figure 4.13 shows post-layout simulation results of transimpedance responses for CTLE, TIS, and signals at input and output of the S2D amplifier. The CTLE creates a 6-dB peaking gain at 31.3 GHz, and at the S2D output, a 59.9-dB dc gain is achieved with 33.6 GHz BW.

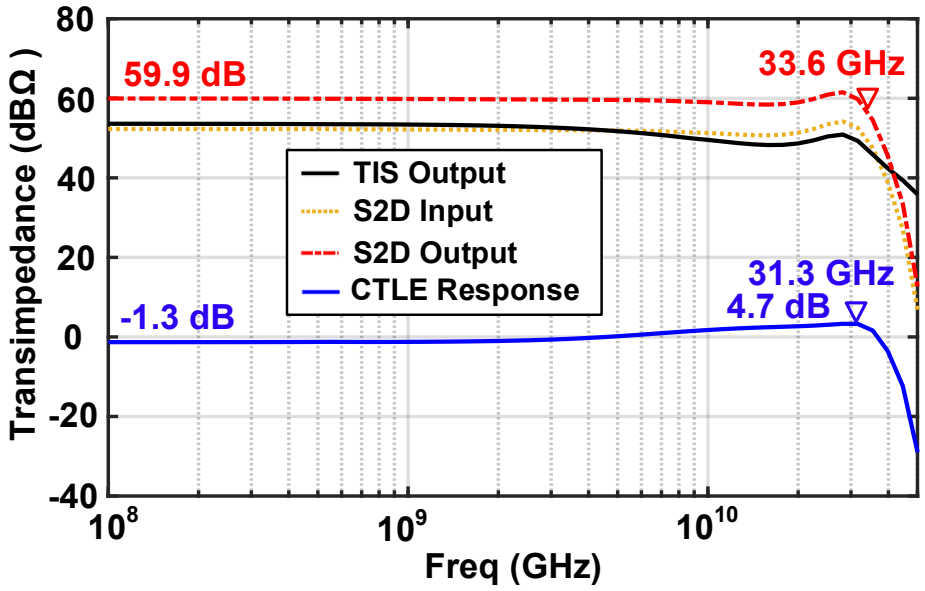


Figure 4.13. Simulated frequency responses of the CTLE, the TIS, and signals at input and output of the S2D circuit.

4.3.3 VGA

Gilbert-cell-based VGAs are commonly used in linear TIAs to realize a wide input dynamic range. However, limited by the gain-BW product of the structure, shunt inductive peaking is usually required to expand the BW as described in Chapter 3. Furthermore, the NMOS- or

PMOS-only differential input pair degrades linearity with large input signal swing. For instance, for preceding stages with a total gain of 60-dBΩ, the amplitude of VGA input can be up to 500 mV_{pp} (500 μA_{pp} input current). Modified Cheery-Hooper amplifiers which consist of an inverter-based TAS, and an inverter-based SF TIS are adopted as VGAs in recent designs by either controlling the transconductance Gm of TAS [42] or changing the shunt resistor R_F of TIS [17]. Such a TAS-TIS topology provides a larger gain-BW product and both the TAS and the TIS use CMOS input pairs to accommodate a large input swing. However, changing Gm to control VGA gain limits the dynamic range. If the Gm of TAS is too small, the overall linearity is degraded, which sets a lower limit of Gm value, and only enlarging the upper limit of Gm is possible to increase the control range, which however increases power. Changing R_F only to control the TAS-TIS VGA has been discussed in Chapter 3, where the fine-tuning would inevitably involve too many resistors to reduce the LSB, bringing too much parasitics and causing BW degradation.

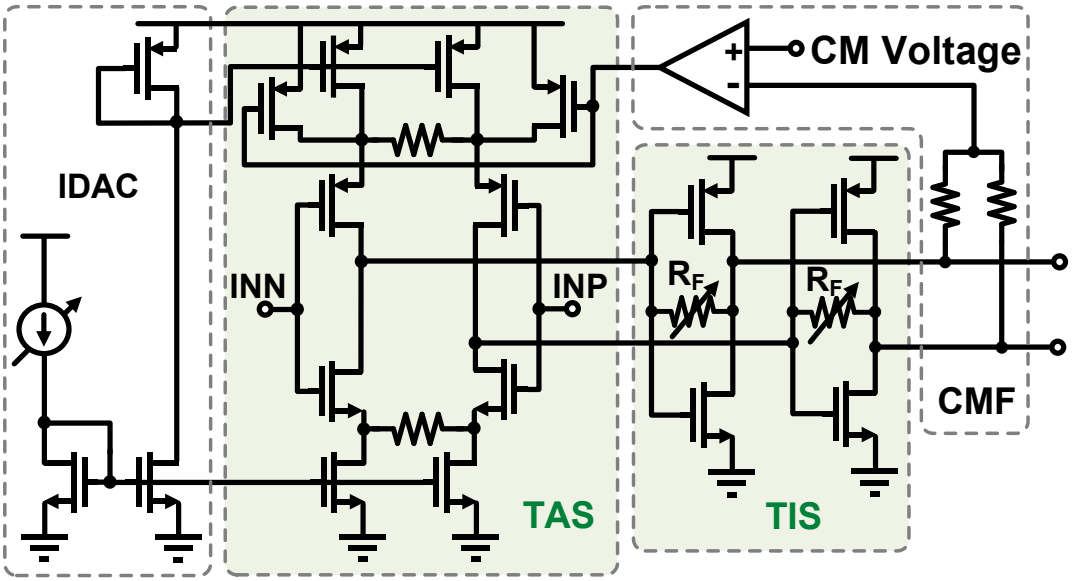


Figure 4.14. Schematic of the proposed current reuse VGA employing the TAS-TIS topology.

Figure 4.14 shows the schematic of the proposed current reuse VGA employing the TAS-TIS topology which combines the tunability of both Gm and R_F. 2-bit R_F control and 3-bit Gm control are implemented for coarse tuning and fine tuning, respectively. Therefore, only two resistors are required, avoiding severe BW variation at different gain settings, and parasitics

from the resistor bank are limited. Controlled by a 3-bit current DAC, the bias current of TAS is maintained at a relatively high value, ensuring linearity performance. Compared to a pseudo-differential inverter-based TAS, tail current sources are added here to improve the common-mode rejection of S2D output signals and increase immunity to supply variations though the voltage headroom is reduced. Source degeneration resistors are used to further enhance linearity. Both passive and active inductors are avoided in the VGA design to achieve a compact and low-noise design. For a TIA input amplitude of 600 μA_{pp}, simulated eye diagrams of 100-Gb/s PAM-4 at both the VGA input and output are depicted in Fig. 4.15 (a) and (b), respectively. Despite the VGA input signal amplitude being above 420 mV_{pp}, a ratio level mismatch (RLM) of over 96% is still achieved at VGA output with a 520-mV_{pp} amplitude, demonstrating excellent linearity performance of the signal flow.

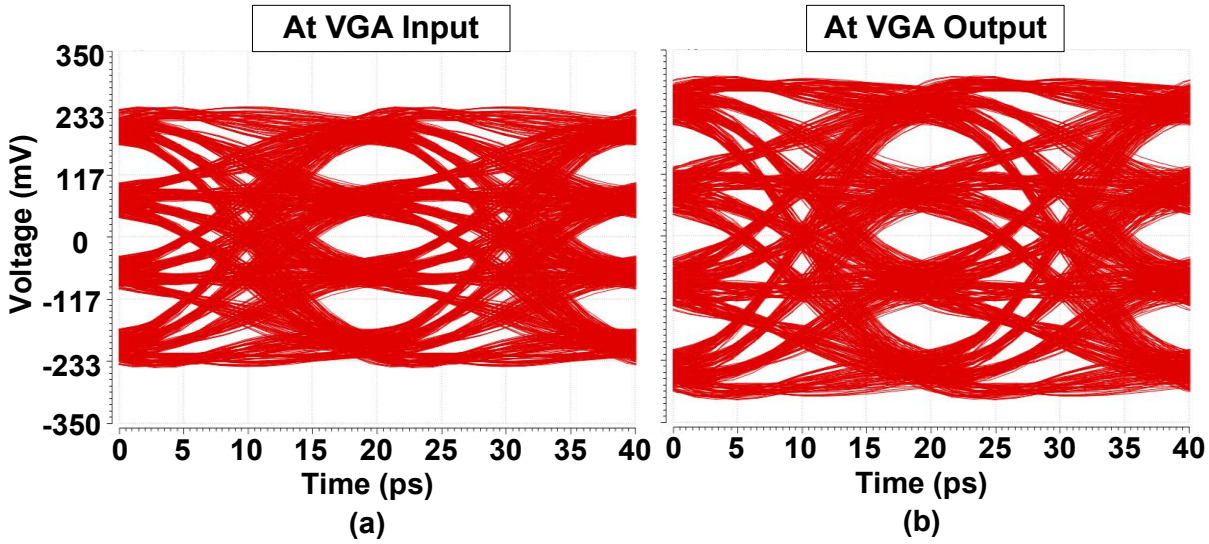


Figure 4.15. Simulated eye diagrams of 100-Gb/s at (a) VGA input, and (b) VGA output, with a TIA input amplitude of 600 μApp.

Figure 4.16 shows the layout of the TIS, the CTLE, the S2D, and the VGA, except passive inductors. The area is only 0.19 × 0.09 mm^2, mainly occupied by capacitors in DCOC circuits and CMFB loops. At tt corner, the TIA except the output buffer achieves a maximum gain of 66.6 dB with a BW of 31.0 GHz, and a minimum gain of 57.8 dB, with a BW of 33.8 GHz.

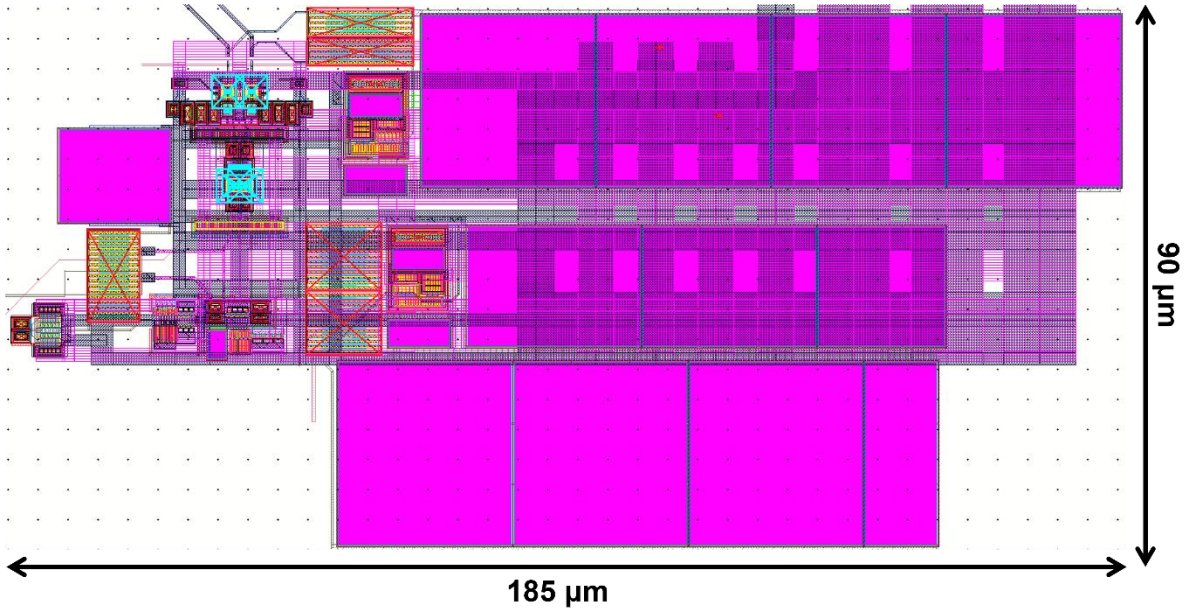


Figure 4.16. Layout of the TIS, the CTLE, the S2D, and the VGA, except passive inductors.

4.3.4 Output Buffer

A CML output buffer which consists of two cascaded differential pairs with shunt-inductive peaking is inserted to drive a 50-Ω off-chip load as shown in Figure 4.17. Multi-layer T-coils are also used to compensate for ESD capacitance at output pads. Both single-ended and differential inductors can be used as shunt-peaking inductors in CML buffers [12], [15], and their selection depends on specific circuit requirements. Differential inductors provide superior common-mode rejection and noise immunity in differential circuits compared to the use of two single-ended inductors [54]. On the other hand, single-ended inductors offer higher inductance density and SRF. If using differential inductors for this design, two 1.4-nH inductors will be required, and the SRF of them is lower than 40 GHz which is only slightly higher than Nyquist frequency of the TIA which is 25 GHz. Therefore, 700-pH multi-layer stacked single-ended inductors are used. To maximize the self-shielding property and thus SRF of the proposed stacked inductors, the layout at different metal layers (M9 and M8) has maximum vertical overlap. Figure 4.18 shows the simulated inductance and quality factor of the single-ended inductor used in the first stage of output buffer, where the low-frequency inductance of each inductor at the first and the second stage buffer is 731 pH and 715 pH, respectively, and the corresponding SFR is 42.5 GHz and 43.4 GHz.

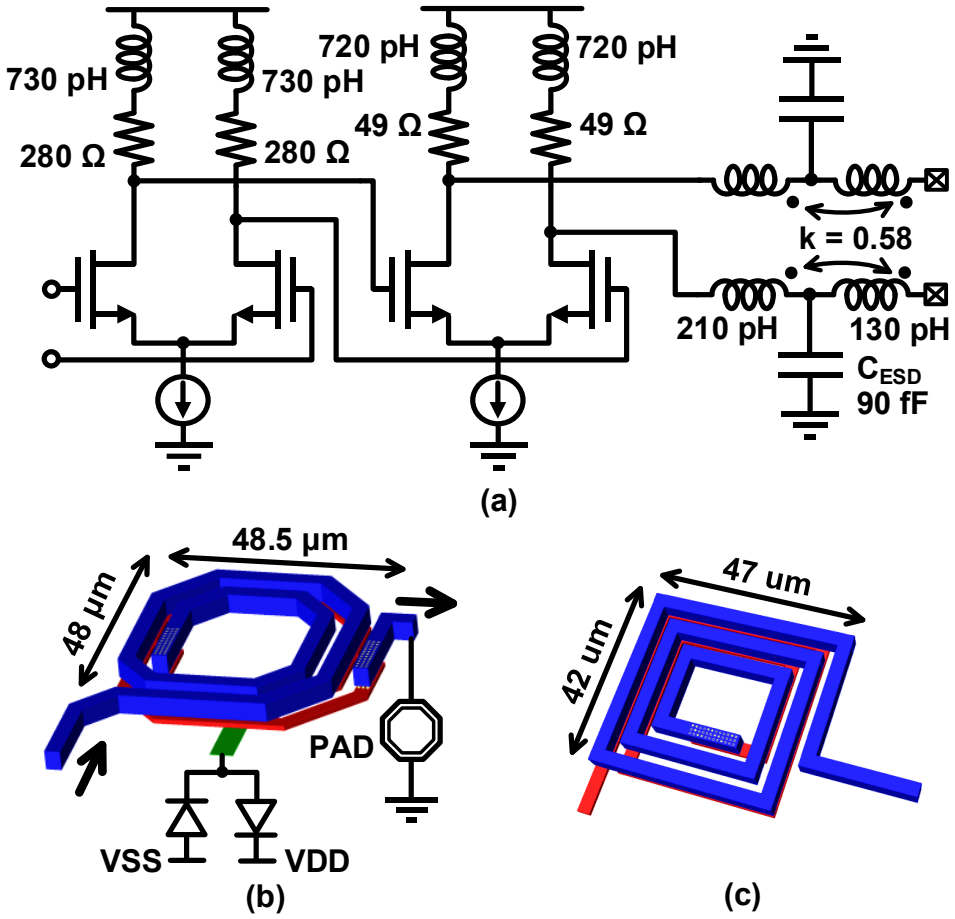


Figure 4.17. (a) Schematic of the output buffer. 3D layout of (a) the T-coil and (b) the single-ended shunt-peaking inductor.

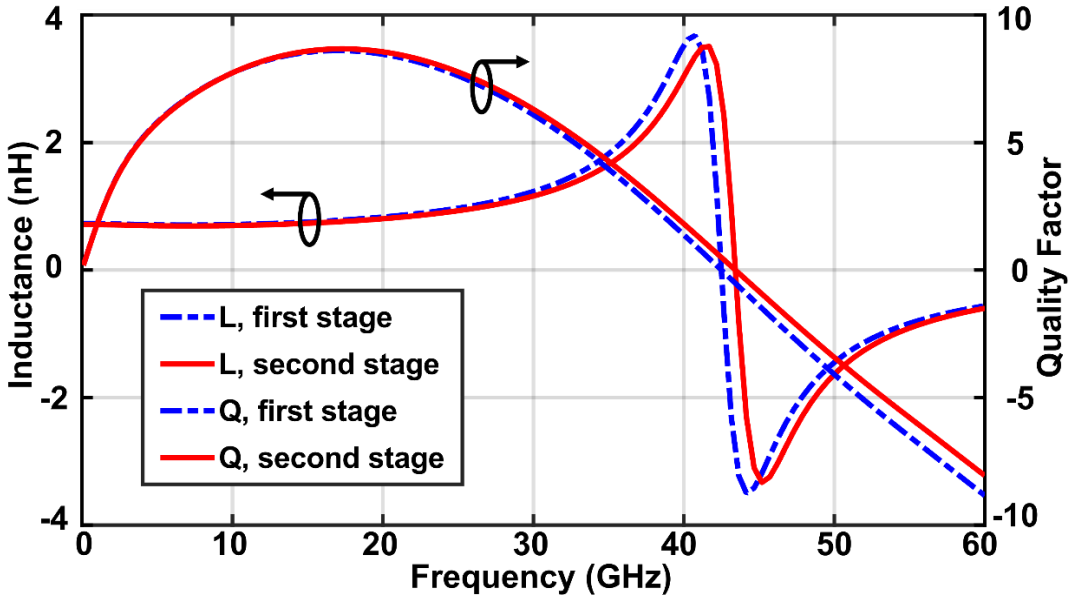


Figure 4.18. Simulated inductance and quality factors of the inductor used in the output buffer.

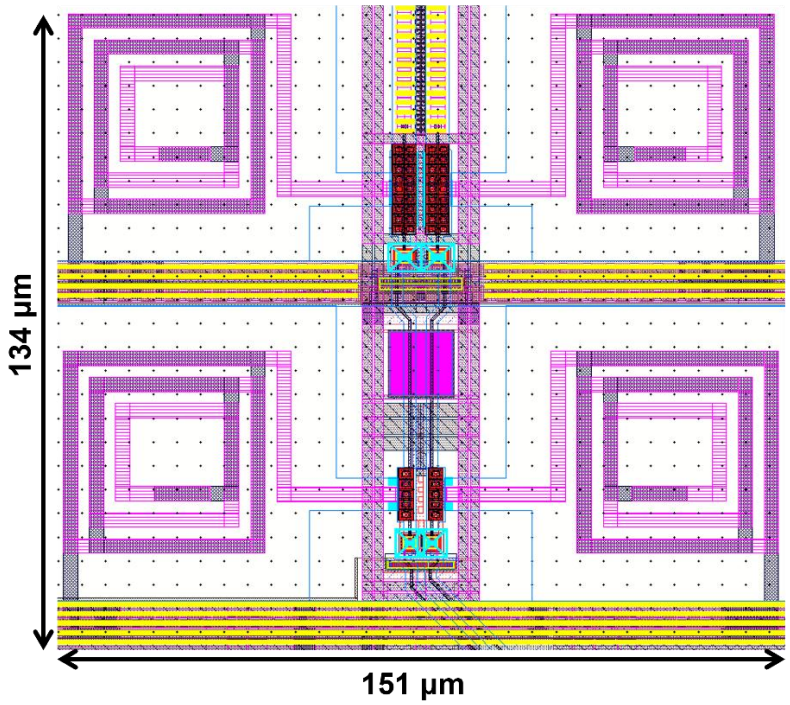


Figure 4.19. Layout of the two-stage output buffer.

The layout of CML circuits employing shunt-peaking single-ended inductors is depicted in Figure 4.19, occupying an area of 0.15 x 0.13 mm^2 area even though four inductors are used. The output buffer with T-coil and ESD diodes provides ~0-dB gain with a BW of 42 GHz. The total transimpedance response in the post-layout simulation is shown in Figure 4.20. The TIA achieved a max. gain of 66.1 dBΩ and a BW up to 31.7 GHz.

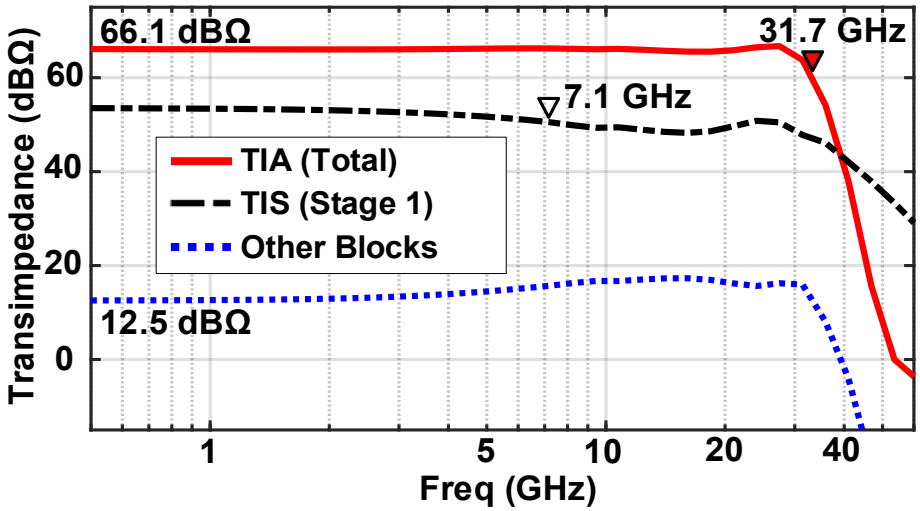


Figure 4.20. TIA frequency response in post-layout simulation.

4.3.5 COB and High-Frequency PCB

Limited by the equipment and testing environment, the chip is wire-bonded to a high-frequency PCB for time-domain measurements. Input and output signals must go through bonding wires, PCB traces, and RF connectors before reaching the chip or any equipment. However, up to 25-GHz Nyquist frequency, high-frequency loss and broadband impedance matching would cause severe degradation to signal quality, and careful design of chip on board (COB) and PCB traces become vital to ultimate performance. 10-mil thick RO4350B material is chosen for laminates to design a 4-layer high-frequency PCB. The substrate of the 4-layer high-frequency PCB is shown in Figure 4.21. Coplanar waveguides are chosen as on-PCB transmission lines to achieve a 50Ω matching up to 30 GHz. The width and gap are calculated to be 16 mil and 6 mil for certain substrate parameters. Figure 4.22 shows the final version of the high-frequency PCB, including the package of RF connectors. The gap between the signal path and ground is kept the same till the connectors to avoid impedance discontinuity and reduce signal reflection. Multiple vias are added to ensure good contact with the ground.

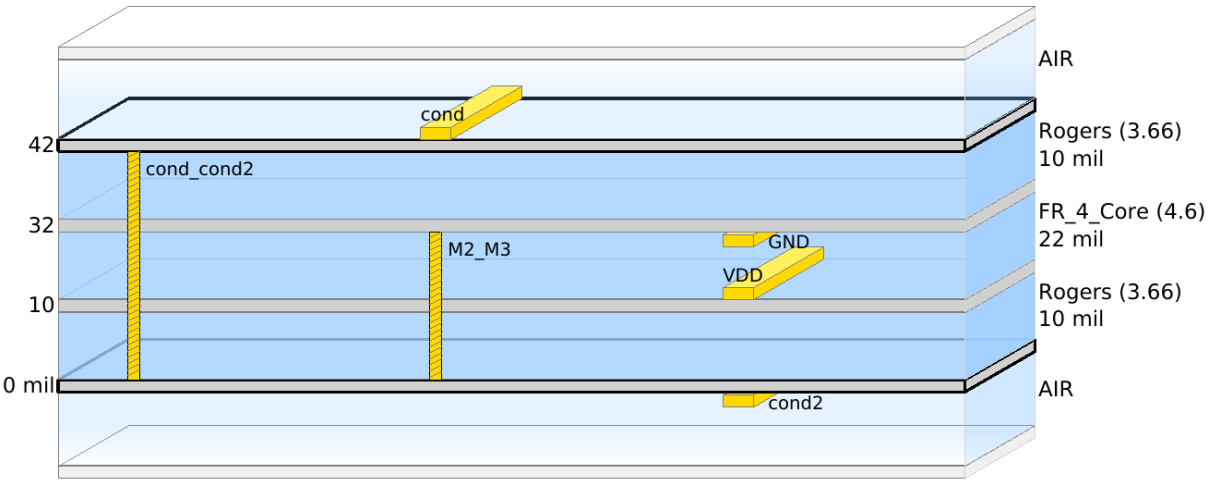


Figure 4.21. 4-layer high-frequency PCB stackup.

Gold fingers connecting the chip and PCB traces are carefully designed. Though the tight space makes a 16-mil golden finger impossible for signal traces, the width of gold fingers for input and output signals are optimized and enlarged to 12 mil to reduce the damage to impedance matching. The PCB is trenched to accommodate the TIA die as shown in Figure

4.22, so that the height difference between the TIA and the PCB can be minimized. In this way, the length of bond wires connecting the TIA and the PCB can be reduced to relieve the BW degradation due to parasitics of bond wires.

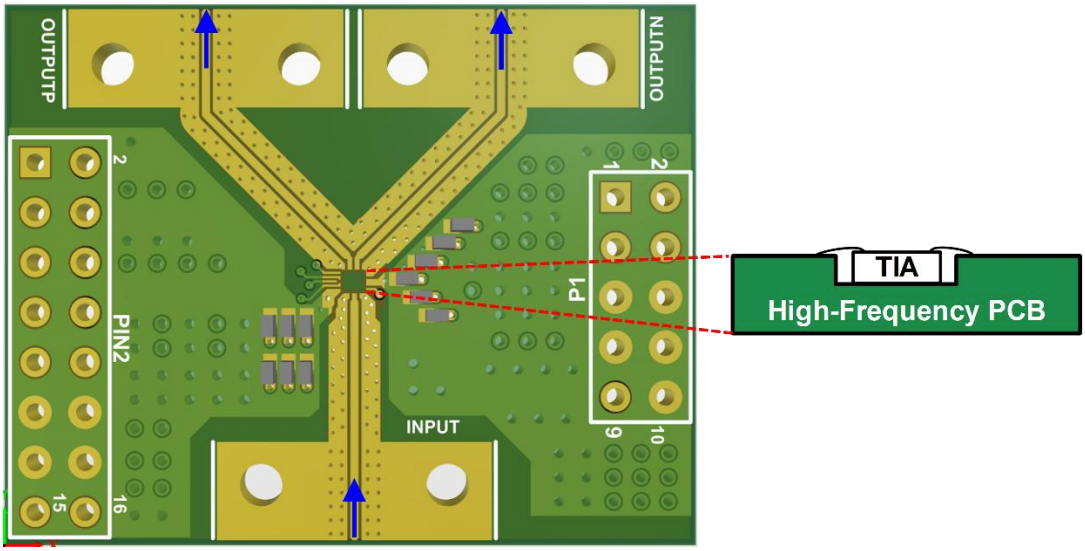


Figure 4.22. High-frequency PCB layout.

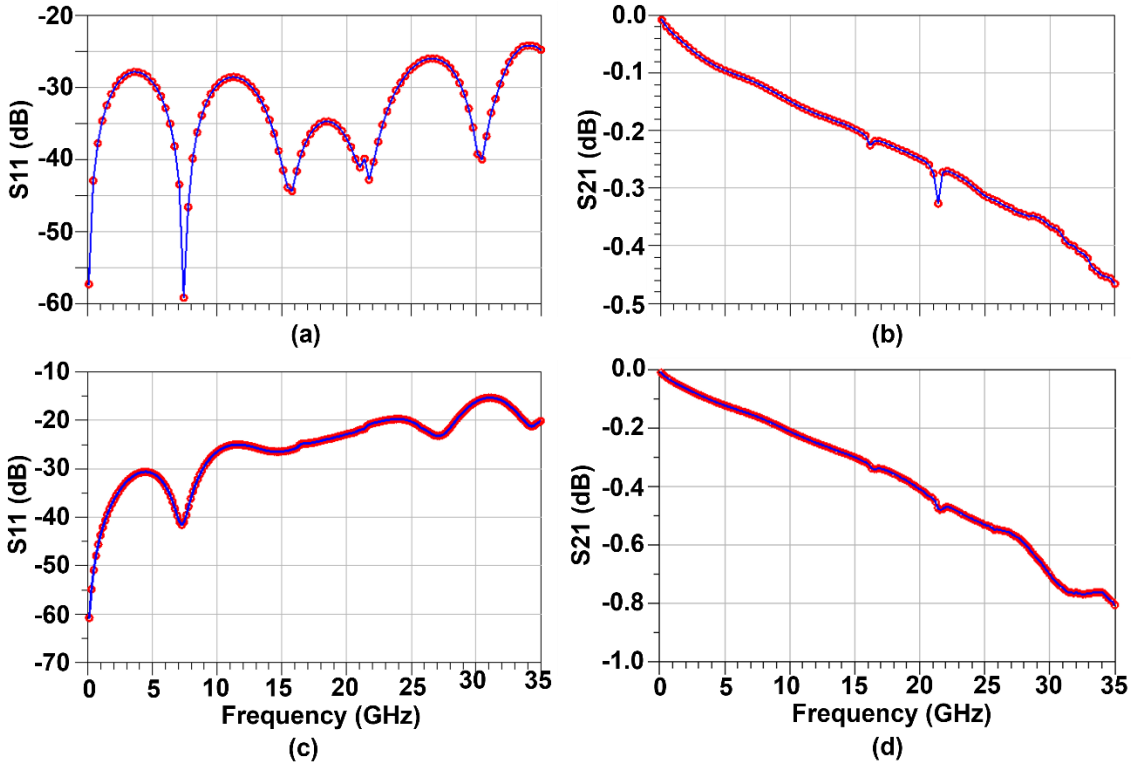


Figure 4.23. (a) Simulated S11 and (b) S21 of the input PCB trace. (c) Simulated S11 and (d) S21 of the output PCB trace.

Simulation results of input and output PCB traces including golden fingers are shown in Figure 4.23. S11 is lower than -20 dB and -10 dB for input and output traces up to 35 GHz, and the loss at 25 GHz is lower than -0.4 dB and -0.6 dB, respectively, ensuring that the signal quality is not affected by the PCB traces.

4.4 Measurement Results

The TIA chip is fabricated in a 28-nm bulk CMOS technology with a die size of 0.69 × 0.53 mm^2 defined by the pad frame. Figure 4.24 shows the die photo and the core area. The chip consumes 26.6 mA from a 1.2 V dc power supply and the power consumption is 32 mW as illustrated in Figure 4.25.

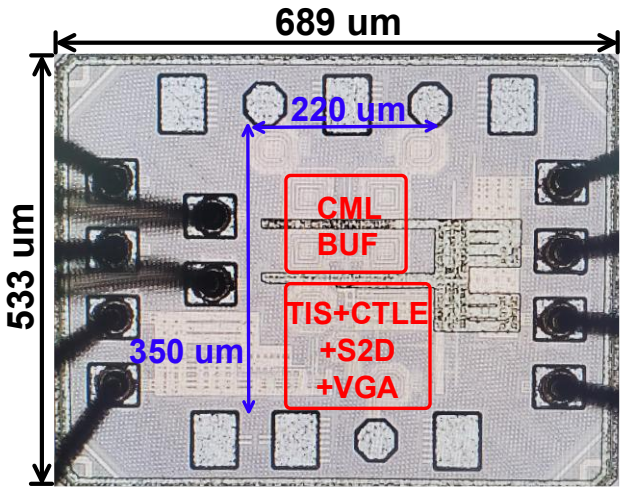


Figure 4.24. Micrograph of the TIA.

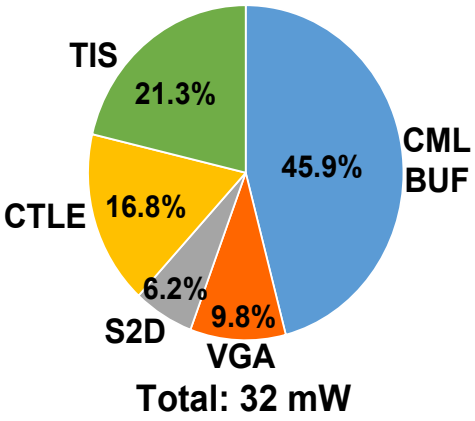


Figure 4.25. TIA power breakdown.

4.4.1 Frequency Domain Measurement

Four-port S-parameters measurements up to 50 GHz are performed using 67-GHz GSG and SGS probes and a Rohde & Schwarz vector network analyzer (VNA) with an input power of -40 dBm as shown in Figure 4.26. The input single-ended signal is sent through a GSG probe, and one output of SGS probe is connected to a 50-Ω load through a dc block. Measured and simulated S-parameters are shown and compared in Figure 4.27. Good matching between measurement and simulation results is observed. S11 is lower than -10 dB and S22 is lower than -6 dB up to 40 GHz. The measured S21 demonstrates a max. gain of 21.1 dB with a 3-dB BW of 30.5 GHz, and a min. gain of 12.1 dB with a BW of 33.5 GHz.

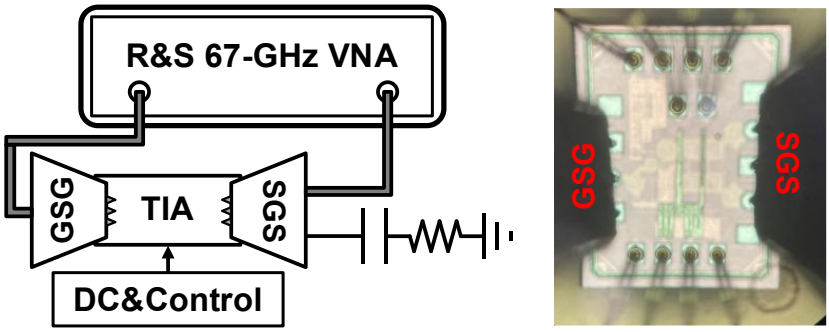


Figure 4.26. Frequency domain measurement setup.

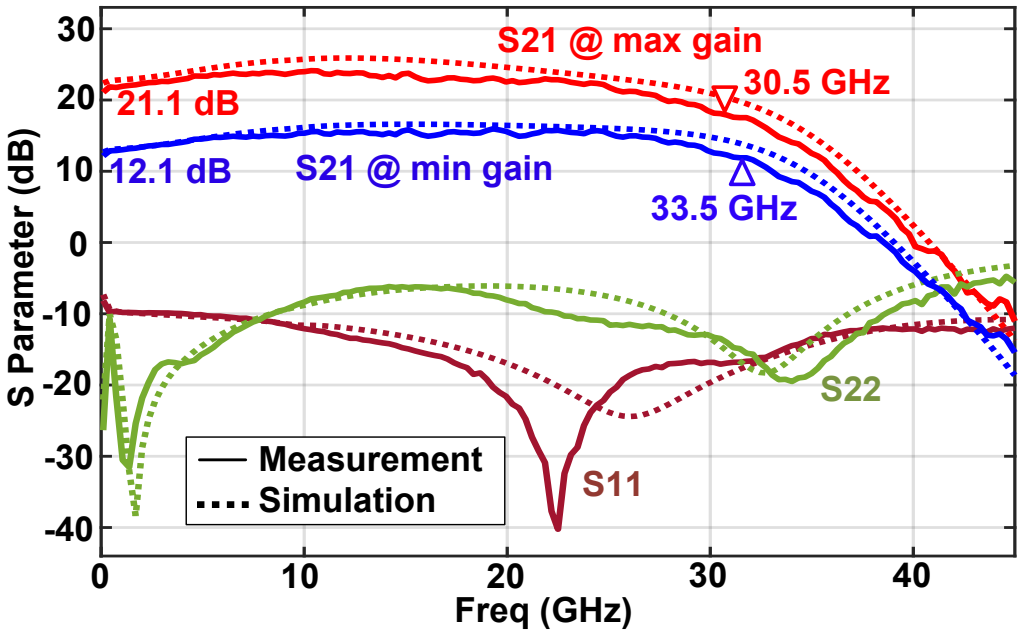


Figure 4.27. Measured and simulated S parameters of the TIA.

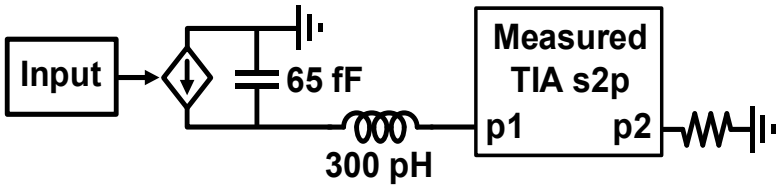


Figure 4.28. Test bench for evaluating transimpedance of the TIA with a PD.

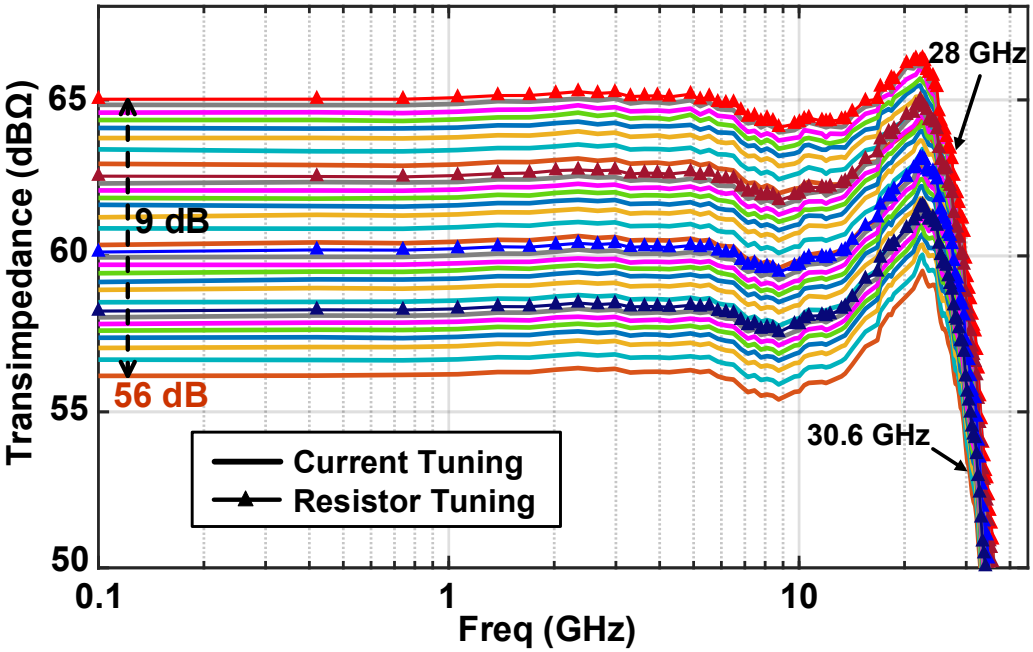


Figure 4.29. Measured transimpedance of the TIA across the whole dynamic range.

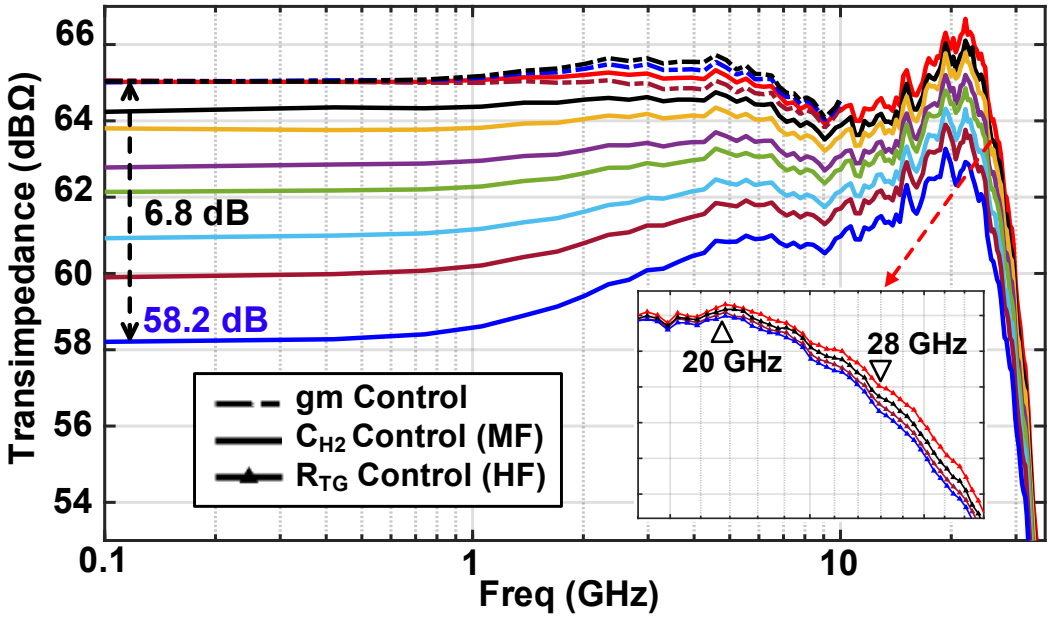


Figure 4.30. Measured CTLE responses with MF and HF tuning.

Figure 4.28 shows the test bench for evaluating the O/E performance of the TIA. By combining the measured S-parameter data, PD junction capacitance of 65 fF, and wire-bonding inductance of 300 pH, the transimpedance response of the TIA across gain control is plotted in Figure 4.29. The TIA achieves a max. gain of 65 dBΩ with a BW of 28 GHz, and a 9-dB control range with an average step size of 0.3 dB. The BW variation across the dynamic range through VGA control is less than 3 GHz. Figure 4.30 shows the measured CTLE frequency responses with a dc gain control range of 6.8 dB. Both MF tuning from 1-10 GHz by controlling C_{H2} and HF tuning at higher than 20 GHz by controlling R_{TG} are also demonstrated.

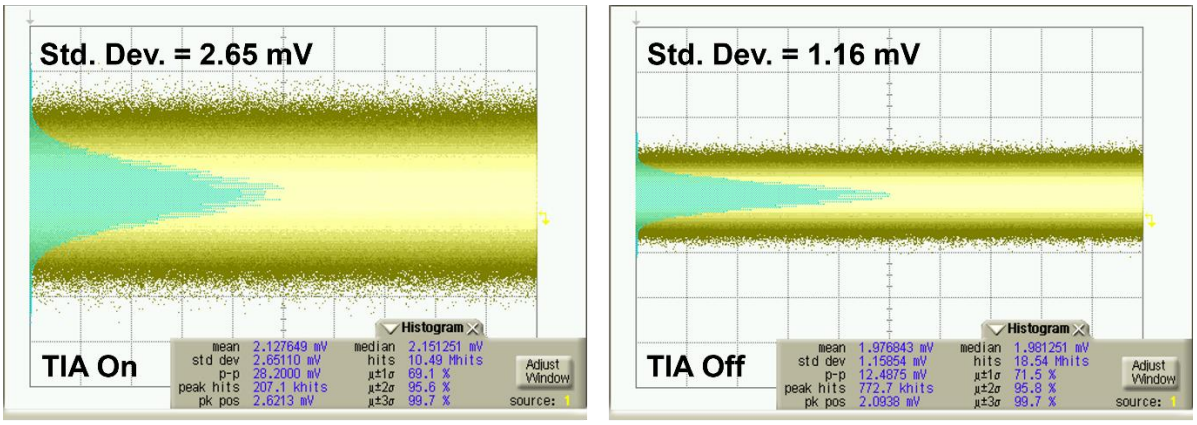
4.4.2 Noise Measurement

Figure 4.31 reports the measured single-ended output noise distribution when the TIA is on and off using a Keysight 80 GHz sampling oscilloscope. The integrated input-referred current noise of the TIA results in

$$i_{n,in(rms)} = \frac{2 \times \sqrt{(2.65\ mV)^2 - (1.16\ mV)^2}}{10^{\left(\frac{65\ dB}{20}\right)}} = 2.68\ \mu A_{rms} \qquad (4.7)$$

By de-embedding the 1.16 mV_{rms} noise from the oscilloscope, an output noise of 2.38 mV_{rms} and an input-referred current noise of 2.68 μA_{rms} are extracted. Equivalently, the average input-

referred current noise density is $2.68\ \mu A_{rms}/\sqrt{28\ GHz} = 16\ pA/\sqrt{Hz}$.



(a) (b)

Figure 4.31. Single-ended output voltage noise distribution measurements: (a) with the TIA on, and (b) with the TIA off.

4.4.3 THD Measurement

Single-ended total harmonic distortion (THD) is measured using a Rohde & Schwarz FSW-67 spectrum analyzer at 1-GHz fundamental frequency with 10 harmonics counted. Figure 4.32 shows the measured THD at maximum and minimum gain. With 5% THD, up to 280 μA_{pp} and 640 μA_{pp} of input current can be handled, corresponding to an output amplitude of 498 mV_{pp} and 404 mV_{pp}, respectively.

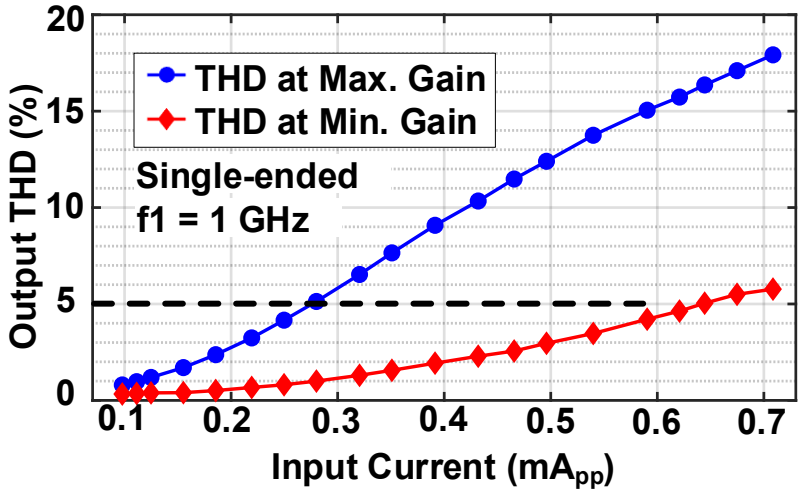


Figure 4.32. Measured single-ended output THD.

4.4.4 Time domain measurement

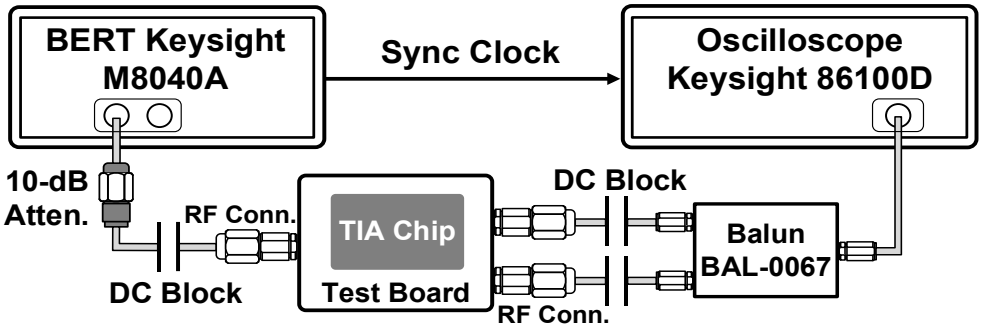


Figure 4.33. Time domain measurement setup.

Time domain measurements are performed using a 64 GBaud Keysight PAM-4 BERT as the data source with a 10-dB attenuator. As described in Section 4.3, the TIA is wire-bonded to a high-frequency PCB for testing. Since the oscilloscope used in the measurement only supports a single-ended input, as illustrated in Figure 4.33, the TIA differential output is first combined using a 67-GHz balun and then captured with the Keysight 80-GHz sampling oscilloscope. To compensate for the loss of RF connectors, dc blocks, cables, and PCB traces, a 3-tap FFE from the transmitter side (i.e., the BERT) is used. No equalization from the oscilloscope is applied, and over 10 kUI of PRBS-9 pattern is measured to generate eye diagrams.

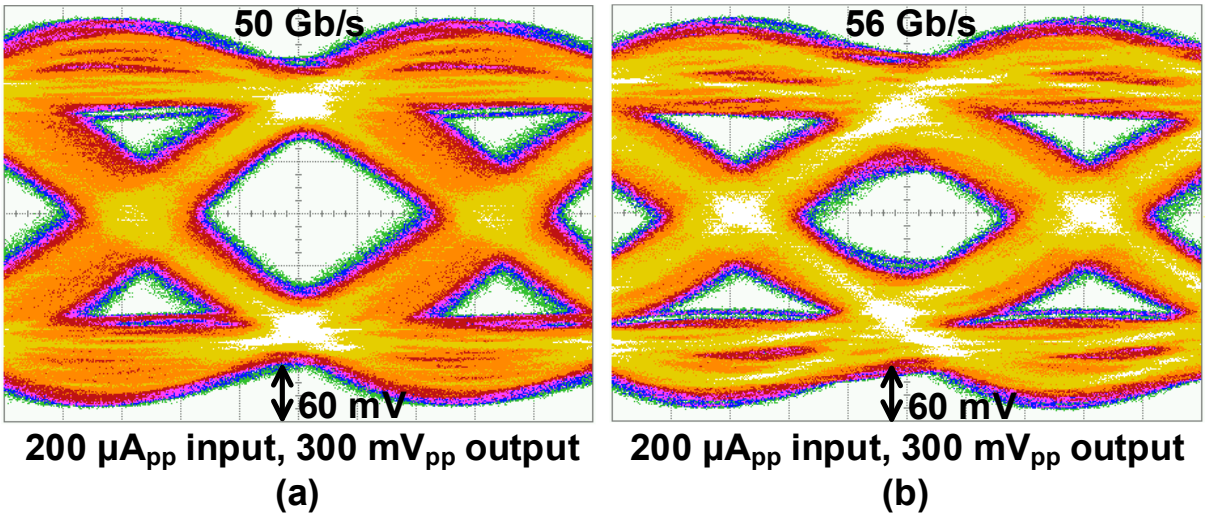


Figure 4.34. Measured eye diagrams of (a) 50 Gb/s and (b) 56 Gb/s, both with 200 uA_{pp} inputs and 300 mV_{pp} outputs.

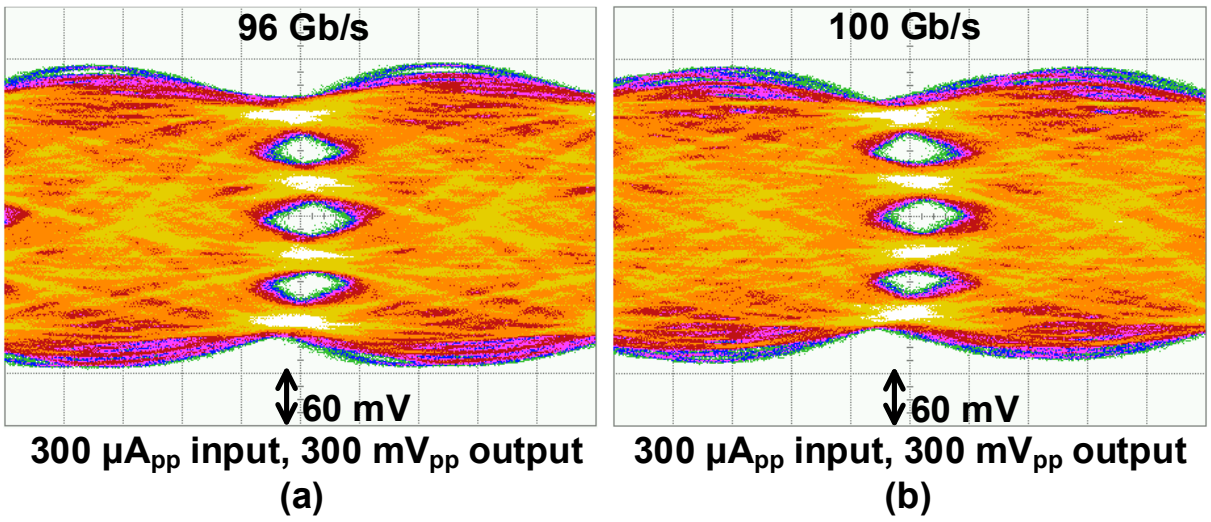


Figure 4.35. Measured eye diagrams of (a) 96 Gb/s and (b) 100 Gb/s, both with 200 uA_{pp} inputs and 300 mV_{pp} outputs.

The measured 50-Gb/s and 56-Gb/s NRZ eye diagrams with an input current of ~200 uA_{pp} are shown in Figure 4.34 (a) and (b), verifying the BW of the TIA. Figure 4.35 (a) and (b) show the 96-Gb/s and 100-Gb/s PAM-4 eye diagrams with an input current of ~300 uA_{pp}. The eyes are totally open at both data rates and the RLM at 96 Gb/s is better than that at 100 Gb/s. Figure 4.36 (a) and (b) show the 100-Gb/s PAM-4 eye diagrams with an input current of ~200 uA_{pp} and ~400 uA_{pp}, respectively, indicating good noise performance and linearity.

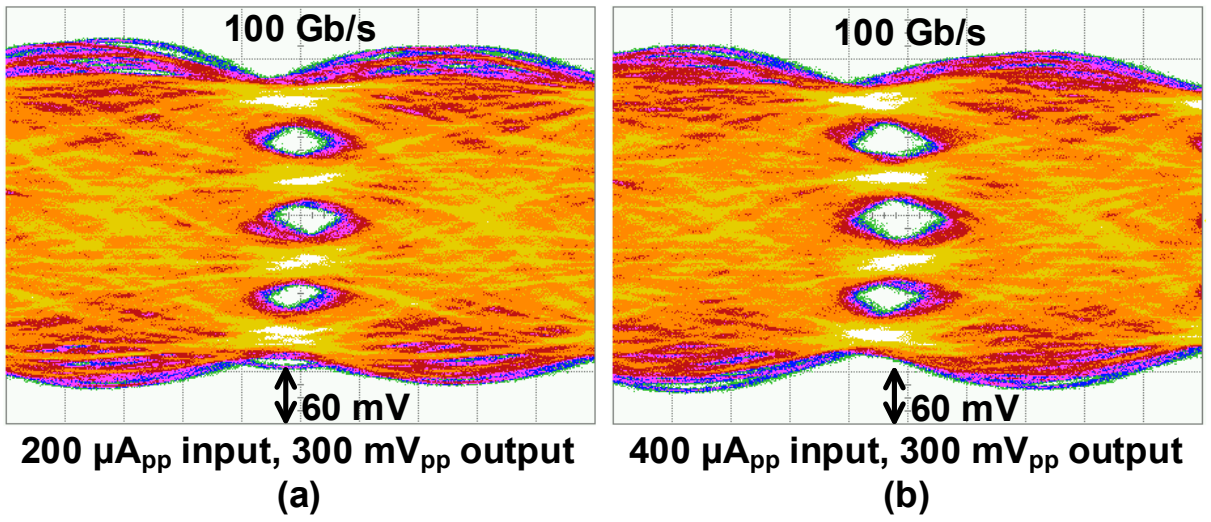


Figure 4.36. Measured eye diagrams of 100 Gb/s with (a) a 200 uA_{pp} input and (b) a 400 uA_{pp} input, both with 300 mV_{pp} outputs.

The BER with different input amplitudes of electrical signals is also measured using the BERT to estimate the optical input sensitivity. Assuming a PD with a responsivity of 0.75 A/W, the corresponding BER versus input OMA sensitivity can be accordingly plotted. Figure 4.37 shows the BER versus input OMA sensitivity with NRZ inputs at 56, 60, and 64 Gb/s for PRBS-9 input pattern. The TIA achieves an error free BER at 64 Gb/s with an input OMA sensitivity of -6.5 dBm, and at a lower data rate of 56 Gb/s, -8.8 dBm sensitivity can be achieved. Figure 4.38 shows the BER versus input OMA sensitivity with PAM-4 inputs at 92, 96, and 100 Gb/s for PRBS-9 input pattern. The TIA achieves a sensitivity of around -7.8 dBm at 100 Gb/s under the 2.4e-4 pre-FEC limit. When the input is increased to around -4 dBm, a BER of 1.5e-5 is achieved with a RLM of 0.89. At a lower data rate of 92 Gb/s, a BER of lower than 1e-6 can be achieved with -4 dBm input sensitivity.

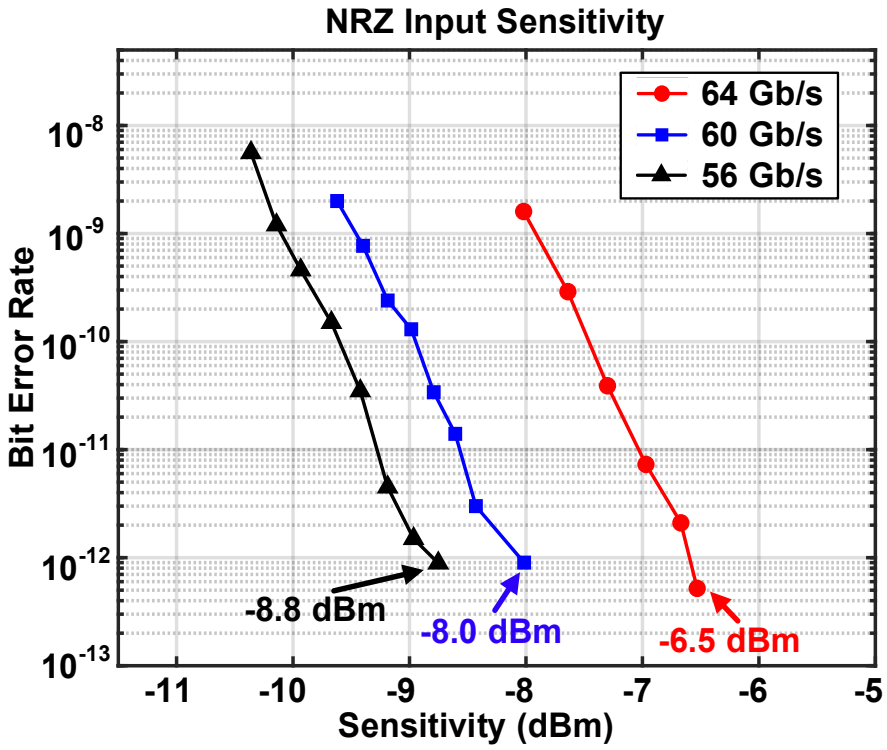


Figure 4.37. BER versus NRZ input OMA sensitivity based on the measured BER at different input amplitudes of electrical signals assuming a PD responsivity of 0.75 A/W.

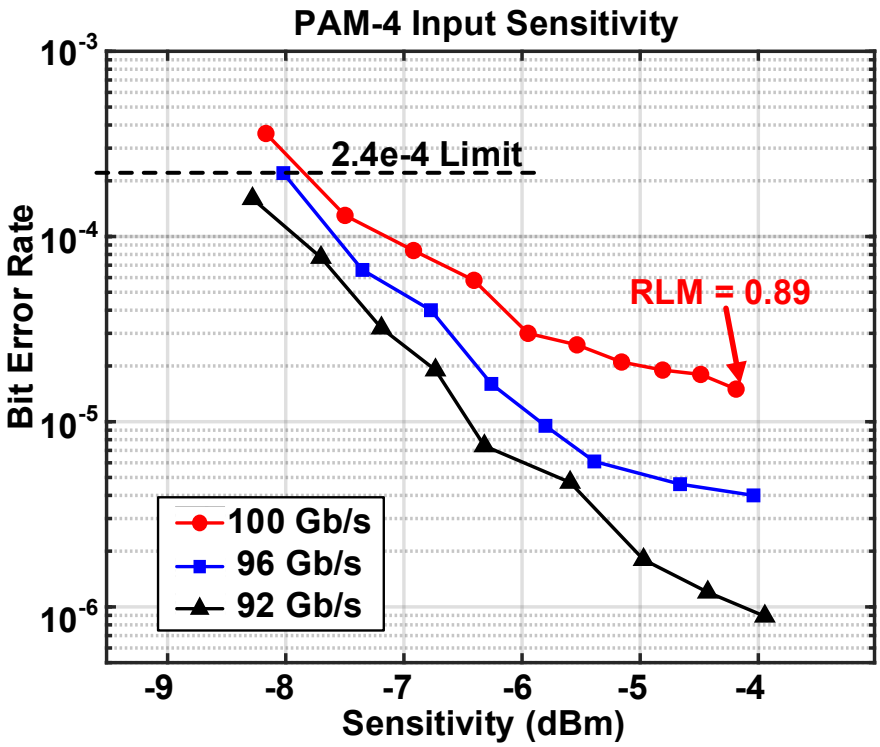


Figure 4.38. BER versus PAM-4 input OMA sensitivity based on the measured BER at different input amplitudes of electrical signals assuming a PD responsivity of 0.75 A/W.

TABLE 4.1

PERFORMANCE SUMMARY AND COMPARISON OF CMOS TIA

	ESSCIRC'18 [11]	JSSC'21 [31]	JSSC'23 [15]	VLSI'23 [55]	CICC'24 [48]	SSCL'24 [51]	This Work
Technology	28-nm CMOS	22-nm FinFET	16-nm FinFET	16-nm FinFET	22-nm FDSOI	28-nm CMOS	28-nm CMOS
Data Rate (Gb/s)	112**	128	112	90	106.25	85**	100**
Signaling	PAM-4	PAM-4	PAM-4	PAM-4	PAM-4	PAM-4	PAM-4
Gain (dBΩ)	65	59.3	65	65	74	65	65
BW (GHz)	60	45.5	32	25	28	24	28
PD Cap. (fF)	70	70	60	70	NA	NA	65
THD @ Input Current, Output Amplitude	<5%@ $1mA_{pp}$, N/A	<5%@ $330\mu A_{pp}$, $304mV_{pp}$	<8%@ $670\mu A_{pp}$, $336mV_{pp}$	<9%@ $600\mu A_{pp}$, N/A	<4%@ $2.46mA_{pp}$, $550mV_{pp}$	<1.77%@ $330\mu A_{pp}$, $660mV_{pp}$	<5%@ $640\mu A_{pp}$, $400mV_{pp}$
Noise ($pA/\sqrt{Hz}$)	19.3	12.6	16.9	13.4	11	10.4	16
Input/Output ESD	No	No	Yes (80f)	Yes	Yes	No	Yes (90f)
Power (mW)	107	11.2	77	29.2	155	56	32

Efficiency (pJ/b)	0.96	0.09	0.69	0.32	1.46	0.66	0.32
FoM* (Ω·GHz/mW)	997	3748	739	1522	905	762	1556

*FoM = $\frac{Gain(\Omega)\times BW_{3dB}(GHz)}{P_{dc}(mW)}$ **Electrical Measurement

Table 4.1 shows the performance summary and comparison with the state-of-the-art CMOS TIAs. Compared to prior TIAs in 28-nm bulk CMOS [11] and [51], this work achieves the best energy efficiency and FoM which is a comprehensive trade-off metric that balances the gain, BW, and power, despite incorporating ESD protection at both input and output. While reference [11] demonstrates the highest BW, this comes at the cost of prohibitively high power. Compared to other TIAs in the comparison table, this work maintains competitive noise, linearity, and BW performance, while particularly attaining superior power efficiency. Although design [31] shows the best performance in both energy efficiency and FoM, it omits the VGA and thus lacking gain adjustment capability, which also contributes to its relatively low linearity in the table. Furthermore, [31] employs a purely single-ended architecture, meaning a S2D circuit would still be required in practical implementations. By delivering TIA performance competitive to other CMOS designs at significantly reduced power levels, this work demonstrates the potential for energy-efficient low-cost CMOS 100-Gb/s+ optical receivers.

4.5 Conclusion

A 0.32-pJ/bit 100-Gb/s PAM-4 linear TIA in a 28-nm bulk CMOS is proposed and designed. Inverter-based TIS, CTLE and S2D circuits are implemented taking advantage of high-speed transistors and complementarity of deep sub-micron CMOS technologies. The TAS-TIS topology in VGA design provides larger gain-BW product compared to the CML topology avoiding the use of both passive and active inductors, and a combination of Gm and RF gain control provides a large tuning range and a small step size with small BW variation across the dynamic range. Multi-layer stacked network, inductors and T-coils further reduce parasitic capacitance and accommodate ESD diodes. The proposed TIA achieves a 3-dB BW of 28 GHz

with a maximum dc transimpedance gain of 65 dBΩ, and a 3-dB BW of 31 GHz with a minimum dc transimpedance gain of 56 dBΩ, dissipating only 32 mW.

Chapter 5

Conclusion and Future Work

5.1 Summary

This thesis focuses on the design of high-speed PAM-4 ORX front end and data path for short-reach data center applications, targeting CPO and LPO scenarios. Chapter 2 analyzes the noise and BW relationship of SF TIAs based on a second-order SF model. Based on the noise-BW model, SF TIA sensitivity enhancement by the CTLE, FFE, and DFE is modelled and analyzed at system level. A 48-Gb/s PAM-4 ORX data path and a 100-Gb/s PAM-4 optical TIA are reported in Chapter 3 and Chapter 4, respectively. In both designs, a TAS-TIS topology in advanced CMOS technologies is explored to replace conventional CML-based topologies.

For the 48-Gb/s PAM-4 ORX data path, the design focus is TIA BW and sensitivity enhancement of post-TIA equalization. To evaluate the performance of TAS-TIS topology and DFE and FFE integrated at PAM-4 sampler, CTLEs and passive inductors are totally avoided, resulting in a compact and low-power design. A Gilbert-TIS VGA is proposed to break the tradeoff between BW variation and dynamic range. A FFE is embedded in the half-rate structure, and slicers are optimized to achieve a low T_{CKQ}, which is vital to close the decision feedback loop and ensure correct data recovery. The ORX is fabricated in a 28-nm CMOS process and wire-bonded to a PD. Optical measurement results at 48-Gb/s PAM4 show the ORX achieves -5.1-dBm sensitivity at 2.4e-4 BER using 61.4 mW, with only 13.1 mW contributed from the TIA, resulting in 1.28-pJ/bit (0.27 pJ/bit for TIA only) efficiency.

For the 100-Gb/s PAM-4 TIA, the design focus is to relax the tradeoff in CMOS linear TIA design among BW, noise, and power while maintaining linearity. Taking advantage of high f_T and complementarity in deep sub-micron CMOS technologies, inverter-based circuits are implemented in most TIA stages. A current reuse VGA employing a TAS-TIS topology with high linearity is proposed to provide a large tuning range with a small tuning step size. Multi-layer stacked networks, T-coils and inductors achieve high inductance density to expand the BW in the existence of ESD diodes at both input and output. Implemented in a 28-nm CMOS

technology, the TIA achieves a BW of 28 GHz with a dc transimpedance gain of 65 dBΩ, while showing an input referred noise density of 16 pA/√Hz and a THD < 5% up to 640 μA_{pp} input current. The TIA dissipates only 32 mW, achieving a good energy efficiency of 0.32-pJ/bit.

5.2 Future Work

On the ORX side, design considerations for improving power efficiency, BW density and linearity are ever more important. Flip-chip co-packaged TIA and PD is becoming a promising solution to reduce parasitics and support high I/O density compared to traditional wire-bonding solutions [15]. The requirement of a large input dynamic range poses another challenge for TIA design [48]. TIA co-design with on-chip LDOs also shows the potential to further improve input sensitivity, not simply by improving the power supply rejection, but also by doubling the current from both terminals of a PD [56]. The Q-shaping approach applied to transformers may provide more peaking capability than tunable inductors. And finally, integrating the clock and data recovery (CDR) into a PAM-4 ORX data path has not been fully explored yet.

5.2.1 Linearity Enhancement for PAM-4 TIA Design

Using a large shunt feedback resistor R_F to improve noise focuses on the scenario where the optical input power is always weak enough. However, for scenarios where high input power (> 0 dBm) may also occur, the use of large R_F turns out to make TIA overload at high power levels. In this case, increasing the dynamic range of VGA does not help much since signal distortion happens right after the TIS at first stage as illustrated in Figure 5.1. In a word, the input signal of VGA is already nonlinear.

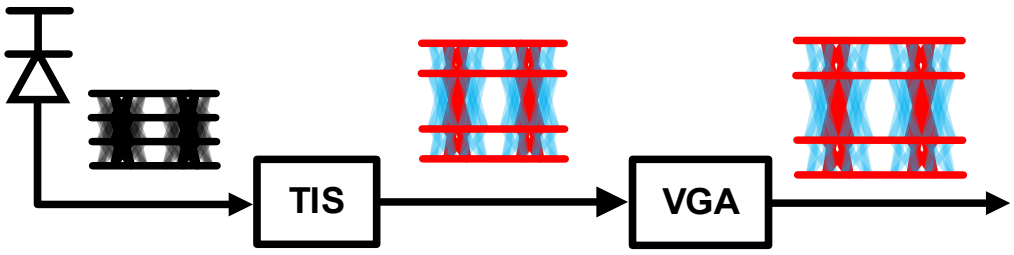


Figure 5.1. Illustration of signal distortion when TIA overloads.

In general, the overload current and sensitivity determines the upper and lower end of TIA

dynamic range, respectively. Considering a SF TIA, both quantities are related to the value of R_F, and therefore, if resistor R_F is adaptive to input signals, then the dynamic range can be extended. Previous works directly change the feedback resistor R_F using switches to solve this problem as shown in Figure 5.2 (a), which is unfavorable for the concern of stability and group delay variation. From Eq. (2.8c) and (2.9), if changing R_F while keeping A and ω_A fixed, both the quality factor Q as well as BW_{3dB} change. More specifically, when R_F is reduced, the open-loop low-frequency pole at $1/(R_F C_T)$ increases, which results in peaking under a fixed loop gain A, and a fixed open-loop high-frequency pole $1/\omega_A$. In reality, it would be challenging to satisfy all specifications for BW, group-delay variation, and peaking over a wide adaptation range [27].

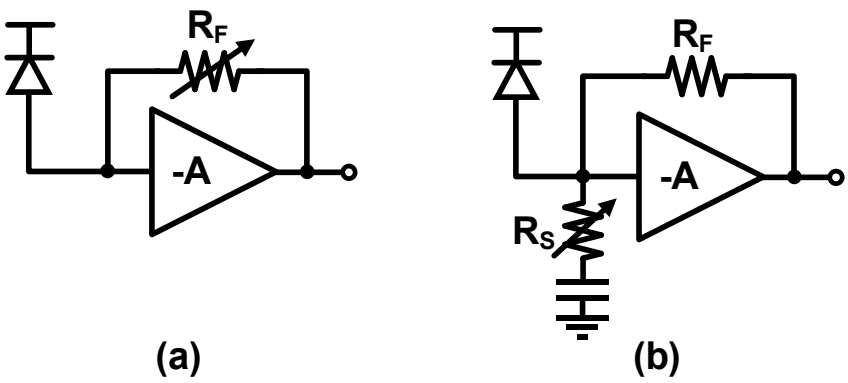


Figure 5.2. TIA with (a) a variable feedback resistor and (b) a variable input shunt resistor.

An alternative to the TIA with variable feedback resistor is the TIA with variable input shunt resistor, Rs, which is shown in Figure 5.2(b). The transimpedance now becomes

$$Z_T = \left(\frac{A}{A+1}\cdot R_F\right)//R_S$$
$$= \frac{A}{A+1+R_F/R_S}\cdot R_F \tag{5.1}$$

Varying the R_S only helps maintain stability and avoid peaking. When R_S is reduced, the open-loop pole at $1/[(R_F//R_S)C_T]$ increases, whereas the loop gain $AR_S/(R_S+R_F)$ decreases by the same amount, thus maintaining an approximately constant closed-loop response [27]. Recent work [48] has already implemented the overload control circuit by tuning

the input shunt resistor, which is realized by a dummy TIA, and more than 15-dB input OMA range has been achieved. In the future, more emphasis should be placed on the R_S control circuits to enlarge the input dynamic range with low power consumption.

Another linearity constraint comes from the output buffer. In Chapter 4, all the circuits are implemented with CMOS input pairs except the output buffer, which is NMOS input, and it becomes the limitation of the overall linearity performance especially considering the large amplitude at buffer input. Besides CML buffers, two kinds of buffers are used in previous works: a SF amplifier [11] and an inverter-based buffer [31], [51]. However, for the SF amplifier, BW limitation may need multiple series and shunt peaking inductors, and for the inverter-based buffer, a large Gm is necessary, resulting in high power consumption. Pseudo-differential structures and impedance matching to 50 Ω in both buffers also affect signal integrities. A TAS-TIS topology can be a good candidate for buffer design due to its high gain-BW product, differential operation, and CMOS-pair availability, as already been described in Chapter 3 and 4. By optimizing the output buffer with new topologies, TIA linearity can be further enhanced.

5.2.2 Transformer-Based Q Shaping

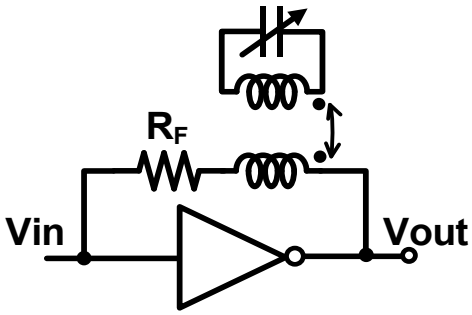


Figure 5.3. Transformer-based Q shaping by modulating the varactor on the secondary side.

Chapter 4 reports a simple implementation of an inductor-based Q-shaping approach to adjust high-frequency peaking, compensating for the peaking variation. However, it only provides relatively narrowband peaking, and the tuning range is restricted by the Q of inductors. Transformer-based Q shaping approaches can be more effective in the tuning range and peaking frequency. As reported in [53], to boost the signal close to 56 GHz without consuming excessive power, a CTLE resorts to passive gain in the form of series peaking by coupling the signal to

the inputs of the subsequent stage through a transformer. This forms a conjugate complex pole pair with the resonant frequency determined by the inductance of the transformer L, the input capacitance of the next stage C_{IN}, and the resonator quality factor Q. High-frequency peaking gain can be controlled by tuning the Q of the transformer leading to an effective peaking adjustment.

Another approach is to integrate the transformer in series with a SF amplifier as shown in Figure 5.3. The Q of the transformer is adjustable by modulating the varactor on the secondary side. This Q shaping approach, in contrast to the conventional inductor in parallel with transmission gates or MOSFETs, provides a higher Q for the transformer, thereby enhancing its peaking capability.

Appendix A

Inverter-based Active Inductor Impedance

The circuits in Figure A.1 (a) and (b) are equivalent to the loading of the previous stage. Its corresponding small signal equivalent circuit is depicted in Figure A.2, and after applying a test voltage at V_{load}, according to Kirchhoff's current law, the current it is given by

$$i_t = \frac{v_t - v_g}{R_F} + G_m v_g + \frac{v_t}{r_o} \tag{A.1}$$

$$v_g = v_t \frac{1}{1 + sRC_{gs}} \tag{A.2}$$

where R_F is the shunt feedback resistor, G_m is the transconductance of inverter, r_o is the output resistance of inverter, and C_{gs} is the total capacitance between gate and source of input MOSFETs.

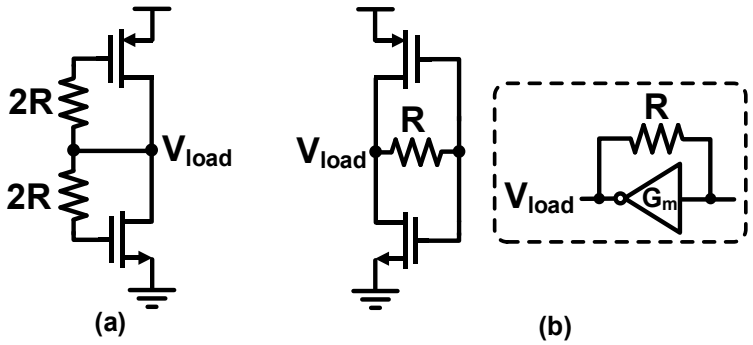


Figure A.1. Inverter-based active inductor circuits.

Substituting Eq. (A.2) into Eq. (A.1) gives the expression for i_t

$$i_t = \frac{v_t}{R_F} + \frac{G_m R_F - 1}{R_F} \frac{v_t}{1 + sR_F C_{gs}} + \frac{v_t}{r_o}$$

$$= v_t \frac{1 + G_m r_o + sr_o C_{gs} + sR_F C_{gs}}{(1 + sR_F C_{gs}) r_o} \tag{A.3}$$

The impedance of the active inductor is derived to be

$$Z_L = \frac{v_t}{i_t} = \frac{1 + sR_F C_{gs}}{G_m + sC_{gs}\left(1 + \frac{R_F}{r_o}\right) + \frac{1}{r_o}} \tag{A.4}$$

If assuming a large enough output resistance r_o, then Z_L can be simplified to

$$Z_L \approx \frac{1 + sR_F C_{gs}}{G_m + sC_{gs}} = \frac{1}{G_m}\frac{1 + sR_F C_{gs}}{1 + sC_{gs}/G_m} \tag{A.5}$$

If the interest of frequency is much lower than G_m/C_{gs}, then Z_L can be simplified to

$$Z_L \approx \frac{1}{G_m} + \frac{sRC_{gs}}{G_m} \tag{A.6}$$

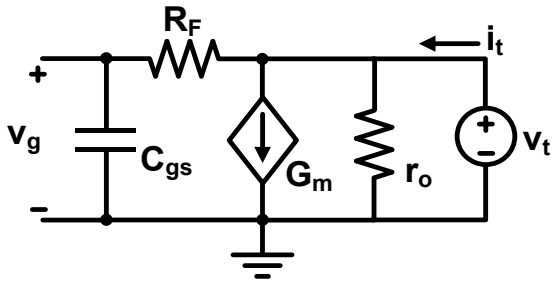


Figure A.2. Test voltage for input impedance of the inverter-based active inductor.

Appendix B

Cherry-Hooper Amplifier Input and Output Resistance

The small-signal resistance seen at nodes X and Y of the Cherry-Hooper amplifier described in Chapter 4 (Figure 4.5) is derived here. For input resistance, a test voltage source v_t is added at the gate of M_2 as shown in Figure B.1, and the corresponding current is given by

$$i_t = g_{m2}v_t + \frac{v_t - i_t R_F}{r_o} \tag{B.1}$$

$$Z_{in} = \frac{v_t}{i_t} = \frac{1 + \frac{R_F}{r_o}}{\frac{1}{r_o} + g_{m2}} \tag{B.2}$$

where g_{m2} is the transconductance of M_2, R_F is the feedback resistor, and r_o is the output resistance of M_2. Assume a large enough output resistance r_o, and Z_{in} can be simplified to

$$Z_{in} \approx \frac{1}{g_{m2}} \tag{B.3}$$

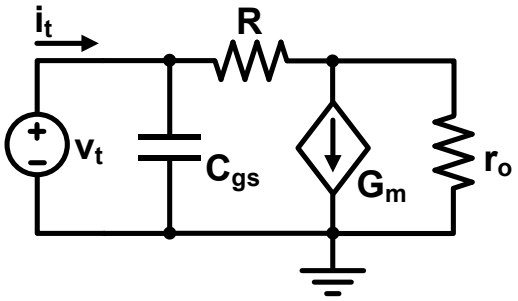


Figure B.1. Test voltage for input resistance of the Cherry-Hooper amplifier.

For output resistance, a test voltage source is added at the output of the amplifier and the input is connected to ground as shown in Figure B.2. The test current i_t is given by

$$i_t = g_{m2}v_t + \frac{v_t}{R_F} + \frac{v_t}{r_o} \tag{B.4}$$

$$Z_{out} = \frac{v_t}{i_t} = \frac{1}{\frac{1}{r_o} + \frac{1}{R_F} + g_{m2}} \tag{B.5}$$

Similarly, Z_{in} can be simplified assuming a large enough output resistance r_o, which is

$$Z_{out} \approx \frac{1}{g_{m2}} \tag{B.6}$$

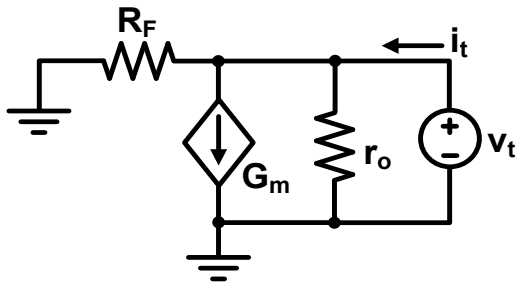


Figure B.2. Test voltage for output resistance of the Cherry-Hooper amplifier.

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